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SINE SYNTHESISED UPS

PROJECT REPORT

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CERTIFICATE

This is to certify that the project report entitled

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Is the bonafide work done by

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For Bright Electro Control Equipments (P) Ltd

N. Shanmugam

Managing Director

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DEDICATED TO OUR BELOVED

PARENTS AND TEACHERS

ABSTRACT

III.EXECUTIVE ABSTRACT

The Microcontroller based UPS system has been developed to provide continuous high quality sine wave power supply to vulnerable electronic equipments.

In normal UPS, square wave is generated. But the sine wave can be generated using analog discrete components. Use of this may lead to increased cost and size.

Using Microcontroller, the sine wave can be generated by employing high frequency switching. Apart from this Microcontroller can be integrated to control some important parameters such as inverter control, low voltage control, over voltage control and short circuit voltage protection etc... Thus the size and cost can be reduced.

Here real time sampling can be done, so that the efficiency of the system can be improved. The sine wave generated in each cycle can be divided in to steps of 15 i.e., seven in the positive half and seven in the negative half. The voltage obtained at each step is compared to that of reference value, the error obtained is corrected in the next step of the same cycle.

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INTRODUCTION

1. INTRODUCTION

At times, power from a wall socket is neither clean nor uninterruptible. Many abnormalities such as blackouts, brownouts, spikes, surges, and noise can occur. Under the best conditions, power interruptions can be inconveniences. At their worst, they can cause loss of data in computer systems or damage to electronic equipment. It is the function of an uninterruptible power supply (UPS) to act as a buffer and provide clean, reliable power to vulnerable electronic equipment. The basic concept of a UPS is to store energy during normal operation (through battery charging) and release energy (through DC to AC conversion) during power failure.

1.1 LITERATURE SURVEY:

In the present scenario, the offline UPS gives square wave as output. In a square wave inverter, peak voltage equals RMS voltage and varies directly with battery voltage. Therefore, when the battery voltage is low, the peak AC output voltage and RMS voltage are also low. This type of inverter has high harmonic distortion (50%) and marginal efficiency (60% to 80%). A square wave inverter often cannot properly power electronic equipment and motors tend to run hotter. Surge capability ranges from poor to good depending upon other design features. For high frequency switching it is not applicable.

Modified sine wave is an attempt to approximate sine wave rectangular or trapezoidal pulses that are easier to generate efficiency with low cost inverter. It can be used to operate only one dedicated load. Equipments with high quality internal power supplies is less sensitive to sharp using edge of modified sine wave. The inrush current and the stress on the output devices of the inverter are not reduced. Extra harmonic distortion is generated. Therefore the generation of sine wave is an important criterion for the industrial applications.

1.2 MICROCONTROLLER BASED UPS:

By using a microcontroller, the design can be greatly simplified. That is, the functions of the DC offset amp, error amp and PWM drive can be implemented in software. Therefore, modifications to the design are made through code changes, not component changes. In addition, there is no need to generate an external sine wave reference; this is embedded in the microcontroller.

The high performance of the Harvard architecture gives the user the throughput needed for high quality sine wave generation. The single-cycle multiply means faster program execution and response to waveform changes. Only 8 bits of the 10-bit PWM is needed to resolve a high quality output waveform. In addition, microcontroller enables the customer to add further enhancements through software changes (flexibility).

The output voltage and current will be monitored by the microcontroller to make adjustments "real-time" to correct for error and load changes.

The microcontroller controls all module synchronization as well as inverter control and feedback. All internal module synchronization is handled by the microcontroller.

The control algorithms and software are written in C for maintainability and transportability.

1.3 OBJECTIVES AND SCOPE OF WORK:

- The main objective of this work is to generate sine wave in the UPS.
- It can be employed to indicate the upper cut off and lower cut off range.
- Can be used to indicate the battery level.
- The efficiency has to be increased and it can be achieved in our work
- Compactness and reliability plays an important role which is satisfied
- The micro controller controls all module synchronization as well as inverter control and feedback.

AN OVERVIEW OF UPS

2. AN OVERVIEW OF UPS

For continuous power supply, for critical loads, even in the event of commercial power failure for a considerable period UPS is only the solution. A proper UPS can provide good quality power to the load at all conditions of supply power. Uninterruptible power supplies (UPS) are designed to protect electronic equipment like computers and phone systems against problems stemming from a temporary failure in the power supply. By providing a constant source of electricity, a UPS can help prevent damage or data loss that can occur with the unexpected shutdown of computers, phone systems, and other sensitive equipment.

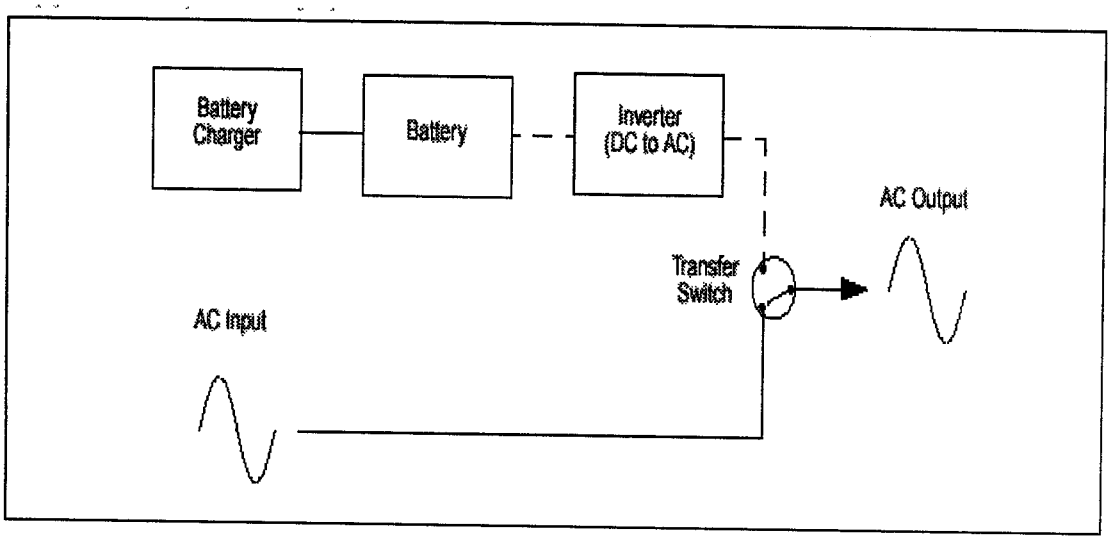
UPS systems work by detecting decreases in the amount of electricity coming from the wall circuit, and boosting power to maintain a constant flow of electricity to connected equipment. This power boost is provided either by a transformer that enhances a weak electrical flow, or from an internal battery that substitutes for the normal source in the event of failure.

All UPS systems are not alike. There are three basic types of UPS available.

2.1 TYPES OF UPS:

- Online UPS
- Offline UPS
- Line interactive

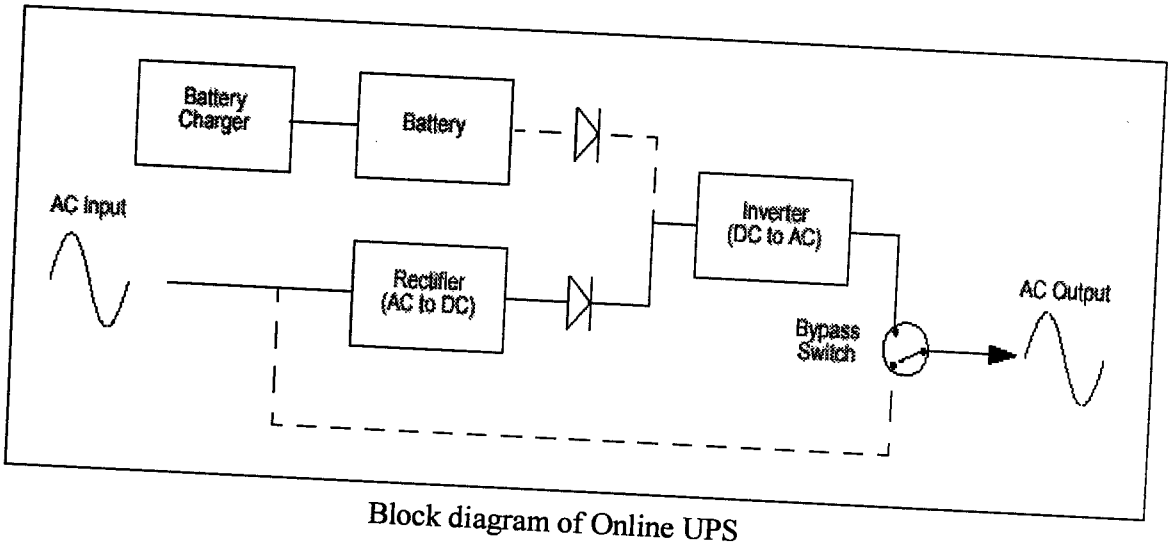
2.1.1 OFFLINE UPS:



Block diagram of Offline UPS

The first topology is known as off-line or standby, meaning that the inverter is normally off-line. A block diagram of an off-line UPS is shown in Figure . (The solid line represents the primary power path and the dashed line represents the secondary or back-up power path.) In normal operation, the output power comes from the input power source. This implies that there is a transfer time in switching the inverter on-line during a power interruption. If this transfer time is too great, there will be a less than smooth transition for the load on the UPS. This could lead to the same problems that the UPS was designed to avoid. The advantage of this topology lies in the fact that the stress on the inverter is decreased due to the inverter being turned off during normal operation. However, since the inverter only runs during power interruptions, this feature lends itself to latent failures when back-up power is needed the most.

2.1.2 ONLINE UPS:



Block diagram of Online UPS

The other major topology is the on-line or true UPS. As the name implies, the inverter is always on-line. A block diagram of the on-line UPS is shown in Figure. At start-up the UPS is in bypass mode until the inverter is running and synchronized with the input power source. Control is then transferred to the inverter. The inverter remains on-line during normal operation and during power failure operation until the battery is exhausted. During an inverter failure, the power is switched back to primary power through the bypass switch. This allows for the failed condition to be corrected while AC input power is still good. The one drawback to the on-line topology is that the inverter is always on-line. This would imply that the "life" of this topology would be shorter than an off-line UPS. However, the life of a UPS in practice has more to do with the robustness of the design than the topology used. The topology used for this reference design is the true (on-line) UPS.

2.1.3 LINE-INTERACTIVE:

The equipment is normally fed through the reserve power supply so that the equipment will not experience a momentary interruption when the normal power is lost. Since this type of UPS is continuously in-line, it often provides additional power conditioning and protection. First, at the same time the rectifier is converting the incoming AC power to DC, many UPS's will also clamp any surges or over voltages present on the incoming power. Second, by feeding the rectified DC signal through the battery prior to converting it back to AC for use by the protected equipment, any voltage sags are eliminated because the output voltage level is stabilized by the battery.

During a power outage, the protected equipment is supplied from the battery through the inverter. This type of system is a true uninterruptible power supply since the protected equipment will not experience a momentary interruption during a power outage. Line interactive UPS systems add a transformer to minimize the need to use an internal battery with every power fluctuation. These units monitor the line voltage at all times, activating the power transformer when the voltage falls below certain parameters. The battery is activated when even lower voltages are recorded.

2.2 OFF-LINE UPS PREFERRED SYSTEMS:

This system includes a storage battery, a battery charger, a static inverter and a static automatic change-over switch. In this system the power is normally passed directly to the load via the static switch S1 while S2 is off the battery charger is a stabilized one which maintains the battery on float at fully charged condition and at the same time provides stabilized power to the inverter. So long the utility supply is present the load is supplied by it and the inverter runs on no load. The inverter is phase synchronized with utility supply.

In case of utility power failure the load is transferred to the inverter power through static switch S2. At this condition the inverter runs from the is capable to supply the total demand of power. The total transfer operation should be complete within ¼ cycles so that the operation of critical equipment is not disturbed.

During the outage period the battery has to supply full load and discharges quickly. The back-up time depends upon the ampere-hour capacity of the battery. The battery should be shed off the load when it discharges to a minimum voltage recommended by the manufacturer.

After the restoration of supply power, the load is transferred to the line through S1 and S2 is switched off. The battery charger now charges the battery in constant current mode during which the battery voltage rises slowly. After the battery reaches the specified voltage, the charging mode automatically changes from constant current mode to constant voltage mode and begins boost charging so that the battery gets fully charged.

This system can not provide complete power protection and mode of operation has to be changed on power failure, so its application is restricted to small systems where the operation is not highly critical.

In this type of UPS, the primary power source is line power from the utility, and the secondary power source is the battery. It is called a standby UPS because the battery and inverter are normally not supplying power to the equipment. The battery charger is using line power to charge the battery, and the battery and inverter are waiting "on stand by" until they are needed. When the AC power goes out, the transfer switch changes to the secondary power source. When line power is restored, the UPS switches back.

While the least desirable type of UPS, a standby unit is still a UPS and will serve well for most users. After all, if standby UPSes didn't work, they wouldn't sell. For a very critical function, however, such as an important server, they are not generally used.

The issue with a standby UPS is that when the line power goes out, the switch to battery power happens very quickly, but not instantly. There is a delay of a fraction of a second while the switch occurs, which is called the switch time or transfer time of the UPS. While rare, it is possible for the UPS not to make the switch fast enough for the PC's power supply to continue operation uninterrupted. Again, in practice this does not normally occur or nobody would bother to buy these units. Still, we should compare the unit's transfer time to the hold time of our power supply unit, which tells us how much time the power supply can handle having its input cut off before being interrupted. If the transfer time is much less than the hold time, the UPS will probably work for us. Standby UPSes are usually available in a size range of up to about 1000VA.

PIC MICROCONTROLLER

3. PIC MICROCONTROLLER

PIC:

PERIPHERAL INTERFACE CONTROLLER

3.1 IMPORTANCE OF PIC:

- PIC is a very popular micro controller worldwide.
- Micro chip is the first manufacturer of 8 pin RISC MCU.
- Variety of end-user Application-specific standard products (ASSP) & Application - specific
- Global network of manufacturing and customer support facilities.
- PIC micro devices have following architectural features to attain the high performance:

  Harvard architecture

  Long word instructions

  Single word instructions

  Single cycle instructions

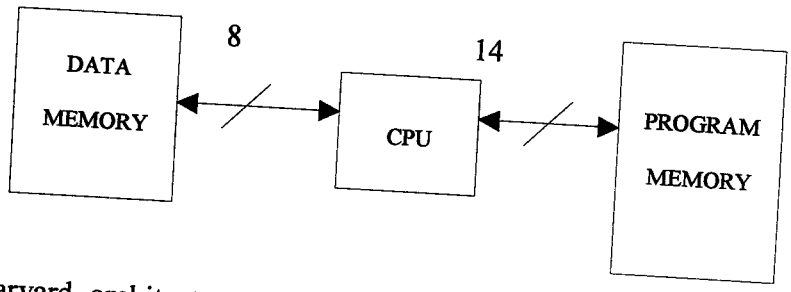
  Instruction pipelining

  Reduced instruction set

  Register file architecture

  Orthogonal (symmetric) instructions.

3.1.1 HARVARD ARCHITECTURE:



Harvard architecture has the program memory and data memory as separate memories and they are accessed from separate buses. This improves bandwidth over traditional Von-Neumann architecture in which program and data are fetched from the same memory using the same bus. With the Harvard architecture, the instruction is fetched in a single instruction cycle (all 14-bits).

3.1.2 LONG WORD INSTRUCTIONS:

Long word instructions have a wider (more bits) instruction bus than the 8-bit data memory bus. This is possible because the two buses are separate.This further allows instructions to be sized differently than the 8-bit wide data word which allows a more efficient use of the program memory, since the program memory width is optimized to the architectural requirements.

3.1.3 SINGLE WORD INSTRUCTIONS:

Single word instruction opcodes are 14-bits wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. With single word instructions, the number of words of program memory locations equals the number of instructions for the device. This means that all locations are valid instructions.

3.1.4 SINGLE CYCLE INSTRUCTIONS:

With the program memory bus being 14-bits wide, the entire instruction is fetched in a single machine cycle (TCY). The instruction contains all the information required and is executed in a single cycle. There may be a one-cycle delay in execution if the result of the instruction modified the contents of the program counter. This requires the pipeline to be flushed and a new instruction to be fetched.

3.1.5 REDUCED INSTRUCTION SET:

When an instruction set is well designed and highly orthogonal (symmetric), fewer instructions are required to perform all needed tasks. With fewer instructions, the whole set can be more rapidly learned.

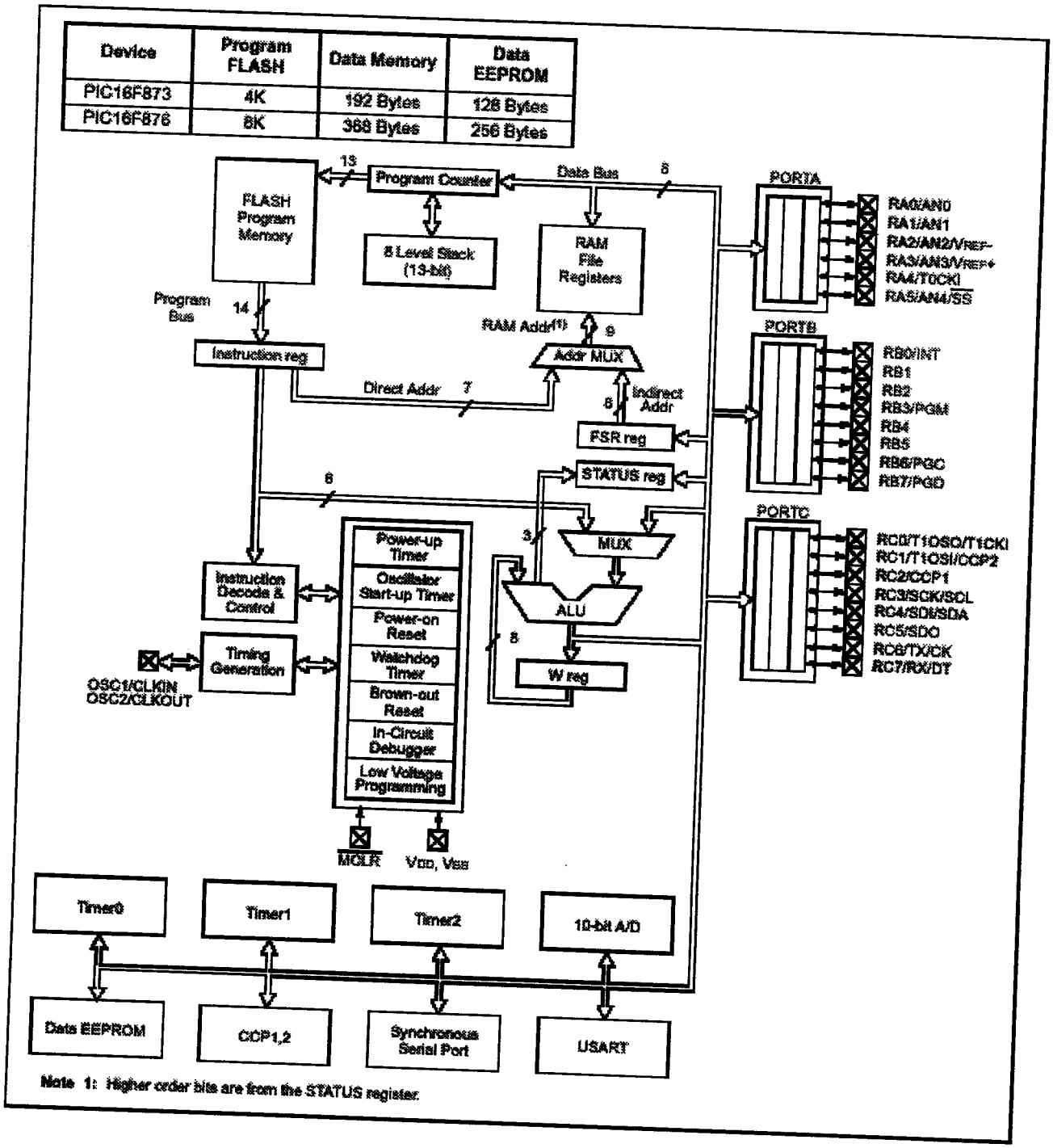
3.1.6 REGISTER FILE ARCHITECTURE:

The register files/data memory can be directly or indirectly accessed. All special function registers, including the program counter, are mapped in the data memory.

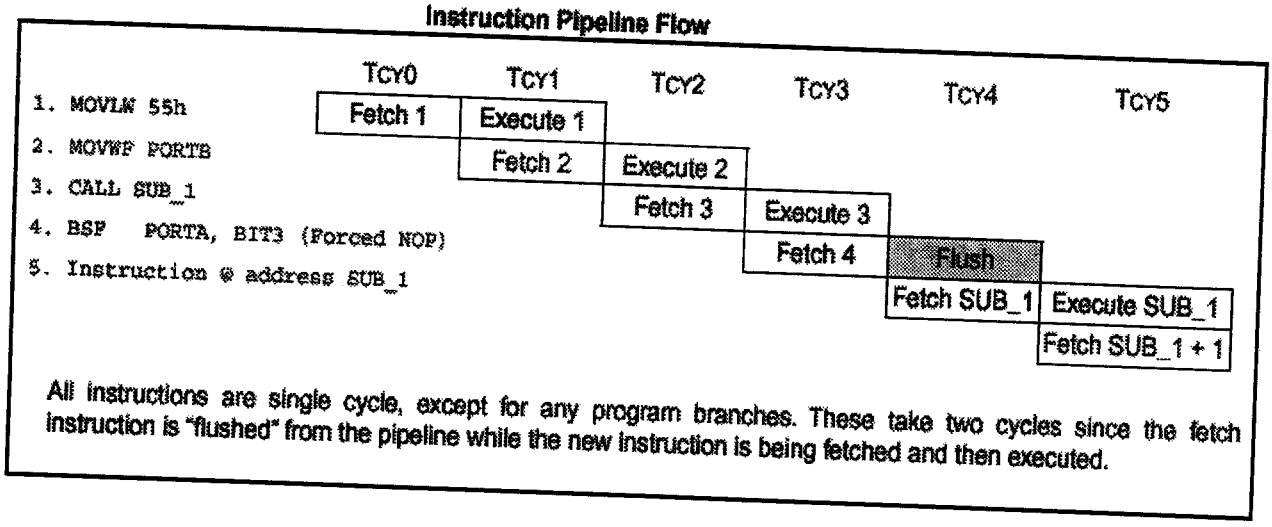
3.1.7 ORTHOGONAL (SYMMETRIC) INSTRUCTIONS:

Orthogonal instructions make it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of "special instructions" make programming simple yet efficient.

3.2 ARCHITECTURE OF PIC



3.3 INSTRUCTION PIPELINING:



An "instruction cycle" consists of four Q cycles (Q1, Q2, Q3 and Q4). Fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g.GOTO) then an extra cycle is required to complete the instruction. The instruction fetch begins with the program counter incrementing inQ1.This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written During Q4 (destination write)

- TCY1-the first instruction executes while the second instruction is fetched.
- TCY2- the second instruction executes while the third instruction is fetched.
- TCY3- the fourth instruction is fetched while the third instruction CALL SUB_1) is executed.

When the third instruction completes execution, the CPU forces the address of instruction four onto the stack and then changes the program counter (PC) to the address of SUB_1. This means that the instruction that was fetched during TCY3 needs to be "flushed" from the pipeline. During TCY4, instruction four is flushed (executed as a NOP) and the instruction at

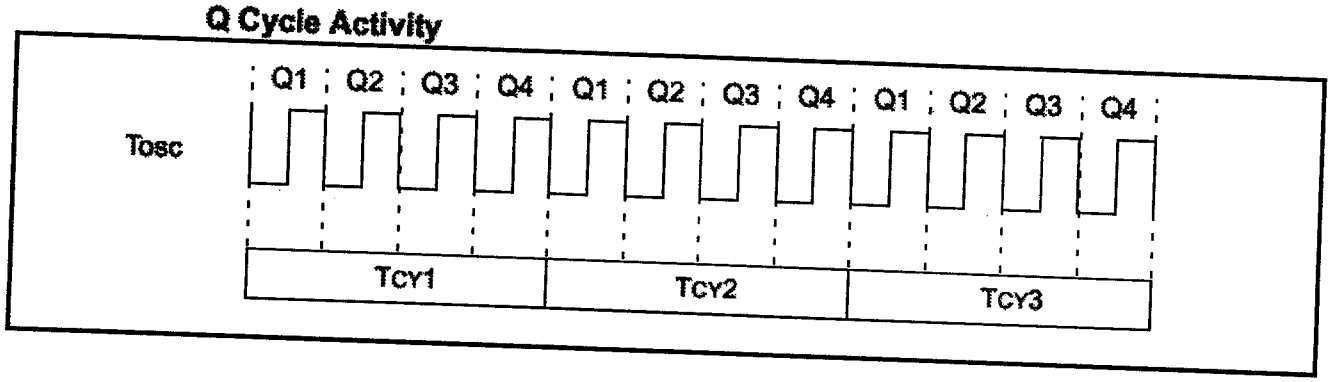
Address SUB_1 is fetched. Finally during TCY5, instruction five is executed and the instruction at address SUB_1+1 is fetched.

3.4 CENTRAL PROCESSING UNIT:

The CPU can be thought of as the "brains "of the device. The central processing unit is responsible for using the information in the program memory (instructions) to control the operation of the device. The CPU sometimes works in conjunction with the ALU to complete the execution of the instruction (in arithmetic and logical operations). The CPU controls the program memory address bus, the data memory

address bus, and accesses to the stack.

3.5 INSTRUCTION CLOCK:



Each instruction cycle (TCY) is comprised of four Q cycles (Q1-Q4). The Q cycle time is the same as the device oscillator cycle time (Tosc). The Q cycles provide the

timing/designation for the decode, read, process Data, Write, etc., of each instruction cycle. The following diagram shows the relationship of the Q cycles to the instruction cycle.

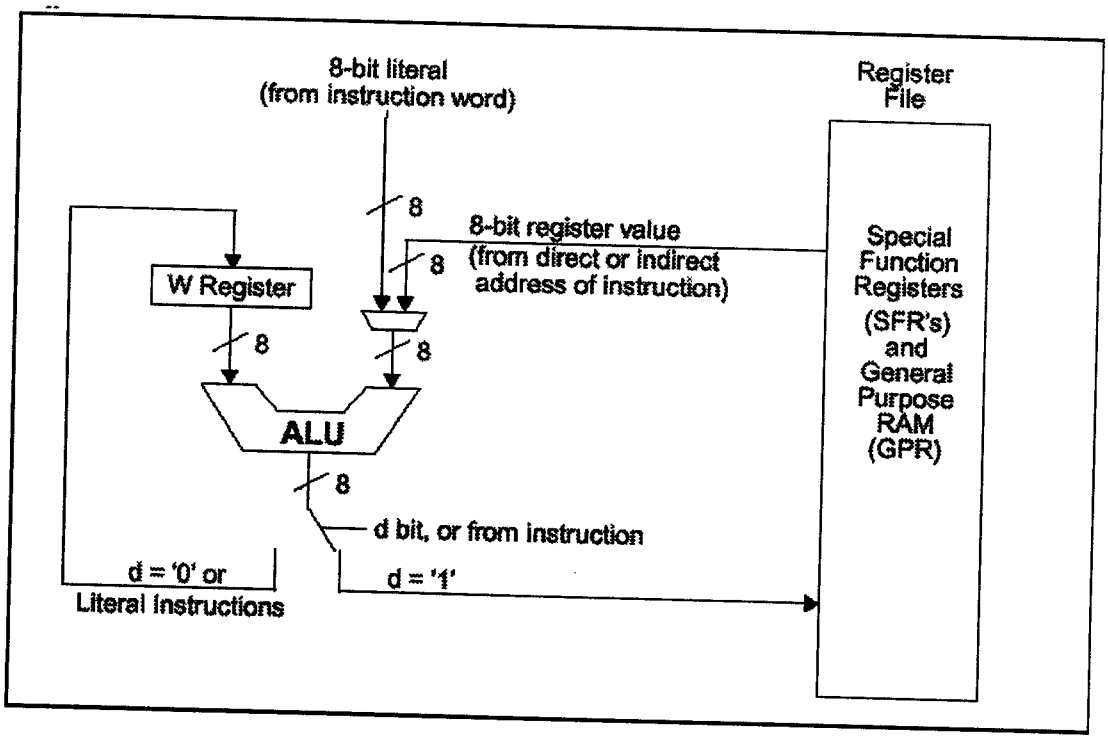
Q1: Instruction Decode Cycle or forced No operation.

Q2: Instruction Read Data Cycle or No operation

Q3: Process the Data.

Q4: Instruction Write Data Cycle or No operation.

3.6 ARITHMETIC AND LOGIC UNIT (ALU):



PIC micro MCU contains an 8-bit ALU and an 8-bit working register. The ALU is a general-purpose arithmetic and logical unit. In two-operand instructions, typically one operand is the working register (W register). The other operand is a file register or an immediate constant.

3.7 STATUS REGISTER:

The STATUS register contains the arithmetic status of the ALU, the RESET status And the bank select bits for data memory. Since this register controls the selection of the Data Memory banks, it is required to be present in every bank. Also, this register is in the same relative position (offset) in each bank.

The STATUS register can be the destination for any instruction, as with any other Register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic.

STATUS REGISTER

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	TO	PD	Z	D	CC
bit 7							bit 0

Bit 7 **IRP:** Register Bank Select bit (used for indirect addressing)

1 = Bank 2, 3 (100h - 1FFh)

0 = Bank 0, 1 (00h - FFh)

Bit 6-5 **RP1:RP**0: Register Bank Select bits (used for direct addressing)

11 = Bank 3 (180h - 1FFh)
10 = Bank 2 (100h - 17Fh)
01 = Bank 1 (80h - FFh)
00 = Bank 0 (00h - 7Fh)
Each bank is 128 bytes

Bit 4 **TO**: Time-out bit

1 = After power-up, CLRWDT instruction, or SLEEP instruction
0 = A WDT time-out occurred

Bit 3 **PD**: Power-down bit

1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

Bit 2 **Z**: Zero bit

1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

Bit 1 **DC**: Digit carry/borrow bit

1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result

Bit 0 C: Carry/borrow bit

1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note: For borrow, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high, or low order bit of the source register.

3.8 MEMORY ORGANIZATION:

There are two memory blocks in memory.

- Program memory
- Data memory

3.8.1 PROGRAM MEMORY ORGANIZATION:

The PIC16876 has a 13-bit program counter capable of addressing an 8kx14 program space. The PIC16873, the 1kx14 (0000h-03FFh) are physically implemented reset vector is at 0000h and the interrupt. The program memory is divided into four pages of2k words each (0h-7FFh, 800-FFFh, 1000-17FFh, and 1800h-1FFFh)

To jump between the program memories pages, the high bits of the program counter (PC) must be modified. This is done by writing the desired value into a SFR called PCLATH (Program Counter Latch High). If sequential instructions are executed, the program counter will cross the page boundaries without any intervention. That is, in a 4k- word device accessing 17FFh actually 7FFh. 2k- word devices (or less) do not require paging.

3.8.1.1 PROGRAM COUNTER:

The program counter (PC) specifies the address of the instruction to fetch for execution. The PC is 13-bits wide. The low byte is called the PCL register. This register is readable and writ able. The high byte is called the PCH register. This register contains the PC<12:8> bits and is not directly readable or writ able. All updates to the PCH register go through the PCLATH register.

3.8.1.2 RESET VECTOR:

On any device, a reset forces the Program Counter (PC) to address 0h. We call this address the "Reset Vector Address" since this is the address that program execution will branch to when a device reset occurs. Any reset will also clear the contents of the PCLATH register. This means that any branch at the Reset Vector Address (0h) will jump to that location in PAGE0 of the program memory.

3.8.1.3 INTERRUPT VECTOR:

When an interrupt is acknowledged the PC is forced to address 0004h. We call this the "interrupt vector address". When the PC is forced to the interrupt vector, the PCLATH register is not modified. Before the PCLATH register is modified by the Interrupt Service Routine (ISR) the contents of the PCLATH may need to be saved.

3.8.1.4 STACK:

Stack contains the return address from this branch in program execution.Mid-Range MCU devices have an 8-level deep x13-bit wide hardware stack. The Stack Space is not part of either program or data space and the stack pointer are not readable or writable. The Pc is PUSHed onto stack when a CALL instruction is executed or an

interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not modified when the stack is PUSHed or POPed .

3.8.1.5 PROGRAM MEMORY PAGING:

All PIC16F87X devices are capable of addressing a continuous 8K word block of program memory. The CALL and GOTO instructions provide only 11 bits of address to allow branching within any 2K program memory page. When doing a CALL or GOTO instruction, the upper 2 bits of the address are provided by PCLATH<4:3>. When doing a CALL or GOTO instruction, the user must ensure that the page select bits are programmed so that the desired program memory page is addressed. If a return from a CALL instruction (or interrupt) is executed, the entire 13-bit PC is popped off the stack. Therefore, manipulation of the PCLATH<4:3> bits is not required for the return instructions (which POPs the address from the stack).

3.8.2 DATA MEMORY ORGANIZATION:

Data memory is made up of the Special Function Registers (SFR) area, and The General Purpose Registers (GPR) area. The SFRs control the operation of the device; While GPRs are the general area for data storage and scratch pad operations.

The data memory is banked for both the GPR and SFR areas. The GPR area is banked to allow greater than 96 bytes of general purpose RAM to be addressed. SFRs are for the registers that control the peripheral and core functions. Baking requires the use of control bits for bank selection. These control bits are located in the STATUS Register (STATUS <7:5>).

To move values from one register to another register, the value must pass through the W register. This means that for all register –to- register moves, two instruction cycles are required. The entire data memory can be accessed directly or indirectly.

3.9 OSCILLATOR:

The internal oscillator circuit is used to generate the device clock. The device clock is required for the device to execute instruction and for the ripherals to function. Our device clock periods generate one internal instruction clock (TCY) cycle. There are up to eight different modes, which the oscillator may have. There are two modes, which allows the selection of the internal RC oscillator clock out (CLKOUT) to be driven on an I/O pin, or allow that I/O pin to be used for a general purpose function. The device configuration bits select the oscillator mode. The device configuration bits are non-volatile memory locations and the operating mode is determined by the value written during device programming. The RC oscillator option saves system cost while the LP crystal option saves power. Configuration bits are used to select the various options.

3.9.1 OSCILLATOR CONFIGURATIONS:

Mid-range devices can have up to eight different oscillator modes. The user can program up to three device configuration bits to select one of these eight modes:

- Low Frequency Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC External Resistor/Capacitor
- EXTRC External Resistor/Capacitor
- EXTRC External Resistor/Capacitor with CLKOUT
- INTRC Internal 4MHz Resistor/Capacitor
- INTRC Internal 4MHz Resistor/Capacitor with CLKOUT

The main difference between the LP, XT and HS modes is the gain of the internal inverter of the oscillator circuit, which allows the different frequency ranges.

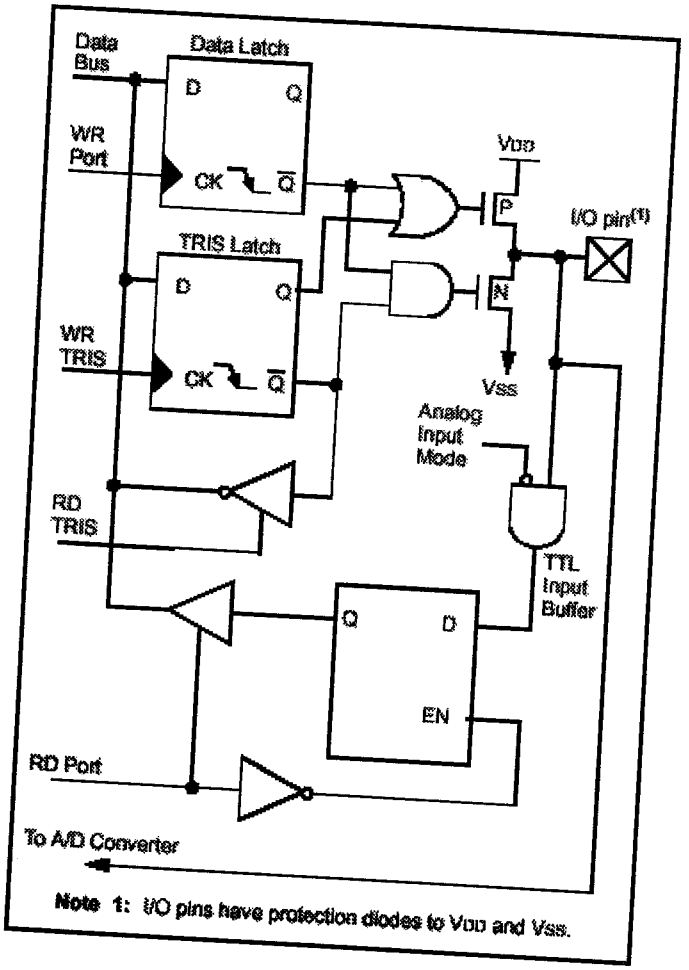
3.10 I/O PORTS:

General purpose I/O pins can be considered the simplest of peripherals. They allow the PIC microcontroller to monitor and control other devices. To add flexibility and functionality to a device, some pins are multiplexed with an alternate function. These functions depend on which peripheral features are on the device. In general, when a perirheral is functioning, that pin may not be used as a general purpose I/O pin. For most ports,the data direction register called the TRIS register controls the I/O pins direction (I/O).

3.10.1 PORTA and the TRISA Register:

PORTA is a 6-bit wide, bi-directional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).The RA4 pin is a Schmitt Trigger input and an open drain output. All other PORTA pins have TTL input levels and full CMOS output drivers.

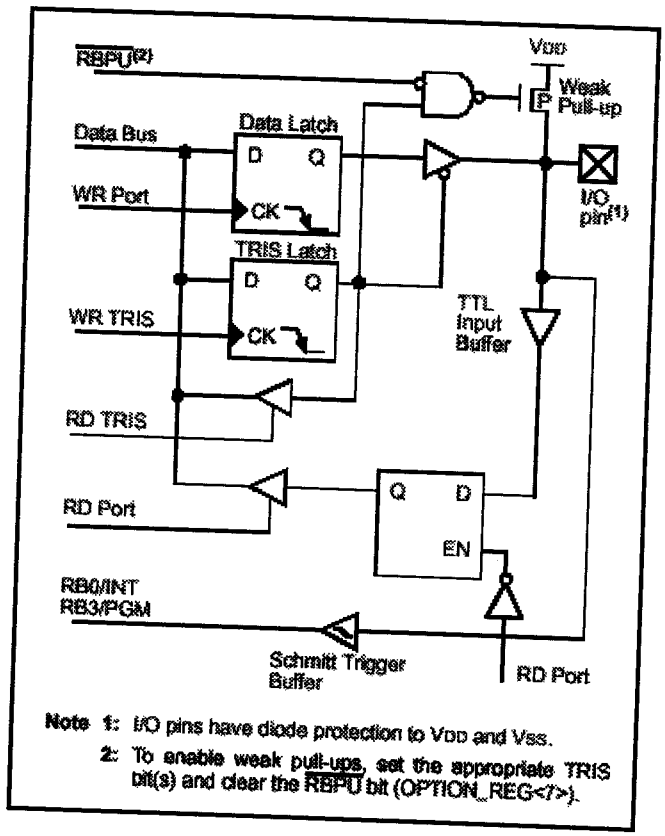
BLOCK DIAGRAM OF RA3:RA0 AND RA5 PINS



3.10.2 PORTB and the TRISB Register:

PORTB is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISB. Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin).

BLOCK DIAGRAM OF RB3:RB0 PINS



3.11 TIMER0 MODULE:

The Timer0 module timer/counter has the following fea-tures:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

3.11.1 TIMER 0 INTERRUPT :

The TMR0 interrupt is generated when the TMR0 reg-ister overflows from FFh to 00h. This overflow sets bit T0IF (INTCON<2>). The interrupt can be masked by clearing bit T0IE (INTCON<5>). Bit T0IF must be cleared in software by the Timer0 module Interrupt Ser-vice Routine before re-enabling this interrupt. The TMR0 interrupt cannot awaken the processor from SLEEP, since the timer is shut-off during SLEEP.

3.11.2 USING TIMER0 WITH AN EXTERNAL CLOCK:

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accom-plished by sampling the prescaler output on the Q2 and
Q4 cycles of the internal phase clocks. Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

OPTION_REG REGISTER:

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7						bit 0	

bit 7 **RBPU**

bit 6 **INTEDG**

bit 5 **T0CS**: TMR0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4 **T0SE**: TMR0 Source Edge Select bit

1 = Increment on high-to-low transition on T0CKI pin

0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA**: Prescaler Assignment bit

1 = Prescaler is assigned to the WDT

0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS2:PS0**: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

3.11.2 TIMER2 MODULE:

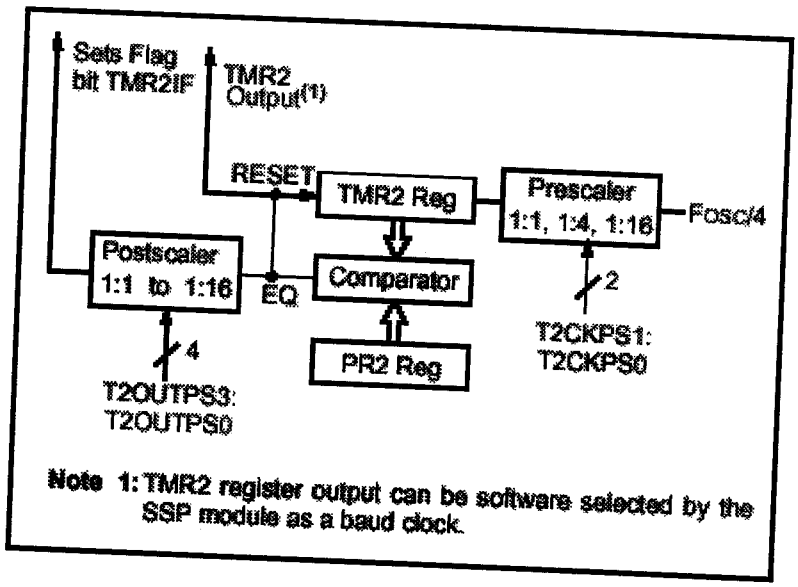
Timer2 is an 8-bit timer with a prescaler and a postscaler. It can be used as the PWM time-base for the PWM mode of the CCP module(s). The TMR2 reg-ister is readable and writable, and is cleared on any device RESET.

The input clock (FOSC/4) has a prescale option of 1:1, 1:4, or 1:16, selected by control bits T2CKPS1:T2CKPS0 (T2CON<1:0>).

The Timer2 module has an 8-bit period register, PR2.Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to FFh upon RESET.

The match output of TMR2 goes through a 4-bit postscaler (which gives a 1:1 to 1:16 scaling inclusive) to generate a TMR2 interrupt (latched in flag bit TMR2IF, (PIR1<1>)). Timer2 can be shut-off by clearing control bit TMR2ON (T2CON<2>), to minimize power consumption.

TIMER2 BLOCK DIAGRAM



T2CON: TIMER2 CONTROL REGISTER:

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit 7							bit 0

bit 7 **Unimplemented:** Read as '0'

bit 6-3 **TOUTPS3:TOUTPS**0: Timer2 Output Postscale Select bits

0000 = 1:1 Postscale

0001 = 1:2 Postscale

0010 = 1:3 Postscale

•

•

•

1111 = 1:16 Postscale

bit 2 **TMR2ON**: Timer2 On bit

1 = Timer2 is on

0 = Timer2 is off

bit 1-0 **T2CKPS1:T2CKPS**0: Timer2 Clock Prescale Select bits

00 = Prescaler is 1

01 = Prescaler is 4

1x = Prescaler is 16

3.12 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE:

The Analog-to-Digital (A/D) Converter module has five inputs for the 28-pin devices and eight for the other devices. The analog input charges a sample and hold capacitor.

The output of the sample and hold capacitor is the input into the converter. The converter then generates a dig-ital result of this analog level via successive approximation. The A/D conversion of the analog input signal results in a corresponding 10-bit digital number. The A/D module has high and low voltage reference input that is software selectable to some combination of VDD, VSS, RA2, or RA3. The A/D converter has a unique feature of being able to operate while the device is in SLEEP

mode. To operate in SLEEP, the A/D clock must be derived from the A/D's internal RC oscillator.

The A/D module has four registers. These registers are:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register0 (ADCON0)
- A/D Control Register1 (ADCON1)

The ADCON0 register, shown , controls the operation of the A/D module. The ADCON1register, shown in Register, configures the functions of the port pins. The port pins can be configured as analog inputs (RA3 can also be the voltage reference), or as digital I/O.

ADCON0 REGISTER:

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON
bit7							bit 0

bit 7-6 **ADCS1:ADCS0:** A/D Conversion Clock Select bits

00 = FOSC/2

01 = FOSC/8

10 = FOSC/32

11 = FRC (clock derived from the internal A/D module RC oscillator)

bit 5-3 **CHS2:CHS**0: Analog Channel Select bits

000 = channel 0, (RA0/AN0)

001 = channel 1, (RA1/AN1)

010 = channel 2, (RA2/AN2)

011 = channel 3, (RA3/AN3)

100 = channel 4, (RA5/AN4)

101 = channel 5, (RE0/AN5) **(1)**

110 = channel 6, (RE1/AN6) **(1)**

111 = channel 7, (RE2/AN7) **(1)**

bit 2 **GO/DONE:** A/D Conversion Status bit

If ADON = 1:

1 = A/D conversion in progress (setting this bit starts the A/D conversion)

0 = A/D conversion not in progress (this bit is automatically cleared by hardware when the A/D
conversion is complete)

bit 1 **Unimplemented**: Read as '0'

bit 0 **ADON**: A/D On bit

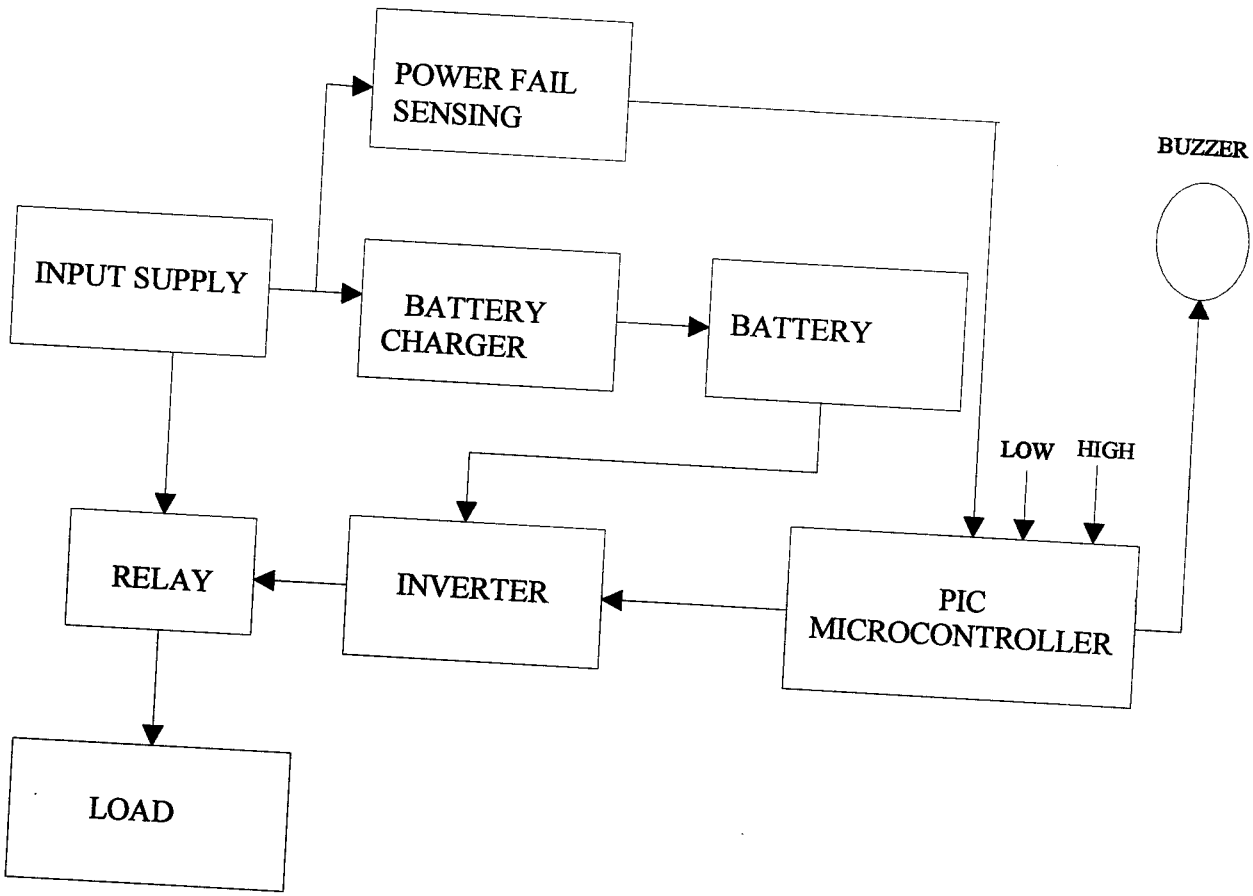
1 = A/D converter module is operating

0 = A/D converter module is shut-off and consumes no operating current

HARDWARE IMPLEMENTATION

4. HARDWARE IMPLEMENTATION

BLOCK DIAGRAM



The following are the essential parts of the UPS:

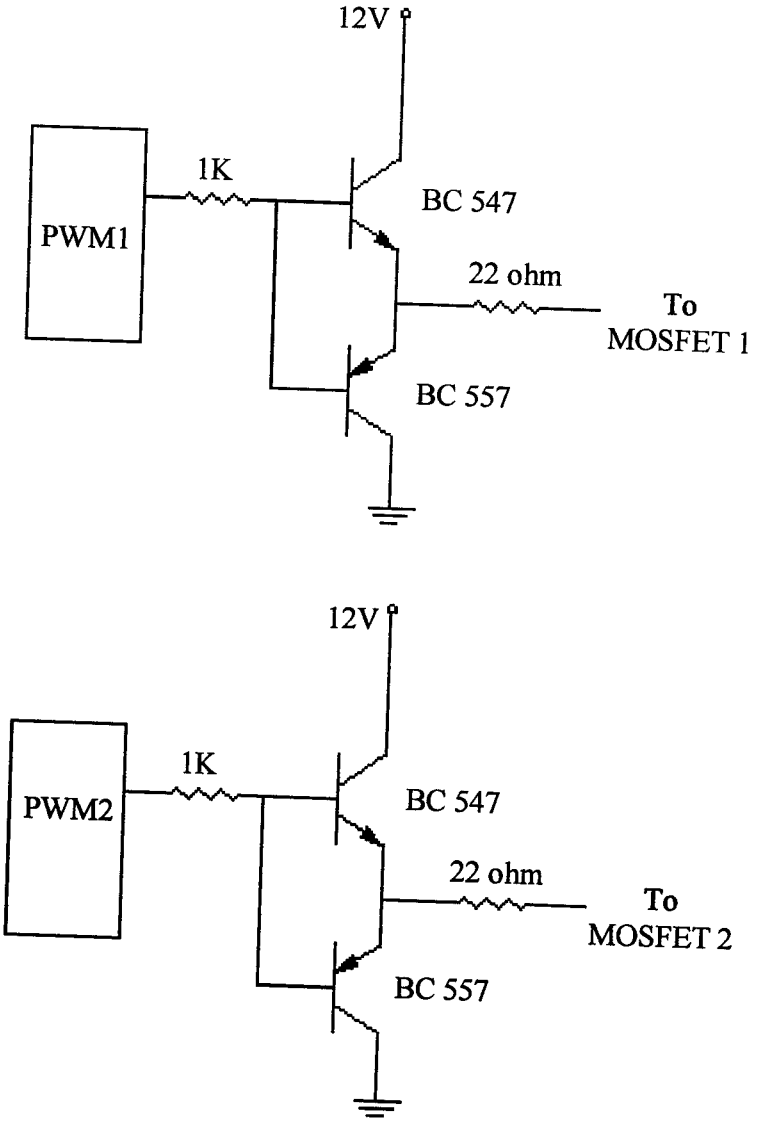
- Battery
- Inverter
- Power supply
- Micro controller (16F846)
- Transformer

The power flow for the system is shown above. When the input supply is on the power to the load is directly supplied from it. But when the input supply goes off or the voltage level exceeds or comes below the specified voltage levels, it is sensed by the microcontroller and the relay is switched so that the power is now supplied from the battery.

The PWM output is generated in the PIC 16F876. As the microcontroller cannot trigger the MOSFET directly, the PWM signals are given to the MOSFET driver circuit, which in turn drives the push-pull inverter. The output of the push pull inverter stepped up and is given to the load after passing through a filter.

An output is stepped down feedback to the PIC16F876 where A/D conversion takes place for output monitoring. All module synchronization, control, and fault detection are handled through the PIC16F876.

4.1 MOSFET DRIVER CIRCUIT



The power supply in any circuit is an important part. Care and protection should be ensured while designing the power supply circuit.

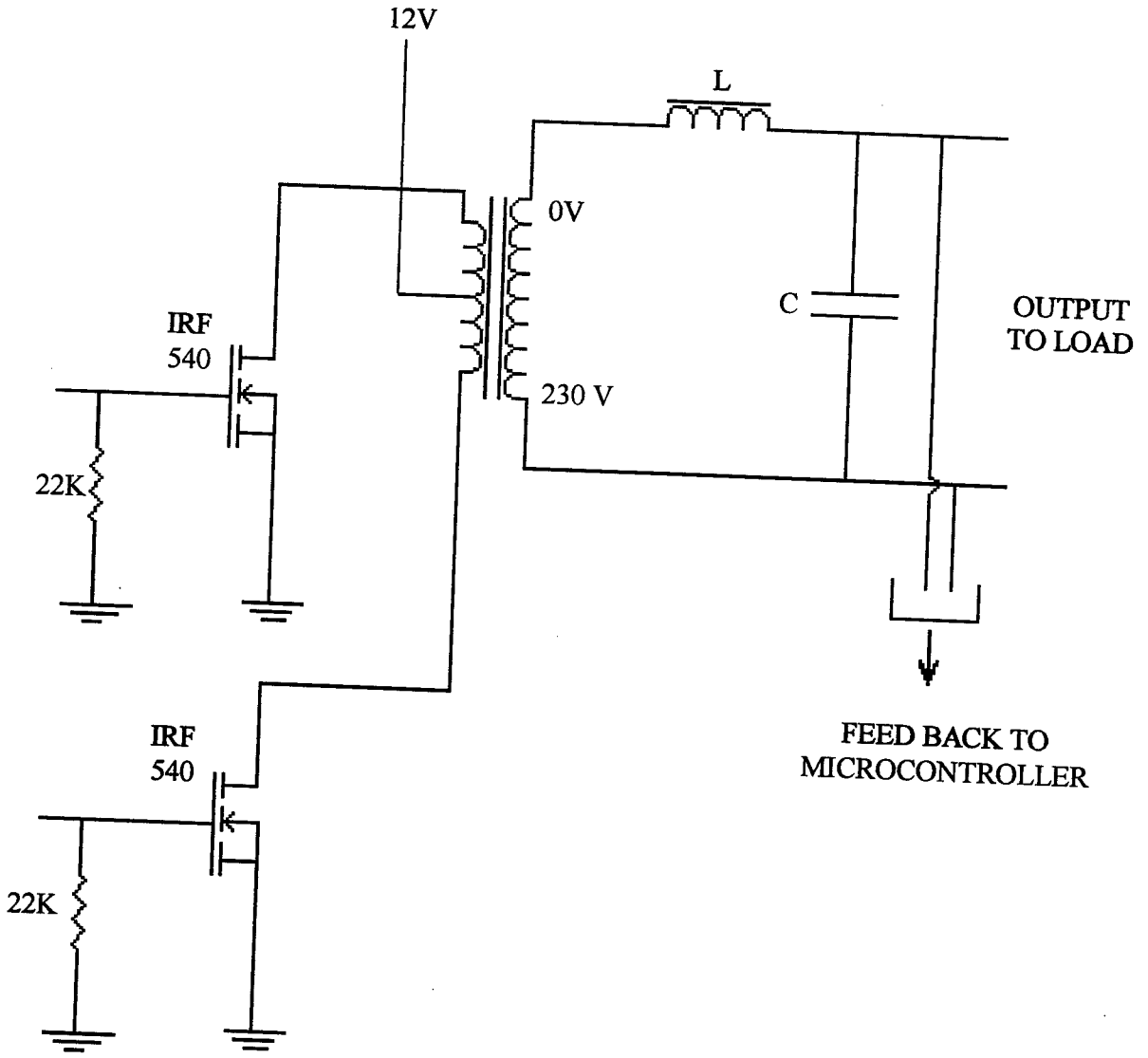
The driving of the MOSFETs should be done by raising the gate to source voltage above the threshold voltage of the MOSFET (IRF 540).

The driving circuit of the MOSFET consists of two transistors BC547 and BC557. The 12v battery is connected to the collector of the transistor. The PWM output from the PIC microcontroller is given as input to the base of the transistors. When the input is high the transistor BC547 is turned on and driving signals are given to the MOSFET. When the input is low the transistor BC547 would be in the floating state, so it is grounded using the transistor BC557.

4.2INVERTER CIRCUIT

The inverter section is of push pull type it has got two mosfets trigered with 180 degree phase shift the mosfet is been triggered by the pwm generated wit reference to the sine angle. the o/p of the inverter section is given to the secondary of a center tapped transformer, the primary of the transformer is connected with a choke to filter the high frequency signal(harmonics) the o/p across the choke is pure AC signal and the same is givwn as i/p to feedback transformer to perform RTS for the controller to improve the o/p efficiency .

INVERTER CIRCUIT



4.3 ANALOG TO DIGITAL CONVERSION:

In analog-to-digital converter (ADC) accepts an analog input a voltage or a current and converts it to a digital value that can be read by a microprocessor. This hypothetical part has two inputs: a reference and the signal to be measured. It has one output, an 8-bit digital word that represents the input value.

The reference voltage is the maximum value that the ADC can convert. Our example 8-bit ADC can convert values from 0V to the reference voltage. This voltage range is divided into 256 values, or steps. The size of the step is given by: $\mathbf{V_{ref}/256}$ where V_{ref} is the reference voltage. The step size of the converter defines the converter's resolution. For a 5V reference, the step size is: **5V/256 = 0.0195V or 19.5Mv**.

Our 8-bit converter represents the analog input as a digital word. The most significant bit of this word indicates whether the input voltage is greater than half the reference (2.5V, with a 5V reference). Each succeeding bit represents half the range of the previous bit.

The resolution of an ADC is determined by the reference input and by the word width. The resolution defines the smallest voltage change that can be measured by the ADC. The resolution is the same as the smallest step size, and can be calculated by dividing the reference voltage by the number of possible conversion values. Resolution can be improved by reducing the reference input. The only way to increase resolution without reducing the range is to use an ADC with more bits. A 10-bit ADC has 2^{10}, or 1,024 possible output codes. So the resolution is 5V/1,024, or 4.88mV; a 12-bit ADC has a 1.22mV resolution for this same reference.

Types of ADCs are flash, successive approximation, and sigma-delta.

4.3.1 CHARACTERISTICS OF ADC:

a) RESOLUTION:

The resolution of the converter indicates the number of discrete values it can produce. It is usually expressed in bits. For example, an ADC that encodes an analog input to one of 256 discrete values has a resolution of eight bits, since

$$2^8 = 256.$$

b) RESPONSE TIME:

Most ADCs are linear, which means that they are designed to produce an output value that is a linear function of, i.e. proportional to, the input. Another common type is the logarithmic ADC, which is used in telecommunications systems where the amplitude of the input signal varies over a wide range. The logarithmic ADC compresses the input signal into a smaller number of bits than a linear ADC with the same input range and resolution.

c) ACCURACY:

Accuracy depends on the error in the conversion. If the ADC is not broken, this error has two components: quantization error and (assuming the ADC is intended to be linear) non-linearity. These errors are measured in a unit called the LSB, which is an abbreviation for least significant bit. In the above example of an eight-bit ADC, an error of one LSB is 1/256 of the full signal range, or about 0.4%. Quantization error is due to the finite resolution of the ADC, and is an unavoidable imperfection in all types of ADC. The magnitude of the quantization error at the sampling instant is between zero and half of one LSB.

d) SAMPLING RATE:

Commonly, the analog signal is continuous in time and it is necessary to convert this to a flow of digital values. It is therefore required to define the rate at which new digital values are sampled from the analog signal. The rate of new values is called sampling rate of the converter.

The key idea here is that a continuously varying band limited signal can be sampled (i.e. the signal values at intervals of time T, the sampling time, are measured and stored.) and then the original signal can be exactly reproduced from the discrete-time values by an interpolation formula. The accuracy is however limited by quantization error. However this faithful reproduction is only possible if the sampling rate is higher than twice the highest frequency component present in the signal. This is essentially what is called Shannon's sampling theorem.

e) ALIASING:

All ADCs work by sampling their input at discrete intervals of time. Their output is therefore an incomplete picture of the behaviors of the input. There is no way of knowing, by looking at the output, what the input was doing between one sampling instant and the next. If the input is known to be changing slowly compared to the sampling rate, then it can be assumed that the value of the signal between two sample instants was somewhere between the two sampled values. If, however, the input signal is changing fast compared to the sample rate, then this assumption is not valid. If the digital values produced by the ADC are, at some later stage in the system, converted back to analog values by a ADC or a DAC, it is desirable that the output of the DAC is a faithful representation of the original signal. If the input signal is changing much faster than the sample rate, then this will not be the case, and spurious signals called aliases will be produced at the output of the DAC.

4.4 SINE SYNTHESIS TABLE:

The sinusoidal reference table for the inverter is generated as follows:

1. Choose Vp such that this number corresponds with the desired output voltage of the inverter.

Example: If the desired output voltage is 230V and the A/D converter used to sample the output voltage has a gain of .8 counts per output volt,
then:

$$Vp = 0.8(230*(2\text{^}.5))$$

and Vp would be equal to 254.6, or 255 rounded to the nearest integer.
The external circuitry interfacing the A/D converter to the output of the inverter should scale the input voltage to the A/D such that the peak of the desired output voltage should correspond to almost a full count on the A/D.

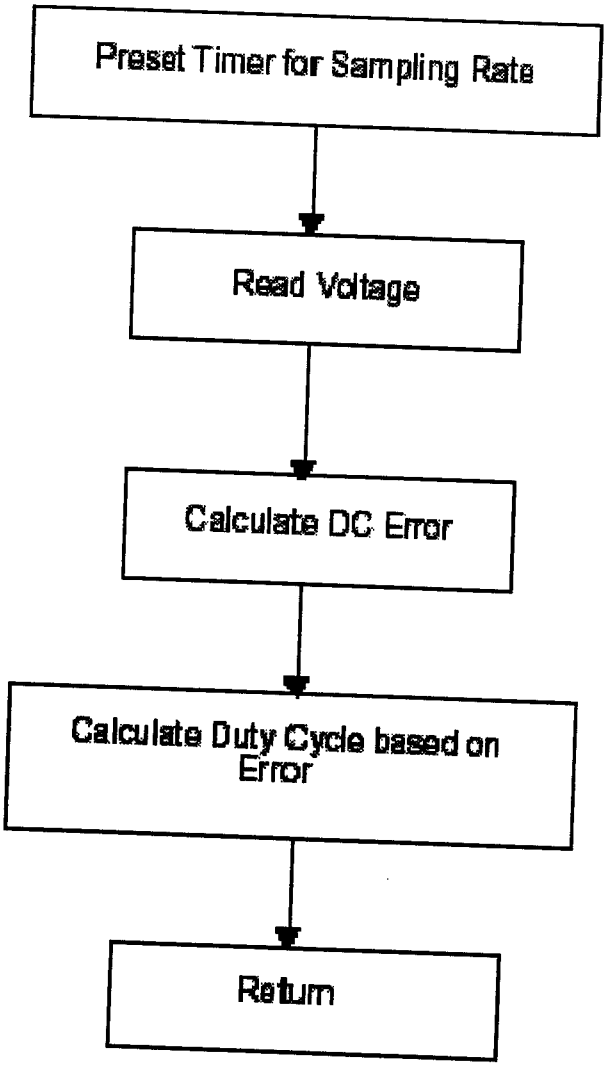
2. The table is generated from the following equation with k = 0.... N/2 - 1 and N = the number of samples per cycle.

$$Vref = Vp \sin(2*pi*k/N)$$

Example: For the Vp of the previous example and N = 15 samples per cycle, this yields the following table entries. Note that only 7 entries are generated as the negative-going half wave may be generated from the negative of the first 7.
Vref = {0, 108, 190, 232, 232, 187, 104}

4.5 REAL TIME SAMPLING

Interrupt Handler Flow

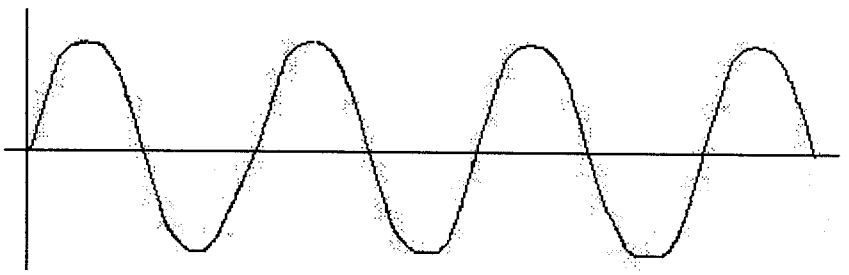


In general sine wave is generated in UPS using discrete components. A sine wave generated in this case can be sampled only after the completion of one cycle. But in case of the sine synthesized UPS, the sine wave generated can be sampled within each cycle by dividing into definite steps.

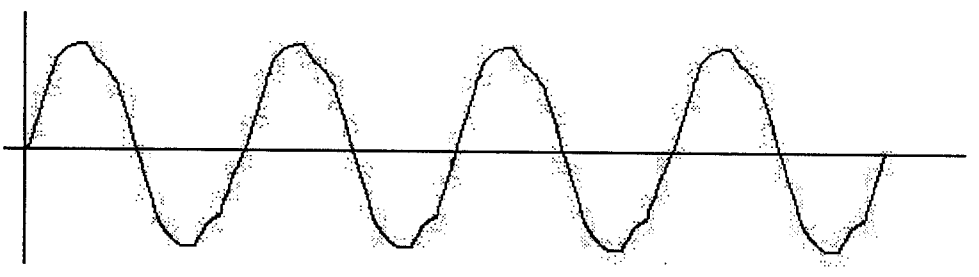
The output at each step is compared to the predefined value at that point obtained using sine synthesis table. If there is no difference between the generated output and the reference value then the next step output is generated without any correction. If there is any difference the necessary correction is done i.e. if the output is more than the reference value then the next step input is decreased to get consistent output and vice versa. Thus a refined sine wave can be obtained with the completion of each cycle.

4.6 OUTPUT WAVEFORMS:

Output wave without feedback:



Output wave with feedback:



SOFTWARE CODING

5.SOFTWARE CODING

```
/*-------------------------------------------------------------------
                    closed loop single phase with soft start
                        working program
                        pushpull inverter

-------------------------------------------------------------------*/
#include<pic.h>
/*-------------------------------------------------------------------
                    sine reference table
-------------------------------------------------------------------*/
const char ref0[]={0,2,4,5,5,4,2,0};
const char ref1[]={0,7,13,16,16,13,7,0};
const char ref2[]={0,10,20,30,30,20,10,0};
const char ref3[]={0,14,30,45,45,30,14,0};   //softstart reference values
const char ref4[]={0,28,50,62,62,50,28,0};
const char ref5[]={0,42,75,91,91,75,42,0};
const char ref6[]={0,56,99,123,123,99,56,0};
const char ref7[]={0,69,125,155,155,125,69,0};



const char refo[]={0,108,190,232,232,187,104,0};//normally used
/*-------------------------------------------------------------------
                    variable declaration
-------------------------------------------------------------------*/
char volt,amps,bamps,bvolt,come,yes=1,refery,start;
char first,s,upson=0,k;
int income;
/*-------------------------------------------------------------------
                    function declaration
-------------------------------------------------------------------*/
init();
posint();
negint();
delay();
/*-------------------------------------------------------------------
                    main routine
-------------------------------------------------------------------*/
main()
{
init();
while(ADRESH>1&&ADRESH<=2)//check for hv/lv/pf
```

```
        {
        CCP1CON=0;          //no check again
        T0CS=1;
        ADCON1=0X80;
        ADCON0=0X89;
        for(s=0;s<10;s++);
        ADGO=1;
        while(ADGO);
        }
        delay();                //delay
        posint();                       //ups o/p starts
        TMR2ON=1;
        first=1;
        income=0;
        T0CS=0;
        TMR0=0X27;
        while(1)
        {
        while(ADRESH>=1&&ADRESH<3&&ADCON0==0X89)        //channel check
        //ra0----feedback  ra1 -------- hv/lv/pf i/p
        {
        ADCON1=0X80;
        ADCON0=0X89;
        for(s=0;s<10;s++);                              // normal operation ups off
        ADGO=1;
        while(ADGO);
        CCP1CON=0X00;
        CCP2CON=0X00;
        first=1;
        income=0;
        upson=1;
        T0CS=1;
        TMR2ON=0;
        }
        delay();
        while(ADRESH<1||ADRESH>2&&ADCON0==0X89)
        {
        ADCON1=0X80;
        ADCON0=0X89;        //channel 1
        for(s=0;s<10;s++);                                      // hv/lv/pf ups on
        ADGO=1;
        while(ADGO);
        if(upson==1)
        {
        upson=0;
```

```
posint();
TMR2ON=1;
first=1;
income=0;
T0CS=0;
TMR0=0X27;
}
}
}
}
/*-----------------------------------------------------------------
                        positive cycle init routine
-----------------------------------------------------------------*/
posint()
{
CCP2CON=0;
CCPR1L=CCPR1H=0;                                    // positive cycle init
CCPR2L=CCPR2H=0;
CCP1CON=0X0C;
TMR2=0;
yes=!yes;
come=0;
volt=bvolt=0;
if(first>0)
income++;
if(income==30)
{
first++;
income=0;
}
}
/*-----------------------------------------------------------------
                        negative cycle init routine
-----------------------------------------------------------------*/
negint()
{
CCP1CON=0;
CCPR1L=CCPR1H=0;
CCPR2L=CCPR2H=0;                                    // negative half cycle init
CCP2CON=0X0C;
yes=!yes;
come=0;
volt=bvolt=0;
TMR2=0;
}
```

```
/*-------------------------------------------------------------------
                        initialisation routine
-------------------------------------------------------------------*/
init()
{
TRISA=0XFF;
TRISB=0X00;
TRISC=0X00;
PORTA=0X00;
PORTB=0X00;
PORTC=0X00;
ADCON1=0;
ADCON0=0;
INTCON=0XC0;
T2CON=0X00;
PR2=250;
T0IE=1;
OPTION=0X04;
}
/*-------------------------------------------------------------------
                        interrupt service routine
-------------------------------------------------------------------*/
static void interrupt isr()
{
if(T0IF==1)
T0IF=0;
come++;
if(first>8)
first=0;

if(come<7)
{
if(first==1)
refery=ref0[(come)];
if(first==2)
refery=ref1[(come)];
if(first==3)
refery=ref2[(come)];
if(first==4)
refery=ref3[(come)];                    // softstart routine
if(first==5)
refery=ref4[(come)];
if(first==6)
refery=ref5[(come)];
if(first==7)
```

```
refery=ref6[(come)];
if(first==8)
refery=ref7[(come)];                    //come-- sine angle spec for change in duty cycle
if(first==0)
refery=refo[(come)];

if(yes==0&&first!=0)
CCPR1L=refery;
if(yes==1&&first!=0)
CCPR2L=refery;
if(first==0)
{
ADFM=1;
ADCON0=0X81;                //channel -0
ADGO=1;
while(ADGO);
volt=(ADRESH*256+ADRESL)*10/43;
bvolt=volt;
volt=volt-refery;
if(CARRY)
{
if(yes==0)
CCPR1L=refery-volt;
if(yes==1)
CCPR2L=refery-volt;
}
if(!CARRY)
{
volt=refery+(refery-bvolt);
if(volt>234)
volt=234;
if(bvolt<5)
volt=refery;
if(yes==0)
CCPR1L=volt;
if(yes==1)
CCPR2L=volt;
}
}
}
if(come==7&&yes==0)
negint();
if(first!=0)
TMR0=0X26;
if(first==0)
```

```
TMR0=0X33;
if(come==7&&yes==1)
posint();
}


delay()
{
T1CON=0;
TMR1ON=1;
for(k=0;k<30;k++)
{
TMR1L=0;
TMR1H=0;
while(!TMR1IF);
TMR1IF=0;
}
}
```

CONCLUSION

6. CONCLUSION

The sine synthesized uninterruptible power supply system was designed, assembled and tested. The set up can be tested for its high quality sine wave output. As the output obtained is sine wave the efficiency and also the life of the loads connected to the UPS are increased.

As the microcontrollers are getting much popular, the sine synthesized UPS will be the trend in the near future. The discrete analog components are effectively replaced by the microcontroller thus reducing the cost.

SCOPE FOR FUTURE WORK:

- In the sine synthesized UPS we have considered only the voltage feed back, by taking current feed back also the power factor correction can be made.

- For higher rating of UPS the MOSFETs can be replaced by IGBTs.

- LCD displays can be provided to display the battery voltage and the output voltage. Also the back up time of system can be displayed usin the microcontroller.

- The UPS may be connected to the computer and when the battery level goes down the computer can be programmed to shut down automatically.

REFERENCES

REFERENCES:

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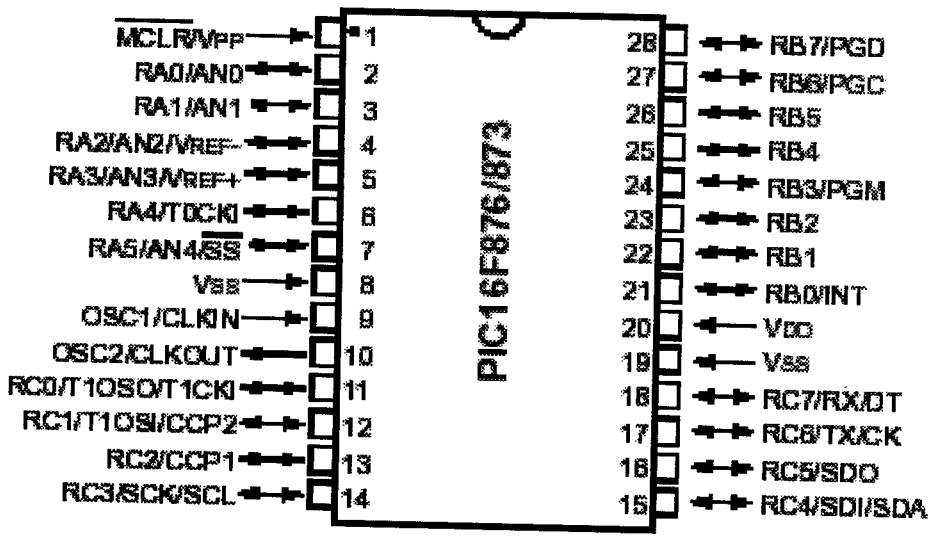
APPENDIX

PIN DIAGRAM OF PIC16F876:



Key Features PICmicro™ Mid-Range Reference Manual (DS33023)	PIC16F876
Operating Frequency	DC - 20 MHz
RESETS (and Delays)	POR, BOR (PWRT, OST)
FLASH Program Memory (14-bit words)	8K
Data Memory (bytes)	368
EEPROM Data Memory	256
Interrupts	13
I/O Ports	Ports A,B,C
Timers	3
Capture/Compare/PWM Modules	2
Serial Communications	MSSP, USART
Parallel Communications	—
10-bit Analog-to-Digital Module	5 input channels
Instruction Set	35 instructions

TABLE 1-1: PIC16F873 AND PIC16F876 PINOUT DESCRIPTION

Pin Name	DIP Pin#	SOIC Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	9	9	I	ST/CMOS(3)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	10	10	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR/VPP	1	1	I/P	ST	Master Clear (Reset) input or programming voltage input. This pin is an active low RESET to the device.
					PORTA is a bi-directional I/O port.
RA0/AN0	2	2	I/O	TTL	RA0 can also be analog input0.
RA1/AN1	3	3	I/O	TTL	RA1 can also be analog input1.
RA2/AN2/VREF-	4	4	I/O	TTL	RA2 can also be analog input2 or negative analog reference voltage.
RA3/AN3/VREF+	5	5	I/O	TTL	RA3 can also be analog input3 or positive analog reference voltage.
RA4/T0CKI	6	6	I/O	ST	RA4 can also be the clock input to the Timer0 module. Output is open drain type.
RA5/$\overline{SS}$/AN4	7	7	I/O	TTL	RA5 can also be analog input4 or the slave select for the synchronous serial port.
					PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	21	21	I/O	TTL/ST(1)	RB0 can also be the external interrupt pin.
RB1	22	22	I/O	TTL	
RB2	23	23	I/O	TTL	
RB3/PGM	24	24	I/O	TTL	RB3 can also be the low voltage programming input.
RB4	25	25	I/O	TTL	Interrupt-on-change pin.
RB5	26	26	I/O	TTL	Interrupt-on-change pin.
RB6/PGC	27	27	I/O	TTL/ST(2)	Interrupt-on-change pin or In-Circuit Debugger pin. Serial programming clock.
RB7/PGD	28	28	I/O	TTL/ST(2)	Interrupt-on-change pin or In-Circuit Debugger pin. Serial programming data.
					PORTC is a bi-directional I/O port.
RC0/T1OSO/T1CKI	11	11	I/O	ST	RC0 can also be the Timer1 oscillator output or Timer1 clock input.
RC1/T1OSI/CCP2	12	12	I/O	ST	RC1 can also be the Timer1 oscillator input or Capture2 input/Compare2 output/PWM2 output.
RC2/CCP1	13	13	I/O	ST	RC2 can also be the Capture1 input/Compare1 output/ PWM1 output.
RC3/SCK/SCL	14	14	I/O	ST	RC3 can also be the synchronous serial clock input/output for both SPI and I^2C modes.
RC4/SDI/SDA	15	15	I/O	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I^2C mode).
RC5/SDO	16	16	I/O	ST	RC5 can also be the SPI Data Out (SPI mode).
RC6/TX/CK	17	17	I/O	ST	RC6 can also be the USART Asynchronous Transmit or Synchronous Clock.
RC7/RX/DT	18	18	I/O	ST	RC7 can also be the USART Asynchronous Receive or Synchronous Data.
Vss	8, 19	8, 19	P	—	Ground reference for logic and I/O pins.
VDD	20	20	P	—	Positive supply for logic and I/O pins.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral modules for controlling the desired operation of the device. These registers are implemented as static RAM. A list of these registers is given in Table

The Special Function Registers can be classified into two sets: core (CPU) and peripheral. Those registers associated with the core functions are described in detail in this section. Those related to the operation of the peripheral features are described in detail in the peripheral features section.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page:
Bank 0											
00h(3)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	27
01h	TMR0	Timer0 Module Register								xxxx xxxx	47
02h(3)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	26
03h(3)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	18
04h(3)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	27
05h	PORTA			PORTA Data Latch when written: PORTA pins when read						--0x 0000	29
06h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	31
07h	PORTC	PORTC Data Latch when written: PORTC pins when read								xxxx xxxx	33
08h(4)	PORTD	PORTD Data Latch when written: PORTD pins when read								xxxx xxxx	35
09h(4)	PORTE						RE2	RE1	RE0	---- -xxx	36
0Ah(1,3)	PCLATH			Write Buffer for the upper 5 bits of the Program Counter						---0 0000	26
0Bh(3)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	20
0Ch	PIR1	PSPIF(2)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	22
0Dh	PIR2		(5)		EEIF	BCLIF			CCP2IF	-r-0 0--0	24
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	52
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	52
10h	T1CON			T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	--00 0000	51
11h	TMR2	Timer2 Module Register								0000 0000	56
12h	T2CON		TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	55
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	70, 73
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	67
15h	CCPR1L	Capture/Compare/PWM Register1 (LSB)								xxxx xxxx	57
16h	CCPR1H	Capture/Compare/PWM Register1 (MSB)								xxxx xxxx	57
17h	CCP1CON			CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	58
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	98
19h	TXREG	USART Transmit Data Register								0000 0000	99
1Ah	RCREG	USART Receive Data Register								0000 0000	101
1Bh	CCPR2L	Capture/Compare/PWM Register2 (LSB)								xxxx xxxx	57
1Ch	CCPR2H	Capture/Compare/PWM Register2 (MSB)								xxxx xxxx	57
1Dh	CCP2CON			CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	58
1Eh	ADRESH	A/D Result Register High Byte								xxxx xxxx	116
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE		ADON	0000 00-0	111

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.
2: Bits PSPIE and PSPIF are reserved on PIC16F873/876 devices; always maintain these bits clear.
3: These registers can be addressed from any bank.
4: PORTD, PORTE, TRISD, and TRISE are not physically implemented on PIC16F873/876 devices; read as '0'.
5: PIR2<6> and PIE2<6> are reserved on these devices; always maintain these bits clear.

CAPTURE/COMPARE/PWM MODULES

Each Capture/Compare/PWM (CCP) module contains a 16-bit register which can operate as a:

• 16-bit Capture register

• 16-bit Compare register

• PWM Master/Slave Duty Cycle register Both the CCP1 and CCP2 modules are identical in operation, with the exception being the operation of the special event trigger. Table 8-2 show the resources and interactions of the CCP module(s). In the following sections, the operation of a CCP module is described with respect to CCP1. CCP2 operates the same as CCP1, except where noted.

CCP1 Module:

Capture/Compare/PWM Register1 (CCPR1) is comprised of two 8-bit registers: CCPR1L (low byte) and CCPR1H (high byte). The CCP1CON regist1.er controls the operation of CCP1. The special event trigger is generated by a compare match and will reset Timer

CCP2 Module:

Capture/Compare/PWM Register2 (CCPR2) is comprised of two 8-bit registers: CCPR2L (low byte) and CCPR2H (high byte). The CCP2CON register controls the operation of CCP2. The special event trigger is generated by a compare match and will reset Timer1and start an A/D conversion (if the A/D module is enabled).

CCPx Mode	CCPy Mode	Interaction
Capture	Capture	Same TMR1 time-base
Capture	Compare	The compare should be configured for the special event trigger, which clears TMR1
Compare	Compare	The compare(s) should be configured for the special event trigger, which clears TMR1
PWM	PWM	The PWMs will have the same frequency and update rate (TMR2 interrupt)
PWM	Capture	None
PWM	Compare	None

CCP1CON REGISTER/CCP2CON REGISTER (ADDRESS: 17h/1Dh)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CCPxX	CCPxY	CCPxM3	CCPxM2	CCPxM1	CCPxM0
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **CCPxX:CCPxY**: PWM Least Significant bits

Capture mode:
Unused

Compare mode:
Unused

PWM mode:
These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPRxL.

bit 3-0 **CCPxM3:CCPxM0**: CCPx Mode Select bits

0000 = Capture/Compare/PWM disabled (resets CCPx module)
0100 = Capture mode, every falling edge
0101 = Capture mode, every rising edge
0110 = Capture mode, every 4th rising edge
0111 = Capture mode, every 16th rising edge
1000 = Compare mode, set output on match (CCPxIF bit is set)
1001 = Compare mode, clear output on match (CCPxIF bit is set)
1010 = Compare mode, generate software interrupt on match (CCPxIF bit is set, CCPx pin is unaffected)
1011 = Compare mode, trigger special event (CCPxIF bit is set, CCPx pin is unaffected); CCP1 resets TMR1; CCP2 resets TMR1 and starts an A/D conversion (if A/D module is enabled)
11xx = PWM mode

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

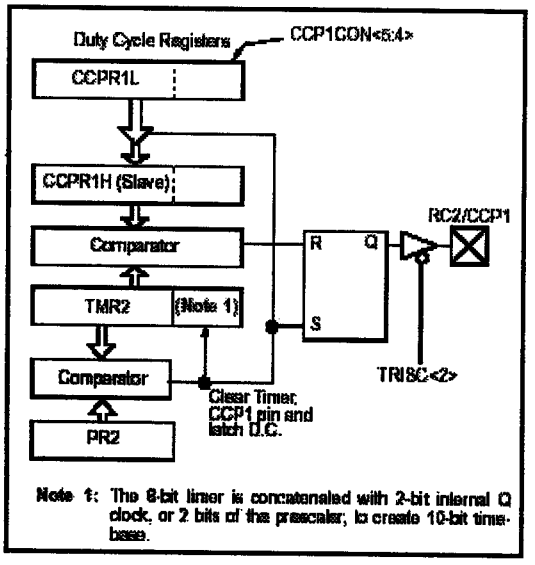
PWM Mode (PWM)

In Pulse Width Modulation mode, the CCPx pin produces up to a 10-bit resolution PWM output. Since the

CCP1 pin is multiplexed with the PORTC data latch, the TRISC<2> bit must be cleared to make the CCP1 pin an output.

Figure shows a simplified block diagram of the CCP module in PWM mode.

SIMPLIFIED PWM BLOCK DIAGRAM



SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Set the PWM period by writing to the PR2 register.
2. Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON<5:4> bits.
3. Make the CCP1 pin an output by clearing the TRISC<2> bit.
4. Set the TMR2 prescale value and enable Timer2 by writing to T2CON.
5. Configure the CCP1 module for PWM operation.

REGISTERS ASSOCIATED WITH CAPTURE, COMPARE, AND TIMER1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
0Bh,8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh	PIR2	—	—	—	—	—	—	—	CCP2IF	----- ---0	----- ---0
8Ch	PIE1	PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh	PIE2	—	—	—	—	—	—	—	CCP2IE	----- ---0	----- ---0
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	--00 0000	--uu uuuu
15h	CCPR1L	Capture/Compare/PWM Register1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM Register1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
1Bh	CCPR2L	Capture/Compare/PWM Register2 (LSB)								xxxx xxxx	uuuu uuuu
1Ch	CCPR2H	Capture/Compare/PWM Register2 (MSB)								xxxx xxxx	uuuu uuuu
1Dh	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by Capture and Timer1.
Note 1: The PSP is not implemented on the PIC16F873/876; always maintain these bits clear.

REGISTERS ASSOCIATED WITH PWM AND TIMER2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
0Bh,8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh	PIR2	—	—	—	—	—	—	—	CCP2IF	---- ---0	---- ---0
8Ch	PIE1	PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh	PIE2	—	—	—	—	—	—	—	CCP2IE	---- ---0	---- ---0
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
11h	TMR2	Timer2 Module's Register								0000 0000	0000 0000
92h	PR2	Timer2 Module's Period Register								1111 1111	1111 1111
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
15h	CCPR1L	Capture/Compare/PWM Register1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM Register1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
1Bh	CCPR2L	Capture/Compare/PWM Register2 (LSB)								xxxx xxxx	uuuu uuuu
1Ch	CCPR2H	Capture/Compare/PWM Register2 (MSB)								xxxx xxxx	uuuu uuuu
1Dh	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PWM and Timer2.
Note 1: Bits PSPIE and PSPIF are reserved on the PIC16F873/876; always maintain these bits clear.

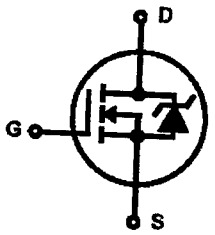
DATA SHEET FOR IRF540
28A, 100V, 0.077 Ohm, N-Channel Power MOSFETs

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Features

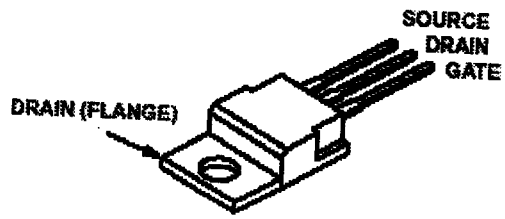
- 28A, 100V
- rDS(ON) = 0.077
- Single Pulse Avalanche Energy Rated
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Symbol



Packaging

JEDEC TO-220AB



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		IRF540, RF1S540SM	UNITS
Drain to Source Breakdown Voltage (Note 1)	V_{DS}	100	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	100	V
Continuous Drain Current			
$T_C = 100^oC$	I_D	28	A
Pulsed Drain Current (Note 3)	I_D	20	A
Gate to Source Voltage	I_{DM}	110	A
Maximum Power Dissipation	V_{GS}	±20	V
Dissipation Derating Factor	P_D	120	W
Single Pulse Avalanche Energy Rating (Note 4)		0.8	W/°C
Operating and Storage Temperature	E_{AS}	230	mJ
Maximum Temperature for Soldering	T_J, T_{STG}	-55 to 175	°C
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	°C
Package Body for 10s, See Techbrief 334	T_{pkg}	260	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to $T_J = 150^oC$.