DIGITIZED INDUSTRIAL MONITORING THROUGH POWER LINE COMMUNICATION

PROJECT REPORT

P_1143

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In partial fulfilment of the requirements for the Award of the degree of BACHELOR OF ENGINEERING in ELECTRICAL AND ELECTRONICS ENGINEERING Branch of BHARATHIAR UNIVERSITY, COIMBATORE.

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

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CERTIFICATE

This is to certify that the project report entitled

DIGITIZED INDUSTRIAL MONITORING THROUGH POWER LINE COMMUNICATION

Is the bonafide work done by

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We would be failing in our duty if we don't express our indebtedness to all our teachers in the Department of Electrical and Electronics Engineering for their suggestions and constant encouragement. We would also like to thank the non-teaching staffs and our friends for their timely help, big and small alike that culminated as good in the end.

SYNOPSIS

Power Line Communications refers to the use of existing electricity cable infrastructure to carry voice and data signals e.g. Internet, telephony, video etc.

Power Line Communications works by transmitting **high frequency digitised data signals** through the same power cable network used for carrying electricity power to household users. Such signal cannot pass through a transformer. This requires devices ("outdoor devices") that combine the voice and data signals with the low-voltage supply current in the local transformer stations to bridge the last mile. In the house, "indoor devices" (modems) are used in order to filter out the voice and data signals and to feed them to the various applications (e.g. PC/Internet, telephone, etc.).

The technology has been around for a while and at a low bandwidth. It has been used by power utilities for simple telemetering and control of electrical equipment in their networks. What is new is the integration of activities outside the building with those inside the building at a much higher bandwidth, 2.5Mbps or higher – this means voice and data transmission via the mains supply voltage network right through to every power socket in the building, as well as in the reverse direction at high speed.

CONTENTS

CHAPTER 1

INTRODUCTION

" Genius is one percent inspiration and ninety nine percent perspiration "

- Thomas Alva Edison

Engineering is all about persistent implementation of what a person perceives from his surroundings and is perhaps the most fruitful path for a person with penchant to enhance his life's standards as well as his surroundings.

Time stands as the testimony for all the inventions and discoveries made by man, which were all fuelled by the desire to make living more comfortable.

1.1 AIM OF THE PROJECT

When the distances involved are large, it will not be economical to provide separate wires for communication purposes. In fact, for such large distances, the power line themselves provide a very good medium of transmission of information. Hence we have combined the various advantages of both **Power Line Communication** and **Digital Technology** for the purpose of controlling various parameters of an industry.

1.2 PROJECT OVERVIEW

Our project involves the use of the concept of **Power Line Communication** to transmit digitized control signals in and around an industrial area to regulate and monitor various parameters, thus enabling us to obviate the need of a separate dedicated data carrying network.

We have taken **Temperature** as the parameter of consideration in the working model of our project. The use of PLC technology as an access technology to deliver broadband capabilities has several key benefits, mainly related to the fact that power wires are already installed in any location here information could be delivered.

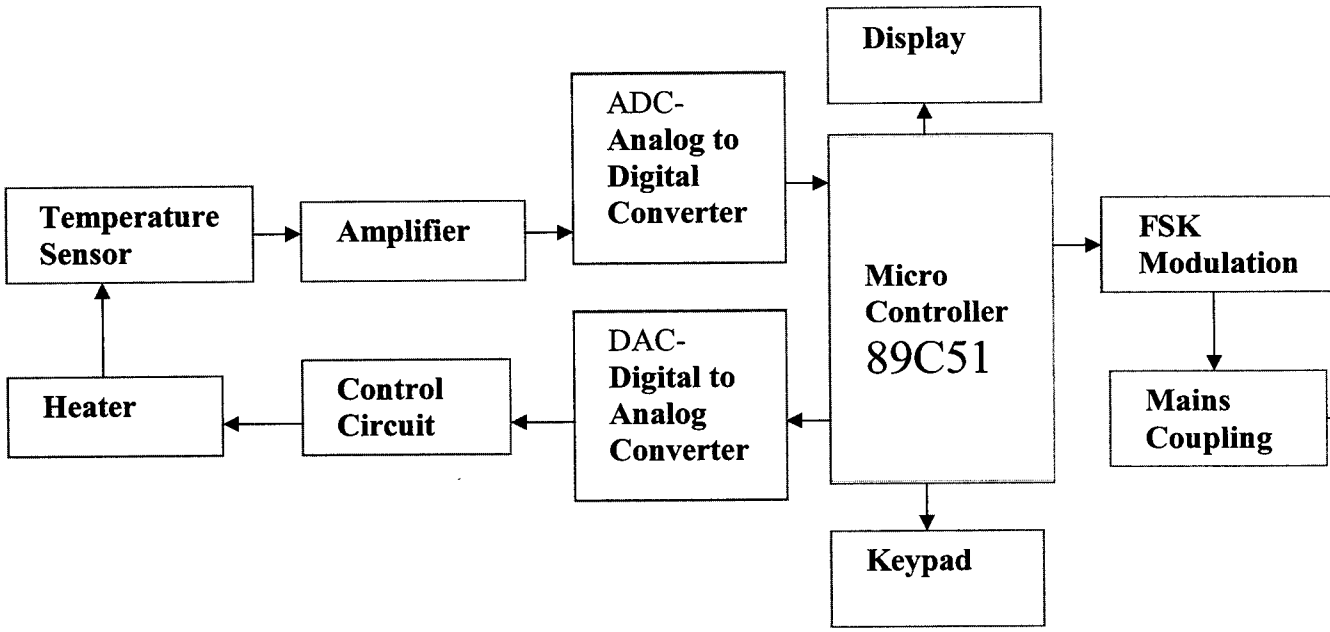
Therefore, no extra wires are required, neither in the house nor in the utility, and the user is not restricted to a few outlets in the house or industry, as is usually the case. One may note that even if it is desired to use a wireless network within a building, this reduces to a simple matter of plugging the base station into any power socket.

We can foresee the tremendous impact on a wider spectrum of applications in existing infrastructure such as traffic lights, information panels, metering systems, to vending machines and of course for home networking and **Industrial Automation**.

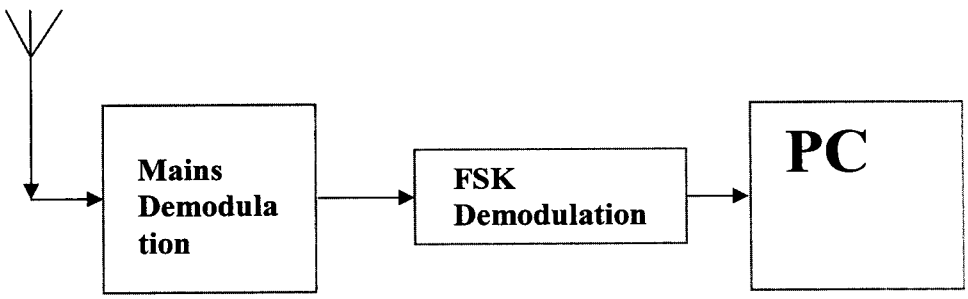
CHAPTER 2

HARDWARE DESCRIPTION

2.1 BLOCK DIAGRAM



...TRANSMITTER SECTION...



...RECEIVER SECTION...

2.2 TEMPERATURE SENSOR

A thermistor is an electronic component that exhibits a large change in resistance with a change in its body temperature. The word **"thermistor"** is actually a contraction of the words "thermal resistor". The thermistors that we shall describe herein are ceramic semiconductors and have either large positive temperature coefficient of resistance (PTC devices) or large negative temperature coefficient of resistance (NTC devices).

Both types of thermistors (PTC and NTC) have definite features and advantages, which make them ideal for certain sensor applications. Manufactured from the oxides of the transition metals - manganese, cobalt, copper and nickel, NTC thermistors are temperature dependant semiconductor resistors. Operating over a range of -200°C to + 1000°C, they are supplied in glass bead, disc, chips and probe formats. NTC's should be chosen when a continuous change of resistance is required over a wide temperature range. They offer mechanical, thermal and electrical stability, together with a high degree of sensitivity.

The thermistor we have selected is of the type NTC with a temperature range of 0-150 degree centigrade.

2.3 CONTROL CIRCUIT – TRIAC

The triac is a semiconductor device that can, once triggered, conduct current in the forward as well as in the reverse direction. This makes them useful for AC or mains power control. The main reason of popularity of a triac is its capability to conduct and control current in both directions, Like the SCR, the triac also has three electrodes but they are called as main terminal No.1, main terminal No.2 and gate.

The triac also exhibits the same forward blocking and forward conducting characteristics of an SCR; but for either polarity of the voltage applied to the main terminal. The triac can thus be called a bi-directional Thyristor, like the SCR. The break over voltage of the triac can be controlled or varied by application of a positive or negative current pulse or to the gate electrode. As the amplitude of the current pulse is increased, the break over point of the triac is decreased. The triac can be thus considered as two SCRs connected back to back in parallel.

TRIGGERING CHARACTERISTICS:

The magnitude of gate current and voltage required to trigger a Thyristor varies inversely with junction temperature. As the junction temperature increases the level of gate signal required to trigger the Thyristor becomes smaller. Worst-case triggering conditions occur,

The GATE-NON TRIGGER VOLTAGE V_{gnt} is the maximum dc gate voltage that may be applied between gate and cathode of the Thyristor for which the device can maintain its rated blocking voltage. This voltage is usually specified at the rated operating temperature of a Thyristor. Noise signals in the gate circuit should be maintained below this level to prevent in wanted triggering of the Thyristor.

When very precise triggering of a Thyristor is desired, the Thyristor gate must be overdriven by a pulse of current much larger than the dc gate current required to trigger the devoice. The use of large current pulse reduces variations in turn-on time, minimizes the effect of temperature variation on triggering characteristics and makes possible very short switching times.

The triac can be triggered in any of four operating modes, as shown in table 1. The quadrant designations refer to the operating quadrant on the principal voltage-current characteristics.

TABLE I TRIAC TRIGERRING MODES

Gate-Mains Terminal No.1 Voltage	**Mains Terminal No.2 to Mains terminal No.1 Voltage**	**Operating quadrant**
Positive	...Positive	**...I (+)**
Negative	... Positive	**...I (-)**
Positive	...Negative	**...III (+)**
Negative	...Negative	**...III (-)**

GATE TRIGGER CIRCUITS

The gate signal used to trigger an SCR or a triac must be of sufficient strength to assure sustained forward conduction. Triggering requirements are usually stated in terms of dc voltage and current. Because it is common practice to pulse-fire thyristors, it is also necessary to consider the duration of firing pulse required. A trigger pulse that has amplitude just equivalent to the dc requirements must be applied for a relatively long period of time (approximately 30 micro seconds) to ensure that the gate signal is provided during the full turn-on period of the Thyristor. As the amplitude of the gate-triggering signal is increased, the turn-on time of the Thyristor is decreased and the width of the gate pulse may be reduced. When highly inductive loads are used, the inductance controls the current-rise portion of the turn-on time. For this type of load, the width of the gate pulse must be made long enough to assure that the principal current rises to a value greater than the latching-current level of the device. The application usually determines whether a simple or somewhat sophisticated triggering circuit should be used to trigger a given triac. The angle of conduction depends on the value of resistor and capacitor.

The simplest method of phase control for a triac is similar to that for and SCR .The gate trigger voltage can be more closely controlled by use of a variety of speed triggering devices, including diacs, neon bulbs, unijunction transistors, etc.

HOLDING AND LATCHING CURRENTS

After a triac has been switched to the ON state, a certain minimum value of anode current is required to maintain it in this low impedance state. If the anode current is reduced below this critical holding current value, the triac cannot maintain regeneration and reverts to the OFF state. The holding current (I_H) is sensitive to changes with temperature (increases with decrease of temperature). It is specified at room temperature with gate open.

The latching current rating of a triac specifies a value of anode current, slightly higher than the holding current, which is the minimum amount required to sustain conduction immediately after the triac is switched from the OFF state to the ON state and the gate signal is removed. Once the latching current (1_C) is reached, the Thyristor remains in the ON state until its anode current is decreased below the holding current value. The I_Z rating is an important consideration when a triac is to be used with an inductive load because the inductance limits the rate of rise of the anode current.

The uses of the triac can be conveniently divided according to the type of firing circuit employed; some of these are described below. Many other verities are used in specialized appliances.

2.4 ADC 0809

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

The features of ADC 0809:

- High speed
- High accuracy
- Minimal temperature dependence
- Excellent long term accuracy and repeatability
- Consume minimal power

These features make this device ideally suited to applications from process and machine control to consumer and automotive applications.

2.5 DAC 0800

The DAC 0800 series are monolithic 8-bit high speed current output digital to analog converter (DAC) featuring typical setting time of 100ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible.

The features of DAC 0800:

- Fast setting output current.
- Full scale error.
- Non linearity over temperature.
- High output compliance ±10V to +18V.
- Complementary current outputs.
- Interface directly with TL, CMOS, PMOS, and others.
- Wide power supply range ±4.5V to ±18V.
- Low power consumption 33mW to ±5V.
- Low cost.

2.6 TRANSMITTER SECTION

The temperature of the system is sensed by the thermistor and is amplified and fed to the micro controller using an ADC, from where it is then given to the FSK generator XR-2206. This data is then transmitted through mains modulation to a remote PC for monitoring.

FSK GENERATOR

In digital data communication, shifting a carrier frequency between two preset frequencies transmits binary code. This type of transmission is called frequency shift keying technique. A 555 timer in astable mode can be used to generate FSK signals. When the input is high, transistor Q is cutoff and 555 timer works in the normal astable mode of operation. The frequency of the output waveform is given by

$$F0 = 1.45/(RA+2RB)\ C$$

When the input is low Q goes on and connects the resistance RC across Ra. The output frequency is given by

$$F0 = 1.45/\ ((RA||RC)+2RB)\ C$$

The resistance is used to get the desired output frequency.

transmitting digital data over telecommunications links. In order to use FSK a modulator-demodulator (modem) is needed to translate digital 1's and 0's into their respective frequencies and back again. In FSK modulation, the carrier frequency is shifted in steps (or) levels corresponding to the levels of the digital modulating signal. In case of binary signal, two carrier frequencies are used; one was corresponding to binary '0' and another to binary '1'.

MODULATION

The purpose of a communication is the source and user being physically separate from each other. To do this, the transmitter modifies the message signal into a suitable form for transmission over the channel. This modification is achieved by a process known as modulation, which involves varying some parameters of a carrier wave in accordance with the message signal. The receiver recreates the original message signal from a degraded version of the transmitted signal after propagation through the channel. A process known as demodulation, which is a reverse process of modulation used in the transmitter, achieves the recreation. However owing to the unavoidable presence of noise and distortion in the received signal, we find that the receiver cannot recreate the original message signal exactly. The type of modulation scheme used influences the resulting degradation in the overall system performance. Specifically we find that some modulation schemes are less sensitive to the effects of noise and distortion than

TYPES OF MODULATION

There are basically two types of modulation

1. Frequency modulation
2. Amplitude modulation

Frequency Modulation

In frequency modulation the amplitude of the modulated carrier is made constant whereas the frequency is varied in accordance with the variation in modulation signal. It has an infinite bandwidth with side bands distributed symmetrically about the carrier frequency. Here the total transmitted power is always remains constant, but with increase in depth of modulation the bandwidth can be increased. The advantages of FM are low noise, less channel interference, and many transmitters as the frequency can be used.

Even though frequency modulation is advantageous over amplitude modulation, in our circuit we are using AM since it occupies less bandwidth than FM. Moreover the FM transmitting and receiving equipment is more complex and hence more expensive.

Amplitude Modulation

The amplitude of the carrier wave is varied in accordance with the amplitude of the modulating signal. Consider a sinusoidal carrier

defined by,

$$C(t) = Ac \cos(2*Pi*Fc*t+\square)$$

Where Ac is the carrier amplitude and Fc is the carrier frequency. We have assumed that the phase of the carrier wave is zero for specification of the message. The source of the carrier wave c (t) is physically independent of the source responsible for generating m (t). An amplitude-modulated wave may thus describe, in its most general form, as a function of time.

In the circuit shown, Schmitt trigger NAND gate CD4011 is used. The carrier frequency is generated using the ceramic filter of value 10.7 MHz. The resistor R1 and R2 provide the necessary biasing. The modulated output is than transmitted through the antenna after passing through a capacitor. The antenna used is of aerial type. In our project the transmitted frequency is 5.5 MHz. The maximum distance to which we can transmit is around 30ft to 40ft. the distance to which it can be transmitted can be improved further by providing some amplification at the output of the amplitude modulation circuit.

IC XR – 2206

GENRAL DESCRIPTION

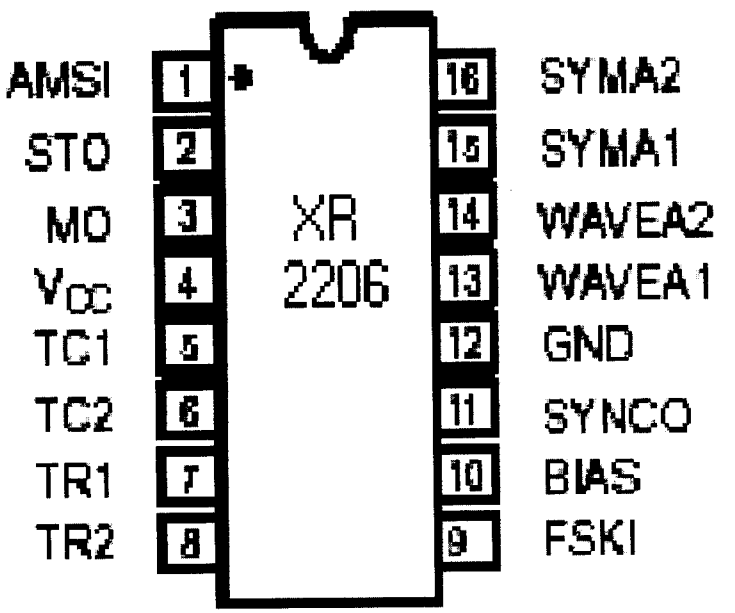
The XR-2206 is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp, and pulse waveforms of high-stability and accuracy. The output waveforms can be both amplitude and frequency modulated by an external voltage. Frequency of operation can be selected externally over a range of .01Hz to more than 1MHz.

The circuit is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, AM, FM, or FSK generation. It has a typical drift specification of 20ppm/°C. The oscillator frequency can be linearly swept over a 2000:1 frequency range with an external control voltage, while maintaining low distortion.

FEATURES

- Low-Sine Wave Distortion, 0.5%, Typical
- Excellent Temperature Stability, 20ppm/°C,
- Wide Sweep Range, 2000:1, Typical
- Low-Supply Sensitivity, 0.01%V
- Linear Amplitude Modulation
- TTL Compatible FSK Controls
- Wide Supply Range, 10V to 26V
- Adjustable Duty Cycle, 1% TO 99%

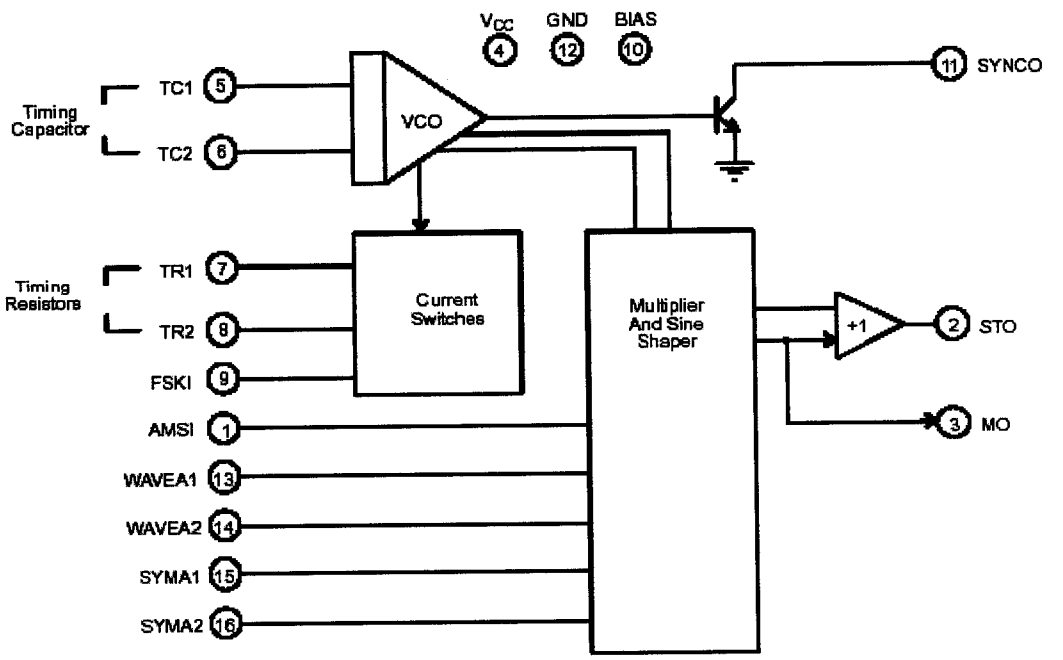
PIN DIAGRAM



PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	AMSI	I	**Amplitude Modulating Signal Input.**
2	STO	O	**Sine or Triangle Wave Output.**
3	MO	O	**Multiplier Output.**
4	V_{CC}		**Positive Power Supply.**
5	TC1	I	**Timing Capacitor Input.**
6	TC2	I	**Timing Capacitor Input.**
7	TR1	O	**Timing Resistor 1 Output.**
8	TR2	O	**Timing Resistor 2 Output.**
9	FSKI	I	**Frequency Shift Keying Input.**
10	BIAS	O	**Internal Voltage Reference.**
11	SYNCO	O	**Sync Output.** This output is a open collector and needs a pull up resistor to V_{CC}.
12	GND		**Ground pin.**
13	WAVEA1	I	**Wave Form Adjust Input 1.**
14	WAVEA2	I	**Wave Form Adjust Input 2.**
15	SYMA1	I	**Wave Symetry Adjust 1.**
16	SYMA2	I	**Wave Symetry Adjust 2.**

BLOCK DIAGRAM OF XR-2206



CIRCUIT DESCRIPTION

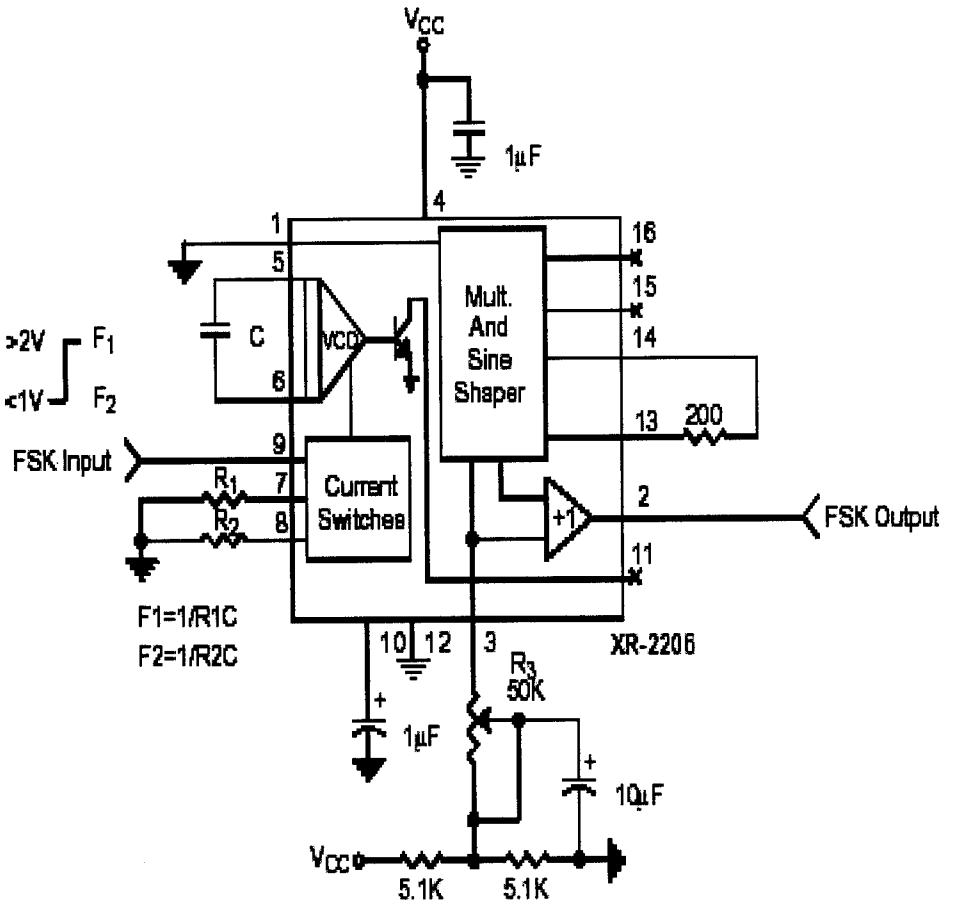
The XR-2206 is comprised of four functional blocks, a voltage-controlled oscillator (VCO), an analog multiplier and sine-shaper; a unity gain buffer amplifier; and a set of current switches. The VCO produces an output frequency proportional to an input current, which is set by a resistor from the timing terminals to ground. With two timing pins, two discrete output frequencies can be independently produced for FSK generation applications by using the FSK input control pin. This input controls the current switches, which select one of the timing resistor currents, and routes it to the VCO.

FREQUENCY SHIFT KEYING

The XR-2206 can be operated with two separate timing resistors, R1 and R2, connected to the timing Pin 7 and 8, respectively, as shown in Figure. Depending on the polarity of the logic signal at Pin 9, either one or the other of these timing resistors is activated. If Pin 9 is open-circuited or connected to a bias voltage • 2V, only R1 is activated. Similarly, if the voltage level at Pin 9 is • 1V, only R2 is activated. Thus, the output frequency can be keyed between two levels, f1 and f2, as

f1 = 1/R1C and f2 = 1/R2C. For split-supply operation, the keying voltage at Pin 9 is referenced to V-.

FSK GENERATOR



FSK GENERATOR

Mark and space frequencies can be independently adjusted by the choice of timing resistors, R1 and R2; the output is phase-continuous during transitions. The pin 9 FSK input terminal of the XR-2206 can also be used to provide the

as shown in figure. Here, a keying or pulse waveform is fed directly to pin 9, and the circuit action is such that when this keying waveform is greater then + 2 V relative to the negative supply rail pin 7's

R1 timing resistor is selected, but when the keying waveform is below +1b V (relative to the negative supply rail) pin 8's R2 timing resistor is selected instead. The FSK signal thus enables either of two operating tones to be selected.

APPLICATIONS

* Waveform Generation
* Sweep Generation
* AM/FM Generation
* V/F Conversion
* FSK Generation
* Phase-Locked Loops (VCO)

2.7 RECEIVER SECTION

The part of telecommunication system that converts transmitted waves into a desired form of output .A complete apparatus for the reception of incoming electrically transmitted messages, signals, etc.

FET AMPLIFIERS

Field Effect transistor is a semiconductor device in which current is controlled by an electric field. In the conventional transistor the operation depends on the flow of carriers of both types namely electrons and holes. The operation of FET depends on the flow of majority carriers only. Hence FET is a unipolar device. It has an advantage of high input impedance.

FILTERS

The filters are used to obtain the desired band of frequency and to suppress the unwanted signals and noise. Filters are of different types. But the ceramic filters are most commonly used for carrier frequency generation and band selection. The ceramic filters are used because of their accurate frequency tuning.

THREE TERMINAL CERAMIC FILTERS

The terminal ceramic filters are used in the transmitter and

desired band of frequencies. It is also used to suppress the unwanted signals and noise from the received signal. A 5.5 MHz ceramic filter is used in this project to generate the carrier frequency in the transmitter side. The same filter is used in the receiver side to obtain the desired band of frequency from the received signal.

DEMODULATION

The process of recovering the original modulation signal from a modulated wave is termed as demodulation or detection. Basically, the demodulation or detection is a process of frequency translation that requires a non-linear device in which the signal lying at a higher frequency in the frequency spectrum are converted to a lower frequency converter circuits are also termed as detectors.

PHASE-LOCKED LOOPS

INTRODUCTION

The phase locked loop (PLL) is an important building block of linear systems. Electronic phase locked loop (PLL) came into vogue in the 1930's when it was used for radar synchronization and communication applications. The high cost of realizing PLL, in discrete form limited its use earlier. Now with the advanced IC technology, PLL's are available as inexpensive monolithic IC's. This technique for electronic frequency control is used today in satellite communication systems, computers, and etc. The basic principle of PLL, different IC's

Basic Principle

The feedback system consists of,

1. Phase detector/comparator.

2. A low pass filter.

3. An error amplifier.

4. A Voltage Controlled Oscillator.

The VCO is a free running multivibrator and operates at a set frequency f0 called free running frequency. An external timing capacitor and an external resistor determine this frequency. It can also be shifted to either side by applying a dc control voltage Vc to an appropriate terminal of the IC. The frequency deviation is directly proportion to the dc control voltage and hence it is called a "Voltage controlled Oscillator" or, in short VCO. If an input signal Vs of frequency fs is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output V0 of the VCO.If the two signals differ in frequency and/or phase, an error voltage Ve is generated. The phase detector is basically a multiplier and produced the sum (fs+f0) and difference (fs-f0) components at its output. The high frequency component (fs+f0) is removed by the low pass filter and the difference frequency component is amplified and then applied as control voltage Vc to VCO.The signal Vc shifts the VCO frequency in a direction to reduce the frequency difference between fs and f0.

Once this action starts, we say that the signal is in the capture range. The VCO continues to change frequency. The circuit is then said to be locked. Once locked, the output frequency f0 of VCO is

identical to fs except for a finite phase difference f. This phase difference f generated a corrective control voltage Vc to shift the VCO frequency from f0 to fs and thereby maintain the lock. Once locked, PLL tracks the frequency changes of the input signal.

Thus, a PLL goes through three stages,

(i) Free running,

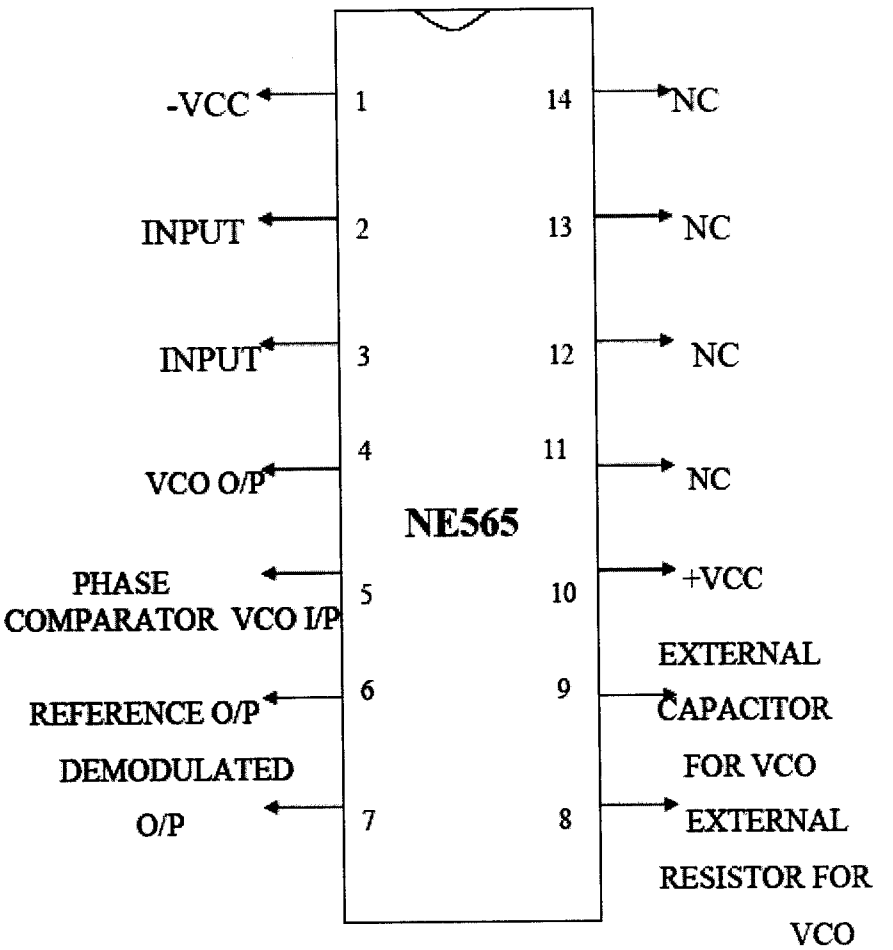
(ii) Capture, and

(iii) Locked or tracking.

As capture starts, a small sine wave appears. This is due to the frequency difference between the VCO and the input signal. The dc component of the beat drives the VCO towards the lock. Each successive cycle causes the VCO frequency to move closer to the input signal frequency. The frequency difference becomes smaller and the filter, shifting the VCO frequency further, passes a larger dc component.

The process continues until the VCO locks on to the signal and the difference frequency is dc. The low pass filter controls the capture range. If VCO frequency is far away, the beat frequency will be too high to pass through the filter and the PLL will not respond. We say that the signal is out of the capture band. However, once locked, the filter no longer restricts the PLL.The VCO can track the signal well beyond the capture band. Thus tracking range is always larger than the capture range.

PIN DIAGRAM:


-VCC
1
INPUT
2
INPUT
3
VCO O/P
4
PHASE COMPARATOR VCO I/P
5
REFERENCE O/P
6
DEMODULATED O/P
7
NE565
14
NC
13
NC
12
NC
11
NC
10
+VCC
9
EXTERNAL CAPACITOR FOR VCO
8
EXTERNAL RESISTOR FOR VCO

IC PLL 565

The phase detector of this PLL is comprised of differential amplifier pairs provided with current sink bias source. The output voltage phase detector is limited by diodes to maximum of +0.7V. This limiting action helps to minimize the effect of high amplitude noise pulses and other transient effects on the operation of the PLL.

The phase detector has a balanced output and is supplied to the differential amplifier pair, which serves an amplifier stage in amplifying the phase detector; output a single ended output is taken from this stage from across the load resistor R1 and connected internally to the VCO. Connection of an external capacitor C between Pin 7 and ground will produce a first order low-pass (lag) network. A capacitor C and a resistor R2 connected in series between pin 7 and ground will result in lag lead network. The VCO consists of a voltage controlled current source, which supplies equal magnitude of charging and discharging currents to an externally connected (pin 9) timing capacitor C0. A timing resistor is connected between pin8 and positive power supply.

The rest of the VCO circuit is Schmitt trigger with a differential amplifier output circuit. This controls the turn-on and turn-off for the switching action of the current source for the charging and discharging.

ENVELOPE DETECTOR

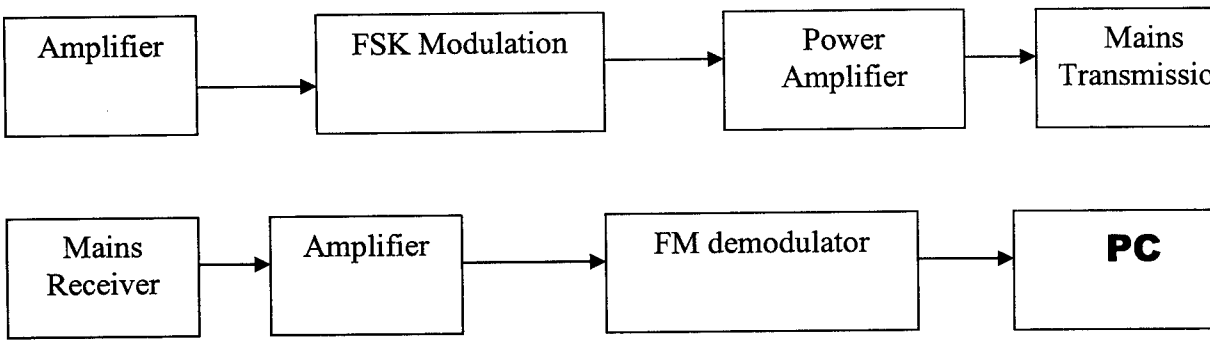
An envelope detector is a simple and yet highly effective device that is well suited for the demodulation of a narrow band AM wave, for which the percentage modulation is less than 100%. Ideally, an envelope detector produces an output signal that follows the envelope of the input signal waveform. Envelope detector consists of a diode and a resistor-capacitor filter. The operation is as follows. On the positive half-cycle of the input signal, the diode is forward-biased and the capacitor C charges up rapidly to the peak value of the input signal. When the input signal falls below this value, the diode becomes reverse biased and the capacitor C discharges slowly to the load resistor RI. The discharging process continues until the next positive half cycle. When the input signal becomes greater than the voltage across the capacitor, the diode conducts again and the process is repeated. Thus the demodulation is carried out. In our circuit we are using 0A79 diode.

In digital data communication and computer peripheral, binary data is transmitted by means of a carrier frequency, which is shifted between two preset frequencies. This type of data transmission is called frequency shift keying (FSK) technique. The binary data can be retrieved using FSK demodulators at the receiving end. The 565 PLL is a very useful as a FSK demodulator. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two

three-stage filter removed the carrier component and the output signal is made logic compatible by the voltage comparator.

2.8 MAINS COMMUNICATION

BLOCK DIAGRAM



BLOCK DIAGRAM EXPLANATION

It uses a mini transmitter to generate a carrier frequency, which can be varied between 70 KHz to 500 KHz. The carrier frequency is frequency modulated. Frequency modulation is characterized by a narrow bandwidth. This narrow bandwidth has the advantage that a large number of channels can be accommodated on a single pair of lines, without causing interference between them.

A frequency separation of 5 KHz between the channels is considered adequate. The signals are first amplified, limited and filtered to get rid of noise and other interfacing signals and then used to frequency modulate an oscillator. After amplification the FM signal is fed into the mains wires via an isolation transformer. Signals transmitted from other stations are picked by the transformer and fed to the receiver section. After amplification, the received signal is demodulated.

TRANSMITTER

The signals are first amplified by the transistor stage. A clipper consisting of the differential stage consisting of two transistor stages follows this stage. The purpose of the clipper is to limit the bandwidth of the outgoing signal to 15 KHz. The clipper is followed by a low pass filter, which ensures that only the signals having the bandwidth 15 KHz pass through the next stage. The resulting signal is fed to the FSK generator.

The frequency range of this FSK generator is between 70 KHz and 500 KHz. The output obtained modulates the frequency of the oscillator. This is frequency modulation. The frequency modulated oscillator signal is then further amplified by the transistor stages. This last stage of amplification is used to drive the power output stage. The power transistor should be fitted with an adequate heat sink. This

output stage is operated in the wide band mode i.e. no tuning is provided for this stage.

RECEIVER

The receiver consists of PLL and AF amplifier. The PLL (Phase Locked Loop) is the most important part of the receiver. Incoming signals are fed via the isolation transformer to the input of the receiver. The output of transmitter and the receiver input are thus connected directly to one another. The receiver input is un-tuned which gives it broadband characteristics. However the PLL characteristic make the receiver selective enough to respond to a specific frequency. The signals is then demodulated using a phase locked loop i.e. the receiver will deliver an output only when the PLL is locked in.

This operation is achieved by employing the IC567, which contains

i) Decoder

ii) PLL

iii) Phase detector

iv) Comparator

v) Driver amplifier with open collector.

The PLL works in conjunction with a VCO, which is built inside the IC 567. The free running frequency of the PLL VCO is adjusted by means of potentiometer. When the received signal is within the capture

locked in there is a sharp increase in DC output voltage of the detector. The amplifier and output driver transistor stage into a logic stage convert this voltage. Taking the LF signal as the control voltage demodulates the FM input signal. If the input frequency band is outside the capture range of the PLL, the PLL will not lock in and the low frequency signal at the output will be suppressed.

POWER SUPPLY

This unit needs two separate sources of DC power supply. A voltage of 7.5 Volts is needed for all the stages except for the output stage of the transmitter and the AF amplifier stage in the receiver which requires a 24 Volt supply.

2.9 RS-232C SERIAL DATA STANDARD

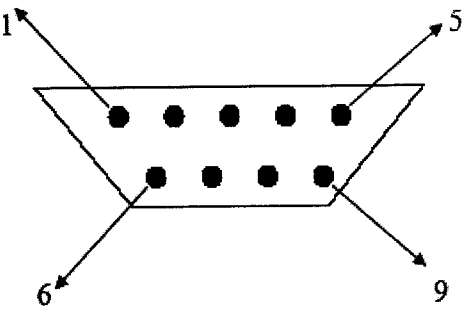
In the 1960s as the use of time-share computer terminals became more widespread, modems were developed so that terminals could use phone lines to communicate with distant computers. As we stated earlier, modems and other devices used to send serial data are often referred to as data communication equipment or DCE. The terminals or computers that are sending or receiving the data are referred to as data terminal equipment or DTE. In response to the need

Electronic Industries Association (EIA) developed EIA standard RS-232C. This standard describes the functions of 25 signal and handshake pins for serial data transfer. It also describes the voltage levels. Impedance levels, rise and fall times, maximum bit rate, and maximum capacitance for these signal lines.

Before we work our way through the 25 pin functions, we will take a brief look at some of the other hardware aspects of RS-232C. RS-232C specifies 25 signal pins and it specifies that the DTE connector should be a male, and the DCE connector should be a female. A specific connector is not given, but the most commonly used connectors are the DB-25P male and the DB-25S female shown in figure. When you are wiring up these connectors. It is important to note the order in which the pins are numbered. The voltage levels for all RS-232C signals are as follows. A logic high, or mark, is a voltage between –3V and –15 V under load (-25 V no load). A logic low or space is a voltage between +3 V and +15 under load (+25 V no load). Voltages such as ±12 V are commonly used.

The output signal level usually swings between +12V and -12V. The "dead area" between +3v and -3v is designed to absorb line noise. In the various RS-232-like definitions this dead area may vary. For instance, the definition for V.10 has a dead area from +0.3v to -0.3v. Many receivers designed for RS-232 are sensitive to differentials of 1v or less.

DB9 PIN CONNECTOR



DB9 PC signals set:

RS232 Pin Assignments	
Pin 1	Received Line Signal Detector (Data Carrier Detect)
Pin 2	Received Data
Pin 3	Transmit Data
Pin 4	Data Terminal Ready
Pin 5	Signal Ground
Pin 6	Data Set Ready
Pin 7	Request To Send
Pin 8	Clear To Send
Pin 9	Ring Indicator

PIN DESCRIPTION

1. DTR (Data terminal ready):

When the terminal is turned on, after going through a self-test, it sends out signal DTR to indicate that it is ready for communication.

2 .DSR (Data set ready):

When DCE is turned on and has gone through the self-test, it asserts DSR to indicate that it is ready to communicate.

3.RTS (Request to send):

When the DTE device (such as a pc) has a byte to transmit, it asserts RTS to signal the modem that it has a byte of data to transmit.

4. CTS (clear to send):

In response to RTS when the modem has room for storing the data it is to receive, it sends out signal CTS to the DTE (PC) to indicate that it can receive the data now.

5.DCD (data carrier detect):

The modem assert signal DCD to inform the DTE (PC) that a valid carrier has been detected and that contact between it and the other modem is established.

6.RI (ring indicator):

An output from the modem (DCE) and an input to a pc (DTE) indicates that the telephone is ringing. It goes on and off in synchronization with the ringing sound.

While signals DTR and DSR are used by the pc and modem respectively, to indicate that they are alive and well, it is RTS and CTS that actually control the flow of data. RTS and CTS are also referred to as hardware control flow signals.

This concludes the description of the 9 most important pins of the RS232 handshake signals plus TxD, RxD and ground.

2.10 POWER SUPPLY DESCRIPTION

INTRODUCTION

Power supplies are extensively used in all industrial applications. They are required to meet all or most of the following specifications:

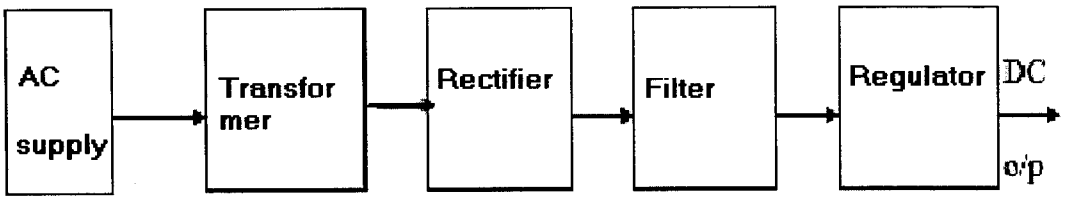
- Isolation between the source and the load.
- High power density for reduction of size and weight.
- Controlled direction of power flow.
- High conversion efficiency.
- Controlled power factor if the source is an AC voltage
- Provides regulated ripple free input and output waveforms.

CIRCUIT DESCRIPTION

Since all electronic circuits work only with low D.C.voltage we need a power supply unit to provide the appropriate voltage supply. This unit consists of transformer, rectifier, filter and regulator. A.C. voltage typically 230V rms is connected to a transformer which steps that AC voltage down to the level to the desired AC voltage. A diode rectifier then provides a full-wave rectified voltage that is initially filtered by a simple capacitor filter to produce a DC voltage. This resulting DC voltage usually has some ripple or AC voltage variations. A regulator

much less ripple voltage but also remains the same DC value even the DC voltage varies some what, or the load connected to the output DC voltages changes.

BLOCK DIAGRAM



TRANSFORMER

A transformer is a static (or stationary) piece of which electric power in one circuit is transformed into electric power of the same frequency in another circuit. It can raise or lower the voltage in a circuit but with a corresponding decrease or increase in current. It works with the principle of mutual induction. In our project we are using step down transformer for providing a necessary supply for the electronic circuits. In our project we are using a transformer with 15-0-15V center-tapped secondary.

RECTIFIER

The DC level obtained from a sinusoidal input can be improved 100% using a process called full-wave rectification. It uses 4 diodes in a bridge configuration. From the basic bridge configuration we see that two diodes (say D2 & D3) are conducting while the other two diodes (D1 & D4) are in "off" state during the period t =0 to T/2. Accordingly for he negative of the input the conducting diodes are D1 & D4. Thus the polarity across the load is the same.

FILTER

The filter circuit used here is the capacitor filter circuit where a capacitor is connected at the rectifier output, and a DC is obtained across it. The filtered waveform is essentially a DC voltage with negligible ripples, which is ultimately fed to the load.

REGULATOR

The output voltage from the capacitor is more filtered and finally regulated. The voltage regulator is a device, which maintains the output voltage constant irrespective of the change in supply variations, load variation and temperature changes. Here we use two fixed voltage regulators namely LM 7812, LM 7805 and LM7912. The IC 7812 is a +12V regulator IC 7912 is a -12V regulator and IC 7805 is a +5V regulator.

CHAPTER 3

MICROCONTROLLER ATMEL 89C51

3.1 ABOUT THE MICROCONTROLLER

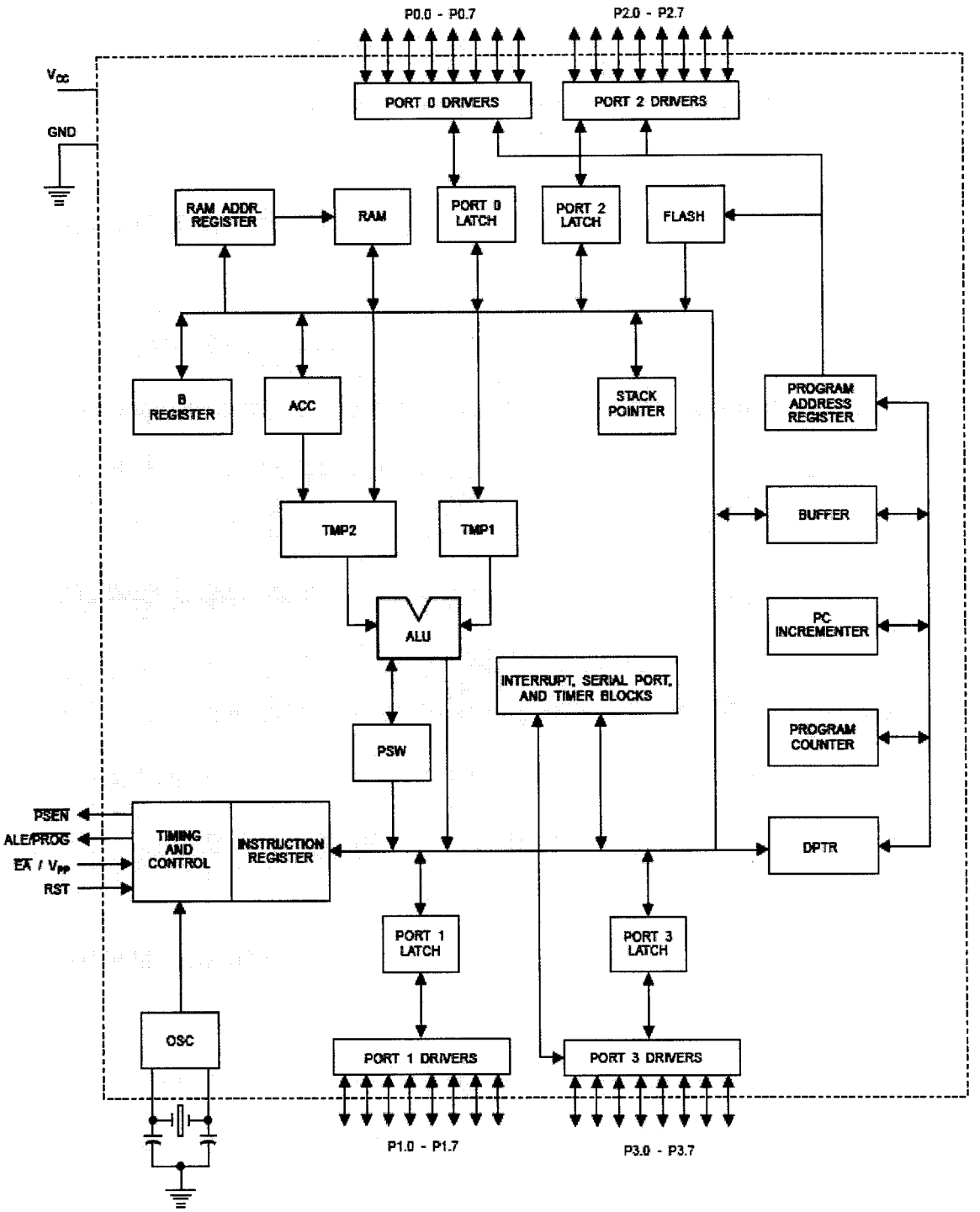
INTRODUCTION:

A Micro controller consists of a powerful CPU tightly coupled with memory (RAM, ROM or EPROM), various I / O features such as Serial ports, Parallel Ports, Timer/Counters, Interrupt Controller, Data Acquisition interfaces-Analog to Digital Converter (ADC), Digital to Analog Converter (ADC), everything integrated onto a single Silicon Chip Depending on the need and area of application for which it is designed. They are mostly used for standalone and real time applications.

A microcomputer system requires memory to store a sequence of instructions making up a program, parallel port or serial port for communicating with an external system, timer / counter for control purposes like generating time delays, Baud rate for the serial port, apart from the controlling unit called the **Central Processing Unit.**

The **MCU** is designed to operate on application-oriented sensor

ARCHITECTURE OF ATMEL 89C51:



oscillator start-up time depends on the oscillator frequency. For a 10 MHz crystal, the start-up time is typically 1ms.With the given circuit, reducing Vcc quickly to 0 causes the RST pin voltage to momentarily fall below 0V. How ever, this voltage is internally I limited and will not harm the device.

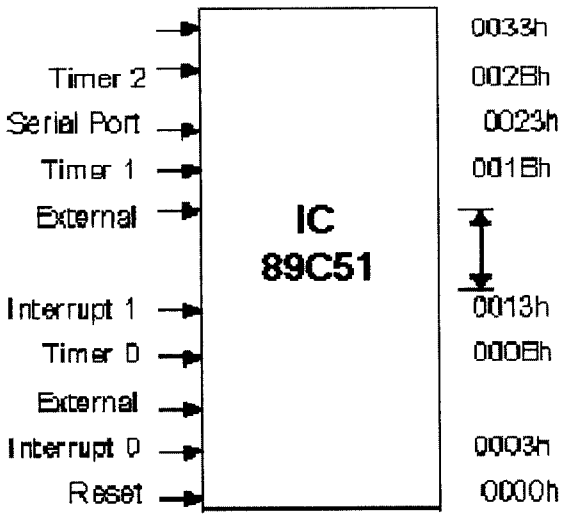
MEMORY ORGANISATION:

Logical separation of program and data memory

All ATMEL flash micro controllers have separate address spaces for program and data memory. The logical separation of the program and data memory allows the data memory to be accessed by 8 bit addresses. Which is quickly stored and manipulated by am 8 bit CPU nevertheless 16 bit data memory addresses can also be generated through the DPTR register.

Program memory can only be read. There can be up to 64K bytes of directly addressable program memory. The read strobe for external program memory is the Program Store Enable Signal (PSEN) Data memory occupies a separate address space from program memory. Up to 64K bytes of external memory can be directly addressed in the external data memory space. The CPU generates read and write signals, RD and WR, during external data memory accesses.

chip Flash, if the EA pin is strapped to Vcc, program fetches to addresses 0000h through 0FFFh are directed to internal Flash. Program fetches to addresses 1000h through FFFFh are directed to external memory.



DATA MEMORY:

The Internal Data memory is dived into three blocks namely,

- The lower 128 Bytes of Internal RAM.
- The Upper 128 Bytes of Internal RAM.
- Special Function Register.

The bit Addressable SFRs are those whose address ends in 000B. The bit addresses in this area are 80h through FFh.

ADDRESSING MODES:

There are three types of addressing. They are

- Direct addressing
- Indirect addressing
- Indexed addressing

DIRECT ADDRESSING:

In direct addressing, the operand specified by an 8-bit address field in the instruction. Only internal data RAM and SFR's can be directly addressed.

INDIRECT ADDRESSING:

In Indirect addressing, the instruction specifies a register that contains the address of the operand. Both internal and external RAM can indirectly address. The address register for 8-bit addresses can be either the Stack Pointer or R0 or R1 of the selected register Bank. The address register for 16-bit addresses can be only the 16-bit data

INDEXED ADDRESSING:

Program memory can only be accessed via indexed addressing this addressing mode is intended for reading look-up tables in program memory. A 16 bit base register (Either DPTR or the Program Counter) points to the base of the table, and the accumulator is set up with the table entry number. Adding the Accumulator data to the base pointer forms the address of the table entry in program memory.

Another type of indexed addressing is used in the "case jump" instructions. In this case the destination address of a jump instruction is computed as the sum of the base pointer and the Accumulator data.

REGISTER INSTRUCTION:

The register banks, which contains registers R0 through R7, can be accessed by instructions whose opcodes carry a 3-bit register specification. Instructions that access the registers this way make efficient use of code, since this mode eliminates an address byte. When the instruction is executed, one of four banks is selected at execution time by the row bank select bits in PSW.

REGISTER - SPECIFIC INSTRUCTION:

Some Instructions are specific to a certain register. For example some instruction always operates on the Accumulator, so no address byte is needed to point OT ir. In these cases, the opcode itself points to the correct register. Instruction that rigger to Accumulator as A assemble as Accumulator - specific Opcodes.

IMMEDIATE CONSTANTS:

The value of a constant can follow the opcode in program memory. For example- MOV A, #100 loads the Accumulator with the decimal number 100. The same number could be specified in hex digit as 64h.

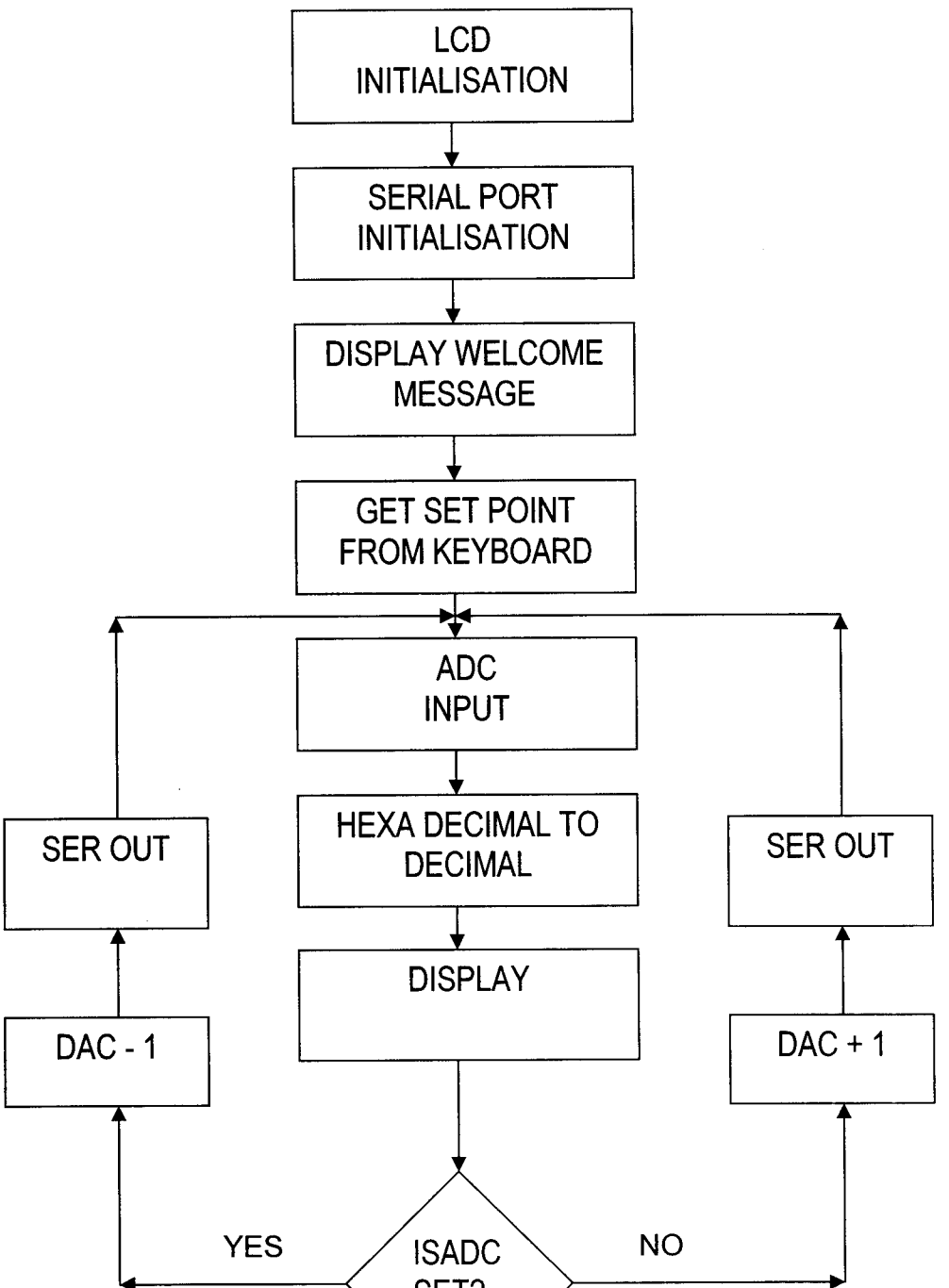
CPU TIMING:

A machine cycle consists of 6 states. Each stare is divided into a phase / half, during which the phase 1 clock is active and phase 2 half. Arithmetic and Logical operations take place during phase1 and internal register - to register transfer take place during phase 2.

CHAPTER 5

SOFTWARE DESCRIPTION

4.1 FLOWCHART REPRESENTATION



```
 }
}

void adc0()
{
 x=chan0;
 delay();
 dat=soc;
 volt1=dat;
}

void htd0()
{
 a0=volt1/0x64;
 b0=volt1%0x64;
 c0=b0/0x0a;
 d0=b0%0x0a;
}

 void dis0()
 {
  porta=0x80;
  read();
  delay();
  porta='T';
  write();
  delay();
  porta='e';
  write();
  delay();
  porta='m';
  write();
  delay();
  porta='p';
  write();
  delay();
  porta='e';
  write();
  delay();
  porta='r';
  write();
  delay();
  porta='a';
  write();
  delay();
  porta='t';
  write();
  delay();
  porta='u';
  write();
  delay();
  porta='r';
  write();
```

```
delay();
porta=' ';
write();
delay();
porta=' ';
write();
delay();
porta=' ';
write();
delay();
porta=' ';
write();
delay();
porta=' ';
write();
delay();
porta=' ';
write();
delay();
porta=' ';
write();
delay();
porta=' ';
write();
delay();

}

void control()
{
 if(volt1<idreg)
 {
  if(portb==250)
  {
  portb=250;
  goto re;
  }
  portb=portb+1;
 }
 if(volt1>idreg)
 {
  if(portb<=8)
  {
  portb=5;
  goto re;
  }
  portb=portb-1;
 }
re:
;
}

void del()
```

```
{
if(set==0)
{
keypad();
}
}
}

void delay()
{

 for(j=0x00;j<=0xfe;j++)
  {
if(set==0)
{
keypad();
}

}
}


void ser_init()
{
 TH1=0x72;
 TMOD=0x21;
 TR1=1;
 delay();
 SCON=0x58;
}

void ser_out()
{
  SBUF=volt1;
  del();
  SCON=0x58;
  del();
}

void keypad()
{
xx:
if(inc==0)
 {
  idreg=idreg+1;
  htd();
  dis1();
  del();
  goto xx;
 }
 if(dec==0)
 {
  idreg=idreg-1;
```

```
 del();
 goto xx;
}
if(ent==0)
 {
 goto yy;
}
 goto xx;
yy:
;
}
void htd()
{
 a=idreg/0x2710;
 b=idreg%0x2710;
 c=b/0x3e8;
 d=b%0x3e8;
 e=d/0x64;
 f=d%0x64;
 g=f/0x0a;
 h=f%0x0a;
}
void dis1()
{
 porta=0xc0;
 read();
 porta='S';
 write();
 porta='e';
 write();
 porta='t';
 write();
 porta=' ';
 write();
 porta='T';
 write();
 porta='e';
 write();
 porta='m';
 write();
 porta='p';
 write();
 porta=' ';
 write();
 porta=':';
 write();
 porta=a+0x30;
 write();
 porta=c+0x30;
 write();
 porta=e+0x30;
 write();
 porta=g+0x30;
```

```
 write();
 porta=' ';
 write();
 porta=' ';
 write();
 porta=' ';
 write();
 porta=' ';
 write();
 porta=' ';
 write();
}
```

4.3 FRONT END USING 'C' PROGRAM

```
#include<stdio.h>
#include<conio.h>
#include<dos.h>
void main()
{
  int data=0x00;
  char a,ch;
  clrscr();
  while(!kbhit())
  {
  _AH=0x03;
  _DX=0x01;
  geninterrupt(0x14);
  a=_AH;
  if(a&0x01==0x01)
  {
  data=inportb(0x2f8);
  gotoxy(35,12);
  textcolor(11);
  cprintf(" Temperature %3d ",data);
}
}
}
```

CHAPTER 5

TEST PROCEDURE

Our project consists of two sections, One comprising of all the control circuits and the transmitter section, the other which is the receiver section interfaced with PC. In brief this is the test procedure that we have followed with Temperature as the parameter in consideration:

First the temperature is set using the keypad controller and displayed on the LCD. We have programmed the micro controller to update the temperature after every sampling cycle. The filament of a bulb has been used for the purpose of obtaining experimental samples of the temperature. Initially the temperature in the filament of the bulb is below the set temperature, so in this case the micro controller has been programmed such that it activates the TRIAC to trigger and send additional current and increase the temperature of the filament of the bulb. The program is such that it sees to that if the temperature increases beyond the set temperature, then the current send to the filament is reduced through the TRIAC circuit.

We have also successfully monitored and displayed this temperature on the PC after every sampling cycle, using the concept of Power Line Communication. In one of our typical our experiments we have observed the following readings.

SET TEMPERATURE: 30 DEGREE CENTIGRADE

TIME (SECONDS)	FILAMENT TEMPERATURE (DEGREE CENTIGRADE)	TEMPERATURE DISPLYED IN THE PC (DEGREE CENTIGRADE)
0	27	27
40	29	29
80	30	30
120	33	33
180	31	31
230	30	30

CHAPTER 6

CONCLUSION

6.1 FUTURE EXPANSION

This project will have a pivotal role in **Industrial Automation and Monitoring** in the future when one can even go to the extent of controlling various parameters from a remote location using power line communication, especially in developing countries like India where it will prove to be a cost saving measure.

Although in our working model we have taken in to account and monitored only a single parameter namely temperature, using the same circuit one can monitor and regulate various other parameters like voltage, current etc. based on the requirements of the industry. Also by adding a **mini-exchange** one can also communicate successfully over large distances in an industry using the concept of power line communication. This will result in cost saving as no additional installation of cables necessary for voice and data transmissions is needed and one can make use of existing low voltage supply network/infrastructure.

6.2 CONCLUSION

Technology is being triggered by ineluctable needs of man and day-by-day several approaches to innovative ideas and inventions are growing with a high range of cliffhanging to make existence of common man more luxurious. We live in a communications era where the world is getting smaller and smaller and the industry demands higher transmission speed of digital signals at a lower cost. Hence power line communication will be able to meet today's industry needs as it makes use of existing electricity cable infrastructure and does not need any extra wired and wireless systems to be installed especially when the distances within an industry are large.

CHAPTER 7

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D.H. & Schilling O.L,"Principles of communication systems"


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atures

- Compatible with MCS-51™ Products
- 4 Kbytes of In-System Reprogrammable Flash Memory
  - Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-Level Program Memory Lock
- 128 x 8-Bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low Power Idle and Power Down Modes

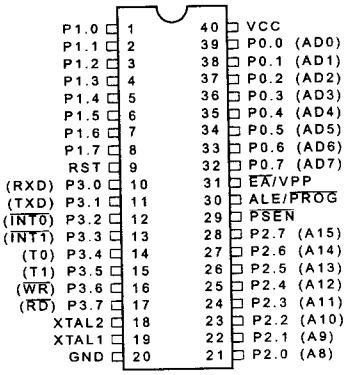
escription

e AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4 ytes of Flash Programmable and Erasable Read Only Memory (PEROM). The vice is manufactured using Atmel's high density nonvolatile memory technology d is compatible with the industry standard MCS-51™ instruction set and pinout. e on-chip Flash allows the program memory to be reprogrammed in-system or by onventional nonvolatile memory programmer. By combining a versatile 8-bit CPU h Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer ich provides a highly flexible and cost effective solution to many embedded control plications.

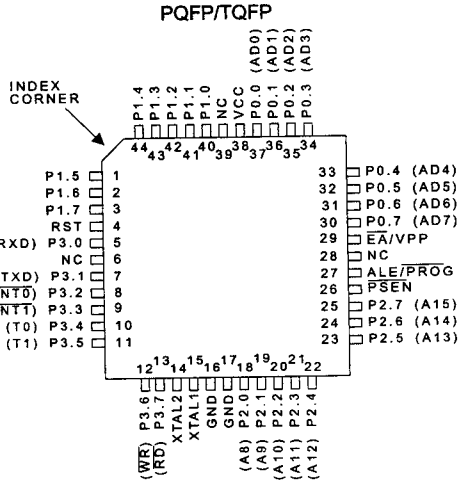
(continued)

in Configurations

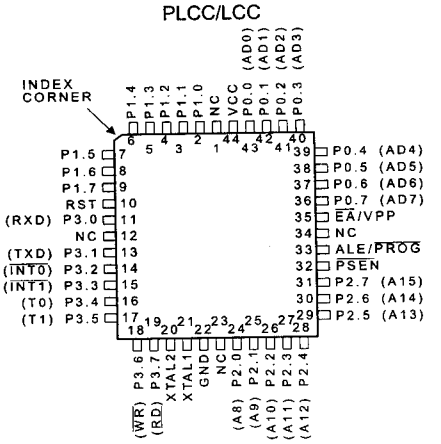
PDIP/Cerdip



PQFP/TQFP



PLCC/LCC



8-Bit Microcontroller with 4 Kbytes Flash

AT89C51

n Description (Continued)

en the AT89C51 is executing code from external pro-
m memory, PSEN is activated twice each machine cy-
except that two PSEN activations are skipped during
h access to external data memory.

VPP

ernal Access Enable. EA must be strapped to GND in
er to enable the device to fetch code from external pro-
m memory locations starting at 0000H up to FFFFH.
e, however, that if lock bit 1 is programmed, EA will be
rnally latched on reset.

should be strapped to VCC for internal program execu-
s.

s pin also receives the 12-volt programming enable
age (VPP) during Flash programming, for parts that re-
e 12-volt VPP.

AL1

ut to the inverting oscillator amplifier and input to the
rnal clock operating circuit.

AL2

put from the inverting oscillator amplifier.

scillator Characteristics

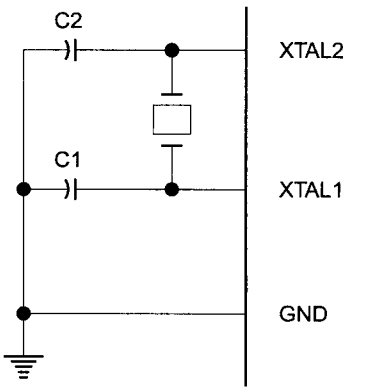
AL1 and XTAL2 are the input and output, respectively,
n inverting amplifier which can be configured for use
an on-chip oscillator, as shown in Figure 1. Either a
rtz crystal or ceramic resonator may be used. To drive
device from an external clock source, XTAL2 should
left unconnected while XTAL1 is driven as shown in
ure 2. There are no requirements on the duty cycle of
external clock signal, since the input to the internal
cking circuitry is through a divide-by-two flip-flop, but
imum and maximum voltage high and low time specifi-
ons must be observed.

e Mode

dle mode, the CPU puts itself to sleep while all the on-
p peripherals remain active. The mode is invoked by
ware. The content of the on-chip RAM and all the spe-
functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

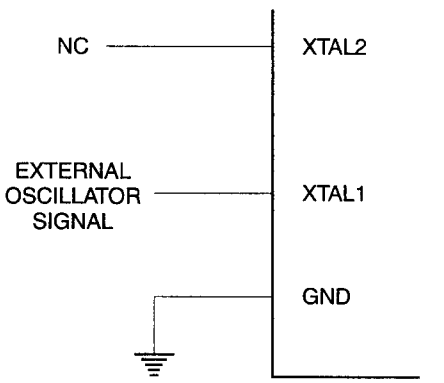
It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hard-

Figure 1. Oscillator Connections



Notes: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 2. External Clock Drive Configuration



atus of External Pins During Idle and Power Down

ode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
le	Internal	1	1	Data	Data	Data	Data
le	External	1	1	Float	Data	Address	Data
ower Down	Internal	0	0	Data	Data	Data	Data
ower Down	External	0	0	Float	Data	Data	Data

e inhibits access to internal RAM in this event, but ac- to the port pins is not inhibited. To eliminate the pos- ty of an unexpected write to a port pin when Idle is inated by reset, the instruction following the one that kes Idle should not be one that writes to a port pin or kternal memory.

wer Down Mode

e power down mode the oscillator is stopped, and the uction that invokes power down is the last instruction cuted. The on-chip RAM and Special Function Regis- retain their values until the power down mode is termi- d. The only exit from power down is a hardware reset. et redefines the SFRs but does not change the on- RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below:

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

ck Bit Protection Modes

Program Lock Bits			
LB1	LB2	LB3	Protection Type
U	U	U	No program lock features.
P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset, and further programming of the Flash is disabled.
P	P	U	Same as mode 2, also verify is disabled.
P	P	P	Same as mode 3, also external execution is disabled.

gramming the Flash

AT89C51 is normally shipped with the on-chip Flash ory array in the erased state (that is, contents = FFH) eady to be programmed. The programming interface pts either a high-voltage (12-volt) or a low-voltage) program enable signal. The low voltage program- mode provides a convenient way to program the C51 inside the user's system, while the high-voltage amming mode is compatible with conventional third Flash or EPROM programmers.

AT89C51 is shipped with either the high-voltage or oltage programming mode enabled. The respective ide marking and device signature codes are listed in llowing table.

	V_{PP} = 12 V	V_{PP} = 5 V
-Side Mark	AT89C51 xxxx yyww	AT89C51 xxxx-5 yyww
nature	(030H)=1EH (031H)=51H (032H)=FFH	(030H)=1EH (031H)=51H (032H)=05H

The AT89C51 code memory array is programmed byte-by-byte in either programming mode. *To program any non-blank byte in the on-chip Flash Memory, the entire memory must be erased using the Chip Erase Mode.*

Programming Algorithm: Before programming the AT89C51, the address, data and control signals should be set up according to the Flash programming mode table and Figures 3 and 4. To program the AT89C51, take the following steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12 V for the high-voltage programming mode.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

Data Polling: The AT89C51 features $\overline{Data}$ Polling to indicate the end of a write cycle. During a write cycle, an at-

ure 3. Programming the Flash

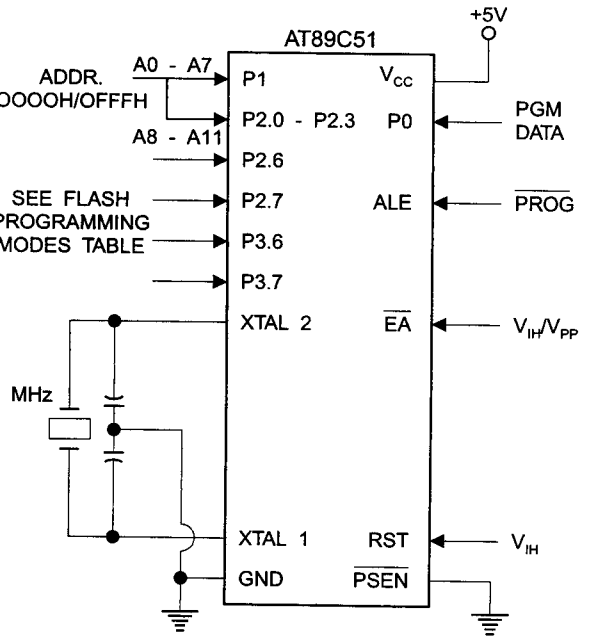
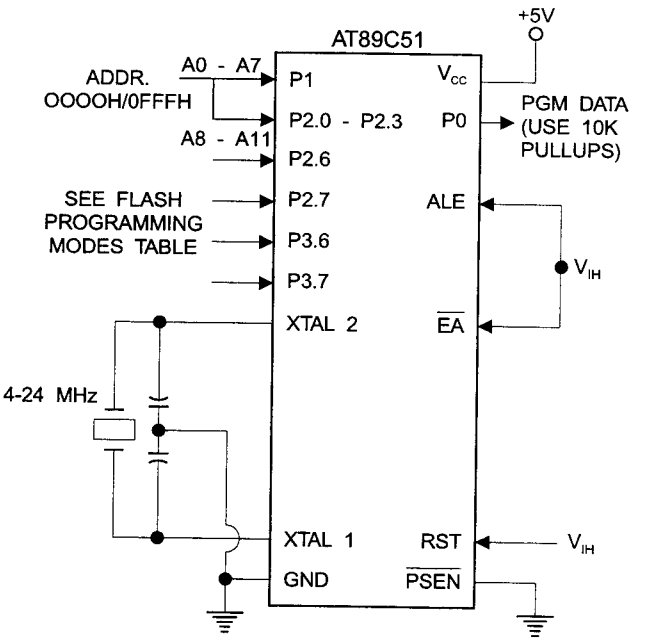


Figure 4. Verifying the Flash



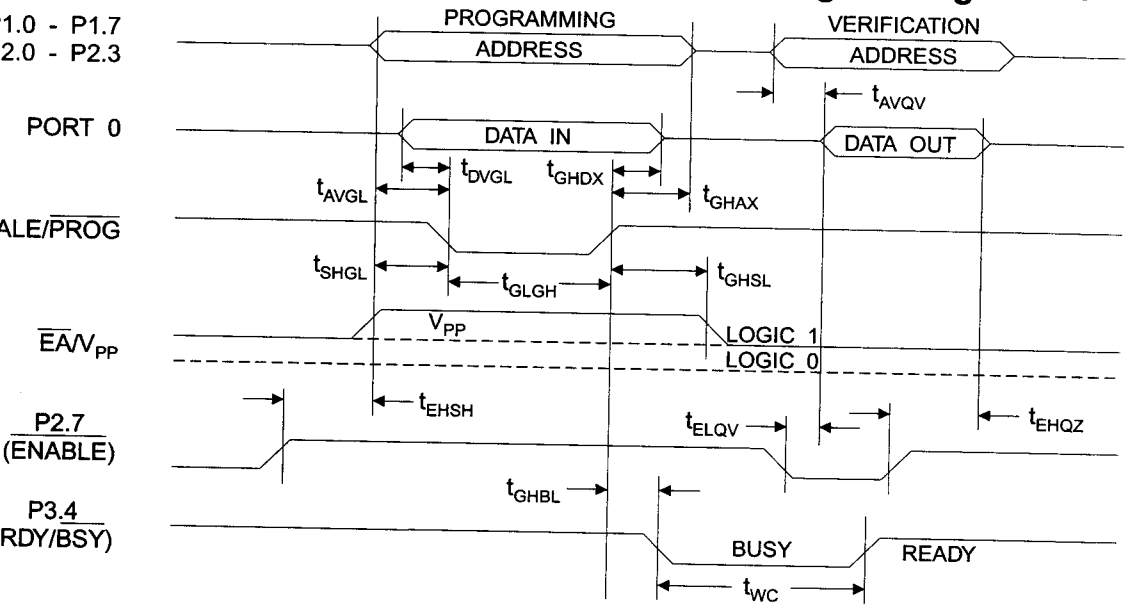
sh Programming and Verification Characteristics

21°C to 27°C, V_{CC} = 5.0 ± 10%

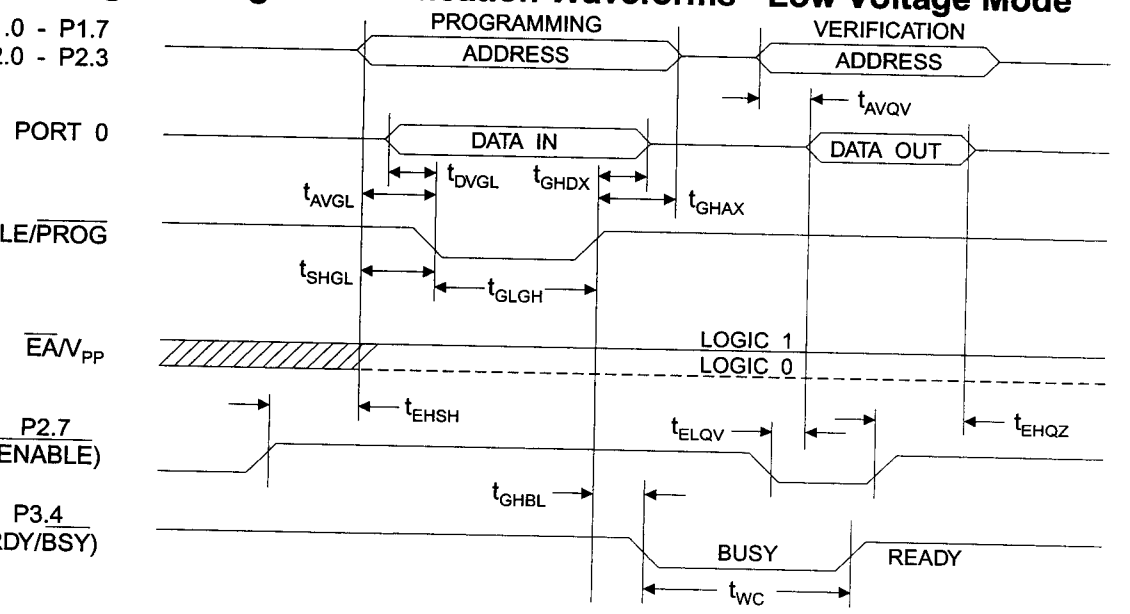
mbol	Parameter	Min	Max	Units
P(1)	Programming Enable Voltage	11.5	12.5	V
(1)	Programming Enable Current		1.0	mA
CLCL	Oscillator Frequency	4	24	MHz
GL	Address Setup to $\overline{PROG}$ Low	48tCLCL		
AX	Address Hold After $\overline{PROG}$	48tCLCL		
GL	Data Setup to $\overline{PROG}$ Low	48tCLCL		
DX	Data Hold After $\overline{PROG}$	48tCLCL		
SH	P2.7 ($\overline{ENABLE}$) High to V_{PP}	48tCLCL		
GL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
SL(1)	V_{PP} Hold After $\overline{PROG}$	10		µs
GH	$\overline{PROG}$ Width	1	110	µs
QV	Address to Data Valid		48tCLCL	
QV	$\overline{ENABLE}$ Low to Data Valid		48tCLCL	
QV	Data Float After $\overline{ENABLE}$	0	48tCLCL	
BL	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
	Byte Write Cycle Time		2.0	ms

1. Only used in 12-volt programming mode.

ash Programming and Verification Waveforms - High Voltage Mode



sh Programming and Verification Waveforms - Low Voltage Mode



bsolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0 V to +7.0 V
Maximum Operating Voltage	6.6 V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

C. Characteristics

= -40°C to 85°C, V_{CC} = 5.0 V ± 20% (unless otherwise noted)

mbol	Parameter	Condition	Min	Max	Units
	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
1	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
1	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
	Output Low Voltage(1) (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
1	Output Low Voltage(1) (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5 V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
1	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5 V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45 V		-50	µA
	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2 V		-650	µA
	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
T	Reset Pulldown Resistor		50	300	KΩ
	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
	Power Supply Current	Active Mode, 12 MHz		20	mA
		Idle Mode, 12 MHz		5	mA
	Power Down Mode(2)	V_{CC} = 6 V		100	µA
		V_{CC} = 3 V		40	µA

1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin:10 mA
   Maximum I_{OL} per 8-bit port:
   Port 0:26 mA
   Ports 1,2, 3:15 mA
   Maximum total IOL for all output pins:71 mA
   If IOL exceeds the test condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum VCC for Power Down is 2 V.

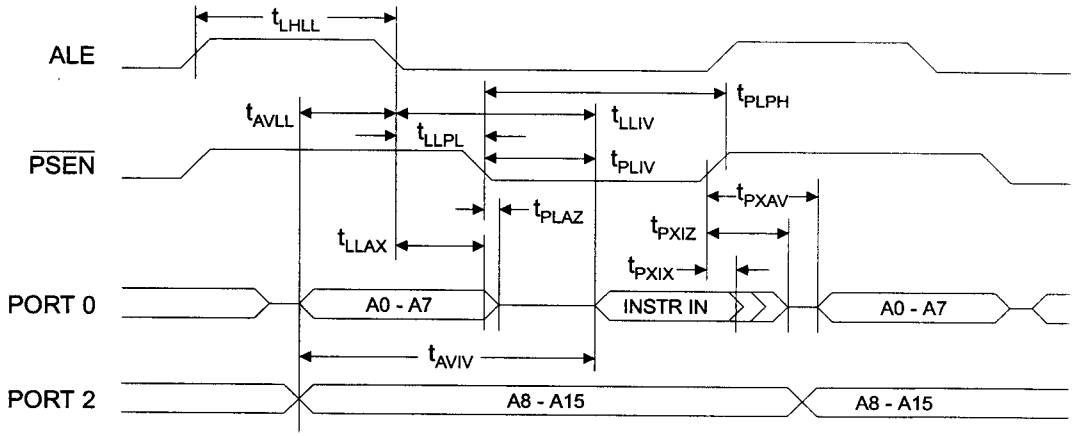
C. Characteristics

der Operating Conditions; Load Capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; Load Capacitance for all er outputs = 80 pF)

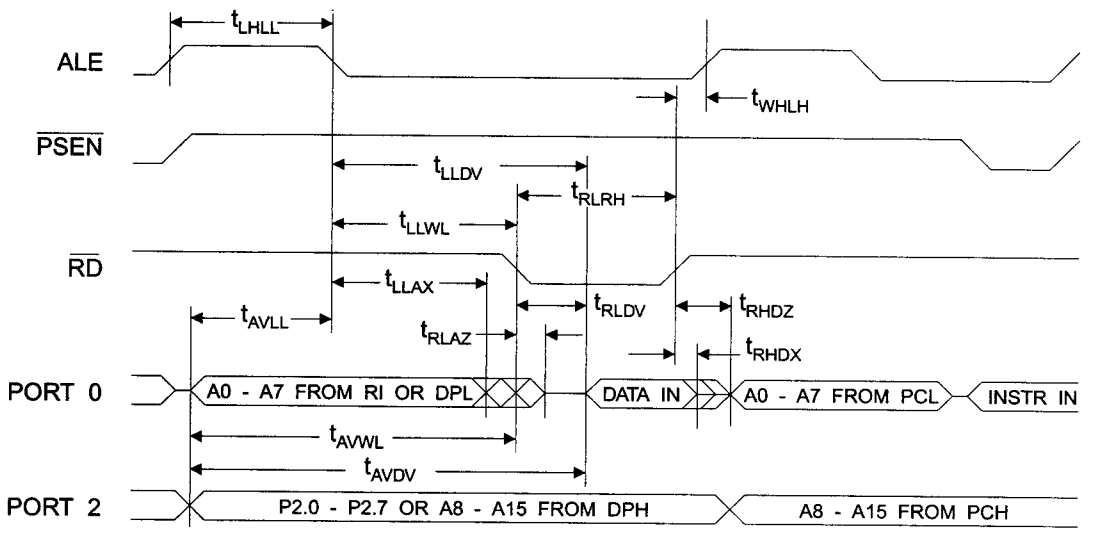
xternal Program and Data Memory Characteristics

ymbol	Parameter	12 MHz Oscillator		16 to 24 MHz Oscillator		Units
		Min	Max	Min	Max	
tCLCL	Oscillator Frequency			0	24	MHz
HLL	ALE Pulse Width	127		2tCLCL-40		ns
VLL	Address Valid to ALE Low	28		tCLCL-13		ns
LAX	Address Hold After ALE Low	48		tCLCL-20		ns
LIV	ALE Low to Valid Instruction In		233		4tCLCL-65	ns
LPL	ALE Low to $\overline{PSEN}$ Low	43		tCLCL-13		ns
PLPH	$\overline{PSEN}$ Pulse Width	205		3tCLCL-20		ns
PLIV	$\overline{PSEN}$ Low to Valid Instruction In		145		3tCLCL-45	ns
PXIX	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
PXIZ	Input Instruction Float After $\overline{PSEN}$		59		tCLCL-10	ns
PXAV	$\overline{PSEN}$ to Address Valid	75		tCLCL-8		ns
AVIV	Address to Valid Instruction In		312		5tCLCL-55	ns
PLAZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
RLRH	$\overline{RD}$ Pulse Width	400		6tCLCL-100		ns
WLWH	$\overline{WR}$ Pulse Width	400		6tCLCL-100		ns
RLDV	$\overline{RD}$ Low to Valid Data In		252		5tCLCL-90	ns
RHDX	Data Hold After $\overline{RD}$	0		0		ns
RHDZ	Data Float After $\overline{RD}$		97		2tCLCL-28	ns
LDV	ALE Low to Valid Data In		517		8tCLCL-150	ns
AVDV	Address to Valid Data In		585		9tCLCL-165	ns
LWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	3tCLCL-50	3tCLCL+50	ns
AVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		4tCLCL-75		ns
QVWX	Data Valid to $\overline{WR}$ Transition	23		tCLCL-20		ns
QVWH	Data Valid to $\overline{WR}$ High	433		7tCLCL-120		ns
WHQX	Data Hold After $\overline{WR}$	33		tCLCL-20		ns
RLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
WHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	tCLCL-20	tCLCL+25	ns

ternal Program Memory Read Cycle



ternal Data Memory Read Cycle

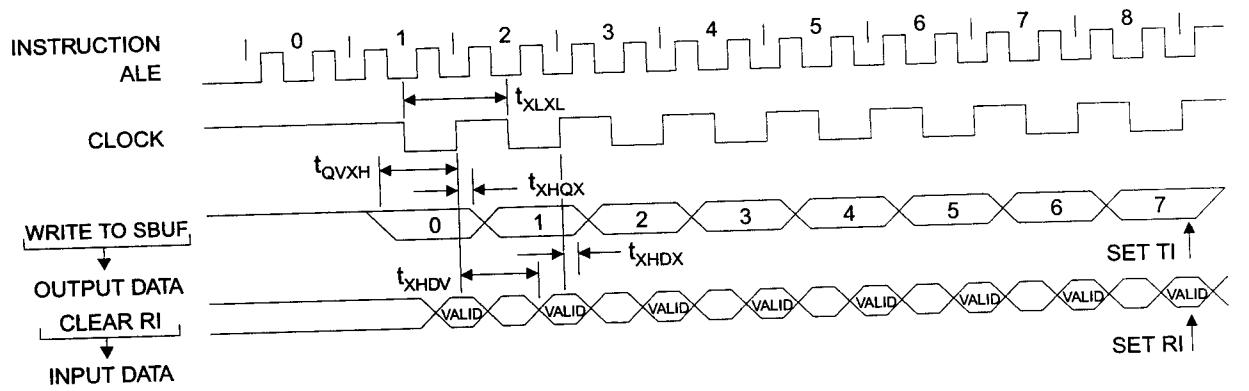


ial Port Timing: Shift Register Mode Test Conditions

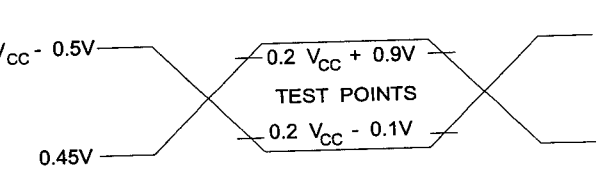
= 5.0 V ± 20%; Load Capacitance = 80 pF)

mbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
XL	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
VXH	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
HQX	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-33		ns
HDX	Input Data Hold After Clock Rising Edge	0		0		ns
HDV	Clock Rising Edge to Input Data Valid		700		10tCLCL-133	ns

ift Register Mode Timing Waveforms

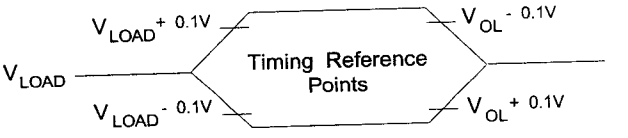


AC Testing Input/Output Waveforms[1]



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5 V for a logic 1 and 0.45 V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms[1]



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

rdering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
12	5 V ± 20%	AT89C51-12AC AT89C51-12JC AT89C51-12PC AT89C51-12QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)
		AT89C51-12AI AT89C51-12JI AT89C51-12PI AT89C51-12QI	44A 44J 40P6 44Q	Industrial (-40°C to 85°C)
		AT89C51-12AA AT89C51-12JA AT89C51-12PA AT89C51-12QA	44A 44J 40P6 44Q	Automotive (-40°C to 125°C)
	5 V ± 10%	AT89C51-12DM AT89C51-12LM	40D6 44L	Military (-55°C to 125°C)
		AT89C51-12DM/883 AT89C51-12LM/883	40D6 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
16	5 V ± 20%	AT89C51-16AC AT89C51-16JC AT89C51-16PC AT89C51-16QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)
		AT89C51-16AI AT89C51-16JI AT89C51-16PI AT89C51-16QI	44A 44J 40P6 44Q	Industrial (-40°C to 85°C)
		AT89C51-16AA AT89C51-16JA AT89C51-16PA AT89C51-16QA	44A 44J 40P6 44Q	Automotive (-40°C to 125°C)
20	5 V ± 20%	AT89C51-20AC AT89C51-20JC AT89C51-20PC AT89C51-20QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)
		AT89C51-20AI AT89C51-20JI AT89C51-20PI AT89C51-20QI	44A 44J 40P6 44Q	Industrial (-40°C to 85°C)

October 1999

National Semiconductor

ADC0808/ADC0809
8-Bit µP Compatible A/D Converters with 8-Channel Multiplexer

General Description

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet. (See AN-247 for more information.)

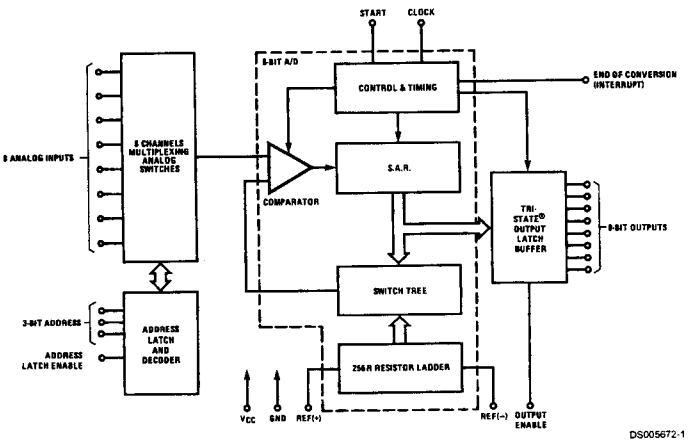
Features

- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- No zero or full-scale adjust required
- 8-channel multiplexer with address logic
- 0V to 5V input range with single 5V power supply
- Outputs meet TTL voltage level specifications
- Standard hermetic or molded 28-pin DIP package
- 28-pin molded chip carrier package
- ADC0808 equivalent to MM74C949
- ADC0809 equivalent to MM74C949-1

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ±1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	100 µs

Block Diagram



See Ordering Information

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Absolute Maximum Ratings (Notes 2, 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage at Any Pin Except Control Inputs	−0.3V to (V_{CC}+0.3V)
Voltage at Control Inputs (START, OE, CLOCK, ALE, ADD A, ADD B, ADD C)	−0.3V to +15V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A=25°C	875 mW
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Molded Chip Carrier Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 8)	400V

Operating Conditions (Notes 1, 2)

Temperature Range (Note 1)	$T_{MIN} \le T_A \le T_{MAX}$
ADC0808CCN,ADC0809CCN	−40°C≤T_A≤+85°C
ADC0808CCV, ADC0809CCV	−40°C ≤ T_A ≤ +85°C
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.0 V_{DC}

Electrical Characteristics

Converter Specifications: V_{CC}=5 V_{DC}=V_{REF+}, $V_{REF(-)}$=GND, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK}=640 kHz unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	ADC0808					
	Total Unadjusted Error	25°C			±½	LSB
	(Note 5)	T_{MIN} to T_{MAX}			±¾	LSB
	ADC0809					
	Total Unadjusted Error	0°C to 70°C			±1	LSB
	(Note 5)	T_{MIN} to T_{MAX}			±1¼	LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	2.5		kΩ
	Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.10		V_{CC}+0.10	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	V_{CC}+0.1	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder		V_{CC}/2-0.1	V_{CC}/2	V_{CC}/2+0.1	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V
I_{IN}	Comparator Input Current	f_c=640 kHz, (Note 6)	−2	±0.5	2	µA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV, 4.75≤V_{CC}≤5.25V, −40°C≤T_A≤+85°C unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
$I_{OFF(+)}$	OFF Channel Leakage Current	V_{CC}=5V, V_{IN}=5V,				
		T_A=25°C		10	200	nA
		T_{MIN} to T_{MAX}			1.0	µA
$I_{OFF(-)}$	OFF Channel Leakage Current	V_{CC}=5V, V_{IN}=0,				
		T_A=25°C	−200	−10		nA
		T_{MIN} to T_{MAX}	−1.0			µA
CONTROL INPUTS						
$V_{IN(1)}$	Logical "1" Input Voltage		V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	V_{IN}=15V			1.0	µA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	V_{IN}=0	−1.0			µA
I_{CC}	Supply Current	f_{CLK}=640 kHz		0.3	3.0	mA

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV, $4.75 \le V_{CC} \le 5.25V$, $-40°C \le T_A \le +85°C$ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 4.75V I_{OUT} = −360µA I_{OUT} = −10µA		**2.4** **4.5**		V(min) V(min)
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O=1.6 mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	I_O=1.2 mA			0.45	V
I_{OUT}	TRI-STATE Output Current	V_O=5V V_O=0	 −3		3	µA µA

Electrical Characteristics

Timing Specifications $V_{CC}=V_{REF(+)}=5V$, $V_{REF(-)}=GND$, $t_r=t_f=20$ ns and $T_A=25°C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	(*Figure 5*)		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	(*Figure 5*)		100	200	ns
t_s	Minimum Address Set-Up Time	(*Figure 5*)		25	50	ns
t_H	Minimum Address Hold Time	(*Figure 5*)		25	50	ns
t_D	Analog MUX Delay Time From ALE	R_S=0Ω (*Figure 5*)		1	2.5	µs
t_{H1}, t_{H0}	OE Control to Q Logic State	C_L=50 pF, R_L=10k (*Figure 8*)		125	250	ns
t_{1H}, t_{0H}	OE Control to Hi-Z	C_L=10 pF, R_L=10k (*Figure 8*)		125	250	ns
t_c	Conversion Time	f_c=640 kHz, (*Figure 5*) (Note 7)	90	100	116	µs
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	(*Figure 5*)	0		8+2 µS	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE Output Capacitance	At TRI-STATE Outputs		10	15	pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless othewise specified.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC}n supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute $0V_{DC}$ to $5V_{DC}$ input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors. See *Figure 3*. None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13*.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence (*Figure 8*). See paragraph 4.0.

Note 7: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

Note 8: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Functional Description

Multiplexer. The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. *Table 1* shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE 1.

SELECTED ANALOG CHANNEL	ADDRESS LINE		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach (*Figure 1*) was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +½ LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0808, ADC0809, the approximation technique is extended to 8 bits using the 256R network.

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0808 as measured using the procedures outlined in AN-179.

Functional Description (Continued)

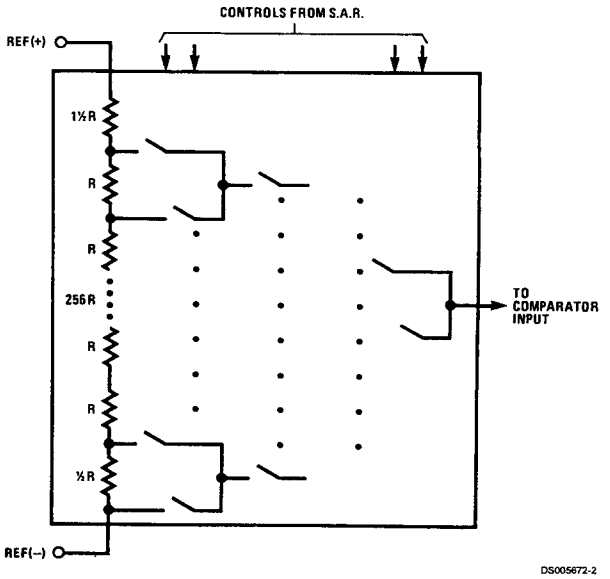


FIGURE 1. Resistor Ladder and Switch Tree

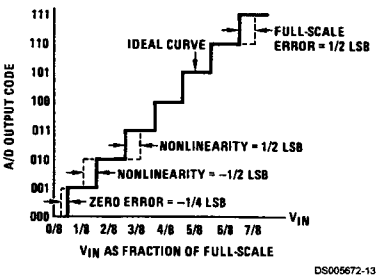


FIGURE 2. 3-Bit A/D Transfer Curve

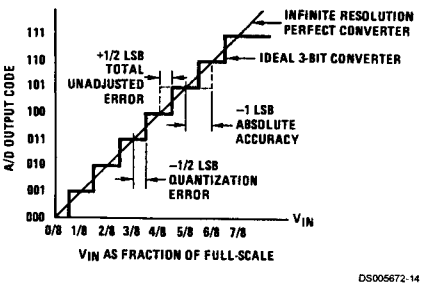


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

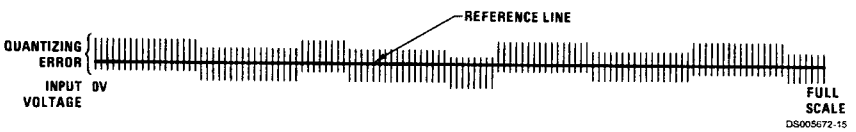


FIGURE 4. Typical Error Curve

Timing Diagram

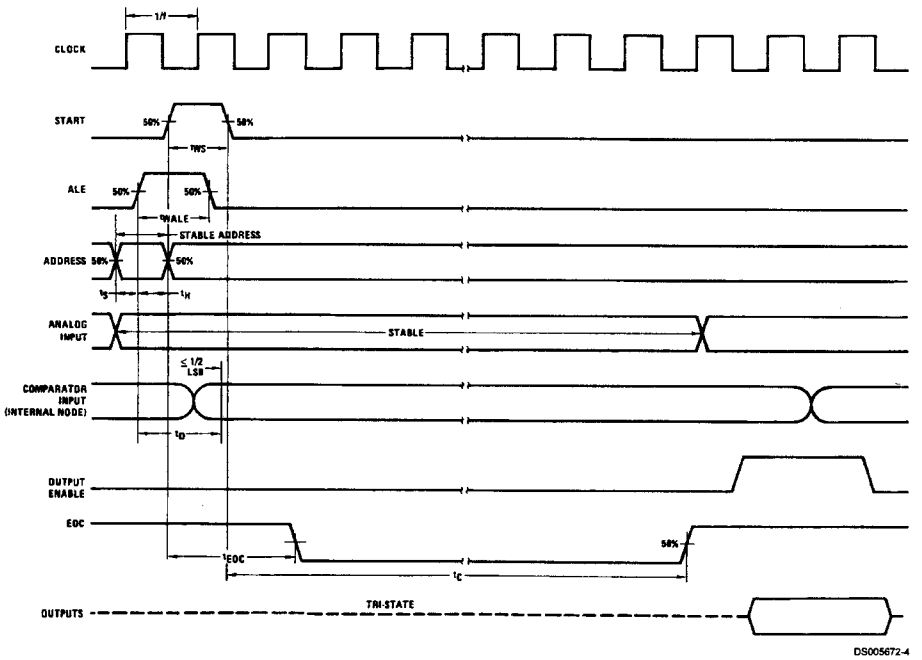


FIGURE 5.

Typical Performance Characteristics

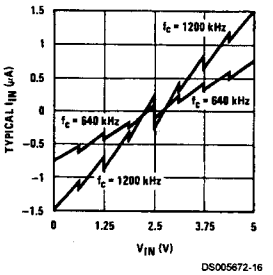


FIGURE 6. Comparator I_{IN} vs V_{IN} (V_{CC}=V_{REF}=5V)

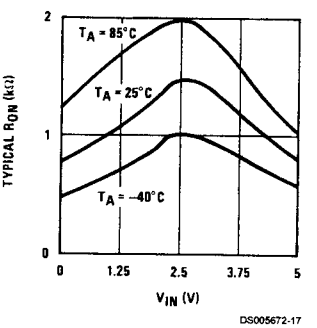


FIGURE 7. Multiplexer R_{ON} vs V_{IN} (V_{CC}=V_{REF}=5V)

TRI-STATE Test Circuits and Timing Diagrams

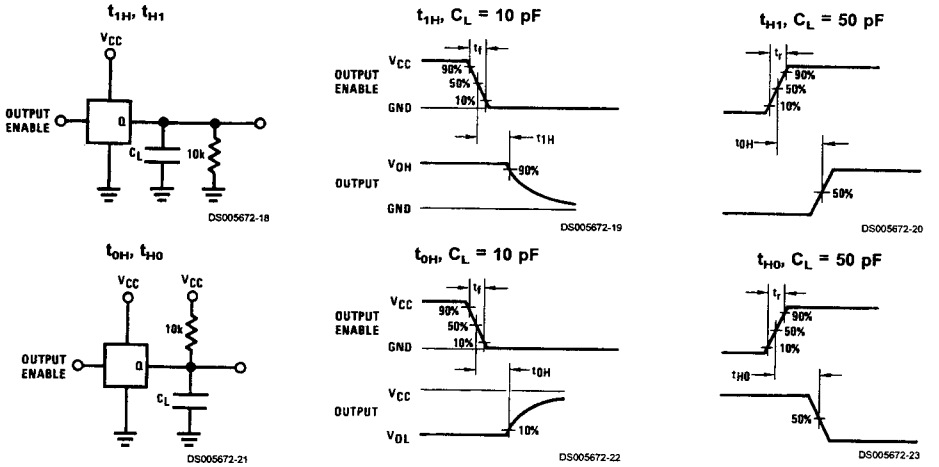


FIGURE 8.

Applications Information

OPERATION

1.0 RATIOMETRIC CONVERSION

The ADC0808, ADC0809 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0808 is expressed by the equation

$$\frac{V_{IN}}{V_{fs}-V_Z}=\frac{D_X}{D_{MAX}-D_{MIN}} \quad (1)$$

V_{IN}=Input voltage into the ADC0808

V_{fs}=Full-scale voltage

V_Z=Zero voltage

D_X=Data point being measured

D_{MAX}=Maximum data limit

D_{MIN}=Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0808, ADC0809 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, (*Figure 9*).

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a sys-

National Semiconductor

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DAC0800/DAC0802
8-Bit Digital-to-Analog Converters

General Description

The DAC0800 series are monolithic 8-bit high-speed current-output digital-to-analog converters (DAC) featuring typical settling times of 100 ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC0800 series also features high compliance complementary current outputs to allow differential output voltages of 20 Vp-p with simple resistor loads as shown in *Figure 1*. The reference-to-full-scale current matching of better than ±1 LSB eliminates the need for full-scale trims in most applications while the nonlinearities of better than ±0.1% over temperature minimizes system error accumulations.

The noise immune inputs of the DAC0800 series will accept TTL levels with the logic threshold pin, V_{LC}, grounded. Changing the V_{LC} potential will allow direct interface to other logic families. The performance and characteristics of the device are essentially unchanged over the full ±4.5V to ±18V power supply range; power dissipation is only 33 mW with ±5V supplies and is independent of the logic input states.

The DAC0800, DAC0802, DAC0800C and DAC0802C are a direct replacement for the DAC-08, DAC-08A, DAC-08C, and DAC-08H, respectively.

Features

- Fast settling output current: 100 ns
- Full scale error: ±1 LSB
- Nonlinearity over temperature: ±0.1%
- Full scale current drift: ±10 ppm/°C
- High output compliance: −10V to +18V
- Complementary current outputs
- Interface directly with TTL, CMOS, PMOS and others
- 2 quadrant wide range multiplying capability
- Wide power supply range: ±4.5V to ±18V
- Low power consumption: 33 mW at ±5V
- Low cost

Typical Applications

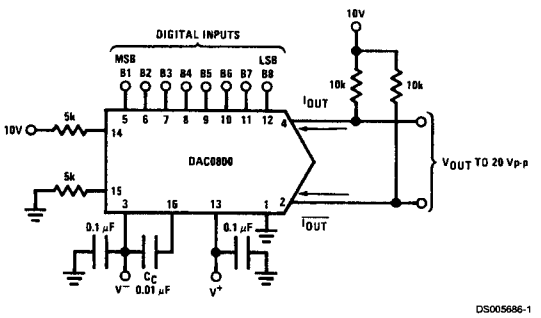


FIGURE 1. ±20 V_{P-P} Output Digital-to-Analog Converter (Note 5)

Ordering Information

Non-Linearity	Temperature Range	Order Numbers				
		J Package (J16A) (Note 1)		N Package (N16E) (Note 1)		SO Package (M16A)
±0.1% FS	0°C ≤ T_A ≤ +70°C	DAC0802LCJ	DAC-08HQ	DAC0802LCN	DAC-08HP	DAC0802LCM
±0.19% FS	−55°C ≤ T_A ≤ +125°C	DAC0800LJ	DAC-08Q			
±0.19% FS	0°C ≤ T_A ≤ +70°C	DAC0800LCJ	DAC-08EQ	DAC0800LCN	DAC-08EP	DAC0800LCM

Note 1: Devices may be ordered by using either order number.

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	±18V or 36V
Power Dissipation (Note 3)	500 mW
Reference Input Differential Voltage (V14 to V15)	V^- to V^+
Reference Input Common-Mode Range (V14, V15)	V^- to V^+
Reference Input Current	5 mA
Logic Inputs	V^- to V^- plus 36V
Analog Current Outputs ($V_S^- = -15V$)	4.25 mA
ESD Susceptibility (Note 4)	TBD V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Operating Conditions (Note 2)

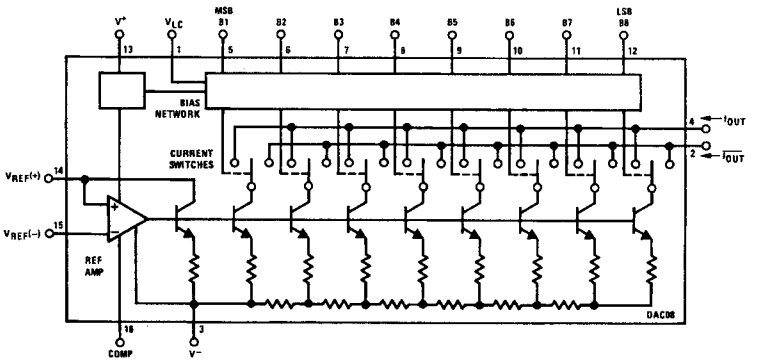
	Min	Max	Units
Temperature (T_A)			
DAC0800L	−55	+125	°C
DAC0800LC	0	+70	°C
DAC0802LC	0	+70	°C

Electrical Characteristics

The following specifications apply for $V_S^- = \pm 15V$, $I_{REF} = 2$ mA and $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

Symbol	Parameter	Conditions	DAC0802LC			DAC0800L/ DAC0800LC			Units
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Nonlinearity				±0.1			±0.19	%FS
t_s	Settling Time	To ±½ LSB, All Bits Switched "ON" or "OFF", T_A=25°C		100	135				ns
		DAC0800L					100	135	ns
		DAC0800LC					100	150	ns
tPLH, tPHL	Propagation Delay	T_A=25°C							
	Each Bit			35	60		35	60	ns
	All Bits Switched			35	60		35	60	ns
TCI_{FS}	Full Scale Tempco			±10	±50		±10	±50	ppm/°C
V_{OC}	Output Voltage Compliance	Full Scale Current Change <½ LSB, R_{OUT}>20 MΩ Typ	−10		18	−10		18	V
I_{FS4}	Full Scale Current	V_{REF}=10.000V, R14=5.000 kΩ R15=5.000 kΩ, T_A=25°C	1.984	1.992	2.000	1.94	1.99	2.04	mA
I_{FSS}	Full Scale Symmetry	$I_{FS4}-I_{FS2}$		±0.5	±4.0		±1	±8.0	µA
I_{ZS}	Zero Scale Current			0.1	1.0		0.2	2.0	µA
I_{FSR}	Output Current Range	V^-=−5V	0	2.0	2.1	0	2.0	2.1	mA
		V^-=−8V to −18V	0	2.0	4.2	0	2.0	4.2	mA
	Logic Input Levels								
V_{IL}	Logic "0"	V_{LC}=0V			0.8			0.8	V
V_{IH}	Logic "1"		2.0			2.0			V
	Logic Input Current	V_{LC}=0V							
I_{IL}	Logic "0"	$-10V \le V_{IN} \le +0.8V$		−2.0	−10		−2.0	−10	µA
I_{IH}	Logic "1"	$2V \le V_{IN} \le +18V$		0.002	10		0.002	10	µA
V_{IS}	Logic Input Swing	V^-=−15V	−10		18	−10		18	V
V_{THR}	Logic Threshold Range	V_S=±15V	−10		13.5	−10		13.5	V
I_{15}	Reference Bias Current			−1.0	−3.0		−1.0	−3.0	µA
dI/dt	Reference Input Slew Rate	(*Figure 11*)	4.0	8.0		4.0	8.0		mA/µs
$PSSI_{FS+}$	Power Supply Sensitivity	$4.5V \le V^+ \le 18V$		0.0001	0.01		0.0001	0.01	%/%
$PSSI_{FS-}$		$-4.5V \le V^- \le 18V$ I_{REF}=1mA		0.0001	0.01		0.0001	0.01	%/%

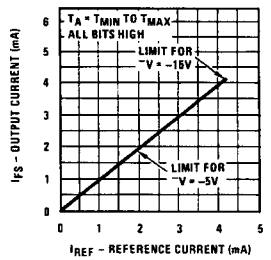
Block Diagram (Note 5)



DS005686-2

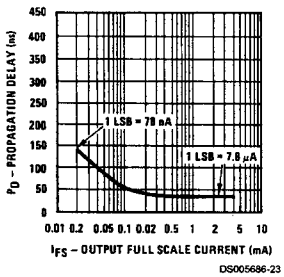
Typical Performance Characteristics

Full Scale Current vs Reference Current



DS005686-22

LSB Propagation Delay vs I_{FS}



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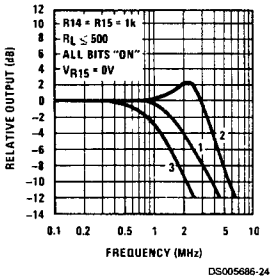
Reference Input Frequency Response



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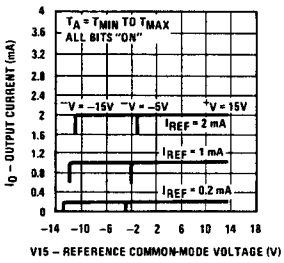
Curve 1: C_C=15 pF, V_{IN}=2 Vp-p centered at 1V.
Curve 2: C_C=15 pF, V_{IN}=50 mVp-p centered at 200 mV.
Curve 3: C_C=0 pF, V_{IN}=100 mVp-p centered at 0V and applied through 50Ω connected to pin 14.2V applied to R14.

Reference Amp Common-Mode Range



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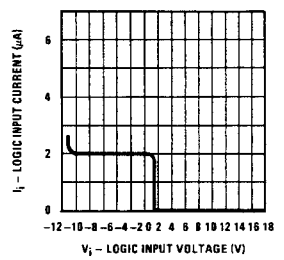
Note. Positive common-mode range is always (V+) − 1.5V.

Logic Input Current vs Input Voltage



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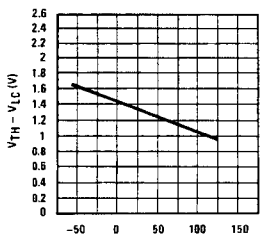
V_{TH} — V_{LC} vs Temperature



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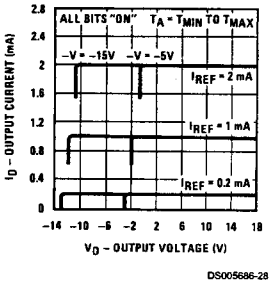
Typical Performance Characteristics (Continued)

Output Current vs Output Voltage (Output Voltage Compliance)



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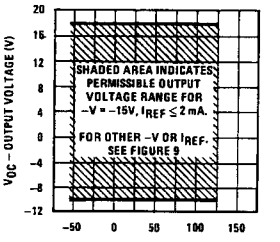
Output Voltage Compliance vs Temperature



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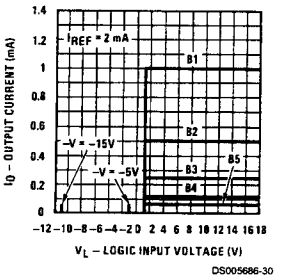
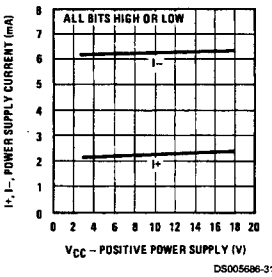
Bit Transfer Characteristics



DS005686-30

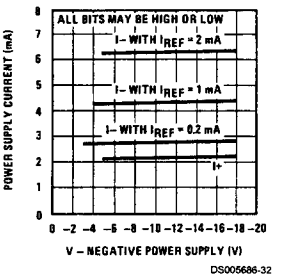
Note. B1–B8 have identical transfer characteristics. Bits are fully switched with less than ½ LSB error, at less than ±100 mV from actual threshold. These switching points are guaranteed to lie between 0.8 and 2V over the operating temperature range (V_{LC} = 0V).

Power Supply Current vs +V



DS005686-31

Power Supply Current vs −V



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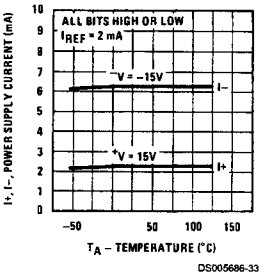
Power Supply Current vs Temperature



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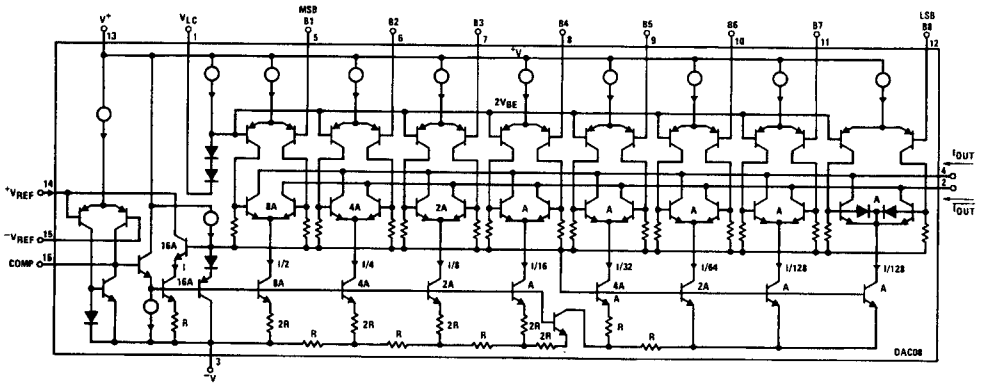
Equivalent Circuit



DS005686-15

FIGURE 2.