ACCIDENT IDENTIFICATION SYSTEM

PROJECT REPORT

P-1146

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Award of the degree of BACHELOR OF ENGINEERING in ELECTRICAL AND ELECTRONICS ENGINEERING Branch of BHARATHIAR UNIVERSITY, COIMBATORE

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

KUMARAGURU COLLEGE OF TECHNOLOGY

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

ISO 9001:2000 Certified

CERTIFICATE

This is to certify that the project report entitled

ACCIDENT IDENTIFICATION SYSTEM

Is the bonafide work done by

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DEDICATED TO

THE INNUMERABLE LIVES

THAT HAVE BEEN LOST IN

ACCIDENTS

SYNOPSIS

SYNOPSIS

Global Positioning System is a growing field made use of in Automobiles for Vehicle tracking. The tracking is done as a precautionary measure and to intimate the observer at the time of emergency. The system designed is mainly used for the "Highways Accident Identification" which is incorporated with the ATMEL 89C51 Microcontroller in Transmitter section, where the input is obtained from a Vibration Sensor, a Piezo electric crystal and a Direction sensor attached to the vehicle. The IC XR-2206 that we have made use of is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp, and pulse waveforms of high-stability and accuracy. The output waveforms can be both amplitude and frequency modulated by an external voltage. Digital Modulation is performed and then through an AM Modulator the signal is transmitted. The receiver section has an AM Demodulator that demodulates the received signal. This demodulated signal is fed into the PC via RS232. The parameters are then observed in the PC monitor. The transmitter section is fixed in the vehicle and receiver section is stationary. At the time of the accident, the vibration sensor is activated due to collision and the circuit for these, switches ON, which are then noted in the PC monitor. From the position of the accident and also the impact, help can be sent for immediately thus saving invaluable live which may otherwise have been lost.

Furthermore, we can extend our project by linking it with a satellite. Using this extension we can track the position of the vehicle anywhere in the world. It can also be used in automatic road traffic control. On the implementation of a vehicle immobilizer, the utility of the system can be further enhanced. Moreover by fitting gas leakage sensors and fire sensors, we can also very easily prevent deadly explosions and accidents in LPG driven vehicles. In order to increase the flexibility of the system, we can replace the PC with a cell-phone making it more compact and user-friendly

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INTRODUCTION

INTRODUCTION

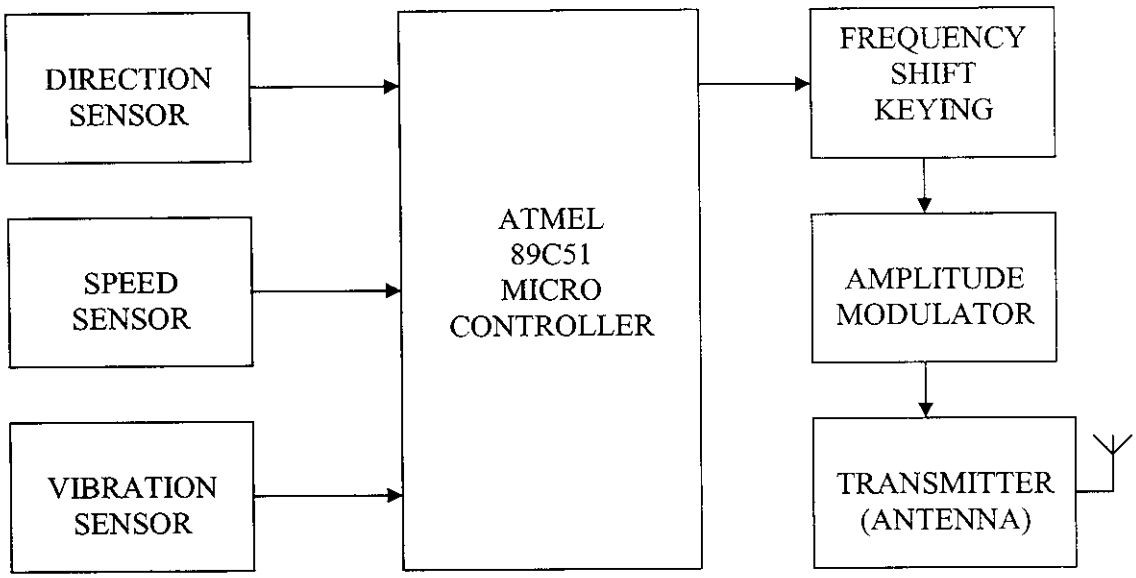
Highways Accident Identification System (Vehicle Tracking System) is a miniature model of Global Positioning System (GPS). GPS is a system used to find out the position or location of vehicles moving anywhere around the globe. In order to implement a GPS, a link with a satellite is required. Separate ranges of frequencies for uplinking and downlinking from the satellite have to be leased. Moreover transponders of very high strength are required. However since this is not viable for a student-level project, we have gone in for a miniature model of the GPS. In order to build the miniature model we have used a single chip micro controller in the vehicle. The vehicle that is used here may be a two-wheeler or four-wheeler with a battery connection. Sensors are fit to the vehicle in order to monitor the direction and speed. Moreover a vibration sensor is also fit into the system so as to detect any possible accident and pass on the information about the accident to the receiver section .The sensor made use of for this unction is a Piezo electric crystal. With the help of the speed sensor, we can calculate the distance with respect to time. The direction and the distance are fed into the micro controller and it is transmitted to the PC using Digital Modulation technique. At the receiver end the signal is detected and demodulated using Digital Demodulation technique. After demodulation is performed, the signal is given to the PC. The micro controller that is made use of in our project is AT89C51. It is manufactured by ATMEL INC., USA. This micro controller is an advanced version of INTEL8051 micro controller. The main advantage of using this micro controller is that it has an inbuilt UART (Universal Asynchronous Receiver & Transmitter), a very essential feature for the working of our system.

As the movement of the vehicle is continuously monitored, any accident or impact that may occur to the vehicle can be detected. As the position of the vehicle is known ,medical help can be easily sent for.

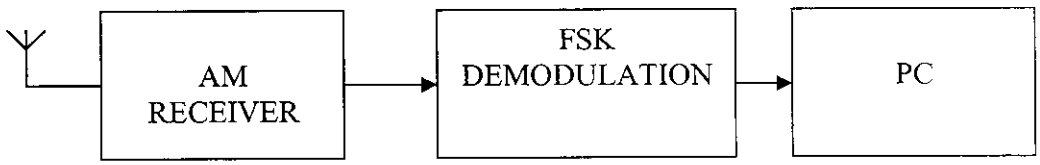
BLOCK DIAGRAM

BLOCK DIAGRAM

TRANSMITTER SECTION:



RECIEVER SECTION:



LIST OF COMPONENTS

COMPONENT LIST

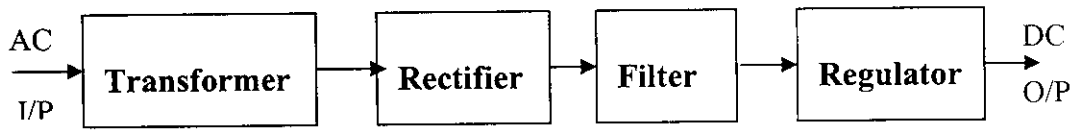
Sl. No	NAME OF ITEM	REQUIRED QTY
1	IC 89C51	1
2	IC LM741	7
3	IC LM565	1
4	IC CD4011	1
5	IC XR2206	1
6	IC 74F04	4
7	IC TL082	1
8	IC HIN232	1
9	IC BASICS	16
10	POTENTIO METER 220K	9
11	CRYSTAL 5.5 MHz	1
12	DB–9 9 – PIN CONNECTOR	1
13	RED LED	5
14	Diode IN 4007	12
15	Diode 0A79	2
16	Filter Capacitor 1000µp/25v	4
17	Filter Capacitor 100µp/25v	6
18	Filter Capacitor 47µp/25v	2
19	Piezo Electric plate	1
20	Transistor BC 547	12
21	Transistor BC494	1
22	FET BFW10	1
23	3 Pin Regulator LM7812	1
24	3 Pin Regulator LM7805	3

POWER SUPPLY

POWER SUPPLY

Since all electronic circuits work with only low D.C. Voltage, we need a power supply unit to provide the appropriate voltage supply. This unit consists of a transformer, rectifier, filter and regulator. A.C. voltage typically 230V rms is connected to a transformer which steps that AC voltage down to the level to the desired AC voltage. A diode rectifier then provides a full-wave rectified voltage that is initially filtered by a simple capacitor filter to produce a DC voltage. The resulting DC voltage usually has some ripple or AC voltage variations. A regulator circuit can use this DC input to provide DC voltage that not only has much less ripple voltage but also remains the same DC value even though DC voltage varies some what, or the load connected to the output DC voltages changes.

BLOCK DIAGRAM:



TRANSFORMER:

A transformer is a static (or stationary) piece of which electric power in one circuit is transformed into electric power of the same frequency in another circuit. It can raise or lower the voltage in a circuit but with a corresponding decrease or increase in current. It works with the principle of mutual induction. In our project we use a step down transformer in order to maintain the necessary power supply for the electronic circuits. The transformer that we use is a 15-0-15 V transformer.

RECTIFIER:

The DC level obtained from a sinusoidal input can be improved 100% using a process called full-wave rectification. It uses 4 diodes in a bridge configuration. From the basic bridge configuration we see that two diodes (say D2 & D3) are conducting while the other two diodes (D1 & D4) are in "off" state during the period t =0 to T/2. Accordingly for the negative of the input the conducting diodes are D1 & D4. Thus the polarity across the load is the same.

FILTER:

The filter circuit used here is the capacitor filter circuit where a capacitor is connected at the rectifier output, and a DC is obtained across it. The filtered waveform is essentially a DC voltage with negligible ripples, which is ultimately fed to the load.

REGULATOR:

The output voltage from the capacitor is more filtered and finally regulated. The voltage regulator is a device, which maintains the output voltage constant irrespective of the change in supply variations, load variation and temperature changes. Here we use two fixed voltage regulators namely LM 7812, LM 7805 and LM7912. The IC 7812 is a+12V regulator IC 7912 is a -12V regulator and IC 7805 is a +5V regulator.

DIRECTION SENSOR

IR SENSOR:

Infrared emitting diodes are solid-state gallium arsenide devices that emit a beam of radiant flux when forward biased. When the junction is a forward biased, electron from the N region will recombine with excess holes of the P material in specially designed recombination region sandwiched between the P&N type materials. During this recombination process, energy is radiated away from the device the form of photons. The generated photons will either be reabsorbed the structure or leave the surface of the device as radiant energy. A few areas of application of such devices include Card and paper tape readers, shaft encoder, data transmission systems and intrusion alarms.

The IR circuit consists of

- Comparator
- Voltage divider
- Switching circuit

Voltage Divider:

A potential or voltage divider provides a convenient way of getting a variable voltage from a fixed voltage supply. In general, if two resistors with values R1 and R2 are connected in series across a supply voltage V and the voltages developed across each are V1 and V2 respectively, then, if I am the current flowing, we can say:

$V1 = I*R1$ .....(1)

$V1 = I*R2$. .....(2)

$V = V1 + V2 = I (R1+R2)$. .....(3)

Dividing (1) by (3) we obtain:

$V1 /V = (I*R1)/(I*(R1+R2))$

Multiplying both sides by V gives:

$V1 = (R1 * V)/ (R1+R2)$

Similarly from (2) and (3) we get:

$V2 = (R2 * V)/ (R1+R2)$

IC 741:

The LM741 series are general-purpose operational amplifiers. The amplifiers offer many features, which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations. The LM741C/LM741E is identical to the LM741/LM741A except that the LM741C/LM741E has their performance guaranteed over a 0ßC to a70ßC temperature range, instead of b55ßC to a125ßC. Here the op-amp is used as a comparator.

COMPARATOR:

A comparator is a circuit, which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input. It is basically an open loop op-amp with an output Vsat (= Vcc). It may be seen that the change in the output state takes place with an increment in input V1 of only 2 mV. This is the uncertainty region where output cannot be directly defined.

There are basically two types of comparators:

1. Non-inverting comparator
2. Inverting comparator

In case of non-inverting comparator a fixed reference voltage Vref is applied to (-) input and a time varying signal Vi is applied to (+) input. The output voltage is at -Vsat for Vi< Vsat and Vo goes to + Vsat for Vi > Vref.

In case of inverting comparator a fixed reference voltage Vref is applied to (+) input and a time varying signal Vi is applied to (-) input. The output voltage is at +Vsat for Vi< Vsat and Vo goes to Vsat for Vi > Vref.

SWITCHING CIRCUIT:

Many solid-state devices are used in power control applications the simplest of these being the discrete bipolar transistor, which is usually used in the switching mode. In the case of the NPN transistor the switch load is wired between collector and supply positive, and in the case of PNP device it is wired between collector and the 0V. In both cases the switch-driving signal is applied to base via R1, which has a typical resistance about twenty times greater than the load resistance value. In the NPN circuit, Transistor Q1 is cut off (acting like an open switch), with its output at the positive supply voltage value, with zero input signal applied, but can be driven to saturation (so that it acts like a closed switch and passes current from collector to emitter) by applying a large positive input voltage, under which condition the output equals Q1's saturation voltage value (typically 200mV to 600 mV).

The action of the PNP circuit is the reverse of that described above, and Q1 is driven to saturation (with its output a few hundred milli-volts below the supply voltage value) and passes current from emitter to collector with zero input drive voltage applied, and is cut off (with its output at zero volts) when the input equals the positive supply value. In our circuit at the transmitting side, when the IR emits a beam of radiant flux, a voltage will be developed in the one input of the comparator. Let the voltage be V1. A reference voltage V2 is developed across the other input. The comparator compares these two voltages (V1 & V2). The output of the comparator is positive and negative going pulses. These pulses are given to the switching circuit to get logic 1 and logic 0.

VIBRATION SENSOR

PIEZO ELECTRIC CRYSTAL:

A crystal exhibits Piezo electric effect. A piezoelectric material is one in which an electrical potential appears across certain surfaces of a crystal if the dimensions of the crystal are changed by the application of a mechanical force. The potential is produced by the displacement charges.

PIEZOELECTRIC EFFECT:

The material causes it to contract or expand according to the sign of the electric field. Piezo electric effect is that which occurs when certain materials are subjected to mechanical stress. An electrical polarization is setup in the crystal and the faces of the crystal became electrically charged. The polarity of the charges reverses if applied across.

CIRCUIT DESCRIPTION:

In the circuit we use IC TL082. This IC is a high speed JFET input dual operational amplifier incorporating well-matched, high voltage J-FET and a bipolar transistor that is monolithic integrated circuit. The device features high slew rates, low input bias and offset current and low offset voltage temperature coefficient. In the circuit diagram IC TL082A acts as a comparator. A comparator is a circuit, which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input. It is basically an open loop op-amp with an output Vsat (= Vcc). It may be seen that the change in the output state takes place with an increment in input V1 of only 2 mV. This is the uncertainty region where output cannot be directly defined. The comparator section used in the circuit has already been discussed above.

MICROCONTROLLER

ATMEL 89C51 MICROCONTROLLER

INTRODUCTION

A Micro controller consists of a powerful CPU tightly coupled with memory RAM, ROM or EPROM), various I / O features such as Serial ports, Parallel Ports, Timer/Counters, Interrupt Controller, Data Acquisition interfaces-Analog to Digital Converter (ADC), Digital to Analog Converter (ADC), everything integrated onto a single Silicon Chip. The various devices can be used independently depending on the need and area of application for which it is designed. A microcomputer system requires memory to store a sequence of instructions making up a program, parallel port or serial port for communicating with an external system, timer / counter for control purposes like generating time delays, Baud rate for the serial port, apart from the controlling unit called the **Central Processing Unit.**

ATMEL 89C51 MICRO CONTROLLER

The major Features of 8-bit Micro controller **ATMEL 89C51**:

- 8 Bit CPU optimized for control applications
- Extensive Boolean processing (Single - bit Logic) Capabilities.
- On - Chip Flash Program Memory
- On - Chip Data RAM
- Bi-directional and Individually Addressable I/O Lines
- Multiple 16-Bit Timer/Counters
- Full Duplex UART
- Multiple Source / Vector / Priority Interrupt Structure
- On - Chip Oscillator and Clock circuitry.
- On - Chip EEPROM
- SPI Serial Bus Interface
- Watch Dog Timer

POWER MODES:

To exploit the power savings available in CMOS circuitry, ATMEL's Flash micro controllers have two software-invited reduced power modes.

They are

1. Idle mode
2. Power down mode.

IDLE MODE:

The CPU is turned off while the RAM and other on – chip peripherals continue operating. In this mode current drawn is reduced to about 15 percent of the current drawn when the device is fully active.

POWER DOWN MODE:

All on-chip activities are suspended while the on – chip RAM continues to hold its data. In this mode, the device typically draws less than 15 Micro Amps and can be as low as 0.6 Micro Amps.

POWER ON RESET:

When power is turned on, the circuit holds the RST pin high for an amount of time that depends on the capacitor value and the rate at which it charges. To ensure a valid reset, the RST pin must be held high long enough to allow the oscillator to start up plus two machine cycles. On power up, Vcc should rise within approximately 10ms. The oscillator start-up time depends on the oscillator frequency. For a 10 MHz crystal, the start-up time is typically 1ms.With the given circuit, reducing Vcc quickly to 0 causes the RST pin voltage to momentarily fall below 0V. However, this voltage is internally limited and will not harm the device.

MEMORY ORGANISATION

Logical separation of program and data memory

All ATMEL flash micro controllers have separate address spaces for program and data memory. The logical separation of the program and data memory allows the data memory to be accessed by 8 bit addresses, which is quickly stored and manipulated by am 8 bit CPU nevertheless 16 bit data memory addresses can also be generated through the DPTR register. Program memory can only be read. There can be up to 64K bytes of directly addressable program memory. The read strobe for external program memory is the Program Store Enable Signal (PSEN) Data memory occupies a separate address space from program memory. Up to 64K bytes of external memory can be directly addressed in the external data memory space. The CPU generates read and write signals, RD and WR, during external data memory accesses. External program memory and external data memory can be combined by a applying the RD and PSEN signal to the inputs of AND gate and using the output of the fate as the read strobe to the external program/data memory.

PROGRAM MEMORY:

The figure shows the map of the lower part of the program memory, after reset, the CPU begins execution from location 0000h. Each interrupt is assigned a fixed location in program memory. The interrupt causes the CPU to jump to that location, where it executes the service routine. External Interrupt 0 for example, is assigned to location 0003h. If external Interrupt 0 is used, its service routine must begin at location 0003h. If the Interrupt I is not used its service location is available as general-purpose program memory. The interrupt service locations are spaced at 8 byte intervals 0003h for External interrupt 0, 000Bh for Timer 0, 0013h for External interrupt 1,001Bh for Timer1, and so on.

DATA MEMORY:

The Internal Data memory is dived into three blocks namely,

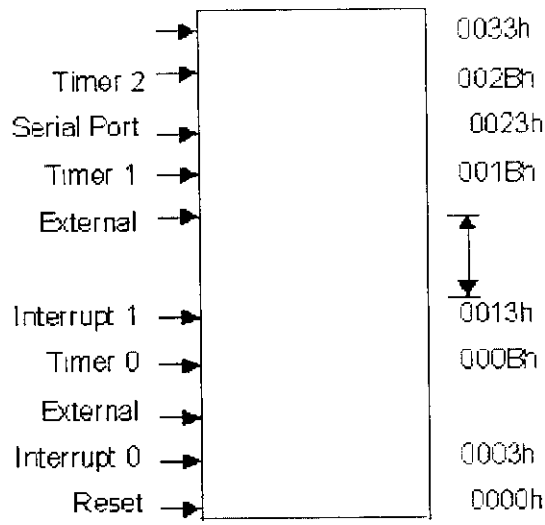
- The lower 128 Bytes of Internal RAM.
- The Upper 128 Bytes of Internal RAM.
- Special Function Register.

Internal Data memory Addresses are always 1 byte wide, which implies an address space of only 256 bytes. However, the addressing modes for internal RAM can in fact accommodate 384 bytes. Direct addresses higher than 7Fh access one memory space and indirect addresses higher than 7Fh access a different Memory Space. The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word (PSW) Select, which register bank, are in use. This architecture allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

The next 16-bytes of the above register banks form a block of bit addressable memory space. The micro controller instruction set includes a wide selection of single - bit instructions and this instruction can directly address the 128 bytes in this area. These bit addresses are 00h through 7Fh. either directs or indirect addressing can access all of the bytes in lower 128 bytes. Indirect addressing can only access the upper 128. The upper 128 bytes of RAM are only in the devices with 256 bytes of RAM. The Special Function Register includes Port latches, timers, peripheral controls etc., direct addressing can only access these register.

In general, all ATMEL micro controllers have the same SFRs at the same addresses in SFR space as the AT89C51 and other compatible micro controllers. However, upgrades to the AT89C51 have additional SFRs. Sixteen addresses in SFR space are both byte and bit Addressable. The bit Addressable SFRs are those whose address ends in 000B. The bit addresses in this area are 80h through FFh.

Lower part of the program memory



If an Interrupt service routine is short enough (as is often the case in control applications) it can reside entirely within that 8-byte interval. Longer service routines can use a jump instruction to skip over subsequent interrupt locations. If other interrupts are in use. The lowest addresses of program memory can be either in the on-chip Flash or in an external memory. To make this selection, strap the External Access (EA) pin to either Vcc or GND. For example, in the AT89C51 with 4K bytes of on-chip Flash, if the EA pin is strapped to Vcc, program fetches to addresses 0000h through 0FFFh are directed to internal Flash. Program fetches to addresses 1000h through FFFFh are directed to external memory.

ADDRESSING MODES:

There are three types of addressing. They are

- Direct addressing-Nine variations.
- Indirect addressing- Nine variations.
- Indexed addressing- Nine variations.

DIRECT ADDRESSING:

In direct addressing, the operand is specified by an 8-bit address field in the instruction. Only internal data RAM and SFR's can be directly addressed.

INDIRECT ADDRESSING:

In Indirect addressing, the instruction specifies a register that contains the address of the operand. Both internal and external RAM can indirectly address. The address register for 8-bit addresses can be either the Stack Pointer or R0 or R1 of the selected register Bank. The address register for 16-bit addresses can be only the 16-bit data pointer register, DPTR.

INDEXED ADDRESSING:

Program memory can only be accessed via indexed addressing this addressing mode is intended for reading look-up tables in program memory. A 16 bit base register (Either DPTR or the Program Counter) points to the base of the table, and the accumulator is set up with the table entry number. Adding the accumulator data to the base pointer forms the address of the table entry in program memory. Another type of Indexed addressing is used in the "case jump" instructions. In this case the destination address of a jump instruction is computed as the sum of the base pointer and the accumulator data.

REGISTER INSTRUCTION:

The register banks, which contains registers R0 through R7, can be accessed by instructions whose op-codes carry a 3-bit register specification. Instructions that access the registers this way make efficient use of code, since this mode eliminates an address byte. When the instruction is executed, one of four banks is selected at execution time by the row bank select bits in PSW.

REGISTER - SPECIFIC INSTRUCTION:

Some Instructions are specific to a certain register. For example some instruction always operates on the Accumulator, so no address byte is needed to point OT. In these cases, the opcode itself points to the correct register. Instruction that rigger to Accumulator as A assemble as Accumulator - specific Opcode.

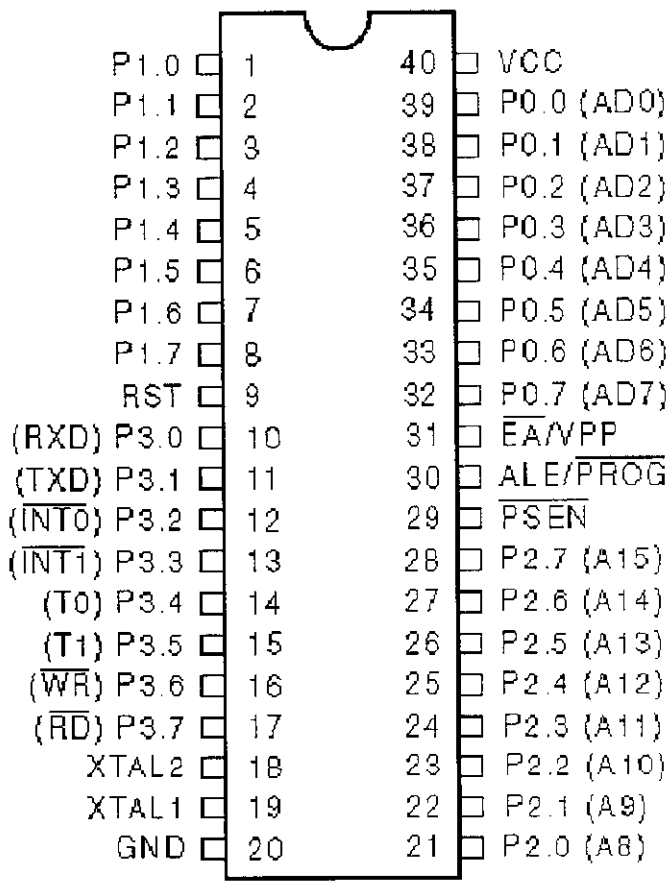
IMMEDIATE CONSTANTS:

The value of a constant can follow the opcode in program memory For example. MOV A, #100 loads the Accumulator with the decimal number 100. The same number could be specified in hex digit as 64h.

CPU TIMING:

A machine cycle consists of 6 states. Each stare is divided into a phase / half, during which the phase 1 clock is active and phase 2 half. Arithmetic and Logical operations take place during phasel and internal register - to register transfer take place during phase 2.

PIN DIAGRAM OF ATMEL 89C51 MICROCONTROLLER



TRANSMITTER

TRANSMITTER

KEY

The message plaintext that has to be kept secured in being enciphered or encoded in the p.c. The enciphering process is done using an algorithm using a C language. The enciphered message is then given to the FSK circuit where the frequency is shifted to 0's and 1's to transmit them serially. This is given to an AM circuit where it modulated by a high frequency carrier and than to the transmitting antenna.

FSK GENERATOR:

In digital data communication, shifting a carrier frequency between two preset frequencies transmits binary code. This type of transmission is called frequency shift keying technique. A 555 timer in astable mode can be used to generate FSK signals. When the input is high, transistor Q is cutoff and 555 timer works in the normal astable mode of operation. The frequency of the output waveform is given by

$F0 = 1.45/(RA+2RB)\ C$

When the input is low Q goes on and connects the resistance RC across Ra. The output frequency is given by

$F0 = 1.45/((RA*RC)+2RB)\ C$

The resistance is used to get the desired output frequency.

Frequency shift keying (FSK) is the mostly used method for transmitting digital data over telecommunications links. In order to use FSK a modulator- demodulator (modem) is needed to translate digital 1's and 0's into their respective frequencies and back again. In FSK modulation, the carrier frequency is shifted in steps (or) levels corresponding to the levels of the digital modulating signal. In case of binary signal, two carrier frequencies are used; one was corresponding to binary '0' and another to binary '1'.

Modulation:

The purpose of a communication is the source and user being physically separate from each other. To do this, the transmitter modifies the message signal into a suitable form for transmission over the channel. This modification is achieved by a process known as modulation, which involves varying some parameters of a carrier wave in accordance with the message signal. The receiver recreates the original message signal from a degraded version of the transmitted signal after propagation through the channel. A process known as demodulation, which is a reverse process of modulation used in the transmitter, achieves the recreation. However owing to the unavoidable presence of noise and distortion in the received signal, we find that the receiver cannot recreate the original message signal exactly. The type of modulation scheme used influences the resulting degradation in the overall system performance. Specifically we find that some modulation schemes are less sensitive to the effects of noise and distortion than others.

Types of Modulation:

There are basically two types of modulation

1. Frequency modulation
2. Amplitude modulation

Frequency modulation

In frequency modulation the amplitude of the modulated carrier is made constant whereas the frequency is varied in accordance with the variation in modulation signal. It has an infinite bandwidth with side bands distributed symmetrically about the carrier frequency. Here the total transmitted power is always remains constant, but with increase in depth of modulation the bandwidth can be increased. The advantages of FM are low noise, less channel interference, and many transmitters as the frequency can be used. Even though frequency modulation is advantageous over amplitude modulation, in our circuit we are using AM since it occupies less bandwidth than FM. Moreover the FM transmitting and receiving equipment is more complex and hence more expensive.

Amplitude modulation:

The amplitude of the carrier wave is varied in accordance with the amplitude of the modulating signal. Consider a sinusoidal carrier wave c (t) defined by,
c (t) = Ac cos (2*Pi*Fc*t+), where Ac is the carrier amplitude and Fc is the carrier frequency. We have assumed that the phase of the carrier wave is zero for specification of the message. The source of the carrier wave c (t) is physically independent of the source responsible for generating m(t). An amplitude-modulated wave may thus describe, in its most general form, as a function of time. In the circuit shown, Schmitt trigger NAND gate CD4011 is used. The carrier frequency is generated using the ceramic filter of value 10.7 MHz. The resistor R1 and R2 provide the necessary biasing. The modulated output is than transmitted through the antenna after passing through a capacitor. The antenna used is of aerial type. In our project the transmitted frequency is 5.5 MHz. The maximum distance to which we can transmit is around 30ft to 40ft. the distance to which it can be transmitted can be improved further by providing some amplification at the output of the amplitude modulation circuit.

IC XR – 2206:

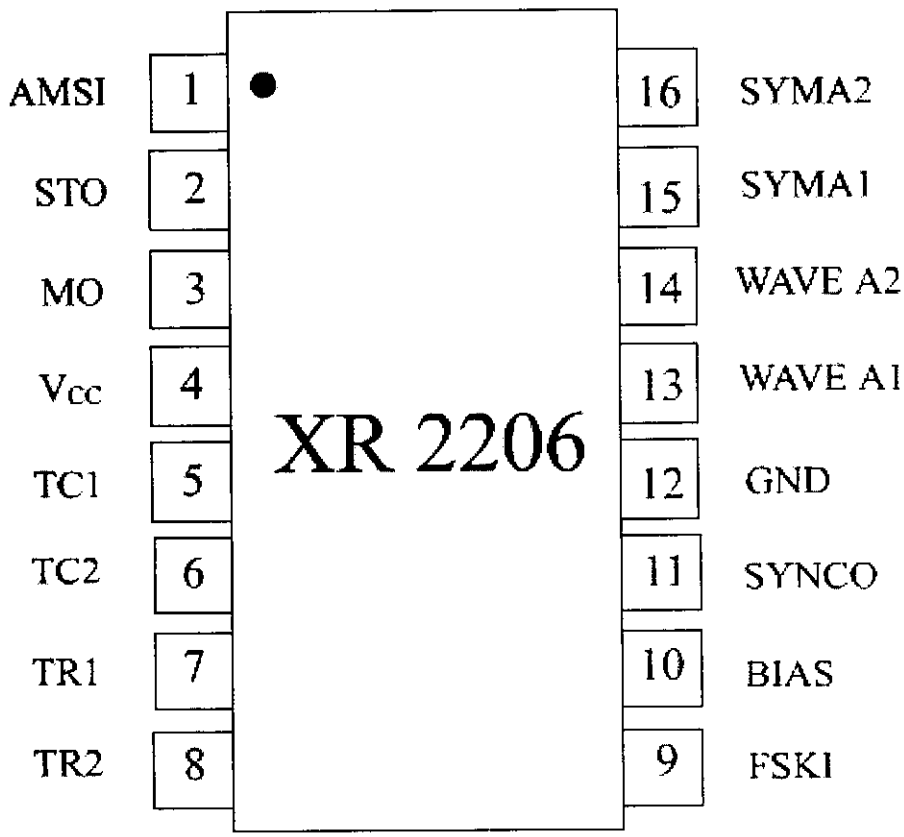
GENRAL DESCRIPTION:

The XR-2206 is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp, and pulse waveforms of high-stability and accuracy. The output waveforms can be both amplitude and frequency modulated by an external voltage. Frequency of operation can be selected externally over a range of .01Hz to more than 1MHz.The circuit is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, AM, FM, or FSK generation. It has a typical drift specification of 20ppm/°C. The oscillator frequency can be linearly swept over a 2000:1 frequency range with an external control voltage, while maintaining low distortion.

FEATURES:

- Low-Sine Wave Distortion, 0.5%, Typical
- Excellent Temperature Stability, 20ppm/°C,
- Wide Sweep Range, 2000:1, Typical
- Low-Supply Sensitivity, 0.01%V
- Linear Amplitude Modulation
- TTL Compatible FSK Controls
- Wide Supply Range, 10V to 26V
- Adjustable Duty Cycle, 1% TO 99%

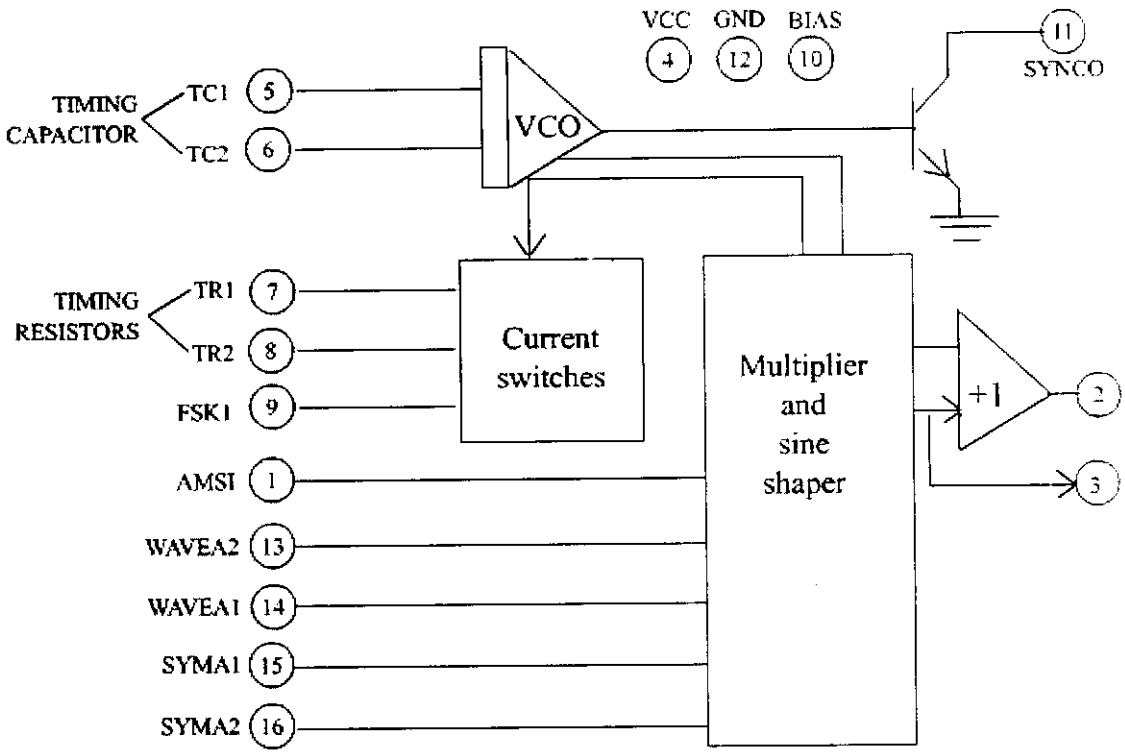
PIN DIAGRAM OF XR2206 :



PIN DISCRIPTION OF XR2206:

PIN	SYMBOL	TYPE	DESCRIPTION
1	AMSI	1	Amplitude Modulating Signal Input
2	STO	0	Sine or Triangle Wave Output
3	MO	0	Multiplier Output
4	Vcc		Positive Power Supply
5	TC1	1	Timing Capacitor Input
6	TC2	1	Timing Capacitor Input
7	TR1	0	Timing Resistor 1 Output
8	TR2	0	Timing Resistor 2 Output
9	FSKI	1	Frequency Shift Keying Input
10	BIAS	0	Internal Voltage Reference
11	SYNCO	0	Sync Output. This output is an open collector and needs a pull up resistor to Vcc
12	GND		Ground Pin
13	WAVEA1	1	Wave Form Adjust Input 1
14	WAVEA2	1	Wave Form Adjust Input 2
15	SYMA1	1	Wave Symmetry Adjust 1
16	SYMA2	1	Wave Symmetry Adjust 2

BLOCK DIAGRAM OF XR-2206



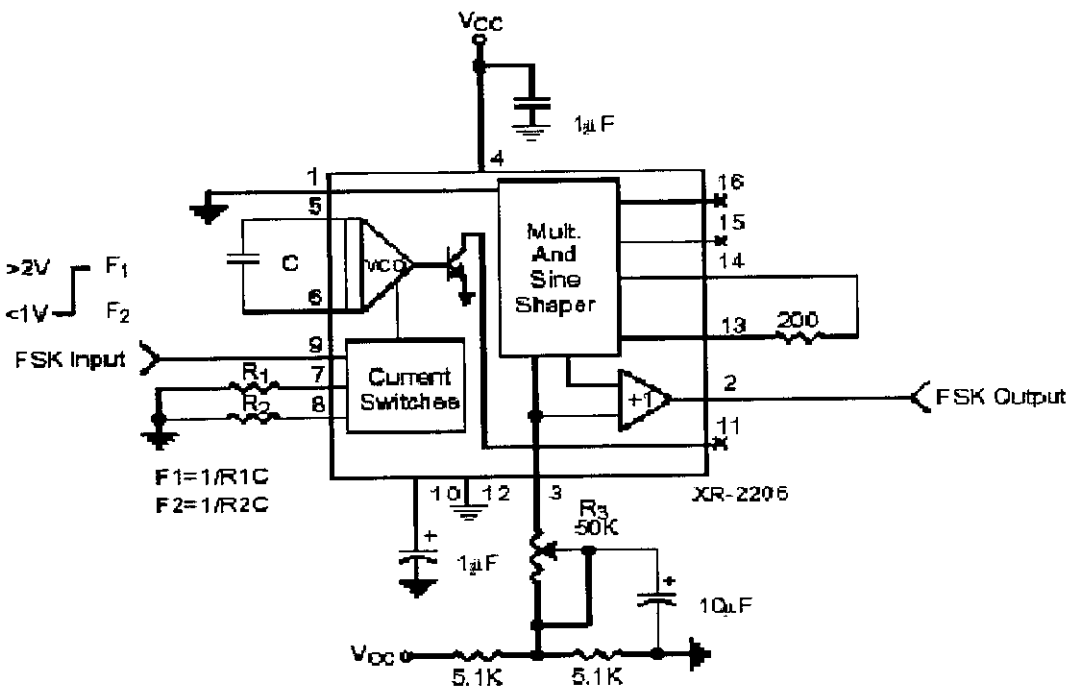
CIRCUIT DESCRIPTION:

The XR-2206 is comprised of four functional blocks, a voltage-controlled oscillator(VCO), an analog multiplier and sine-shaper; a unity gain buffer amplifier; and a set of current switches. The VCO produces an output frequency proportional to an input current, which is set by a resistor from the timing terminals to ground. With two timing pins, two discrete output frequencies can be independently produced for FSK generation applications by using the FSK input control pin. This input controls the current switches, which select one of the timing resistor currents, and routes it to the VCO.

FREQUENCY SHIFT KEYING:

The XR-2206 can be operated with two separate timing resistors, R1 and R2, connected to the timing Pin 7 and 8, respectively, as shown in Figure. Depending on the polarity of the logic signal at Pin 9, either one or the other of these timing resistors is activated. If Pin 9 is open-circuited or connected to a bias voltage • 2V, only R1 is activated. Similarly, if the voltage level at Pin 9 is • 1V, only R2 is activated. Thus, the output frequency can be keyed between two levels; fl and f2, as fl = 1/R1C and f2 = 1/R2C. For split-supply operation, the keying voltage at Pin 9 is referenced to V-.

FSK GENERATION:



FSK Generator:

The circuit connection for FSK signal operation. Mark and space frequencies can be independently adjusted by the choice of timing resistors, R1 and R2; the output is phase-continuous during transitions. The pin 9 FSK input terminal of the XR-2206 can also be used to provide the waveform generator with frequency-shift keyed (FSK) operation, as shown in figure. Here, a keying or pulse waveform is fed directly to pin 9, and the circuit action is such that when this keying waveform is greater then + 2 V relative to the negative supply rail pin 7's R1 timing resistor is selected, but when the keying waveform is below +1b V (relative to the negative supply rail) pin 8's R2 timing resistor is selected instead. The FSK signal thus enables either of two operating tones to be selected.

APPLICATIONS:

- Waveform Generation
- Sweep Generation
- AM/FM Generation
- V/F Conversion
- FSK Generation
- Phase-Locked Loops (VCO)

RECEIVER

Three terminal ceramic filters:

The terminal ceramic filters are used in the transmitter and receiving circuits to generate the carrier frequency and to get the desired band of frequencies. It is also used to suppress the unwanted signals and noise from the received signal. A 5.5 MHz ceramic filter is used in this project to generate the carrier frequency in the transmitter side. The same filter is used in the receiver side to obtain the desired band of frequency from the received signal.

Diode Demodulation:

Demodulation:

The process of recovering the original modulation signal from a modulated wave is termed as demodulation or detection. Basically, the demodulation or detection is a process of frequency translation that requires a non-linear device in which the signal lying at a higher frequency in the frequency spectrum are converted to a lower frequency converter circuits are also termed as detectors.

AM Detectors:

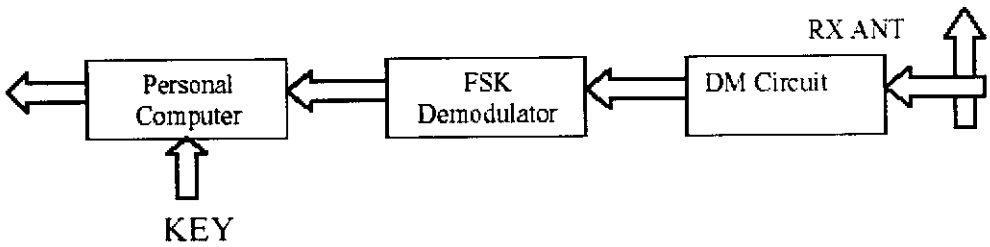
The envelope of an amplitude-modulated signal follows the wave shape of the modulating signal. A detector circuit whose output follows the peak of the carrier will, therefore, reproduce the modulating signal. Such a detector may be termed as peak detector or envelope detector. The circuit employs the linear region of a diode characteristic for this purpose. As such, the circuit is also termed as linear-diode detector. For linear region operation, the input signal strength required is relatively large. AM detectors consists of diode connected in series to a parallel combination of R and Cosine the diode is operated in linear region, the output voltage is proportional to the input signal voltage during the positive half cycle.

During the negative half cycle, there is no conduction in the diode but the output voltage is maintained by the capacitor which discharges during this period. The extent of

RECEIVER SECTION

RECEIVER:

The part of telecommunication system that converts transmitted waves into a desired form of output .A complete apparatus for the, reception of incoming electrically transmitted messages, signals, etc.



FET Amplifiers:

Field Effect transistor is a semiconductor device in which current is controlled by an electric field. In the conventional transistor the operation depends on the flow of carriers of both types namely electrons and holes. The operation of FET depends on the flow of majority carriers only. Hence FET is a unipolar device. It has an advantage of high input impedance.

Filters:

The filters are used to obtain the desired band of frequency and to suppress the unwanted signals and noise. Filters are of different types. But the ceramic filters are most commonly used for carrier frequency generation and band selection. The ceramic filters are used because of their accurate frequency tuning.

charge and discharge of the capacitor depends upon the time constant CR. If the time constant is chosen correctly, the output voltage will follow the modulation envelope very closely. An appropriate filter filters out the RF ripple and the DC component is blocked by a series capacitor. A small-time constant CR results in an output voltage that falls off considerably during the non conduction period of the diode and may not follow modulation envelope. The output is quite low and contains a high RF ripple. An increased time constant CR results in a marginal output and the output follows modulation envelope. A further increase in time constant makes the discharge rate of the capacitor very low and the discharge curve become almost horizontal.

Phase-Locked Loops:

Introduction:

The phase locked loop (PLL) is an important building block of linear systems. Electronic phase locked loop (PLL) came into vogue in the 1930's when it was used for radar synchronization and communication applications. The high cost of realizing PLL, in discrete form limited its use earlier. Now with the advanced IC technology, PLL's are available as inexpensive monolithic IC's. This technique for electronic frequency control is used today in satellite communication systems, computers, and etc. The basic principle of PLL, different IC's and important applications are discussed.

Basic Principle:

The feedback system consists of,

1. Phase detector/comparator.
2. A low pass filter.
3. An error amplifier.
4. A Voltage Controlled Oscillator.

The VCO is a free running multi-vibrator and operates at a set frequency f0 called free running frequency. An external timing capacitor and an external resistor determine

this frequency. It can also be shifted to either side by applying a dc control voltage Vc to an appropriate terminal of the IC. The frequency deviation is directly proportion to the dc control voltage and hence it is called a "Voltage controlled Oscillator" or, in short VCO. If an input signal Vs of frequency fs is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output V0 of the VCO. If the two signals differ in frequency and/or phase, an error voltage Ve is generated. The phase detector is basically a multiplier and produced the sum (fs+f0) and difference (fs-f0) components at its output.

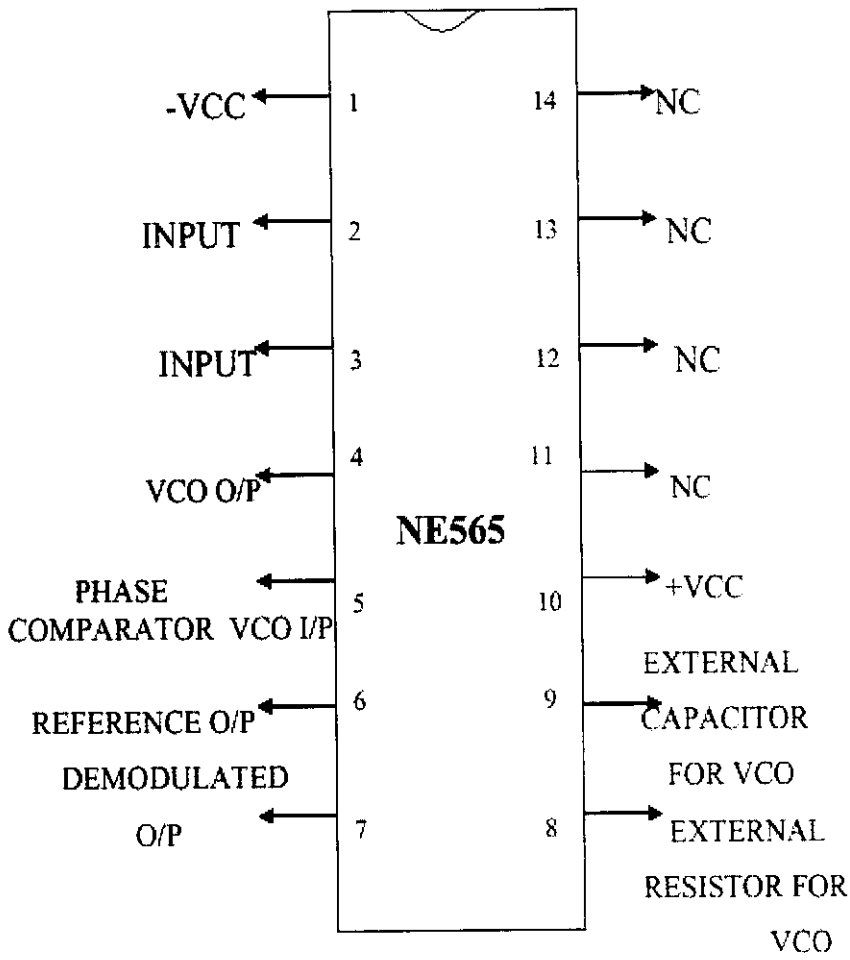
The high frequency component (fs+f0) is removed by the low pass filter and the difference frequency component is amplified and then applied as control voltage Vc to VCO.The signal Vc shifts the VCO frequency in a direction to reduce the frequency difference between fs and f0. Once this action starts, we say that the signal is in the capture range. The VCO continues to change frequency. The circuit is then said to be locked. Once locked, the output frequency f0 of VCO is identical to fs except for a finite phase difference. This phase difference generated a corrective control voltage Vc to shift the VCO frequency from f0 to fs and thereby maintain the lock. Once locked, PLL tracks the frequency changes of the input signal. Thus, a PLL goes through three stages,

- Free running,
- Capture, and
- Locked or tracking.

As capture starts, a small sine wave appears. This is due to the frequency difference between the VCO and the input signal. The dc component of the beat drives the VCO towards the lock. Each successive cycle causes the VCO frequency to move closer to the input signal frequency. The frequency difference becomes smaller and the filter, shifting the VCO frequency further, passes a larger dc component. The process continues until the VCO locks on to the signal and the difference frequency is dc. The low pass filter controls the capture range. If VCO frequency is far away, the beat frequency will be too high to pass through the filter and the PLL will not respond. We say that the signal is out of the capture band. However, once locked, the filter no longer.

restricts the PLL. The VCO can track the signal well beyond the capture band. Thus tracking range is always larger than the capture range.

PIN DIAGRAM OF NE565



IC PLL 565:

The phase detector of this PLL is comprised of differential amplifier pairs provided with current sink bias source. The output voltage phase detector is limited by diodes to maximum of +0.7V. This limiting action helps to minimize the effect of high amplitude noise pulses and other transient effects on the operation of the PLL.The phase detector has a balanced output and is supplied to the differential amplifier pair, which serves an amplifier stage in amplifying the phase detector; output a single ended output is taken from this stage from across the load resistor R1 and connected internally to the VCO.

Connection of an external capacitor C between Pin 7 and ground will produce a first order low-pass (lag) network. A capacitor C and a resistor R2 connected in series between pin 7 and ground will result in lag lead network. The VCO consists of a voltage controlled current source, which supplies equal magnitude of charging and discharging currents to an externally connected (pin 9) timing capacitor C0. A timing resistor is connected between pin8 and positive power supply. The rest of the VCO circuit is Schmitt trigger with a differential amplifier output circuit. This controls the turn-on and turn-off for the switching action of the current source for the charging and discharging.

CIRCUIT DESCRIPTION:

AM RECEIVER:

These receivers can be used to receive the speech or music radiated from AM broadcast transmitting operating on long wave, medium wave or short wave band. The encoded message has to now be decoded. The encoded message is received by receiving antenna and than given to demodulator circuit. This is then given to a DFSK circuit where 0's and 1's are separated out by using carrier at two different frequencies. Then the output is given to a P.C where message is decoded using the same algorithm as in encipherment process and the original message is taken out.

ENVELOPE DETECTOR:

An envelope detector is a simple and yet highly effective device that is well suited for the demodulation of a narrow band AM wave, for which the percentage modulation is less than 100%. Ideally, an envelope detector produces an output signal that follows the envelope of the input signal waveform. Envelope detector consists of a diode and a resistor-capacitor filter. The operation is as follows. On the positive half-cycle of the input signal, the diode is forward-biased and the capacitor C charges up rapidly to the peak value of the input signal. When the input signal falls below this value, the diode becomes reverse biased and the capacitor C discharges slowly to the load resistor RI. The discharging process continues until the next positive half cycle. When the input signal becomes greater than the voltage across the capacitor, the diode conducts again and the process is repeated. Thus the demodulation is carried out.

In our circuit we are using 0A79 diode. In digital data communication and computer peripheral, binary data is transmitted by means of a carrier frequency, which is shifted between two preset frequencies. This type of data transmission is called frequency shift keying (FSK) technique. The binary data can be retrieved using FSK demodulators at the receiving end. The 565 PLL is a very useful as a FSK demodulator. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding and the DC shift at the output. A three-stage filter removed the carrier component and the output signal is made logic compatible by the voltage comparator.

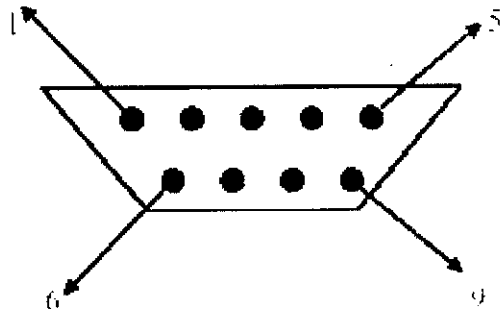
RS232 CABLE

RS-232C SERIAL DATA STANDARD

In the 1960s as the use of time-share computer terminals became more widespread; modems were developed so that terminals could use phone lines to communicate with distant computers. As we stated earlier, modems and other devices used to send serial data are often referred to as data communication equipment or DCE. The terminals or computers that are sending or receiving the data are referred to as data terminal equipment or DTE. In response to the need for signal and handshake standards between DTE and DCE, the Electronic Industries Association (EIA) developed EIA standard RS-232C. This standard describes the functions of 25 signal and handshake pins for serial data transfer. It also describes the voltage levels. Impedance levels, rise and fall times, maximum bit rate, and maximum capacitance for these signal lines. Before we work our way through the 25 pin functions, we will take a brief look at some of the other hardware aspects of RS-232C.

RS-232C specifies 25 signal pins and it specifies that the DTE connector should be a male, and the DCE connector should be a female. A specific connector is not given, but the most commonly used connectors are the DB-25P male and the DB-25S female shown in figure, when you are wiring up these connectors. It is important to note the order in which the pins are numbered. The voltage levels for all RS-232C signals are as follows. A logic high, or mark, is a voltage between –3V and –15 V under load (-25 V no load). A logic low or space is a voltage between +3 V and +15 under load (+25 V no load). Voltage such as 12 V is commonly used. The output signal level usually swings between +12V and -12V. The "dead area" between +3v and -3v is designed to absorb line noise. In the various RS-232-like definitions this dead area may vary. For instance, the definition for V.10 has a dead area from +0.3v to -0.3v. Many receivers designed for RS-232 are sensitive to differentials of 1v or less.

DP9 PIN CONNECTOR



RS232 Pin Assignments	
Pin 1	Received Line Signal Detector (Data Carrier Detect)
Pin 2	Received Data
Pin 3	Transmit Data
Pin 4	Data Terminal Ready
Pin 5	Signal Ground
Pin 6	Data Set Ready
Pin 7	Request To Send
Pin 8	Clear To Send
Pin 9	Ring Indicator

PIN DESCRIPTION:

1. DTR (Data terminal ready):

When the terminal is turned on, after going through a self-test, it sends out signal DTR to indicate that it is ready for communication.

2. DSR (Data set ready):

When DCE is turned on and has gone through the self-test, it asserts DSR to indicate that it is ready to communicate.

3. RTS (Request to send):

When the DTE device (such as a pc) has a byte to transmit, it asserts RTS to signal the modem that it has a byte of data to transmit.

4. CTS (clear to send):

In response to RTS when the modem has room for storing the data it is to receive, it sends out signal CTS to the DTE (PC) to indicate that it can receive the data now.

5.DCD (data carrier detect):

The modem assert signal DCD to inform the DTE (PC) that a valid carrier has been detected and that contact between it and the other modem is established.

6.RI (ring indicator):

An output from the modem (DCE) and an input to a PC (DTE) indicates that the telephone is ringing. It goes on and off in synchronization with the ringing sound.
While signals DTR and DSR are used by the pc and modem respectively, to indicate that they are alive and well, it is RTS and CTS that actually control the flow of data. RTS and CTS are also referred to as hardware control flow signals. This concludes the description of the 9 most important pins of the RS232 handshake signals plus TxD, RxD, and ground. ground is also referred to as SG (signal ground).

APPLICATIONS

The main motto of our project is to continuously track the vehicle and find the location of the vehicle and find the place of accident. Various applications of our project are listed below

- Invaluable lives can be saved by implementing this system.
- The vehicle can be monitored from a distant location.
- The various parameters are visually displayed on a remote PC.
- Incase of theft we can easily identify the vehicle.
- In military applications, the vehicle can be continuously monitored thereby facilitating safe transfer of arms and ammunition.

FUTURE ENHANCEMENT

We can implement our project by linking with satellite; with these help we can find the position of the vehicle anywhere in the world. It can be used in automatic road traffic control. In our project vehicle immobilizer can also be added. In case of LPG driven vehicles gas leakage can be detected and fire sensors also added. On further development the vibration sensor can also be directly connected to the cell phone thus enabling a fast medical aid.

CONCLUSION

This HIGHWAYS ACCIDENT IDENTIFICATION SYSTEM helps as to find the location or position of vehicle. Direction sensor is used to find the direction of vehicle. The vibration sensors are used to indicate the accident the output of these sensors is fed in to the micro controller. The micro controller ATMEL89C51 is the heart of our system. The data from the micro controller are transmitted and received by digital demodulation techniques. The signals from the receiver are fed in to pc through RS232 cable. In pc a visualize map is shown from that we can observe the direction of the vehicle. The speed of the vehicle is displayed on the monitor. If accident occurs an alert beep sound is heard and accident message will be displayed. The main motto of our project is to find location of the vehicle, where an accident took place. By implementing this project it is very helpful to save the people immediately.

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ABBREVIATION

AC - Alternating Current

DC - Direct Current

CMOS - Complementary MOSFET

DCE - Data Communication Equipment

DTE - Data Terminal Equipment

EPROM - Erasable Programmable Read Only Memory

I/P - Input

O/P - Output

IC - Integrated Circuit

LED - Light Emitting Diode

I/O - Input, Output

OP-AMP - Operational Amplifier

PC - Personal Computer

RAM - Random Access Memory

ROM - Read Only Memory

PLL - Phased Locked Loop

VCO - Voltage Controlled Oscillator

IR - Infra Red

DATA SHEETS

ures

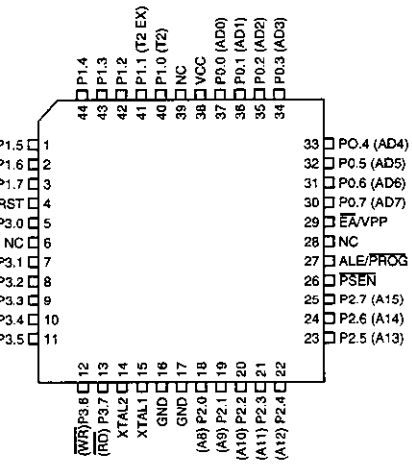
patible with MCS-51™ Products
ytes of In-System Reprogrammable Flash Memory
Endurance: 1,000 Write/Erase Cycles
Static Operation: 0 Hz to 24 MHz
e-level Program Memory Lock
x 8-bit Internal RAM
rogrammable I/O Lines
16-bit Timer/Counters
nterrupt Sources
grammable Serial Channel
-power Idle and Power-down Modes

cription

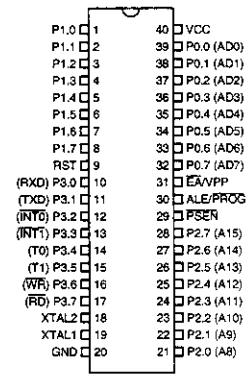
T89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K of Flash programmable and erasable read only memory (PEROM). The device nufactured using Atmel's high-density nonvolatile memory technology and is atible with the industry-standard MCS-51 instruction set and pinout. The on-chip allows the program memory to be reprogrammed in-system or by a conven- nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash nonolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides ly-flexible and cost-effective solution to many embedded control applications.

Configurations

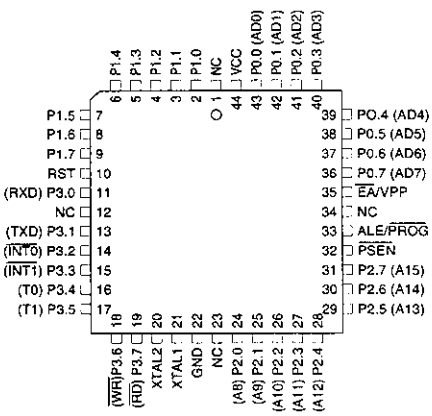
PQFP/TQFP



PDIP



PLCC



8-bit Microcontroller with 4K Bytes Flash

AT89C51

Rev. 0265G–02/00

T89C51 provides the following standard features: 4K of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit counters, a five vector two-level interrupt architecture, duplex serial port, on-chip oscillator and clock cir- In addition, the AT89C51 is designed with static logic eration down to zero frequency and supports two are selectable power saving modes. The Idle Mode the CPU while allowing the RAM, timer/counters, port and interrupt system to continue functioning. The r-down Mode saves the RAM contents but freezes cillator disabling all other chip functions until the next are reset.

Description

y voltage.

nd.

)

) is an 8-bit open-drain bi-directional I/O port. As an t port, each pin can sink eight TTL inputs. When 1s ritten to port 0 pins, the pins can be used as high- dance inputs.

) may also be configured to be the multiplexed low- address/data bus during accesses to external pro- and data memory. In this mode P0 has internal os.

) also receives the code bytes during Flash program- , and outputs the code bytes during program cation. External pullups are required during program cation.

1

1 is an 8-bit bi-directional I/O port with internal pullups. Port 1 output buffers can sink/source four TTL inputs. n 1s are written to Port 1 pins they are pulled high by nternal pullups and can be used as inputs. As inputs, 1 pins that are externally being pulled low will source nt (I_{IL}) because of the internal pullups.

1 also receives the low-order address bytes during programming and verification.

2

2 is an 8-bit bi-directional I/O port with internal pullups. Port 2 output buffers can sink/source four TTL inputs. n 1s are written to Port 2 pins they are pulled high by nternal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and verification.

RST

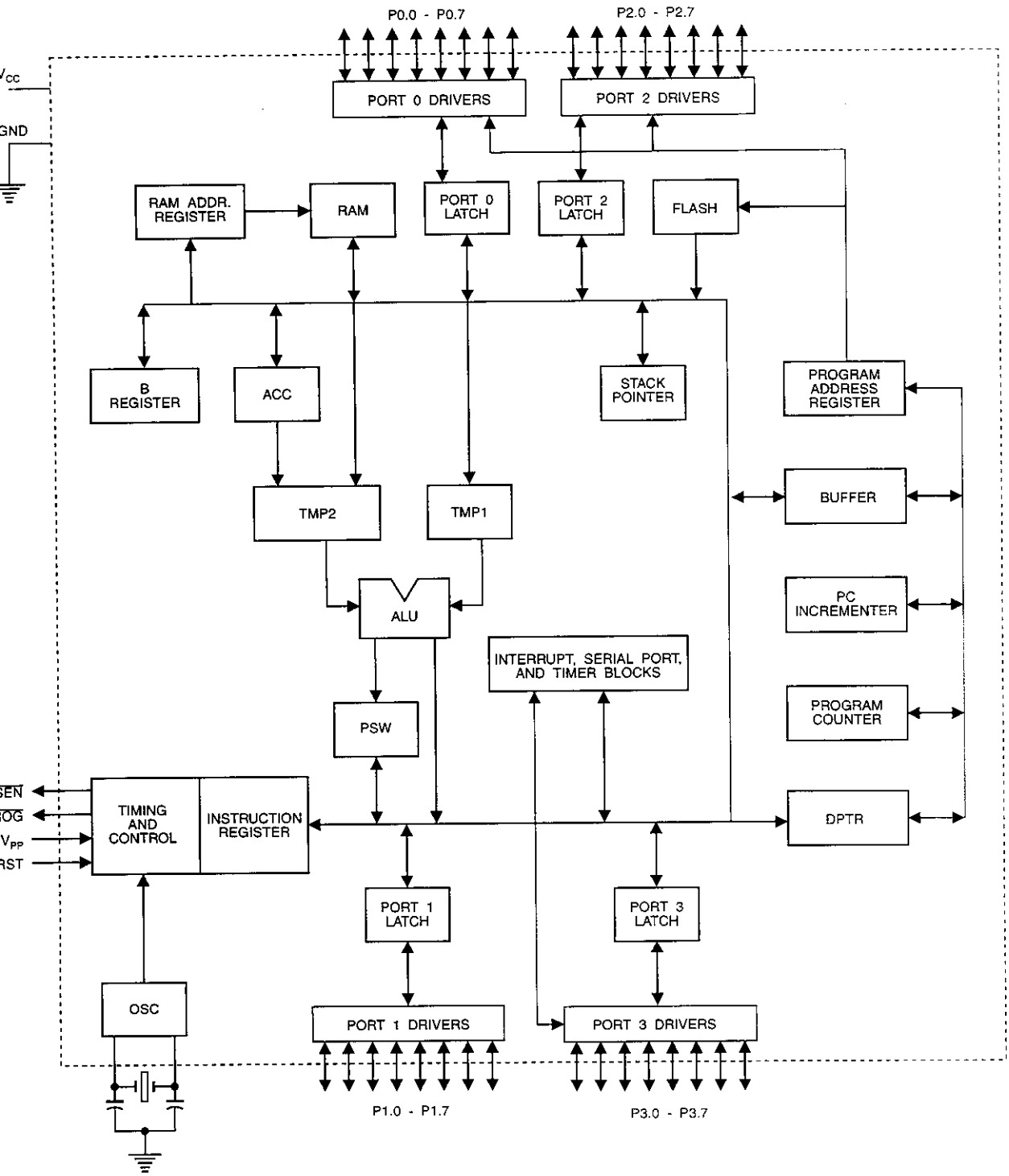
Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE

k Diagram


P0.0 - P0.7
P2.0 - P2.7
PORT 0 DRIVERS
PORT 2 DRIVERS
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
BUFFER
TMP2
TMP1
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PROGRAM COUNTER
PSW
TIMING AND CONTROL
INSTRUCTION REGISTER
DPTR
PORT 1 LATCH
PORT 3 LATCH
OSC
PORT 1 DRIVERS
PORT 3 DRIVERS
P1.0 - P1.7
P3.0 - P3.7

is skipped during each access to external Data
y.

ed, ALE operation can be disabled by setting bit 0 of
cation 8EH. With the bit set, ALE is active only dur-
MOVX or MOVC instruction. Otherwise, the pin is
y pulled high. Setting the ALE-disable bit has no
f the microcontroller is in external execution mode.

am Store Enable is the read strobe to external pro-
nemory.

the AT89C51 is executing code from external pro-
memory, $\overline{PSEN}$ is activated twice each machine
except that two $\overline{PSEN}$ activations are skipped during
access to external data memory.

PP

nal Access Enable. $\overline{EA}$ must be strapped to GND in
to enable the device to fetch code from external pro-
memory locations starting at 0000H up to FFFFH.
however, that if lock bit 1 is programmed, $\overline{EA}$ will be
ally latched on reset.

nould be strapped to V_{CC} for internal program
tions.

in also receives the 12-volt programming enable volt-
V_{PP}) during Flash programming, for parts that require
t V_{PP}.

1

to the inverting oscillator amplifier and input to the
al clock operating circuit.

2

t from the inverting oscillator amplifier.

illator Characteristics

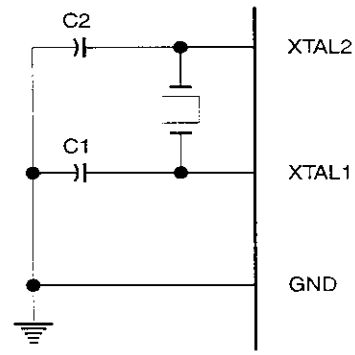
1 and XTAL2 are the input and output, respectively,
inverting amplifier which can be configured for use as
-chip oscillator, as shown in Figure 1. Either a quartz
al or ceramic resonator may be used. To drive the
e from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when idle is terminated by a hard ware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Figure 1. Oscillator Connections

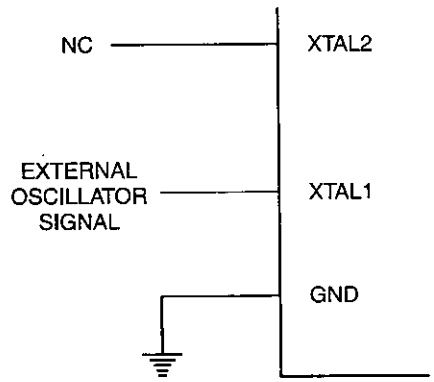


Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

us of External Pins During Idle and Power-down Modes

e	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
	Internal	1	1	Data	Data	Data	Data
	External	1	1	Float	Data	Address	Data
r-down	Internal	0	0	Data	Data	Data	Data
r-down	External	0	0	Float	Data	Data	Data

2. External Clock Drive Configuration



er-down Mode

power-down mode, the oscillator is stopped, and the ction that invokes power-down is the last instruction ted. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. The only exit from power-down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

k Bit Protection Modes

	Program Lock Bits			
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash is disabled
3	P	P	U	Same as mode 2, also verify is disabled
4	P	P	P	Same as mode 3, also external execution is disabled

ramming the Flash

T89C51 is normally shipped with the on-chip Flash y array in the erased state (that is, contents = FFH) ady to be programmed. The programming interface :s either a high-voltage (12-volt) or a low-voltage program enable signal. The low-voltage program- mode provides a convenient way to program the C51 inside the user's system, while the high-voltage mming mode is compatible with conventional third- Flash or EPROM programmers.

T89C51 is shipped with either the high-voltage or ltage programming mode enabled. The respective de marking and device signature codes are listed in lowing table.

	V_{PP} = 12V	V_{PP} = 5V
Side Mark	AT89C51 xxxx yyww	AT89C51 xxxx-5 yyww
ature	(030H) = 1EH (031H) = 51H (032H) =F FH	(030H) = 1EH (031H) = 51H (032H) = 05H

T89C51 code memory array is programmed byte-by- n either programming mode. *To program any non- byte in the on-chip Flash Memory, the entire memory be erased using the Chip Erase Mode.*

ramming Algorithm: Before programming the C51, the address, data and control signals should be according to the Flash programming mode table and e 3 and Figure 4. To program the AT89C51, take the ing steps.

1. put the desired memory location on the address nes.
2. put the appropriate data byte on the data lines.
3. ctivate the correct combination of control signals.
4. aise $\overline{EA}/V_{PP}$ to 12V for the high-voltage program- ing mode.
5. ulse ALE/$\overline{PROG}$ once to program a byte in the lash array or the lock bits. The byte-write cycle is elf-timed and typically takes no more than 1.5 ms.
6. epeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89C51 features $\overline{Data}$ Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The code array is written with all "1"s. The chip erase operation must be executed before the code memory can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H, 031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(030H) = 1EH indicates manufactured by Atmel
(031H) = 51H indicates 89C51
(032H) = FFH indicates 12V programming
(032H) = 05H indicates 5V programming

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.