TELEMATICS BASED HOME APPLIANCES CONTROLLER-

EMBEDDED SYSTEM

PROJECT REPORT

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In partial fulfillment of the requirements for the

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

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CERTIFICATE

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Head of the Department

Certified that the candidate _____ with University Register No._____ was examined in Project work Viva-Voce Examination on 12.03.04

DEDICATED TO ALMIGHTY GOD

ACKNOWLEDGEMENT

ACKNOWLEDGEMENT

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SYNOPSIS

SYNOPSIS

Today's world which revolves around the word Time Management and the Hitech automation requiring remote controlling of appliances. It is a field which aims to bringing the whole world to our finder tips and thus making our lives more comfortable and easy going.

This is achieved by the characteristic of PIC, PIC switching operation can be controlled by telephone or cell phone. The tele switch is capable of controlling up six mains powered loads with the aid of the commands received via telephone. Any tone dialing (DMTF) telephone set may be used to send commands to the switching unit and remotely control a wide range of main appliances in and around the home. On being called, the circuit waits for a predetermined period and then answers the call. Next it waits for a pre-programmed system access code, which the caller must transmit the DTMF keypad on telephone.

CONTENTS

CONTENTS

CERTIFICATE i

ACKNOWLEDGEMENT iv

SYNOPSIS vi

CONTENTS viii

1. INTRODUCTION

1.1 Need for DTMF 2

1.2 Telephone Unit 3

1.3 Tones used in Automatic Telephony 7

2. BLOCK DIAGRAM

2.1 General Explanation 10

2.2 Block Diagram 11

3. SWITCHING CIRCUIT

3.1 Ringer Circuit 13

3.2 Loop Enabling Circuit 15

3.3 DTMF 18

4. PERIPHERAL INTERFACE CONTROLLER

4.1 Why PIC? 27

4.2 Architecture of PIC16F4A 28

4.3 Memory Organisation 29

4.4 Input and Output Ports 33

4.5 Timer0 37

4.6 Instruction set summary 38

4.7 Oscillator 42

4.8 Resets 44

5. POWERSUPPLY UNIT

5.1 Introduction 48

5.2 Power Supplies 50

6. FABRICATION AND TESTING OF THE CIRCUIT

6.1 Circuit Operation 53

6.2 Salient features of the circuit 54

7. CONCLUSION 57

REFRENCES

APPENDICES

INTRODUCTION

1. INTRODUCTION

Current scenario demands that an individual's focus be mainly directed towards his / her time management at the most economizing and effective way. In mostly people look forward for facilities that could be remotely controlled thus eliminating the need for physical presence of the person and save time from waiting in most economical way. Here the embedded system provides us with a key to this problem. Our project provides the solution for the above problem. A process that goes for remotely controlled appliances, enabling an individual at an unreachable distance to access appliances to change its status of functioning resulting in a good time management.

1.1 NEED FOR TONE DIALING (DTMF)TELEPHONE

The earliest automatic exchanges provided cheaply for automatic call for subscribers on the same exchanges. Although in some cases automatic calls could be made to subscribers on a neighboring automatic exchange. For most part, calls to subscribers on the other exchanges had to be passed through an operator in large urban areas, this was a disadvantage since the large proportions of the telephone calls are made between subscribers on different exchanges. However it was year before fully automatic working between subscribers in large conurbations become possible and wide adoption of automatic exchange could proceed. The improvements in long distance transmission techniques have not only reduced circuit cost to a fraction of their former value but has also greatly improved the quality of transmitted speech. A substantial improvement over the rotary telephone dials was accomplished through the uses of push button dialing called touch-tone. This was made possible as a solid state technology and for a more rapid and accurate means of customer dialing. This method also provides means for communication between the customer's telephone and other associated equipment. The rotary dial could not provide this service since it could control only telephone company local central office equipment. The tone dialing system makes use of tones instead of pulses. Each dialed digit is represented by a unique pair of sine wave tones , and the tone pair, is sent to the phone company office as each digit is pushed on the phone. The numbers are arranged four row by three column rectangular matrix. Each row and column has a unique tone. When a key corresponding to a digit is pushed ,the tones for its row and column are transmitted. The technical name for this scheme is dial tone multi

1.1.1 ADVANTAGES OF DTMF:

The advantages of using DTMF are in the areas of both the usefulness of the tones and the circuitry ,which can be used to determine which tones are sent.
The usefulness of DTMF is enhanced in following ways:

1. The time to send a complete number is greatly reduced. A three digit phone number taken only 1.25 sec, regardless of the digits, using the .25 sec value for tone and inter tones times. The average person can send a seven-digit number in 3.25 sec. this means that the phone circuits are tied for much less time with dialing information.
2. The time to send a number is the same regardless of the actual digits themselves. All the seven digit numbers take the same time, all long distance numbers (1+area code + number) take amount of time. The circuitry to receive this is easier to design.
3. The tones can be used for signaling purposes once the dialing is over. The phone system is designed to ignore any and all frequencies within the frequency band that the voice uses since circuitry assigned to take some specific action once the call is established may be accidentally tripped by the user voice. The tones can therefore be used to turn on the equipment or send coded message to the system at the other end.
4. This is in contrast to the pulse dialing signals, in which the phone system is designed to look, at all tones ,for the opening of the loop to the phone, since this indicates that phone has hung up.

1.2 TELEPHONE UNIT

Telephone unit is nothing but the receiver set in our home. Inside, which are some electronic circuit to receive the signal when calling person dials a number. In a subscriber's telephone set , they are the following parts

1. Telephone hand set
2. Dialer
3. ASTIC coil
4. Ringing bell

1.2.1 TELEPHONE HAND SET

The telephone hand set consists of two parts namely, the transmitter or the micro phone and the receiver both fitted in a bakelite mounted hand set which can be easily taken up hand for use. The microphone is used for converting speech sounds in electrical currents and is placed in front of the mouth. The receiver is used to convert the electrical currents into speech sounds and is therefore held in front of the ear during conversation.

The speech sounds consists of frequency ranging from 100-3000 hertz. Therefore the transmitter and receiver must be capable of handling atleast the frequencies speech consists of many words made of vowels and consonant vowels contain very low frequency fundamentals but have greater acoustic power consonants have much higher frequency components and in addition to steady waves they contain transients. These high frequencies are responsible for the quality of speech.

(a) TELEPHONE RECEIVER

The receiver consists of permanent magnet or horseshoe type having two pole pieces in front of which there are two coils carrying a steady value of d.c current. In front of these coils ,there is a diaphragm made of alloy of 10 mils thickness and of diameter of about two inches.

When speech sounds impinge on the diaphragm, it vibrates and so the flux due to permanent magnet varies and this varying flux induces alternating emf in coils varying currents flowing through the same type of instruments at the receiving end produce again change of flux and so the pull on the diaphragm varies and so it vibrates and speech sounds are produced.

(b) MODERN INSET TRANSMITTER:

This is an improved type of carbon microphone transmitter. This is known as an post office transmitter.

1. The improvements that are incorporated in this type are stated below, it is an immersed type of carbon transmitter .the carbon electrodes are completely

insulated chamber. This ensures uniform pressures of carbon granules on the carbon electrodes in all position of the carbon microphones. The quiet resistance of microphone is thus same in whatever position it is held. This has got an advantage in telephone sets where are held in different positions during use by different subscribers.

2. The diaphragm is very light and stiff and is made of duralumine and moving electrode is also very light . The mass of the moving parts is $1/10^{th}$ the mass in the case of solid back type. The sensitivity is thus much higher in this case .
3. The moving system is free from damping and is also very light ,consequently there is an improvement in the overall performance of the transmitter.
4. The granules used are of hard furnished carbon of selected grain and size, and this also ensures uniform performance of the transmitter.
5. The silk and mice washers keep the carbon granule in the carbon chambers . but at the same time , they offer little resistance to the movement of carbon values and to the carbon electrodes and thus more sensitive and uniform output is obtained .
6. The breathing hold keep the temperature and pressure of the carbon chamber equal to that of the outside atmosphere thus making the instrument performance independent of outside conditions.

The overall frequency characteristics depend upon the following factors.

1.Constants of diaphragm such as mass, mechanical resonance etc.

2.Constants of the mass of the air.

3.Nature of the mouth piece.

4.Type of carbon granules and its packing.

1.2.2 DIALER

The dialer circuit produces current pulses in the line while dialing the number of a subscriber. In conventional telephone sets, the dialer makes / breaks mechanically, producing pulses of current of duration. In electronic telephones, electronic dialer circuit is employed for this purpose. The rotary dial is replaced by a keypad.

1.2.3 ASTIC COILS

Side tone is the tone or speech sounds heard by the subscribers in his own telephone receiver when he speaks on his microphones. Too much of this side tones is not desirable in a telephone sets and the coil arrangement that is used to achieve. This is known as Ant side tone induction coils (ASTIC).

1.2.4 RINGING BELL

This circuit gives audible signals to attract the attention of the subscriber to an incoming telephone all. Electromagnetic bell is commonly used for this purpose in conventional telephones but in electronic telephones, the ringer comprises of an electronic circuit that gives AF signals to a piezo transducer or to the telephone receiver when a call is incoming.

1.2.5 CRADLE SWITCH

This switch is used to connect / disconnect the ringer and speed circuits to the line. When telephone handset is on the cradle (called ON-HOOK condition), the speech circuit is disconnected, but ringer is connected to the line, so that the ringer can given an indication in case a call is incoming. OFF-HOOK condition, ringer is disconnected and speech circuit is connected to the line.

1.3 TONES USED IN AUTOMATIC TELEPHONY

Four different types of types are used and these are known as

a. Dial tone
b. Busy tone
c. Ringing tone.
d. N.U. Tone

1.3.1 DIAL TONE:

In order that the subscriber may dial only after his lines are connected to a free first selector switch in the automatic exchange, it is necessary to give some indication to that subscriber when he should start dialing and this is indicated by sending a tone called dial tone from the telephone exchange. No subscriber must dial before he obtains this dial tone. This tone is a continuous burble sound of low frequency of 400 Hz modulated by 25 Hz.

1.3.2 BUSY TONE

When the call subscriber is engaged with the some other call, this should also be indicated to the calling subscriber, as the later cannot get connection with the former. The connection cannot be established if free trunks are not available throughout within the automatic exchange and this also should be indicated to the calling subscriber . in either case sending another tone is known as busy sends the indication

Tone and its consisted of 400 Hz, which is regularly interrupted at equal intervals. It is generally on for 0.75 secs and off for also 0.75 secs, and this is continuously sent

1.3.3 RINGING TONE

It may be that the telephone of the called subscriber, although ringing is not attended due to either to the absence o any person or due to any other cause. In such cases also the calling subscriber should get this information and this is indicated by sending ringing tone interrupted 400 Hz, modulated by 25 Hz. It may be 0.4 sec on ,0.2 sec on and 2 sec off and so on or it may be 0.75 sec on, and 0.75 sec off and so on. When this ringing tone is received, the calling subscriber knows that the connection is completed and that the bell of the called subscriber is ringing.

1.3.4 N.U.TONE

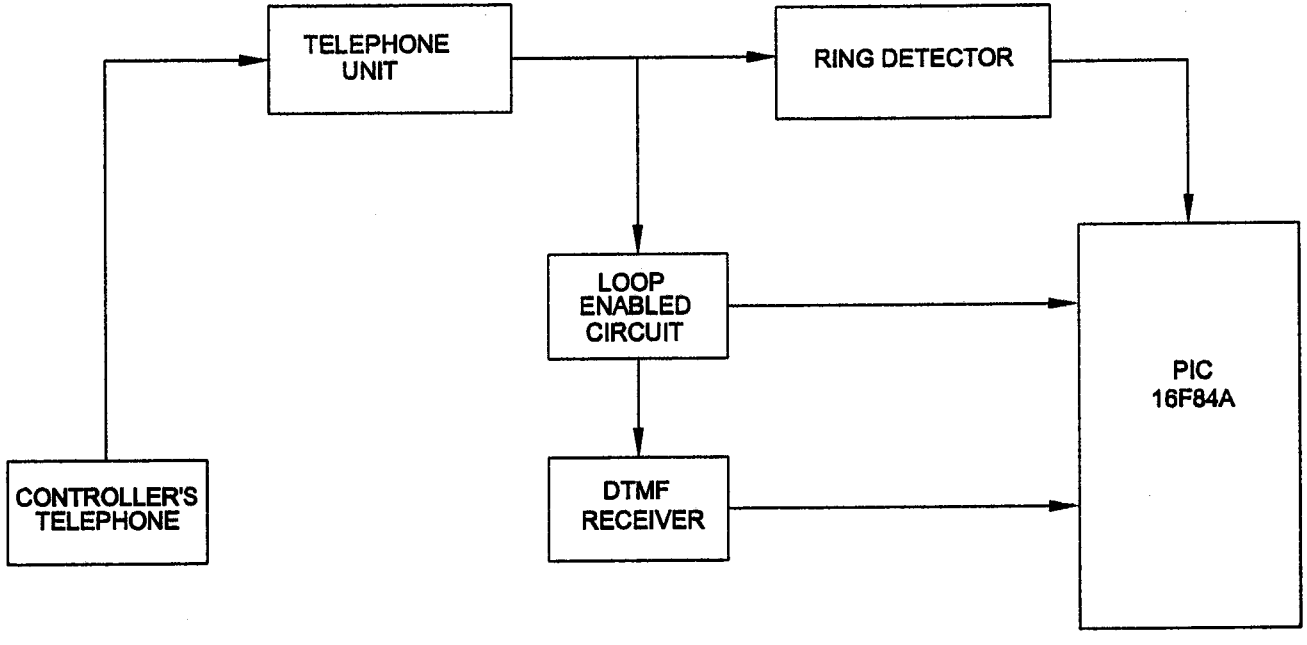
This is number unobtainable tone and this is sent when the number dialled is cannot be obtained if any subscriber dials a number, which is not actually connected to the exchange this indication is sent. This is also a tone of 400 Hz with interruption of 200 milli secs, every three seconds

BLOCK DIAGRAM

2. BLOCK DIAGRAM

2.1 GENERAL EXPLANATION

The block diagram figure 2.1 shows the general arrangement of the components involved in our project. When we dial the number from outside telephone or cell phone, the telephone unit will ring. The ringing pulses are detected by using ring detector and it is sent to the PIC micro controller. The micro controller checks the signal pulses and generate corresponding out put. Then it is given to the relay coil of the loop enable circuit. Now the outside telephone is connected to micro controller through DTMF receiver. So now we can switch "ON or OFF" the load by using the corresponding keys in the telephone, which is already programmed in the micro controller.



BLOCK DIAGRAM

SWITCHING CIRCUIT

3. SWITCHING CIRCUIT

3.1 RINGER CIRCUIT

When we dial the number from outside telephone / cell phone, the telephone will ring. The ringing pulses are detected by using ring detector and the signal is sent to PIC.

3.1.1 RING DETECTOR

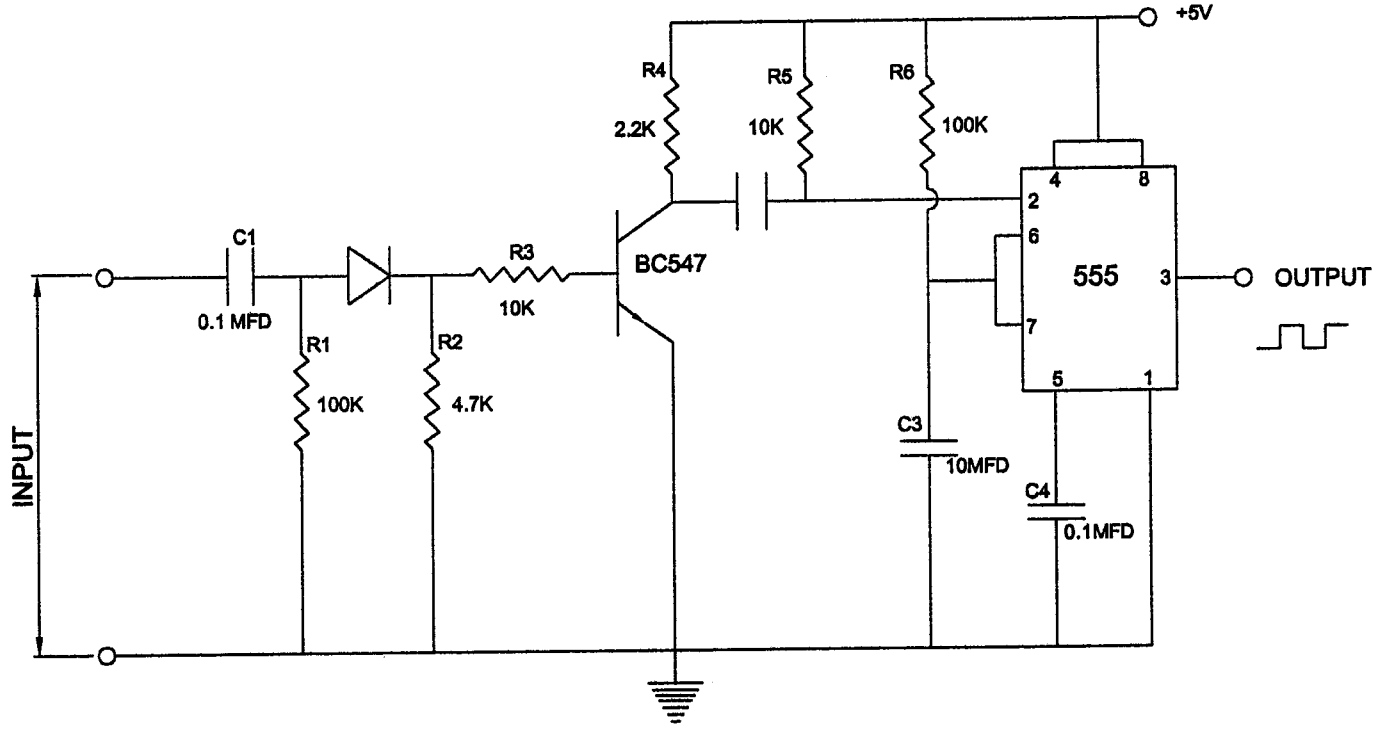
The circuit for the ring detector is as shown in the figure3.1. The capacitor C1 acts as the filter for the incoming AC signal. This AC signal is fed to the diode IN4007, which acts as the rectifier. Resistors R1 & R2 are used for current limiting purposes. The base resistors R3 prevents the high current from reaching the transistor BC547 that is it prevents the transistor from getting damaged the resistor R5 is used for signal boosting.

Initially the capacitor C2 is in the charged condition when the ring signal is given as the input the transistor becomes ON and the capacitor C2 discharges, which in turn helps in triggering the timer 555 depending upon R6 and C3 the timer is oscillated and the pulses generated at the output. Thus the ring detector detects the number of ring pulses. The number of ring pulses can be set according to our need using software and electromechanical relay is used for hook switch release.

This relay consists of a core and a coil is wound around the core. When the coil is energized the core becomes magnetised and the contact is made. When the electricity is removed, demagnatisation of core occurs and contact is removed

3.1.2 555 TIMER

555 timer is used in ring detector circuit. It is a highly stable device for getting accurate time delay or oscillation. A single 555 TIMER can provide time delay ranging from micro seconds to hours. The 555 TIMER can be used with supply voltage in the range of +5volts to +18volts and drive load upto 200mA.it is compatible with both TTL and CMOS logic circuits. Because of the wide range of supply voltage the 555TIMER are versatile and are easy to use in various applications include oscillator, pulse generator, ramp and square wave generator, mono shot multi vibrator, burglar alarm, traffic light control and voltage monitor etc.



RING DETECTOR

3.2 LOOP ENABLING CIRCUIT

3.2.1 RELAYS

Relays are electro magnetic devices by which the operating of one or more circuits are control led by the operations of some other circuits or circuit. These devices are provided with some mechanical contacts and with their help they control operation of other circuits in telephony, the relays that are used vary widely in their nature from very simple to very complicated types. They may have from one to as many as twenty sets of contacts also vary in nature. There are mainly 4 types of contact as given below

(a) MAKE CONTACTS :

In this, the contacts which are normally broken, are made when the relay is operated.

(b) BREAK CONTACTS:

These are normally made contacts that are broken by the operation of the relay.

(c) CHANGE OVER CONTACTS :

In this the movable contact which while changing over, its position by operation of the relay, breaks with one contact and makes with other.

(d) MAKE-BEFORE –BREAK CONTACT :

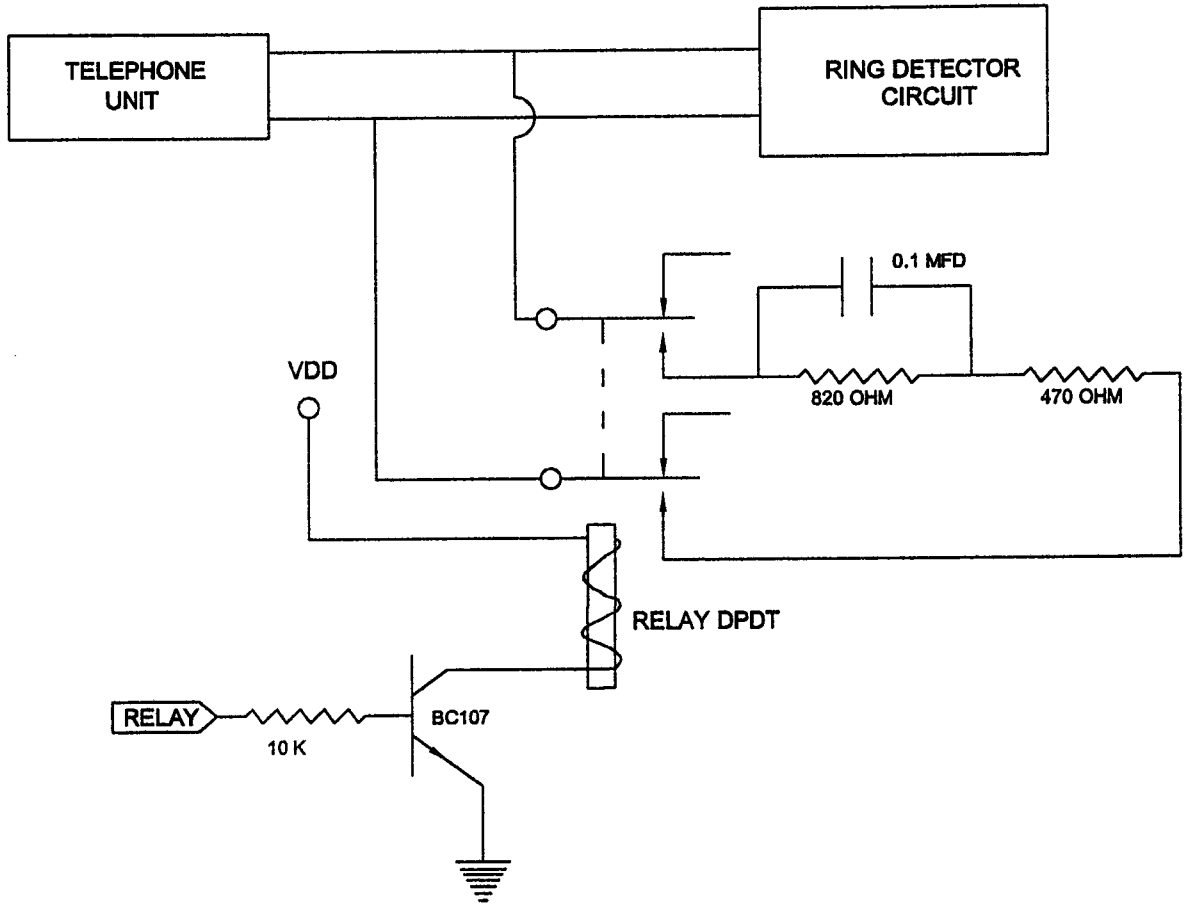
In this type when the relay is operated, one normally broken contact is first made when it is operated, the only a second normally made contact is broken.

There are various types of telephone relays according to specific requirements of different circuits. Most of them are of ordinary types whose main object is to make or break some circuits when some currents flows to flow through some other circuit or circuits on special importance is given to the time of operation ordinary relays, of course vary in their types so far in the operating current and the number and types of contacts provided are concerned.

3.2.2 THEORY OF OPERATION OF THE RELAY :

When a current is passed through the coil of the relay a magnetic flux is produced through the core whose path is completed throughout the yoke, the armature and the air gap between the armature and the core. So a force is exerted on the armature and it moves against the force exerted by different spring contacts and when it moves, the pin also moves up, there by moving all the spring contacts fixed to the pin so the various contacts are operated.

The circuit is as shown in the figure 3.2.After the ringing pulses are detected, the PIC sends a signal to the loop enabling circuit, where the relay coil get charged. The key is now attracted and the resistances are now added to the main line. Now the telephone line is in engaged position.



LOOP ENABLING CIRCUIT

3.3 DTMF (Dual Tone Multi-frequency)

This is a full DTMF receiver that integrates both band split filter and decoder functions into a single 18-pin DIP or SOIC package. Manufactured using state of the art CMOS process technology, the M-8870 offers low power consumption and precise data handling. Its filter section uses switched capacitor technology for both the low and high group filters and for dial tones rejection. Its decoder uses digital counting techniques to detect and decode all 16DTMF tone pairs into 4 bit code. External component count is minimized by provision of a on chip differential input amplifier, clock generator and latched tri-state interface bus. Minimal external components required include a low cost 3.579545 MHz color burst crystal, a timing resistor and a timing capacitor.

The new M-8870-02 provides a "power down" option which, when enabled, drops consumption too less than .5 mw. The 02 versions can also inhibit the decoding of the fourth column digits.

DTMF is the generic name for pushbutton telephone signaling equivalent to the bell system's touch-tone. Dual tone multi frequency (DTMF) signaling is quickly replacing dial-pulse signaling in telephone banking or electronic mail systems , in which the user can select options from a menu by sending signals from a telephone.

3.3.1 DTMF STANDARDS:

The DTMF tone-signaling standard is also known as touch tone or MFPB (Multi frequency push button). Bell labs for use by ATT&T in the dial pulse signaling standard developed touch tone. Each administration has defined its own DTMF specifications. They are very similar to the CCITT standard, varying by small amounts in the guard bands allowed in frequency, power twist and talk-off.

Two tones are used to generate a DTMF digit. One tone is chosen out of four row tones, and the other is chosen out of four column tones. Two of eight tones can be combined so as to generate sixteen different DTMF digits. Of these sixteen keys shown in the figure, twelve are the familiar keys of a touch-one keypad and four are reserved for future uses.

A 90-minute audio cassette to test the DTMF decoders is available from Mitel semiconductors. There also exists a standard describing requirements for systems ,which

test DTMF systems . This standard is available from the IEEE as ANSI/IEEE standard 752-1986.

3.3.2 DTMF DECODER :

The DTMF signals transmitted over the telephone lines can be received and decoded outputs can be suitably used along with certain additional circuitry to design a DTMF code detection unit.

The DTMF digits transmitted over the telephone lines would have a normal width of 50ms followed by a pause of similar duration between consecutive digits would be transmitted in one second . the on-cradle and off-cradle status of handset can be detected , based on the line voltage state, before the start of ringing. The voltage drops to 10 to 12 DC on lifting of the handset from the cradle.

An integrated DTMF decoder type M-8870 decodes the tone dialing codes received via the telephone line. The telephone line interface consists of two parts : one to detect the ring signals that enable the unit to answer the call at right moment, and another to receive and transmit tones via telephone line.

3.3.3 FEATURES:

- Low power consumption
- Adjustable acquisition and release times
- Central office quality and performance
- Power-down and inhibit modes
- Single 5-volt power supply
- Dial tone suppression

3.3.4 APPLICATIONS:

- Telephone switch equipment
- Mobile radio
- Remote control
- Remote data entry

3.3.5 FUNCTIONAL DESCRIPTION :

The M-8870 operating functions as shown in the figure 3.3.1 include a band split filter that separates the high and low tones of the received pair, and a digital decoder that verifies both the frequency and duration of the received tones before passing the resulting 4-bit code to the output bus.

3.3.6 FILTER

The low and high group tones are separated by applying the dual tone signal to the inputs of two 9^{th} order switched capacitor band pass filters with bandwidths that corresponds to the bands enclosing the low and high group tones. The filter also incorporates notches at 350 and 440Hz, providing excellent dial tone rejection. A single order switched capacitor section that smoothers the signals prior to limiting follows each filter output. High gain comparator provided with hysteresis to prevent detection of unwanted low-level signals and noise performs signal limiting. The comparator outputs provide full rail logic swings at the frequencies of the incoming tones.

3.3.7 DECODER

The M-8870 decoder uses a digital counting technique to determine the frequencies of the limited tones and to verify that they correspond to standard DTMF frequencies as shown in the table3.3.1. Complex averaging algorithm is used to protect against tone simulation by extraneous signals while tolerating small frequency variations the algorithm ensures an optimal combination of immunity to talk off and tolerance to interfacing signals and noise. When the detector recognizes the simultaneous presence of two valid tones, it raises the early steering flag (EST). Any subsequent loss of signal condition will cause EST to fall.

3.3.8 STEERING CIRCUIT

Before a decoded tone pair is registered, the receiver checks for valid signal duration. This check is performed by an external RC time constant driven by EST. Logic high on EST causes Vcc to raise as capacitor discharges. Provided that the signal condition is maintained for the validation period Vcc reaches the threshold (Vtst) of the steering logic to register the tone pair thus latching its corresponding 4 bit code into the output latch.

At this point, the GT output is activated and drives VCC to VDD. GT continues to drive high as long as EST remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flat (Std) goes high, signaling that received tone pair has been registered. The contents of the output latch are made available on the four-bit output bus by raising the three-state control input (OE) to logic high.

The steering circuit works in reverse to validate the inter digit pause between signals. Thus as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions too short to be considered a valid pause. This capability, together with the ability to select the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

3.3.9 GUARD TIME ADJUSTMENT:

Where independent selections of receive and pauses are not required the simple steering circuit is applicable. Component values are chosen according to the formula:

Trec = tdp + Tgtp

Tgtp = 0.67 rc

The value of tdp is a parameter of the device and Trec is the minimum signal to be recognized by the receiver. The value for C of 0.1μF is recommended for most applications, leaving r to be selected by the designer. For example suitable value of R for a Trec of 40ms would be 300k ohm. The timing requirements for most telecommunications are satisfied with this arrangement.

Different steering arrangements may be used to select independently the guard times for tone present (Tgtp) and tone absent (Tgta). This may be necessary to meet system specifications that place both accept and reject limits on both tone and inter-digit pause.

Guard time adjustments also allow the designer to tailor system parameters such as talk off and noise immunity. Increasing to tailor system parameter such as talk off and noise immunity. Increasing trec improves talk off performance, since it reduces the probability that tones simulated by speech will maintain signal condition long enough to

be registered. On the other hand a relatively short tree with a long to do would be appropriate for extremely noisy environment where fast acquisition time and immunity to dropouts would be required.

3.3.10 INPUT CONFIGURATION:

The input arrangement of the M-8870 provides a differential input operational amplifier as well as bias source to bias the inputs at mid rail. Provision is made for connection of a feedback resistor to the op-amp output (GS) for gain adjustments.

In a single ended configuration, the input pins are connected with the op-amp connected for unity gain and Vref biasing the input at ½ VDD. Adjustable gain configuration is possible with the help of the feedback resistor.

3.3.11 DTMF CLOCK CIRCUIT:

The internal clock circuit is completed with the addition of a standard 3.579545mHZ color burst crystal. The crystal can be connected to a single M-8870 or to a series of M-8870's a single crystal can be used to connect a series of M-8870 by coupling the oscillator output of each M-8870 through a 30pH capacitor to the oscillator input of the next M-8870.

3.3.12 PIN FUNCTIONS:

IN+: Non-inverting input connected to the front-end of the differential Amplifier.

IN-: Inverting input. Connected to the front-end of the differential Amplifier.

GS: Gain select. It gives access to output of front-end amplifier for connection of feedback resistor.

VREF: Reference voltage output. May be used to bias the inputs at mid rail.

INH*: Inhibits detection of tones representing keys A, B, C and D.

PD*: Power down. Logic high powers down the device and inhibits the oscillator.

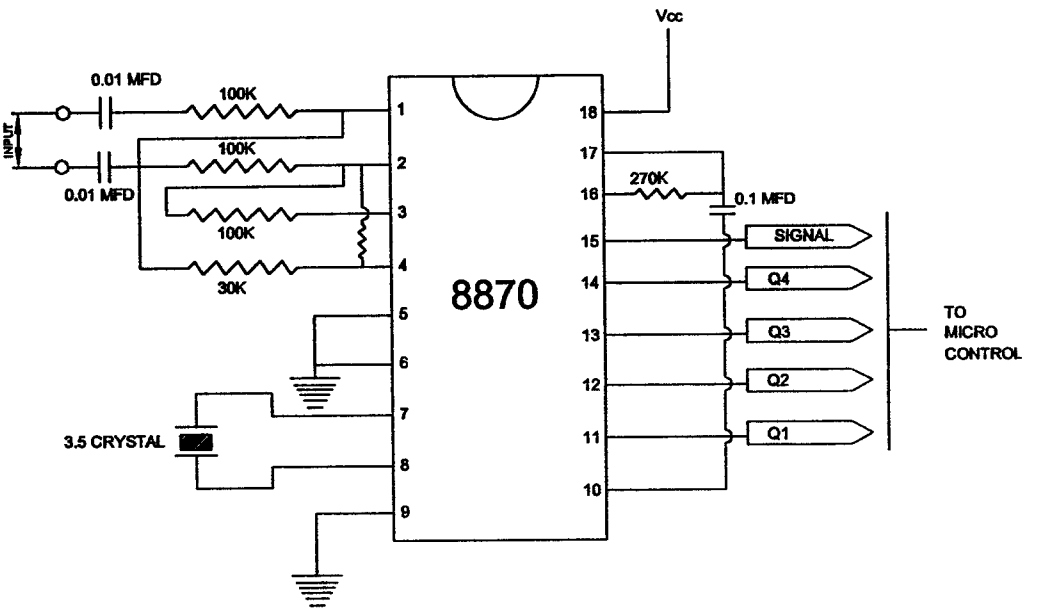
OSC1: Clock input. 3.579545 MHz crystal connected between these pins complete the internal oscillator.

OSC2: Clock input. 3.579545 MHz crystal connected between these

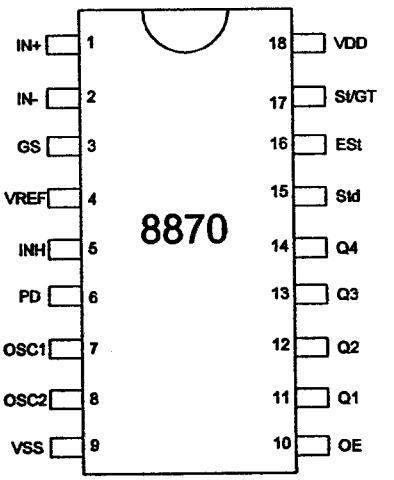
VSS:	Negative power supply (normally connected to 0v)
OE:	Three state output enable (input). Logic high enables the outputs Q1, Q4. Internal pull up.
Q1, Q2:	Three state outputs. When enabled by OE,
Q3, Q4:	Provides the code corresponding to the last valid tone pair received.
Std:	Delayed steering output. Presents logic high when a received tone pair has been registered and the output latch is updated. Returns to logic low when the voltage on St/Gt falls below Vtsi.
Est:	Early steering output presents logic high immediately when the digital algorithm detects a recognizable tone pair. Any momentary loss of signal condition will cause Est to return to logic low.
St/GT:	Steering input/guard time output voltage greater than VTSt detected at St cause the device to register the detected tone pair and update the output latch. A voltage less than VTSt free the device to accept a new tone pair. The GT output acts to reet the external steering time constant, and its state is a function of Est and the voltage on St.
VDD:	Positive power supply.

3.3.13 WORKING OF THE DTMF:

As soon as the loop is enabled, a current flowing through the DTMF receiver enables to generate the signal, which is given to the PIC and then the M-8870 decodes the tone dialing codes received into 4 bit code. The input signal is given to the 1^{st} and 2^{nd} pin and signal to given to PIC is from 15^{th} pin and the binary coded outputs are taken from 14^{th}, 13^{th}, 12^{th} and 11^{th} pin.



DTMF DECODER



PIN DETAILS OF IC 8870

3.3.1 Table TONE DECODING

Flow	F High	Key (Ref.)	OE	Q4	Q3	Q2	Q1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1336	0	H	1	0	1	0
941	1209	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	1	0
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
1.ANY	ANY	ANY	L	Z	Z	Z	Z

High = High

L = Low

Z = High Impedance

PERIPHERAL INTERFACE CONTROLLER

4. PERIPHERAL INTERFACE CONTROLLER

4.1 WHY PIC?

- PIC is a very popular micro controller worldwide.
- Micro chip is the first manufacturer of 8 pin RISC MCU.
- Variety of end-user Application-specific standard products (ASSP) & Application - specific
- Global network of manufacturing and customer support facilities.

PIC micro devices have following architectural features to attain the high performance.

Harvard architecture

Long word instructions

Single word instructions

Single cycle instructions

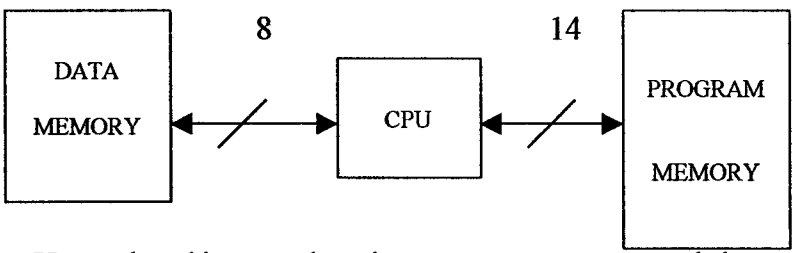
Instruction pipelining

Reduced instruction set

Register file architecture

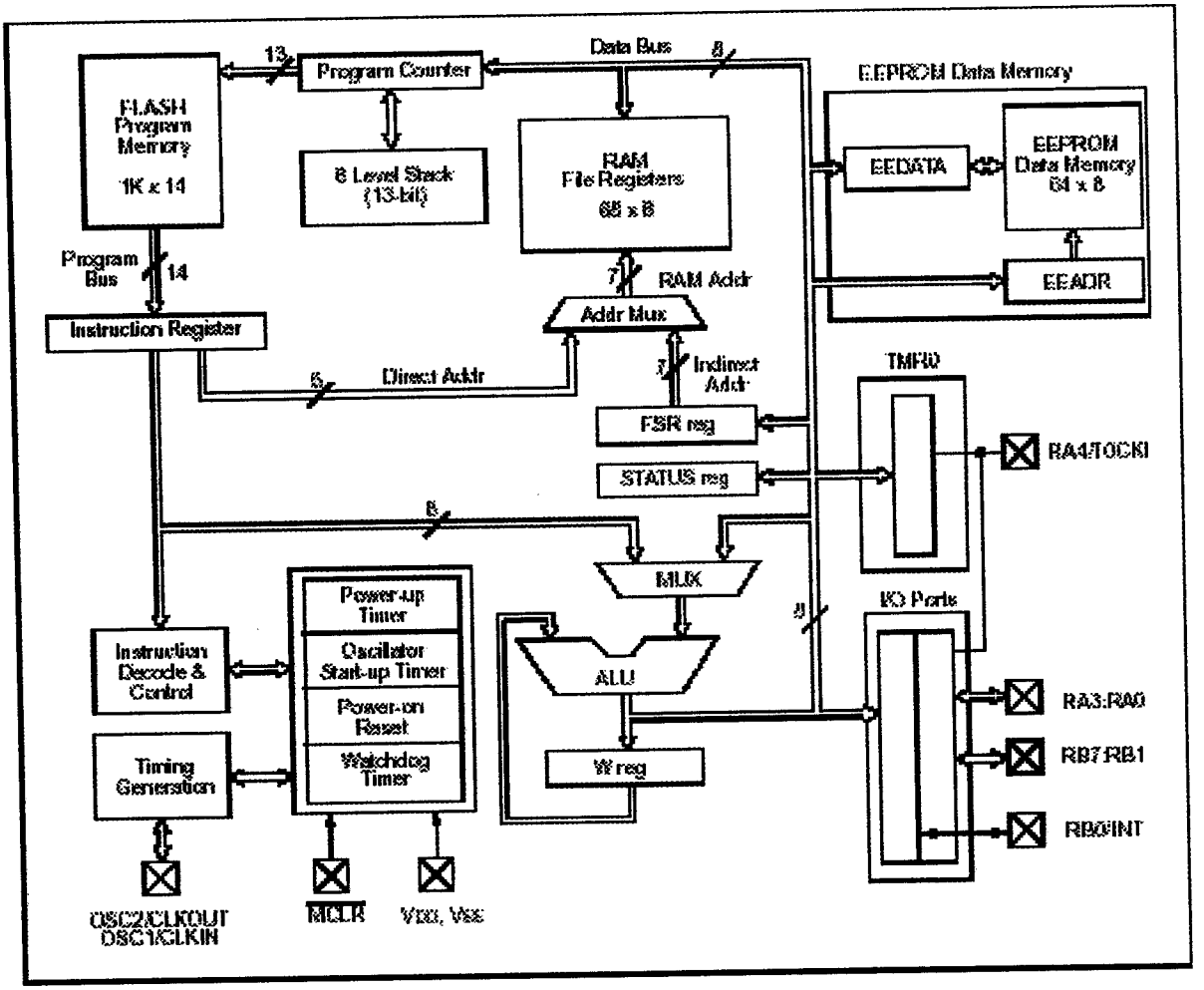
Orthogonal(symmetric) instructions.

4.1.1 HARVARD ARCHITECTURE:



Harvard architecture has the program memory and data memory as separate memories and they are accessed from separate buses. This improves bandwidth over traditional Von-Neumann architecture in which program and data are fetched from the same memory using the same bus. With the Harvard architecture , the instruction is fetched in a single instruction cycle(all 14-bits).

4.2 ARCHITECTURE OF PIC 16F84A



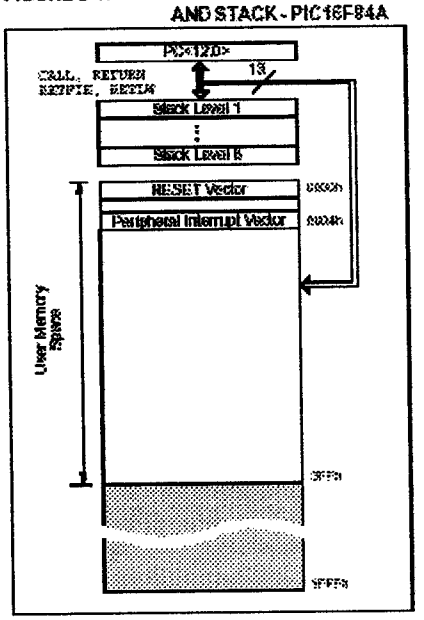
4.3 MEMORY ORGANIZATION

There are two memory blocks in PIC16F84A. These are program memory and the data memory. The data memory consists of special function registers and general purpose RAM. The data memory also consists of Data EEPROM memory which has 64 bytes of address have 0H-3FH.

4.3.1 PROGRAM MEMORY ORGANIZATION

The PIC16FXCX has a 13- bit program counter capable of addressing an 8K x 14 program memory space. The PIC 16F84A, the first 1K x 14 (000h – 3FFh) are physically implemented reset vector is at 0000h and the interrupt.

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK - PIC16F84A



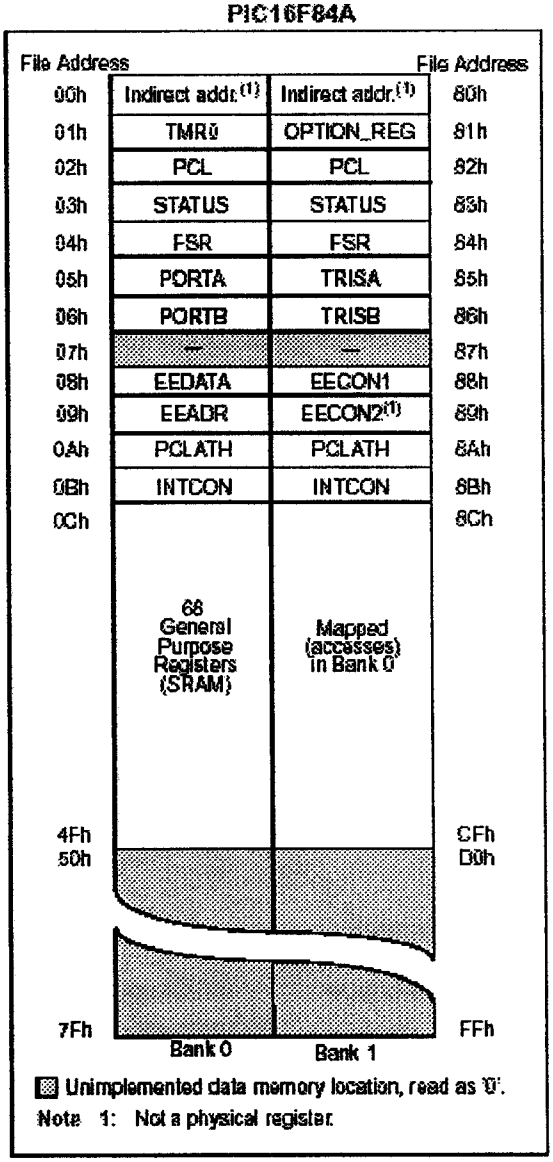
4.3.2 DATA MEMORY ORGANIZATION

The data memory is partitioned into two areas. The first is the Special Function Register (SFR) area, while the second the General Purpose Registers (GPR) area. The SFR control the operation of the device. The GPR area is blanked to allow greater than 116 bytes of general purpose RAM.

The banked areas of the SFT are for the registers that control the peripheral functions. Banking requires the use of control bits for bank selection. These control bits are located in the STATUS Register. Instructions MOVWF and MOVF can move values

data memory can be accessed either directly using the absolute address of each register file or indirectly through the File Select Register (SFSR) (Section (2.4). Indirect addressing uses the present value of the RP0 bit for access into the blanked which contain the general purpose registers and the special function registers. Bank 0 is selected by clearing the RP0 bit (STATUS <5>). Setting the RP0 bit selects Bank 1. Each Bank extends upto 7Fh (128 bytes). The first twelve locations of each Bank are reserved for the Special Function Registers. The remainder are General Purpose Registers implemented as static RAM.

FIGURE 2-2: REGISTER FILE MAP - PIC16F84A



4.3.3 REGISTERS

(a) SPECIAL FUNCTION REGISTERS

The Special Function Registers are used by the CPU and Peripheral functions to control the device operation. These registers are static RAM. The special function registers can be classified into two sets, core and peripheral.

REGISTER 2-1: STATUS REGISTER (ADDRESS 03h, 83h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit 7							bit 0

bit 7-6 Unimplemented: Maintain as '0'

bit 5 RP0: Register Bank Select bits (used for direct addressing)
1 = Bank 1 (80h - FFh)
0 = Bank 0 (00h - 7Fh)

bit 4 $\overline{TO}$: Time-out bit
1 = After power-up, CLRWDT instruction, or SLEEP instruction
0 = A WDT time-out occurred

bit 3 $\overline{PD}$: Power-down bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

bit 2 Z: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 DC: Digit carry/$\overline{borrow}$ bit (ADDWF, ADDLW, SUBLW, SUBWF instructions) (for $\overline{borrow}$, the polarity is reversed)
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result

bit 0 C: Carry/$\overline{borrow}$ bit (ADDWF, ADDLW, SUBLW, SUBWF instructions) (for $\overline{borrow}$, the polarity is reversed)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note: A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low order bit of the source register.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

The STATUS register contains the arithmetic status of the ALU, the RESET status and the bank select bit for data memory. As with any register, the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to device logic. Furthermore, the TO and PD bits are not writable. Therefore the result of an instruction with the STATUS register as destination may be different than intended. For example, CLRF

STATUS will clear the upper – three bits and set the Z bit. This leave the STATUS register as 000u u1uu (where u = unchanged). Only the BCF, BSF, SWAPF and MOVWF instructions should be used to alter the STATUS register because these instructions do not affect any status bit.

(b) PCL AND PCLATH

The program counter (PC) specifies the address of the instruction to fetch for execution. The PC is 13 bits wide. The low byte is called the PCL register. This register is readable and writable. The high byte is called the PCH register. This register contains the PC<12:8> bits and is not directly readable or writable. All updates to the PCH register go through the PCLATH register.

(c) STACK

The stack allows a combination of up to 8 program calls and interrupts to occur. The stack contains the return address from this branch in program execution. Midrange devices have an 8 level deep x 13-bit wide hardware stack. The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, TETLW or a RETFIE instruction execution. PCLATCH is not modified when the stack is PUSHed or POPed. After the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

4.4 INPUT AND OUTPUT PORTS

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

4.4.1 PORT A AND TRISA REGISTERS

PORT A is a 5-bit wide bi-directional port. The corresponding data direction register is TRISA. Setting a TRISA bit (=1) will make the corresponding PORT A pin an output, i.e., put the contents of the output driver in a hi-impedance mode. Clearing a TRISA bit (=0) will make the corresponding PORT A pin an output, i.e., put the contents of the output latch on the selected pin. Reading the PORT A register reads the status of the pins whereas writing to it will write to the port latch. All write operations are ready-modify-write operations. Therefore a write to a port implies that the port pins are read, this value is modified, and then written to the port data latch. Pin RA4 is multiplexed with the Timer0 module clock input to become the RA4/T0CK1 pin. The RA4/T0CKI pin kis a Schmitt Trigger input and an open drain output. All other RA port pins have TTL input levels and full CMSO output drivers.

TABLE 4-1: PORTA FUNCTIONS

Name	Bit0	Buffer Type	Function
RA0	bit0	TTL	Input/output
RA1	bit1	TTL	Input/output
RA2	bit2	TTL	Input/output
RA3	bit3	TTL	Input/output
RA4/T0CKI	bit4	ST	Input/output or external clock input for TMR0. Output is open drain type.

Legend: TTL = TTL input, ST = Schmitt Trigger input

FIGURE 4-1: BLOCK DIAGRAM OF PINS RA3:RA0

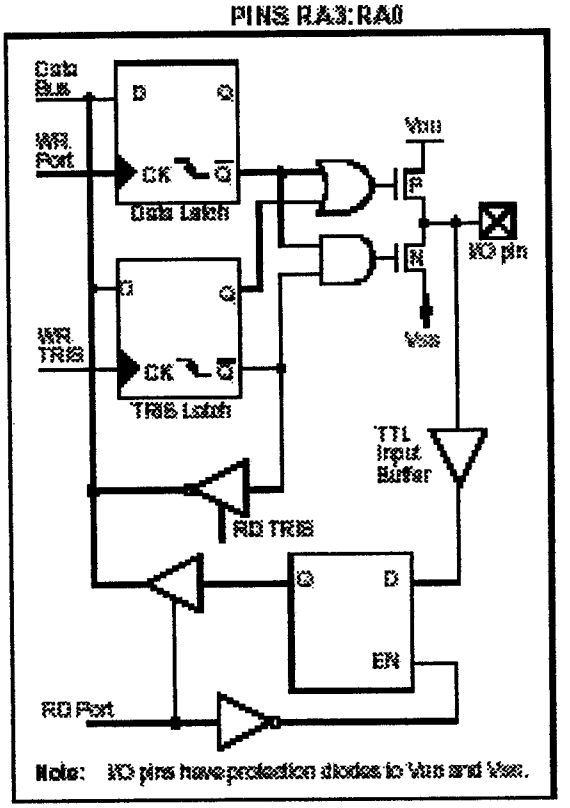
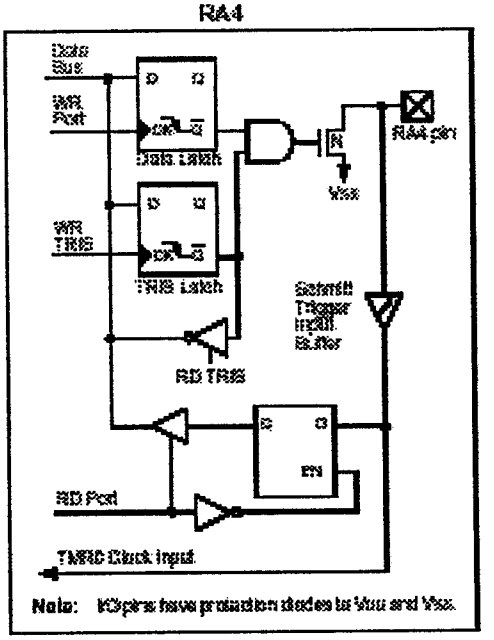


FIGURE 4-2: BLOCK DIAGRAM OF PIN RA4



4.4.2 INITIALIZING PORT A

```
BCF STATUS, RP0   ; Bank0
CLRF PORT         ; Initialize PORT A by clearing output
                  ; Data latches
BSF STATUS, RP0   ; Select Bank 1
MOVLW 0 x 0 F     ; Value used to initialize data direction
MOVWF TRISA       ; Set RA<3:0> as inputs RA4 as output
                  ; TRISA <7:5> are always read as '0'.
```

4.4.3 PORT B AND TRISB REGISTERS

PORT B is an 8-bit wide bi-directional port. The corresponding data direction register is TRISB. Setting a TRISB bit (=1) will make the corresponding PORTB pin an input, i.e., put the corresponding output driver in a hi-impedance mode. Clearing a TRISB bit (=0) will make the corresponding PORTB pin an output, i.e., put the contents of the output latch on the selected pin.

4.4.4 INITIALIZING PORT B

```
BCF STATUS, RP0   ; Bank0
CLRF PORTB        ; Initialize PORT B by clearing output
                  ; data latches
BSF STATUS,  RP0  ; Select Bank 1
MOVLW  0Xcf       ; Value used to initialize data direction
MOVWF  TRISB      ; Set RB <3:0> as inputs, RB<5:4> as outputs
                  ; PORTB <7:6> as inputs
```

Each of the PORT B pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit RBPU (OPTION <7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

Four of PORTB's pins, RB7:RB4, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB) pin configured as an output is excluded from the interrupt on change comparison). The input pins (of RB7 :RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are 'OR'ed together to generate the RB Port Change

SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner: a) Any read or write of PORTB. This will end the mismatch condition. B) Clear flag bit RBIF.A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition, and allow flag bit RBIF to be cleared. The interrupt on change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt on change feature. Polling of PORTB is not recommended while using the interrupt on change feature.

TABLE 4-3: PORTB FUNCTIONS

Name	Bit	Buffer Type	I/O Consistency Function
RB0/INT	bit0	TTL/ST(1)	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3	bit3	TTL	Input/output pin. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB6	bit6	TTL/ST(2)	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up. Serial programming clock.
RB7	bit7	TTL/ST(2)	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger.
Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

FIGURE 4-3: BLOCK DIAGRAM OF PINS RB7:RB4

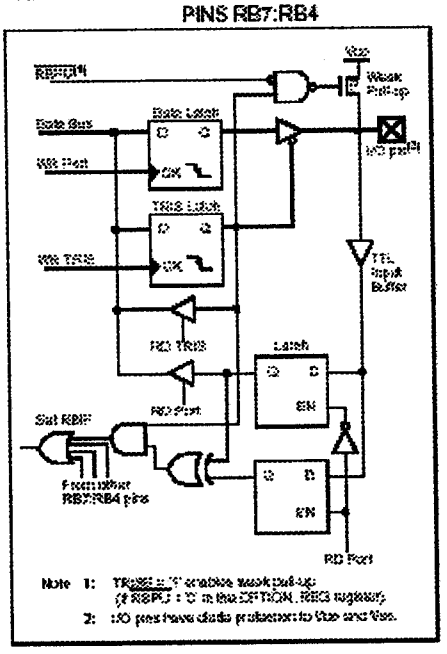
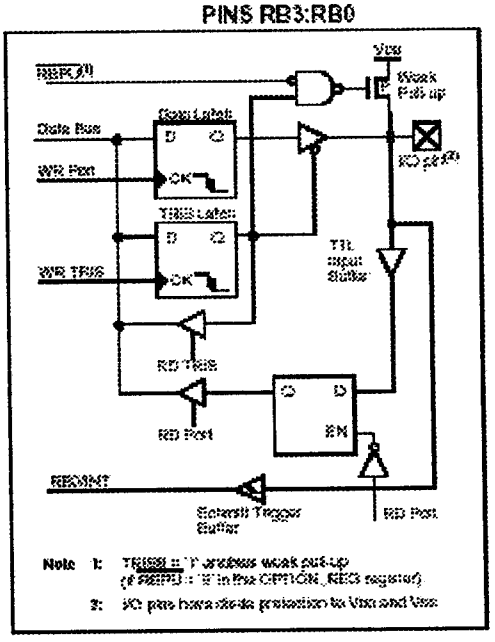


FIGURE 4-4: BLOCK DIAGRAM OF PINS RB3:RB0



4.5 TIMER 0

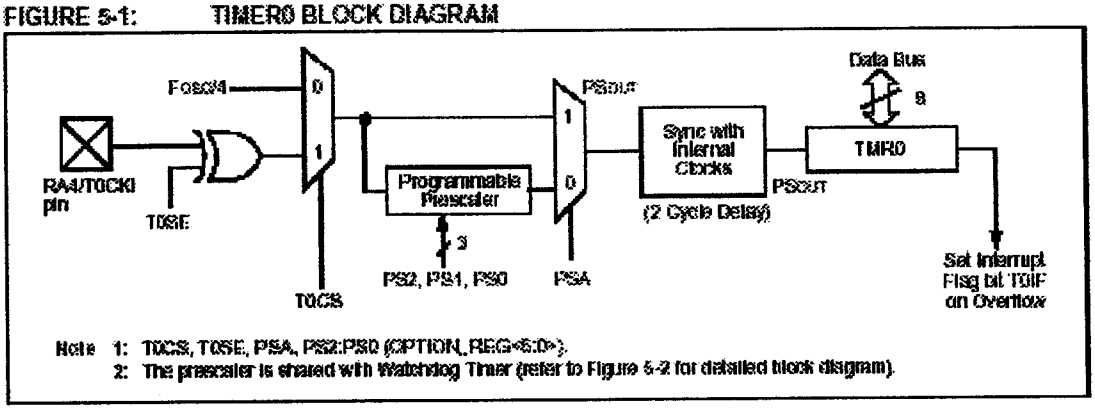
The Timer 0 module timer / counter has the following features:

- 8 – bit timer/ counter
- Readable and writable
- Internal or external clock select
- Edge select for external clock
- 8-bit software programmable prescaler
- Interrupt on overflow from FFh to 00h.

4.5.1 TIMER R0 OPERATION

Timer 0 can operate as a timer or as a counter.Timer mode is selected by clearing bit T0CS (OPTION REG<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register. Counter mode is selected by setting bit T0CS (OPTIONREG<5>). In counter mode, Timer0 will increment either on every rising or falling edge of pin RA4/T0CK1. The incrementing edge is determined by the Timer 0 Source Edge Select bit T0SE (OPTION_REG<4>). Clearing bit T0SE selects the rising edge. Restrictions on the external clock input are discussed below. When an external clock input is used for Timer0, it must meet certain requirements. The requirements ensure the external clock can be synchronized with the internal phase clock (TOSC). Also, there is a delay in the actual incrementing of Timer 0 after synchronization.

FIGURE 5-1: TIMER0 BLOCK DIAGRAM



Note 1: T0CS, T0SE, PSA, PS2:PS0 (OPTION_REG<5:0>).
2: The prescaler is shared with Watchdog Timer (refer to Figure 5-2 for detailed block diagram).

4.6 INSTRUCTION SET SUMMARY

4.6.1 TYPES OF INSTRCTION

Each PIC16CXXX instruction is a 14-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction.

For byte-oriented instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction. The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For bit- oriented instructions, 'b' represents a bit field designator which selects the number of bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For literal and control operations, 'k; represents an eight or eleven bit constant or literal value.

TABLE 7-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1
PC	Program Counter
TO	Time-out bit
PD	Power-down bit

FIGURE 7-1: GENERAL FORMAT FOR INSTRUCTIONS

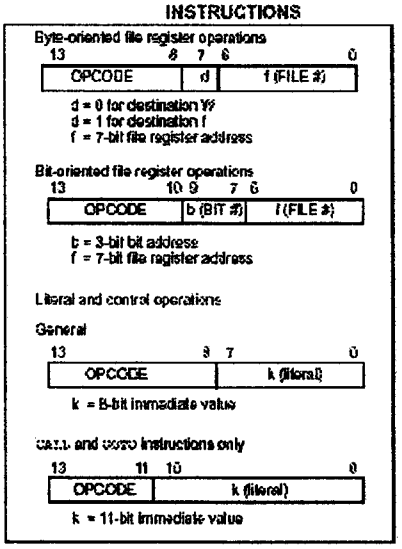


TABLE 7-2: PIC16CXXX INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode MSB	LSB	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS							
ADDWF	f, d	Add W and f	1	00 0111 dfff ffff		C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00 0101 dfff ffff		Z	1,2
CLRF	f	Clear f	1	00 0001 1fff ffff		Z	2
CLRW	-	Clear W	1	00 0001 0xxx xxxx		Z	
COMF	f, d	Complement f	1	00 1001 dfff ffff		Z	1,2
DECF	f, d	Decrement f	1	00 0011 dfff ffff		Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1 (2)	00 1011 dfff ffff			1,2,3
INCF	f, d	Increment f	1	00 1010 dfff ffff		Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1 (2)	00 1111 dfff ffff			1,2,3
IORWF	f, d	Inclusive OR W with f	1	00 0100 dfff ffff		Z	1,2
MOVF	f, d	Move f	1	00 1000 dfff ffff		Z	1,2
MOVWF	f	Move W to f	1	00 0000 1fff ffff			
NOP	-	No Operation	1	00 0000 0xx0 0000			
RLF	f, d	Rotate Left f through Carry	1	00 1101 dfff ffff		C	1,2
RRF	f, d	Rotate Right f through Carry	1	00 1100 dfff ffff		C	1,2
SUBWF	f, d	Subtract W from f	1	00 0010 dfff ffff		C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00 1110 dfff ffff			1,2
XORWF	f, d	Exclusive OR W with f	1	00 0110 dfff ffff		Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS							
BCF	f, b	Bit Clear f	1	01 00bb bfff ffff			1,2
BSF	f, b	Bit Set f	1	01 01bb bfff ffff			1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01 10bb bfff ffff			3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01 11bb bfff ffff			3
LITERAL AND CONTROL OPERATIONS							
ADDLW	k	Add literal and W	1	11 111x kkkk kkkk		C,DC,Z	
ANDLW	k	AND literal with W	1	11 1001 kkkk kkkk		Z	
CALL	k	Call subroutine	2	10 0kkk kkkk kkkk			
CLRWDT	-	Clear Watchdog Timer	1	00 0000 0110 0100		TO,PD	
GOTO	k	Go to address	2	10 1kkk kkkk kkkk			
IORLW	k	Inclusive OR literal with W	1	11 1000 kkkk kkkk		Z	
MOVLW	k	Move literal to W	1	11 00xx kkkk kkkk			
RETFIE	-	Return from interrupt	2	00 0000 0000 1001			
RETLW	k	Return with literal in W	2	11 01xx kkkk kkkk			
RETURN	-	Return from Subroutine	2	00 0000 0000 1000			
SLEEP	-	Go into standby mode	1	00 0000 0110 0011		TO,PD	
SUBLW	k	Subtract W from literal	1	11 110x kkkk kkkk		C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11 1010 kkkk kkkk		Z	

4.6.2 I/O PROGRAMMING CONSIDERATIONS

BI-DIRECTIONAL I/O PORTS

Any instruction which writes, operates internally as a read followed by a write operation. The BCF and BSF instructions, for example, read the register into the CPU, execute the bit operation and write the result back to the register. Caution must be used when these instruction are applied to a port with both inputs and outputs defined. For example, a BSF operation on bit 5 of PORT B will cause all eight bits of PORT B to be read into the CPU. Then the BSF operation takes place on bit 5 and PORTB is written to the output latches. If another bit of PORT B is used as a bi-directional I/O pin (i.e,. bit0) and it is defined as an input at this time, the input signal present on the pin itself particular pin, overwriting the previous content. As log as the pin stays in the input mode, no problem occurs. However, if bit 0 is switched into output mode later on, the content of the data latch is unknown. Reading the port register, reads the values of the port pins. Writing to the port register writes the value to the port latch. When using read-modify-write instructions (i.e, BCF, BSF, etc.,) on a port, the value of the port pins is read , the desired

operation is done to this value, and this value is then written to the port latch. A pin actively outputting a Low or High should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output current may damage the chip.

4.6.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-5). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such that the pin voltage stabilizes (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous stats of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port. Example 5-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

4.6.3 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits to deal with the needs of real time applications. The PIC16F8X has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operation mode and offer code protection.

These features are:

- OSC selection
- Reset – Power-on Reset (POR)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP
- Code Protection
- ID locations
- In-circuit serial programming

The PIC16F8X has a Watchdog Timer which can be shut off only through

timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only. This design keeps the device in reset while the power supply stabilizes. With these two timers on-chip, most applications need no external reset circuitry. SLEEP through external reset, Watchdog Timer time-out or through an interrupt. Several oscillator options are provided to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select the various options.

4.6.4 CONFIGURATION BITS

The configuration bits can be programmed (read as '0') or let un programmed (read as '1') to select various device configuration. These bits are mapped in program memory location 2007h. Address 2007h is beyond the user program memory space and it belongs to the special test / configuration memory space (2000h – 3FFFh). This space can only be accessed during programming. To find out how to program the PIC 16C84, refer to PIC16C84 EEPROM Memory Programming Specification (DS30189).

REGISTER 6-1: PIC16F84A CONFIGURATION WORD

R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u
CP	CP	CP	CP	CP	CP	CP	CP	CP	CP	PWRTE	WDTE	FOSC1	FOSC0
bit13													bit0

bit 13-4 CP: Code Protection bit
1 = Code protection disabled
0 = All program memory is code protected

bit 3 $\overline{\text{PWRTE}}$: Power-up Timer Enable bit
1 = Power-up Timer is disabled
0 = Power-up Timer is enabled

bit 2 WDTE: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0 FOSC1:FOSC0: Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

4.7 OSCILLATOR

The internal oscillator circuit is used to generate the device clock. The device clock is required for the device to execute instructions and for the peripherals to function. The device configuration bits select the oscillator mode. The device configuration bits are nonvolatile memory locations and the operating mode is determined by the value written during device programming. Configuration bits are used to select the various options.

4.7.1 OSCILLATOR TYPES

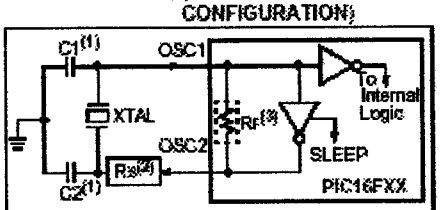
The PIC16F84A can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal / Resonator
- HS High Speed Crystal / Resonator
- RC Resistor / Capacitor

(i) CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes a crystal or ceramic resonator is connected to the OSC1 / CLKIN and OSC2 / CLKOUT pins to establish oscillation.

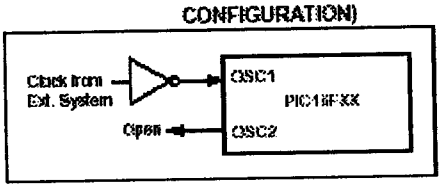
FIGURE 6-1: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)



Note 1: See Table 6-1 for recommended values of C1 and C2.
2: A series resistor (RS) may be required for AT strip cut crystals.

The PIC16F84A oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HR modes, the device can have an external clock source to drive the OSC1/CLKIN pin.

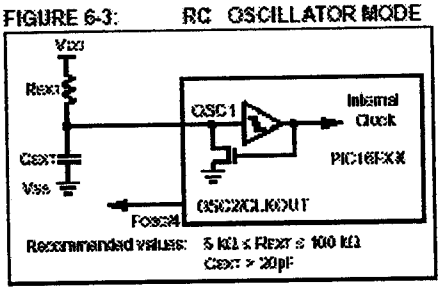
FIGURE 6-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)



(ii) RC OSCILLATOR

For timing insensitive applications the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) values, capacitor (Cext) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types also affects the oscillation frequency, especially for low Cext values. The user needs to take into account variation due to tolerance of the external R and C components.

FIGURE 6-3: RC OSCILLATOR MODE



4.8 RESET

4.8.1 INTRODUCTION

The reset logic is used to place the device into a known state. The source of the reset can be determined by using the device status bits. The reset logic is designed with features that reduce system cost and increase system reliability. Devices differentiate between various kinds of rest.

The PIC 16F84A differentiates between various kinds of reset:

- Power-on Reset (POR)
- MCLR reset during normal operation
- MCLR reset during SLEEP
- WDT Reset (during normal operation)
- WDT Wake-up (during SLEEP)

RESET CONDITION FOR PC AND SR

Condition	Program Counter	STATUS Register
Power-on Reset	000h	0001 1xxx
MCLR during normal operation	000h	000u uuuu
MCLR during SLEEP	000h	0001 0uuu
WDT Reset (during normal operation)	000h	0000 1uuu
WDT Wake-up	PC + 1	uuu0 0uuu
Interrupt wake-up from SLEEP	PC + 1(1)	uuu1 0uuu

TABLE 6-4: RESET CONDITIONS FOR ALL REGISTERS

Register	Address	Power-on Reset	MCLR during: – normal operation – SLEEP WDT Reset during normal operation	Wake-up from SLEEP: – through interrupt – through WDT Time-out
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h	---- ----	---- ----	---- ----
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h	0000 0000	0000 0000	PC + 1[2]
STATUS	03h	0001 1xxx	000q quuu[3]	uuuq quuu[3]
FSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA[4]	05h	---x xxxx	---u uuuu	---u uuuu
PORTB[5]	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
EEDATA	08h	xxxx xxxx	uuuu uuuu	uuuu uuuu
EEADR	09h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCLATH	0Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh	0000 000x	0000 000u	uuuu uuuu[1]
INDF	80h	---- ----	---- ----	---- ----
OPTION_REG	81h	1111 1111	1111 1111	uuuu uuuu
PCL	82h	0000 0000	0000 0000	PC + 1[2]
STATUS	83h	0001 1xxx	000q quuu[3]	uuuq quuu[3]
FSR	84h	xxxx xxxx	uuuu uuuu	uuuu uuuu
TRISA	85h	---1 1111	---1 1111	---u uuuu
TRISB	86h	1111 1111	1111 1111	uuuu uuuu
EECON1	88h	---0 x000	---0 q000	---0 uuuu
EECON2	89h	---- ----	---- ----	---- ----
PCLATH	8Ah	---0 0000	---0 0000	---u uuuu
INTCON	8Bh	0000 000x	0000 000u	uuuu uuuu[1]

4.8.2 POWER ON RESET (POR)

A POWER – on Reset pulse is generated on-chip when VDD rise is detected in the range of 1.2 V – 1.7 V). To take advantage of the POR, just tie the MCLR pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A minimum rise time for VDD must be met for this to operate properly. See Electrical Specifications for details. When the device starts normal operation (exists the reset condition), device operating parameters (voltage, frequency, temperature,..) must be meet to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met. For additional information, refer to Application Note AN 607, "Power-up Trouble Shooting". The POR circuit does not produce an internal reset when VDD declines.

4.8.3 POWER-UP TIMER (PWRT)

The Power-up Timer (PWRT)A provides a fixed 72 ms nominal timeout (TPWRT) from POR. The power-up Timer operates on an internal RC oscillator. The

rise to an acceptable level. A configuration bit, PWRTE, can enable / disable the PWRT. The power-up time delay TPWRT will vary from chip to chip due to VDD, temperature, and process variation.

4.8.4 OSCILLATOR START-UP TIMER (OST)

The oscillator Start-up Timer (OST) provides a 1024 oscillator cycle delay (from OSC1 input) after the PWRT delay ends. This ensures the crystal oscillator or resonator has started and stabilized. The OST time-out (TOST) is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP. When VDD rises very slowly, it is possible that the TPWRT time-out and TOST time-out will expire before VDD has reached its final value. In this case, an external power-on rest\et circuit may be necessary.

POWER SUPPLY UNIT

5. POWER SUPPLY UNIT

5.1 INTRODUCTION

Since all electronic circuits work only with low D.C. voltage we need a power supply unit to provide the appropriate voltage supply. This unit consists of transformer, rectifier, filter and regulator. A.C. voltage typically 230V rms is connected to a transformer which steps that AC voltage down to the level to the desired AC voltage. A diode rectifier then provides a full-wave rectified voltage that is initially filtered by a simple capacitor filter to produce a DC voltage. This resulting DC voltage usually has some ripple o AC voltage variations. A regulator circuit can use this DC input to provide DC voltage that not only has much less ripple voltage but also remains the same DC value even the DC voltage varies some what, or the load connected to the output DC voltages changes.

5.2 BLOCK DIAGRAM

5.2.1 TRANSFORMER

A transformer is a static (or stationary) piece of which electric power in one circuit is transformed into electric power of the same frequency in another circuit. It can raise or lower the voltage in a circuit but with a corresponding decrease or increase in current. It works with the principle of mutual induction. In our project we are using step down transformer for providing a necessary supply for the electronic circuits. In our project we are using a 15-0-15 center tapped transformer.

5.2. 2 RECTIFIER

The DC level obtained from a sinusoidal input can be improved 100% using a process called full-wave rectification. It uses 4 diodes in a bridge configuration. From the basic bridge configuration we see that two diodes (say D2 and D3) are conducting while the other two diodes (D1 & D4) are in "off" state during the period t = 0 or T/2.

Accordingly for the negative of the input the conducting diodes are D1 and D4. Thus the polarity across the load is the same.

5.2.3 FILTER

The filter circuit used here is the capacitor filter circuit where a capacitor is connected at the rectifier output, and a DC is obtained across it. The filtered waveform is essentially a DC voltage with negligible ripples, which is ultimately fed to the load.

5.3 POWER SUPPLIES

5.3.1 THREE – TERMINAL VOLTAGE REGULATORS

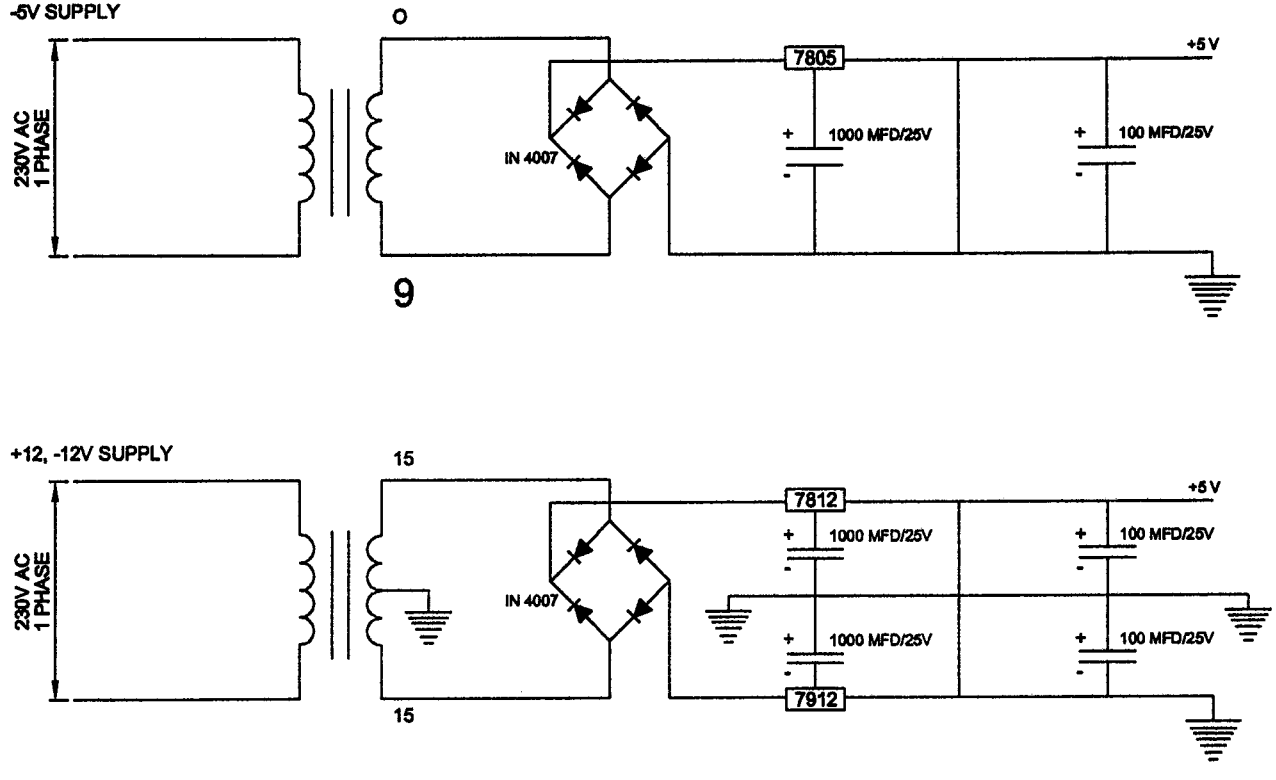
Fig. Shows the basic connection of a three-terminal voltage regulator IC to a load. The fixed voltage regulator has an unregulated DC input voltage, Vi, applied to one input terminal, a regulated output DC voltage, Vo, from a second terminal, with the third terminal connected to ground. For a selected regulator, IC device specifications list a voltage range over which the input voltage can carry to maintain a regulated output voltage over a range of load current. The specifications also list the amount of output voltage change resulting from a change in load current (load regulation) or in input voltage (line regulation)

5.3.2 Fixed Positive Voltage Regulators:

The series 78 regulators provide fixed regulated voltages from 5 to 24 V. Figure shows how one such IC, a 7812 is connected to provide voltage regulation with output from this unit of +12V dc. An unregulated input voltage Vi is filtered by capacitor C1 and connected to the IC's IN terminal. The IC's OUT terminal provides a regulated +12V which is filtered by capacitor C2 (mostly for any high-frequency noise). The third IC terminal is connected to ground (GND). While the input voltage may vary over some permissible voltage range, and the output load may vary over some acceptable range, the output voltage remains constant within specified voltage variation limits. These limitations are spelled out in the manufacturer's specification sheets. A table of positive voltage regulated ICs is provided in table.

Table 5.3.1 Positive Voltage Regulators in 7800 Series

IC Part	Output Voltage (V)	Minimum Vi (V)
7805	+5	7.3
7806	+6	8.3
7808	+8	10.5
7810	+10	12.5
7812	+12	14.6
7815	+15	17.7
7818	+18	21.0
7824	+24	27.1



REGULATED POWER NSUPPLY UNIT

FABRICATION AND TESTING OF THE CIRCUIT

6. FABRICATION AND TESTING OF THE CIRCUIT

6.1 CIRCUIT OPERATION

The operation of the Micro controller based switching operation can be categorized as

1.Ring detection.

2.Loop enabling.

3.DTMF reception.

6.1.1 RING DETECTION:

When we dial the number the particular receiver line gets AC signal. This signal is given to the transistor so it becomes ON, which in turn helps in the triggering the timer 555. It generates pulses and the ring detector detects the number of ring pulses. The number of ring pulses can be set according to our need using software. The output is applied to pin 3.2 of PIC. The micro controller checks the pin 3 and when it detects the voltage at 3.2 (high) ring signal is detected.

6.1.2 LOOP ENABLING :

When the pin 3.2 goes high, the pin 3.4, which is connected to the relay, becomes high. The relay coil gets charged. The key is attracted and the current flows through the loop. Now the telephone line remains engaged.

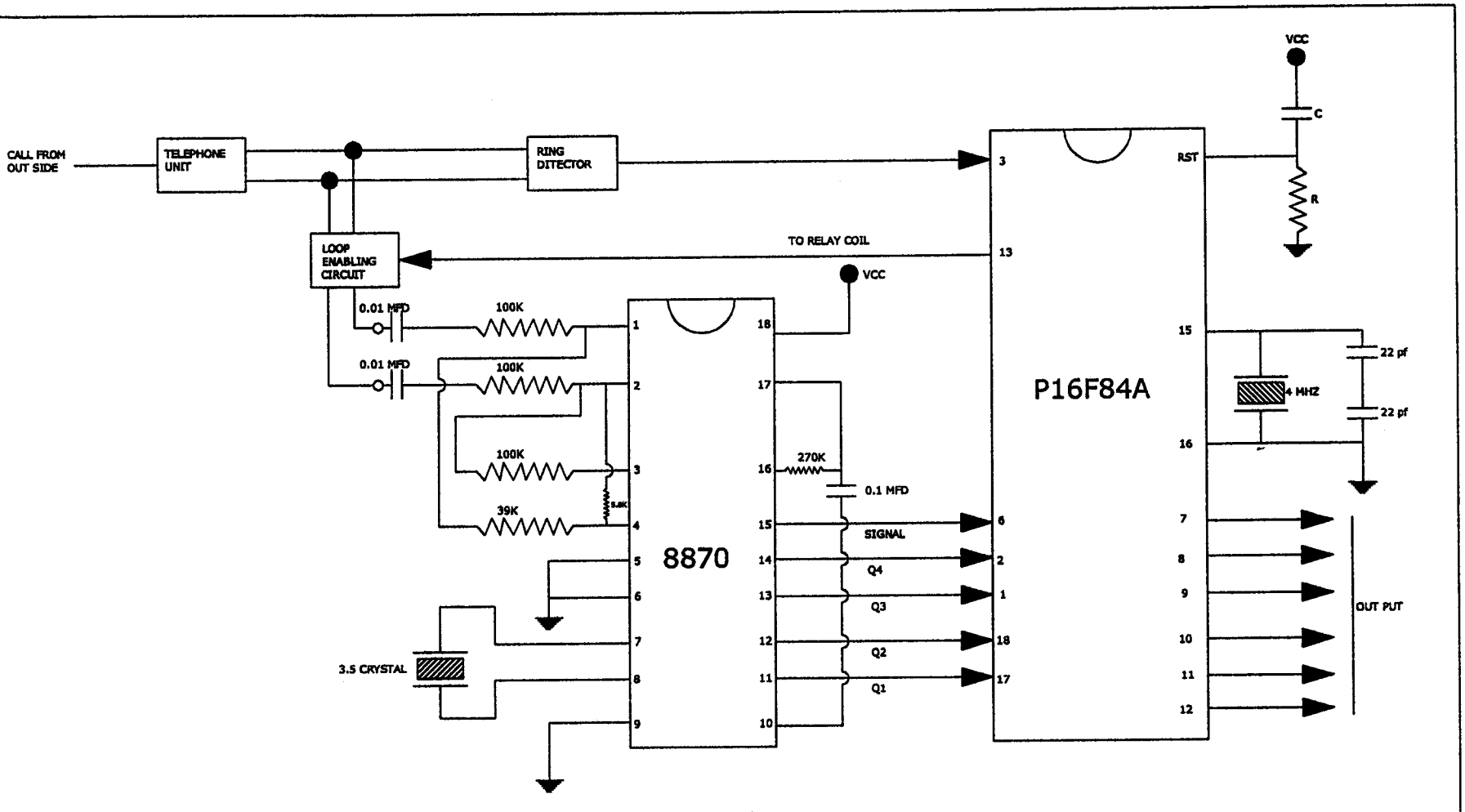
6.1.3 DTMF RECEPTION:

As soon as the loop is enabled the current flows to the DTMF receiver. This current enables to generate the signal (SIGIN), which is given to the Micro controller port 3.3. After the signal is sensed at port 3.3, it waits for a maximum of 5 secs, the relay gets released and the telephone line gets disconnected. Within 5 secs, the number on the DTMF keypad has to be pressed. The DTMF decoder, decodes the number into 4 bits (Q1, Q2, Q3, Q4) which is given to the first 4 bits of port 1 of PIC. Accordingly the output is obtained in the other 4 bits of port 1. This output voltage is used to switch "ON" or "OFF" the devices.

It is assembled as in figure shown in 6.1 and the software is attached in Appendix. It is tested with keeping 3 loads, (Tape Recorder, Fan, Bulb) eventhough it is programmed six appliances.

6.2 SALIENT FEATURES OF THE CIRCUIT

1. Does not require any sensors but just the DTMF telephone network already existing.
2. Signals are not restricted to the line of sight made but rather, the unit can be accessed from any terminal on the network.
3. System access codes serves the purpose of maintaining secrecy of the code and authorized use of the unit.
4. Device status Feed Back using tones is the highlight of the system.



CIRCUIT OPERATION

CONCLUSION

7. CONCLUSION

The fabrication and testing of the "Telematics based Home appliances controller-Embedded System" was a success. The highlight of the prototype of the switching system made by us is its ability to control i.e to switch "ON" or "OFF" a particular device from any terminal by a telephone network. A note worthy aspect of this unit is Multiple access property where in "n" number of devices can be controlled with a slight changes in program which is programmed for six devices and tested for three devices.

Thus this project is a novice attempt of ours to use communication principles for Switching Systems as efficiently as possible. This principle needn't be applied only to home appliances, but to control any devices remotely i.e., industries, offices, etc.

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REFERENCE

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6) Elektor India Magazine, (Nov, 2003).
7) www.microchip.com

APPENDIX

ASSEMBLY PROGRAM FOR RING IDENTIFICATION AND DTMF DETECTION OF NUMBERS PRESSED

```
#include<pic.h>

char command,i,j,local,times;
char dev1,dev2,dev3;
#define loopen  RB1
#define enable  RB0
#define ring       RA4
main()
{
TRISA=0X1F;
TRISB=0X01;
PORTA=0X00;
PORTB=0X00;
OPTION=0X40;
delay();
INTCON=0X80;
PORTB=0;
while(1)
{
INTE=1;
local=1;
for(i=0;i<4;i++)
chring();
local=0;
loopen=1;
command=0;
}
}


chring()
{
while(RA4);
while(!RA4);
}

delay()
{
for(i=0;i<200;i++)
{
OPTION=0X07;
T0IF=0;
TMR0=0XD9;
while(!T0IF);
}
}

static void interrupt isr()
{
if(INTF==0)
return;
if(INTF==1)
{
INTF=0;
if(local==1)
times++;
```

```
if(times==8&&local==1)
{
times--;
command=PORTA&0X0F;

if(command==0x0c&&RB2==0)
{
RB2=1;
command=0;
}
if(command==0x0c&&RB2==1)
{
RB2=0;
command=0;
}
if(command==0x0b&&RB3==0)
{
RB3=1;
command=0;
}
if(command==0x0b&&RB3==1)
{
RB3=0;
command=0;
}
if(command==0x0a&&RB4==0)
{
RB4=1;
command=0;
}
if(command==0x0a&&RB4==1)
{
RB4=0;
command=0;
}
command=0;
}
if(local==0)
{
command=PORTA&0X0F;

if(command==0x0c&&RB2==0)
{
RB2=1;
command=0;
}
if(command==0x0c&&RB2==1)
{
RB2=0;
command=0;
}
if(command==0x0b&&RB3==0)
{
RB3=1;
command=0;
}
if(command==0x0b&&RB3==1)
{
RB3=0;
```

```
}
if(command==0x0a&&RB4==0)
{
RB4=1;
command=0;
}
if(command==0x0a&&RB4==1)
{
RB4=0;
command=0;
}
command=0;
}
}
}
```

TABLE 7-2: PIC16CXXX INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode MSb			LSb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1 (2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1 (2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	lfff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	$\overline{TO}$,$\overline{PD}$	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into standby mode	1	00	0000	0110	0011	$\overline{TO}$,$\overline{PD}$	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.

Note: Additional information on the mid-range instruction set is available in the PICmicro™ Mid-Range MCU Family Reference Manual (DS33023)

7.0 INSTRUCTION SET SUMMARY

Each PIC16CXX instruction is a 14-bit word, divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16CXX instruction set summary in Table 7-2 lists **byte-oriented, bit-oriented,** and **literal and control** operations. Table 7-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the address of the file in which the bit is located.

For **literal and control** operations, 'k' represents an eight or eleven bit constant or literal value.

TABLE 7-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1
PC	Program Counter
TO	Time-out bit
PD	Power-down bit

The instruction set is highly orthogonal and is grouped into three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles with the second cycle executed as a NOP. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 µs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 µs.

Table 7-2 lists the instructions recognized by the MPASM™ Assembler.

Figure 7-1 shows the general formats that the instructions can have.

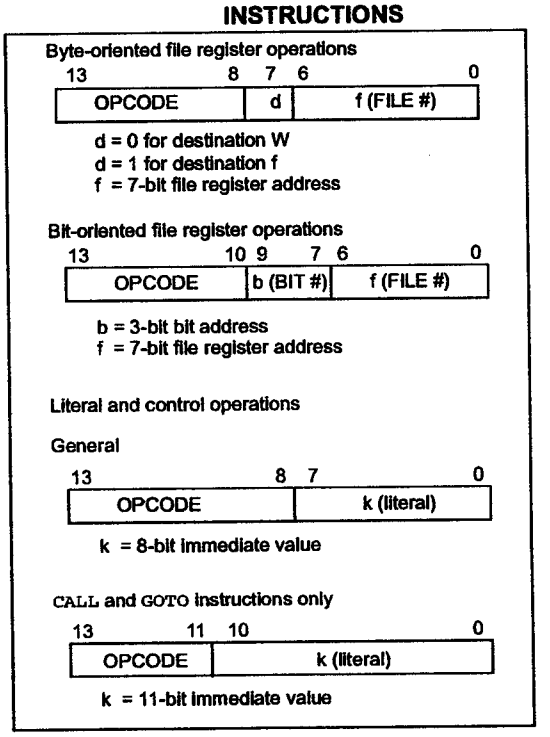
Note: To maintain upward compatibility with future PIC16CXX products, do not use the OPTION and TRIS instructions.

All examples use the following format to represent a hexadecimal number:

0xhh

where h signifies a hexadecimal digit.

FIGURE 7-1: GENERAL FORMAT FOR INSTRUCTIONS



A description of each instruction is available in the PICmicro™ Mid-Range Reference Manual (DS33023).

5.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- Internal or external clock select
- Edge select for external clock
- 8-bit software programmable prescaler
- Interrupt-on-overflow from FFh to 00h

Figure 5-1 is a simplified block diagram of the Timer0 module.

Additional information on timer modules is available in the PICmicro™ Mid-Range Reference Manual (DS33023).

5.1 Timer0 Operation

Timer0 can operate as a timer or as a counter.

Timer mode is selected by clearing bit T0CS (OPTION_REG<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting bit T0CS (OPTION_REG<5>). In Counter mode, Timer0 will increment, either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the Timer0 Source Edge Select bit, T0SE (OPTION_REG<4>). Clearing bit T0SE selects the rising edge. Restrictions on the external clock input are discussed below.

When an external clock input is used for Timer0, it must meet certain requirements. The requirements ensure the external clock can be synchronized with the internal phase clock (Tosc). Also, there is a delay in the actual incrementing of Timer0 after synchronization.

Additional information on external clock requirements is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

5.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer, respectively (Figure 5-2). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusively shared between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The prescaler is not readable or writable.

The PSA and PS2:PS0 bits (OPTION_REG<3:0>) determine the prescaler assignment and prescale ratio.

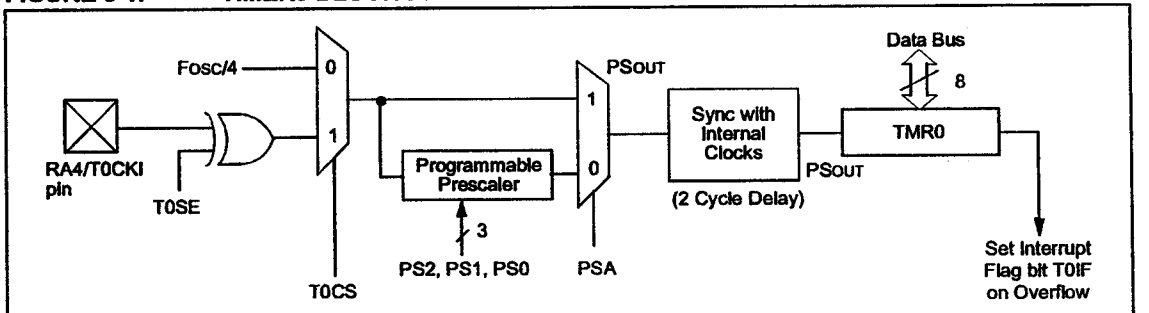
Clearing bit PSA will assign the prescaler to the Timer0 module. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4, ..., 1:256 are selectable.

Setting bit PSA will assign the prescaler to the Watchdog Timer (WDT). When the prescaler is assigned to the WDT, prescale values of 1:1, 1:2, ..., 1:128 are selectable.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF 1`, `MOVWF 1`, `BSF 1`, etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the WDT.

Note: Writing to TMR0 when the prescaler is assigned to Timer0 will clear the prescaler count, but will not change the prescaler assignment.

FIGURE 5-1: TIMER0 BLOCK DIAGRAM



Note 1: T0CS, T0SE, PSA, PS2:PS0 (OPTION_REG<5:0>).
2: The prescaler is shared with Watchdog Timer (refer to Figure 5-2 for detailed block diagram).

4.2 PORTB and TRISB Registers

PORTB is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISB. Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin).

EXAMPLE 4-2: INITIALIZING PORTB

```
BCF     STATUS, RP0 ;
CLRF    PORTB       ; Initialize PORTB by
                    ; clearing output
                    ; data latches
BSF     STATUS, RP0 ; Select Bank 1
MOVLW   0xCF        ; Value used to
                    ; initialize data
                    ; direction
MOVWF   TRISB       ; Set RB<3:0> as inputs
                    ; RB<5:4> as outputs
                    ; RB<7:6> as inputs
```

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit RBPU (OPTION<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

Four of PORTB's pins, RB7:RB4, have an interrupt-on-change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupt-on-change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>).

This interrupt can wake the device from SLEEP. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

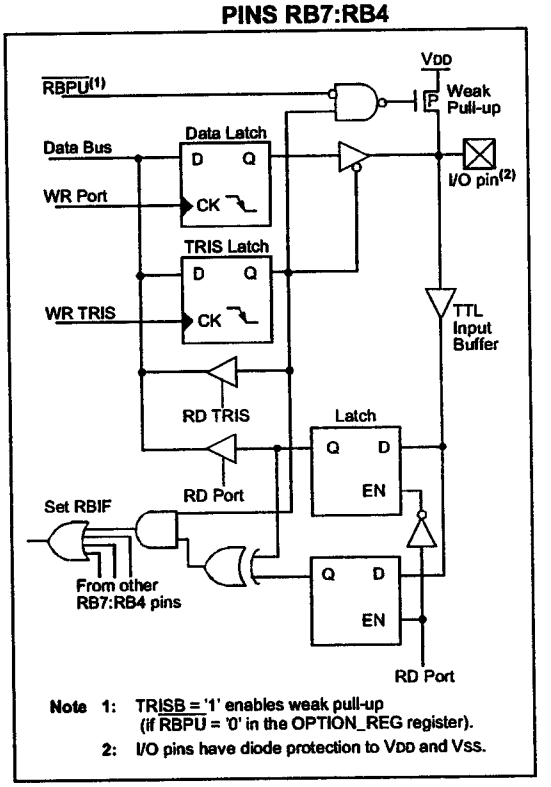
a) Any read or write of PORTB. This will end the mismatch condition.

b) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

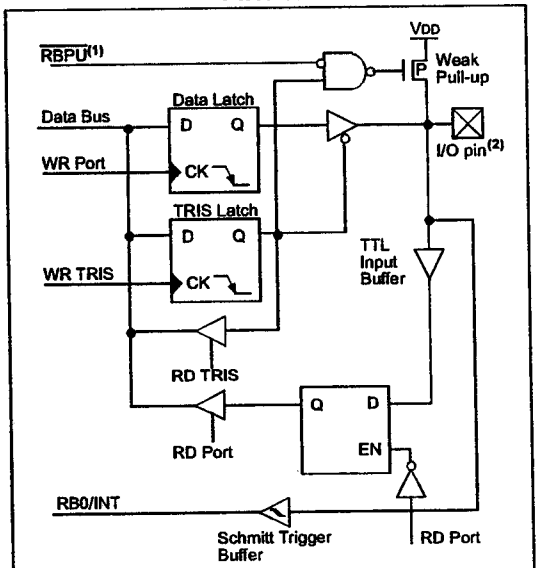
FIGURE 4-3: BLOCK DIAGRAM OF PINS RB7:RB4



Note 1: TRISB = '1' enables weak pull-up (if RBPU = '0' in the OPTION_REG register).

2: I/O pins have diode protection to VDD and VSS.

FIGURE 4-4: BLOCK DIAGRAM OF PINS RB3:RB0



Note 1: TRISB = '1' enables weak pull-up (if RBPU = '0' in the OPTION_REG register).

2: I/O pins have diode protection to VDD and VSS.

4.0 I/O PORTS

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Additional information on I/O ports may be found in the PICmicro™ Mid-Range Reference Manual (DS33023).

4.1 PORTA and TRISA Registers

PORTA is a 5-bit wide, bi-directional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).

Note: On a Power-on Reset, these pins are configured as inputs and read as '0'.

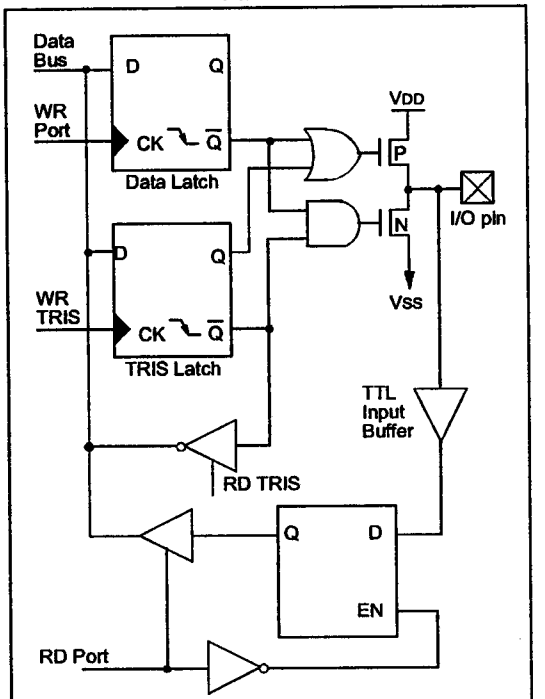
Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read. This value is modified and then written to the port data latch.

Pin RA4 is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA4/T0CKI pin is a Schmitt Trigger input and an open drain output. All other RA port pins have TTL input levels and full CMOS output drivers.

EXAMPLE 4-1: INITIALIZING PORTA

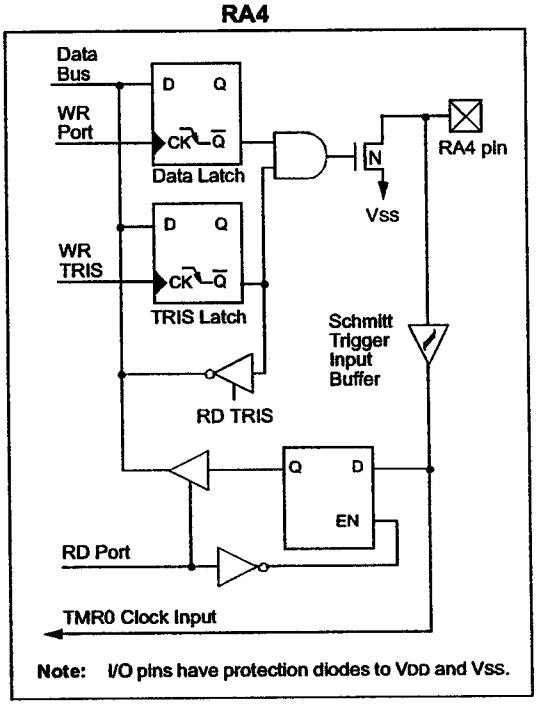
```
BCF     STATUS, RP0 ;
CLRF    PORTA       ; Initialize PORTA by
                    ; clearing output
                    ; data latches
BSF     STATUS, RP0 ; Select Bank 1
MOVLW   0x0F        ; Value used to
                    ; initialize data
                    ; direction
MOVWF   TRISA       ; Set RA<3:0> as inputs
                    ; RA4 as output
                    ; TRISA<7:5> are always
                    ; read as '0'.
```

FIGURE 4-1: BLOCK DIAGRAM OF PINS RA3:RA0



Note: I/O pins have protection diodes to VDD and Vss.

FIGURE 4-2: BLOCK DIAGRAM OF PIN RA4



Note: I/O pins have protection diodes to VDD and Vss.

2.3 Special Function Registers

The Special Function Registers (Figure 2-2 and Table 2-1) are used by the CPU and Peripheral functions to control the device operation. These registers are static RAM.

The special function registers can be classified into two sets, core and peripheral. Those associated with the core functions are described in this section. Those related to the operation of the peripheral features are described in the section for that specific feature.

TABLE 2-1: SPECIAL FUNCTION REGISTER FILE SUMMARY

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on RESET	Details on page
Bank 0											
00h	INDF	Uses contents of FSR to address Data Memory (not a physical register)								---- ----	11
01h	TMR0	8-bit Real-Time Clock/Counter								xxxx xxxx	20
02h	PCL	Low Order 8 bits of the Program Counter (PC)								0000 0000	11
03h	STATUS(2)	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	8
04h	FSR	Indirect Data Memory Address Pointer 0								xxxx xxxx	11
05h	PORTA(4)	---	---	---	RA4/T0CKI	RA3	RA2	RA1	RA0	---x xxxx	16
06h	PORTB(5)	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0/INT	xxxx xxxx	18
07h	---	Unimplemented location, read as '0'								---	---
08h	EEDATA	EEPROM Data Register								xxxx xxxx	13,14
09h	EEADR	EEPROM Address Register								xxxx xxxx	13,14
0Ah	PCLATH	---	---	---	Write Buffer for upper 5 bits of the PC(1)					---0 0000	11
0Bh	INTCON	GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	10
Bank 1											
80h	INDF	Uses Contents of FSR to address Data Memory (not a physical register)								---- ----	11
81h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	9
82h	PCL	Low order 8 bits of Program Counter (PC)								0000 0000	11
83h	STATUS (2)	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	8
84h	FSR	Indirect data memory address pointer 0								xxxx xxxx	11
85h	TRISA	---	---	---	PORTA Data Direction Register					---1 1111	16
86h	TRISB	PORTB Data Direction Register								1111 1111	18
87h	---	Unimplemented location, read as '0'								---	---
88h	EECON1	---	---	---	EEIF	WRERR	WREN	WR	RD	---0 x000	13
89h	EECON2	EEPROM Control Register 2 (not a physical register)								---- ----	14
0Ah	PCLATH	---	---	---	Write buffer for upper 5 bits of the PC(1)					---0 0000	11
0Bh	INTCON	GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	10

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0', q = value depends on condition

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a slave register for PC<12:8>. The contents of PCLATH can be transferred to the upper byte of the program counter, but the contents of PC<12:8> are never transferred to PCLATH.

2: The $\overline{TO}$ and $\overline{PD}$ status bits in the STATUS register are not affected by a $\overline{MCLR}$ Reset.

3: Other (non power-up) RESETS include: external RESET through $\overline{MCLR}$ and the Watchdog Timer Reset.

4: On any device RESET, these pins are configured as inputs.

5: This is the value that will be in the port output latch.

2.4 PCL and PCLATH

The program counter (PC) specifies the address of the instruction to fetch for execution. The PC is 13 bits wide. The low byte is called the PCL register. This register is readable and writable. The high byte is called the PCH register. This register contains the PC<12:8> bits and is not directly readable or writable. If the program counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP. All updates to the PCH register go through the PCLATH register.

2.4.1 STACK

The stack allows a combination of up to 8 program calls and interrupts to occur. The stack contains the return address from this branch in program execution.

Mid-range devices have an 8 level deep x 13-bit wide hardware stack. The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not modified when the stack is PUSHed or POPed.

After the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

2.5 Indirect Addressing; INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is indirect addressing.

EXAMPLE 2-1: INDIRECT ADDRESSING

- Register file 05 contains the value 10h
- Register file 06 contains the value 0Ah
- Load the value 05 into the FSR register
- A read of the INDF register will return the value of 10h
- Increment the value of the FSR register by one (FSR = 06)
- A read of the INDF register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no-operation (although STATUS bits may be affected).

A simple program to clear RAM locations 20h-2Fh using indirect addressing is shown in Example 2-2.

EXAMPLE 2-2: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```
        movlw   0x20    ;initialize pointer
        movwf   FSR     ;to RAM
NEXT    clrf    INDF    ;clear INDF register
        incf    FSR     ;inc pointer
        btfss   FSR,4   ;all done?
        goto    NEXT    ;NO, clear next
CONTINUE
        :               ;YES, continue
```

An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 2-3. However, IRP is not used in the PIC16F84A.

2.2 Data Memory Organization

The data memory is partitioned into two areas. The first is the Special Function Registers (SFR) area, while the second is the General Purpose Registers (GPR) area. The SFRs control the operation of the device.

Portions of data memory are banked. This is for both the SFR area and the GPR area. The GPR area is banked to allow greater than 116 bytes of general purpose RAM. The banked areas of the SFR are for the registers that control the peripheral functions. Banking requires the use of control bits for bank selection. These control bits are located in the STATUS Register. Figure 2-2 shows the data memory map organization.

Instructions MOVWF and MOVF can move values from the W register to any location in the register file ("F"), and vice-versa.

The entire data memory can be accessed either directly using the absolute address of each register file or indirectly through the File Select Register (FSR) (Section 2.5). Indirect addressing uses the present value of the RP0 bit for access into the banked areas of data memory.

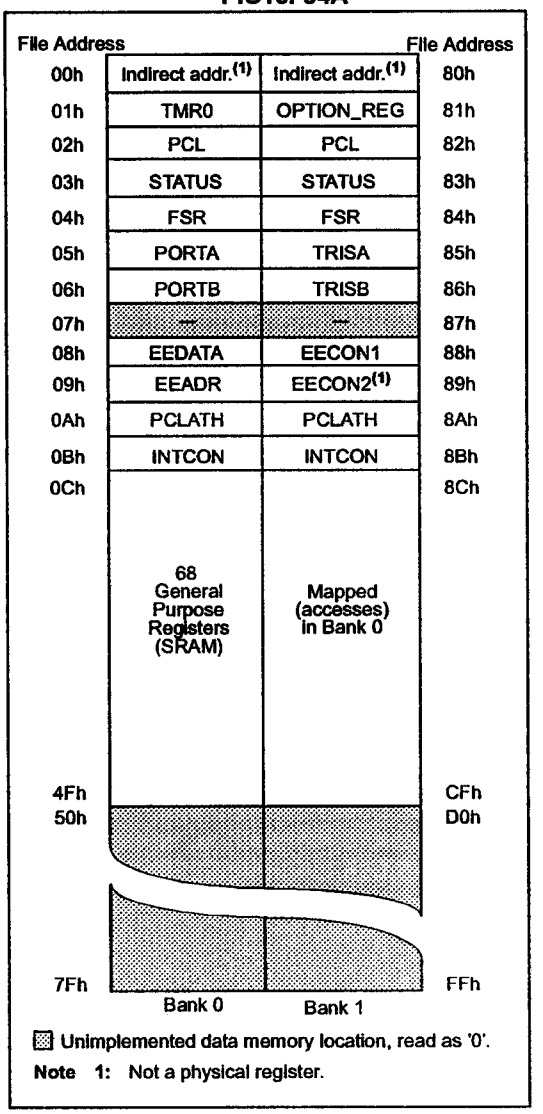
Data memory is partitioned into two banks which contain the general purpose registers and the special function registers. Bank 0 is selected by clearing the RP0 bit (STATUS<5>). Setting the RP0 bit selects Bank 1. Each Bank extends up to 7Fh (128 bytes). The first twelve locations of each Bank are reserved for the Special Function Registers. The remainder are General Purpose Registers, implemented as static RAM.

2.2.1 GENERAL PURPOSE REGISTER FILE

Each General Purpose Register (GPR) is 8-bits wide and is accessed either directly or indirectly through the FSR (Section 2.5).

The GPR addresses in Bank 1 are mapped to addresses in Bank 0. As an example, addressing location 0Ch or 8Ch will access the same GPR.

FIGURE 2-2: REGISTER FILE MAP - PIC16F84A



2.0 MEMORY ORGANIZATION

There are two memory blocks in the PIC16F84A. These are the program memory and the data memory. Each block has its own bus, so that access to each block can occur during the same oscillator cycle.

The data memory can further be broken down into the general purpose RAM and the Special Function Registers (SFRs). The operation of the SFRs that control the "core" are described here. The SFRs used to control the peripheral modules are described in the section discussing each individual peripheral module.

The data memory area also contains the data EEPROM memory. This memory is not directly mapped into the data memory, but is indirectly mapped. That is, an indirect address pointer specifies the address of the data EEPROM memory to read/write. The 64 bytes of data EEPROM memory have the address range 0h-3Fh. More details on the EEPROM memory can be found in Section 3.0.

Additional information on device memory may be found in the PICmicro™ Mid-Range Reference Manual, (DS33023).

2.1 Program Memory Organization

The PIC16FXX has a 13-bit program counter capable of addressing an 8K x 14 program memory space. For the PIC16F84A, the first 1K x 14 (0000h-03FFh) are physically implemented (Figure 2-1). Accessing a location above the physically implemented address will cause a wraparound. For example, for locations 20h, 420h, 820h, C20h, 1020h, 1420h, 1820h, and 1C20h, the instruction will be the same.

The RESET vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK - PIC16F84A

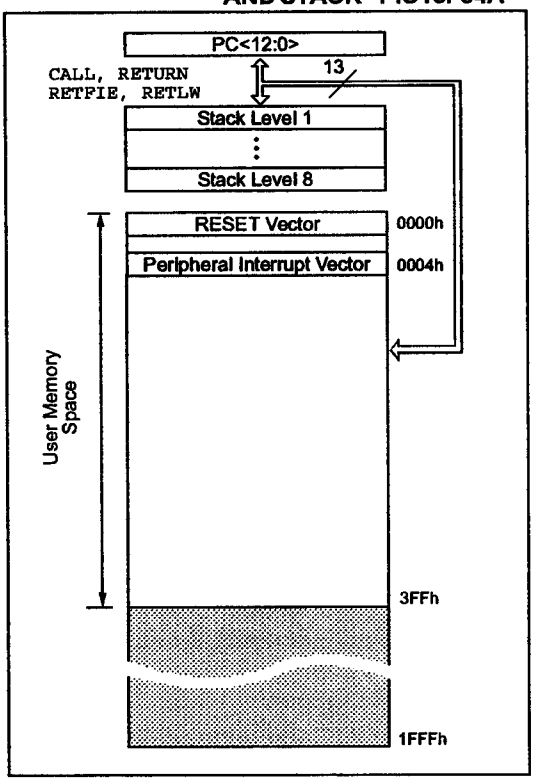


TABLE 1-1: PIC16F84A PINOUT DESCRIPTION

Pin Name	PDIP No.	SOIC No.	SSOP No.	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	16	16	18	I	ST/CMOS(3)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	15	19	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKOUT, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
$\overline{MCLR}$	4	4	4	I/P	ST	Master Clear (Reset) input/programming voltage input. This pin is an active low RESET to the device.
						PORTA is a bi-directional I/O port.
RA0	17	17	19	I/O	TTL	
RA1	18	18	20	I/O	TTL	
RA2	1	1	1	I/O	TTL	
RA3	2	2	2	I/O	TTL	
RA4/T0CKI	3	3	3	I/O	ST	Can also be selected to be the clock input to the TMR0 timer/counter. Output is open drain type.
						PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	6	6	7	I/O	TTL/ST(1)	RB0/INT can also be selected as an external interrupt pin.
RB1	7	7	8	I/O	TTL	
RB2	8	8	9	I/O	TTL	
RB3	9	9	10	I/O	TTL	
RB4	10	10	11	I/O	TTL	Interrupt-on-change pin.
RB5	11	11	12	I/O	TTL	Interrupt-on-change pin.
RB6	12	12	13	I/O	TTL/ST(2)	Interrupt-on-change pin. Serial programming clock.
RB7	13	13	14	I/O	TTL/ST(2)	Interrupt-on-change pin. Serial programming data.
VSS	5	5	5,6	P	—	Ground reference for logic and I/O pins.
VDD	14	14	15,16	P	—	Positive supply for logic and I/O pins.

Legend: I= input O = Output I/O = Input/Output P = Power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

1.0 DEVICE OVERVIEW

This document contains device specific information for the operation of the PIC16F84A device. Additional information may be found in the PICmicro™ Mid-Range Reference Manual, (DS33023), which may be downloaded from the Microchip website. The Reference Manual should be considered a complementary document to this data sheet, and is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

The PIC16F84A belongs to the mid-range family of the PICmicro® microcontroller devices. A block diagram of the device is shown in Figure 1-1.

The program memory contains 1K words, which translates to 1024 instructions, since each 14-bit program memory word is the same width as each device instruction. The data memory (RAM) contains 68 bytes. Data EEPROM is 64 bytes.

There are also 13 I/O pins that are user-configured on a pin-to-pin basis. Some pins are multiplexed with other device functions. These functions include:

- External interrupt
- Change on PORTB interrupt
- Timer0 clock input

Table 1-1 details the pinout of the device with descriptions and details for each pin.

FIGURE 1-1: PIC16F84A BLOCK DIAGRAM