8088 System Board with Signal Reception Interface

P 1272 Project Work

Submitted in partial fulfilment of the requirements for the Award of the Degree of Bachelor of Engineering in Electronics and Communication Engineering of the Bharathiar University, Coimbatore-641 046

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during the academic year 1989-90

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P-1272

SYNOPSIS

The project comprises of the design and fabrication of an 8088 Add-on board to the existing 8085 and Z80 kits. This involves the design and fabrication of the proto type card, developing the monitor program for the use and testing sample programs in the developed board. The board is designed such that it can be inserted in the same edge connector sockets of the 8085/Z84 board.

A signal receiver card using the ADC 0804 is also developed. The software for signal reception is also dealt with and discussed.

CONTENTS

INTRODUCTION

In the last decade, microprocessors have had a major impact in the area of industrial process control. The introduction of fast 16-bit microprocessors like the 8086/8088 have added a new dimension towards control capabilities.

The microprocessor is a general purpose programmable logic device. The microprocessor requires both concepts and skills both hardware and software. The hardware is the physical structure of the microprocessor while the software concerned makes it come alive.

This project is centred around the 8088, which can be used for analysis of signals received that can be used for control applications.

The 8088 which was introduced after the 8086 retained all the powers of 8086, including the 16 bit manipulations of Arithmetic and logic, but the external data bus was made to have just 8 bits for convenience. Hence, the 8088 became more popular for it simplified the hardware and retained the 16-bit power. The 8088 board designed and fabricated here is compatible with the hexadecimal keyboard and input/output board. It can be inserted in the same edge connector sockets of the 8085/Z-80 board. A signal receiver card with ADC 0804 is developed.

CHAPTER - 1

DISCRIPTION OF THE CIRCUIT

1.1 SYSTEM BOARD

The 8088 has built-in logic to handle bus access priorities in multi-chip systems. In such systems each processor will have its own memory and each processor can also share a common memory. The 8088 has a 16 bit data path internally. In this both bytes operation and word operations are possible. Thus one could write a program to add bytes or words.

The clock signal for the basic 8088 chip is a 5 MHz derived via a divide by-three circuit used in the 8284 clock chip, from a standard 15MHz crystal connected to it. The simplest instruction of the 8088 takes about three clock cycles and mainly it depends on the type of operation performed.

The circuit diagramof the system board is shown in Fig1.1 The 8284 clock generator uses a 15 MHz crystal, divides it by three and generates the clock for the 8088. It also generates the RESET and READY signals, synchronised with the clock. A RESET switch is therefore connected to the 8284. The HOLD, $\overline{\text{TEST}}$, NMI pins are tied through resistors to ground, since there is no need to use them now. Since we are used signal reception channel the INTR and $\overline{\text{INTA}}$ pins are brought to the edge connector, otherwise these two pins can tied through resistors to ground.

The AD0-AD7 multiplexed address-data lines are fed to the 74LS 374 whose output provides the A_0-A_7 low-order address lines, after demultiplexing them with the address-latch enable (ALE) pulse going to pin 11. The AD_0-AD_7 lines also go to the 74LS 245 buffer. The DEN and DT/R pin 26 and 27 respectively are connected to the enable and direction control pins of this bidirectional bus-buffer chip. This chip features a chip enable (CE) input for easy cascading and a send/Receive (S/R) input for direction control. Hence, the pins 11 to 18 of this chip provide the buffered data bus for use by the systems.

The address decoder 74 LS 155 chip is given the high order address lines A13, A14 and A15 as well as the memory enable signal. This chip is a dual 1-of-4 decoder with common address inputs and separate gated enable inputs. These 8 combinations are available from the output pins of the 74LS 155 decoder. The corresponding hexadecimal ranges are shown in fig1.1 . Among the available ranges, the 8K block from E000 to FFFF is used for the selection of EPROM and the 8K block lying in the lowest memory range (0000 to 1FFF) is used for the selection of RAM. The remaining 8K memory blocks are used for addressing other peripheral chips which may be used. The unique feature of the system board is that these lines are brought out of the via the edge connector pins of the 8085 board so that these boards are interchangeable.

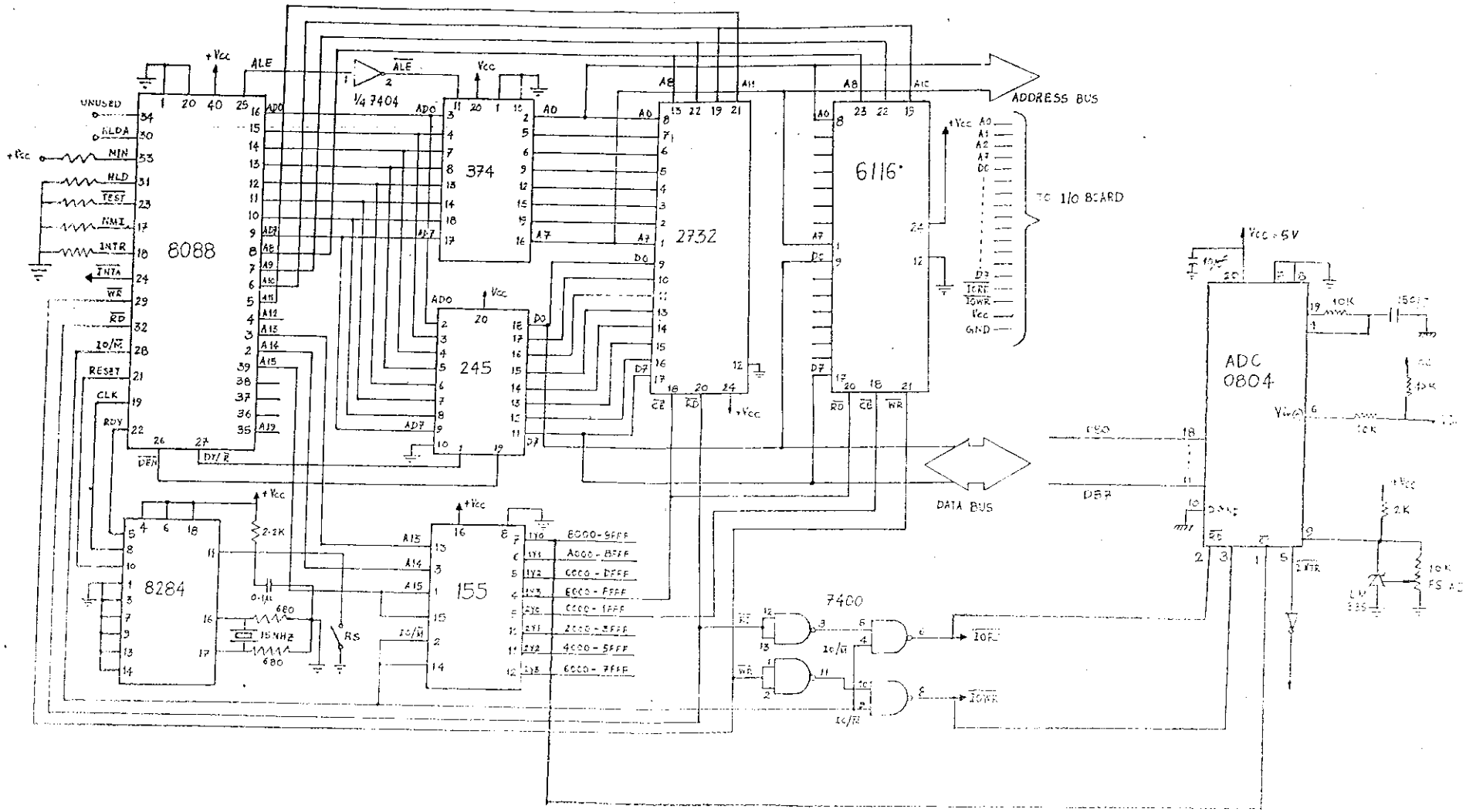


Fig: 1.1 CIRCUIT DIAGRAM

The address lines A_0-A_7 and A_8, A_9, A_{10}, A_{11} go to the address pins of the 2732 EPROM. It is seen that the RD Signal goes to the output enable pin of the EPROM.

Address lines A_0-A_7, A_8,A_9,A_{10} go to the address-input pins of the RAM. As in the EPROM, the 8088 RD and WR signals go to its output enable and write enable pins.

The EPROM address is in high end of the memory since the 8088, upon RESET, causes the program to begin, fetching instructions from the address FFFO. Hence this address must be in the non-volatile memory or PROM. so that program execution of the monitor takes place as soon as power is applied and RS (reset) switch is pressed.

The RAM is kept in the lowest part of memory since the interrupt vectors are designed by the 8088 to access this space.

1.2 System Processor:

The heart of the system board is the INTEL 8088 microprocessor. This processor is eight bit extended version of INTEL 16-bit 8086 processor and is software compatible with 8086. The pin diagram of the 8088 is shown in fig. 1.2 Since the processor can access upto one megabyte of memory it needs four more address lines than the 8085. This processor contains the 8-bit data bus is named AD_0 to AD_7 and also these lines contain the address lines of low order i.e. A_0 to A_7 in a multiplexed manner.

The 8088 processor needs a clock generator chip separately. It needs just a single 5V power supply. For accessing input output ports and memory, the IO/M signal indicates that it the pin goes high an input-output operations occur and if it is low a memory read write operation takes place. The signal DT/R becomes necessary when bi-directional buffer is required, since data can either go in or out of the 8088 processor.

There are two possible interrupts, one the non-maskable interrupt NMI (pin 17) and the other the usual INTR Pin 18. The INTR Pin when takes high, interrupts the processor and an interrupt-acknowledge signal comes via pin 24 (INTA). The RESET and READY input signals are derived from the 8284 clock-chip because these inputs should he synchronised with the clock signal. There is another pin called the MN/MX, control pin. When this is tied to 5V, the processor works in its 'minimum system' hardware configurations. In the system

board we have caused only minimum mode. In the maximum mode, some of the pins perform a dual function with the help system controller chip 8288.

1.2.1. THE 8088 MPU

The 8088 microprocessor is actually just one IC chip in a family of 16-bit processors. The 8088 can read memory only 8 bits at a time. CPU Model for 8088 is shown fig.1.3.

The 8088 CPU Architecture

The study of microprocessors is broadly divided under:

1) The CPU Architecture, including the internal registers and flags and the instruction set i.e., the dictionary of program instructions. The µp will recognize and execute.

2) The electrical interface, including the data, address and control buses and the clock generation circuitry.

The µp generates the timing signals and synchronizes the transfer of data between memory, I/O and itself. It accomplishes this task via the 3-bus system architecture.

The µp also has a software fn., It must recognize, decode and execute program instructions fatched from the memory unit. This requires an ALU within the CPU to perform arithmetic and logical functions.

It is organized as two separate processors, called the bus interface unit (BIU) and the execution unit (EU). The BIU provides hardware fns, including generation of the memory and I/O addresses for the transfer of bata between the outside world outside the CPU, that is and the EU.

The EU receives program instruction codes from the BIU, executes these instructions and stores the results in general registers By passing the data back to the BIU, data can also be stored ina memory location or written to an O/P device. The EU has no connections to the system buses. it receives and O/Ps all its data through the BIU. In the 8088, the BIU bus path is 8 bits wide. The 8088 instruction queue is four bytes long.

Fetch and Execute

1) The BIU o/ps the contents of the instruction pointer register (IP) onto the address bus, causing the selected byte or word to be read into the BIU.

2) Register IP is incremented by 1 to prepare for the next instruction fetch.

3) Once inside the BIU, the instruction is passed to the "queue". This is a first-in, first-out storage register.

4) Assuming that the queue is initially empty, the EU immediately draws this instruction from the queue and begins execution.

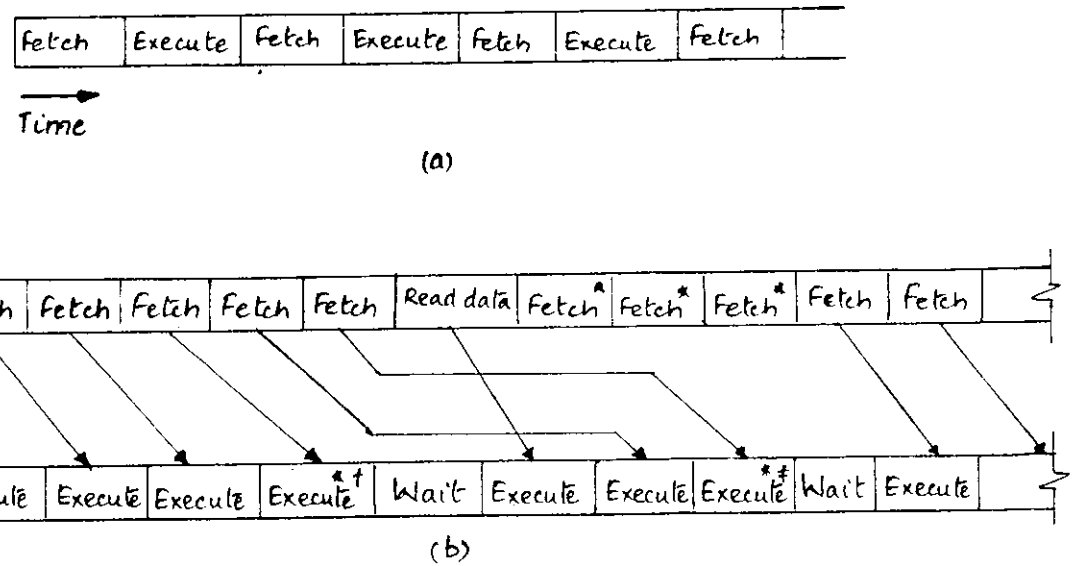
5) While the EU is executing this instruction, the BIU proceeds to fetch a new instruction. Depending on the execution time of the first instruction, the BIU may fill the queue with several new instructions before the EU is ready tc draw its next instruction.

P 1272

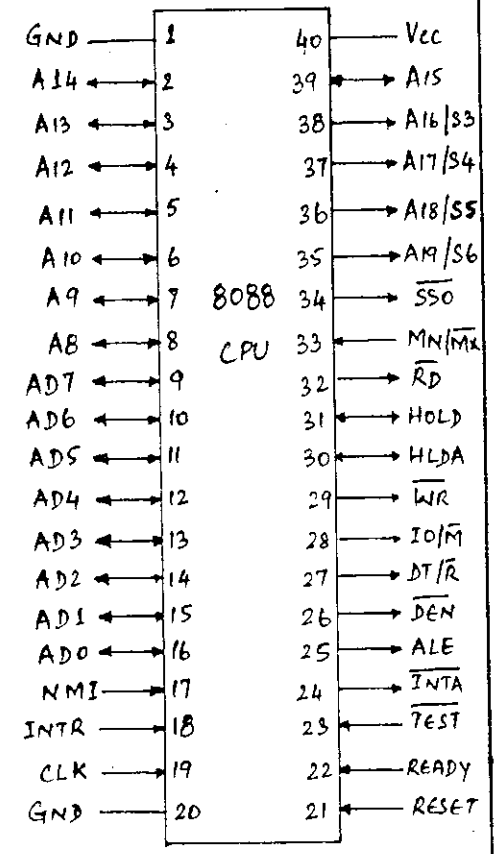
The BIU is programmed to fetch a new instruction whenever the queue has room for one (with the 8088) additional byte. The advantage of this pipelined architecture is that the EU can execute instructions almost continually instead of having to wait for the BIU to fetch a new instruction. This is shown schematically in the fig!.4

There are 3 conditions that will cause the EU to enter a "wait mode". The first occurs when an instruction requires access tc a memory location not in the queue. The BIU must suspend fetching instructions and output the address of this memory location.Afting waiting for the memory access, the EU can resume executing instruction codes from the queue.

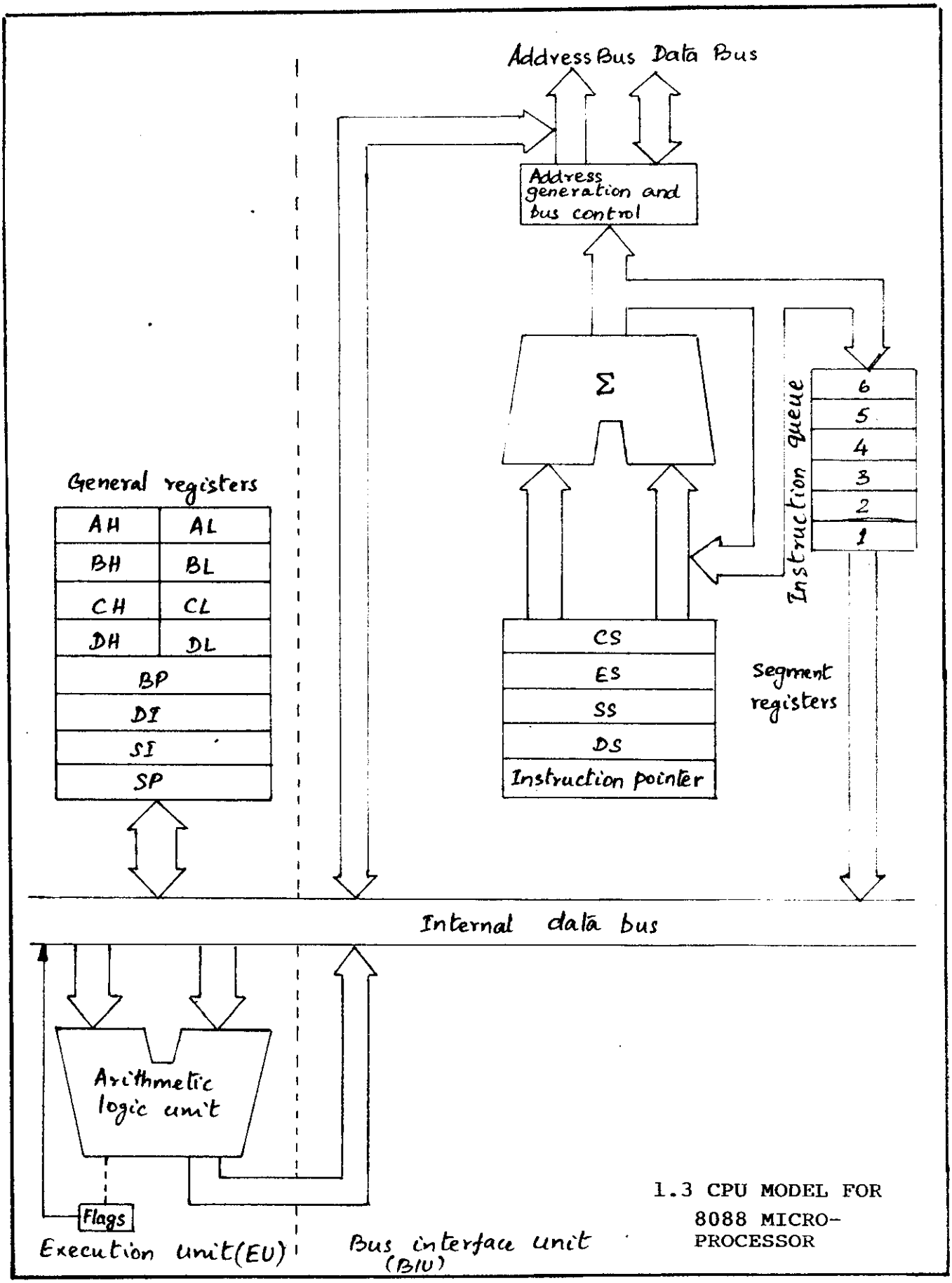
The second condition occurs when the instruction to be executed is a "jump" instruction. In this cases control is to be transferred to a new address. The queue, however, assumes that instructions will always be executed in sequence and thus will be holding the "wrong" instruction codes. The EU must wait while the instruction at the jump address is fetched. Note that any bytes presently in the queue must be discarded.



1.4 FETCH EXECUTE CYCLE OF 8088 MICROPROCESSOR



1.2 PIN OUT DIAGRAM FOR 8088 MICROPROCESSOR



1.3 CPU MODEL FOR 8088 MICRO-PROCESSOR

One other condition can cause the BIU to suspend fetching instructions that are slow to execute. At four clock cycles per instruction fetch, the queue will be completely filled during the execution of this single instruction.

A subtle advantage to the pipelined architecture is that the BIU can access memory at a somewhat "leisurely" pace because the next serveral instructions usually in the queue.

1.2.2 Segmented Memory

8088, being a 16-bit processor, reads memory at a rate of 8 instructions at a time. There are two main reasons for it to use an 8 bit memory. First it allows the proocessor to work on bytes as well as words. This is especially important with I/O devices such as printers, terminals which are designed to transfer 8 bit data generally. Second, many of the 8088 codes are single bytes. Other instructions may require anywhere from 2 to 7 bytes. By being able to access individual bytes, these odd lengthened instructions can be handled.

The memory of 8088 is segmented into small spaces each space possessing a byte in turn. If the memory consists of 2^{10} bytes of different addresses then there has to be that much of segments. Moreover, 8088 with its 8-bit data bus interfaces to the 1 MB of memory as a single bank unlike the 8086 which goes on with 2 separate memory banks.

Memory map is an important aspect with 8088. It is nothing

but a guide like system, showing how the system memory is allocated. The blocks of memory are alloted is a proper way to ROM, RAM etc and the programme is intimated about that.

Within the 1 MB of mem. space, 8088 defines 4 major blocks called the code segment, stack segment, data segment, extra segment. Code segement holds the program instruction codes. Data segment stores data for the program. Stack separate stores interrupt and subroutine return addresses. Extra segment is an extra data segment and is often meant for shared data. The very concept of segmented memory is to provide more space for the user for processers.

An address within a segment is called an 'offset or logical address'. But logical address say 5H in a code segment (say B00H) actually corresponds to the real address which is B00H + 5H = B005H which is called as physical address. Physical address is 20 bits long and corresponds to the actual binary code O/P by the BIU on the address bus lines whereas logical address is an offset from location 0 of a given segment.

The main aspect to be noticed with segmented memory is that the program opcodes will be fetched from the code segment, while program data variables will be stored in the data and extra segment. The advantage of having separate data and code segment is that one program can work on different sets of data. Perhaps the greatest advantage of segmented memory is that program that reference logical addresses only can be loaded and run anywhere in the memory.

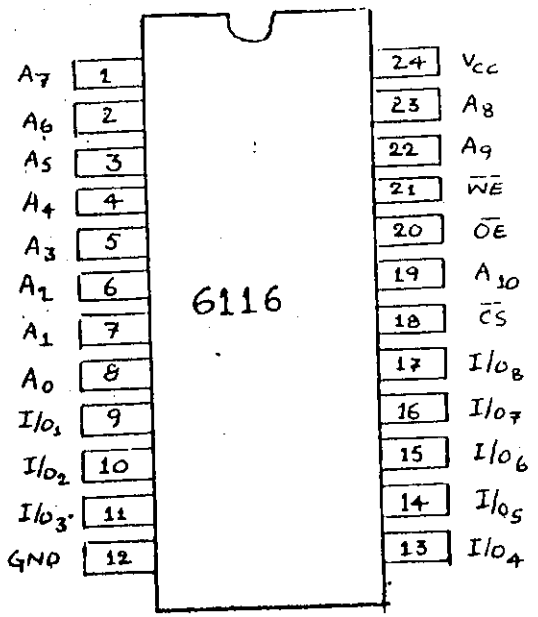
1.3 Memory devices:

The system board designed uses on board permanent and volatice memory devices (2732 - Erasable programmable ROM and 6116 - RAM) respectively) and can hold system program upto 32 kilo bytes. A previously stored BIOS in the EPROM controls the system operations temporary operations performed in the system use the RAM locations and hence the time of accessing problems get minimised. The mapping of the chips are done considering them as extensions of the main memory inside the 8088 itself. The program sequence used for data reception from the ADC is stored in the EPROM and the received data stored in pre defined memory locations. The various stages of transfer taking place through registers in the 8088 and the RAM.

1.3.1. 6116 RAM

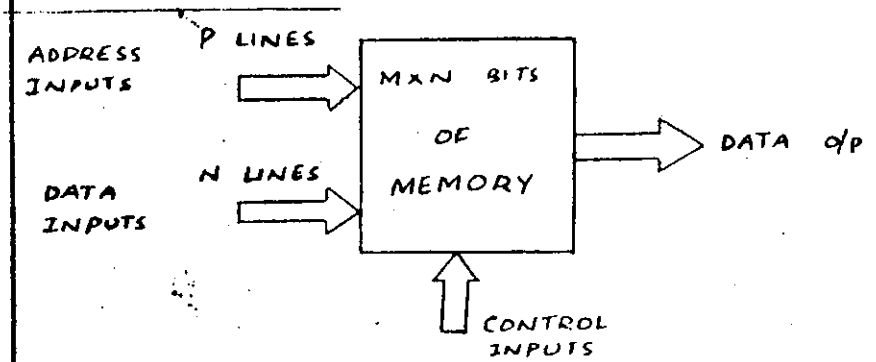
In this project we are using the 6116 2K x 8 light speed CMOS RAM. The 6116 uses 16 K D Flip-Flops for its storage calls. These are organized in 2K groups of 8. The product of the number of unique locations and the number of memory cells at each location gives the total number storage devices in the memory IC.

Refer to fig1.5 By observing the number Of address inputs we can calculate the total number of unique storage locations. The pin out in fig1.6 indicates that the 6116 has address pins. 2^{11} = 2K unique memory locatioins. Because the 6116 has eight I/O pims, there must be eight storage cells at each unique location. This agrees with the 2K x 8 description Of the 6116.



1.6 PIN DIAGRAM OF 6116

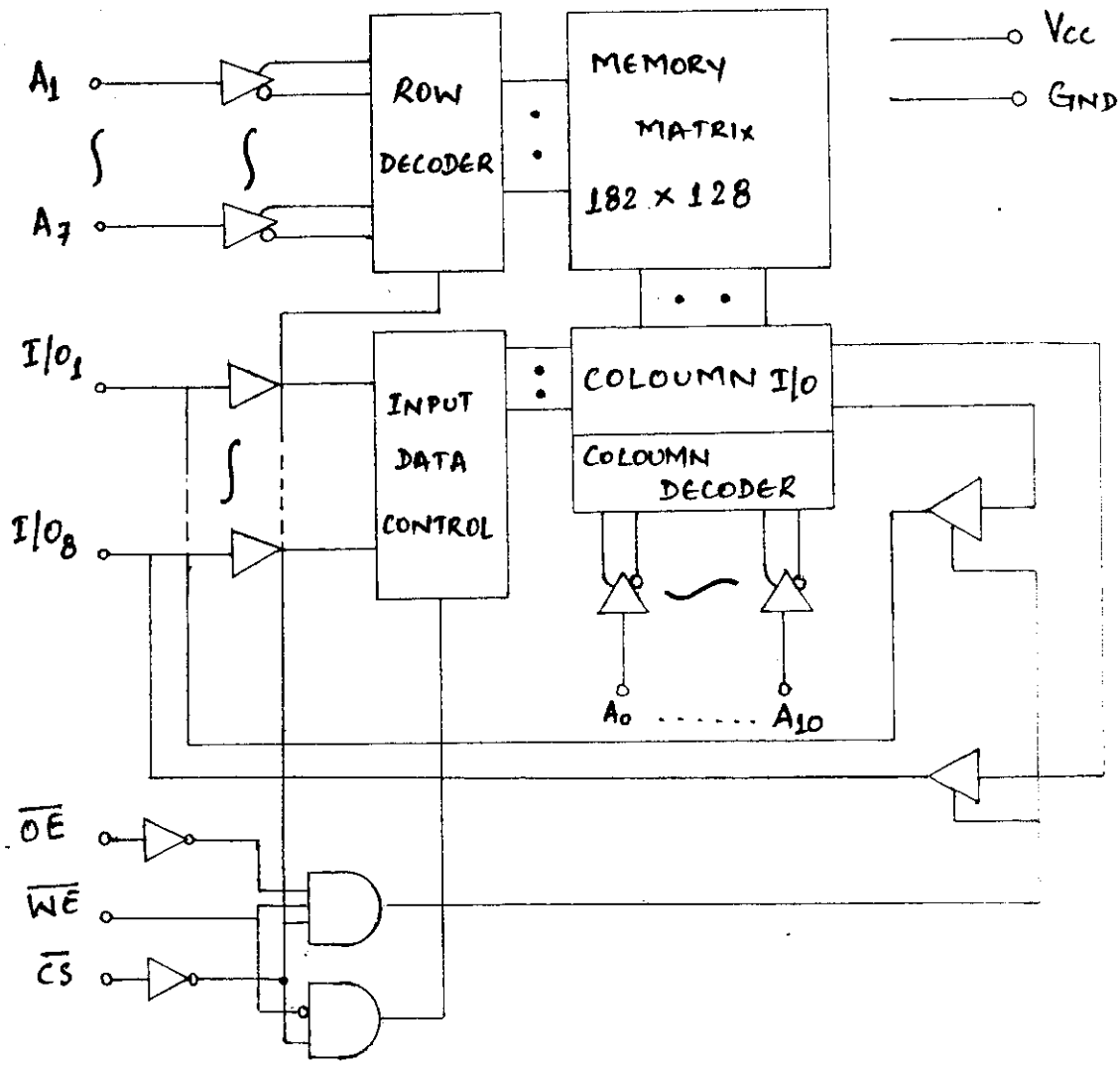
1.5 BLOCK DIAGRAM OF ANY MEMORY DEVICE



Refer to the functional block diagram 1.7 Notice the address inverter - like devices that the 11 address lines are driving. The inverter like drivers imply that both the true and inverted values of the address lines are applied to the row and column decode circuitry.

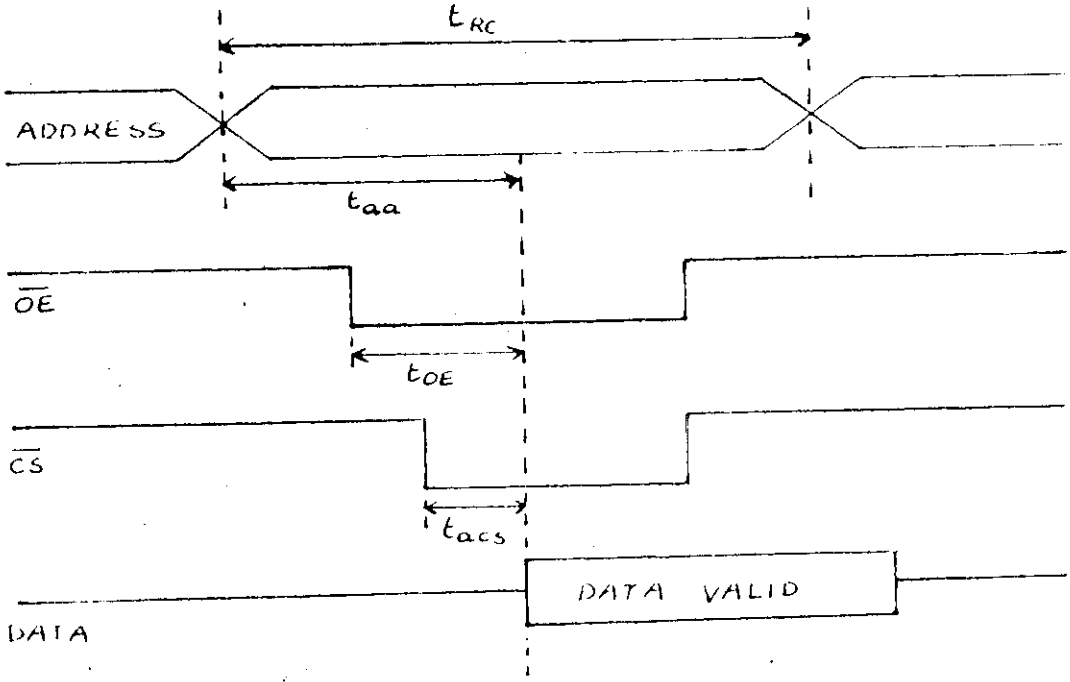
The data I/O lines are buffered on the input and driven by three-state drivers on the output. The only power requirements of the 6116 is +5V and ground. The last part of the functional diagram consists consists of the control bus inputs. Those are output enable (OE), write enable (WE) and chip select (CS). If the o/P of the top AND gate goes active high, the three state data outputs buffers are enabled. This AND gate control the memory read operation. Where as the active high output of the bottom AND gate controls the memory write operations. The read operation will occur when both the chip select and output enable inputs are active low. The write operation will occur when both the chip select and write enable inputs are active low.

The microprocessor performing the read and write operation will have an 8 bit bidirectional data bus, 16 bit address bus, and a control bus with the active low signals memory request, write and read. The 6116 has different read access times (120, 150 and 200ns), so it in necessary to mention this specification with chip. The write cycle time is the write equivalent of the read cycle time. The WE signal is held at the inactive high level through out the read cycle. The processor will provide a 16 bit address denoting the memory loca-

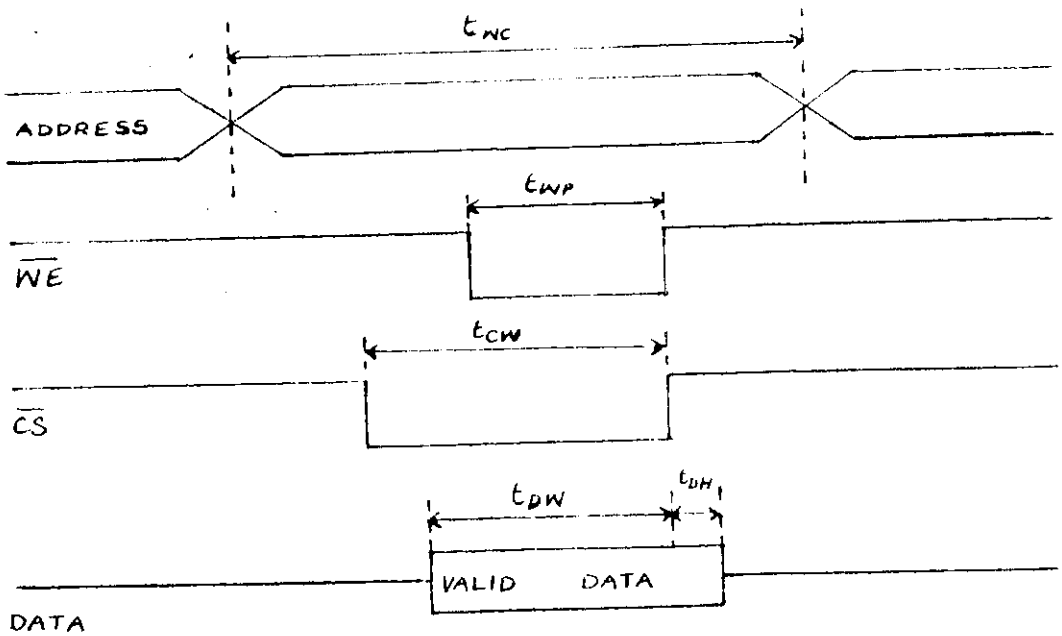


1.7 FUNCTIONAL DIAGRAM OF 6116

tion to be read. Address bits A_0 through A_{10} are directly connected to the 6116. Where as address bits A_0 through A_{15} and MEMRQ will be used to create the chip select pulse. The output enable of the 6116 is driven by the RD of utput of the microprocessor. The typical read cycle shown in fig. 1.8 There are two possible ways to perform a 6116 write. The signal OE is held at an inactive logic 1 level. This will assure that the three state output buffers in the 6116 are never enabled when the microprocessor is outputting data or to the data bus. When the chip select goes active, the three state buffers will momentarily be enable until the write enable goes active. A typical (6116 memory write cycle is shown in fig.1.9



1.8 READ CYCLE OF 6116



1.9 WRITE CYCLE OF 6116

1.3.2. EPROM

The EPROM is a type of ROM that can be erased and reprogrammed many times. The EPROM 2732 is used here in the system board. The 2732 has 4K bytes of programming sites on the metal oxide FETS. It is a 5V operating type.

The 2732 is exactly same as chip 2716 except for pin 21 which takes the next address input A11, so that it has a 4K access. In this chip the pin 20 needs 25V for programming and a low signal (ground) for reading. One of the important features of this chip is that the otput enable (OE) is separate from the chip enable (CE) control. The OE control eliminates bus contention in microprocessor systems. The CE is used by the 2732 to place it in a stand by mode ($CE=V_4$) which reduces power consumption without increasing access time. The programming pulse applied to pin 18 is a negative going pulse of 50 ms. The pin out diagram is shown in appendix.

Erasure Characteristics

If a mistake occurs in the data programmed the whole EPROM should be erased and reprogrammed. The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelength shorter than approximately 4000 A°. The recommended and standard erasure procedure is exposure to short wave ultraviolet light which has a wavelength of 2537 A°. In the center of an EPROM is a clear and round window. If this is exposed to UV (Ultraviolet) light.

the previously programmed information will be erased. The integrated dose for erasure should be a minimum of 15W sec/m^2. The erasure time with this dosage is 15 to 20 minutes using an UV lamp with a 1200 $\mu w/cm^2$ power rating. After each erasure, all bits of the EPROM are in the '1' state. Data is introduced by selectively programming '0' s into the bit locations. The only way to change a '0' to a '1' in cerdip EPROMS is by UV light erasure.

1.4 System Clock

The circuit uses a clock frequency of 5 MHz, since the 8088 is a chip operating at 5 MHz. Each instruction utilizes at least three clock cycles and the maximum depends on the type of operation performed. We use a 15 MHz crystal in the clock generation circuitry. This used along with the 8284 oscillator circuitry provides a precise 5 MHz signal output with the chip having a divide by three facility.

1.4.1. 8284 Clock Generator and Driver

The 8284 is a single chip clock generator which generates the system clock for the IAPX 88 microprocessor. The chip contains a crystal synchronization and reset logic. Refer to appendix for pin configuration. The oscillator circuit of the 8284 is designed with an external series resonant, fundamental mode, crystal from which the basic operating frequency is derived.

The crystal frequency should be selected at three times the required CPU clock. X_1 and X_2 are the two crystal input crystal connections. The clock generator consists of a synchronous divide by three counter with a special clear if input that inhibits the counting. The clock output is a 33% duty cycle mosclock driver designed to drive the IAPX 88 processor directly. The reset signal is synchronized to the falling edge of clk. The clock cycle period for this chip is about 125 ns.

CHAPTER - 2

ADC INTERFACE

2.1. Signal reception and Analysis

Any Analysis operation on random signals can be done only by storing the received signal and observation. With the advent of digital systems a microprocessor based reception and analysis has become very common. This essentially consists in converting the signal in to digital equivalent and input to the microprocessor for processing.

The system can be expanded by using a multichannel input by a multiplexer cum sample and hold set up. The microprocessor giving the command for a particular channel to be selected and issuing command to the ADC module to convert the input signal into a digital code. The output inturn is read by the processor. The above steps are performed repeatedly.

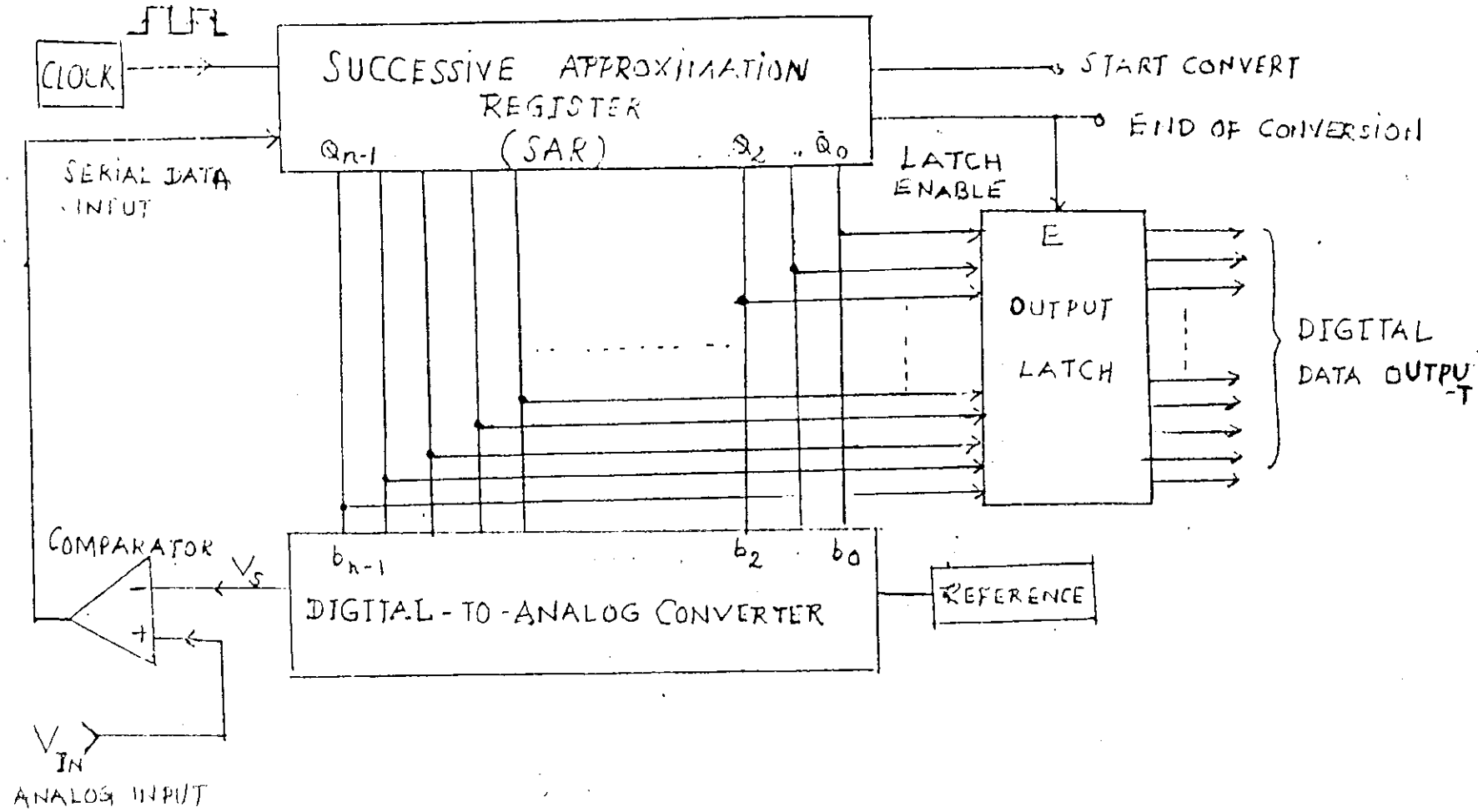
The data is read in discrete intervals known as sampling. The sampling frequency is related to the signal frequency and should be atleast twice the maximum frequency of signal.

2.2 Data Converters

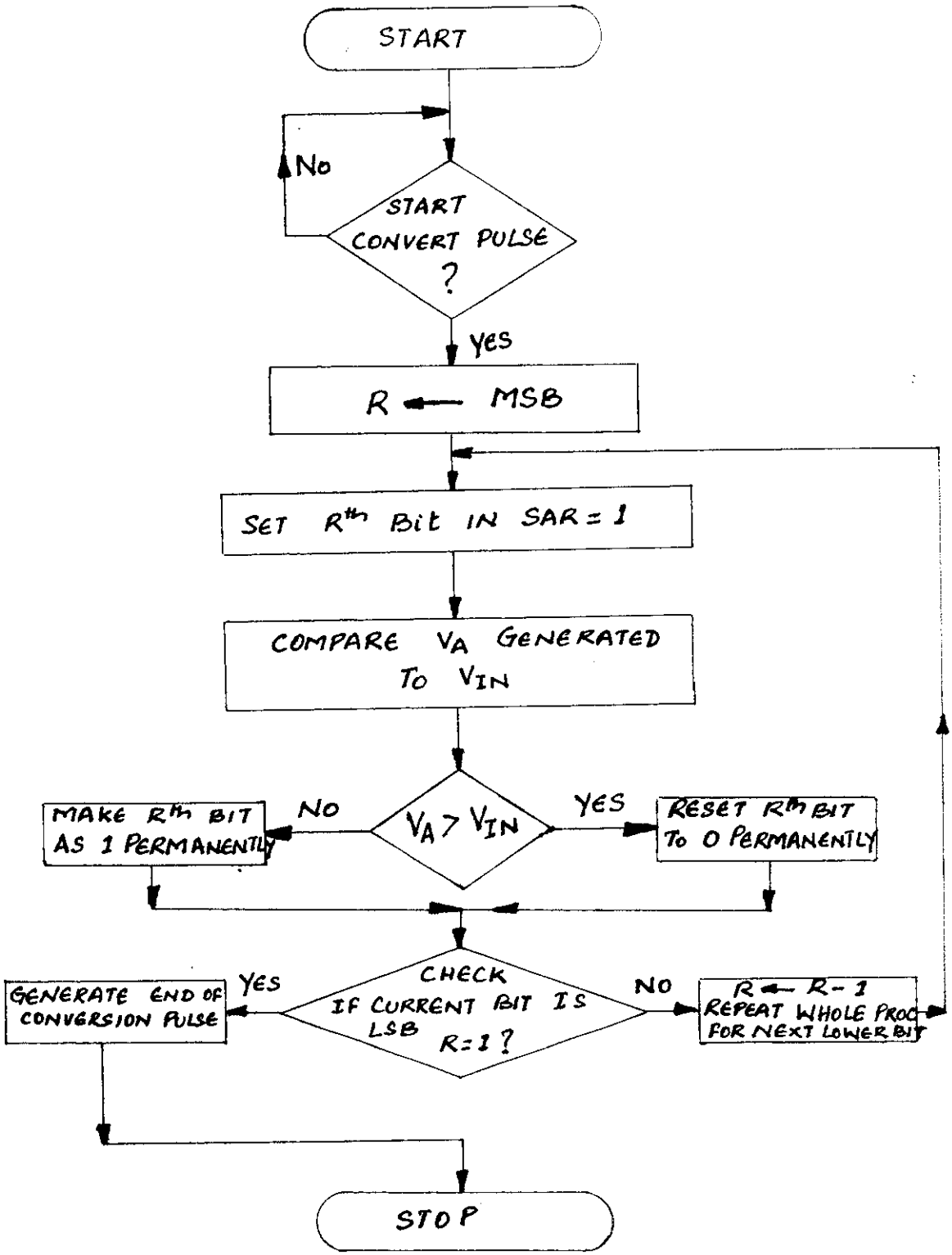
The analog signals from transducers are required to be digitised before entering into the processor. This necessitates the use of a converter. A typical Analog to digital converter converts an analog voltage to a digital output that best represents the input. The commonly employed technique for conversion is that the input signal is directly compared with a known reference signal.

A successive approximation type of ADC is better equipped for processor interfaces than any other type of ADC's. A successive approximation A/D converter as in fig1.1 Consists of a D/A converter with a precision voltage reference comparator,successive approximation register, clock and output latch.

The conversion takes place by successive comparison and approximation of binary output between the input signal and the reference signal. The input signal should in no case exceed the refence. The number of steps of comparison and approximation in this type of ADC is equal to the number of bits in the digital output. The flow chart of conversion is shown in fig2.2 The advantage of SA ADC is its high speed and excellent resolution. The main factors involved are conversion speed, accuracy and cost. The SA ADC features high speed. and the accuracy slightly decreases as the resolution increases.



2.1 SUCCESSIVE APPROXIMATION TYPE ADC



2.2 SUCCESSIVE APPROXIMATION METHOD

The AD574 is such a flexible and retiable converter having a very fast conversion rate, even faster than the process or itself that it can be used for receiving multichannel reception and continuously probing all the channels. The conversion is at such fast rate that the waveform received from each channel will not be distorted for a typical 16 channel multiplexing i.e. the time between the 1st sample of 1st channel signal and its second sample i.e. after the 1st samples of all other 15 channels are taken is still well within sampling theorem requirements that the received data will be of such clarity as to enable brief analysis of them.

AD 574 : CHIP CHS:

Interface Timing Adjustments:

The Chip has the following control signals whose signal requirements are to be precisely met for correct conversion.

(i) the $\overline{CS}$ signal which selects the card for conversion. This can be achieved by activating this by the address out of the 8088 (decoded)

(ii) The CE signal enables the chip and it should be enabled before the $\overline{CS}$ is done. This includes one less propagation delay and is a faster input.

(iii) A R/$\overline{C}$ signal which decides whether conversion process or data reading is going on. The signals RD and WR from the 8088 can be used to decide the process.

(iv) A 12/8 pin which decides weather a 12 bit conversion, an 8 bit conversion or 12 bit conversion with 8 bit output is going on.

(v) The pin A_0 along with R/C determines 2 byte reading of 12 bit conversion. By connecting this to A0 of μP this can be achieved by reading from successive addresses.

(vi) A STS signal which gives the E OC signal out and hence can be used to interrupt the processor.

All these signals need precise timing adjustments for perfect functioning and hence needs proper delays to be introduced and proper signals to be chosen for each and every pin. The operation of the ADC along with its turning diagrams are given in the appendix.

Such an interface along with a DAC and multichannel facility will serve as an excellent communication interface.

The circuit developed with all such facilities and proper printed circuit board layout was developed with theoretical analysis of the chip.

2.3 Microprocessor interface:

The data receiver card can be interfaced to the processor easily. The points to be considered in interfacing being a) the resolution (no.of bits) of the ADC is equal to the resolution of the processor data bus. b) the speed of operation and timings of the ADC coincide with the processor timings and speed. The operation can be a)synchronous: the processor executing the instruction for a time equal to the conversion time of the ADC b)Asynchronous: processor checking the part for End of conversion or c) in interrupt mode: The processor will then read the data from the ADC.

The throughput rate of an acquisition system is the number of samples/sec/channel, the system can handle. The above factor is important if one expands the system to a modified multichannel card with sample & hold circuitry.

The sequence of operation in a normal data receiving system are:

a) Sending command to the part for start command operation, by selecting the chip and switching the input signal ON.

b) The ADC goes into a conversion cycle. The address may be updated during conversion.

c) After conversion the data can be read through the data lines.

d) The above sequence is repeatedly executed for continuous data reception.

2.4 Why the microprocessor? - 8088

The Intel 8088 has the same Arithmetic Logic unit, the same registers and the same instruction set as 8086. The 8088 also has a 20 bit address bus, so that address as any one of the 1 Mb in memory. The 8088 has an 8 bit data bus so it can read or write 8 or 16 bits at a time. To read a 16-bit word from two successive memory locations, The 8088 will always have to do two read operations. The 8088 is more popular due to its simplified hardware while retaining the same power. The 8088 coupled with a numerical co-processor is capable of executing powerful floating point operations, many times faster than 8088 and is extremely useful in data processing. So, an ideal converter for an extremely fast processor is the AD574 which has a conversion time of 25 μs. This is a 12 bit A/D converter which has a built in zener reference. This chip is capable of accepting bipolar voltage ranges. The advantage of this chip is that the 12 bits of output data can be as one 12-bit A/D converter which has a built in zener reference. This chip is capable of accepting bipolar voltage ranges. The advantage of this chip is that the 12 bits of output data can be read as one 12-bit word or as two 8-bit bytes (one with 8 data bits, the other with 4 data bits and 4 trailing zeros. This chip operates on the successive approximation principle.

The design of an interface, a typical data acquisition load using AD 574 is an asset in itself in any high frequency signal reception, like, for e.g. extraterrestrial signal by use of antenna elements.

2.5 ADC Interface

The converter used is a CMOS 8 bit successive approximation type. The operational characteristics and interface design of the 0804 chip with the microprocessor is discussed here. The chip uses a differential potentiometric ladder. The inbuilt output latches drive the data bus of the processor. These A/D s appear like memory locations or I/o ports to the processor and no interfacing logic is needed. A new differential voltage allows increasing the common mode rejection and offsetting the analog zero input. In addition the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits resolution.

The chip exhibits an on chip clock generator. This has an easy interfacing facility with all microprocessors or it operates stand alone. The interfacing schematic is shown in appendix The design part of the interface is just an enhanced form of the block shown with various signal and voltage level adjustment.

The various step taken to the above effect include:

1) The conversion of Analog signal to digital is initiated by a CSsignal output to the card and writing to the port the channel to be selected if multiplexing is done. Once the conversion cycle is started the processor will go into its usual routine. Address of the channel can be any one of the address for which 1YO gets activated.

2) The device will be interupted by the ADC after conversion so the end of conversion is given to the INTR of system board

3) The data will be read after interrupt so the IORD is connected to the o/p latch enable (RO) of the 0804.

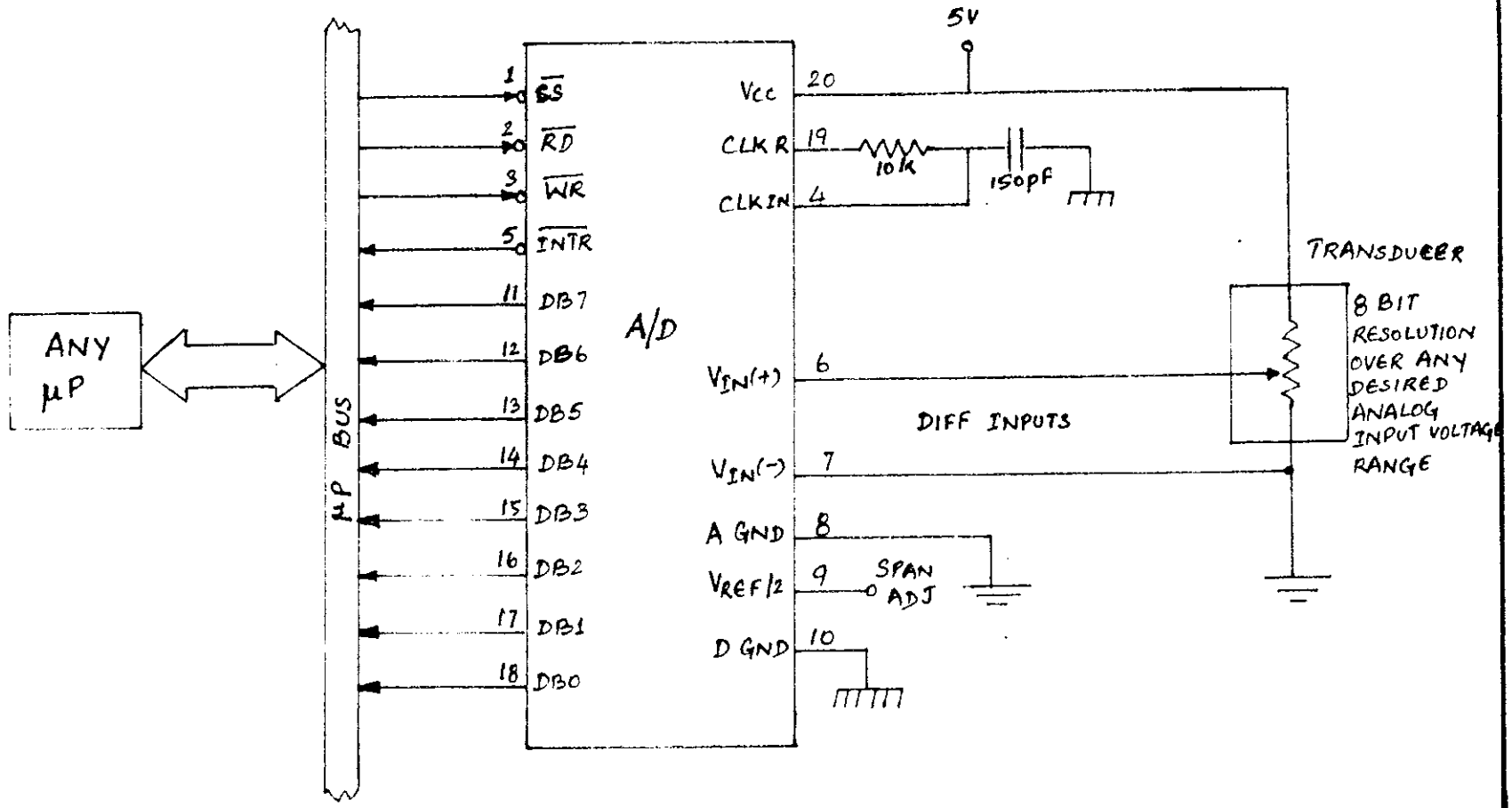
4) The 2 inputs vin (-) and vin (+) are combined through a resistive devider to provide a constant range of input in both +ve and -ve direction. A multiplexer may be used at the vin (+) if many data channels need to be interfaced, but for simplicity the option is left open.

5) The clock inside the chip itself is used as clock in the design.

6) The reference voltage is maintained precisely at 2.5v by a Zener voltage adjust. The Zener adjust does the Vcc to V ref conversion 4 maintains the Vref.

7) The data outputs are connected directly to the system data bus and output the data when the RD pin of the system goes low or when the processor is ready to receive the data.

The whole circuitry employing the above feautres is shown in fig2.3 The circuit board for the same was designed in smart & tested. The software for data reception is listed in the software section.



2.3 ADC INTERFACE CIRCUITARY

The data receiving operation is explained in brief as below:

1) The processor initiates a conversion cycle.

2) The device interrupts the processor after the conversion terminates.

3) The processor reads the data from the O/P latches of the ADC.

4) The processor starts the next conversion cycle and the above sequence is repeated until sufficient signal samples are taken.

The data stored is analysed using software instructions and feedback actions taken.

CHAPTER - 3

3.1 INTERRUPTS IN 8088

The 8088 has seven different interrupt types:

NMI, INTR, INTn, INT 3, INTO, Divide-by-0, Single-step, INTn, INTO, and the special single-byte INT3 breakpoint instruction are software interrupts placed as desired within a program. The divide-by-0 and single step interrupts are initiated by the CPU: the former if the quotient produced by a divide instruction exceeds the capacity of the destination register and the latter at the completion f each instruction if TF is set. The flow chart of the 8088's response to each of these types of interrupts in fig3 In all cases the current instruction is allowed to finish before the interrupt is processed. Interrupt interrupts (except single-step) have precedence or priority over simultaneous (with the same instruction) external interrupt requests. For example, if an interrupt request occurs on INTR, but the current instruction causes a divide-by-zero interrupt, the later will be serviced first. Similarly if simultaneous interrupts occur on INTR and NMI, NMI will be serviced first.

When the interrupt is serviced, the flags, CS and IP registers are pushed on the stack, saving the CPU's "place" in the memory. This means that six bytes will be pushed onto the stack. The TF status is saved so that the interrupted instruction will still be single-stepped (if TF is set). However, before executing the ISR, TF and IF are cleared, disabling INTR and the single-step mechanism within

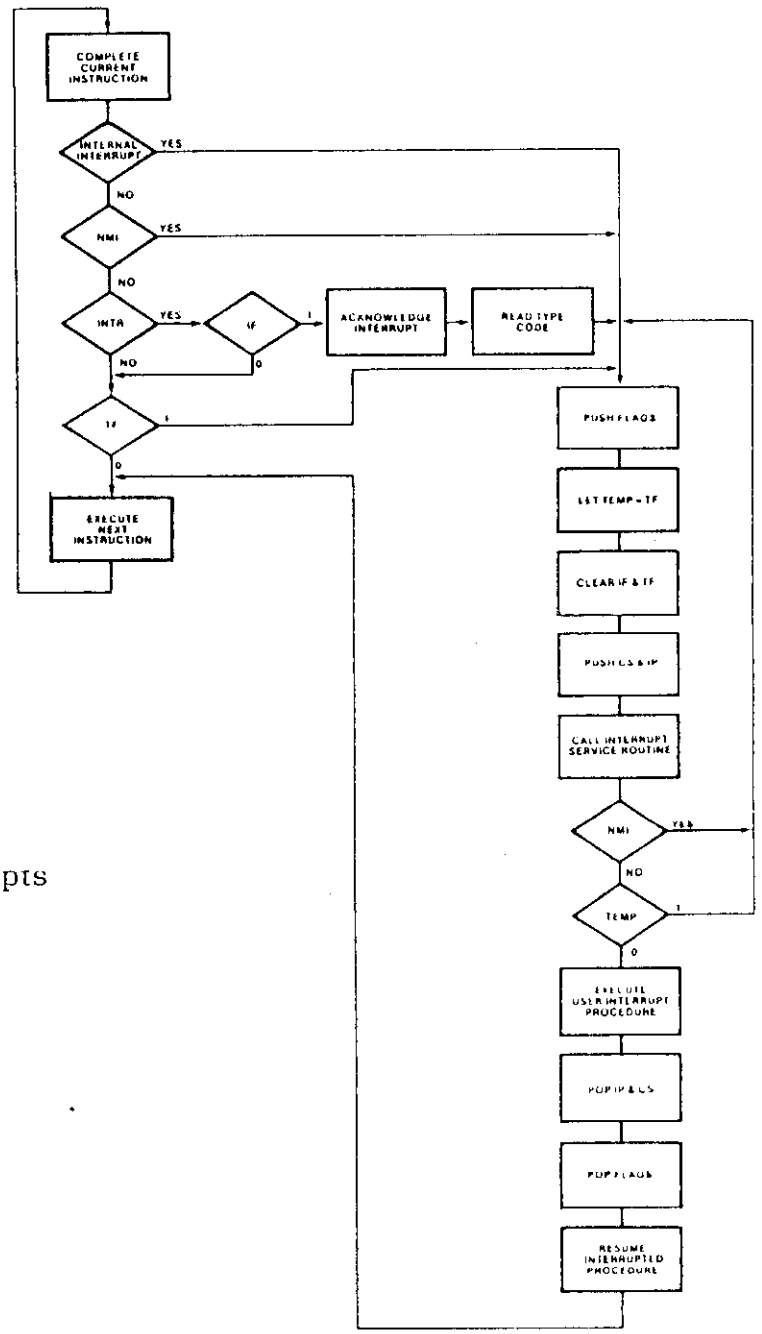


Fig.3

Flowchart for

types of interrupts

this routine. If desired, these flags can be set, enabling these interrupts. That is, the interrupts can be allowed to interrupt themselves.

If an internal interrupt is being serviced and an NMI (on INTR if IF is set) occurs, the ISR for the internal interrupt will be suspended and the external interrupt honored, even though it is of low priority. The priority structure applies to only simultaneous interrupt requests.

NMI is a non maskable interrupt which means that it cannot be blocked. INTR, on the other hand, is maskable via the IF flag. Only when this flag is set will interrupts on this live be accepted. Although internal interrupts have priority over external interrupts, the NMI I request will be honoured as the internal interrupt's ISR begins. This is not true for the INTR input however. This is because IF is cleared automatically when the internal interrupt is serviced.

As the NMI interrupt is non maskable, the NMI interrupt is reserved for catastrophic events such as memory error or an impending power failure.

The INT instruction causes the program to jump indirectly to the memory pointed by a vector in 00 to 03 pages. The INT instruction pushes on the stack the PC, CS and flags. An IRET instruction in the interrupt service routine will restore these, after returning from such an interrupt.

The pages 00 to 03, totally 1024 bytes, can contain 256 vector addresses (4 bytes/vector ; bytes for jump addresss ; 2 bytes for code segment). Thus 256 software interrupts are permissible.

However, some of the interrupt vectors are reserved for certain functions. For example, the first vector which is at 00 00 has;

00 00	Low address and	of interrupt service routine for
00 01	High address	overflow upon divisin (divide
00 02	Low part	by 0) of code segment in
00 03	High part	which you might have written a routine to be executed when DIV by 0 occurs.

Thus, the first software interrupt is reserved for taking suitable action whenever a divide-by-zero occurs. Hence, it is called a type-0 interrupt. It automatically occurs upon divisionally by zero.

04 00	MOV AX FF 10	B8 FF 10	Move AX with the value 10 FF (some number).
04 03	MOV CL_1 00	B1 00	Make the divisor purposely a zero.
04 05	DIV CL	F6 F1	Divide by CL (a zero)
04 07	MOV $LABEL_1$ AX	A3 00 05	Move quotient and remainder in 05 00 and 05 01.

04 0A	HLT	F4	

Also load the interrupt service routine (ISR) to take necessary action upon a division by zero occurring.

00 D0 00	00		Start address of division.
00 01	06		by-zero interrupt service routine.
00 02	00		Code segment value is 00 00
00 03	00		
06 00	MOV AL, EE	B0 EE	Move a flag EE in AL
06 02	OUT AL, 04	E6 04	Output the error flag on port-4
06 04	IRET	CF	Program returns.

Upon executing the division program at 04 00, the output in port-4 is EE, indicating that division by zero was attempted. No division is really performed.

3.1.1 Type-1 Interrupt (single step mode):

Type-1 software interrupt vector which is stored in 00 04 to 00 07 (program counter and code segment values as before) is to have an interrupt routine which enables debugging a program ins-

truction by instruction. This interrupt is maskable and will work only if the TF bit in the flag register is set. So, in order to do single stepping of instructions, one has to set the IF flag, write an interrupt service routine for debugging and load the addresses 00 04 to 00 07 with the address code segment values of this routine. For example,

04 00	PUSH F	9C	Push the flags on the stack
04 01	POP AX	58	Move the flags into AH & AL
04 02	OR AH, 01	80 CC 01	Set the 8th bit (0th bit in AH) to 1. This is for setting TF flag subsequently.
04 05	PUSH AX	50	Push this altered flag value on stack.
04 06	POP F	9D	Get the TF-set flags on to the flag register.
04 07	MOV AL, 02	B0 02	Here after the program which is to be single-stepped follows: Let AL = 02
04 09	P: INC AL	FE C0	Increment AL
04 0B	JMP P	EB FC	Jump to Loop.

After entering the above program, the interrupt vector as well as the service routine for single step are loaded (at 06 00).

00 04 00

00 05 00

00 06 00

00 07 00

06 00	OUT AL 04	E6 04	Output AL on port-4.
06 02	POP 00 05	8F 06 00	Pop the stack to get at the previous prog. ctr. value at some memory say 05 00.
06 06	PUSH 00 05	FF 36 00 05	Push it back again in place.
06 0A	PUSH AX	50	PUSH AX
06 0B	PUSH BX	53	Push BX
06 0C	MOV BX, 00 05	8B 1E 00 05	Move the contents of 05 00 05 00 (the previous prog. ctr.) into BX. So that the monitor software display can show it.
06 10	CALL KBD	9A 80 F2 00 00	Call monitor display prog.

06 15	POP BX	5B	Restore register sel
06 16	POP AX	58	
06 17	IRET	CF	Return from interrupt.

The program is executed at 04 00 as usual. The program advances step by step after reaching 04 09 address and the key board can be pressed (any her key) to step it. In this program, it jumps between the addresses 04 09, 04 0B (because it has a loop there).

3.1.2. Type-2-interrupt

The type-2 is a non-maskable interrupt which is got by a low to high pulse on NMI pin. It vectors to the address 08 on page 0.

CHAPTER - 4

SOFTWARE LISTINGS

4.1 Monitor Program and the use of the 8088 board developed.

The monitor program which is listed is written and developed on similar lines of the 8085 monitor. Upon RESET, the 8088 sets its CS register to FFFF and hence the program memory should be at the highest end of the one megabyte memory. As seen, we have left the addresses A_{16} - A_{19} addresses, the first F in the CS register is a 'don't care' digit for us. Hence, the EPROM (2732) is selected at FF FFO and thus the first jump instruction is placed at the last (Fth) page of the EPROM at FO. This is an intersegment jump which jumps to F500, i.e. to the 5th page of the 2732. The CS register is simultaneously made 00 00. Thus, all further program has identical values for CS, DS, ES, SS all of which are 00 00. The values of the segment register, not necessarily have only the values 00 00. They can be chosen and redefined by the user himself. The user memory RAM occupies the first 2K space (0000-07FF).

4.1.1 Sample Programs to illustrate the 8088 instructions.

a) Program to find the average of a number of bytes

Address			Code	Comments
0400		MOV S1, 0005	BE 00 05	SI points to 05 00 where the numbers are stored.
0403		MOV Cx, 0B 00	B9 0B 00	Cx stored with the number; (OB) bytes to be averaged.
0406		PUSH CX	51	Save CX register
0407	TOP:	ADD AL, (SI)	02 04	Add the first number with AL
0409		ADC AH, 00	80 D4 00	And then ADD carry into AH
040C		INC SI	46	Increment SI to get the next number.
040D		LOOP	E2 F8	Decrement CX and return to loop top if non-zero.
040F		POP CX	59	Restore original CX value.

0410	DIVCL	F6 F1	Divide AX by CL
0412	OUT AL, 04	E6 04	Output the averaged number of port 4.
0414	HLT	F4	

The numbers to be averaged are stored in 0500 onwards.

Address

05	00	01	02	03	04	05	06	07	08
	08	09	0A	0B					

Result: The number 66 is the average.

b) **BINARY MULTIPLICATION**

Address	Mnemonics	Code	Comments
0400	MOV AL, 08	B0 08	Multiplicand - 08 is in AL
0402	MOV CL, 05	B1 05	Multiplier - 05 is in CL.
0404	MUL CL	F6 E1	Multiply AL by CL contents
0406	MOV 05 00,	AX A3 00 05	Store result in 0500
0409	HLT	F4	

After executing the program, 05 00 contains 28. 0501 contains 00.

c) **DIVISION**

Binary division (byte division)

0400	MOV AX, FF 00	B8 FF 00	Dividend 00 FF is in AX.
0403	MOV CL, 10	B1 10	Divisor in CL register
0405	DIV CL	F6 F1	Now AX is divided by CL
0407	MOV 05 00, AX	A3 00 05	Move AX into C500, 0501
040A	HLT	F4	Halt

The result will be FF/10, which gives a quotient of OF and a remainder of OF. For division the quofient is in AL, remainder in AH.

d) STRING TRANSFER INSTRUCTION

1) Transfer one page of FF bytes.

0400	MOV SI, 05 00	BE 00 05	SI register points to source area 05 00
0403	MOV DI, 06 00	BF 00 06	DI register points to destination area.

0406	MOV CX, 00 FF	B9 FF 00	CS is stored with the number FF (a page)
0409	CLD	FC	Clear direction for auto increment in string instruction which follows.
040A	Pt.P: MOVS B	A4	Moves the contents of the SI pointer to DI.
040B	LOOP P	E2 FD	Development CX, return to top of loop if not zero.
04 0D	HLT F4	F4	Halt

The contents of 05 page in RAM would have got transferred into 06 page after this program is run.

String transfer and test while transfering:

0400	CLD	FC	Clear the direction flag.
0401	MOV SI, 0006	BE 00 06	SI points to a source string at 06 00

0404		MOV DI, 0005	BF 00 05	DI Pts to 05 00, the place where it is to be stored.
0407		MOV CX, FF 00	B9 FF 00	CS is stored with the code FF.
040A	P:	LODB	AC	The contents of SI area got into AL.
040B		STOB	AA	Then moved into DI area.
040C		TEST AL, FF	A8 FF	Test if Al = FF.
040E		LOOP NE, P	E2 FA	Loop until AL finds the code FF.
0410		HLT	F4	Halt

The program will duplicate the contents of 06 page into 05, until senses an FF in the former. In string transfer the destination index points to the extra segment memory. But, in the monitor program developed, all the segment registers are made 0000 and hence access within the same memory block.

4.2. ADC Program

This program illustrates that it accepts the 8-bit output from an Analog to Digital converter and scales it to a value between OV & 5V. The output is displayed on two seven segment displays as a units digit and a tenths digit.

```
=    ----    DPORT    EQU    ---H        ; Data in port,
=    ----    DSPY     EQU    ---H        ; Display port
=    0005    MPLR     EQU    5           ; Full scale = 5V
```

One byte of uninitalised storage is reqd. TEMP is defined in a segment called DATA.

```
0000              DATA        SEGMENT
0000 ??           TEMP        DB      ?     ; Unde fined
0001              DATA        ENDS
```

The program codes are stored in a segment called CODE. The Assume statement tells the assembler to use CODE for CS and DATA for DS. The SS and ES segment registers are not defined.

```
0000        CODE SEGMENT
                ASSUME CS:  CODE, DS-DATA
```

The operating system loads CS at run time but not DS. The next two instructions load DS with the DATA segment base address.

```
0000 B8 ---- R      START :  MOV AX, DATA ; Segment base
                             MOV DS, AX ; to DS
0003 8E D8
```

Get data from ADC & Form value between 0V & 5V

```
0005 E4 D6      AGAIN :  IN AL, DPORT ; GET Data
0007 B3 05               MOV BL, MPLR; Multiply times
0009 F6 E3               MUL BL       ; full scale
000B BA 0000             MOV DX, 0    ; Divide 32 bit
                                      ; Dividend in
                                      ; DX : AX
000E BB 0100             MOV  BX, 256 ; by 256 for an
0011 F7 F3               DIV BX       ; 8 bit ADC
```

Shift quotient four bits left so it will appear in the left most display.

```
0013 B1 04               MOV CL, 4    ; 4 shifts left
0015 D2 E0               SAL AL, CL   ;
0017 A2 0000R            MOV TEMP, AL; Save units digit
```

Fetch remainder and calculate tenths digit.

```
001A BA C2                  MOV AL, 0L   ; Reminder to A1
001C B3 0A                  MOV BL, 10   ; Multiplier
001E F6 E3                  MUL BL       ;
0020 BA 0000                MOV DX,  0   ; Do division
0023 BB 0100                MOV BX, 256  ; for the
0026 F7 F3                  DIV BX       ;  tenths digit
```

Check remainder, round tenths digit up & output result to the displays.

```
0028 80 FA 80               CMP DL, 128  ; Less than
002B 72 02                  JB SKIP      ; half?
002D FE C0                  INC AL       ; No
002F 27                     DAA          ; Keep decimal
0030 02 06 0000R  SKIP:     ADD AL,TEMP  ; form result
0033 E6 D4                  OUT DSPY, AL ; and show it
0035 EB CE                  JMP AGAIN    ; Repeat cycle
0037                CODE ENDS
                            END START
```

The flow chart for the ADC conversion is shown. The units digit is called X and the tenths digit is called Y. After inputting the digital word, the units digit is calculated using the formula as shown above.

We require a 16-bit divisor to divide the data by 256 and thus a 32-bit dividend in registers DX:AX.

The multiplication and division instructions can be performed on (a) 8-or (b) 16 bit register or memory source operates specific registers are dedicated to these functions as shown.

After the division X will be a number between 0 & 4. At this point Y represents the remainder of the division and could be any number between 0 & 255.

Because the units digit must appear in the left most display, it is shifted left four places (or multiplied by 16). The remainder is then multiplied by 10 and divided by 256 to calculate the tenths digit. If the remainder from this division is greater than 127, one is added to Y to round up one-tenth.

Finally, adding X and Y assembles the two-digit result and it can be output to the displays. The process is then repeated.

The assembly language listing for the program is also shown. The EQU statements are used to give names to constants & port addresses. After a value for X has been calculated, the result is temporarily stored until the tenths digit has been calculated. One byte in a (data) segment called DATA is used for this purpose. This segment is bracketed between the DATA SEGMENT and DATAENDS segment. All the segments must have an opening & closing statement like this or the assembler will issue an error message.

The program itself is stored in a segment called CODE. The ASSUME CS: CODE, DS: DATA Statement tells the assembler what to assume for the segment registers as it assembles the following instructions. This statment does not load the registers. The assume is required so that the assembler will know if it needs to generate far or near calls and jumps. It is also required to determine if a segment override is required.

The operating system will pick a value for CS based on available memory. The remaining segment registers must be loaded by the user.

There are two instructions beginning at the label START. The MOV AX, DATA instruction will cause the assembler to reserve two bytes of the MOV op-code for the segment address. Normally, this move instruction would load the contents of memory location DATA to AX. In this case, however, because DATA identifies a segment statement, the segment address is used. This can be seen in the left most column: B8.....R. The R means that this address is relative and cannot be determined at this time. When the program is linked and loaded, the actual segment address will be placed in these two bytes.

When the program is run, the data segment address will be loaded into AX and the next instruction will transfer this value to DS. The remainder of the program follows the flow chart.

4.3 8088 MONITOR PROGRAM LISTING

Address		Hex. Code						Mnemonics
HI	LOW							
FF	F0	EA	00	F5	00	00		JMP, BRANCH, SEGMENT
F5	00	BC	FF	07				MOV SP, DATA 16
F5	03	BB	00	04				MOV BX, 00 04
F5	06	8A	2F				Scan. 2	MOV CH, (BX)
F5	08	9A	80	F2	00	00	Scan. 1	CALL KBD
F5	0D	3C	40					CMP AL, 40
F5	0F	73	08					JNB To Pt. D
F5	11	B1	04					MOV CL, 04
F5	13	D2	E5					SAL CH, N
F5	17	EB	EF					JMP TO SCAN 1
F5	19	3C	42				Pt. D	CMP AL, 42
F5	18	75	04					JNZ To Pt. E
F5	1D	8A	DD					MOV BL, CH
F5	1F	EB	E5					JMP To SCAN 2
F5	21	3C	41				Pt. E	CMP AL, 41
F5	23	75	04					JNZ To Pt. F
F5	25	8A	FD					MOV BH, CH
F5	27	EB	DD					JMP To Scan 2
F5	29	3C	44				Pt. F	CMP AL, 44
F5	2B	75	03					JNZ Pt. P
F5	2D	4B						DEC BX
F5	2E	EB	D6					JMP To Scan. 2

F5	30	3C	47		Pt. P	CMP AL,47
F5	32	75	05			JNZ Pt. G
F5	34	88	2F			MOV (BX), CH
F5	36	43				INC BX
F5	37	EB	CC			JMP To Scan. 2
F5	39	3C	43		Pt. G	CMP AL, 43
F5	3B	75	C8			JMP To Scan. 2
F5	3D	A1	00	F6		MOV AX, 00 F6
F5	40	E7	01			OUT AX, PORT-01
F5	42	FF	E3			JMP BX

SOFTWARE DISPLAY ROUTINE:

F2	00	51			PUSH CS
F2	01	9C			PUSH F
F2	02	8A	C7		MOV AL, BH
F2	04	24	F0		AND AL, F0
F2	06	B1	04		MOV CL, 04
F2	08	D2	C8		ROR AL, N
F2	0A	8A	D0		MOV DL, AL
F2	0C	B0	7F		MOV AL, 7F
F2	0E	E6	01		OUT AL, 01
F2	10	E8	4D	00	CALL seg. display (F2 60)
F2	13	8A	C7		MOV AL, BH
F2	15	24	0F		AND AL, 0F

F2	17	8A	D0	MOV DL, AL
F2	19	B0	BF	MOV AL, BF
F2	1B	E6	01	OUT AL, 01
F2	1D	E8	40 00	CALL seg. display
F2	20	8A	C3	MOV AL, BL
F2	22	24	FO	AND AL, FO
F2	24	B1	O4	MOV CL,O4
F2	26	B2	C8	ROR AL,N
F2	28	8A	DO	MOV DL AL
F2	2A	BO	EF	MOV AL,EF
F2	2C	E6	O1	OUT A .O1
F2	2E	E8	2F .OO	CALL SEG. DISPLALY
F2	31	8A	C3	MOV AL,BL
F2	33	24	OF	AND AL,OF
F2	35	8A	DO	MOV DL,AL
F2	37	BO	F7	MOV AL,F7
F2	39	E6	O1	OUT AL,O1
F2	3B	E8	22 OO	CALL SEG. DISPLAY
F2	3E	8A	C5	MOV AL,CH
F2	40	24	FO	AND AL FO
F2	42	B1	O4	MOV EL,O4
F2	44	D2	C8	ROR AL N
F2	46	8A	DO	MOV DL AL
F2	48	BO	FD	MOV AL,FD

F2	4A	E6	01		OUT AL, 01
F2	4C	E8	11 00		CALL seg. display
F2	4F	8A	C5		MOV AL, CH
F2	51	24	0F		AND AL, CF
F2	53	8A	D0		MOV DL, AL
F2	55	B0	FE		MOVAL, FE
F2	57	E6	01		OUT AL, 01
F2	59	E8	04 00		CALL seg. display
F2	5C	9D			POPF
F2	5D	59			POPCX
F2	5E	CB			RET (inter-segment)

SEGMENT DISPLAY ROUTINE:

F2	60	B6	F2		MOV DH, F2
F2	62	B0	F0		MOVAL, F0
F2	64	0A	D0		OR DL, AL
F2	66	8B	F2	MOV S1. DX	MOV S1, DX
F2	68	8A	04		MOVAL, (S1)
F2	6A	E6	02		OUT AL, 02
F2	6A	E6	02		OUT AL, 02
F2	6C	BA	3F 00		MOV DX, 3F 00
F2	6F	4A		Pt. P;	DEC DX
F2	70	75	FD		JNZ disp 8 to. pt P

F2	72	B0	00	MOV AL, 00
F2	74	E6	02	OUT AL,02
F2	76	C3		RET (displacement based)

KEYBOARD SUBROUTINE;

F2	80	E4	02			KBD:IN	AL,O2
F2	82	0A	CO				ORAL,AL
F2	84	78	FA				JS disp 8 to KBD
F2	86	E8	36	00			CALL lime display (F2BF)
F2	89	E4	02			LOOP1:IN	AL,02
F2	8B	0A	CO				OR AL,AL
F2	8D	9A	00	F2	00 00		CALL software display
F2	92	79	F1				JNS TO LOOP 1
F2	94	E8	28	00			CALL TIME DELAY
F2	97	E4	02				IN AL 02
F2	99	OA	CO				OR AL,AL
F2	9B	79	EC				JNS,TO LOOP 1
F2	9D	34	CO				XOR AL,CO
F2	9F	24	4F				AND AL,4F
F2	A1	CB					RET(inter-segment)

TIME DELAY ROUTINE;

F2	BF	50			PUSHAX
F2	C0	9C			PUSHF
F2	C1	B8	FF	09	MOV AX,FF 09
F2	C4	48			PtA:DEC AX
F2	C5	75	FD		JNZ TO PT.A (disp 8)
F2	C7	9D			POPF
F2	C8	58			POP AX
F2	C9	C3			RET (displacement based)

LOOK UP TABLE FOR SEGMENTS;

F2	F0	7E	0
F2	F1	0C	1
F2	F2	B6	2
F2	F3	9E	3
F2	F4	CC	4
F2	F5	DA	5
F2	F6	FA	6
F2	F7	0E	7
F2	F8	FE	8
F2	F9	CE	9
F2	FA	EE	A

F2	FB	F8	B
F2	FC	72	C
F2	FD	BC	D
F2	FE	F6	E
F2	FF	E2	F

CHAPTER - 5

APPLICATIONS

5.1 APPLICATIONS

The discussions made earlier was on the implementation of the system logic and control software for signal reception. The signal itself is from some sensors and transducers which will constantly monitor the process variables of a physical system.

The above type of card can be used in a number of applications like measurement of physical variables for eg, temperature of ovens can be measured using a temperature sensor.

Pressure of small capacity boilers by use of a pressure sensor.

Motor speed, rotor position, displacement etc., can also be measured.

The system board itself can be used as a mini-processor system with proper keyboard and display connections. The PCB layout for the system board itself is done in such a way that it can go directly into a 8085 system ie. the 8085 main board can be replaced by this. The 8088 processor kit as such can be used to analyse a lot of software details including analog signal analysis, as in this case.

5.2. Scope for improvement:

The developed system can be improved to a microprocessor based data acquisition system which controls the physical variables of mechanical systems.

Such a facility can be extended by

1) including a keyboard and display interface for the main board.

2) A two way data card having a) A DAC b) A multiplexer for multichannel system c) A sample hold circuitry for updating of channels during conversion.

If all the above facilities are incorporated the system can be made to operate as a real time high precision control system.

5.3 Advantages

The development of a digital processor oriented data analyser provides a convenient, flexible and cost effective control of production in a factory. This lessons errors and decreases the time factor in the problems of machinery. This board with added facilities will be more helpful as an analyser of data since it uses a highly flexible microprocessor with auxilliary memory faciltiy. The ADC add on card developed provides an added dimension in that if provides faciltiy for real time monitoring and analysis of performance of physical systems.

CHAPTER - 6

FABRICATION

The circuits were designed as per procedure elaborated in the previous sections were tested individually and later fabricated.

The printed circuit board was made professionally in a copper clad hylam circuit board.

The necessary components for the boards were purchased. The components were soldered properly on the board. The monitor program in software sec. for the same is recorded in the EPROM with a Z-80 EPROM recorder.

CHAPTER - 7

CONCLUSION

The system board developed is designed so that it can directly replace the 8085 system boards. With the simple board and using the same I/O board cum hex keyboard, the powerful microprocessor instruction set can be practised for various application. The sample programs illustrated in the previous sections can be demonstrated by replacing the 8085 board with the 8088 system board developed.

The system board along with the signal receiver card can be used for control applications for monitoring parameters in industrial applications, where speed and accuracy are the key specifications.

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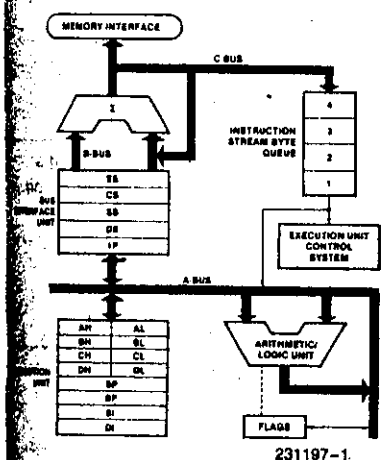
- Byron W. PUTMAN

80C88/80C88-2
8-BIT CHMOS MICROPROCESSOR

- **Pin-for-Pin and Functionally Compatible to Industry Standard HMOS 8088**
- **Direct Software Compatibility with 80C86, 8086, 8088**
- **Fully Static Design with Frequency Range from D.C. to:**
  - **— 5 MHz for 80C88**
  - **— 8 MHz for 80C88-2**
- **Low Power Operation**
  - **— Operating I_{CC} = 10 mA/MHz**
  - **— Standby I_{CCs} = 500 μA max**
- **Bus-Hold Circuitry Eliminates Pull-Up Resistors**
- **Direct Addressing Capability of 1 MByte of Memory**
- **Architecture Designed for Powerful Assembly Language and Efficient High Level Languages**
- **24 Operand Addressing Modes**
- **Byte, Word and Block Operations**
- **8 and 16-Bit Signed and Unsigned Arithmetic**
  - **— Binary or Decimal**
  - **— Multiply and Divide**
- **Will be Available in 40-Lead Plastic DIP and 44-Lead PLCC Packages**

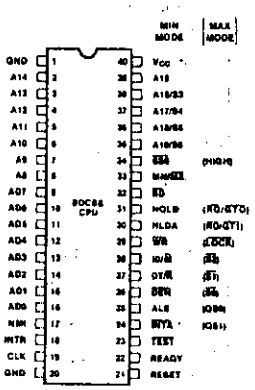
(See Packaging Spec., Order #231369)

The Intel 80C88 is a high performance, CHMOS version of the industry standard HMOS 8088 8-bit CPU. The processor has attributes of both 8 and 16-bit microprocessors. It is available in 5 MHz clock rate and will be available in 8 MHz clock rate in 1st half of 1986. The 80C88 offers two modes of operation: MINimum for small systems and MAXimum for larger applications such as multi-processing. It is available in 40-pin DIP and will be available in 44-pin plastic leaded chip carrier (PLCC) package in 1st quarter of 1986.



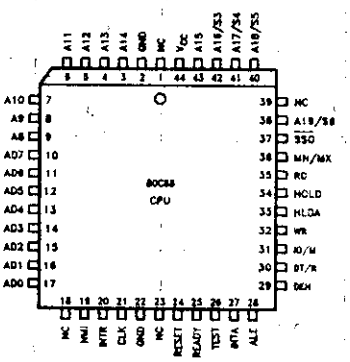
231197-1

Figure 1. iAPX 80C88 CPU Functional Block Diagram



231197-2

Figure 2a. 80C88 40-Lead DIP Configuration



231197-3

Figure 2b. 80C88 44-Lead PLCC Configuration

Order Number: 231197-002

Table 1. Pin Description

The following pin function descriptions are for 80C88 systems in either minimum or maximum mode. Th "local bus" in these descriptions is the direct multiplexed bus interface connection to the 80C88 (witho regard to additional bus buffers).

Symbol	Pin No.	Type	Name and Function
AD7–AD0	9–16	I/O	**ADDRESS DATA BUS:** These lines constitute the time multiplexed memory/IO address (T1) and data (T2, T3, Tw, and T4) bus. These lines are active HIGH and float to 3-state OFF(1) during interrupt acknowledge and local bus "hold acknowledge".
A15–A8	2–8, 39	O	**ADDRESS BUS:** These lines provide address bits 8 through 15 for the entire bus cycle (T1–T4). These lines do not have to be latched by ALE to remain valid. A15–A8 are active HIGH and float to 3-state OFF(1) during interrupt acknowledge and local bus "hold acknowledge".
A19/S6, A18/S5, A17/S4, A16/S3	35–38	O	**ADDRESS/STATUS:** During T1, these are the four most significant address lines for memory operations. During I/O operations, these lines are LOW. During memory and I/O operations, status information is available on these lines during T2, T3, Tw, and T4. S6 is always low. The status of the interrupt enable flag bit (S5) is updated at the beginning of each clock cycle. S4 and S3 are encoded as shown. This information indicates which segment register is presently being used for data accessing. These lines float to 3-state OFF(1) during local bus "hold acknowledge".

S4	S3	CHARACTERISTICS
0(LOW)	0	Alternate Data
0	1	Stack
1(HIGH)	0	Code or None
1	1	Data
S6 is 0(LOW)		

$\overline{RD}$	32	O	**READ:** Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the IO/$\overline{M}$ pin or S2. This signal is used to read devices which reside on the 80C88 local bus. $\overline{RD}$ is active LOW during T2, T3 and Tw of any read cycle, and is guaranteed to remain HIGH in T2 until the 80C88 local bus has floated. This signal floats to 3-state OFF(1) in "hold acknowledge".
READY	22	I	**READY:** is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The RDY signal from memory or I/O is synchronized by the 82C84A clock generator to form READY. This signal is active HIGH. The 80C88 READY input is not synchronized. Correct operation is not guaranteed if the set up and hold times are not met.

Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
INTR	18	I	**INTERRUPT REQUEST:** is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.
$\overline{TEST}$	23	I	**$\overline{TEST}$:** input is examined by the "wait for test" instruction. If the $\overline{TEST}$ input is LOW, execution continues, otherwise the processor waits in an "idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.
NMI	17	I	**NON-MASKABLE INTERRUPT:** is an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
RESET	21	I	**RESET:** causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution, as described in the instruction set description, when RESET returns LOW. RESET is internally synchronized.
CLK	19	I	**CLOCK:** provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
V_{CC}	40		**V_{CC}:** is the +5V ±10% power supply pin.
GND	1, 20		**GND:** are the ground pins. Both must be connected.
MN/$\overline{MX}$	33	I	**MINIMUM/MAXIMUM:** indicates what mode the processor is to operate in. The two modes are discussed in the following sections.

The following pin function descriptions are for the 80C88 minimum mode (i.e., MN/MX = V_{CC}). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described above.

IO/$\overline{M}$	28	O	**STATUS LINE:** is an inverted maximum mode $\overline{S2}$. It is used to distinguish a memory access from an I/O access. IO/$\overline{M}$ becomes valid in the T4 preceding a bus cycle and remains valid until the final T4 of the cycle (I/O = HIGH, M = LOW). IO/$\overline{M}$ floats to 3-state OFF(1) in local bus "hold acknowledge".
$\overline{WR}$	29	O	**WRITE:** strobe indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the IO/$\overline{M}$ signal. WR is active for T2, T3, and Tw of any write cycle. It is active LOW, and floats to 3-state OFF(1) in local bus "hold acknowledge".
$\overline{INTA}$	24	O	**INTA:** is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T2, T3, and Tw of each interrupt acknowledge cycle.

Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
ALE	25	O	**ADDRESS LATCH ENABLE:** is provided by the processor to latch the address into an address latch. It is a HIGH pulse active during clock low of T1 of any bus cycle. Note that ALE is never floated.
DT/$\overline{R}$	27	O	**DATA TRANSMIT/RECEIVE:** is needed in a minimum system that desires to use a data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically, DT/$\overline{R}$ is equivalent to $\overline{S1}$ in the maximum mode, and its timing is the same as for IO/$\overline{M}$ (T = HIGH, R = LOW). This signal floats to 3-state OFF(1) in local "hold acknowledge".
$\overline{DEN}$	26	O	**DATA ENABLE:** is provided as an output enable for the transceiver in a minimum system which uses the transceiver. $\overline{DEN}$ is active LOW during each memory and I/O access, and for $\overline{INTA}$ cycles. For a read or $\overline{INTA}$ cycle, it is active from the middle of T2 until the middle of T4, while for a write cycle, it is active from the beginning of T2 until the middle of T4. $\overline{DEN}$ floats to 3-state OFF(1) during local bus "hold acknowledge".
HOLD, HLDA	30, 31	I, O	**HOLD:** indicates that another master is requesting a local bus "hold". To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" request will issue HLDA (HIGH) as an acknowledgement, in the middle of a T4 or T1 clock cycle. Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor lowers HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. Hold is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the set up time.
$\overline{SSO}$	34	O	**STATUS LINE:** is logically equivalent to $\overline{S0}$ in the maximum mode. The combination of $\overline{SSO}$, IO/$\overline{M}$ and DT/$\overline{R}$ allows the system to completely decode the current bus cycle status.

IO/$\overline{M}$	DT/$\overline{R}$	$\overline{SSO}$	CHARACTERISTICS
1(HIGH)	0	0	Interrupt Acknowledge
1	0	1	Read I/O port
1	1	0	Write I/O port
1	1	1	Halt
0(LOW)	0	0	Code access
0	0	1	Read memory
0	1	0	Write memory
0	1	1	Passive

Table 1. Pin Description (Continued)

The following pin function descriptions are for the 80C88/82C88 system in maximum mode (i.e., MN/MX = GND.) Only the pin functions which are unique to maximum mode are described; all other pin functions are as described above.

Symbol	Pin No.	Type	Name and Function
$\overline{S2}$, $\overline{S1}$, $\overline{S0}$	26–28	O	**STATUS:** is active during clock high of T4, T1, and T2, and is returned to the passive state (1,1,1) during T3 or during Tw when READY is HIGH. This status is used by the 82C88 bus controller to generate all memory and I/O access control signals. Any change by $\overline{S2}$, $\overline{S1}$, or $\overline{S0}$ during T4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T3 or Tw is used to indicate the end of a bus cycle. These signals float to 3-state OFF(1) during "hold acknowledge". During the first clock cycle after RESET becomes active, these signals are active HIGH. After this first clock, they float to 3-state OFF.

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	CHARACTERISTICS
0(LOW)	0	0	Interrupt Acknowledge
0	0	1	Read I/O port
0	1	0	Write I/O port
0	1	1	Halt
1(HIGH)	0	0	Code access
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Passive

$\overline{RQ}/\overline{GT0}$, $\overline{RQ}/\overline{GT1}$	30, 31	I/O	**REQUEST/GRANT:** pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with $\overline{RQ}/\overline{GT0}$ having higher priority than $\overline{RQ}/\overline{GT1}$. $\overline{RQ}/\overline{GT}$ has an internal pull-up resistor, so may be left unconnected. The request/grant sequence is as follows (see timing diagram): 1. A pulse of one CLK wide from another local bus master indicates a local bus request ("hold") to the 80C88 (pulse 1). 2. During a T4 or T1 clock cycle, a pulse one clock wide from the 80C88 to the requesting master (pulse 2), indicates that the 80C88 has allowed the local bus to float and that it will enter the "hold acknowledge" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "hold acknowledge". The same rules as for HOLD/HOLDA apply as for when the bus is released. 3. A pulse one CLK wide from the requesting master indicates to the 80C88 (pulse 3) that the "hold" request is about to end and that the 80C88 can reclaim the local bus at the next CLK. The CPU then enters T4.

Table 1. Pin Descriptions (Continued)

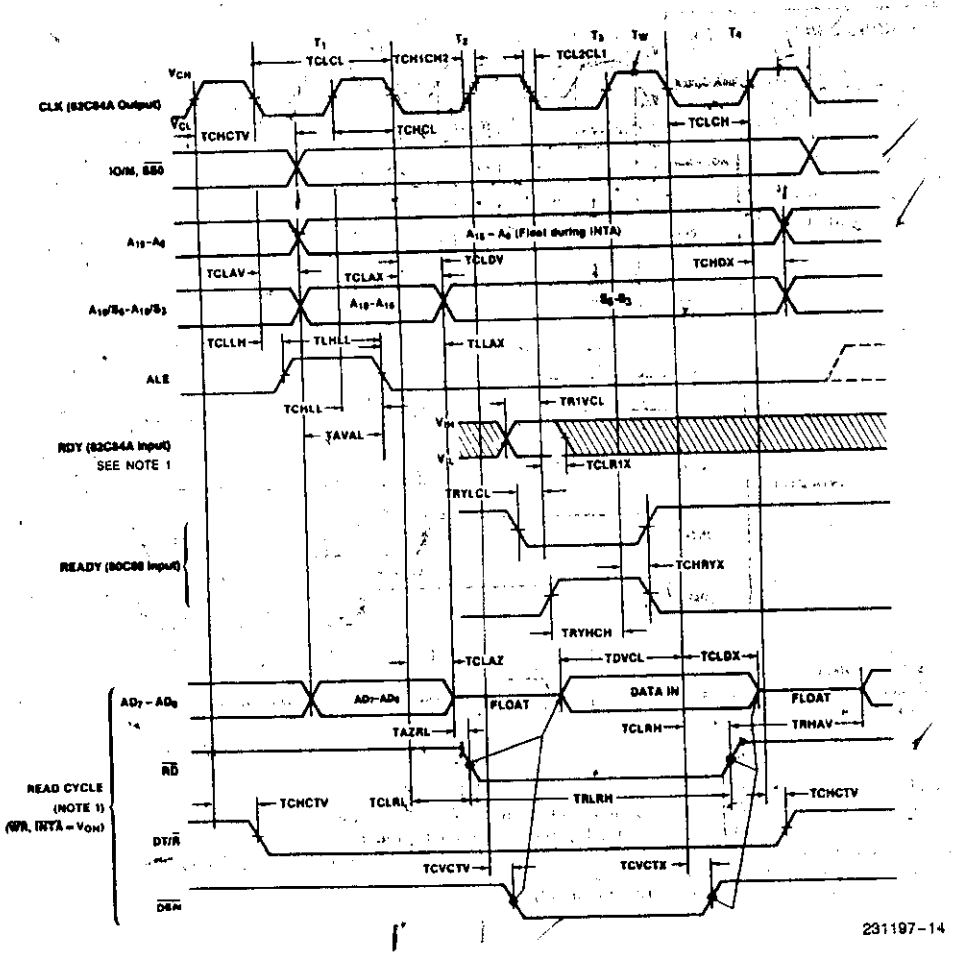
Symbol	Pin No.	Type	Name and Function
$\overline{RQ}/\overline{GT0}$, $\overline{RQ}/\overline{GT1}$	30, 31	I/O	Each master-master exchange of the local bus is a sequence of three pulses. There must be one idle CLK cycle after each bus exchange. Pulses are active LOW. If the request is made while the CPU is performing a memory cycle, it will release the local bus during T4 of the cycle when all the following conditions are met: 1. Request occurs on or before T2. 2. Current cycle is not the low bit of a word. 3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence. 4. A locked instruction is not currently executing. If the local bus is idle when the request is made the two possible events will follow: 1. Local bus will be released during the next clock. 2. A memory cycle will start within 3 clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.
$\overline{LOCK}$	29	O	**$\overline{LOCK}$:** indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active (LOW). The $\overline{LOCK}$ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and floats to 3-state OFF(1) in "hold acknowledge".
QS1, QS0	24, 25	O	**QUEUE STATUS:** provide status to allow external tracking of the internal 80C88 instruction queue. The queue status is valid during the CLK cycle after which the queue operation is performed.
—	34	O	Pin 34 is always high in the maximum mode.

QS1	QS0	CHARACTERISTICS
0(LOW)	0	No operation
0	1	First byte of opcode from queue
1(HIGH)	0	Empty the queue
1	1	Subsequent byte from queue

NOTE:
1. See the section on Bus Hold Circuitry.

WAVEFORMS

BUS TIMING — MINIMUM MODE SYSTEM



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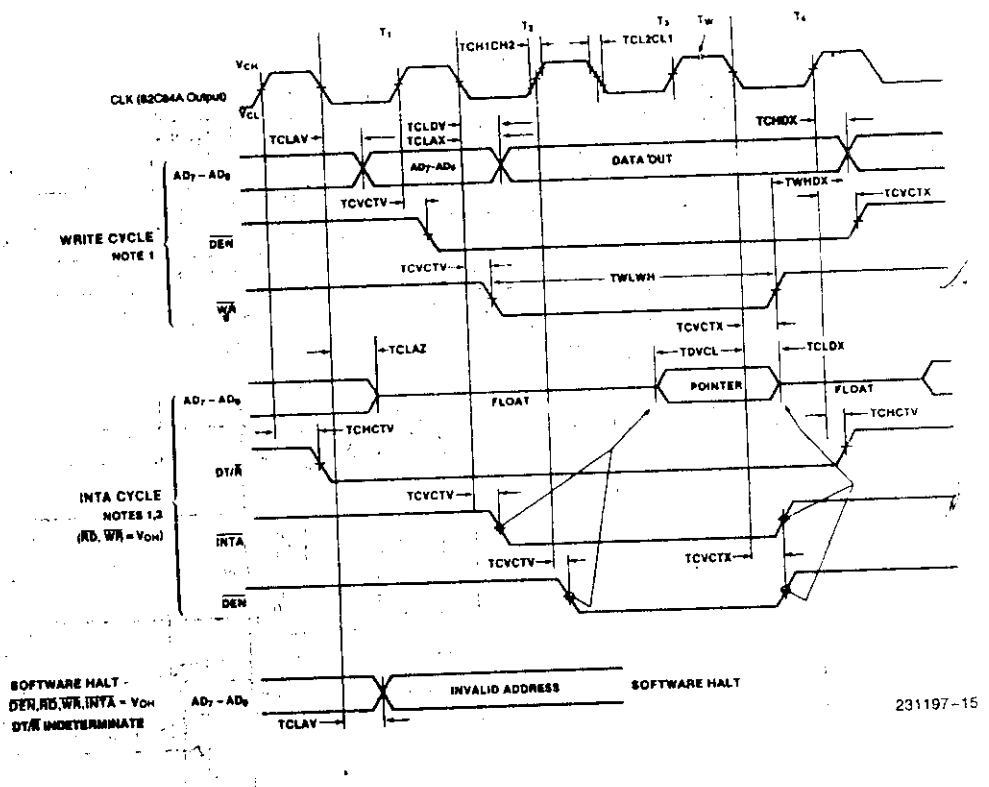
WAVEFORMS (Continued)

BUS TIMING — MINIMUM MODE SYSTEM (Continued)



NOTES:
1. All output timing measurements are made at 0.8V and 2.0V unless otherwise noted.
2. RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted.
3. Two INTA Cycles run back-to-back. The 80C88 local ADDR/Data bus is floating during both INTA Cycles. Control signals are shown for the second INTA cycle.
4. Signals at 82C84A are shown for reference only.

A.C. CHARACTERISTICS (80C88: T_A = 0°C to 70°C, V_{CC} = 5V ±10%)
(80C88-2: T_A = 0°C to 70°C, V_{CC} = 5V ±5%)

MINIMUM COMPLEXITY SYSTEM TIMING REQUIREMENTS

		80C88		80C88-2			
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Test Conditions**
TCLCL	CLK Cycle Period	200	D.C.	125	D.C.	ns	
TCLCH	CLK Low Time	118		68		ns	
TCHCL	CLK High Time	69		44		ns	
TCH1CH2	CLK Rise Time		10		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		20		ns	
TCLDX	Data in Hold Time	10		10		ns	
TR1VCL	RDY Setup Time into 82C84A (Notes 1, 2)	35		35		ns	
TCLR1X	RDY Hold Time into 82C84A (Notes 1, 2)	0		0		ns	
TRYHCH	READY Setup Time into 80C88	118		68		ns	CL = 20−100 pF
TCHRYX	READY Hold Time into 80C88	30		20		ns	
TRYLCL	READY Inactive to CLK (Note 3)	−8		−8		ns	
THVCH	HOLD Setup Time	35		20		ns	
TINVCH	INTR, NMI, $\overline{\text{TEST}}$ Setup Time (Note 2)	30		15		ns	
TILIH	Input Rise Time (Except CLK) (Note 4)		15		15	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK) (Note 4)		15		15	ns	From 2.0V to 0.8V

NOTES:
1. Signal at 82C84A or 82C88 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T2 state (8 ns into T3 state).
4. Characterization only.

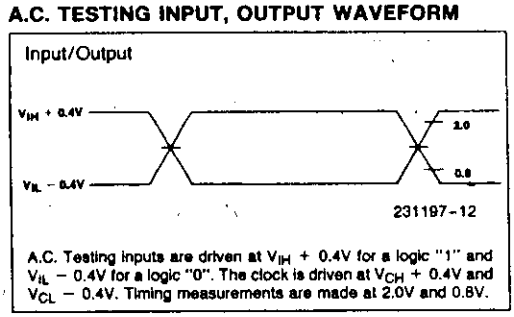
A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES

		80C88		80C88-2			
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Test Conditions**
TCLAV	Address Valid Delay	10	110	10	60	ns	C_L = 20–100 pF for all 80C88 Outputs in addition to internal loads
TCLAX	Address Hold Time	10		10		ns	
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50	ns	
TLHLL	ALE Width	TCLCH–20		TCLCH–10		ns	
TCLLH	ALE Active Delay		80		50	ns	
TCHLL	ALE Inactive Delay		85		55	ns	
TLLAX	Address Hold Time to ALE Inactive	TCHCL–25		TCHCL–25		ns	
TCLDV	Data Valid Delay	10	110	10	60	ns	
TCHDX	Data Hold Time	10		10		ns	
TWHDX	Data Hold Time After $\overline{WR}$	TCLCH–30		TCLCH–30		ns	
TCVCTV	Control Active Delay 1	10	110	10	70	ns	
TCHCTV	Control Active Delay 2	10	110	10	60	ns	
TCVCTX	Control Inactive Delay	10	110	10	70	ns	
TAZRL	Address Float to READ Active	0		0		ns	
TCLRL	$\overline{RD}$ Active Delay	10	165	10	100	ns	
TCLRH	$\overline{RD}$ Inactive Delay	10	150	10	80	ns	
TRHAV	$\overline{RD}$ Inactive to Next Address Active	TCLCL–45		TCLCL–40		ns	
TCLHAV	HLDA Valid Delay	10	160	10	100	ns	
TRLRH	$\overline{RD}$ Width	2TCLCL–75		2TCLCL–50		ns	
TWLWH	$\overline{WR}$ Width	2TCLCL–60		2TCLCL–40		ns	
TAVAL	Address Valid to ALE Low	TCLCH–60		TCLCH–40		ns	
TOLOH	Output Rise Time (Note 1)		15		15	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time (Note 1)		15		15	ns	From 2.0V to 0.8V

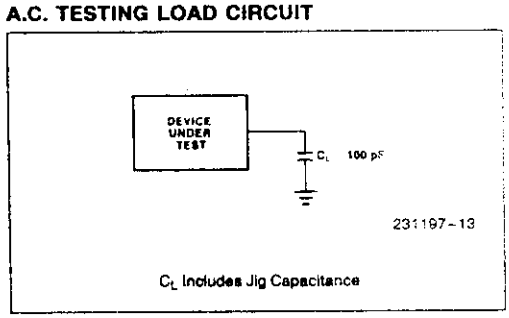
NOTE:
1. Characterization only.

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. Testing inputs are driven at V_{IH} + 0.4V for a logic "1" and V_{IL} – 0.4V for a logic "0". The clock is driven at V_{CH} + 0.4V and V_{CL} – 0.4V. Timing measurements are made at 2.0V and 0.8V.

A.C. TESTING LOAD CIRCUIT



C_L Includes Jig Capacitance

2732A
32K (4K x 8) PRODUCTION AND UV ERASABLE PROMS

- **200 ns (2732A-2) Maximum Access Time ... HMOS*-E Technology**
- **Compatible with High-Speed Microcontrollers and Microprocessors ... Zero WAIT State**
- **Two Line Control**
- **10% V_{CC} Tolerance Available**
- **Low Current Requirement**
  —100 mA Active
  —35 mA Standby
- **Int$_e$ligent Identifier™ Mode**
  —Automatic Programming Operation
- **Industry Standard Pinout ... JEDEC Approved 24 Pin Ceramic and Plastic Package**

(See Packaging Spec. Order #221369)

The Intel 2732A is a 5V-only, 32,768-bit ultraviolet erasable (cerdip) Electrically Programmable Read-Only Memory (EPROM). The standard 2732A access time is 250 ns with speed selection (2732A-2) available at 200 ns. The access time is compatible with high performance microprocessors such as the 8 MHz iAPX 186. In these systems, the 2732A allows the microprocessor to operate without the addition of WAIT states.

The 2732A is currently available in two different package types. Cerdip packages provide flexibility in prototyping and R & D environments where reprogrammability is required. Plastic DIP EPROMs provide optimum cost effectiveness in production environments. Inventoried in the unprogrammed state, the P2732A is programmed quickly and efficiently when the need to change code arises. Costs incurred for new ROM masks or obsoleted ROM inventories are avoided. The tight package dimensional controls, inherent non-erasability, and high reliability of the P2732A make it the ideal component for these production applications.

An important 2732A feature is Output Enable ($\overline{OE}$) which is separate from the Chip Enable ($\overline{CE}$) control. The $\overline{OE}$ control eliminates bus contention in microprocessor systems. The $\overline{CE}$ is used by the 2732A to place it in a standby mode ($\overline{CE}$ = V_{IH}) which reduces power consumption without increasing access time. The standby mode reduces the current requirement by 65%; the maximum active current is reduced from 100 mA to a standby current of 35 mA.

*HMOS is a patented process of Intel Corporation.

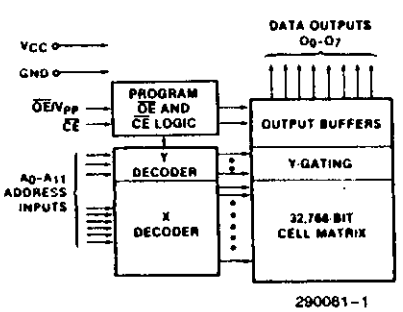
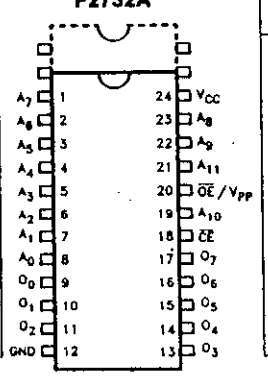


Figure 1. Block Diagram

Pin Names

A_0–A_{11}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable/V_{PP}
O_0–O_7	Outputs

27128 27128A	2764 2764A 27C64 87C64	2716
V_{PP}	V_{PP}	
A_{12}	A_{12}	
A_7	A_7	A_7
A_6	A_6	A_6
A_5	A_5	A_5
A_4	A_4	A_4
A_3	A_3	A_3
A_2	A_2	A_2
A_1	A_1	A_1
A_0	A_0	A_0
O_0	O_0	O_0
O_1	O_1	O_1
O_2	O_2	O_2
GND	GND	GND



2716	2764 2764A 27C64 87C64	27128 27128A
	V_{CC} PGM	V_{CC} PGM
V_{CC}	N.C.	A_{13}
A_8	A_8	A_8
A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$ ALE/$\overline{DE}$	$\overline{CE}$
O_7	O_7	O_7
O_6	O_6	O_6
O_5	O_5	O_5
O_4	O_4	O_4
O_3	O_3	O_3

290081-2

NOTE:
Intel "Universal Site" compatible EPROM configurations are shown in the blocks adjacent to the 2732A pins.

Figure 2. Cerdip/Plastic DIP Pin Configuration

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

READ OPERATION

D.C. CHARACTERISTICS

Electrical Parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for:

Symbol	Parameter	TD2732A LD2732A		Test Conditions
		Min	Max	
I_{SB}	V_{CC} Standby Current (mA)		45	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC_1}(1)	V_{CC} Active Current (mA)		150	$\overline{OE} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature (mA)		125	$\overline{OE} = \overline{CE} = V_{IL}$, $V_{PP} = V_{CC}$, $T_{Ambient} = 85°C$

NOTE:
1. Maximum current value is with outputs O_0 to O_7 unloaded.

EXPRESS EPROM PRODUCT FAMILY

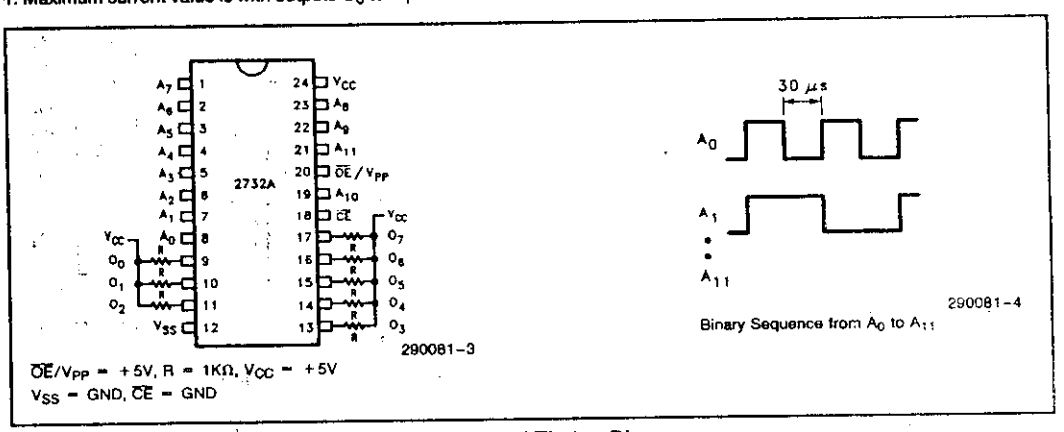
PRODUCT DEFINITONS

Type	Operating Temperature	Burn-In 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

2732A Versions

Packaging Options		
Speed Versions	Cerdip	Plastic
−2	Q	
STD	Q, T, L	
−3	Q	
−4	Q, T, L	
−20	Q	
−25	Q, T, L	
−30	Q	
−45	Q, T, L	



Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temp. During Read .....0°C to +70°C
Temperature Under Bias .....−10°C to +80°C
Storage Temperature .....−65°C to +125°C
All Input or Output Voltages with Respect to Ground.....−0.3V to +6V
Voltage on A9 with Respect to Ground.....−0.3V to +13.5V
V_{PP} Supply Voltage with Respect to Ground During Programming .....−0.3V to +22V
V_{CC} Supply Voltage with Respect to Ground .....−0.3V to +7.0V

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

READ OPERATION

D.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ(3)	Max		
I_{LI}	Input Load Current			10	µA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current			10	µA	$V_{OUT} = 5.5V$
I_{SB}(2)	V_{CC} Current (Standby)			35	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC1}(2)	V_{CC} Current (Active)			100	mA	$\overline{OE} = \overline{CE} = V_{IL}$
V_{IL}	Input Low Voltage	−0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ µA

A.C. CHARACTERISTICS $0°C \le T_A \le 70°C$

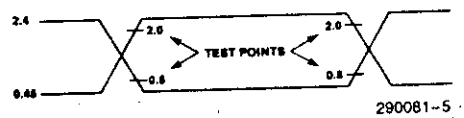
Versions	$V_{CC} \pm 5\%$	2732A-2 P2732A-2		2732A P2732A		2732A-3 P2732A-3		2732A-4 P2732A-4		Units	Test Conditions
	$V_{CC} \pm 10\%$	2732A-20		2732A-25		2732A-30		2732A-45			
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max		
t_{ACC}	Address to Output Delay		200		250		300		450	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		200		250		300		450	ns	$\overline{OE} = V_{IL}$
t_{OE}	$\overline{OE}/V_{PP}$ to Output Delay		70		100		150		150	ns	$\overline{CE} = V_{IL}$
t_{DF}(4)	$\overline{OE}/V_{PP}$ High to Output Float	0	60	0	60	0	130	0	130	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}/V_{PP}$, Whichever Occurred First	0		0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

NOTES:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. The maximum current value is with outputs O_0 to O_7 unloaded.
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.

CAPACITANCE [2] T_A = 25°C, f = 1 MHz

Symbol	Parameter	Typ	Max	Unit	Conditions
C_{IN1}	Input Capacitance Except $\overline{OE}/V_{PP}$	4	6	pF	V_{IN} = 0V
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance		20	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

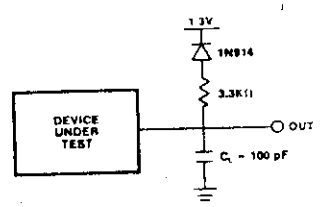
A.C. TESTING INPUT/OUTPUT WAVEFORM



290081-5

A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

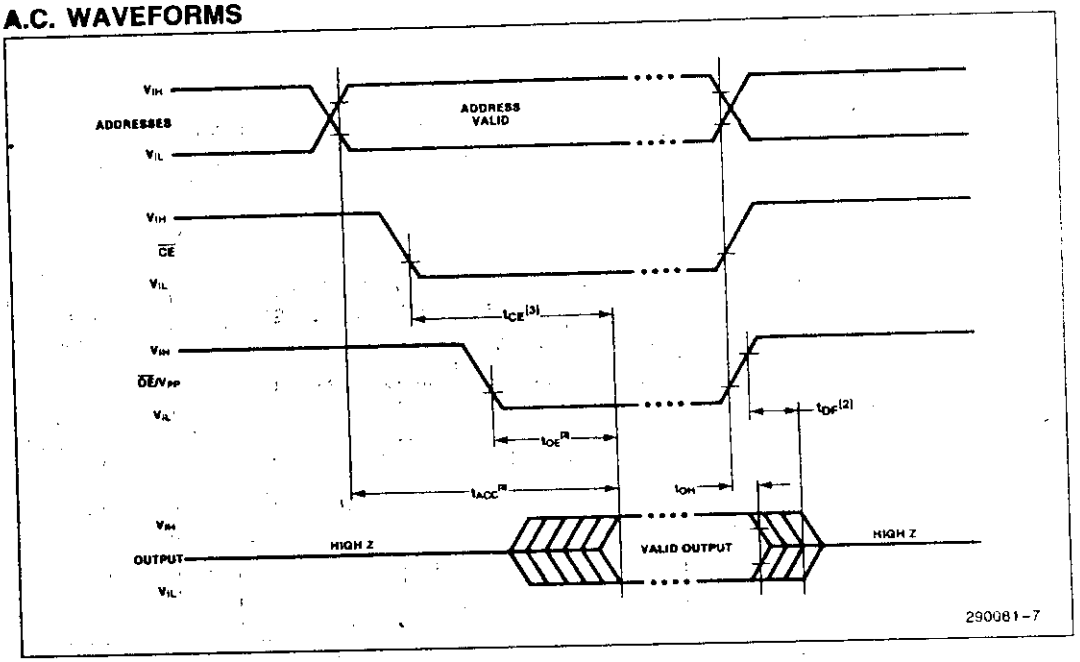
A.C. TESTING LOAD CIRCUIT



290081-6

C_L = 100 pF
C_L Includes Jig Capacitance

A.C. WAVEFORMS

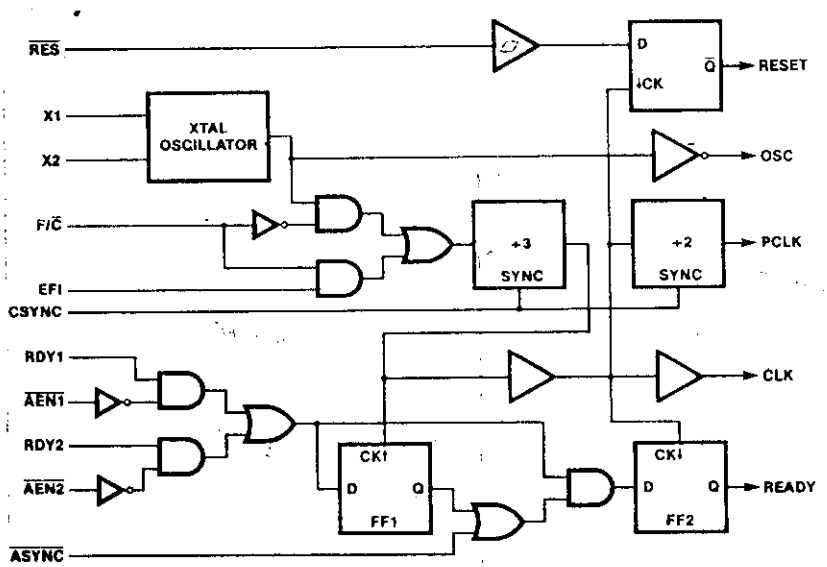


290081-7

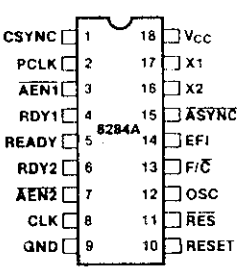
NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested. Output float is defined as the point where data is no longer driven—see timing diagram.
3. $\overline{OE}/V_{PP}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{CE}.

8284A/8284A-1
CLOCK GENERATOR AND DRIVER FOR iAPX 86, 88 PROCESSORS

- Generates the System Clock for the iAPX 86, 88 Processors:
  5 MHz, 8 MHz with 8284A
  10 MHz with 8284A-1
- Uses a Crystal or a TTL Signal for Frequency Source
- Provides Local READY and MULTIBUS® READY Synchronization
- 18-Pin Package
- Single +5V Power Supply
- Generates System Reset Output from Schmitt Trigger Input
- Capable of Clock Synchronization with Other 8284As
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range



8284A/8284A-1 Block Diagram



8284A/8284A-1 Pin Configuration

Table 1. Pin Description

Symbol	Type	Name and Function
$\overline{AEN1}$, $\overline{AEN2}$	I	**Address Enable:** $\overline{AEN}$ is an active LOW signal. AEN serves to qualify its respective Bus Ready Signal ($\overline{RDY1}$ or RDY2). $\overline{AEN1}$ validates RDY1 while $\overline{AEN2}$ validates RDY2. Two AEN signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Busses. In non Multi-Master configurations the $\overline{AEN}$ signal inputs are tied true (LOW).
RDY1, RDY2	I	**Bus Ready:** (Transfer Complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available. RDY1 is qualified by $\overline{AEN1}$ while RDY2 is qualified by $\overline{AEN2}$.
$\overline{ASYNC}$	I	**Ready Synchronization Select:** $\overline{ASYNC}$ is an input which defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is low, two stages of READY synchronization are provided. When $\overline{ASYNC}$ is left open (internal pull-up resistor is provided) or HIGH a single stage of READY synchronization is provided.
READY	O	**Ready:** READY is an active HIGH signal which is the synchronized RDY signal input. READY is cleared after the guaranteed hold time to the processor has been met.
X1, X2	I	**Crystal In:** X1 and X2 are the pins to which a crystal is attached. The crystal frequency is 3 times the desired processor clock frequency.
F/$\overline{C}$	I	**Frequency/Crystal Select:** F/$\overline{C}$ is a strapping option. When strapped LOW, F/$\overline{C}$ permits the processor's clock to be generated by the crystal. When F/$\overline{C}$ is strapped HIGH, CLK is generated from the EFI input.
EFI	I	**External Frequency:** When F/$\overline{C}$ is strapped HIGH, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output.

Symbol	Type	Name and Function
CLK	O	**Processor Clock:** CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus (i.e., the bipolar support chips and other MOS devices). CLK has an output frequency which is ⅓ of the crystal or EFI input frequency and a ⅓ duty cycle. An output HIGH of 4.5 volts (V_{CC} = 5V) is provided on this pin to drive MOS devices.
PCLK	O	**Peripheral Clock:** PCLK is a TTL level peripheral clock signal whose output frequency is ½ that of CLK and has a 50% duty cycle.
OSC	O	**Oscillator Output:** OSC is the TTL level output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.
$\overline{RES}$	I	**Reset In:** $\overline{RES}$ is an active LOW signal which is used to generate RESET. The 8284A provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.
RESET	O	**Reset:** RESET is an active HIGH signal which is used to reset the 8086 family processors. Its timing characteristics are determined by $\overline{RES}$.
CSYNC	I	**Clock Synchronization:** CSYNC is an active HIGH signal which allows multiple 8284As to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC needs to be externally synchronized to EFI. When using the internal oscillator CSYNC should be hardwired to ground.
GND		**Ground.**
V_{CC}		**Power:** +5V supply.

FUNCTIONAL DESCRIPTION

General

The 8284A is a single chip clock generator/driver for the iAPX 86, 88 processors. The chip contains a crystal-controlled oscillator, a divide-by-three counter, complete MULTIBUS "Ready" synchronization and reset logic. Refer to Figure 1 for Block Diagram and Figure 2 for Pin Configuration.

Oscillator

The oscillator circuit of the 8284A is designed primarily for use with an external series resonant, fundamental mode, crystal from which the basic operating frequency is derived.

The crystal frequency should be selected at three times the required CPU clock. X1 and X2 are the two crystal input crystal connections. For the most stable operation of the oscillator (OSC) output circuit, two series resistors ($R_1 = R_2 = 510\ \Omega$) as shown in the waveform figures are recommended. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.

For systems which have a V_{CC} ramp time ≥ 1V/ms and/or have inherent board capacitance between X1 or X2, exceeding 10 pF (not including 8284A pin capacitance), the two 510Ω resistors should be used. This circuit provides optimum stability for the oscillator in such extreme conditions. It is advisable to limit stray capacitances to less than 10 pF on X1 and X2 to minimize deviation from operating at the fundamental frequency.

If EFI is used and no crystal is connected, it is recommended that X_1 or X_2 should be tied to V_{CC} through a 510Ω resistor to prevent the oscillator from free running which might produce HF noise and additional I_{CC} current.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
All Output and Supply Voltages ..... −0.5V to +7V
All Input Voltages ..... −1.0V to +5.5V
Power Dissipation ..... 1 Watt

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
I_F	Forward Input Current ($\overline{ASYNC}$) Other Inputs		−1.3 −0.5	mA mA	V_F = 0.45V V_F = 0.45V
I_R	Reverse Input Current ($\overline{ASYNC}$) Other Inputs		50 50	μA μA	$V_R = V_{CC}$ V_R = 5.25V
V_C	Input Forward Clamp Voltage		−1.0	V	I_C = −5mA
I_{CC}	Power Supply Current		170	mA	
V_{IL}	Input LOW Voltage		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V	
V_{IHR}	Reset Input HIGH Voltage	2.6		V	
V_{OL}	Output LOW Voltage		0.45	V	5mA
V_{OH}	Output HIGH Voltage CLK Other Outputs	4 2.4		V V	−1mA −1mA
$V_{IHR} - V_{ILR}$	$\overline{RES}$ Input Hysteresis	0.25		V	

A.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%)

TIMING REQUIREMENTS

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_{EHEL}	External Frequency HIGH Time	13		ns	90% - 90% V_{IN}
t_{ELEH}	External Frequency LOW Time	13		ns	10% - 10% V_{IN}
t_{ELEL}	EFI Period	33		ns	(Note 1)
	XTAL Frequency	12	30	MHz	
t_{R1VCL}	RDY1, RDY2 Active Setup to CLK	35		ns	$\overline{ASYNC}$ = HIGH
t_{R1VCH}	RDY1, RDY2 Active Setup to CLK	35		ns	$\overline{ASYNC}$ = LOW
t_{R1VCL}	RDY1, RDY2 Inactive Setup to CLK	35		ns	
t_{CLR1X}	RDY1, RDY2 Hold to CLK	0		ns	
t_{AYVCL}	$\overline{ASYNC}$ Setup to CLK	50		ns	
t_{CLAYX}	$\overline{ASYNC}$ Hold to CLK	0		ns	
t_{A1VR1V}	$\overline{AEN1}$, $\overline{AEN2}$ Setup to RDY1, RDY2	15		ns	
t_{CLA1X}	$\overline{AEN1}$, $\overline{AEN2}$ Hold to CLK	0		ns	
t_{YHEH}	CSYNC Setup to EFI	20		ns	
t_{EHYL}	CSYNC Hold to EFI	10		ns	
t_{YHYL}	CSYNC Width	$2 \cdot t_{ELEL}$		ns	
t_{I1HCL}	$\overline{RES}$ Setup to CLK	65		ns	(Note 1)
t_{CLI1H}	$\overline{RES}$ Hold to CLK	20		ns	(Note 1)

National Semiconductor

ADC0801, ADC0802, ADC0803, ADC0804, ADC0805 8-Bit μP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters which use a differential potentiometric ladder similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus, and TRI-STATE® output latches directly drive the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

A new differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

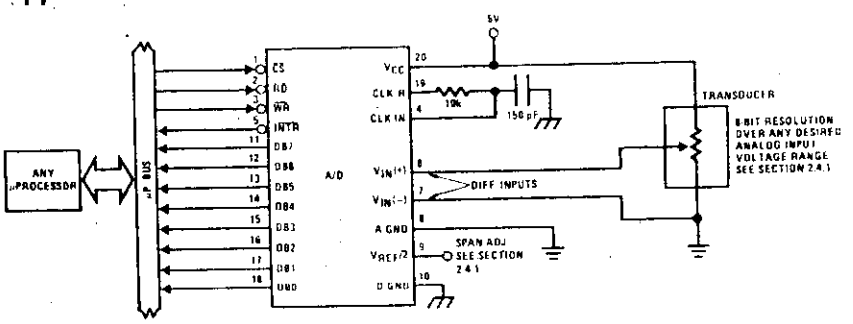
Features

- Compatible with 8080 μP derivatives—no interfacing logic needed — access time — 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and T^2L voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20 pin DIP package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

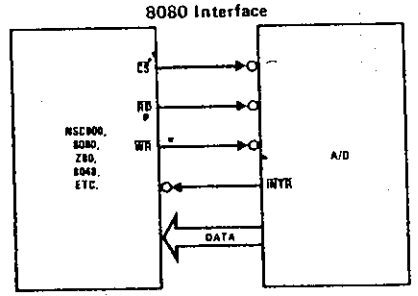
Key Specifications

- Resolution: 8 bits
- Total error: ±1/4 LSB, ±1/2 LSB and ±1 LSB
- Conversion time: 100 μs

Typical Applications



8080 Interface



ERROR SPECIFICATION (INCLUDES FULL SCALE, ZERO ERROR, AND NON-LINEARITY)			
PART NUMBER	FULL SCALE ADJUSTED	$V_{REF}/2$ = 2.500 V_{DC} (NO ADJUSTMENTS)	$V_{REF}/2$ = NO CONNECTION (NO ADJUSTMENTS)
ADC0801	±1/4 LSB	±1/2 LSB	±1 LSB
ADC0802	±1/2 LSB		
ADC0803		±1 LSB	
ADC0804			
ADC0805			

A single point analog ground should be used which is separate from the logic ground points. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of 1/4 LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

3.0 TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in *Figure 7*.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560 V_{DC} and a V_{CC} supply voltage of 5.12 V_{DC} should be used. This provides an LSB value of 20 mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090 V_{DC} (5.120 − 1 1/2 LSB) should be applied to the $V_{IN}(+)$ pin with the $V_{IN}(-)$ pin grounded. The value of the $V_{REF}/2$ input voltage should then be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital output LED display can be decoded by dividing the 8 bits into 2 hex characters, the 4 most significant (MS) and the 4 least significant (LS). Table I shows the fractional binary equivalent of these two 4-bit groups. By adding the decoded voltages which are obtained from the column: Input voltage value for a 2.560 $V_{REF}/2$ of both the MS and the LS groups, the value of the digital display can be determined. For example, for an output LED display of 1011 0110 or B6 (in hex), the voltage values from the table are 3.520 + 0.120 or 3.640 V_{DC}. These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.

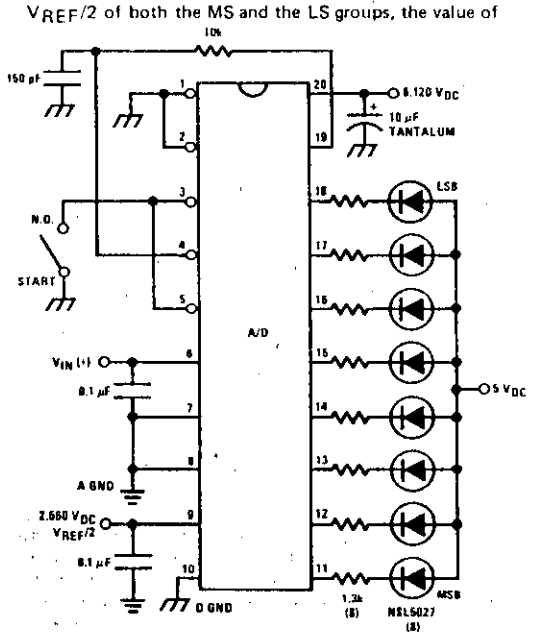


FIGURE 7. Basic A/D Tester

For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be provided as either analog voltages or differences in 2 digital words.

A basic A/D tester which uses a DAC and provides the error as an analog output voltage is shown in *Figure 8*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to directly readout the difference voltage, "A−C". The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis). The construction details of a tester of this type are provided in the NSC application note AN-179, "Analog-to-Digital Converter Testing".

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 9*, where the output code transitions can be detected as the 10-bit DAC is incremented. This provides 1/4 LSB steps for the 8 bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

4.0 MICROPROCESSOR INTERFACING

To discuss the interface with 8080A and 6800 microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored in 16 successive memory locations. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

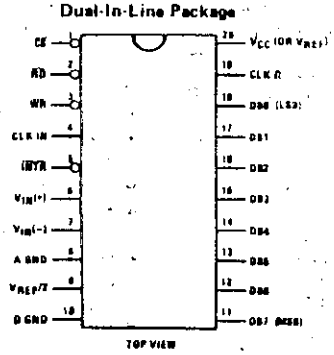
This converter has been designed to directly interface with derivatives of the 8080 microprocessor. The A/D can be mapped into memory space (using standard memory address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15 as they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in *Figure 10*.

Ordering Information

TEMPERATURE RANGE		0°C TO 70°C	−40°C TO +85°C	−40°C TO +85°C	−55°C TO +125°C
ERROR	±1/4 Bit Adjusted		ADC0801LCN	ADC0801LCD	ADC0801LD
	±1/2 Bit Unadjusted		ADC0802LCN	ADC0802LCD	ADC0802LD
	±1/2 Bit Adjusted		ADC0803LCN	ADC0803LCD	
	±1 Bit Unadjusted	ADC0804LCN	ADC0805LCN	ADC0804LCD	
PACKAGE OUTLINE		N20A—MOLDED DIP		D20A—CAVITY DIP	D20A—CAVITY DIP

Connection Diagram

ADC080X
Dual-In-Line Package



TOP VIEW

ANALOG DEVICES

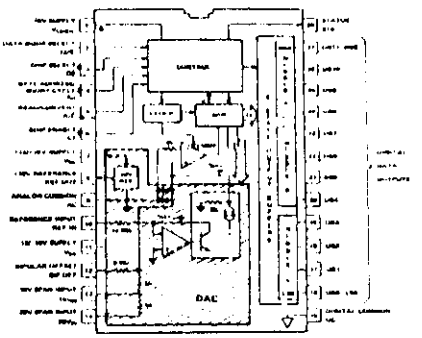
Fast, Complete 12-Bit A/D Converter with Microprocessor Interface

AD574A

FEATURES

- Complete 12-Bit A/D Converter with Reference and Clock
- Full 8- or 16-Bit Microprocessor Bus Interface
- 250ns Bus Access Time
- Guaranteed Linearity Over Temperature
  - 0 to +70°C – AD574AJ, AK, AL
  - −55°C to +125°C – AD674AS, AT, AU
- No Missing Codes Over Temperature
- Fast Successive Approximation Conversion – 25µs
- Buried Zener Reference for Long-Term Stability and Low Gain T.C. 10ppm/°C max AD574AL
  12.5ppm/°C max AD574AU
- Low Profile 28-Pin Ceramic DIP
- Low Power: 390mW

AD574A FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD574A is a complete 12-bit successive-approximation analog-to-digital converter with 3-state output buffer circuitry for direct interface to an 8-, 12-or 16-bit microprocessor bus. The AD574A design is implemented with two LSI chips each containing both analog and digital circuitry, resulting in the maximum performance and flexibility at the lowest cost.

One chip is the high performance AD565A 12-bit DAC and voltage reference. It contains the high speed current output switching circuitry, laser-trimmed thin film resistor network, low T.C. buried zener reference and the precision input scaling and bipolar offset resistors. This chip is laser trimmed at the wafer stage (LWT) to adjust ladder network linearity, voltage reference tolerance and temperature coefficient, and the calibration accuracy of input scaling and bipolar offset resistors.

The second chip uses the proven LCI (linear-compatible integrated injection logic) process to provide the low-power I²L successive-approximation register, converter control circuitry, clock, bus interface, and the high performance latching comparator. The precision, low-drift comparator is adjusted for initial input offset error at the wafer stage by the "zener-zap" technique which trims the comparator input stage to 1/10 LSB typical error. This form of trimming, while cumbersome for complex ladder networks, is an attractive alternative to thin film resistor trimming for a simple offset adjustment and eliminates the need for thin film processing for this portion of the circuitry.

The AD574A is available in six different grades. The AD574AJ, AK, and AL grades are specified for operation over the 0 to +70°C temperature range. The AD574AS, AT, and AU are specified for the −55°C to +125°C range. All grades are packaged in a low-profile, 0.600 inch wide, 28-pin hermetically-sealed ceramic DIP.

PRODUCT HIGHLIGHTS

1. The AD574A interfaces to most popular microprocessors with an 8-, 12-, or 16-bit bus without external buffers or peripheral interface controllers. Multiple-mode three-state output buffers connect directly to the data bus while the read and convert commands are taken from the control bus. The 12-bits of output data can be read either as one 12-bit word or as two 8-bit bytes (one with 8 data bits, the other with 4 data bits and 4 trailing zeros).
2. The precision, laser-trimmed scaling and bipolar offset resistors provide four calibrated ranges, 0 to +10 and 0 to +20 volts unipolar, or −5 to +5 and −10 to +10 volts bipolar. Typical bipolar offset and full scale calibration of ±0.1% can be trimmed to zero with one external component each.
3. The internal buried zener reference is trimmed to 10.00 volts with 1% maximum error and 15ppm/°C typical T.C. The reference is available externally and can drive up to 1.5mA beyond that required for the reference and bipolar offset resistors.

CIRCUIT OPERATION

The AD574A is a complete 12-bit A/D converter which requires no external components to provide the complete successive-approximation analog-to-digital conversion function. A block diagram of the AD574A is shown in Figure 1. The device consists of two chips, one containing the precision 12-bit DAC with voltage reference, the other containing the comparator, successive-approximation register, clock, output buffers and control circuitry.

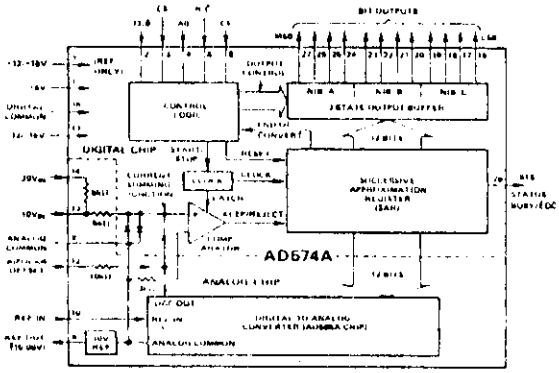


Figure 1. Block Diagram of AD574A 12-Bit A-to-D Converter

When the control section is commanded to initiate a conversion (as described later), it then enables the clock and resets the successive-approximation register (SAR) to all zeros. Once a conversion cycle has begun, it cannot be stopped or re-started and data is not available from the output buffers. The SAR, timed by the clock, will then sequence through the conversion cycle and perform an end of convert flag to the control section. The control section will then disable the clock, bring the output status flag low, and enable control functions to allow data read functions by external command.

During the conversion cycle, the internal 12-bit current output DAC is sequenced by the SAR from the most-significant-bit (MSB) to least significant bit (LSB) to provide an output current which accurately balances the input signal current through the 5kΩ (or 10kΩ) input resistor. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±½LSB.

The temperature-compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10.00 volts ± 1%; it can supply up to 1.5mA to an external load in addition to that required to drive the reference input resistor (0.5mA) and bipolar offset resistor (1mA) when the AD574A is powered from ± 15V supplies. If the AD574A is used with + 12V supplies, or if external current must be supplied over the full temperature range, an external buffer amplifier is recommended. Any external load on the AD574A reference must remain constant during conversion. The thin film application resistors are trimmed to match the full scale output current of the DAC. There are two 5kΩ input scaling resistors to allow either a 10 volt or 20 volt span. The 10kΩ bipolar offset resistor is grounded for unipolar operation or connected to the 10 volt reference for bipolar operation.

DRIVING THE AD574A ANALOG INPUT

The AD574A is a successive-approximation type analog-to-digital converter. During the conversion cycle, the ADC input current is modulated by the DAC test current at approximately a 500kHz rate. Thus it is important to recognize that the signal source driving the AD574A must be capable of holding a constant output voltage under dynamically-changing load conditions.

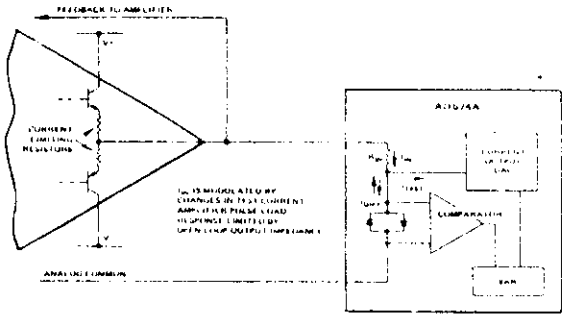


Figure 2. Op Amp – AD574A Interface

The closed loop output impedance of an op amp is equal to the open loop output impedance (usually a few hundred ohms) divided by the loop gain at the frequency of interest. It is often assumed that the loop gain of a follower connected op amp is sufficiently high to reduce the closed loop output impedance to a negligibly small value, particularly if the signal is low frequency. However, the amplifier driving an AD574A must either have sufficient loop gain at 500kHz to reduce the closed loop output impedance to a low value or have low open loop output impedance.

This can be accomplished either by using a wideband op amp or by placing a discrete-transistor or integrated buffer inside the amplifier's feedback loop.

SUPPLY DECOUPLING AND LAYOUT CONSIDERATIONS

It is critically important that the AD574A power supplies be filtered, well-regulated, and free from high frequency noise. Use of noisy supplies will cause unstable output codes to be generated. Switching power supplies are not recommended for circuits attempting to achieve 12-bit accuracy unless great care is used in filtering any switching spikes present in the output. Remember that a few millivolts of noise represents several counts of error in a 12-bit ADC.

Decoupling capacitors should be used on all power supply pins; the + 5V supply decoupling capacitor should be connected directly from pin 1 to pin 15 (digital common) and the $+V_{LA}$ and $-V_{LA}$ pins should be decoupled directly to analog common (pin 9). A suitable decoupling capacitor is a 47µF tantalum type in parallel with a 0.1µF disc ceramic type.

Circuit layout should attempt to locate the AD574A, associated analog input circuitry, and interconnections as far as possible from logic circuitry. For this reason, the use of wire-wrap circuit construction is not recommended. Careful printed circuit construction is preferred.

UNIPOLAR RANGE CONNECTIONS FOR THE AD574A

The AD574A contains all the active components required to perform a complete 12-bit A/D conversion. Thus, for most situations, all that is necessary is connection of the power supplies (+5, +12/+15 and −12/−15 volts), the analog input, and the conversion initiation command, as discussed on the next page. Analog input connections and calibration are easily accomplished; the unipolar operating mode is shown in Figure 4.

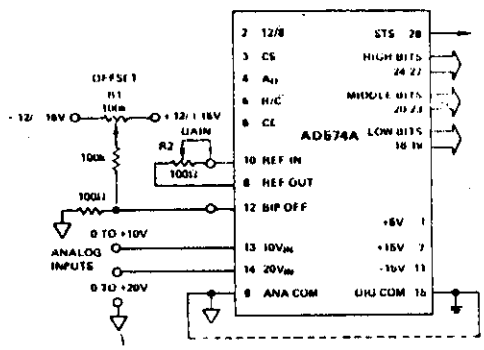


Figure 3. Unipolar Input Connections

All of the thin film application resistors of the AD574A are trimmed for absolute calibration. Therefore, in many applications, no calibration trimming will be required. The absolute accuracy for each grade is given in the specification tables. For example, if no trims are used, the AD574AK guarantees ±2LSB max zero offset error and ±0.25% (10LSB) max full scale error. (Typical full scale error is ±2LSB.) If the offset trim is not required, pin 12 can be connected directly to pin 9; the two resistors and trimmer for pin 12 are then not needed. If the full scale trim is not needed, a 50Ω ±1% metal film resistor should be connected between pin 8 and pin 10.

The analog input is connected between pin 13 and pin 9 for a 0 to +10V input range, between 14 and pin 9 for a 0 to +20V input range. The AD574A easily accommodates an input signal beyond the supplies. For the 10 volt span input, the LSB has a nominal value of 2.44mV, for the 20 volt span, 4.88mV. If a 10.24V range is desired (nominal 2.5mV/bit), the gain trimmer (R2) should be replaced by a 50Ω resistor, and a 200Ω trimmer inserted in series with the analog input to pin 13 (for a full scale range of 20.48V (5mV/bit), use a 500Ω trimmer into pin 14). The gain trim described below is now done with these trimmers. The nominal input impedance into pin 13 is 5kΩ, and 10kΩ into pin 14.

UNIPOLAR CALIBRATION

The AD574A is intended to have a nominal ½LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above and below it). Thus, when properly calibrated, the first transition (from 0000 0000 0000 to 0000 0000 0001) will occur for an input level of +1/2LSB (1.22mV for 10V range).

If pin 12 is connected to pin 9, the unit typically will behave in this manner, within specifications. If the offset trim (R1) is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately ±15mV of offset trim range.

The full scale trim is done by applying a signal 1 1/2LSB below the nominal full scale (9.9963 for a 10V range). Trim R2 to give the last transition (1111 1111 1110 to 1111 1111 1111).

BIPOLAR OPERATION

The connections for bipolar ranges are shown in Figure 4. Again, as for the unipolar ranges, if the offset and gain specifications are sufficient, one or both of the trimmers shown can be replaced by a 50Ω ±1% fixed resistor. The analog input is applied as for the unipolar ranges. Bipolar calibration is similar to unipolar calibration. First, a signal ½LSB above negative full scale (−4.9988V for the ±5V range) is applied and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then a signal 1½LSB below positive full scale (+4.9963V for the ±5V range) is applied and R2 trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

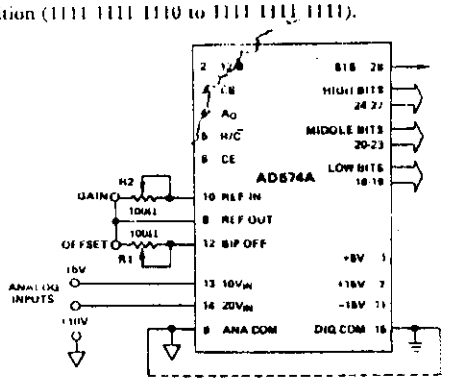


Figure 4. Bipolar Input Connections

GROUNDING CONSIDERATIONS

The analog common at pin 9 is the ground reference point for the internal reference and is thus the "high quality" ground for the AD574A; it should be connected directly to the analog reference point of the system. In order to achieve all of the high accuracy performance available from the AD574A in an environment of high digital noise content, it is required that the analog and digital commons be connected together at the package. In some situations, the digital common at pin 15 can be connected to the most convenient ground reference point; analog power return is preferred.

Signetics

74LS245
Transceiver

Octal Transceiver (3-State)
Product Specification

Logic Products

FEATURES
- Octal bidirectional bus interface
- 3-State buffer outputs
- PNP inputs for reduced loading
- Hysteresis on all Data inputs

DESCRIPTION
The 'LS245 is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The outputs are all capable of sinking 24mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features a Chip Enable (CE) input for easy cascading and a Send/Receive (S/R) input for direction control. All data inputs have hysteresis built in to minimize AC noise effects.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS245	8ns	54mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74LS245N
Plastic SOL-20	N74LS245D

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
All	Inputs	1LSul
All	Outputs	30LSul

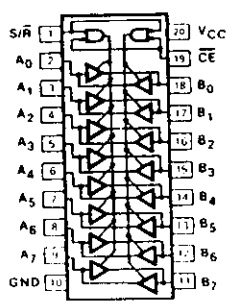
NOTE:
Where a 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}

FUNCTION TABLE

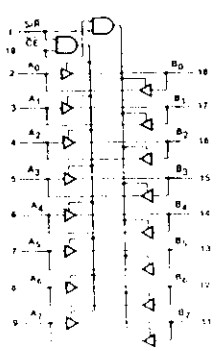
INPUTS		INPUTS/OUTPUTS	
$\overline{CE}$	S/$\overline{R}$	A_n	B_n
L	L	A = B	INPUTS
L	H	INPUT	B = A
H	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance "off" state

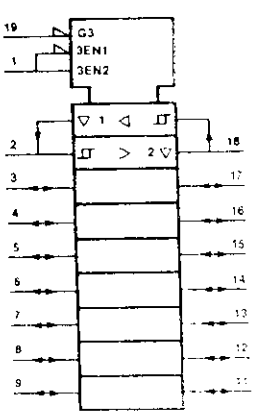
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Signetics

74155, LS155
Decoders/Demultiplexers

Dual 2-Line To 4-Line Decoder/Demultiplexer
Product Specification

Logic Products

FEATURES
- **Common Address Inputs**
- **True or complement data demultiplexing**
- **Dual 1-of-4 or 1-of-8 decoding**
- **Function generator applications**

DESCRIPTION
The '155 is a Dual 1-of-4 Decoder/Demultiplexer with common Address inputs and separate gated Enable inputs. Each decoder section, when enabled, will accept the binary weighted Address input (A_0, A_1) and provide four mutually exclusive active-LOW outputs ($\overline{0} - \overline{3}$). When the enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74155	18ns	25mA
74LS155	17ns	6.1mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74155N, N74LS155N
Plastic SO	N74LS155D

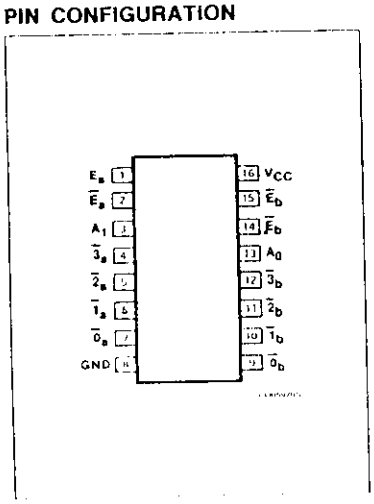
NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

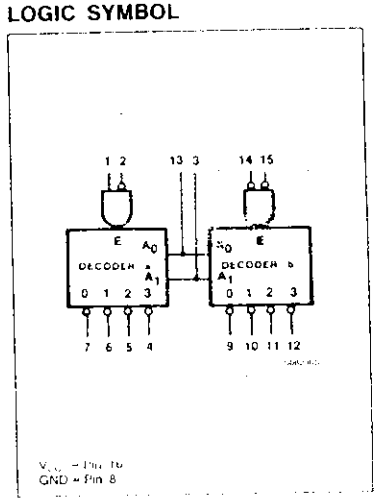
PINS	DESCRIPTION	74	74LS
All	Inputs	1ul	1LSul
All	Outputs	10ul	10LSul

NOTE:
Where a 74 unit load (ul) is understood to be 40µA I_{IH} and −1.6mA I_{IL}, and a 74LS unit load (1 Sul) is 20µA I_{IH} and −0.4mA I_{IL}.

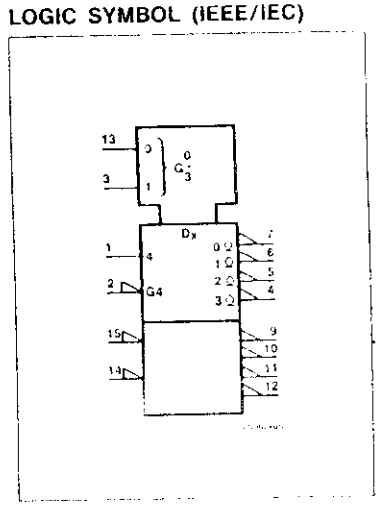
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			74LS245			UNIT
					Min	Typ[2]	Max	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = MIN			0.2	0.4		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_L = MAX	I_{OH} = MAX		2.0			V
			I_{OH} = −3mA		2.4	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX				0.5	V
			I_{OL} = 12mA (74LS)				0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$					−1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_O = 2.7V, $\overline{CE}$ = 2.0V					20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_O = 0.4V, $\overline{CE}$ = 2.0V					−200	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V	A, B inputs			0.1	mA
			V_I = 7.0V	S/$\overline{R}$, $\overline{CE}$ inputs			0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					−0.2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−40		−130	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH			48	70	mA
			I_{CCL} Outputs LOW			62	90	mA
			I_{CCZ} Outputs OFF			64	95	mA

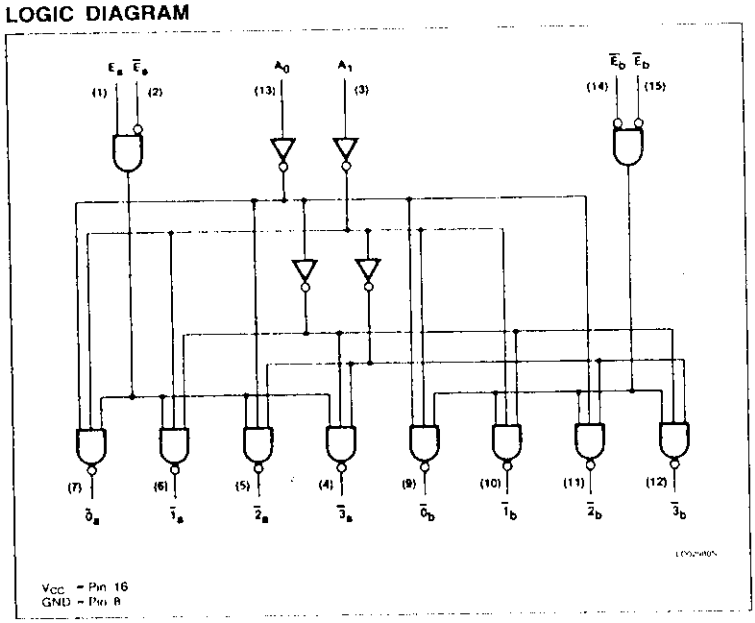
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with outputs open.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	74LS C_L = 4pF, R_L = 667Ω		UNIT
			Min	Max	
t_{PLH}	Propagation delay	Waveform 1		12	ns
t_{PHL}	Propagation delay	Waveform 1		12	ns
t_{PZH}	Enable to HIGH	Waveform 2		40	ns
t_{PZL}	Enable to LOW	Waveform 3		40	ns
t_{PHZ}	Disable from HIGH	Waveform 2, C_L = 5pF		25	ns
t_{PLZ}	Disable from LOW	Waveform 3, C_L = 5pF		25	ns

LOGIC DIAGRAM



Both decoder sections have a 2-input enable gate. For decoder "a" the enable gate requires one active-HIGH input and one active-LOW input ($E_a \cdot \overline{E}_a$). Decoder "a" can accept either true or complemented data in demultiplexing applications, by using the E_a or $\overline{E}_a$ inputs respectively. The decoder "b" enable gate requires two active-LOW inputs ($\overline{E}_b \cdot \overline{E}_b$). The device can be used as a 1-of-8 decoder/demultiplexer by tying E_a to $\overline{E}_b$ and relabeling the common connection address as (A_2); forming the common enable by connecting the remaining $\overline{E}_b$ and $\overline{E}_a$.

FUNCTION TABLE

ADDRESS		ENABLE "a"		OUTPUT "a"				ENABLE "b"		OUTPUT "b"			
A_0	A_1	E_a	$\overline{E}_a$	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{E}_b$	$\overline{E}_b$	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 70		°C