DEPARTMENT OF

ELECTRONICS AND COMMUNICATION ENGINEERING

KUMARAGURU COLLEGE OF TECHNOLOGY

COIMBATORE - 641 006

P - 1278

CERTIFICATE

THIS IS TO CERTIFY THAT THE REPORT ENTITLED

MICROPROCESSOR BASED DIGITAL FAREMETER

HAS BEEN SUBMITTED BY

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TIRUMALASETTY RAVI
V. VENKATARAMANA.

IN PARTIAL FULFILLMENT OF THE AWARD OF THE DEGREE OF BACHELOR OF ENGINEERING IN ELECTRONICS AND COMMUNICATION ENGINEERING BRANCH OF THE BHARATHIAR UNIVERSITY, COIMBATORE - 46 DURING THE ACADEMIC YEAR 1991-92.

20/3/92

GUIDE

20/3/92

HEAD OF THE DEPARTMENT

CERTIFIED THAT THE CANDIDATE WAS EXAMINED BY US IN THE PROJECT WORK VIVA-VOCE EXAMINATION HELD ON _____

AND THE UNIVERSITY REGISTER NUMBER WAS _____

_____

INTERNAL EXAMINER

_____

EXTERNAL EXAMINER

ACKNOWLEDGEMENT

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We express our sincere Thanks to our Professor and the Head of the Department K. **PALANISWAMI, M.E.,M.IEEE.,MIE., MISTE.,MCSI.,FIETE.,** for all the valuable informations he has provided us to make our project success.

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Last but not least we thank the lab technicians for their co-operation.

INDEX

SYNOPSIS

It is very clear from the day-to-day life that the electronic field is improving enormously in such a way that all the analog devices are replaced by digital circuits for better accuracy and reliability. The Project Fare meter is strictly confined to the measurement and display of various parameters like speed, distance and Fare (which can be preset per kilometer to desired value) in digital format.

In this system the microprocessor (8085) plays a very important role in arithmetic and logical operations and to generate control signals to the various parts of the system.

The Faremeter can be easily implemented in hire vehicles where the display is very much useful for the public. The parameters like speed, distance and Fare can be determined without any manipulations.

INTRODUCTION

Nowadays the taxis and autos are using analog devices for displaying fare speed etc. Electronic field is developed in such a way that these analog devices are replaced by digital devices. Digital devices have greater accuracy, increased relability, high resolution, easy readability and less maintenance compared to analog devices.

Our project confines to the following

1. Displaying the speed of the moving vehic le.
2. Displaying the distance travelled by the vehic le.
3. Displaying the fare for the distance travelled.

CHAPTER I SYSTEM DESCRIPTION

1.1 Hardware Description

1.2 Software Description

1.1 HARDWARE DESCRIPTION:

The hardware circuit is designed to convert the rotations of rotor of the motor into the pulses, to regulate the pulses in required manner, to count the number of pulses, to display the speed, distance and fare. The system block diagram is shown in fig. (1.1).

The system consists of the following parts.

1. Motor
2. Transducer (Proximity Switch)
3. Pulse shaping network (Schmitt Trigger) (74LS132)
4. Decade counter (74LS93)
5. Microprocessor (8085)
6. EPRDM (2732A), RAM (6116)
7. Keyboard and Display interface (8279)
8. 6 digit 7 segment display.

MOTOR:

A 5V DC motor having the maximum of 2400 rpm is used for rotating the wheel, for the demonstration purpose.

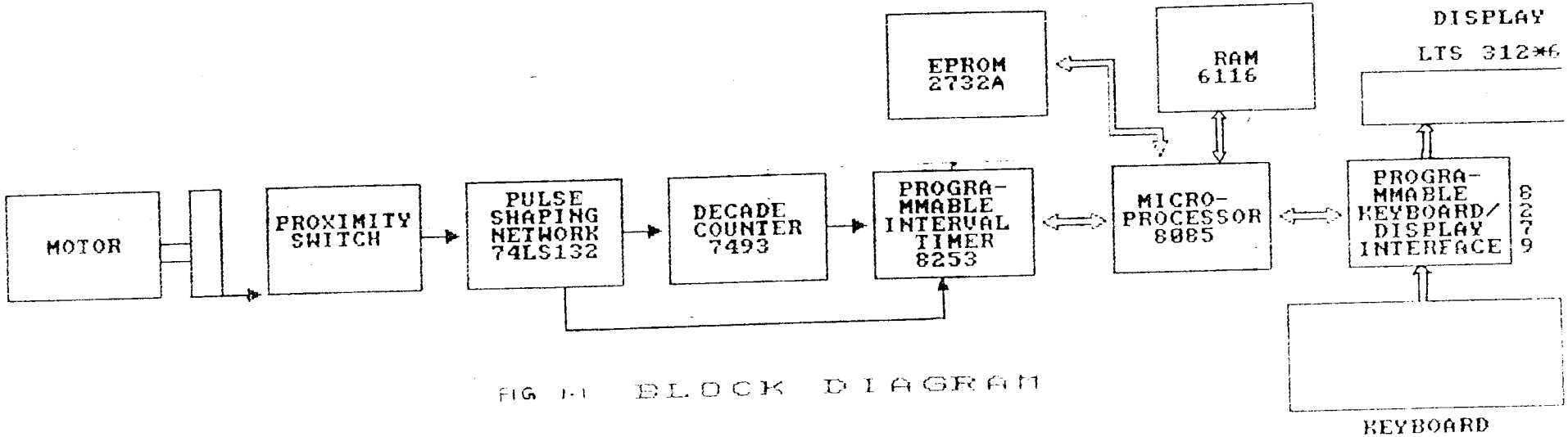


FIG 4.1 BLOCK DIAGRAM

The radius of the rotor of the motor is r = 0.106m. An iron piece is attached to the shaft of the motor. The iron piece will rotate with the speed equal to the motor speed. The motor speed can be varied by varying the voltage given to the motor.

Atleast 3V should be applied to the motor inorder to rotate it at optimum speed. Since the speed of the motor is directly proportional to the armature voltage, speed increase with the applied voltage.

The maximum voltage applied to the motor shouldn't exceed 5V because the rated voltage of the motor is 5V. If the voltage exceeds the rated value, then, the motor gets damaged.

The motor is positioned on the base of the iron stand for our system. The motor has two wires. One wire from the motor is connected to the supply and the other to ground of the supply.

PROXIMITY SWITCH:

Proximity Switch is a transducer which convert rotations into pulses. Proximity switch is covered by a metallic frame for mechanical stability and rough usage of the machine. The

environmental conditions like temperature and pressure will not affect the properties and active operation of the switch.

The proximity switch is placed inside the Brake drum, at a distance of 8mm apart from the metallic piece which is attached to the rotor of the motor. For demonstration purpose we are using a metallic stand to which the switch is fixed. At the bottom of the switch the motor is placed. The distance between the metallic piece and the switch is maintained at a distance of 8mm apart.

The number of pulses generated by the proximity switch are proportional to the number of rotations of the rotor of the motor. The main advantage of the proximity switch is that there is no neccessity for a physical contact between the rotor and the transducer. This improve the life time of the switch and it reduces maintenance problem.

The proximity switch is capable of generating pulses upto 200 Hz. Here in this system the maximum frequency of 60Hz is generated. Because of generation of pulses at higher frequencies, it can be used for high speed vehichles.

The proximity switch has 3 wires namely Red, Black and Green. The Red wire is connected to the positive terminal

of the supply and the Black wire to ground. The load is connected across the Red wire and Green wire through which the output is taken.

OPERATION OF THE SWITCH:

The operation of the switch is as follows.
When the rotor of the motor starts rotating, the metallic piece which is connected to the rotor of the motor starts rotating with the speed equal to that of the rotor of the motor.

Whenever the metallic piece crosses the head of the proximity switch, due to magnetic induction between metallic piece and switch, pulses are generated from the output of the proximity switch.

For every rotation of the motor, the metallic piece crosses the proximity switch head two times. Thus in this way two pulses are generated for every rotation of the motor.

The proximity switch consists of a metallic switch to which a small magnet is attached. Whenever the metallic piece crosses the head of the proximity switch, the switch is closed. Hence whatever input voltage is fed, is available at the output of the proximity switch.

The minimum voltage that can be fed to the proximity switch for normal operation is 5V and the maximum voltage is 30V. Here we are adjusting the input voltage of the proximity switch to 5.1V such that the output voltage is 5V exactly. The excess voltage of (0.1)V is due to the drop inside the switch.

PULSE SHAPING NETWORK:

Pulse shaping network regulates the irregular pulses into regular well defined pulses. For this purpose we are using a Schmitt NAND gate (74LS132).

The pulses are fed to the junction of two diodes as shown in the circuit diagram. The negative cycle of the input are bypassed to ground through diode D_1 which is forward biased and diode D_2 is reverse biased. Then there won't be any pulses fed to the Schmitt NAND gate.

When the positive pulses are fed to the input the diode D_1 is reverse biased where as the diode D_2 is forward biased. Now the positive cycle of the input are fed to the Schmitt NAND gate. The output of the Schmitt NAND inverter goes low. We are getting the pulses of (0 to 5V) at the output of the Schmitt NAND inverter.

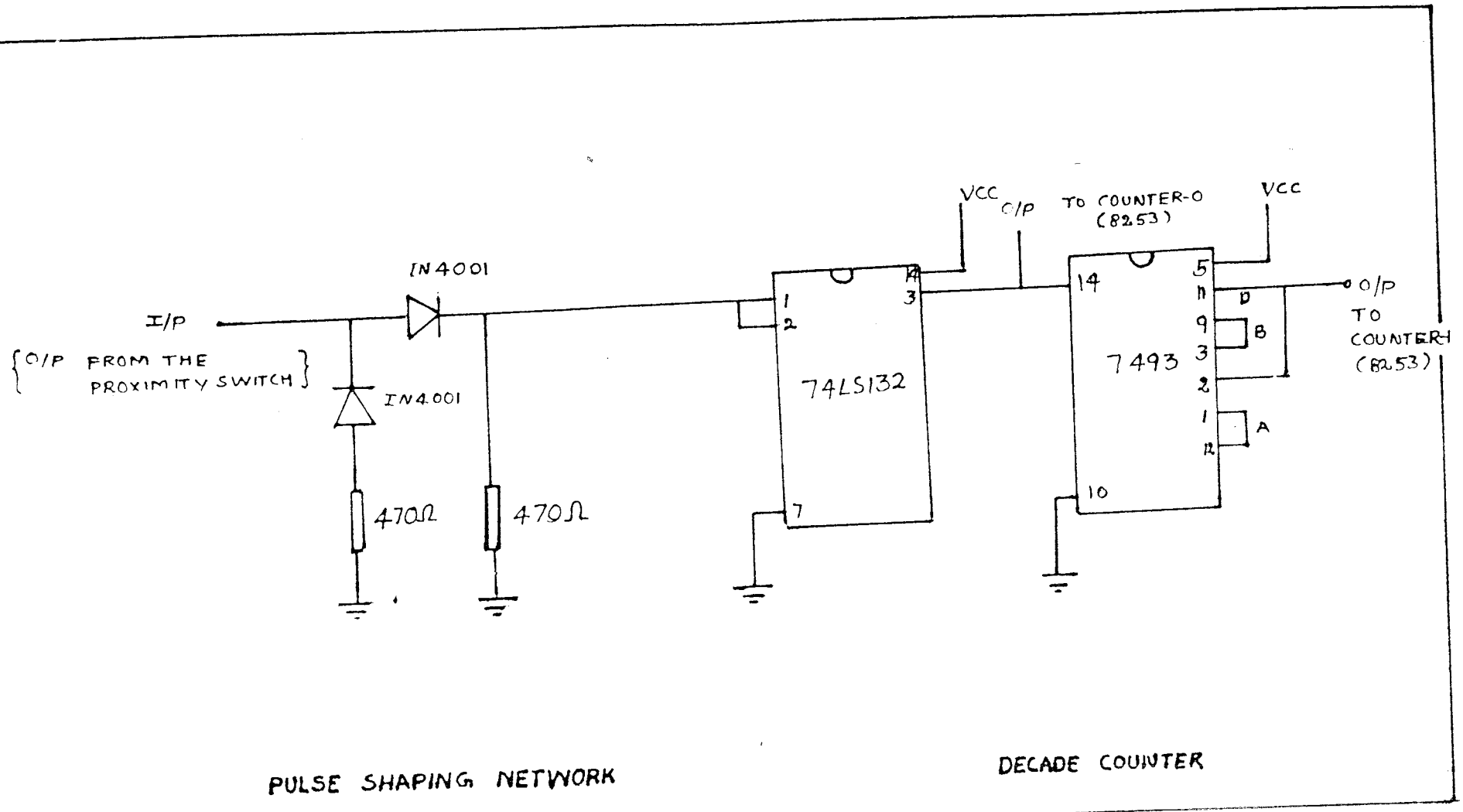

IN4001
I/P
O/P FROM THE PROXIMITY SWITCH
IN4.001
470Ω
470Ω
74LS132
VCC
O/P
TO COUNTER-0 (8253)
VCC
7493
14
5
11
D
9
B
3
2
1
A
12
10
O/P TO COUNTER (8253)
PULSE SHAPING NETWORK
DECADE COUNTER

FIG 1·3

DECADE COUNTER:

Decade counter is used to generate one output pulse for every 10 pulses of the input. Here IC 74LS93 is used for this purpose.

There are two pulses coming out of the pulse shaping network for each revolution of the rotor of the motor. These pulses are fed to the decade counter which generates 0.2 pulses per revolution (ie) 2 pulses for every 10 revolutions of the motor. These pulses are fed to the 8253 Timer of the micro processor system. Here 8253 is operated at mode 2 and counter 1 is used for fare and distance measurement.

PROGRAMMABLE TIMER (8253):

8253 is a programmable timer which consists of three 16-bit down counters. Here we are using the counter - 0 and counter - 1. Counter - 2 is left free for future development of the system.

The timer can be operated in any one of the six modes. We are using the second mode (mode-2). The control word is stored in the control register of the 8253 for mode setting. The control word is 34.

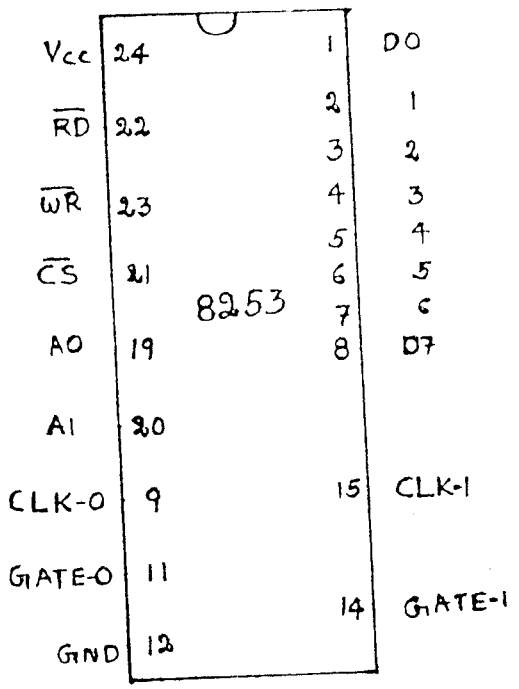


FIG 1·4

SCHEMATIC DIAGRAM OF 8253

00	11	010	0
Counter-0	LSB First MSB Next	Mode-2	Binary

The control word to latch the counter is 04.

00	00	010	0
Counter-0	Latch	Mode-2	Binary

Counter-0 => E0

Counter-1 => E1

Counter-2 => E2

Control Register => E3

The number of pulses from the pulse shaping network counted in counter-0 is used to measure the speed of the vehichle and counter-1 is used to measure the distance and the fare for the distance travelled.

The counter is initially loaded with the value FFFF, and for each pulse the contents of the counters are decremented by one. The counter-0 is decremented twice for every revolutions of the motor and the counter-1 is decremented twice for every 10 revolutions of the motor.

No. of Revolutions of motor	No. of Pulses	Counter - 0 15.....0	Counter - 1 15.....0
0	0	1111 1111 1111 1111	1111 1111 1111 1111
1	2	1111 1111 1111 1101	1111 1111 1111 1111
10	20	1111 1111 1110 1011	1111 1111 1111 1101

Gate - 0 and Gate - 1 are always kept at higher level inorder to enable the counter - 0 and counter - 1. If the gate level goes low the counter is disabled.

MICROPROCESSOR (8085):

The 8 bit 8085 Microprocessor is Heart of the system. It generates and sends control signals to all parts in the system. It access and process the data and the result is fed to the display unit to display the various parameters like speed, distance and fare.

The 8085 Microprocessor is a 8 bit processor. It consists of six general purpose scratch pad registers namely B,C,D,E,H and L. It consists of an Accumulator, stack pointer and a program counter.

The Microprocessor can be effectively programmed to perform required arithmetic and logic operation for the given data, by selecting necessary instructions from its set. These instructions are given to the microprocessor by writing into ints memory. Writing the instruction and data in memory is done through an input device, keyboard. The Microprocessor read each instruction at a time from the memory and executes the instruction accordingly with a help of various registers. The results are either be stored in its memory or be sent to the output display. In addition to the normal execution of the program, it can respond external signals and interrupts.

The various functions performed by the Microprocessor can be classified into three general categories. They are as follows.

1. Microprocessor - initiated operations
2. Internal data operations
3. Peripheral initiated operations.

To perform these functions, the microprocessor requires a group of logic circuits and a set of signals called the control signals.

In this system the microprocessor initialises the counter and waits for a certain period of time. Then it takes the data from the counter and processes it.

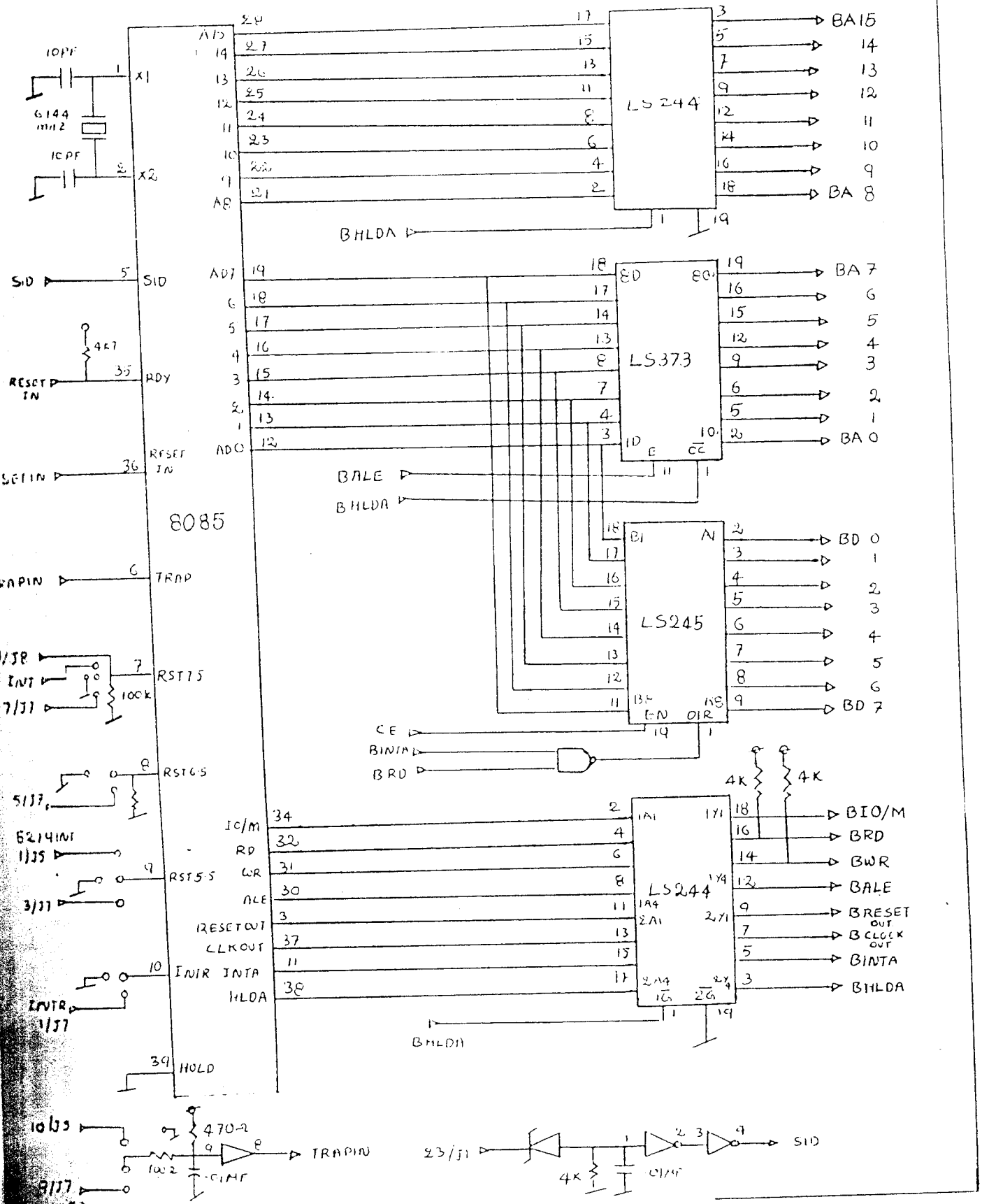
MEASUREMENT OF SPEED:

Initially the count in the counter-0 was FFFF. The Microprocessor initiates the counter and now counter starts decrementing bit by bit. After one second delay the counted value is loaded into the register. The final value loaded in the register is subtracted from FFFF and this gives the count for one second. Thus the count for one second is determined and the speed of the vehichle is calculated by arithmetical operation over the data. These operations are explained in a detailed manner in the forthcoming chapter under speedometer. After the completion of the operation over the data, the speed calculated so far in memory is brought to the display unit.

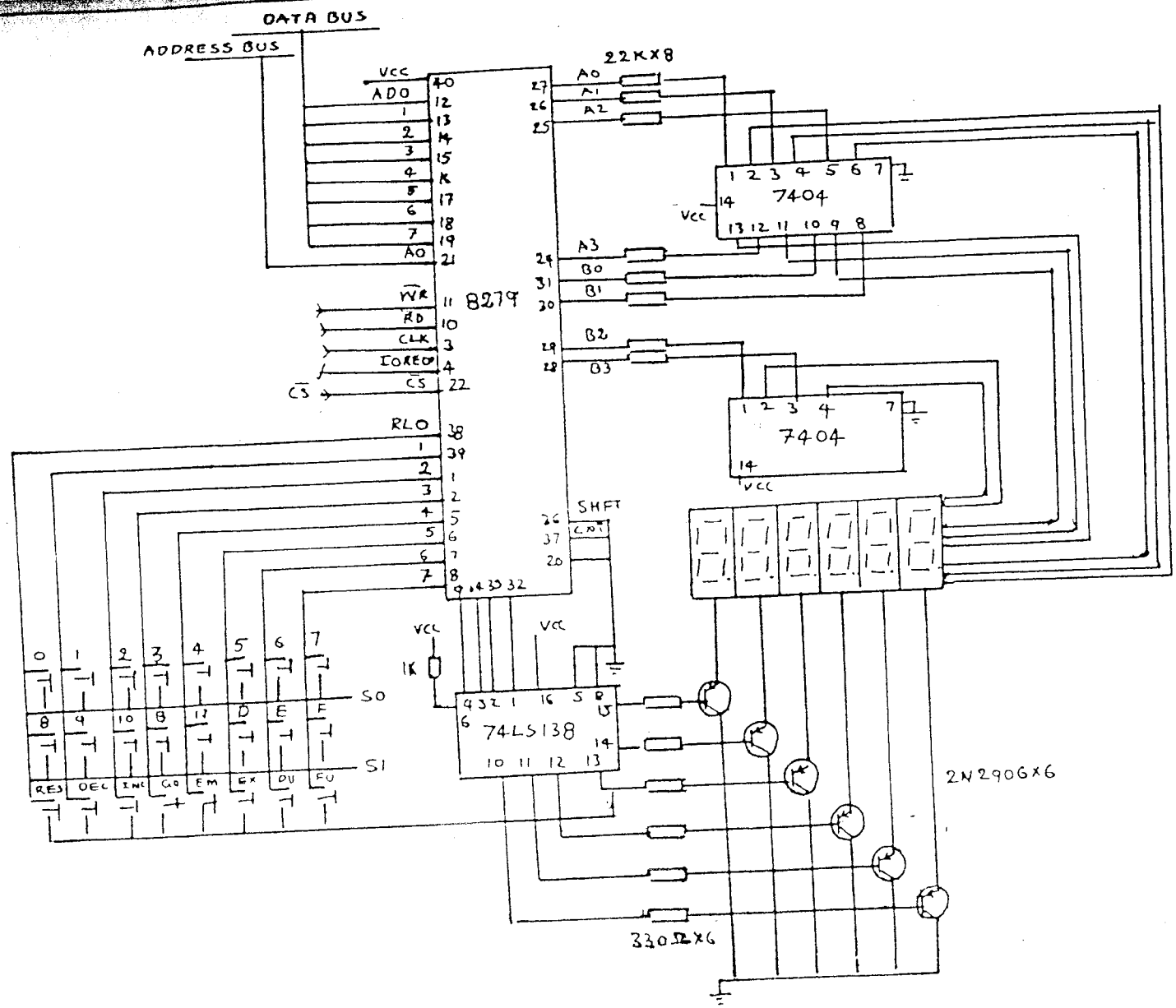
MEASUREMENT OF FARE:

For determining the fare the counter is initialised and the data FFFF is stored in it. Now the counter is decremented. The Microprocessor waits for 30 seconds and the final data is loaded. The difference between FFFF and the data gives the count. The arithmetical operations are performed over the count and the fare is displayed in the 7 segment display unit.

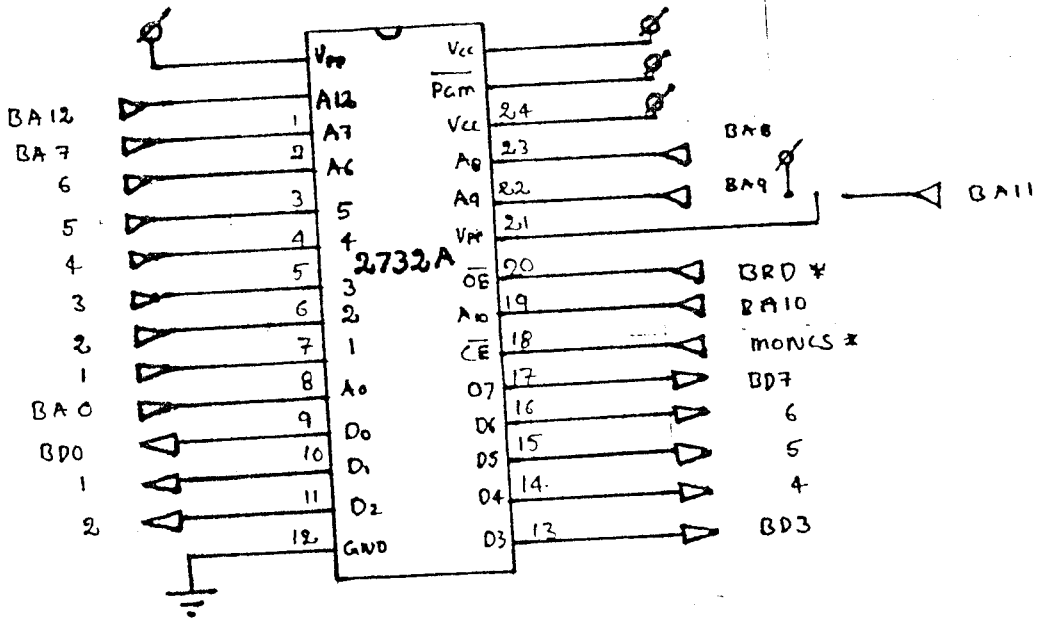
The details of EPROM, RAM, Keyboard Interface and 6 digit 7 segment display are given in the Appendix.

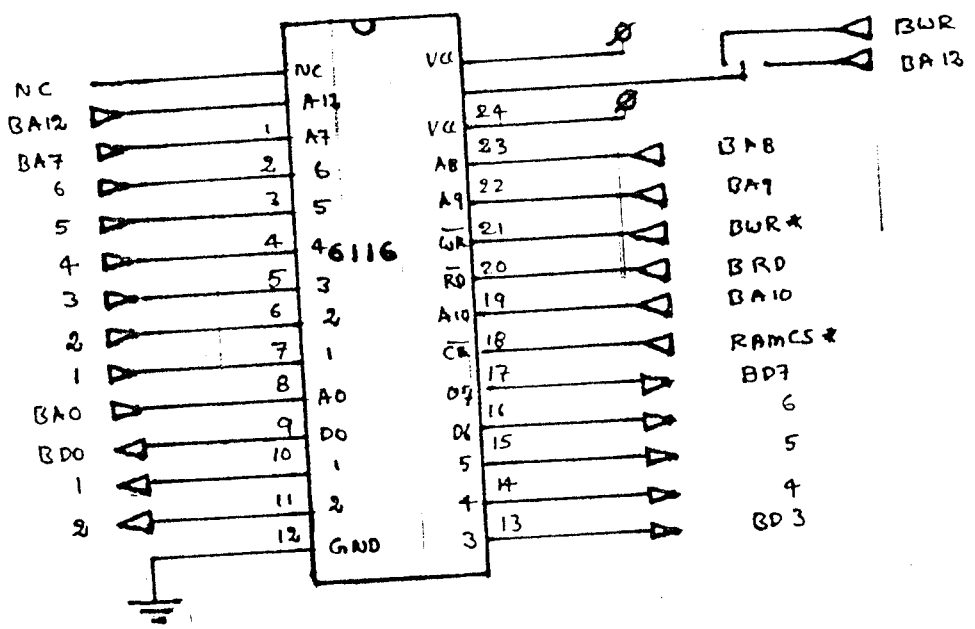


8085 INTER-FACING CIRCUIT 1.1.1



KEY BOARD INTERFACING CIRCUIT FIG. 1.1.1





MEMORY INTERFACING CIRCUIT FIG. 1.1.3

1.2 SOFTWARE DESCRIPTION

1.2.a SPEEDOMETER:

The pulses from the pulse shaping network are fed to programmable interval timer 8253. The counter 0 in 8253 is used for counting the number of pulses. The counter is loaded with data FFFF. For each pulse the counter is decremented by two.

The counter is initialised first. Decrementing the counter by a factor one as well as the delay routine for one second is executed simultaneously. After completion of one second delay, the counter is latched and the count value in the taken from the counter. Then the arithmetical operations are done over the count.

PRINCIPLE OF SPEEDOMETER:

The Speed calculation depends on the number of rotations of the wheel. For each rotation of the wheel the counter is decremented by two. The radius of the wheel is assumed as 10.6 cm.

Radius of the wheel (r) = 10.6 cm

r = 0.106 m.

The number of pulses generated for 1m distance is 3.

$$\text{Speed} = \frac{\text{Distance}}{\text{Time}} \quad \frac{\text{Km}}{\text{Hr}}$$

$$1 \text{ Km} = 1000 \text{ m}$$

$$1 \text{ Hr} = 3600 \text{ Sec.}$$

$$\frac{1 \text{ Km}}{1 \text{ Hr}} = \frac{1000 \text{ m}}{3600 \text{Sec}} = \frac{10}{36} \frac{\text{m}}{\text{s}}$$

$$\text{Speed} = (3.6) \left[\frac{\text{Distance}}{\text{Time}}\right] \text{KmpH}$$

Here time = 1 Sec.

$$\text{Speed} = (3.6) \text{ (Distance) KmpH}$$

$$= (3.6) \left[\frac{\text{Number of pulses}}{3}\right] \text{KmpH}$$

$$= \frac{3.6}{3} \text{ (Number of pulses) KmpH}$$

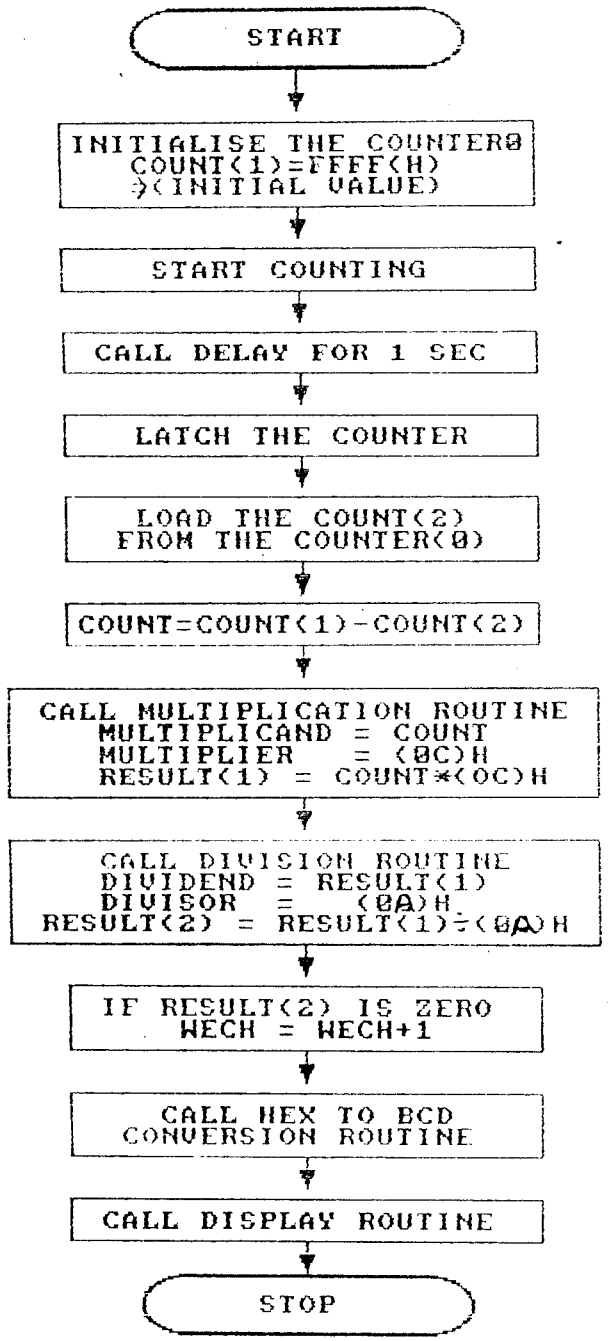
$$\text{Speed} = \frac{12}{10} \text{ (Number of pulses) KmpH}$$

For example,

Number of pulses = 80

$$\text{Speed} = \frac{12}{10} (80)$$

Speed = 96 KmpH



1.2.1 FLOW CHART FOR SPEED

1.2.b ODOMETER:

The pulses from decade counter is fed to the counter 1 of 8253. The counter is initialised with the data FFFF. For each pulse the counter is decremented by 1. The final count from the counter is loaded and the arithmetical operations are made over the count.

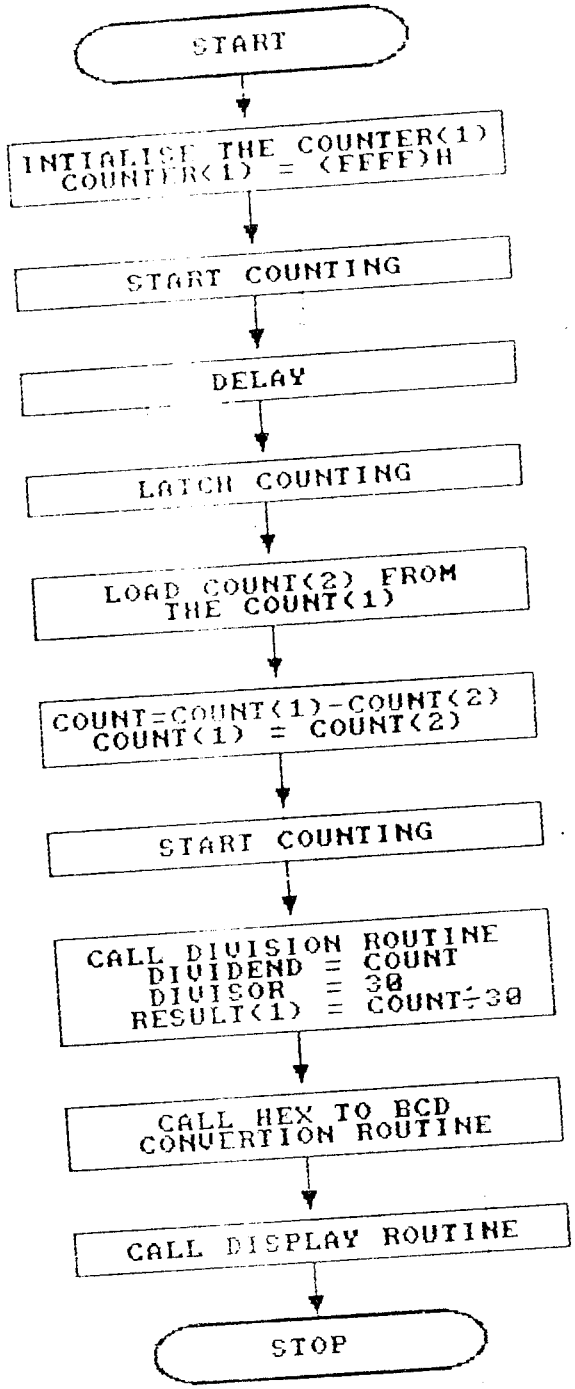
The calculation of distance is as follows

Here 0.3 pulses = 1 m

Distance travelled = Number of pulses $\left[\frac{10}{3} \right]$ m

Distance in Km = Number of pulses $\left[\frac{10}{3} \times \frac{1}{1000} \right]$ Km

Distance = Number of pulses $\left[\frac{1}{300} \right]$ Km



1.2.2 FLOW CHART FOR DISTANCE

1.2.c FAREMETER:

The pulses from decade counter is fed to the counter 1 of 8253. The counter is initialised with the data FFFF. For each pulse the counter is decremented by 1. The final count from the counter is loaded and the arithmetical operations are made over the count.

The calculations of distance travelled and fare is as shown below.

Here 0.3 pulses = 1 m

Distance travelled = Number of pulses $\left[\frac{10}{3} \right]$ m

Distance in Km = Number of pulses $\left[\frac{10}{3} \times \frac{1}{1000} \right]$ Km

Distance = Number of pulses $\left[\frac{1}{300} \right]$ Km

For 1000 m = 220 Ps

(ie) For 1000m, Fare = 220 Ps

Fare F1 = Distance in metres $\times \frac{220}{1000}$

= Distance in metres $\times \frac{22}{100}$

= [Number of pulses $\times \frac{10}{3}$] $\left[\frac{22}{100} \right]$

F1 = (Number of pulses) $\left[\frac{22}{30} \right]$

Perimeter of the wheel $= \frac{2x22}{7} r$

$= 2 \times \frac{22}{7} \times 0.106$

$= 0.6669$ m.

Therefore for one full rotation of the wheel the distance travelled is 0.6669 m $= 6.669 \times 10^{-4}$ km. From this rotation the total distance travelled can be calculated.

For each revolution of the wheel, two pulses are generated by the proximity switch. These pulses are counted by 8253.

Initially the 8253 counter 0 is loaded with data FFFF. For each revolution of the wheel the counter is decremented by two. As the counter starts counting one second delay is executed. After completing the one second delay, the final count of the counter is taken and is subtracted from FFFF which gives the count for one second.

Initial count = FFFF

[(Initial count - Final count) = Number of pulses/Delay]

Here delay is for one second.

Count for one second = Initial count - Final count.

Calculation of Waiting Charge:

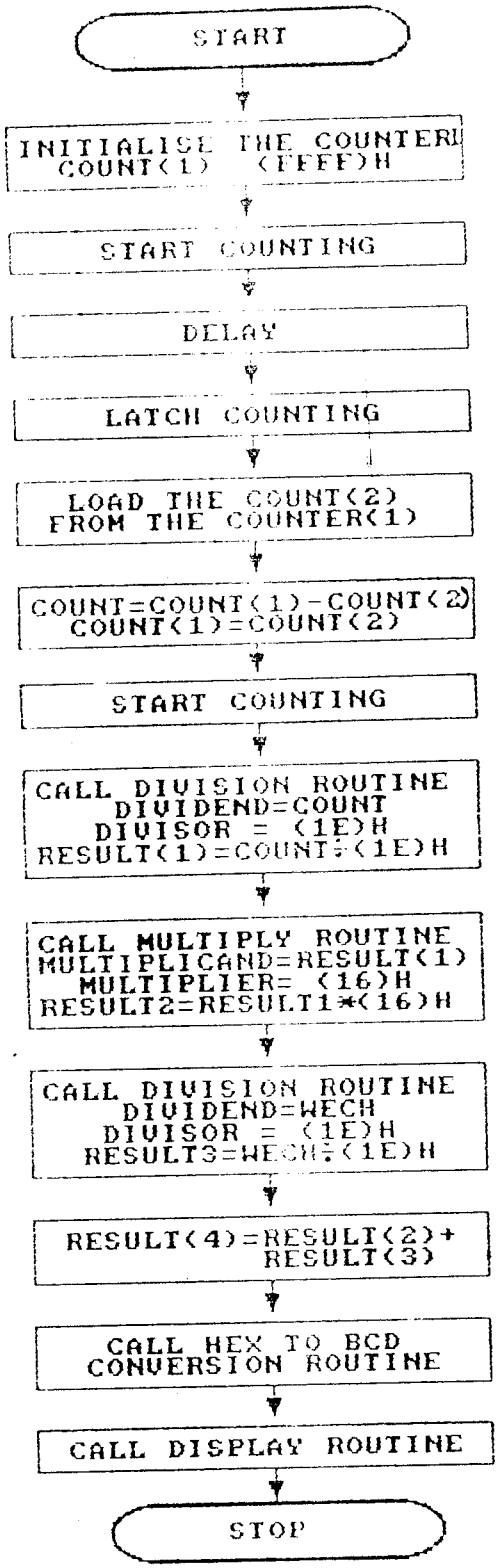
Waiting charge for 10 minutes = 20 Ps

For 1 minute = 2 Ps

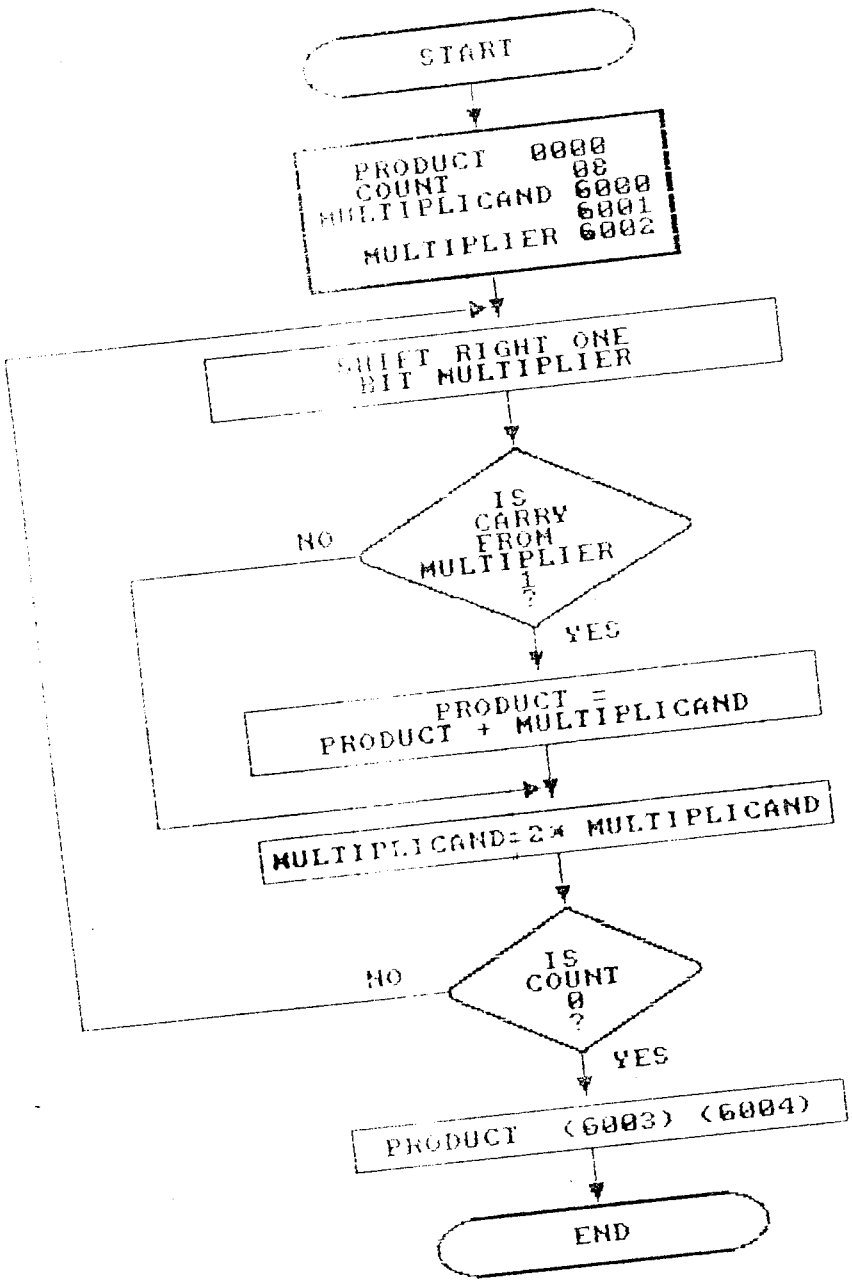
For 1 second = $\left[\frac{2}{60}\right]$ Ps

Fare F2 = (Number of Seconds) $\left[\frac{2}{60}\right]$

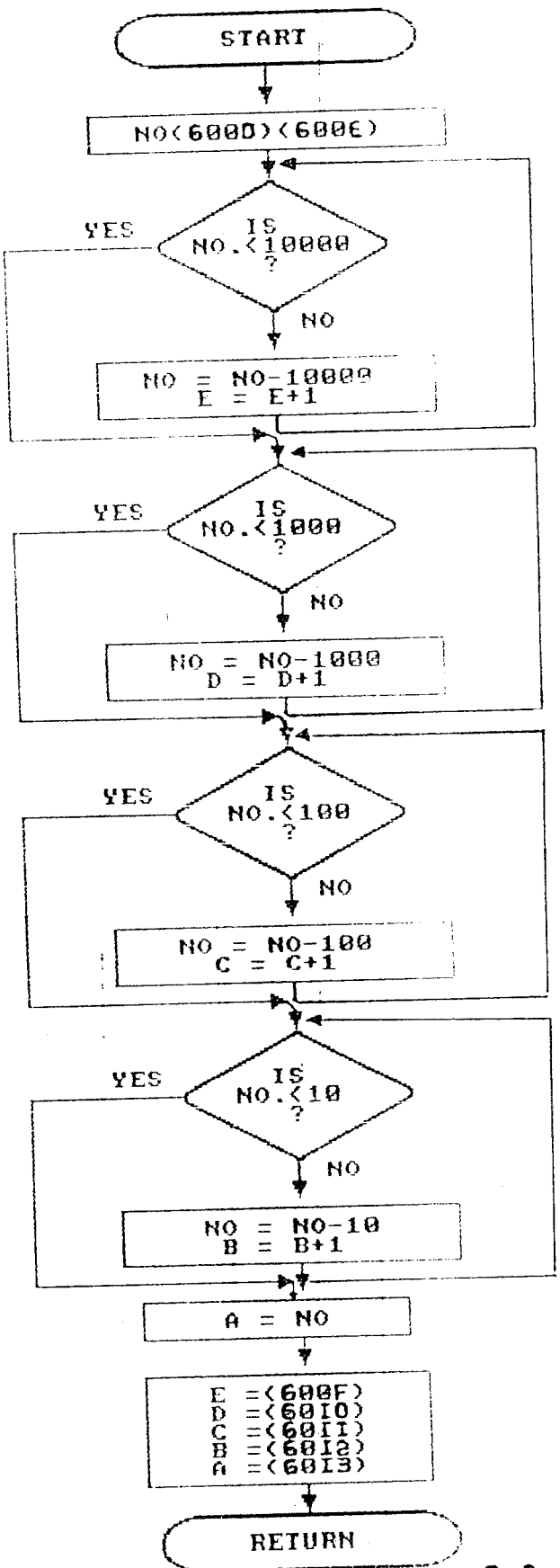
Total Fare F = F1 + F2.



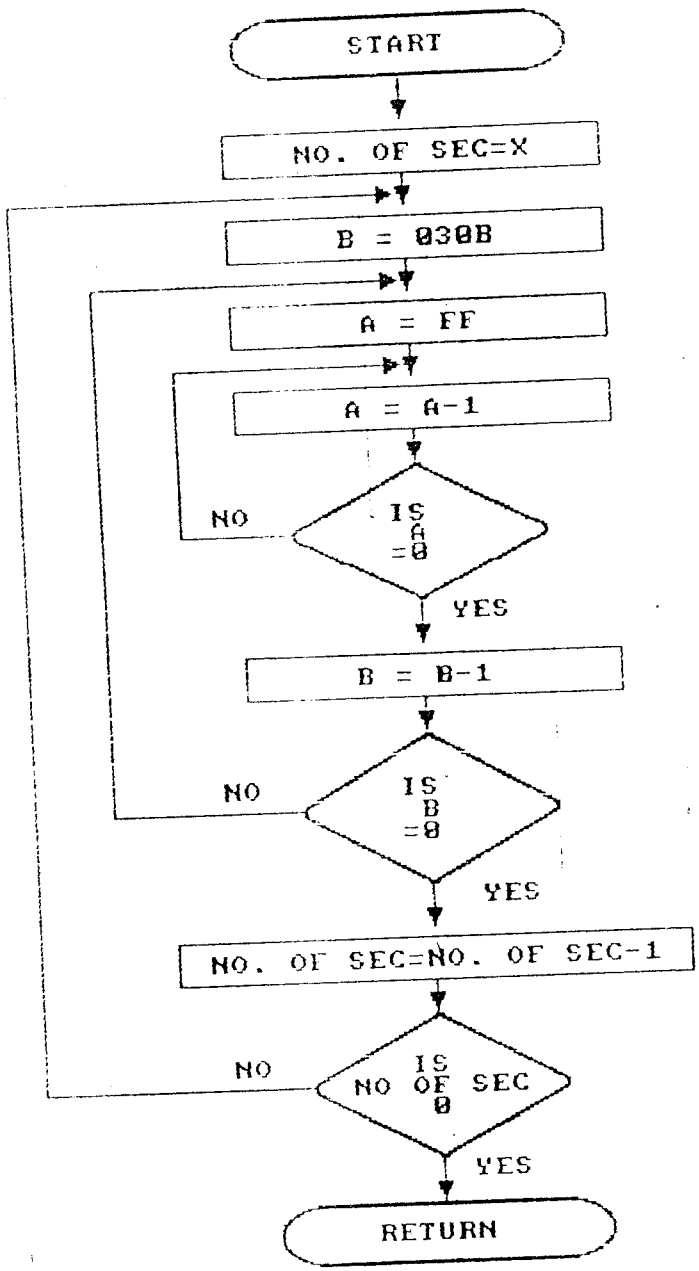
1.2.3 FLOW CHART FOR FARE



1.3.1 16*8 BIT MULTIPLICATION


START
NO(6000)(600E)
IS NO.<10000 ?
YES
NO
NO = NO-10000
E = E+1
IS NO.<1000 ?
YES
NO
NO = NO-1000
D = D+1
IS NO.<100 ?
YES
NO
NO = NO-100
C = C+1
IS NO.<10 ?
YES
NO
NO = NO-10
B = B+1
A = NO
E =(600F)
D =(60I0)
C =(60I1)
B =(60I2)
A =(60I3)
RETURN

1.3.2



1.3.3 DELAY FOR NO. OF SEC

HEXADECIMAL		MNEMONIC INSTRUCTION			COMMENTS
ADDRESS	INSTR.	LABLE	OPCODE	OPERAND	
0000	MVI A	00	3E	00	
0002	STA	631D	32	1D,63	
0005	STA	631E	32	1E,63	
0008	MVI A	00	3E	00	
000A	STA	6319	32	19,63	
000D	STA	631A	32	1A,63	
0010	MVI A	FF	3E	FF	
0012	STA	6313	32	13,63	
0015	STA	6314	32	14,63	
0018	MVI A	74	3E	74	
001A	OUT	E3	D3	E3	
001C	MVI A	FF	3E	FF	
001E	OUT	E1	D3	E1	
0020	OUT	E1	D3	E1	
0022	CALL	0210	CD	10,02	
0025	MVI B	OA	06	0A	
0027	PUSH B	-	C5	-	
0028	CALL	0500	CD	00,05	
002B	POP B	-	C1	-	
002C	DCR B	-	05	-	
002D	JNZ	0027	C2	27,00	
0030	CALL	0390	CD	90,03	
0033	MVI B	OA	06	0A	
0035	PUSH B	-	C5	-	
0036	CALL	0500	CD	00,50	
0039	POP B	-	C1	-	
003A	DCR B	-	05	-	
003B	JN Z	0035	C2	35,00	
003E	CALL	02D0	CD	D0,02	
0041	MVI B	0A	06	OA	
0043	PUSH B	-	C5	-	
0044	CALL	0500	CD	00,05	

HEXADECIMAL		MNEMONIC INSTRUCTION			COMMENTS
ADDRESS	INSTR.	LABLE	OPCODE	OPERAND	
0047	POP B	-	C1	-	
0048	DCR B	-	05	-	
0049	JNZ	0043	C2	43,00	
004C	JMP	0010	C3	10,00	
0100	LHLD	6000	2A	00,60	
0103	XCHG	-	EB	-	
0104	LDA	6002	3A	02,60	
0107	LXIH	0000	21	00,00	
010A	MVI B	08	06	08	
010C	RAR	-	1F	-	
0100	JNC	0111	D2	11,01	
0110	DAD D	-	19	-	
0111	XCHG	-	EB	-	
0112	DAD H	-	29	-	
0113	XCHG	-	EB	-	
0114	DCR B	-	05	-	
0115	JNZ	010C	C2	0C,01	
0118	SHLD	6003	22	03,60	
011B	RET	-	C9	-	
0120	LHLD	6007	2A	07,60	
0123	MOV C,L	-	4D	-	
0124	MOV B,H	-	44	-	
0125	MVI D	FF	16	FF	
0127	MVI E	FF	1E	FF	
0129	LDA	6005	3A	05,60	
012C	INX D	-	13	-	
012D	SUB C	-	91	-	
012E	STA	6005	32	05,60	
0131	LDA	6006	3A	06,60	
0134	SBB B	-	98	-	
0135	STA	6006	32	06,60	
0138	JNC	0129	D2	29,01	

HEXADECIMAL		MNEMONIC INSTRUCTION			COMMENTS
ADDRESS	INSTR.	LABLE	OPCODE	OPERAND	
013B	XCHG	-	EB	-	
013C	SHLD	6009	22	09,60	
013F	RET	-	C9	-	
0140	LXIB	2710	01	10,27	
0143	CALL	0180	CD	80,01	
0146	LDA	6014	3A	14,60	
0149	STA	600F	32	0F,60	
014C	LXIB	03E8	01	E8,03	
014F	CALL	0180	CD	80,01	
0152	LDA	6014	3A	14,60	
0155	STA	6010	32	10,60	
0158	LXIB	0064	01	64,00	
015B	CALL	0180	CD	80,01	
015E	LDA	6014	3A	14,60	
0161	STA	6011	32	11,60	
0164	LXIB	000A	01	0A,60	
0167	CALL	0180	CD	80,01	
016A	LDA	6014	3A	14,60	
016D	STA	6012	32	12,60	
0170	LDA	600D	3A	0D,60	
0176	RET	-	C9	-	
0180	LXIH	6014	21	14,60	
0183	MVI M	FF	36	FF	
0185	INR M	-	34	-	
0186	LDA	600D	3A	0D,60	
0189	SUB C	-	91	-	
018A	STA	600D	32	0D,60	
018D	LDA	600E	3A	0E,60	
0190	SBB B	-	98	-	
0191	STA	600E	32	0E,60	
0194	JNC	0185	D2	85,01	
0173	STA	6013	32	13,60	

HEXADECIMAL		MNEMONIC INSTRUCTION			COMMENTS
ADDRESS	INSTR.	LABLE	OPCODE	OPERAND	
0197	LHLD	600D	2A	0D,60	
019A	DAD B	-	09	-	
019B	SHLD	600D	22	0D,60	
019E	RET	-	C9	-	
01A0	LXI B	6013	01	13,60	
01A3	MVI H	12	26	12	
01A5	MVI D	85	16	85	
01A7	MVI E	05	1E	05	
01A9	LDAX B	-	0A	-	
01AA	MOV L,A	-	6F	-	
01AB	MOV A,D	-	7A	-	
01AC	OUT	C1	D3	C1	
01AE	MOV A,M	-	7E	-	
01AF	OUT	C0	D3	C0	
01B1	DCX B	-	15	-	
01B2	DCR D	-	1D	-	
01B3	DCR E	-	1D	-	
01B4	JNZ	01A9	C2	A9,01	
01B7	RET	-	C9	-	
0200	-	-	-	F3	
0201	-	-	-	60	
0202	-	-	-	B5	
0203	-	-	-	F4	
0204	-	-	-	66	
0205	-	-	-	D6	
0206	-	-	-	D7	
0207	-	-	-	70	
020D	-	-	-	F7	
0209	-	-	-	F6	
020A	-	-	-	77	
020B	-	-	-	C7	
020C	--	-	-	93	

HEXADECIMAL		MNEMONIC INSTRUCTION			COMMENTS
ADDRESS	INSTR.	LABLE	OPCODE	OPERAND	
020D	-	-	-	F3	
020E	-	-	-	97	
020E	-	-	-	17	
0210	MVI A	85	3E	85	
0212	OUT	C1	D3	C1	
0214	MVI A	F3	3E	F3	
0216	OUT	C0	D3	C0	
0218	MVI A	84	3E	84	
021A	OUT	C1	D3	C1	
021C	MVI A	97	3E	97	
021E	OUT	C0	D3	C0	
0220	MVI A	83	3E	83	
0222	OUT	C1	D3	C1	
0224	MVI A	97	3E	97	
0226	OUT	C0	D3	C0	
0228	MVI A	82	3E	82	
022A	OUT	C1	D3	C1	
022C	MVI A	37	3E	37	
022E	OUT	C0	D3	C0	
0230	MVI A	81	3E	81	
0232	OUT	C1	D3	C1	
0234	MVI A	D6	3E	D6	
0236	OUT	C0	D3	C0	
0238	MVI A	80	3E	80	
023A	OUT	C1	D3	C1	
023C	MVI A	00	3E	00	
023E	OUT	C0	D3	C0	
0240	LXI H	601F	21	1F,60	
0243	MVI M	2F	36	2F	
0247	OUT	E3	D3	E3	
0249	MVI A	FF	3E	FF	
0245	MVI A	34	3E	34	

HEXADECIMAL		MNEMONIC INSTRUCTION			COMMENTS
ADDRESS	INSTR.	LABLE	OPCODE	OPERAND	
0248	OUT	E0	D3	E0	
024D	OUT	E0	D3	E0	
024F	CALL	0500	CD	00,05	
0252	MVI A	04	3E	04	
0254	OUT	E3	D3	E3	
0256	LXI H	6000	21	00,60	
0258	IN	E0	DB	E0	
025A	MOV M,A	-	77	-	
025B	IN	E0	DB	E0	
025D	INX H	-	23	-	
025E	NOP	-	00	-	
025F	NOP	-	00	-	
0260	MOV M,A	-	77	-	
0261	LDA	6000	3A	00,60	
0264	MOV L,A	-	4F	-	
0265	MVI A	FF	3E	FF	
0267	SUB C	-	91	-	
0268	STA	6000	32	00,60	
026B	LDA	6001	3A	01,60	
026E	MOV B,A	-	47	-	
026F	MVI A	FF	3E	FF	
0271	SBB B	-	98	-	
0272	STA	6001	32	01,60	
0275	MVI A	0C	3E	0C	
0277	CALL	0100	CD	00,01	
027A	MVI A	0A	3E	0A	
027C	STA	6007	32	07,60	
027F	MVI A	00	3E	00	
0281	STA	6008	32	08,60	
0284	LDA	6003	3A	03,60	
0287	STA	6005	32	05,60	
028A	LDA	6004	3A	04,60	

HEXADECIMAL		MNEMONIC INSTRUCTION			COMMENTS
ADDRESS	INSTR.	LABLE	OPCODE	OPERAND	
028D	STA	6006	32	06,60	
0290	CALL	0120	CD	20,01	
0293	LDA	6009	3A	09,60	
0297	STA	600D	32	0D,60	
029A	LDA	600A	3A	0A,60	
029D	STA	600E	32	0E,60	
02A0	CALL	0140	CD	40,01	
02A3	MVI A	80	3E	80	
02A5	OUT	C1	D3	C1	
02A7	MVI A	D6	3E	D6	
02A9	OUT	C0	D3	C0	
02AB	CALL	01A0	CD	A0,01	
02AE	MVI A	81	3E	81	
02B0	OUT	C1	D3	C1	
02B2	MVI A	00	3E	00	
02B4	OUT	C0	D3	C0	
02B6	MVI A	82	3E	82	
02B8	OUT	C1	D3	C1	
02BA	MVI A	00	3E	00	
02BC	OUT	C0	D3	C0	
02BE	LXI H	601F	21	1F,60	
02C1	DCR M	-	35	-	
02C2	JNZ	0245	C2	45,02	
02C5	RET	-	C9	-	
02D0	MVI A	85	3E	85	
02D2	OUT	C1	D3	C1	
02D4	MVI A	97	3E	97	
02D6	OUT	C0	D3	C0	
02D8	MVI A	84	3E	84	
02DA	OUT	C1	D3	C1	
02DC	MVI A	77	3E	77	
02DE	OUT	C0	D3	C0	

HEXADECIMAL		MNEMONIC INSTRUCTION			COMMENTS
ADDRESS	INSTR.	LABLE	OPCODE	OPERAND	
02E0	MVI A		3E	83	
02E2	OUT		D3	C1	
02E4	MVI A		3E	77	
02E6	OUT		D3	CO	
02E8	MVI A		3E	82	
02EA	OUT		D3	C1	
02EC	MVI A		3E	17	
02EE	OUT		D3	CO	
02F0	CALL	0500	CD	00,05	
02F3	CALL	0500	CD	00,05	
02F6	MVI A		3E	44	
02F8	OUT		D3	E3	
02FA	LXI H	6315	21	15,63	
02FD	IN	E1	DB	E1	
02FF	MOV M,A	-	77	-	
0300	INX H	-	23	-	
0301	MOV M,A	-	77	-	
0302	LDA	6315	3A	15,63	
0305	MOV C,A	-	4F	-	
0306	LDA	6316	3A	16,63	
0309	MOV B,A	-	47	-	
030A	LDA	6313	3A	13,63	
030D	SUB C	-	91	-	
030E	STA	6005	32	05,60	
0311	LDA	6314	3A	14,63	
0314	SBB B	-	98	-	
0315	STA	6006	32	06,60	
0318	LDA	6315	3A	15,63	
031E	LDA	6316	3A	16,63	
0321	STA	6314	32	14,63	
0324	MVI A	1E	3E	1E	
031B	STA	6313	32	13,63	

HEXADECIMAL		MNEMONIC INSTRUCTION			COMMENTS
ADDRESS	INSTR.	LABLE	OPCODE	OPERAND	
0326	STA	6007	32	07,60	
0329	MVI A	00	3E	00	
032B	STA	6008	32	08,60	
032E	CALL	0120	CD	20,01	
0331	LDA	6009	3A	09,60	
0334	STA	6000	32	00,60	
0337	LDA	600A	3A	0A,60	
033A	STA	6001	32	01,60	
033D	MVI A	16	3E	16	
033F	STA	6002	32	02,60	
0341	CALL	0100	CD	00,01	
0344	LDA	6003	3A	03,60	
0347	MOV L,A	-	6F	-	
0348	LDA	6004	3A	04,60	
034B	MOV M,A	-	67	-	
034C	LDA	6319	3A	19,63	
034F	MOV E,A	-	5F	-	
0350	LDA	631A	3A	1A,63	
0353	MOV D,A	-	57	-	
0354	DAD D	-	19	-	
0355	SHLD	6319	22	19,63	
0358	SHLD	600D	22	0D,60	
035B	CALL	0140	CD	40,01	
035E	LDA	6010	3A	10,60	
0361	STA	600F	32	0F,60	
0364	LDA	6011	3A	11,60	
0367	STA	6010	32	10,60	
0368	MVI A	80	3E	80	
036C	OUT	C1	D3	C1	
026E	MVI A	17	3E	17	
0370	OUT	C0	D3	C0	
0372	CALL	01A0	CD	A0,01	

HEXADECIMAL		MNEMONIC INSTRUCTION			COMMENTS
ADDRESS	INSTR.	LABLE	OPCODE	OPERAND	
0375	MVI A	83	3E	83	
0377	OUT	C1	D3	C1	
0379	MVI A	04	3E	04	
037V	OUT	C0	D3	C0	
037D	RET	-	C9	-	
0390	MVI A	80	3E	80	
0392	OUT	C1	D3	C1	
0394	MVI A	04	3E	04	
0396	OUT	C0	D3	C0	
0398	MVI A	81	3E	81	
039A	OUT	C1	D3	C1	
039C	MVI A	F3	3E	F3	
039E	OUT	C0	D3	C0	
03A0	MVI A	82	3E	82	
03A2	OUT	C1	D3	C1	
03A4	MVI A	60	3E	60	
03A6	OUT	C0	D3	C0	
03A8	MVI A	83	3E	83	
03AA	OUT	C1	D3	C1	
03AC	MVI A	D6	3E	D6	
03AE	OUT	C0	D3	C0	
03B0	MVI A	84	3E	84	
03B2	OUT	C1	D3	C1	
03B4	MVI A	04	3E	04	
03B6	OUT	C0	D3	C0	
03B8	MVI A	85	3E	85	
03BA	OUT	C1	D3	C1	
03BC	MVI A	00	3E	00	
03BE	OUT	C0	D3	C0	
03C0	CALL	0500	CD	00,05	
03C3	CALL	0500	CD	00,05	
03C6	MVI A	44	3E	44	

HEXADECIMAL		MNEMONIC INSTRUCTION			COMMENTS
ADDRESS	INSTR.	LABLE	OPCODE	OPERAND	
03C8	OUT	E3	D3	E3	
03CA	LXI H	6315	21	15,63	
03CD	IN	E1	DB	E1	
03CF	MOV M,A	-	77	-	
03D0	IN	E1	DB	E1	
03D2	INX H	-	23	-	
03D3	MOV M,A	-	77	-	
03D4	LDA	6315	3A	15,63	
03D7	MOV C,A	-	4F	-	
03D8	MVI A	FF	3E	FF	
03DA	SUB C	-	91	-	
03DB	STA	6005	32	05,60	
03DE	LDA	6316	3A	16,63	
03E1	MOV B,A	-	47	-	
03E2	MVI A	FF	3E	FF	
03E4	SBB B	-	98	-	
03E5	STA	6006	32	06,60	
03E8	MVI A	1E	3E	1E	
03EA	STA	6007	32	07,60	
03ED	MVI A	00	3E	00	
03EF	STA	600D	32	08,60	
03F2	CALL	0120	CD	20,01	
03F5	LDA	631D	3A	1D,63	
03F8	MOV E,A	-	5F	-	
03F9	LDA	631E	3A	1E,63	
03FC	MOV D,A	-	57	-	
03FD	LHLD	6009	2A	09,60	
0400	DAD D	-	19	-	
0401	SHLD	631D	22	1D,63	
0404	SHLD	600D	22	0D,60	
0407	CALL	0140	CD	40,01	
040A	LDA	6010	3A	10,60	

HEXADECIMAL		MNEMONIC INSTRUCTION			COMMENTS
ADDRESS	INSTR.	LABLE	OPCODE	OPERAND	
040D	STA	600F	32	0F,60	
0410	LDA	6011	3A	11,60	
0413	STA	6010	32	10,60	
0416	LDA	6012	3A	12,60	
0419	STA	6011	32	14,60	
041C	CALL	01A0	CD	A0,01	
041F	MVI A	80	3E	80	
0421	OUT	C1	D3	C1	
0423	MVI A	F3	3E	F3	
0425	OUT	C0	D3	C0	
0427	MVI A	813E	3E	81	
0429	OUT	C1	D3	C1	
042B	MVI A	04	3E	04	
042D	OUT	C0	D3	C0	
042F	MVI A	84	3E	84	
0431	OUT	C1	D3	C1	
0433	MVI A	08	3E	08	
0435	OUT	C0	D3	C0	
0437	RET	-	C9	-	
0500	MVI D	02	16	02	
0502	LXI B	FFFF	01	FFFF	
0505	DCX D	-	0B	-	
0506	MOV A,L	-	79	-	
0507	ORA , B	-	B0	-	
0508	JNZ	0505	C2	05,05	
050B	DCR D	-	15	-	
050C	JNZ	0502	C2	02,05	
050F	RET	-	C9	-	

CHAPTER II

CONCLUSION

CHAPTER 2 CONCLUSION

We have succeeded in displaying speed, distance and fare alternately with constant delay. The fare cannot be constant. It may vary due to various reasons such as variation in petrol price etc. This difficulty is avoided by changing the software slightly to get the desired value of fare.

The idea of using optocounter to convert the rotations of the wheel into pulses was not used because the light source has to be replaced periodically. The light detector has to be prevented from the external sources and also it has poor mechanical strength. Considering all these factors, proximity switch is used for the purpose. The proximity switch operates accurately over a wide range of speed.

The interfacing and software had possessed many practical problems. We were successful in overcoming all these problems.

For future expansion and development the following parameters can be included in the project to make the system more sophisticated. The petrol consumption of the vehichle flow rate, Indication of fuel availability, Ampere rating and Radiator temperature indication.

CHAPTER III

BIBLIOGRAPHY

CHAPTER 3 BIBLIOGRAPHY

1. MICROPROCESSOR ARCHITECTURE, PROGRAMMING, AND APPLICATIONS - GOANKAR

2. INTRODUCTION TO MICROPROCESSORS - ADITYA P. MATHUR

CHAPTER 4 APPENDIX

DESCRIPTION OF CHIPS:

8085:

It is an 8 bit general purpose microprocessor. It has 16 line address bus and is capable of addressing 64 k of memory. Its operating frequency is 3 MHz (single phase clock). It has 40 pins and requires a power supply of +5V. It is an enhanced version of 8080 A. Its instruction set is upward compatible with that of 8080 A.

ADDRESS AND DATA BUS:

The address bus consists of A_0 - A_{15} out of which A_{15} - A_8 is unidirectional. A_0 - A_7 is bidirectional as it is multiplexed for data and it is also the lower order bus.

CONTROL AND STATUS SIGNAL:

This signals are usd to identify the nature of operation. They are

FIG 4-1-A Schematic to Generate Read/Write Control Signals for Memory and I/O

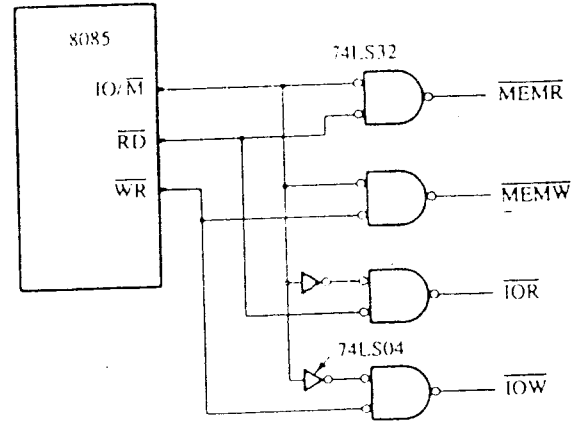
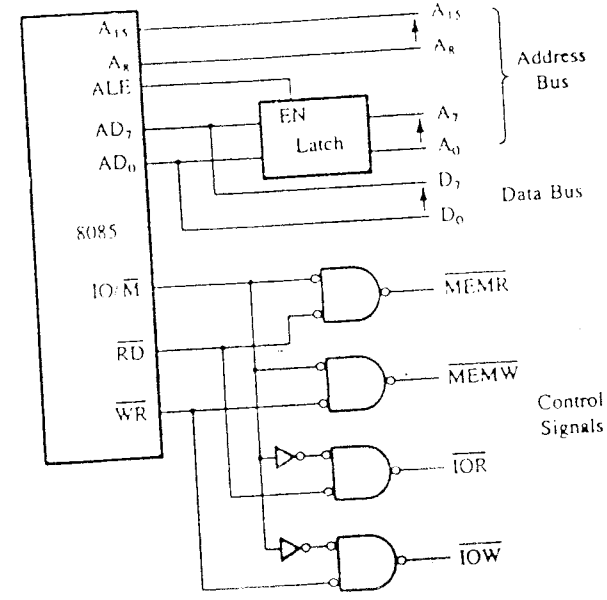


FIG 4-1-B 8085 Demultiplexed Address and Data Bus with Control Signals



ADDRESS LATCH ENABLE (ALE):

This is a positive going pulse generated every time the 8085 begins an operation. It indicates that the bits on AD_7 - AD_0 are address bits. This signal is used primarily to latch the low order address from the multiplexed bus and generate a separate set of eight address line A_7 - A_0.

READ ($\overline{RD}$):

This is a read control signal (active low). This signal indicates that the selected I/O or memory device is to be read and data are available on the data bus.

WRITE ($\overline{WR}$):

This is a write control signal (active low). This signal indicates that the data on the data bus are to be written into a selected memory or I/O location.

IO/$\overline{M}$:

This is a status signal used to differentiate between I/O and memory operations. When it is high, it indicates an I/O operation, when it is low, it indicates a memory operation. This signal is combined with RD and WR to generate I/O and memory control signals.

S1 AND S0:

These status signals, similar to IO/$\overline{M}$ can identify various operations, but they are rarely used in small systems.

8085 MACHINE CYCLE STATUS AND CONTROL SIGNALS

Machine Cycle	IO/$\overline{M}$	Status		Control Signals
		S1	S0	
Opcode Fetch	0	1	1	$\overline{RD}$ = 0
Memory Read	0	1	0	$\overline{RD}$ = 0
Memory write	0	0	1	$\overline{WR}$ = 0
I/O Read	1	1	0	$\overline{RD}$ = 0
I/O Write	1	0	1	$\overline{WR}$ = 0
INTR Acknowledge	1	1	1	$\overline{INTA}$ = 0
Halt	Z	0	0	$\overline{RD}$, $\overline{WR}$ = Z $\overline{INTA}$ = 1
Hold	Z	X	X	
Reset	Z	X	X	

CLOCK FREQUENCY:

X1, X2 : Crystal is connected at these two pins. The frequency is internally divided by two ; therefore, to operate a system at 3 MHz, the crystal should have a frequency of 6 MHz.

INTERRUPTS AND EXTERNALLY INITIATED OPERATIONS:

The 8085 has got five interrupt signals that can be used to interrupt a program execution.

INTR — Inter Request

This is used as a general purpose interrupt

RST 7.5

RST 6.5 — Restart Interrupt

RST 5.5

These are vectored interrupts and transfer the program control to specific memory location. Among these three the priority order is 7.5, 6.5 and 5.5.

TRAP — This is a non-maskable interrupt and has got the highest priority.

HOLD — This signal indicates that a peripheral such as a DMA controller is requesting the use of address and data buses.

$\overline{\text{INTA}}$ — This is an output signal and is used to acknowledge the interrupt.

HLDA — Hold acknowledge. This signal acknowledges the Hold request.

READY — This is also an output signal. This signal is used to delay the microprocessor Read or Write.

cycles until a slow responding signal goes low, the microprocessor waits for an integral number of clock cycles until it goes high.

GENERATING CONTROL SIGNALS:

RD since this signal is used both for reading memory and for reading an input device, it is necessary to generate two different read signals one for memory and another for input. Similarly two separate write signals must be generated.

Fig. (4.1) shows that four different control signals are generated by combining $\overline{RD}$, $\overline{WR}$ and IO/$\overline{M}$

ALU:

The Arithmatic logic unit (ALU) performs the computing functions, it includes the accumulator, the temporary register, the arithmetic and logic operations. The result is stored in the accumulator and flags are set or reset according to the result of operation. The descriptions and functions of the flags are as follows :

SIGN FLAG S:

After the execution of an arithmetic or logic operation, if bit D7 of the result is 1, the sign flag is set. This

flag is used with signal numbers. In a given byte, if D7 is 1, the number will be viewed as a negative number. If it is 0, the number will be considered as positive. In arithmetic operations with signed numbers, bit D7 is reserved for indicating the sign, and the remaining seven bits are used to represent the magnitude of a number.

ZERO FLAG (Z):

The Zero flag is set if the ALU operation results in 0, and the flag is reset if the result is not 0. This flag is modified by the results in the accumulator as well as in the other registers.

AUXILLARY CARRY FLAG (AC):

In an arithmetic operation, when a carry is generated by digit D3 and passed on to digit D4, the AC flag is set. The flag is used only internally for BCD operations, and is not available for the programmer to change the sequence of a program with a jump instruction.

PARITY FLAG (P):

After an arithmetic or logic operation, if the result has an even number of 1s, the flag is set. If it has an odd number of 1s, the flag is reset.

CARRY FLAG (CY):

If an arithmetic operation results in a carry the carry flag is set, otherwise it is reset.

EXECUTION:

The MPU places the memory address of the instruction of the address bus and it indicates the operation status on the status lines. MPU sends sthe MEMR signal to enable the memory, fetches the instruction byte and places it in the instruction decoder and also the MPU executes the instruction.

SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR [8085 A]:

* Single + 5V power supply.
* 100% software compatible with 8080 A.
* 1.3 micro seconds instruction cycle.
* On chip system controller, advanced cycle status information available for large system control.
* On chip clock generator (with external crystal, LC or RC Network.
* Four Vectored interrupt inputs (one is non-maskable) plus an 8080 A compatible interrupt.
* Serial In / Serial Out port.

* Decimal, binary and double precision arithmetic.
* Direct addressing capability to 64 k bytes of memory.

The 8085 A is complete 8 bit parallel central processing unit (CPU). Its instruction set is 100% software compatible with the 8080 A microprocessor, and it is designed to improve the present 8080 A's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's [8085 A (CPU), 8156 (RAM/IO) and 8355/8755 A (ROM/PROM/IO) while maintaining total system expandability.

The 8085 A incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080 A, thereby offering a high level of system integration.

The 8085 A uses a multiplexed data bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on - chip address latches of 8155/8156/8355/8755 A memory products allow a direct interface with the 8085 A.

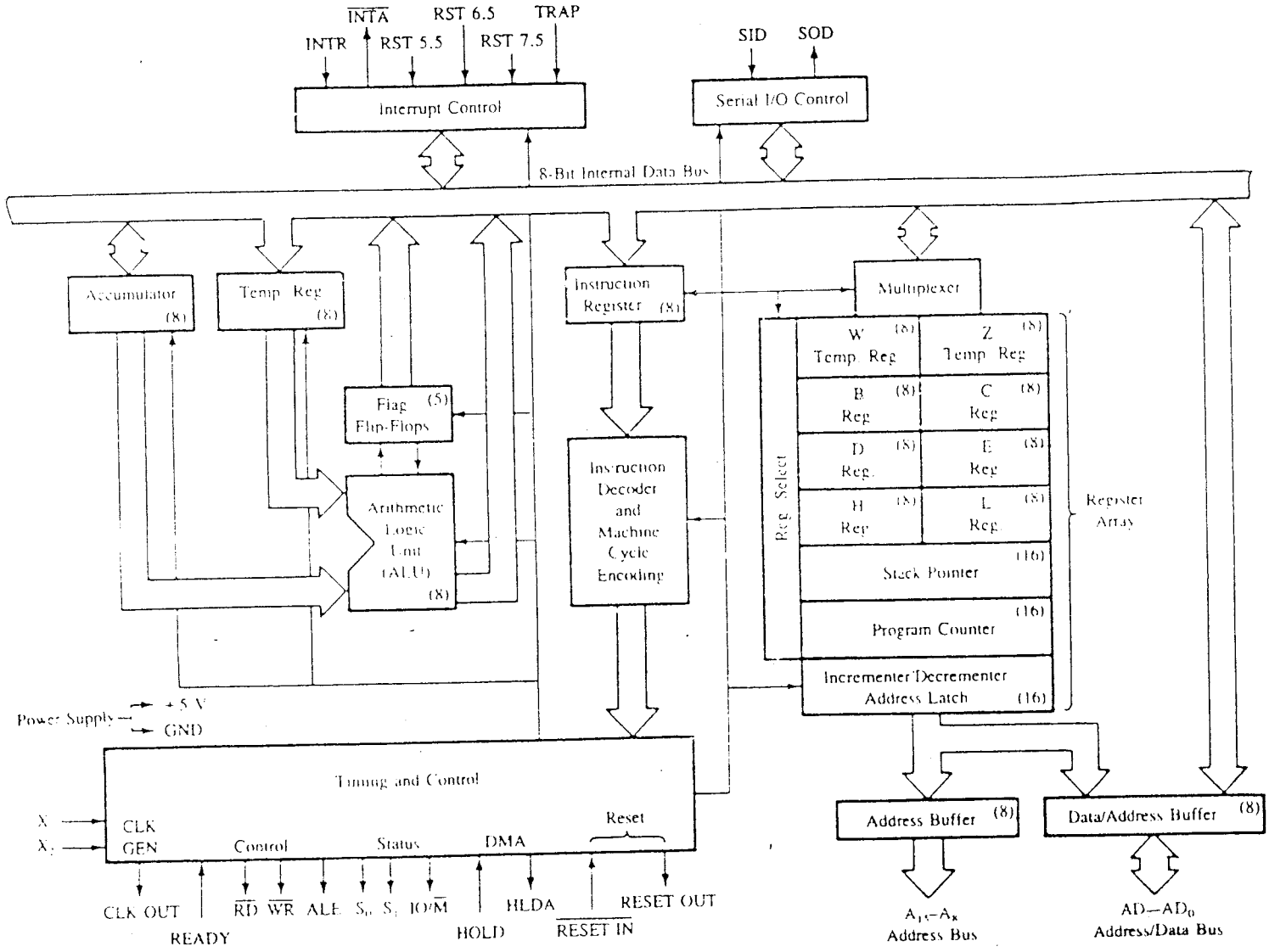
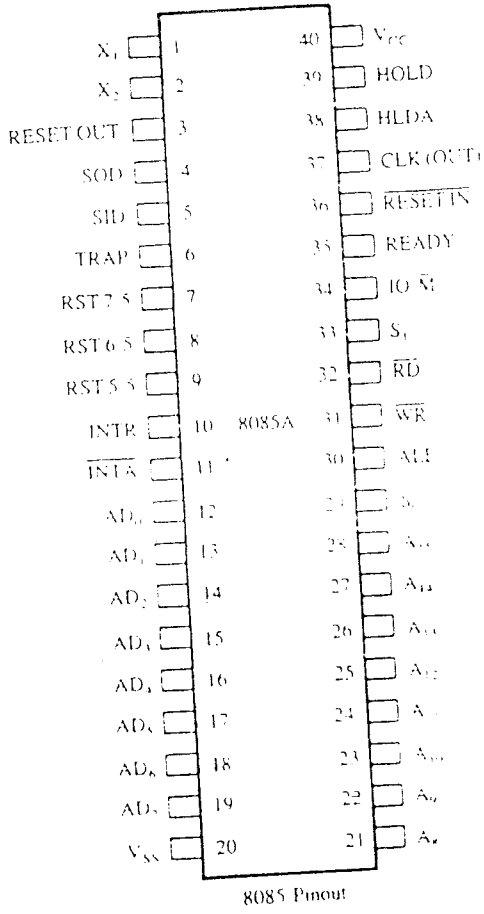


FIG. 4-2 The 8085A Microprocessor: Functional Block Diagram



8085 Pinout

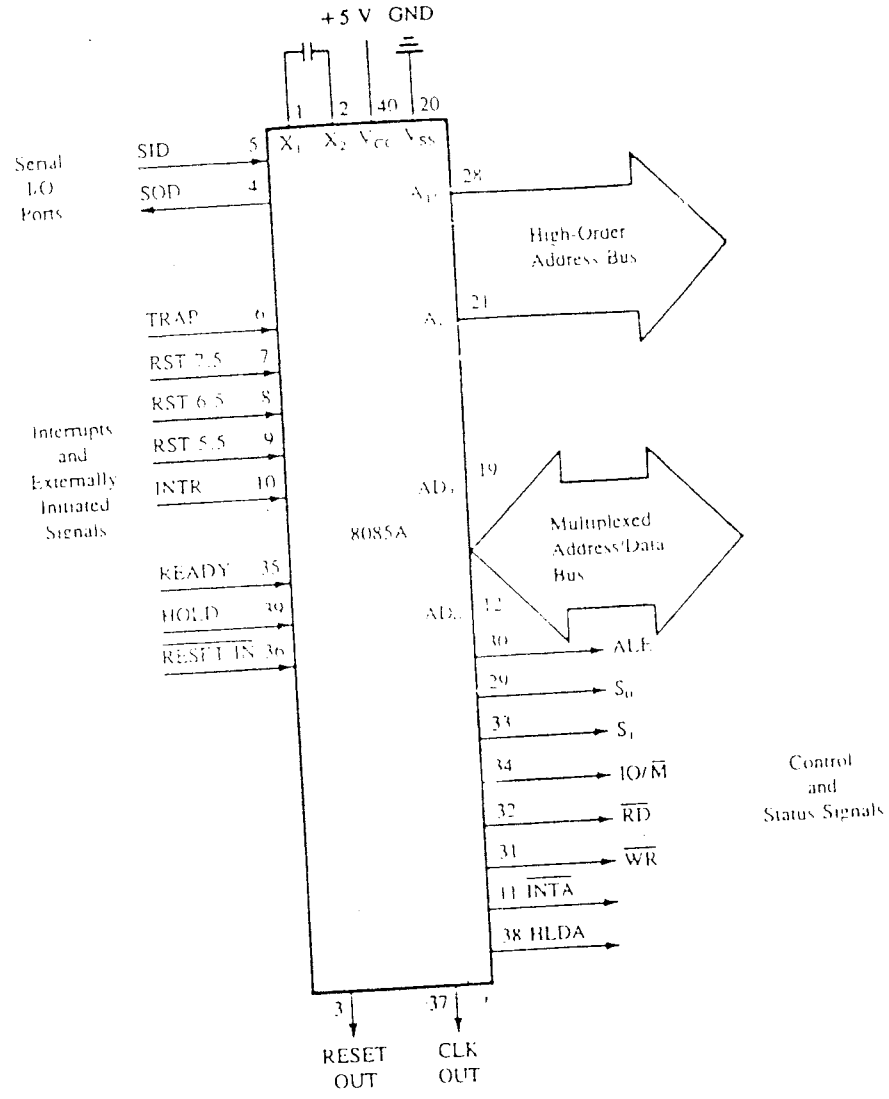


FIG. 4-3 The 8085 Microprocessor Pinout and Signals

THE 8253 (PROGRAMMABLE INTERVAL TIMER)

The 8253 . programmable interval timer / counter is functionally similar to the software designed counters and timers. it generates accurate time delays and can be used for applications such as a real time clock, an event counter, a digital one-shot, a square wave generator, and a complex waveform generator.

The 8253 includes three identical 16-bit counters that can operate independently in any one of the six modes. It is packaged in a 24-pin DIP and requires a single +5V power supply. To operate a counter, a 16-bit count is loaded in its register and, on command, it begins to decrement the count until it reaches 0. At the end of the count, it generates a pulse that can count either in binary or. In addition, a count can be read by the M-PU while the counter is decrementing.

8253 includes three counters (0,1 and 2), a data bus buffer, Read/write control logic and a control register. Each counter has two input signals-clock and gate-and one OUTPUT signal-OUT.

DATA BUS BUFFER

This tri-state, 8 bit, bi-directional buffer is connected to the data bus of the MPU.

CONTROL LOGIC

The control section has five signals: $\overline{RD}$ (Read), $\overline{WR}$ (Write) $\overline{CS}$ (Chip Select), and the address lines A0 and A_1. In the peripheral I/O mode, the RD and WR signals are connected to $\overline{IOR}$ and $\overline{IoW}$, respectively. In memory-mapped I/O, these are connected to $\overline{MEMR}$ (Memory read) and $\overline{MEMW}$ (Memory Write). Address lines A0 and A1 of the MPU are usually connected to lines A0 and A1 of the 8253 and CS is tied to a decoded address.

The control word register and counters are selected according to the signals on lines A0 and A1 as shown below.

A_1	A_0	Selection
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Register

CONTROL WORD REGISTER

This register is accessed when lines A_0 and A_1 are at logic 1. It is used to write a command word which specifies the counter to be used, its mode and either a Read or write operation. Howver the control word register is not available for a Read Operation.

MODE

The 8253 can operate in six different modes. The gate of a counter is used either to disable or enable counting.

PROGRAMMING THE 8253

The 8253 can be programmed to provide various types of outputs through write operations, or to check a count while counting through Read operations. The details of these operations are given below.

WRITE OPERATIONS

To initialize a counter, the following steps are necessary.

1. Write a control word into the control register.
2. Load the low-order byte of a count in the counter register.
3. Load the high-order byte of a count in the counter register.

With a clock (maximum 2 MHz) and an appropriate gate signal to one of the counters the above steps should start the counter and provide appropriate output according to the control word.

READ OPERATIONS:

In some applications, especially in event counters, it is necessary to read the value of the count in progress. This can be done by either of two methods. One method involves reading a count after initialising (stopping) the counter to be read. The second method involves reading a count while the count is in progress. (Known as reading on the fly).

In the first method, counting is stopped (or initialised) by controlling the gate input or the clock input of the selected counter, and two I/O read operations are performed by the MPV. The first I/O operation reads the low-order byte, and the second I/O operations reads the high-order byte.

8253 CONTROL WORD FORMAT

D7	D6	D5	D4	D3	D2	D1	D0
SC		R/L		M		C	CODE 0 = Binary 1 = BCD

D7	D6	Select Counter
0	0	0
0	1	1
1	0	2
1	1	Illegal

D5	D4	Read/ Load
0	0	Latch Counter
0	1	LSB only
1	0	MSB only
1	1	LSB first MSB next

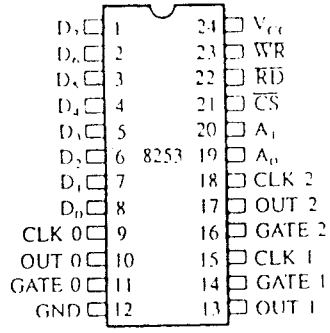
D3	D2	D1	Mode
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

GATE SETTINGS OF A COUNTER

Signal status / Modes	Low or Going low	Rising	High
0	Disables counting	-	Enables Counting
1	-	1. Initiates Counting	
		2. Resets output after next clock	-
2	1. Disables counting	1. Re loads Counter	Enables counting
	2. Sets output immediatelyhigh	2. Initiates counting	
3	1. Disables counting	Initiates counting	Enables Counting
	2. Sets output immediately high		
4	Disables counting	-	Enables Counting
5	-	Initiates counting	-

In the second method, an appropriate control word is written into the control register to latch a count in the input latch, and two I/O Read Operations are performed by the M.P.U.

Pin Configuration



Pin Names

D_7–D_0	Data Bus (8 Bit)
CLK N	Counter Clock Inputs
GATE N	Counter Gate Inputs
OUT N	Counter Outputs
$\overline{RD}$	Read Counter
$\overline{WR}$	Write Command or Data
$\overline{CS}$	Chip Select
A_0–A_1	Counter Select
V_{CC}	+5 Volts
GND	Ground

Block Diagram

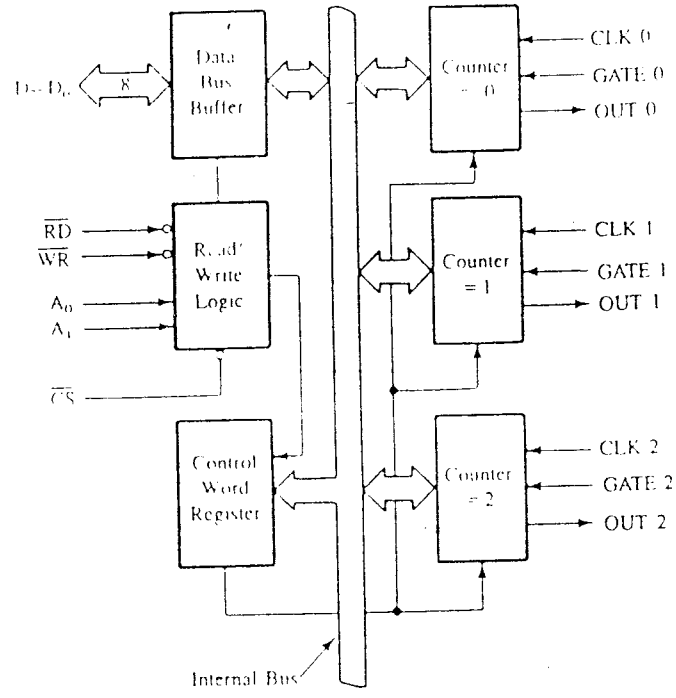


FIG 4-4 8253 Block Diagram

ADDRESS LOCATIONS

	ADDRESS
Counter 0	E0
Counter 1	E1
Counter 2	E2
Control register	E3

THE 8279 PROGRAMMABLE KEYBOARD / DISPLAY INTERFACE

The 8279 is a hardware approach to interfacing a matrix keyboard and a multiplexed display. The disadvantage of the software approach is that microprocessor is occupied for a considerable amount of time inchecking the keyboard and refreshing the display. The 8279 relieves the processor from these two tasks. The disadvantage of using 8279 is the cost. The trade-offs between the hardware approach and the software approach are the production cost vs the processor time and the software development cost.

The 8279 is a 40-pin device with two major segments. Keyboard and display. The keyboard segment can be connected to a 64-contact key matrix. Key board entries are debounced

and stored in the internal FIFO memory. While an interrupt signal is generated with each entry. The display segment can provide a sixteen - character scanned display interface with such devices as LEDS. This segment has 16 x 8 R/W memory (RAM), which can be used to read/write information for display purposes. This display can be set up either in right-entry or left entry format. The block diagram shows four major sections of the 8279 key board, scan, display and MPU interface. The function of these sections are described below.

KEYBOARD SECTION:

This section has 8 lines (RL_0 - RL_7) that can be connected to eight column of a keyboard, plus two additional lines. Shift and CNTL/STB (Control/Strobe). The status of the shift key and the control key can be stored along with a key closure. The keys are automatically debounced, and the key board can operate in two modes two key lockout or N-key rollover. In the two-key lockout mode, if two keys are pressed almost simultaneously, only the first key is recognized. In the N-key rollover mode, simultaneous keys are recognised and their codes are stored in the internal buffer, it can also be set up so that no key is recognized until only one key remains pressed.

The key board section also includes 8 x 8 FIFO RAM. The FIFO RAM consists of the eight key-board entries each is then read in the order of entries. The status logic keeps track of the number of entries and provides and IRQ. (Interrupt Request) signal when the FIFO is not empty.

SCAN SECTION

The Scan section has a Scan counter and four scan lines (SL_0 - SL_3). These four scan lines can be decoded using 4 to 16 decoder to generate sixteen lines for scanning. These lines can be connected to the rows of a matrix keyboard and the digit drivers of a multiplexed display.

DISPLAY SECTION:

The Display section has eight output lines divided into two groups A0 - A3 and B0 - B3. These lines can be used, either as a group of eight lines or as two groups of four in conjunction with the scan lines for a multiplexed display. The display can be blanked by using the BD line. This section includes 16 x 8 display RAM. The MPU can read from or write into any of these registers.

MPU INTERFACE SECTION:

This section includes eight bi-directional data lines (DB0 - DB7) one Interrupt Request line (IRQ), and six lines for interfacing, including the buffer address line (A0).

When A0 is high signals are interpreted as control words or status ; when A0 is low, signals are interpreted as data. The IRQ line goes high whenever data entries are stored in the FIFO. This signal is used to interrupt the MPU to indicate the availability of data.

PROGRAMMING THE 8279:

The 8279 is a complex device that can accept eight different commands to perform various function.

The initial commands can specify,

1. Left of Right entry and key rollover.
2. Clock frequency Prescaler.
3. Starting address and incrementing mode of the FIFO RAM.
4. RAM address to read and write data and incrementing mode.
5. Blanking format.

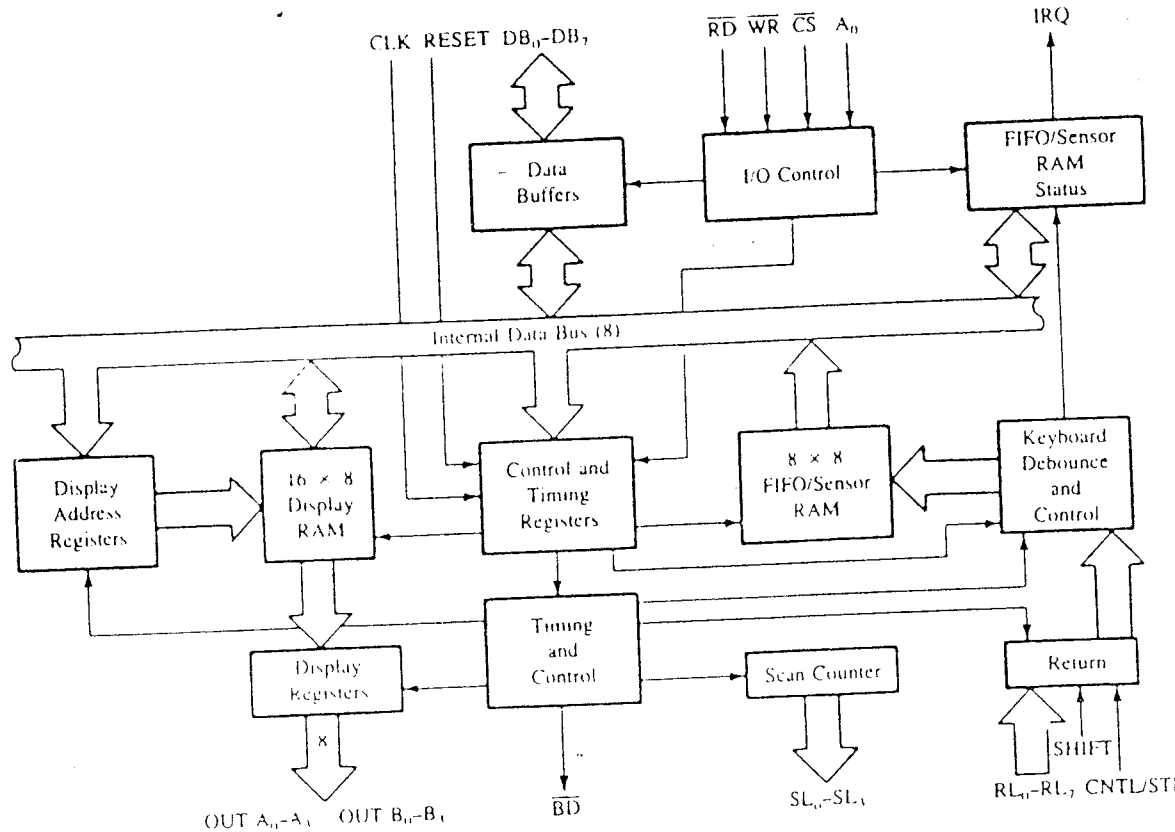
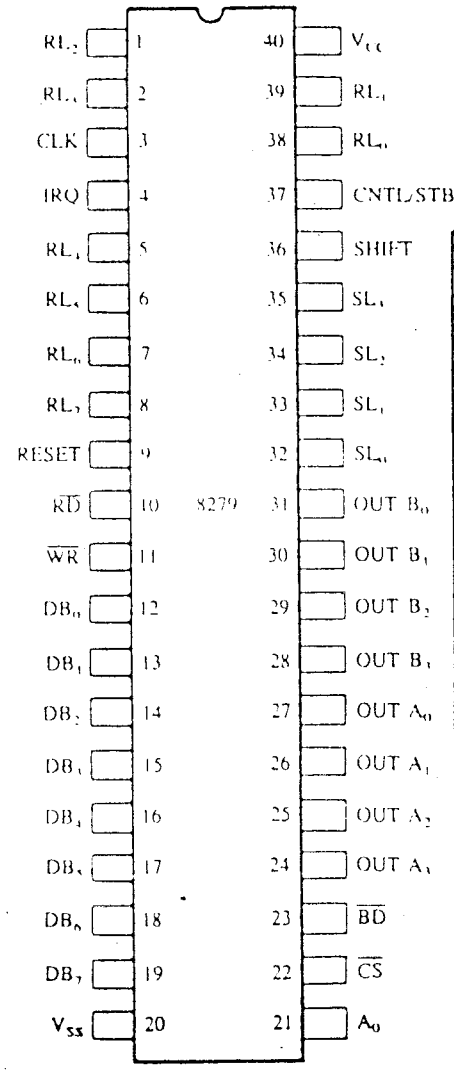


FIG 4-5 The 8279 Logic Block Diagram

Pin Configuration



Pin Names

DB_{0-7}	I/O	Data Bus (Bidirectional)
CLK	I	Clock Input
RESET	I	Reset Input
$\overline{CS}$	I	Chip Select
$\overline{RD}$	I	Read Input
$\overline{WR}$	I	Write Input
A_0	I	Buffer Address
IRQ	O	Interrupt Request Output
SL_{0-3}	O	Scan Lines
RL_{0-7}	I	Return Lines
SHIFT	I	Shift Input
CNTL/STB	I	Control Strobe Input
$OUT A_{0-3}$	O	Display (A) Outputs
$OUT B_{0-3}$	O	Display (B) Outputs
$\overline{BD}$	O	Blank Display Output

Logic Symbol

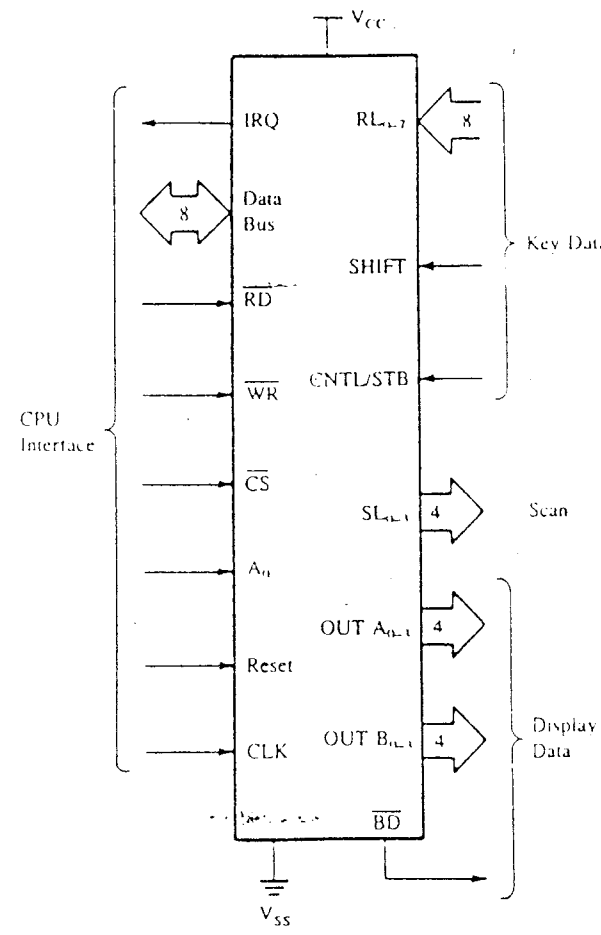


Fig. 4.6 The 8279 Logic Pinout

6116:

As microprocessor operates at high speed the memory that the microprocessor access must be capable of operating at the speed of microprocessor. In earlier days of computers main memories were constructed from small iron doughnuts called magnetic cores. The modern use of magnetic core memory is limited to extremely specialised applications. To this day the main memory in computers is still often called core memory even though it has long since been replaced by IC memories.

Read/write main memory devices are called RAM's The RAM's are volatile memory devices. RAM's are used as temporary storage for programs and data loaded into the computer from mass memories.

There are two types of RAMs, static and dynamic RAMs. Once a bit of information is written into a static RAM no further action is required to assume that it is not lost Dynamic RAMs are constant from MOS capacitors. When a logic 1 is stored in a dynamic RAM cell, MOS capacitor is charged to a logic 1 level. When a logic 0 is stored in a dynamic RAM cell, a MOS capacitor is discharged to 0V. All capacitors suffer from leakage current. In a matter of a few milliseconds the logic 1 stored on the MOS capacitor may discharge to a

logic 0 level. Because of these leakage it's discharge memories must be 'refreshed' at least once every few milliseconds. The refresh process will read the logic level stored in a MOS capacitor memory cell, and then rewrite it.

Because static RAMs do not require refreshing, they are often used in simple microprocessor applications, static RAMs have two major disadvantages.

1. They are limited to small storage capacities. DFF require much space on the surface of an IC. This greatly limits the number of memory cells that can be integrated into a single chip. One or two circuit boards of static RAM must be used to achieve the same storage capacity of eight dynamic RAM IC's
2. Because more ICs are required to gain the same storage capacity, static RAMs, tend to consume great amounts of power. As power supplies grown in capacity, they also increase in price, size, weight.

6116 uses 16 k D flipflops for its storage cells. These flipflops are organised in 2 k groups of 8. 6116 has 11 address pins 2^{11} = 2 k unique memory location. There are 8 bi-directional pins. The data input output lines are buffered on the input and driven by three-state drivers on the output. This tells us that the input out lines are capable

of going to high Z. The power requirement is +5V and this makes it compatible with TTL and microprocessor circuitry. The control bus input are OE (Output Enable). WE (Write Enable) and CS (Chip Select) which are active low the read operation will occur when chip select and output enable are at active-low levels and the write enable input is at an inactive high level. The write operation will occur when both the chip select and write enable inputs are active low.

BUFFER:

Buffer is a logic circuit which amplifies the current or power. It has one input line and one output line. The logic level of the output is the same as that of the input, logical input provides logical 1 output. The buffer is used primarily to increase the driving capability of a logic circuit. It is also known as driver.

The buffer is commonly used to increase the driving capability of the data bus and address bus.

74LS244 is a tristate buffer which is known as bus driver, which is used to drive the address bus so it is a unidirectional buffer. 74LS245 is a bidirectional buffer, is also called as octal bus transceiver. This is used to drive data bus thus justifying its bidirectional driving capability.

DM54LS244/DM74LS244
Octal TRI-STATE® Buffers/Line Drivers/Line Receivers

General Description

These buffers/line drivers are designed to improve both the performance and PC board density of TRI-STATE buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs and can be used to drive terminated lines down to 133Ω.

Features

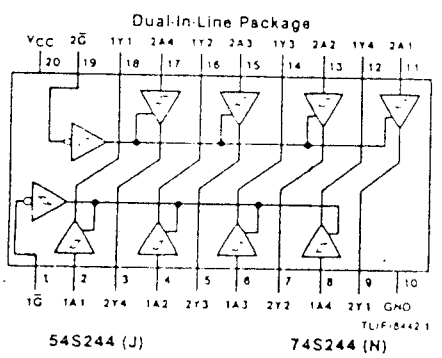
- TRI-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at inputs improves noise margins
- Typical I_{OL} (sink current)
  - 54LS 12 mA
  - 74LS 24 mA
- Typical I_{OH} (source current)
  - 54LS − 12 mA
  - 74LS − 15 mA
- Typical propagation delay times
  - Inverting 10.5 ns
  - Noninverting 12 ns
- Typical enable/disable time 18 ns
- Typical power dissipation (enabled)
  - Inverting 130 mW
  - Noninverting 135 mW

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram



54S244 (J) 74S244 (N)

Function Table

$\overline{G}$	A	Y
L	L	L
L	H	H
H	X	Z

L = Low Logic Level
H = High Logic Level
X = Either Low or High Logic Level
Z = High Impedance

DM54LS245/DM74LS245 TRI-STATE® Octal Bus Transceiver

General Description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

Features

- Bi-directional bus transceiver in a high-density 20-pin package
- TRI-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at bus inputs improve noise margins
- Typical propagation delay times, port-to-port 8 ns
- Typical enable/disable times 17 ns
- I_{OL} (sink current)
  - 54LS 12 mA
  - 74LS 24 mA
- I_{OH} (source current)
  - 54LS − 12 mA
  - 74LS − 15 mA

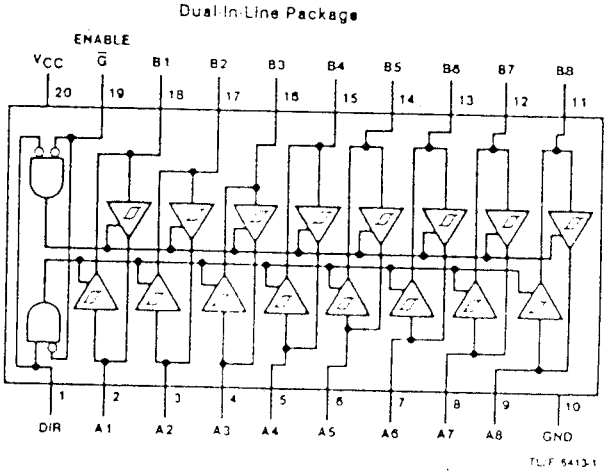
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	
DIR or $\overline{G}$	7V
A or B	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/5413-1

54LS245 (J) 74LS245 (N)

Function Table

Enable $\overline{G}$	Direction Control DIR	Operation
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = high level, L = low level, X = irrelevant

74LS139:

74LS139 comprises two separate two-line-to-four line decoders in a single package. The active low enable input can be used as a data line in demultiplexing applications. The decoder is fully buffered inputs, presenting only one normalised load to its driving circuit. All inputs are clamped with high performance schottky diode to suppress line-ringing and simplify system design. The delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible. The typical propagation delay is 21ns.

74LS373:

The eight latches of 74LS373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

DM54LS138/DM74LS138, DM54LS139/DM74LS139 Decoders/Demultiplexers

General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The LS138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The LS139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

Features

- Designed specifically for high-speed:
  - Memory decoders
  - Data transmission systems
- LS138 3-to-8-line decoders incorporates 3 enable inputs to simplify cascading and/or data reception
- LS139 contains two fully independent 2-to-4-line decoders/demultiplexers
- Schottky clamped for high performance
- Typical propagation delay (3 levels of logic)
  - LS138 21 ns
  - LS139 21 ns
- Typical power dissipation
  - LS138 32 mW
  - LS139 34 mW

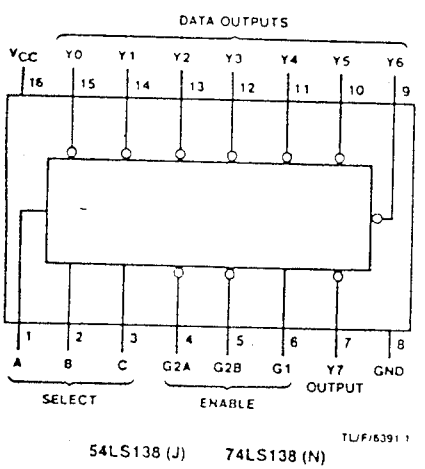
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

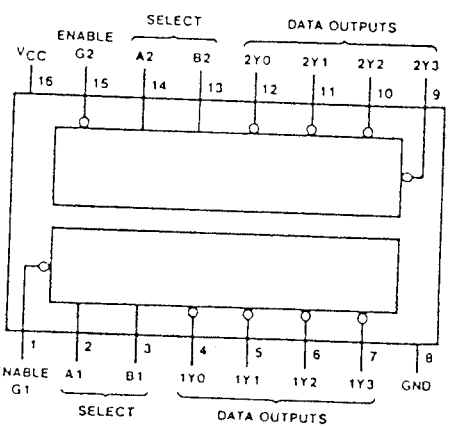
Dual-In-Line Package



TL/F/6391-1

54LS138 (J) 74LS138 (N)

Dual-In-Line Package



TL/F/6391-2

54LS139 (J) 74LS139 (N)

DM54LS373/DM74LS373, DM54LS374/DM74LS374 TRI-STATE® Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the DM54/74LS373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

(Continued next page)

Features

- Choice of 8 Latches or 8 D-Type Flip-Flops in a Single Package
- TRI-STATE Bus-Driving Outputs
- Full Parallel-Access for Loading
- Buffered Control Inputs
- Clock Enable Input Has Hysteresis to Improve Noise Rejection
- P-N-P Inputs Reduce D-C Loading on Data Lines

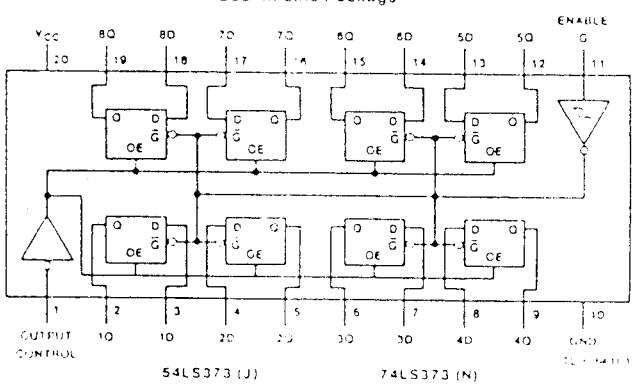
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

Dual-In-Line Package



2732A
32K (4K x 8) PRODUCTION AND UV ERASABLE PROMS

- 200 ns (2732A-2) Maximum Access Time ... HMOS*-E Technology
- Compatible with High-Speed Microcontrollers and Microprocessors ... Zero WAIT State
- Two Line Control
- 10% V_{CC} Tolerance Available
- Low Current Requirement
  - −100 mA Active
  - −35 mA Standby
- Intelligent Identifier™ Mode
  - −Automatic Programming Operation
- Industry Standard Pinout ... JEDEC Approved 24 Pin Ceramic and Plastic Package

(See Packaging Spec. Order # 221369)

The Intel 2732A is a 5V-only, 32,768-bit ultraviolet erasable (cerdip) Electrically Programmable Read-Only Memory (EPROM). The standard 2732A access time is 250 ns with speed selection (2732A-2) available at 200 ns. The access time is compatible with high performance microprocessors such as the 8 MHz iAPX 186. In these systems, the 2732A allows the microprocessor to operate without the addition of WAIT states.

The 2732A is currently available in two different package types. Cerdip packages provide flexibility in prototyping and R & D environments where reprogrammability is required. Plastic DIP EPROMs provide optimum cost effectiveness in production environments. Inventoried in the unprogrammed state, the P2732A is programmed quickly and efficiently when the need to change code arises. Costs incurred for new ROM masks or obsoleted ROM inventories are avoided. The tight package dimensional controls, inherent non-erasability, and high reliability of the P2732A make it the ideal component for these production applications.

An important 2732A feature is Output Enable ($\overline{OE}$) which is separate from the Chip Enable ($\overline{CE}$) control. The $\overline{OE}$ control eliminates bus contention in microprocessor systems. The $\overline{CE}$ is used by the 2732A to place it in a standby mode ($\overline{CE}$ = V_{IH}) which reduces power consumption without increasing access time. The standby mode reduces the current requirement by 65%; the maximum active current is reduced from 100 mA to a standby current of 35 mA.

*HMOS is a patented process of Intel Corporation.

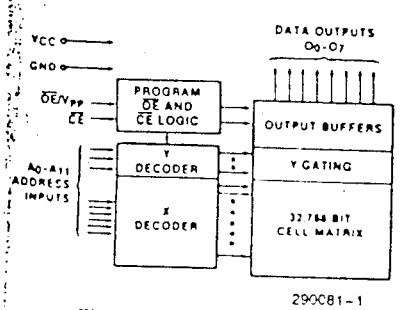


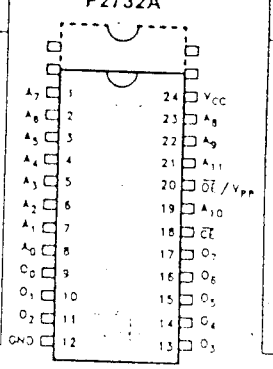
Figure 1. Block Diagram

Pin Names

A_0-A_{11}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable/V_{PP}
O_0-O_7	Outputs

27128 27128A	2764 2764A 27C64 87C64	2716
V_{PP}	V_{PP}	
A_{12}	A_{12}	
A_7	A_7	A_7
A_6	A_6	A_6
A_5	A_5	A_5
A_4	A_4	A_4
A_3	A_3	A_3
A_2	A_2	A_2
A_1	A_1	A_1
A_0	A_0	A_0
O_0	O_0	O_0
O_1	O_1	O_1
O_2	O_2	O_2
GND	GND	GND

2732A
P2732A



2716	2764 2764A 27C64 87C64	27128 27128A
	V_{CC} $\overline{PGM}$	V_{CC} $\overline{PGM}$
V_{CC}	N.C.	A_{13}
A_8	A_8	A_8
A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$ ALE/$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7
O_6	O_6	O_6
O_5	O_5	O_5
O_4	O_4	O_4
O_3	O_3	O_3

NOTE:
Intel "Universal Site" compatible EPROM configurations are shown in the blocks adjacent to the 2732A pins.

Figure 2. Cerdip/Plastic DIP Pin Configuration

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

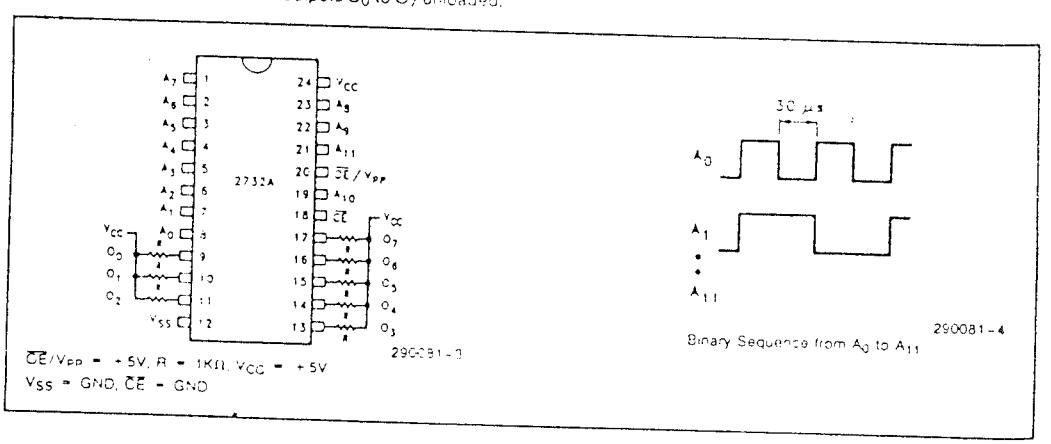
READ OPERATION

D.C. CHARACTERISTICS

Electrical Parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for:

Symbol	Parameter	TD2732A LD2732A		Test Conditions
		Min	Max	
I_{SB}	V_{CC} Standby Current (mA)		45	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC1}(1)	V_{CC} Active Current (mA)		150	$\overline{OE} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature (mA)		125	$\overline{OE} = \overline{CE} = V_{IL}$, $V_{PP} = V_{CC}$, $T_{Ambient} = 85°C$

NOTE:
1. Maximum current value is with outputs O_0 to O_7 unloaded.



EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITONS

Type	Operating Temperature	Burn-In 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

2732A Versions

Speed Versions	Packaging Options	
	Cerdip	Plastic
−2	Q	
STD	Q, T, L	
−3	Q	
−4	Q, T, L	
−20	Q	
−25	Q, T, L	
−30	Q	
−45	Q, T, L	