Digital Phase Meter

Project Work

SUBMITTED BY

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In partial fulfilment of the requirements
for the award of the degree of
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Department of Electronics and Communication Engineering
Kumaraguru College of Technology
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CERTIFICATE

This is to Certify that the project entitled

Digital Phase Meter

has been Submitted by

Mr. Binoy Vithayathil, T. Rajeev Kumar Ramdas, A. Ravichandra Reddy.

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During the academic year 1991 - '92

Guide

Head of the Dept.

Certified that the Candidate was examined by us in the Project–work Viva–Voce Examination held on .....

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OVERVIEW

Phase meters are rare instruments. Even in the laboratory of audio and Hi-fi Engineers and enthusiasts these instruments are difficult to be found. Perhaps that is because until the advent of reliable digital techniques it was fairly difficult to design an accurate direct reading phasemeter. In the 1970's the phasemeters had an accuracy of about 3 degrees from 10 Hz to 30 KHz. Clearly for modern audio equipment, that is no longer acceptable. Another reason may be that a phasemeter is a fairly specialized instrument. Many engineers and technicians measure phase shift with the aid of Lissaqious figures which does not give very accurate results either.

The phase meter presented in this project is accurate to within 0.5 degrees over frequency range 10 Hz to 20 KHz.

1.1. What is Phase?

When a sinusoidal signal is input to a device, It arrives at the output of the device only after a certain time period. This delay is defined as the phase difference between two signals. This delay between input and output may be expressed as a proportion of the sine wave cycle, usually in degrees, one cycle is 360^{o}, one half cycle is 180^{o} etc.

So the phase difference between two signals will vary from $0\text{-}360^{o}$.

Phase is a notation in which the time of one period of a sine wave is divided into 360^{o}. It is a relative quantity, and although it can be defined with respect to any reference point in a cycle, it is convenient to start (0^{o}) with the upward, or positive going, zero crossing and to end (360^{o}) at precisely the same point at the beginning of the next cycle. (Fig. 1.1). Phase shift expresses in degrees the fraction of a period or wavelength by which a single frequency component is shifted in the time doman. For example a phase shift of 90^{o} corresponds to a shift of 1.4th period. For different frequencies this translates into different time shifts.

In the fig (1.2) shown the output signal lags in phase with respect to the input signal and the input signal leads in phase with respect to the output signal.

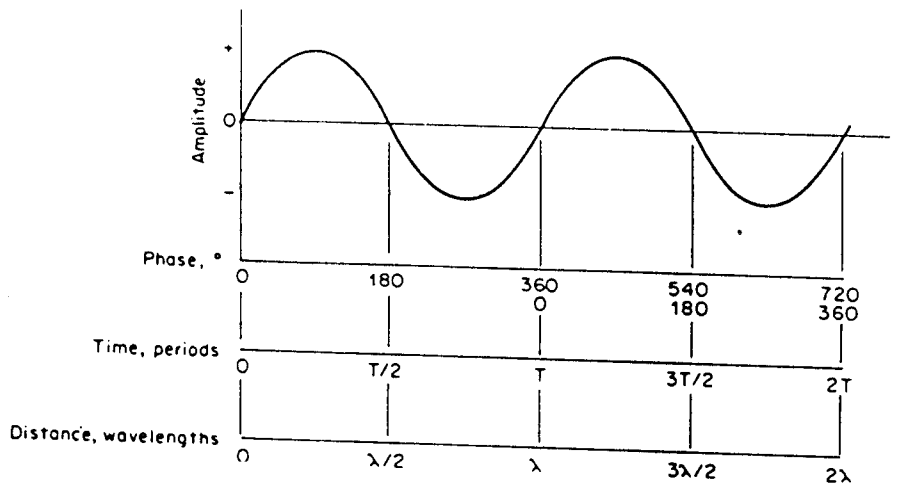


FIG. 1.1
RELATIONSHIP BETWEEN THE PERIOD (T) AND WAVELENGTH OF A SINUSOIDAL WAVEFORM AND PHASE EXPRESSED IN DEGREES.

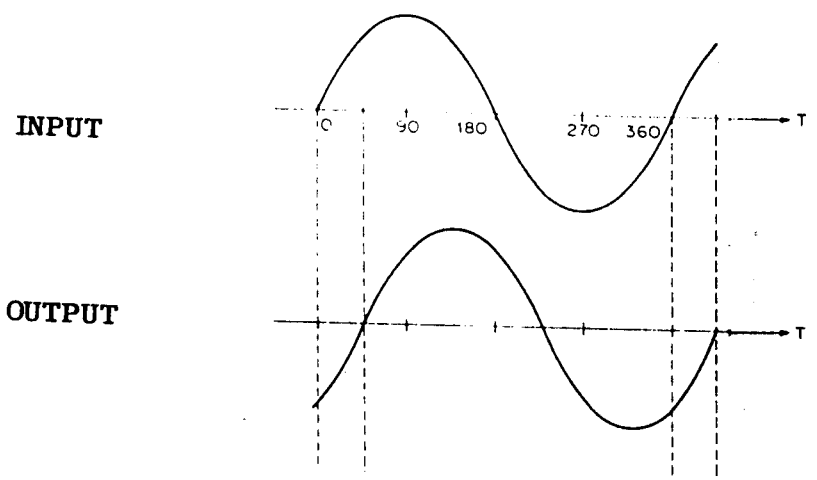


FIG. 1.2
PHASE SHIFT BETWEEN INPUT AND OUTPUT SIGNAL

2.1 MEASUREMENT OF PHASE (Lissagious Patterns)

2.2 METHODS OF PHASE MEASUREMENT

PHASE DETECTION TECHNIQUES

2.1. MEASUREMENT OF PHASE (LISSAGIOUS PATTERNS)

It is interesting to consider the characteristics of patterns that appear on the screen of the CRT when sinusoidal voltages are simultaneously applied to horizontal and vertical plates. These patterns are called Lissagious patterns.

When two sinusoidal voltages of equal frequency which are in phase with each other are applied to the horizontal and vertical deflection plates, the pattern appearing on screen is a straight line as clear from Fig.2.1. When two equal voltages of equal frequency but with 90° phase displacement are applied to a CRO, the trace on the screen is a circle. This is shown in Fig.2.2.

When two equal voltages of equal frequency but with a phase shift (0° or 90°) are applied to a CRO we obtain an ellipse (Fig.2.3). An ellipse is also obtained when unequal voltages of same frequency are applied to the CRO.

A number of conclusion can be drawn from the above discussions. When two sinusoidal voltages of the same

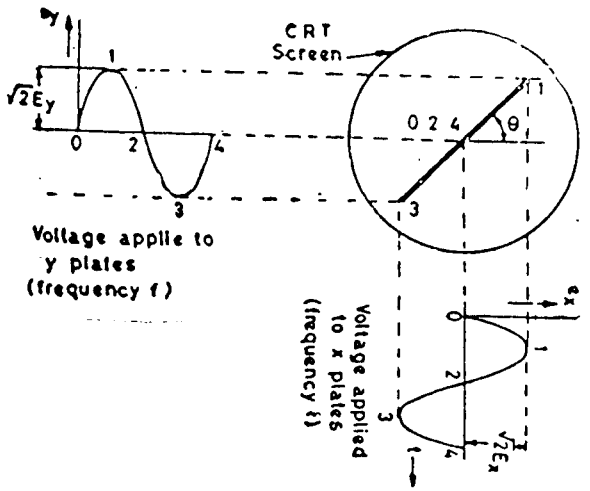


Fig 2.1 Lissajous pattern with equal frequency voltages and zero phase shift.

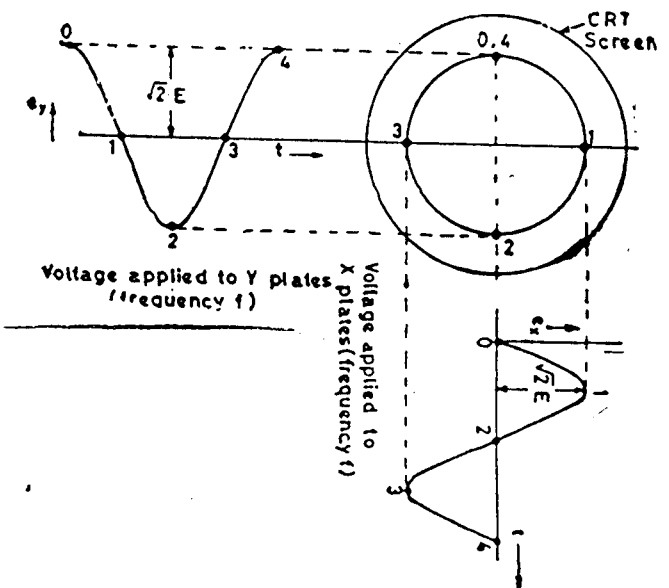


Fig 2.2 Lissajous pattern with equal voltages of equal frequency and a phase shift of 90°.

frequency are applied.

(i). A straight line results when the two voltages are equal and are in phase with each other or 180^{o} out of phase with each other. The angle formed with the horizontal is 45^{o}, when the magnitudes of the voltages are equal. An increase in the vertical deflection voltage causes the line to have an angle greater than 45^{o} with the horizontal. On the other hand a greater horizontal deflection voltage makes the angle less than 45^{o} with the horizontal.

(ii). Two sinusoidal waveforms of the same frequency produce a lissagious pattern which may be a straight line, a circle or an ellipse depending upon the phase and magnitude of the voltages. A circle can be formed only when the magnitude of the two signals are equal and the phase difference between them is either 90^{o} or 270^{o}. However if the two voltages are not equal and are out of phase an ellipse is formed. If the Y voltage is larger, an ellipse with vertical major axis is formed while if the X plate voltage has a greater magnitude, the major axis of the ellipse lies along horizontal axis.

(iii). It is clear from Fig.2.4 that for equal voltages of same frequency, progressive variation of phase voltage causes the pattern to vary from a straight diagnoal line to ellipse of different eccentricities and then to a

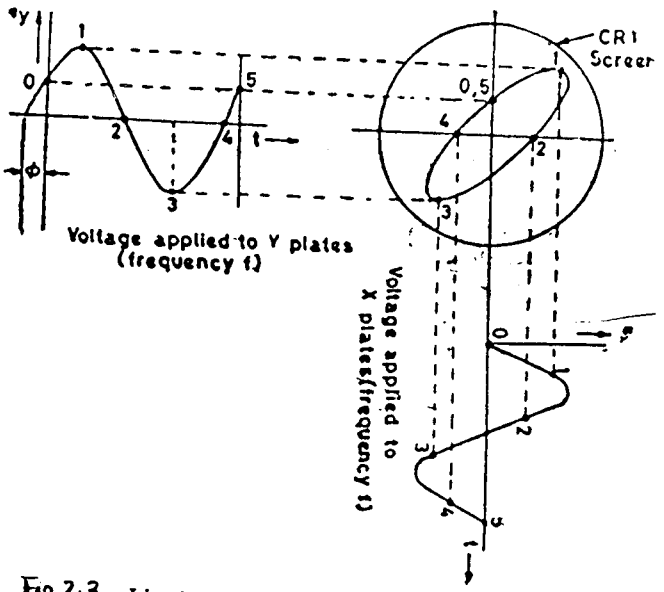


Fig 2.3 Lissajous pattern with two equal voltages of same frequency and phase shift of ϕ.

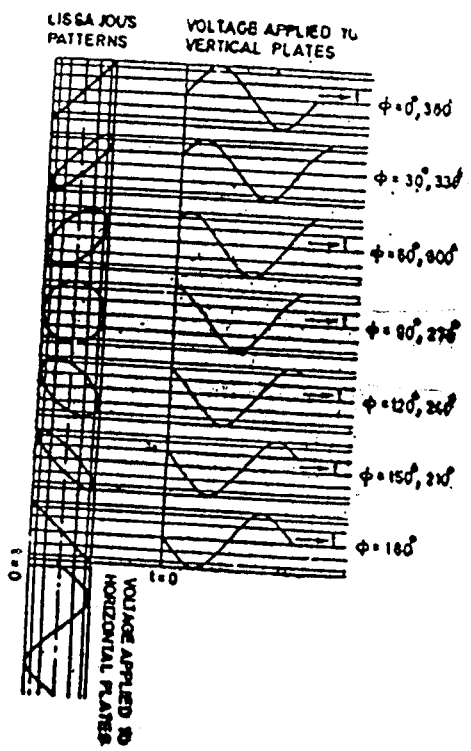


Fig 2.4 Lissajous patterns with different phase shifts.

circle, after that through another series of ellipses and finally a diagonal straight line again.

Regardless of the two amplitudes of the applied voltages the ellipse provides a simple means of finding phase difference between two voltages. Referring to Fig.2.5, the sine of the phase angle between the voltages is given by

$$\text{Sin } \phi = \frac{Y_1}{Y_2} = \frac{X_1}{X_2}$$

For conveniance the gain of the vertical and horizontal amplifiers are adjusted so that the ellipse fits exactly to a square marked by the lines on the graticule.

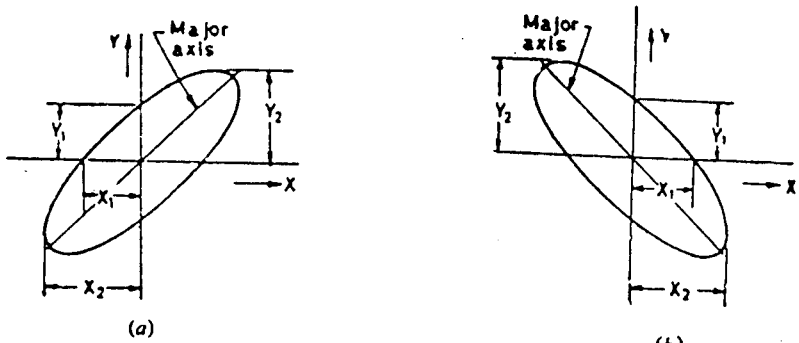
If the major axis of the ellipse lies on the first and third guadrants (ie. slope is positive) as in Fig.2.5. (a). the phase angle is either between 0^{o} and 90^{o} or between 270^{o} to 360^{o}. When the major axis of ellipse lies in the second and fourth guadrants, ie., when its slope is negative as in Fig.2.5. (b), the phase angle is between 90^{o} and 180^{o} or between 180^{o} and 270^{o}.

2.2. METHODS OF PHASE MEASUREMENTS

There are two methods that are widely used for measuring the phase difference between two given signals. They are,

i. Dual Trace Method

ii. X - Y Method



(a) (b)

Determination of angle of phase shift.

FIG. 2.5

2.2.1. Dual Trace Method

The dual trace method of phase measurement provides a high degree of accuracy at all frequencies, but it is especially useful at frequencies above 100 KHz, where phase measurement may provide inaccurate readings owing to inherant internal phase shift.

The dual trace method also has the advantage of measuring phase difference of signals with different amplitudes, frequency and waveshape. The method can be applied directly to those oscilloscopes having a built in dual trace feature, or to a conventional single trace oscilloscope using an electronic switch or "chopper". Either way the procedure consists essentially of displaying both traces on the oscilloscope screen simultaneously, measuring the distance (in scale divisions) between related points on the two traces, and then converting the distance into phase.

1. Connect the equipment as shown in Fig.2.6.
2. Place the oscilloscope in operation.
3. Set the step attenuators to deflection factor that will allow the expected signal to be displayed without overdriving the amplifiers.
4. Switch on the oscilloscope internal recurrent sweep.

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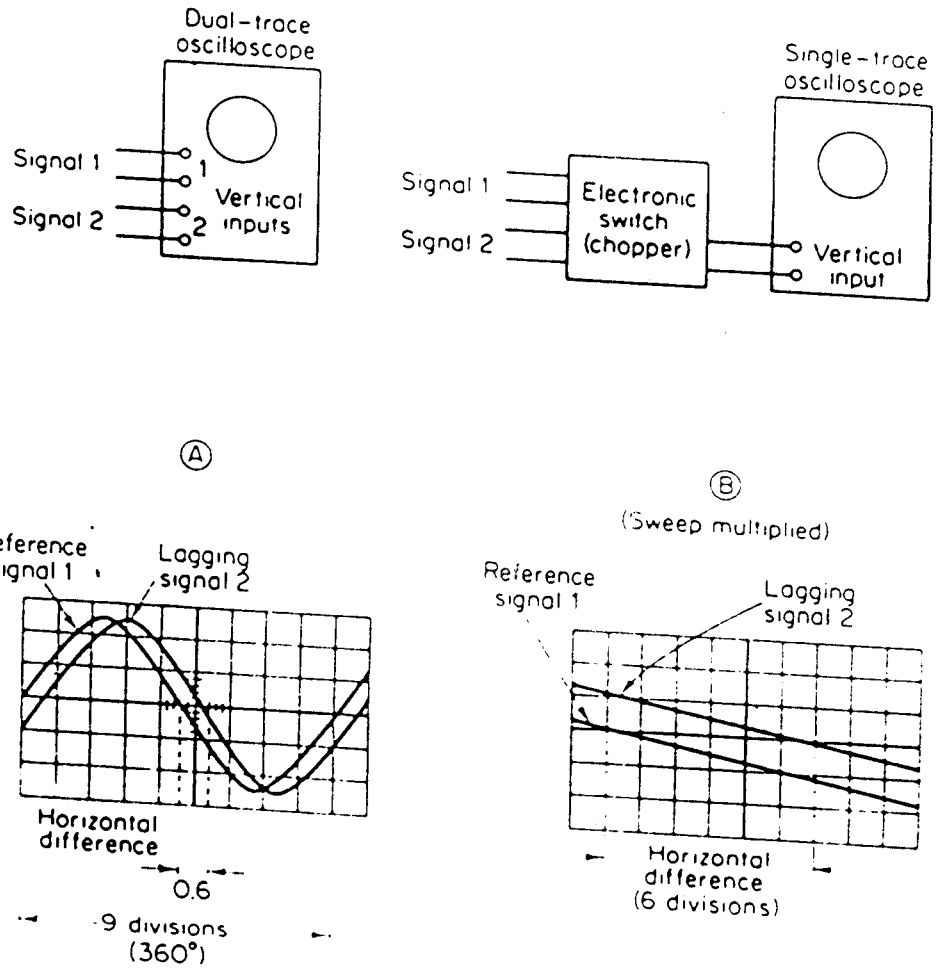


Fig. 2.6 Measuring phase difference with dual traces.

5. Set the position controls (horizontal and vertical) to spread the patterns over as much of the screen as desired.

6. Switch on the dual trace function of the oscilloscope or switch on the electronic chopper.

7. Adjust the sweep controls until one cycle of the reference signal occupies exactly 9 divisions of the screen.

8. Determine the phase factor of the reference signal.

9. Measure the horizontal difference between corresponding points on the waveform. Multiply the measured distance (in centimeters) by 40^{o} (phase factor) to obtain the exact amount of phase difference.

10. If the oscilloscope is provided with a sweep magnification control where the sweep rate is increased by a fixed amount and only a portion of one cycle can be displayed, more accurate phase measurements can be made. In this case, the phase factor is determined as in Step-9. Then the approximate phase difference is determined as described in step -10. Without changing any other controls, the sweep rate is increased (by the sweep magnification control or the sweep rate control) and a new horizontal distance measurement is made, as shown in Fig.2.6. (b).

Note:Either of the two signals can be used as the reference signal, unless otherwise specified by the requirements of the particular test. It is usually simpler if the signal of the lowest frequency is used as the reference signal.

Disadvantage

For more accurate results, the cables connecting the two signals to the oscilloscope input should be of the same length and characteristics. At higher frequencies a difference in cable length or characteristics could introduce a phase shift.

2.2.2. X - Y Method

The X - Y phase measurement method can be used to measure the phase difference between two sine wave signals of the same frequency. This method provides a method of measurement for signal frequencies upto about 100 KHz, more precise than the dual trace method. Above this frequency however the inherant phase difference between the horizontal and vertical systems make accurate phase measurement difficult. Therefore, the X-Y method should be limited to phase measurement of lower frequency signals and to signals of the same frequency.

In the X - Y method, one of the sine wave signals provide horizontal deflection (X), and the other provides the vertical deflection (Y). The phase angle between the two signals can be determined from the resulting lissagious pattern.

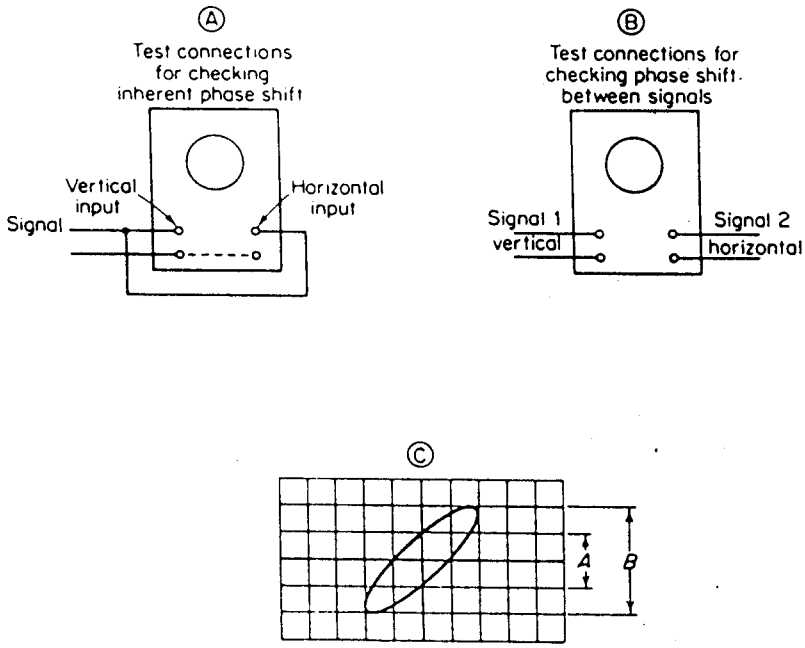
1. Connect the equipment as shown in Fig.2.7.(a).
2. Place the oscilloscope in operation.
3. Set the step attenuators to deflection factors that will allow the expected signal to be displayed without overdriving the amplifiers.
4. Switch off the oscilloscope internal recurrent sweep.
5. Set the gain controls (horizontal and vertical) to spread the patterns over as much of the screen as desired.
6. Set the position control (horizontal and vertical) until the pattern is centered on the screen. Center the display in relation to the vertical graticule line. Measure distance A and B as shown in Fig.2.7.(c). A is the vertical measurement between the two points where the trace crosses the vertical centerline. Distance B is the maximum vertical height of the display.
7. Divide A by B to obtain the phase angle between the two signals. The angle can then be obtained by taking the inverse sine of this value.

8. Once the inherant phase shift has been determined, connect the equipment as shown in Fig.2.7.(b). Repeat steps 3 through 7 to find the phase angle between the two signals.
9. Substract the inherent phase difference from the phase angle to determine the true phase difference.

Note:

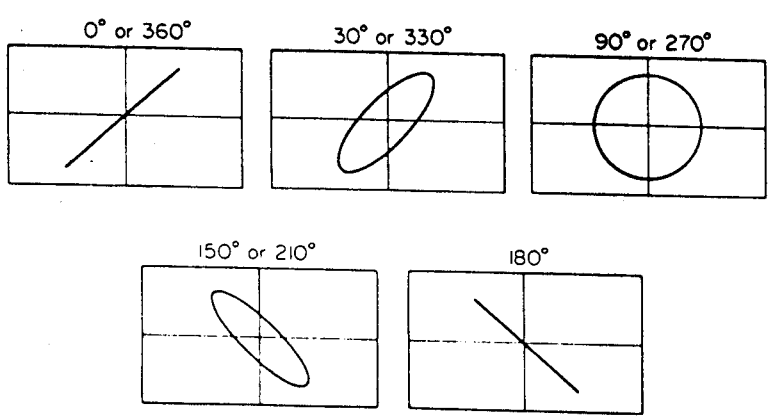
Figure 2.7.(a) shows the test condition necessary to determine the inherent phase shift (if any) between the horizontal and vertical deflection systems of the oscilloscopes. Even the most expensive laboratory oscilloscopes with identical vertical and horizontal amplifiers will have some inherant phase shift, particularly at the high frequencies. Therefore all frequencies should be checked and the inherent phase shift recorded before any phase measurements are made. If there is excessive phase shift (in relation to anticipated phase shift) the oscilloscope should not be used. A possible exception exists when the signals to be measured are of sufficient amplitude to be applied directly to the oscilloscopic deflection plates, and thus bypass the horizontal and vertical amplifiers.

If the display appears as a diagonal straight line, the two amplifiers are either in phase (tilted upper right to lower left) or 180^{o} out of phase (tilted upper left to lower



Measuring phase difference with X-Y method.

FIG. 2.7



Phase of typical X-Y displays.

FIG. 2.8

right). If the display is a circle, the signals are 90^{o} out of phase. Fig.2.8 shows Lissagious displays produced between 0^{o} and 360^{o}. Notice that above 180^{o} phase shift, the resultant diaplay, will be the same as at some lower frequency. Therefore it may be difficult to tell whether the signal is leading or lagging. One way to determine correct phase (leading or logging) is to introduce a small, known phase shift to one of the inputs. The proper angle may then be determined by noting the direction in which the pattern changes.

3.1 BLOCK DIAGRAM OF THE SYSTEM

3.2 BUFFER SECTION

3.3 ZERO CROSSING DETECTOR

3.4 BISTABLE MULTIVIBRATOR

3.5 MONOSTABLE MULTIVIBRATOR

HARDWARE DESCRIPTION

3.1. BLOCK DIAGRAM OF THE SYSTEM

The basic design of the phase meter is presented in the block diagram shown in Fig.3.1. For the sake of simplicity the LED digital display has been replaced by an analogue meter.

The two analogue signals whose phase difference is to be measured are fed into two input stages respectively. These input stages are just buffers which are used for avoiding the loading on the signals. It matches the impedances of the comparator with the signal source.

These signals from the buffer are given to two zero crossing detectors which are basically A to D converters. The analogue signals are digitised before they are processed. Since alternating signals are involved this is a simple process; the positive part of the signals are converted to a logic low (o), And the negative part to a logic high (1). The timing diagram for a typical signal is shown in Fig.3.2. It shows the analogue signals A and B (which are the inputs) together with their digitised varients A' and B'.

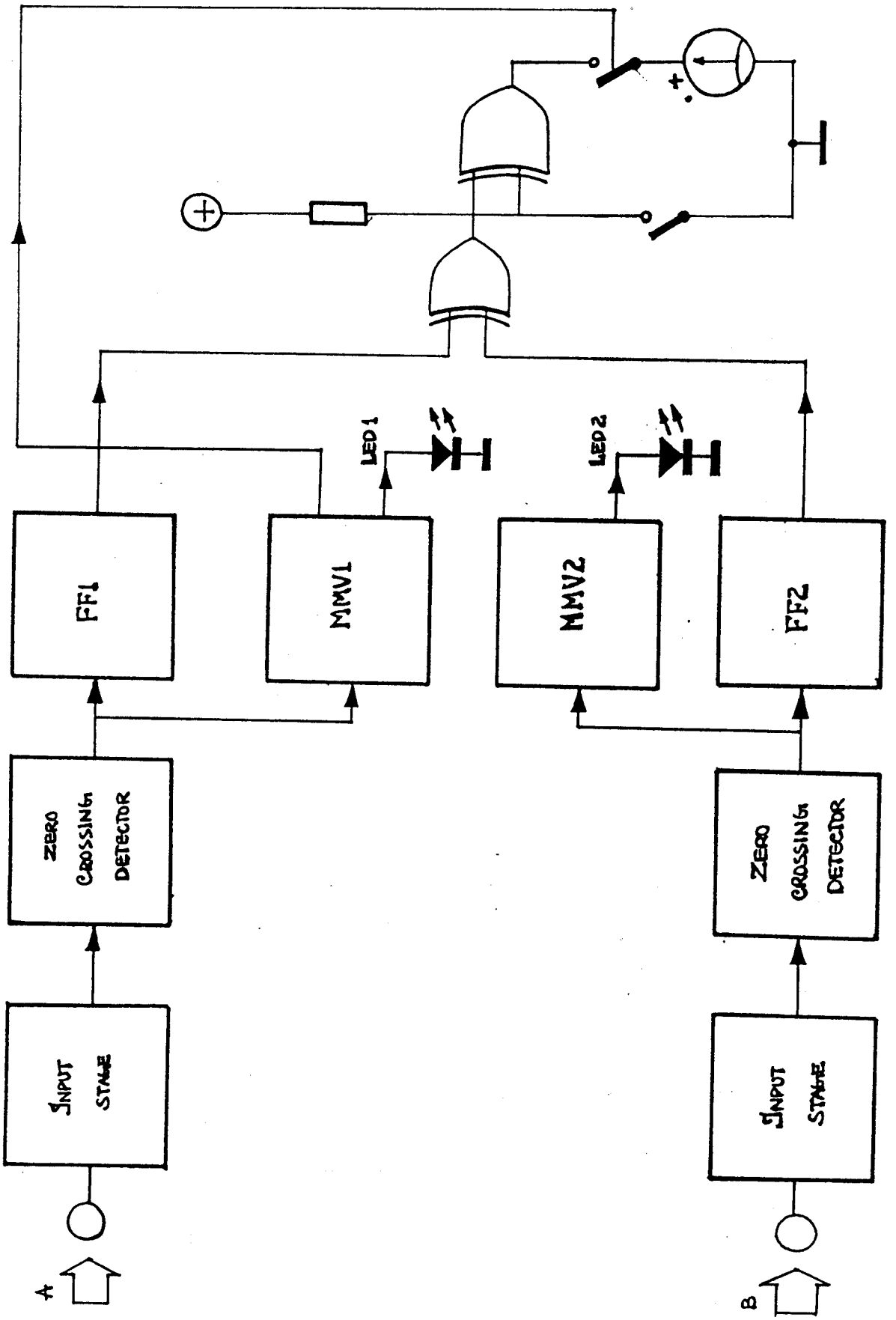


FIG. 3.1 BLOCK DIAGRAM OF THE DIGITAL PHASE METER

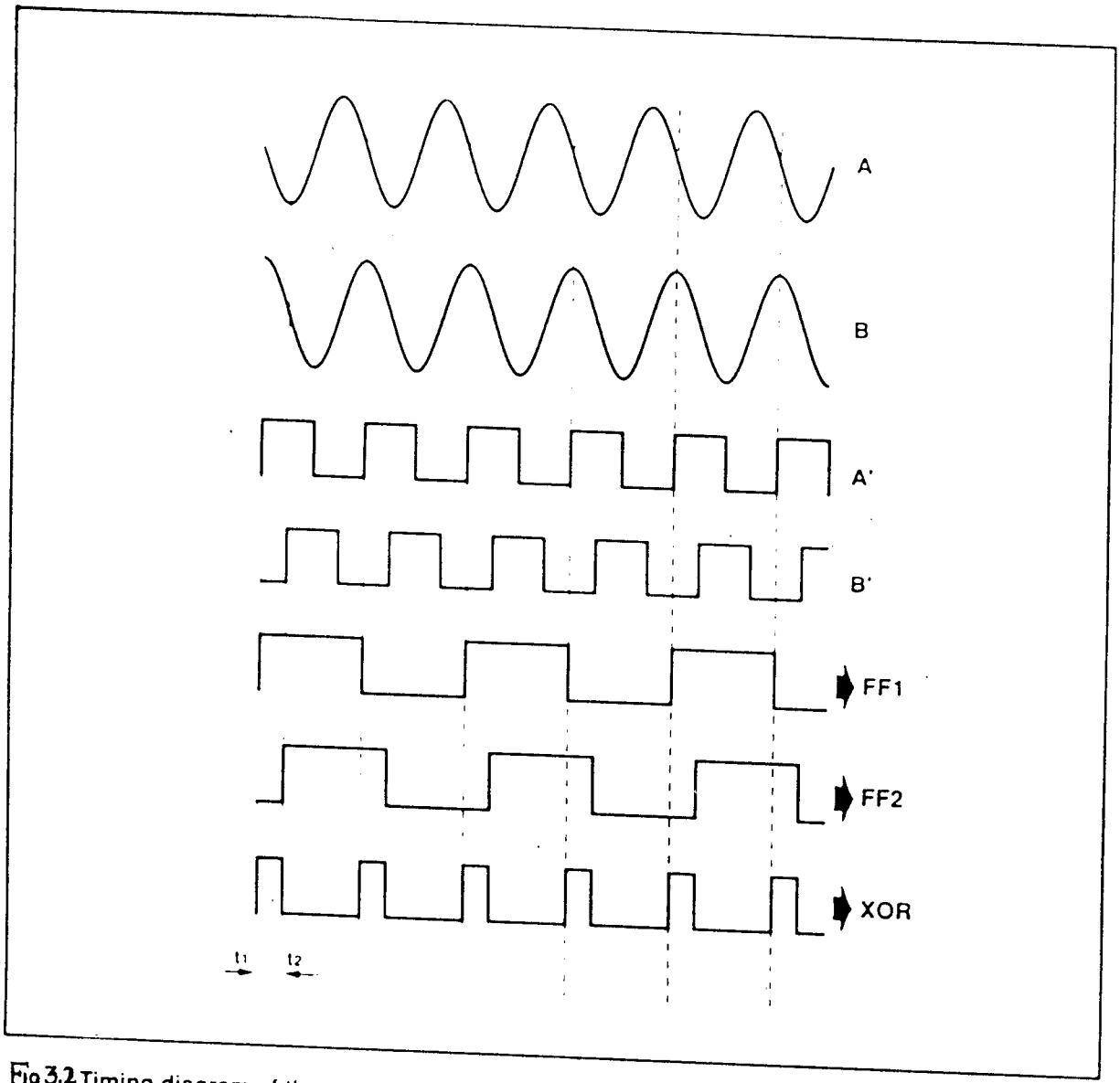


Fig 3.2 Timing diagram of the analogue-to-digital conversion section.

The output of the zero crossing detector are fed to two flip-flops FF_1 and FF_2. The use of digitised signals as the clock for bistable flip flop ensures a perfectly symmetrical (ie. duty cycle is 50 per cent) digital output signal at a frequency equal to half that of the input signal. This guaranties that differing lengths of positive and negative half periods, noise, have no effect on the accuracy of the measurements.

The time difference between the leading edges of the signals eminating from the bistables is a measure of the phase shift between the two input signals. These outputs of the bistables are fed to the two inputs of an EXOR gate. The output of the EXOR gate is high during the time difference only. The ratio of the width of the logic high signal at the output of the EXOR gate to that of the output signal of bistable FF1 gives the phase shift, which only has to be converted to degrees. The width of the output pulse of the EXOR gate indicates at all times by how much signal B lags signal A. Therefore the pulse represents the phase difference of 0^{o} to 360^{o}. Since it may also be of interest to measure the lag of signal A with respect to signal B, there is a second EXOR gate whose output may be inverted.

Monostables MMVI and MMV2 indicate by LED's that usable signals, ie signals whose phase difference is to be

measured, exist at the associated inputs. Furthermore the output of MMVI is used to actuate the meter. If only signal A is present, the meters must remain stably in center position. If it does not, the input signal is unstable and therefore not suitable for measurements.

Since the width of the pulse at the output of the EXOR gate is a measure of the phase shift, it would seem that a simple analogue interface in the form of an integrator would be sufficient for driving a moving meter. That would, however, present certain difficulties, such as a strong dependance on temperature and the fact that to obtain a stable meter deflection a high integration constant would have to be used. That would make the measurement very slow and the instrument inconvenient to use.

A digital meter was therefore chosen, which can accurately indicate any phase difference between 0^{o} and 360^{o} with a resolution of 1^{o}.

3.2. BUFFER SECTION

The input signals (A and B) are supplied separately to two buffer circuits. An operatitonal amplifier is made use for this purpose. A CMOS IC 3140 is selected for this purpose.

3.2.1. Description

This IC has two inputs : the inverting input and the non-inverting input. These inputs go to a pair of P-channel FET's which act as a differential amplifier.

Any small voltage difference on the (+) and (-) inputs is sensed, strongly amplified by the three internal gain stages and the output is received at pin-6. A rising signal at the non-inverting (or +) input drives the output positive, while a rising signal on the inverting (or -) input drives the output negative. Since the two input signals are applied to two gates of the CMOS transistors, the input impedence is virtually infinite.

All operational amplifiers have an inherent offset voltage at their inputs that cannot be distinguished from an input signal. The buffer IC 3140 shown in Fig.3.3. has an offset voltage of about 8 mv and hence we use the offset potentiometer P_1, which is a potentiometer variable till 5K. This potentiometer unbalances the current mirror just enough to compensate for input offset. For adjusting the preset, we short the two inputs under in circuit conditions and then adjust the potentiometer until we get an open circuit, midrange output voltage. The two diodes D_5 and D_6 provide protection against over voltage. Frequency compensation is

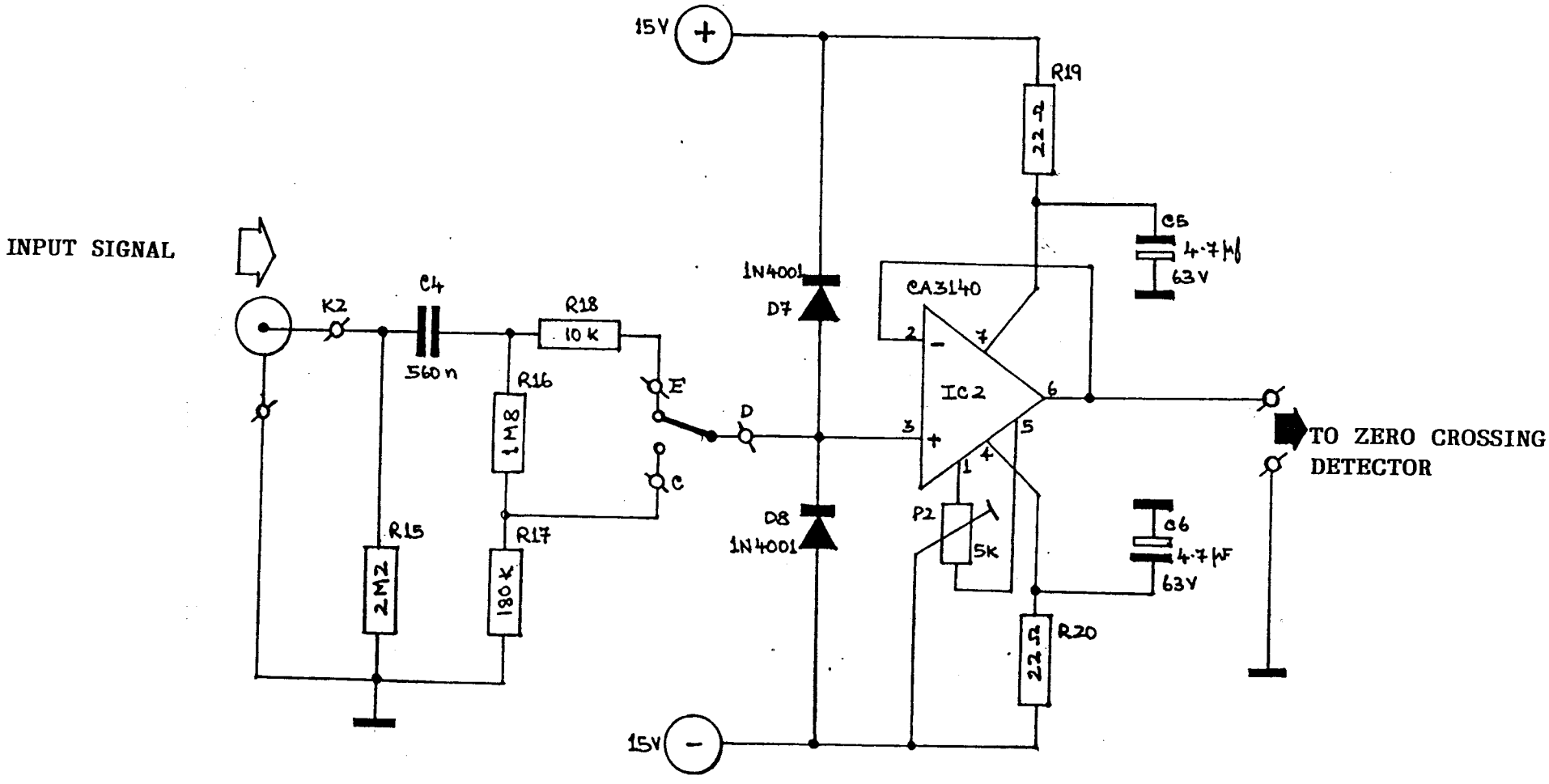


FIG. 3.3 BUFFER CIRCUIT

internally provided. The output stage is capable of driving capacitive loads.

When the inverting input terminal is shorted to the output pin (ie.pins 2 and 6). The op-amp acts as a unity gain amplifier which is a voltage follower. It gives a very high input impedace because the inverting input terminal does not act as a virtual ground. It can be compared to a super emitter follower with zero offset. The output is a low impedance, same size, same frequency, same polarity replica of an input signal which we cannot afford to load heavily.

Since all the voltage is fed back to the (-) input, the (-ve) input voltage will equal the output voltage. The high gain of the Op-Amp will force the (-) input to follow the (+) input.

3.3. ZERO CROSSING DETECTOR

The zero crossing detector, is the circuit used to convert the buffered input signal into its digitised varient. We are making use of an operational amplifier IC for this purpose. One of the most important applications of the operational amplifier is the zero crossing detector (A to D converter).

The buffered input signals are applied to the circuit shown in figure.3.4. there it is an open circuit operation of the Op-amp. The inverting terminal of the operational

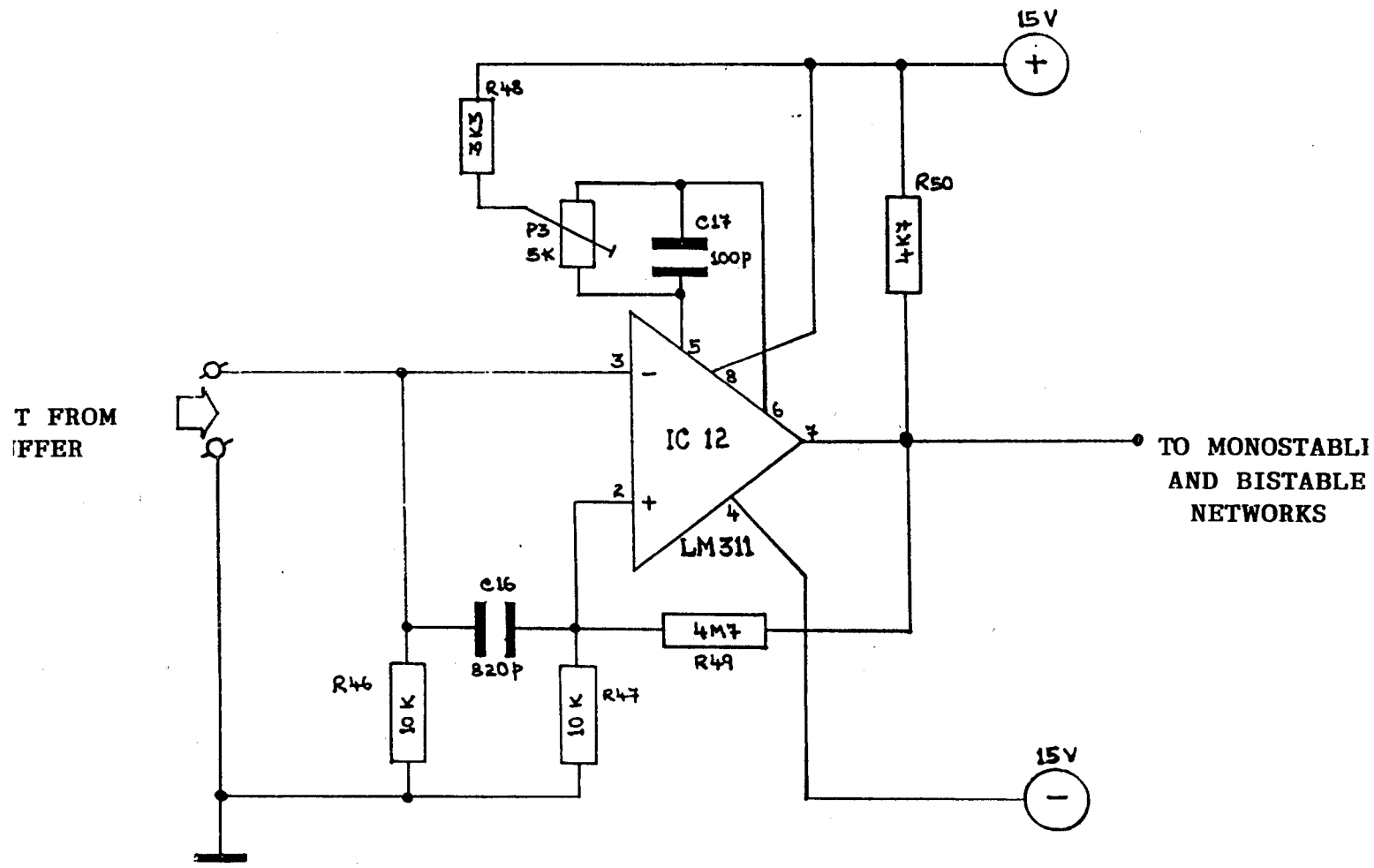


FIG.3.4 ZERO CROSSING DETECTOR

amplifier is connected directly to the input signal. The offset voltage compensation is provided by connecting a Rheostat in between pins five and six.

The principle of positive feedback is used here. The output voltage is fed back to the non-inverting terminal of the operational amplifier. The feed back resistor R_{49} is made a very high value compared to the series resistance R_{47} to provide significant hysterisis for the circuit, which ensures rapid output voltage transitions.

In open loop operation of the operational amplifier when it is used as a comparator the output voltage is positive when the amplitude of the voltage applied to the non-inverting terminal is greater than the amplitude of the voltage applied at the inverting terminal. The output voltage is negative when the voltage applied to the inverting terminal is greater than that applied to the non inverting terminal when a constant voltage is applied to the non inverting terminal of the Op-amp and a varying amplitude signal to the inverting terminal. The output changes states (0 and 1), when the input voltage crosses the threshold voltage in both directions.

So the output of this zero crossing detector is a digitized signal which has a high state during the -ve 1/2 cycle of the signal and a logical low state during the +ve

1/2 cycle of the analogue input signal as shown in figure 3.2.

The resistance R_{50} which is connected in between the +ue supply and the output pin acts as a voltage pull up resistor which increases the amplitude of the output voltage.

3.4. BISTABLE MULTIVIBRATOR

3.4.1. Description

Any device or circuit that has two stable states is said to be bistable. It's output is either in logical high stage or logical low state depending on the states of the input signals. Flip flop is a bistable electronic circuit that has two stable states (1 or 0). Any change in the logical status of the input signals are transmitted immediately to the outputs. It is also called a latch.

If we consider a R-S flip flop (set Reset flip flop), the status of the outputs are as shown in table 3.1. Fig.3.5. represents an R - S flip flop.

When we provide two AND gates as the input stage for an R-S flip flop as shown in Fig.3.6, we get a clocked R-S flip flop whose output changes depend on the clock signal. When enable input is low, the AND gate outputs are both low and hence there is no change in the output states of the flip

flop. The latch is said to be disabled. When the enable signal is high the R and S inputs are passed through and hence the output Q of the flip flop changes. This flip flop is called a clocked R-S flip flop.

J - K FLIP FLOP

JK flip flops are ideal circuit elements that can be used for the purpose of counting. Fig.3.7. shows how to build J - K flip flops.

The variables J and K are called control inputs because they determine what the flip flop does when a positive clock edge arrives. As before the Rc circuit has a short time constant, thus converting the rectangular clock pulse into narrow spikes. Because of the AND gates the circuit is positive edge triggered.

Table 3.2. shows the truth table for J-K flip flops. When J and K are both low, both AND gates are disabled. Therefore clock pulses have no effect. This first possibility is the initial entry in the truth table. As shown when J and K are both O's, Q retains its last value.

When J is low and K is high, the upper gate is disabled, so there is no way to set the flip flop. The only possibility is reset. When Q is high the lower gate passes a reset trigger as soon as the next positive clock edge

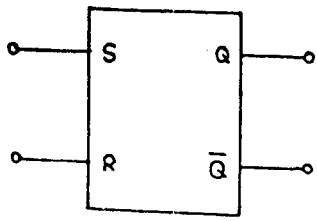


FIG. 3.5

LOGIC SYMBOL FOR AN RS FLIP FLOP

Table 3.1

R	S	Q
0	0	Last state
0	1	1
1	0	0
1	1	? (forbidden)

TRUTH TABLE

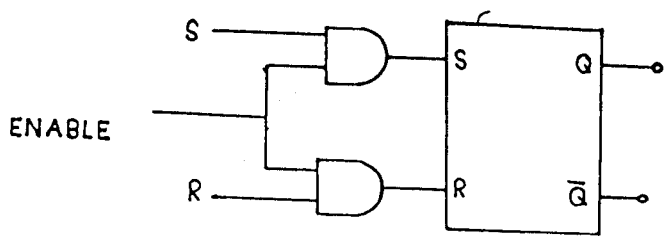


FIG. 3.6
LOGIC DIAGRAM FOR A CLOCKED RS FLIP FLOP

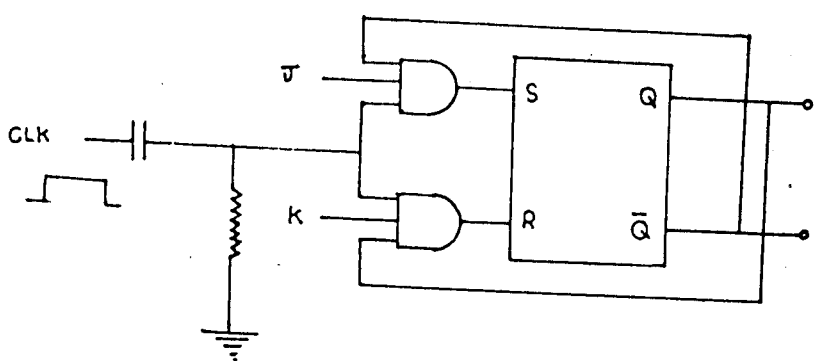


FIG. 3.7
J-K FLIP FLOP

Table 3.2

CLK	J	K	Q_{n+1}
×	0	0	Q_n
↑	0	1	0
↑	1	0	1
↑	1	1	$\overline{Q_n}$

TRUTH TABLE

arrives. This forces Q to go low. Therefore J = 0 and K = 1, means that the next positive clock edge resets the flip flop (unless $\overline{Q}$ is already reset). When J is high and K is low, the lower gate is disabled, so it is impossible to reset the flip flop.

But you can reset the flip flop as follows. When Q is low, Q is high; therefore the upper gate passes a SET trigger on the next positive clock edge. This drives Q into the high state. As you can see J = 1 and K = 0 means the flip flop will be SET for the next clock edge (Unless Q is already high).

When J and K are both high (notice that this is the forbidden state with an RS flip flop), it's possible to set or reset the flip flop. If Q is high, the lower gate passes a RESET trigger on the next positive clock edge. On the other hand, when Q is low, the upper gate passes a SET trigger on the next positive clock edge. Either way, Q changes to the complement of the last state. Therefore J = 1 and K = 1 means the flip flop will toggle on th next positive clock edge. Toggle means to switch to the opposite state. J - K master slave flip flops are used to prevent "racing".

The last entry in the truth table is effectively used to build a frequency divider.

The output of the zero crossing detector is a digitized varient of the input analogue signal. This signal has the same frequency as the input signal. This output from the zero crossing detector is used as the clocking signal for a J-K flip flop. In the circuit we are using a CMOS IC 4027 which is a dual J-K flip flop. We are using this as a frequency divider. We use the condition where, when J = 1 and K = 1 at the clock edge, the output of the flip-flop toggles ie., changes to the opposite state.

The IC 4027 is used to half the frequency of the signal that is the digitized version of the input sinusoidal signal. This IC has two negative edge triggered J-K flip flops.

3.4.2. Operation

The two inputs J and K are tied together and are connected to the positive DC voltage of 15 volts. So now the two inputs J and K are at a logical high state.

The outputs of the zero crossing detectors are applied to the clock input of each of the two flip flops. At every negative clock edge of the clock input, the output of the J-K flip flops change to their opposite state (ie toggles).

This occurs because both J and K inputs are at a logical high state. So at the Q outputs of the two flip flops we get two pulse trains as shown in the timing diagram shown in Fig.3.2.

From the figure we can easly see that the time period of each pulse has been doubled. So in effect the frequency of the output of the flip flop is half that of the input pulse train.

$$F_{out} = F_{in}/2$$

This halving of the frequency ensures a perfectly symmetrical signal (1/2 the frequency of the input signal) (duty factor is 50 per cent). This guarantees that differing lengths of positive and negative 1/2 periods, noise and other spacious signals have no effect on the accuracy of measurement.

Now at the output of the two J-K flip flops IC 13a and IC 13 b we have two digital signals which are the digitized varients of the two input signals whose phase difference is to be measured, with half their frequency.

3.5. MONOSTABLE MULTIVIBRATOR

3.5.1. Description

Monostables have one stable state and one unstable state. They remain in their stable state until they are

triggered. Triggering places them temporarly in the other state. After a certain time delay, the monostable snaps back into its original condition.

Monostables are generally used for medium accuracy pulse genrators and time delay generators. They are also used to detect leading and trailing edges of waveforms.

Here we are using the monostable to indicate the presence of two input signals whose phase difference has to be measured.

In the circuit we are using a dual retriggerable monostable IC (4528). Here both retriggerable monostables are used separately.

In normal operation the clear inputs (3 and 13) are held high. Pins 1 and 15 are grounded. If we are using the monostable to detect the leading edge of a waveform then we use the +ve inputs (4 and 12) to give the pulse and the -ve inputs (5 and 11) are given the supply voltage V_{cc}. If we are using the monostable to detect the trailing edge of the signal then we give the input pulses to pins (5 and 11) and the positive inputs (4 and 12) are connected to the ground. Figure to detect leading edges is shows in Fig.3.8. (a), and that which illustrates detection of trailing edges is shown in Fig.3.8. (b).

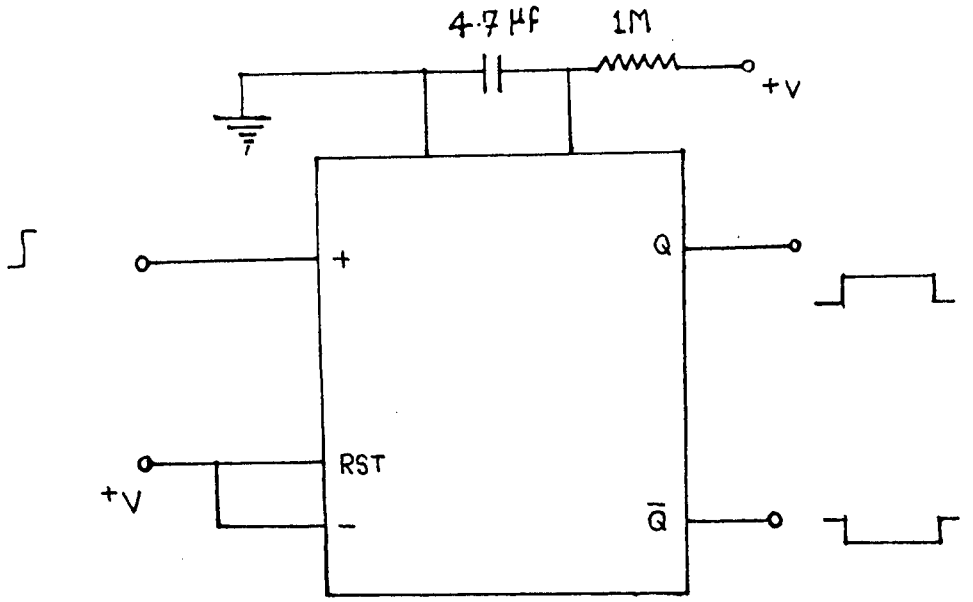


FIG. 3.8 (a)

POSITIVE EDGE TRIGGERED USING 4528

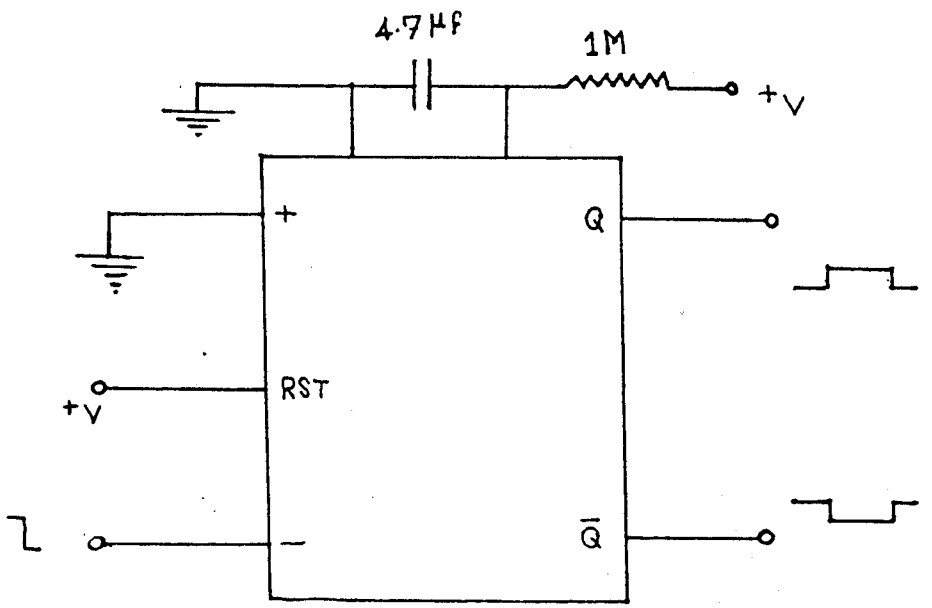


FIG. 3.8 (b)

NEGATIVE EDGE TRIGGERED USING 4528

When we supply the pulse, triggering will drive the Q output high and $\overline{Q}$ output low for a length of time set by the resistor and capacitor. The one time can be shortened by bringing the clear input low. A low clear input also prevents output pulses during power up times.

The timing resistor can range from 10 K to 10M ohms while the timing capacitor can range from 20 Pf upwards. The circuit is retriggerable ; If more than one triggering pulse arrives during the ON time, the RC product determines the delay after the last triggering edge arrives.

$$T = RC$$

The timing capacitor is discharged after every triggering. This causes a capacitor dependent delay between the time you trigger and the time you actually get any output. This delay is almost a microsecond with a 1000 PF timing capacitor and a 5 volts supply. Several milliseconds can elapse before you get an output after triggering with microfarad sized timing capacitors.

Always we should use a large timing resistor for a given ON time to minimise start up delay.

The minimum input pulse width is 70 nanoseconds at 5 volts, and 30 nanoseconds at 10 volts. Minimum output pulse width is 550 ns at 5 volts and 350 ns at 10 volts.

3.5.2. Operation

The digitized output of the zero crossing detector is applied to the manostable multivibrator IC shown in Fig.3.8.(a). The input is given to the positive pin. So this multivibrator detects the leading edge of the input signal. As soon as the positive edge occurs the monostable goes into quasistable high state. The duration of the quasistable state is determined by the timing capacitors (C_{20} and C_{21}). When the monostable is set by the positive edge of the input pulse, the capacitor starts charging and the period of the quasistable state depends on the product of the timing capacitor and resistance. So the LED's (D_9 and D_{10}) glow showing the presence of two signals at the input whose phase difference is to be measured. The output of the monostable drives the bases of the two transistors to whose collectors are connected the corresponding LED's.

The $\overline{Q}$ output of monostable multivibrator 1 also drives the reference counter.

CHAPTER 4

DIGITAL MEASURING SECTION

4.1. COUNTER SECTION

A counter is probably one of the most useful and versatile subsystem in a digital system. A counter driven by a clock can be used to count the number of clock cycles. Since the clock pulses occur at known intervals, the counter can be used as an instrument to measure times and therefore period or frequency. There are basically two different types of counters synchronous and asynchronous.

The ripple counter is simple and straight forward in construction and usually requires the minimum of hardware. It does, however, have a speed limitation. Each flip flop is triggered by the previous flip flop and thus the counter has a cumulative settling time. Counters such as these are called serial or asynchronus.

An increase in the speed of operation can be achieved by the use of parallel or synchronous counters. Here every flip flop is triggered by a clock (in synchronism), and thus settling time is simply equal to the delay time of a single flip flop. The increase in speed is usually obtained at the price of increased hardware.

Serial and parallel counters are used in combination to compramise between speed of operation and hardware size, serial, parallel or combination counters can be designed such that each clock pulse advances the contents of the counter by one. It is then operating in a count up mode. The opposite is also possible, the counter then operates in a count down mode.

Futher more the counters can be either "cleared' so that every flip flop containes a zero, or preset such that the contents of the flip flop represents any desired binary number.

4.1.1. Asynchronous Counters

A binary ripple counter can be constructed by use of clocked J-K flip flops. Fig.4.1. shows three masterslave, J-K flip flops connected in cascade. The system clock, a square wave drives flip flop. The output of A drives B, and the output of B drives flip flop C. All the J and K inputs are tied to $+V_{cc}$. This means that each flip flop will change state (toggle) with a negative transition at its clock input.

When the output of a flip flop is used as the clock input for the next flip flop, we call the counter a ripple counter or asynchronous counter. The A flip flop must change

states before it can trigger the B flip flop, and the B flip flop has to change states before it can trigger the C flip flop. The triggers move through the flip flops like ripples on water. Because of this the overall propagation delay time is the sum of the individual delays. For instance, if each flip flops in the counter has a propagation delay of 10 ns, th overall propagation delay time for the counter is 30 ns.

The waveforms given in Fig 4.1(b) shows the action of the counter as the clock runs. Let's assume that the flip flops are all initially reset to produce 0 outputs. If we consider A to be the least significant bit (LSB) and C the most significant bit, we can say the contents of the counter is 000.

Every time there is a -ve clock transition flip flop A changes states. Thus at the first -ve clock transition A goes high, at the second -ve edge it goes back low. At point C it again goes back high. Notable is the feature that the output of the flip flop A is 1/2 that of the input frequency.

Since A acts as the clock for B, each time the waveform at A goes low, flip flop B will toggle. Thus at point B on the time line B goes high. It then goes low at point b and toggles back high at point f. The waveform at the output of

flip flop B is one half the frequency of A and one fourth that of the clock frequency.

Since B acts as the clock for C, each time the waveform at B goes low, flip flop C will toggle thus C goes high at point d on the time line and goes back low again at point ah. The frequency of the waveform at C is one half that at B, but it is only one eighth of the clock frequency.

The output condition of the flip flops is a binary number equivalent to the number of negative clock transitions that have occurred. Prior to the point 'a' on the time line the output condition is CBA = 000. At point 'a' on the time line the output becomes 001. At point 'b' it changes of 010 and so on. In fact a careful examination of the waveforms will reveal the counter count advances one count for each clock transition until the count reaches 111. At this point the counter resets back to 000 and begins the count cycles all over again we can say that this ripple counter is acting in count up mode.

n flip flops in cascade have 2^n output conditions and represents a maximum binary equivalent of the decimal $2^n - 1$.

The modules of a counter is the total number of states through which the counter can progress. A counter with n flip

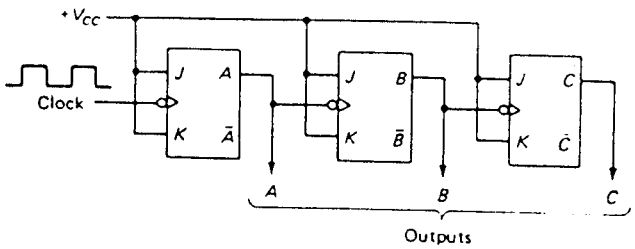
flops is called a modulus 2^n counter.

When the $\overline{A}$ output is used as the clock for flip flop B and $\overline{B}$ as the clock for flip flop C the counter acts as a down counter and counts from 7 downwards till zero.

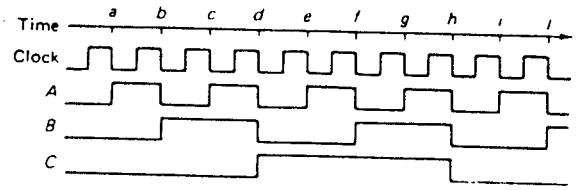
4.1.2. Synchronous Counters

A ripple counter is the simplest to build, but there is a limit to its highest operating frequency. As previously discussed, each flip flop has a delay time. In a ripple counter these delay times are additive and the total "settling" time for the counter is approximately the delay times the total number of flip flops. Furthermore there is the possibility of glitches occurring at the outputs of decoding gates used with a ripple counter. Both of these problems can be overcome by the use of a parallel counter. The only difference is that every flip flop is triggered in synchronism with the clock.

The construction of one type of parall binary counter is shown in Fig.4.2. (a), along with the truth table and the waveforms of a natural count sequence in Fig.4.2. (b). Since each state corresponds to an equivalent binary number (or count), we refer to each state as a count from now on. The basic idea here is to keep the J and K inputs of each flip flop high, such that the flip flop will toggle with any negative clock transition at its clock input. We then use



(a) Three-bit binary ripple counter

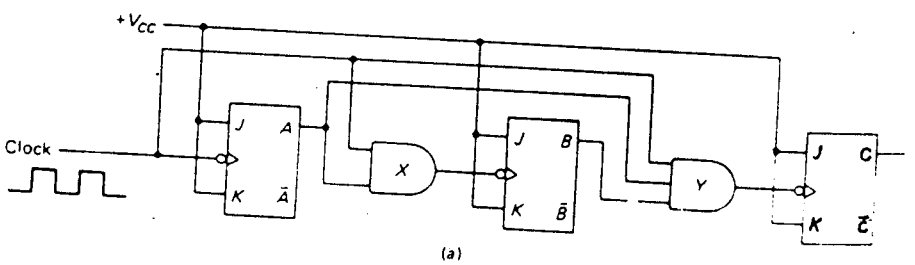


(b) Waveforms

Clock transitions	C	B	A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
0	0	0	0

(c) Truth table

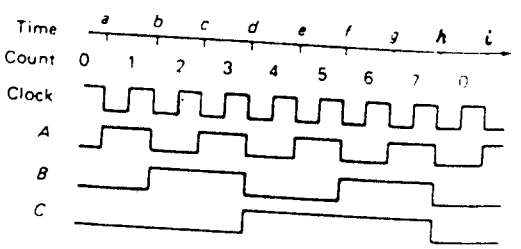
FIG. 4.1



(a)

C	B	A	Count
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7
0	0	0	

(b)



(c)

Mod-8 parallel binary counter

FIG. 4.2

and gates to gate every second clock to flip flop B, every fourth clock to flip flop C and so on. This logic configuration is often referred to as steering logic since the clock pulses are gated or steered to each individual flip flop.

The clock is applied directly to flip flop A. Since the J - K flip flop is used to respond to a negative clock transition. Its o/p toggles for each -ve transition of the clock.

Since, AND gate Y is enabled and will transmit the clock to flip flop C only when both A and B are high flip flop C changes state with every fourth negative clock transition. This is a mod-8, parallel or synchronous binary counter operating in the count up mode.

Advantages

1. Whenever a flip flop changes state, It toggles at exactly the same time as all the other flip flops; in other words all the flip flops change state in synchronism.
2. As a result of synchronous change of state. It is not possible to produce a glitch at the output of the decoding gate. So the decoding gates need not be strobed.

Till now we have explained the construction of synchronous and Asynchronus counters to count the multiples of two ie., till 2, 4, 8, 16, 32 etc. It is often desirable to construct counter having moduli other than 2, 4, 8. For example, a counter having modulus 3 or 5. A smaller modulus counter can always be constructed from a counter of high modulus by skipping states.

The correct number of flip flops is determined by choosing the lowest natural count that is greater than the desired modified count.

Operation

1. Prior to point a on time line A = 0 B = 0 a -ve clock transition at a will cause.
   a. A to toggle to 1, since its J and K inputs are high
   b. B to reset to 0
2. Prior to point b on the time line A = 1 and B = 0. A negative clock transition at b will cause.
   a. A to toggle to a 0, since its J and K inputs are high
   b. B to toggle to 1, since its J and K inputs are high
3. Prior to point c on the time line, A = 0 and B = 1. A negative clock transition at C causes.
   a. A to reset to zero
   b. B to reset to zero since its J input is low and its

K input is high.

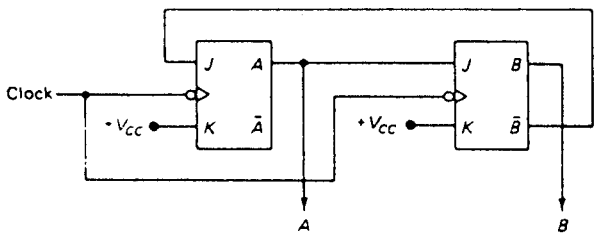
This can be considered as a devide by 3 block, since the output waveform at B (or at A) has a period equal to three times that of the clock in another words, this counter divides the clock frequency by 3. A MOD-3 synchronous counter and its timing diagram is shown in Fig.4.3. (a) and Fig.4.3. (b) respectively.

4.1.4. Mod-5 Counter

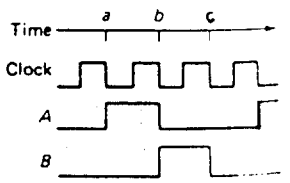
The 3 flip flop counter shown in Fig.4.4. (a) has a 4.1.(a) natural count of 8. But in the circuit shown in fig. 4.1(a), the circuit is connected
such that it advances one count at a time, beginning with 000 and ending at 100. Therefore this is a mod-5 counter.

The waveforms shown in Fig.4.4. (b) show that flip flop A changes states each time the clock goes negative except during the transition from count 4 to count 0. Thus flip flop A should be triggered by the clock and must have an inhibit during count 4 - ie some signal must be provided during the count from 4 to count 0. $\overline{C}$ is high during all the counts except count 4.

If $\overline{C}$ is connected to the J input of flip flop A, we have the desired inhibit signal. This is true
since the J and K to inputs the flip flop A are both true for



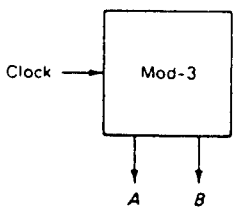
(a) Logic diagram



(b) Waveforms

B	A	Count
0	0	0
0	1	1
1	0	2
0	0	0

(c) Truth table



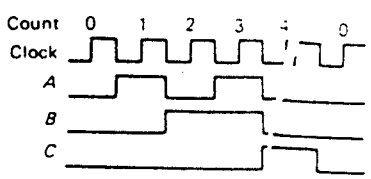
(d) Logic block

Mod-3 counter

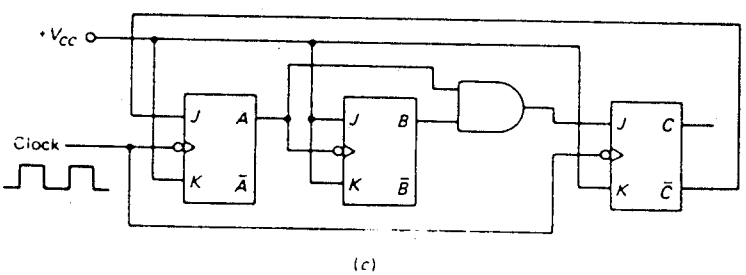
FIG. 4.3

C	B	A	Count
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
0	0	0	0

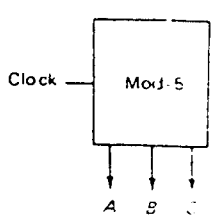
(a)



(b)



(c)



(d) Logic block

Mod-5 binary counter

FIG. 4.4

all counts except count 4. Thus the flip flop triggers each time the clock goes negative. However, during count 4, the J side is low and next time the clock goes negative the flip flop will be prevented from being set.

The desired waveforms in fig 4.4 (b) shows that flip flop B must change state each time A goes negative. Thus the clock input of flip flop B will be driven by A as shown in Fig.4.4. (a).

If flip flop C is triggered by the clock while the J input is held low and K input is high, every clock pulse will reset it. Now if the J input is high only during count 3, C will be high during count 4 and low during all other counts. The necessary levels for the J input can be obtained by AND ing flip flops A and B. Since, A and B are both high only during count 3 the J input to flip flop C is high only during count 3. Thus when the clock goes negative during the transition from count 3 to count 4, flip flop C will be set. At all other times, the J input to flip flop C is low and is held at a reset state. The complete mod-5 counter is shown in Fig.4.4. (a).

The 3 flip flop counter does not count 5, 6 and 7 during its normal operating sequence, but there is a very real possibility that these three counters may initially set in any one of these three (illegal) states when power is

initially switched on. None of these three states cause the counter to malfunction, and it will automatically work itself out of any illegal state after only one clock transition.

Mod-5 counter can be used in cascade to construct higher modulus counters. For example modulus 10 or Decade Counter.

4.2. DESCRIPTION

The block diagram of the measuring section in shown in Fig.4.6. A crystal oscillator in used to generate a central clock frequency of 6 MHz. This central clock frequency of 6 MHz is applied continuously to one branch of the circuit, and to other branch only when the output of the XOR gate of the phase comparator is high. In both the branches of the circuit, the clock pulses are divided by 2^n before they are applied to the respective stage. The factor n can be set manually by using a rotary switch. It in important to observe that since the division takes place after the AND gate, this gate, has no effect on the accuracy of the instrument.

The counting always starts at the beginning of a period. As soon as the content of the reference counter has reached a value of 3,600 one output of the counter goes high

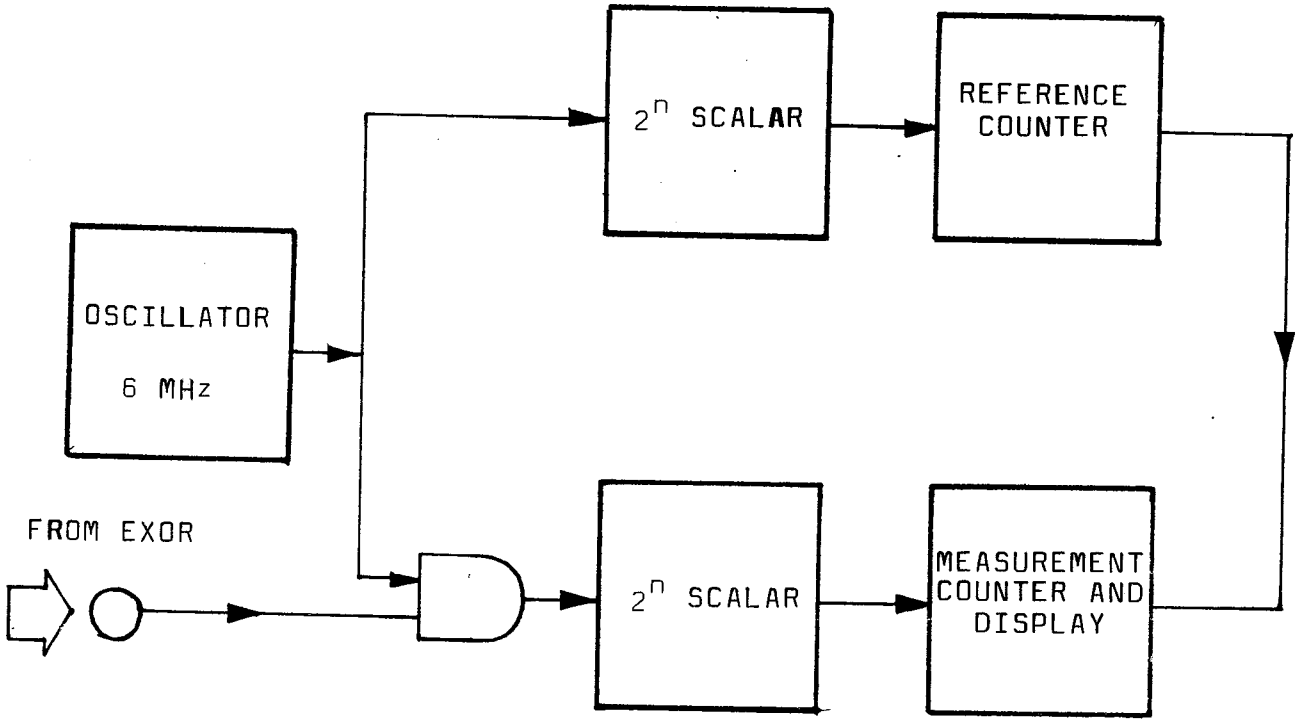


Fig. 4.6. BLOCK DIAGRAM OF THE DIGITAL MEASURING SECTION.

to indicate that measurement in complete and that 3600/2n pulses were processed during it.

At the instant the reference counter has counted 3,600 pulses the display memory in prompted to take over the contents of the measurement counter. The display will then show the number of the counted pulses, that is, when the phase shift in 0^{o}, no pulses were counted, if the phase shift is 360^{o}, 3600 pulses were counted. The last digit of the number of pulses is omitted to make the display read the no.of degrees.

It sould be noted that the accuracy of the measurement depends on the ratio of the measuring time to the frequency of the reference signal. The measurand is therefore sampled at a frequency of 6 MHz. Even at the highest signal frequency of 20 KHz, the error introduced by this is negligible.

Further more the design of the instrument arranges that counting always starts at the beginning of a period. Therefore it is never known how much of the last period is measured and steps must be taken to ensure that last period has negligible influence on the measurement. This in done by taking many periods per measurement. For instance, a measurement over 10 periods has a possible error of 10 per cent whereas over 200 periods the error would be only 0.5 per cent. Because of that the instrument contarly a counter

(in error indicating circuit) that moniters over how many signal periods a measurement was spread.

CHAPTER 5

DESCRIPTION OF THE CIRCUIT

The instrument in constructed on three printed circuit boards, the associated circuits are shown in Fig.5.1, 5.2 and 5.3.

The fig (5.1) is the circuit diagram for the mother board the power supply in a straight forward, conventional type with a bridge rectifier and two integrated regulators.

The buffered and possibly attenuated (-20dB) signal is applied to terminals A and B. Input A in used as reference signal and for actuating the metering section.

The incoming analogue signal is converted into a digital signal in IC 12 (channel A and IC 14 (Channel B). The offset of these Op-Amps is compensated by presets P_3 and P_4 respectively. Bistables IC 13a and IC 13b split, the digitized signal into symmetrical signal (duty factor - 50 per cent) that is suitable for measurements.

Monostables IC 15a and IC 15b actuate the LED's (D_9 and D_{10}) on the front panel to indicate that suitable signals are input.

The outputs of IC 13a and IC 13b are combined Via EXOR Gate IC 16a. Another XOR Gate IC 16b and switch S4 on the

front panel make it possible to invert the phase difference as discussed before.

Finally IC 17a which is an AND gate combines the output of the phase comparator with the clock frequency (6 MHz). When the output of XOR gate IC 16a is high, the clock is passed on and the measurement may be carried out.

The clock signal is generated by a crystal oscillator based on IC 16c. This clock signal is buffered by IC 16d before it is applied to the relevant stages.

At the end of measurement a reset cycle in started by IC 24, which is a 12 stage binary counter. As soon as this IC has counted 3600 poines, IC 23b (J-K flip flop) is set via IC 25a (And gate) and OR gate D_{11} - D_{12} and in its turn resets decade scaler IC 26. This actuates the latch signal, where upon the counter state is transferred to the display drivers. Subsequently IC 22 receives a clock pulse and stores data concerning any measurement error, after which IC 21 is reset. All relevant measurement data are then stored and the remainder of the circuit in reset via bistable IC 23a. When the reset cycle in over, IC 23a is returned to the relevant output state via, AND gate IC 17b. At the same time, IC 24 is reset by the clock pulse that appears at the Q 9 O/P of

decade counter IC 26. This circuit in then ready for next measurement.

As mentioned before, the more periods are used, the more accurate the measurement. The counter in error detector IC 18 countes the number of periods between the onset of the measurement and the generated latch pulse. Four AND gates decode the result at 360, 180, 90 and 36 periods in one measurement. These counts correspond to errors of 0.5^{o}, 1^{o}, 2^{o} and 5^{o} respectively. Depending on the no.of counted periods, one or more LED's light; when they all light, the error is negligibly small.

Figure 5.2. shows the circuit of display the indicators the i/p stages and the stage for selecting the measurement duration. The indicator LED's are driven by transistors; the control lines are connected to relevant points on the mother board via K5.

The input impedance in about 1 M. ohms large input signals may be attenuated by 20dB (S_1 and S_2). All input signals are buffered by type CA3140 Op-Amps before they are applied to the comparator on the mother board. The inputs of these buffer are protected against over voltage by diodes. Presets P_1 and P_2 serve to minimize the offset at the output of the Op-amps.

Circuits IC 3 and IC 4 (4020) are programmable 2^n dividers IC 3 counts the clock pulses passed by AND gate IC 17a, that is, the pulses that indicate how long the output of XOR gate IC 16b has been high. The no.of these pulses depends entirely on the phase shift between the two input signals. IC4 is the reference counter that receives clock pulses continually.

The scaling factor in set with S_3; it enables the user to select a measurement time that is most suitable for the frequency of the input signal. The error indicators on the display show whether the correct time has been selected.

Fig.5.3. shown the circuit contained on the third PCB; the seven IC'S form the display counter and interface for the LED displays.

The clock pulses to be counted are applied to cascaded counters IC 5 - IC 8 (4510) via pin 3 of K8.

As soon as the latch signal in active, the counter state in stored in display drivers IC 9 - IC 11 (4543). The displays, connected with this part of the circuit via K_9, light to show the correct value measured.

At the reset command at pin2 of K_8 the counters are returned to zero and a new measurement cycle can be started. The previous measurement value in retained on the displays

because the display drivers are not reset. The next measurement is thus carried out while the displays show previous result.

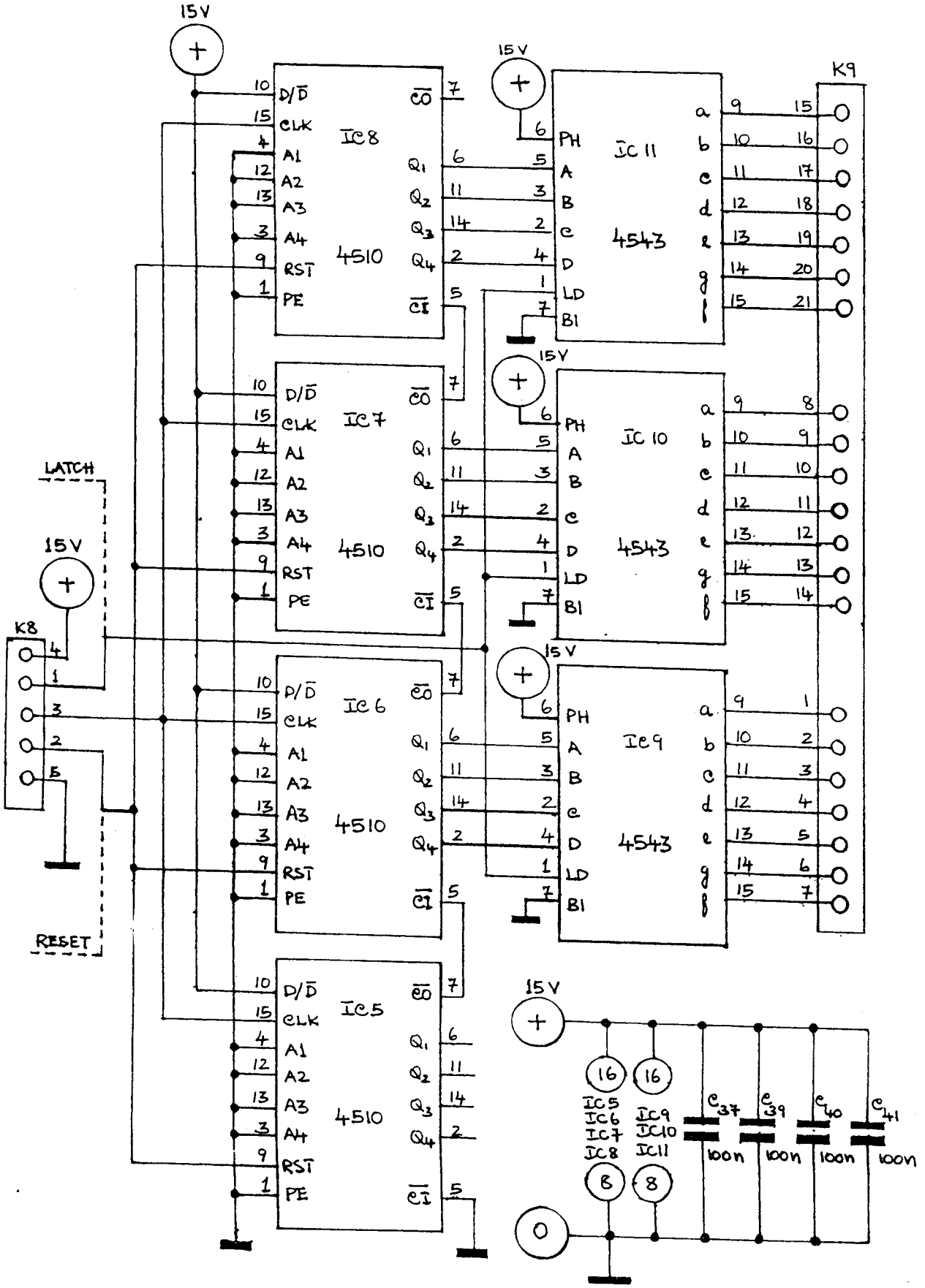


Fig.5.3. DIAGRAM OF THE LOGIC CIRCUITS FOR LED DISPLAYS.

CIRCUIT CONSTRUCTION

The 3 PCBs are shown in the figures B-1 to B-6 in the Appendix - B. Their population is straight forward, but it is best to begin with boards 2 and 3.

Connectors K_8 and K_9 on the board 3 may be replaced by right angle print headers. As a bonus, such headers would ensure a firm mechanical link between boards 2 and 3. In any case, the boards are provided with poles to enable corner braces to be used for strong mechanical linking.

The LED displays should be mounted on the board 2 about 1 cm (3/8 inch) above the board with the aid of wive wrap IC scokets.

Now connect the switches S_1, S_2 and S_4, to the board with short lengths of wire and fit S_3 directly to the board.

Cut the terminal wires of D_1 to D_4 and D_9 and D_{10} to about 2 cm (13/16 inches); this will ensure that they will be located exactly behind the windows in the front panel.

Fit soldering pins at A and B and adjacent earth points at the track side of board 2. The power on indicator, D_{13},

is best fitted to the front panel with the aid of an LED clip or super glue.

Fit board 2 on suitable spacers directly behind the front panel. Just prior to tightening the screws, connect the input sockets to the board via short wires. Next, screw the three toggle switches to the front panel.

Finally mount board 3 at right angles to the track side of board 2.

Mount the board on the bottom plate of the enclosure, after which all necessary electrical connections to the other boards, the power on LED, and ON-OFF switch to mains entry plug can be made.

Finally, interlink points A and B, and associated earthing points, on the mother board and board 2 by single screened audio cable.

CHAPTER 7

CALIBRATION AND USE

Having constructed the circuit of the digital phase meter, it in now required to calibrate it.

Calibration of the phase meter is confined to adjusting the four presets.

Short circuit inputs A and B and adjust P_1 and P_2 for zero output of IC 1 and IC 2.

Now remove the short circuit from the inputs and apply a sinusoidal audio frequency at a level of about 10 mV to the inputs. Adjust P_3 until comparator IC 12 toggles exactly at the zero crossing point, check this on an oscilloscope. Finally adjust P_4 until the display shows a phase difference of 0^{o}.

Start measuring the phase shift by applying the two signals to the inputs and turning S_3 (gate time) fully clock wise. Then turn the switch anti clock wise step by step (when the accuracy increases). When the indicator, marking a measuring error of 0.5^{o} lights, the optimum position for this measurement has been reached. Since the measurement period increases all the time, it may take a few seconds at

low frequencies before the indicator lights. That is, however, the price to be paid for accuracy at low signal frequencies.

CHAPTER 8

POWER SUPPLY OF THE SYSTEM

This project utilizes CMOS IC's. The minimum voltage required for these chips is ± 15V dc supply. The operational amplifiers used also need ± 15 dc supply. The block schematic shown in the Fig.8.1, describes the method to obtains a dc supply of + 15 V and -15 V from an Ac voltage of 230 V and 50 Hz.

This schematic contains a step down centre tapped transformer T_{r1}, a bridge rectifier Bl and regulators. The i/p dc supply is fed to the primary of transformer Tr_1. The switch K_{10} is a mains entry plug. It has got a provision for the fuse. This switch K_{10} acts as the main switch. The secondary winding of the transformer Tr_1 is a centre tapped one and the output obtained in 18V, 2A. This voltage is now fed into a bridge rectifier (Bl) LB 15604A for obtaining the dc voltage of ± 15 V. The secondary voltage from the transformer is full wave rectified by the diodes. The dc voltage obtained will generally be in the form of dc pulsatory wave. This is due to the ripple ie., the ac component present in the dc output received from the bridge rectifier circuit. In order to successfully eliminate this ripple a capacitor network in used. This network contains

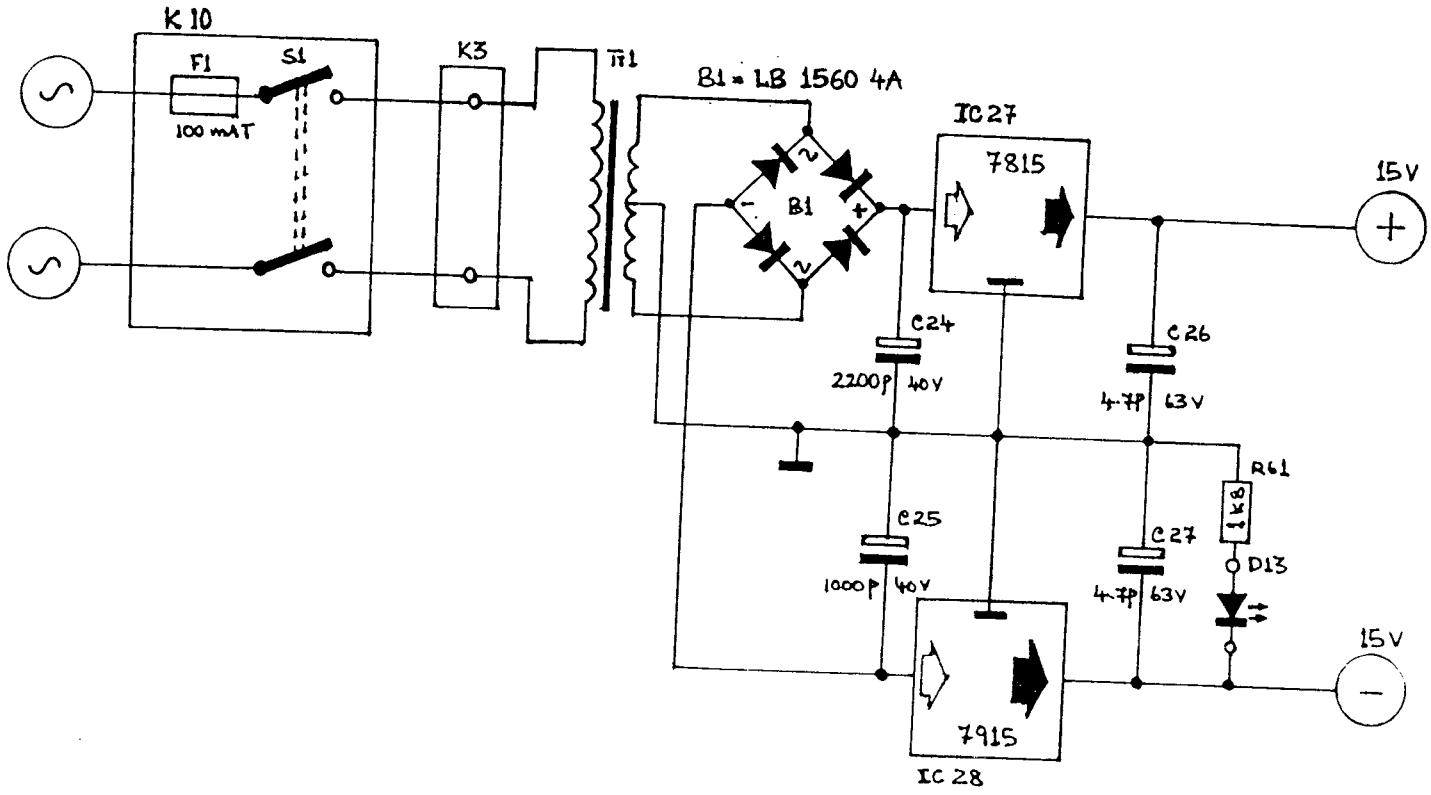


Fig.8.1 POWER SUPPLY OF THE SYSTEM.

capacitors C_{24} and C_{25} in parallel. The filtered output is fed to the regulator IC's 7815 and 7915 for obtaining a stabilised dc voltage of + 15V and -15 V respectively. Still if there is any ripple present in the dc component of regulator outputs, the capacitor C_{26} and C_{27} eliminate them. The output in obtained across this capacitor and this will be a pure dc supply.

The 78XX series of regulators which come in a T0220 package generally can supply 500 ma. Therefore the maximum power dissapated in them is probably going to be 500 ma times the voltage difference between the input and output terminals. This might mean that the regulator has to dissapate 5W of heat, therefore an adequate heat sink is provided to it.

In the above metnioned circuit, the fitting of the main input socket, the fuse holder and the mains transformer is fairly straight forward.

PRINTED CIRCUIT BOARD DESIGN

Printed circuit boards are generally used for laying out complex digital circuits.

The common problems which we meet with if not properly designed are listed as follows:

1. Reflections (causing signal delays and also double pulsing i.e., conversion of one pulse into two or more pulses).
2. Cross talk (interference between neighbouring signal lines).
3. Ground and supply line noise.
4. Electromagnetic interference from pulse type EM fields (under high noise conditions).

REFLECTIONS

In families of fast t_r (rise time) of IC's the conductors must be looked as a piece of transmission lines rather than short circuits. The transmission lines are normally mismatched on both sides so that multiple reflections take place based on the particular value of wave impedance of the conductor.

While designing the main points to be looked is that it must be having a proper value of wave impedance a value which has least reflections.

This wave impedance is chosen by selecting the width of the signal lines lower values of wave impedance such as needed in ECL IC's require broader signal conductors. Relatively larger value of wave impedance as needed by TTL, CMOS etc., require small width signal conductors. As in a digital circuit we are having a low operating frequency, double pulsing can't be tolerated. The double pulsing is the result of reflections.

For TTL logic, a wave impedance of 100 to 150 is desirable. The signal lines hence is 0.5 mm wide. The standard width of PCB dielectric is 1.6 mm. The signal lines can be even 1 mm wide only if then ground lines are farther away.

Current drawn or sunk back into the IC will be very large 20 mA and -55 mA for 50 line PCB for the rising and trailing edges respectively. These currents spikes have to be supplied by the Vcc line, (rising edge) or fed to the ground lines (trailing edge). Hence, in TTL PCB's wave impedance of 50 or less must be avoided. Very high impedance such as 720 ohms also cause problems making voltage as

well as double pulsing very high. Hence, in TTL IC's loose wiring (high impedance) must be avoided and signal connections must run always near the ground line.

For CMOS circuits, broad PCB conductors for signal lines is avoided. The wave impedance must be high and the signal line width is 0.5 mm. If the wave impedance is 150 to 300 ohms, the transitions will be considerably faster. The above value can be obtained if signal line width is low, the ground lines are not too broad and kept too near the signal lines. In the wiring between PCB's one should definitely avoid using 50 ohm cables and also the wave impedance must be high.

CROSS TALK

The considerations that cross talk can be kept low are uncritical, if ground line or a ground plate is nearby. A ground line that runs between two signal lines eliminates almost all cross talk and should be used whenever the situation becomes too critical. A special problematic situation occurs, when signal lines run next to each other with a logical flow (signal flow) on opposite directions. Then it will be generally advisable to run a ground line between the two signal lines, specially for the more critical cases of TTL and ECL IC's.

GROUND AND SUPPLY LINE NOISE

This is perhaps the most serious problem with TTL - IC's and is present in reduced form with ECL - IC's and in very much reduced form, with CMOS IC's. This problem can definitely be solved with proper PCB layout and with a few, very simple measures.

The two principal measures are:

a. To have a low impedance Zw between proper supply line and ground line. This is obtained by providing a large copper surface for ground either full ground broad as it is possible in the case of multilayer boards or at least a ground mesh on finally leaving the copper in all unused ports of PCB such as corners etc., and connecting it to the ground.

Current spikes are drawn from the Vcc line and fed in to the ground line during the IC's transition. These currect spikes are partly needed to charge or discharge the transistor within the IC while they switch and this current is referred as internal current spike which is required to chage on discharge the transmission lines (i.e., conductors) connected to the IC's output. Internal and external spike are super imposed and must be carried by the same Vcc and ground lines. If many synchronous gates or flip flops are connected to the same point, the situation becomes even worse. Thus ground and supply line noise is reduced.

CHAPTER 11

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CMOS FEATURES

Complimentary metal oxide semiconductors (CMOS)

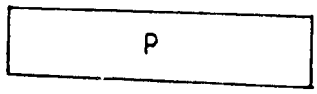
Advantages

1. It is ultra low in cost.
2. It is available in hundreds of devices from a dozen major manufacturers.
3. Works over a wide, non critical power supply range.
4. It uses zero power when inputs aren't changing and very little power when they are.
5. Inputs are essentially opencircuits, and its outputs swing the whole range between supply limits.
6. Output drive to other CMOS packages in unlimited.
7. It is very forgiving to system noise and does'nt generate much noise on its own.
8. It is easily converted to linear operation and offers dozens of options towards high performance, count timers, oscillators and pulse sources.

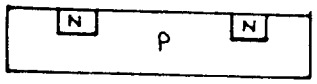
The above mentioned advantages are ample reasons for chosing CMOS IC's for this project.

The CMOS process

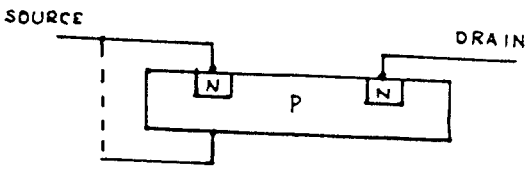
Fig (A-1) shows how we build a transistor called an n-channel enhancement mode Mos devise. We start with a bar of



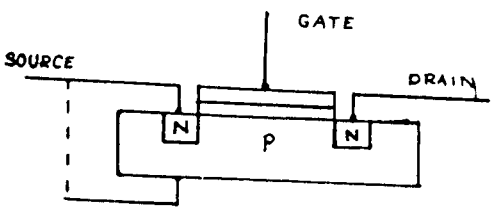
START WITH A BLOCK OF P-TYPE SILICO
(P MATERIAL HAS EXCESS HOLES)



DIFFUSE OR IMPLANT TWO N REGIONS, FORMING PN JUNCTIONS.(N REGIONS HAVE EXCESS ELECTRONS)

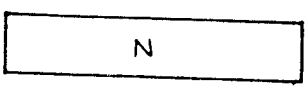


ADD OHMIC CONTACTS AND CALL THE THREE REGIONS SOURCE, DRAIN, AND SUBSTRATE. FOR SOME USES SOURCE AND SUBSTRATE MAY BE CONNECTED TOGETHER. (OHMIC CONTACTS ARE CONNECTIONS THAT DONT RECTIFY)

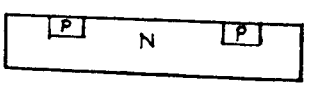


A VERY THIN LAYER OF SIO_2 OR ANOTHE INSULATOR IS BUILT UP BETWEEN SOURC AND DRAIN, A CONDUCTOR IS ADDED TO THE TOP OF THIS INSULATOR, FORMING A CAPACITOR.

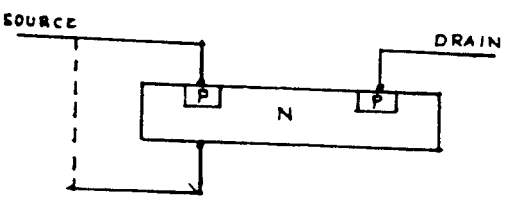
FIG A-1. BUILDING AN n-channel MOS transistor.



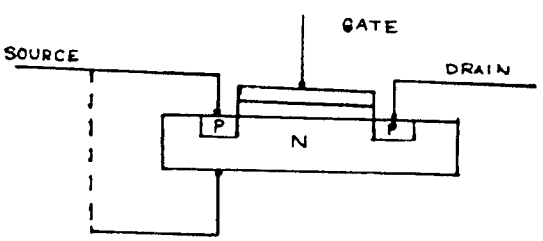
START WITH A BLOCK OF N-TYPE SILICON.



DIFFUSE OR IMPLANT TWO P REGIONS FORMING PN JUNCTIONS.



ADD OHMIC CONTACTS AND CALL THE THREE REGIONS SOURCE, DRAIN, AND SUBSTRATE.



A VERY THIN LAYER OF SIO_2 OR ANOTHER INSULATOR IS BUILT UP BETWEEN SOURCE AND DRAIN. A CONDUCTOR IS ADDED TO THE TOP OF THIS INSULATOR , FORMING A CAPA-CITOR.

FIG A-2. BUILDING A P-CHANNEL MOS TRANSISTOR

p-type silicon. P-type silicon is ultrapure, single crystal silicon (derived from ordinary beach sand). With just enough of an impurity introduced that there all too few electrones to go around. The absence of an electron where an electron is expected to be is called a hole. We say that P-type silicon has an excess of holes. A hole has an equivalent positive charge that equals and offsets the negative charge of an electron.

Now we diffuse two junctions into our silicon block, or substrate. This builds up two n-type silicon regions. The n-type silicon regions have an excess of electrones in them. These two regions are introduced by diffusing or ion-implanting, additional impurities that are carefully selected to tip the balance towards an excess of electrones in these new regions.

P-N junction conducts current when P is more positive than N, blocks current when N is more positive.

Ohmic contacts are made with the three regions of the silicon bar. One of the n-regions is called the source and the other n-region the drain.

To control the current flow between out source/substrate terminal and our drain terminal, we build a

special capacitor between source and drain on the surface of the transistor.

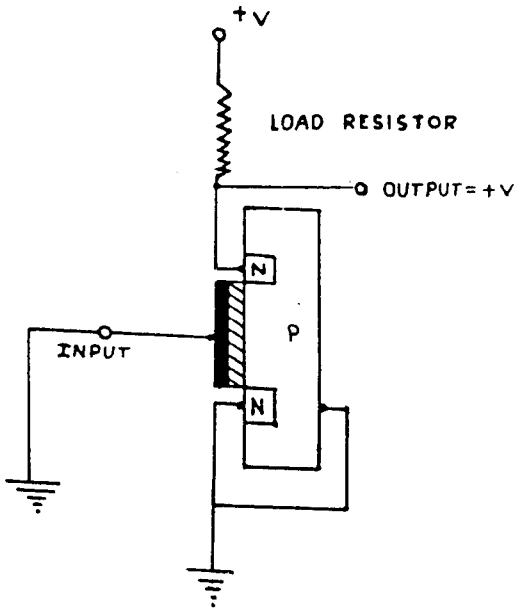
We begin building our capacitor with a dielectric or insulating layer of silicon dioxide, glass, or some other insulator. This layer of dielectric is extremely thin. On top of this insulator we place a new conductor we call a gate. An ohmic contact is provided for the gate too, called the gate lead. The conductor can be a metal. Silicon gates are more sensitive and faster.

Biasing voltages or currents are applied to this basic transistor to actuate this device.

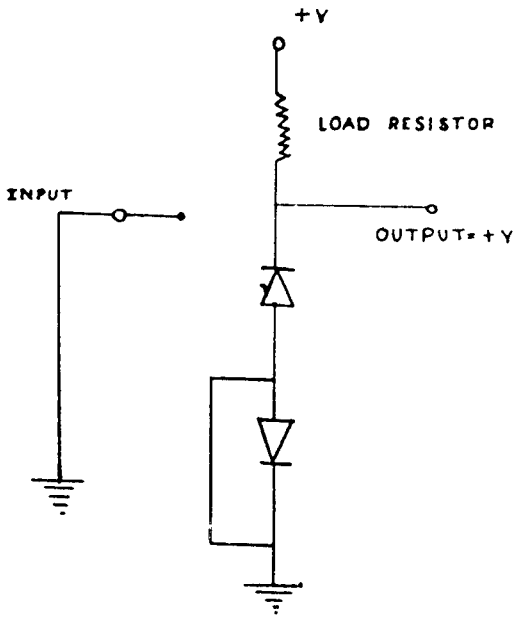
Fig A-3 shows how we bias our transistor. We usually are the gate as the input, drain as the output, substrate and source all connected to ground or some other voltage.

In Fig.A-3 (a) we have grounded our source and substrate and drain connected to a -ve voltate, +V, through a load resistor. Gate input is also grounded.

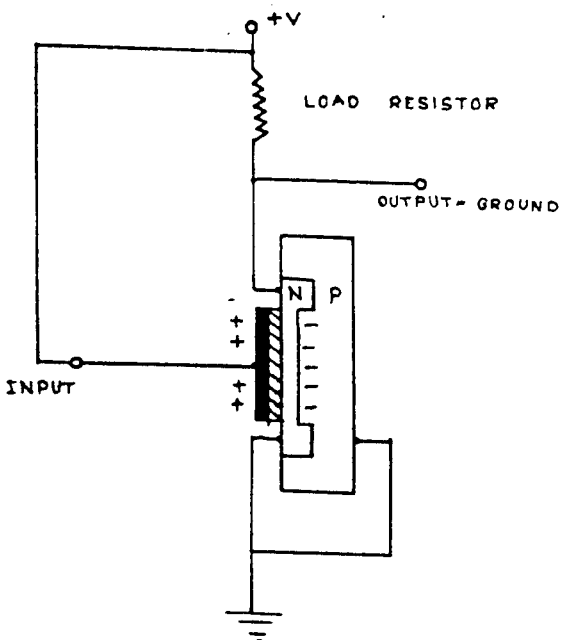
Due to the circuit connections the drain junction acts as a reverse bias (open circuit). The capacitor being grounded doesnot charge. So the output become +Vcc. So a grounded I/P gies a +ve O/P.



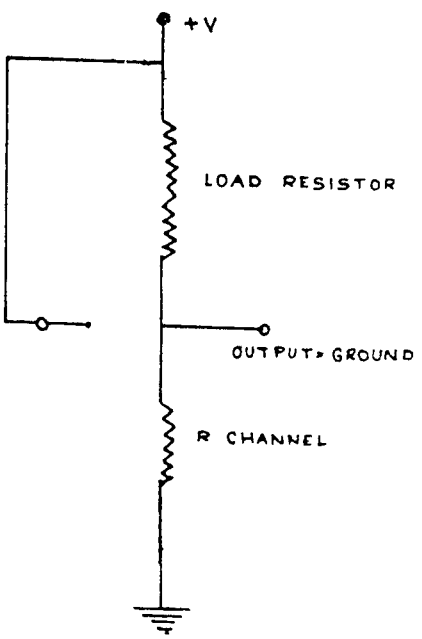
(A) OFF. Grounded input prevents channel from forming. Output is high.



(B) Equivalent OFF circuit.

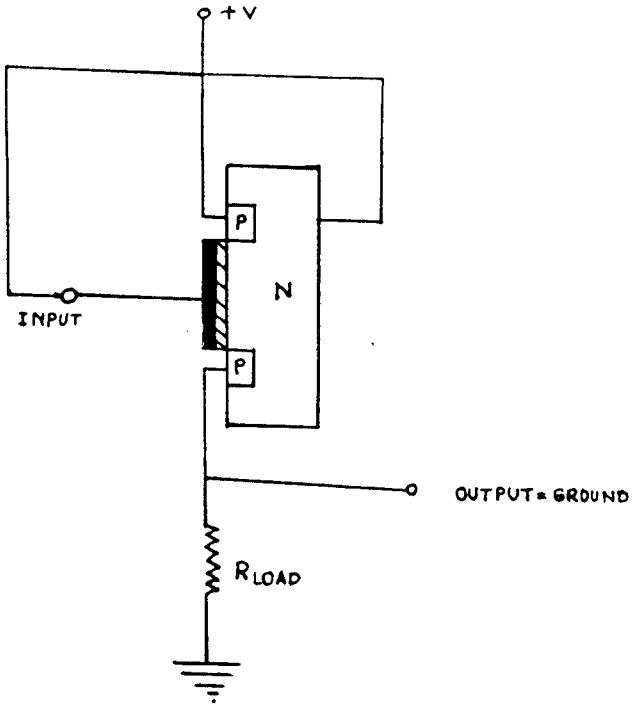


(C) ON. + V gate input forms low resistance n-channel.

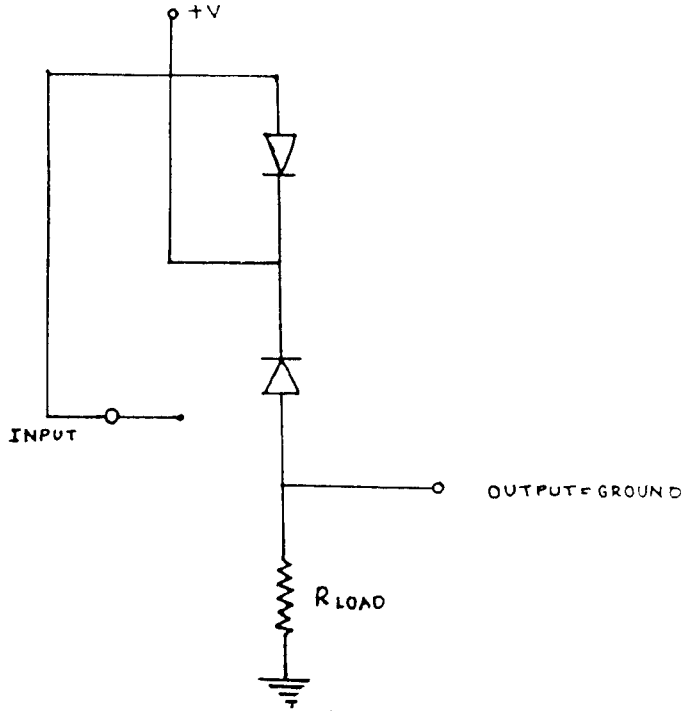


(D) Equivalent ON circuit.

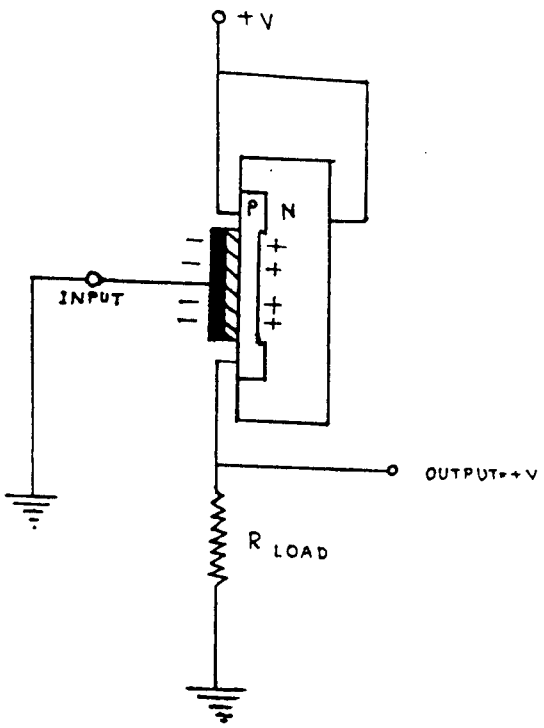
Fig.A-3. BIASING AN N-CHANNEL MOS TRANSISTOR.



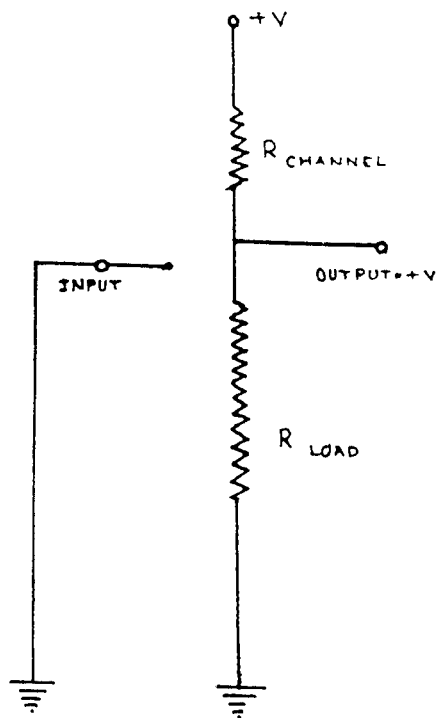
(A) OFF. Input at + V Prevents channel from forming. Output is grounded.



(B) Equivalent OFF circuit.



(C) ON. Grounded gate input forms low-resistance p-channel in response to charge on gate.



(D) Equivalent ON circuit.

Fig.A-4. BIASING A P-CHANNEL MOS TRANSISTOR.

If gate is connected to the supply +v source as in fig 4.3. (c). The left side of the capacitor now has positive charges, or holes, placed on it. When the capacitor charges, it must end up with extra electrons on the right side.

The surface just under the dielectric was a p-type material meaning it was deficient of electrons. The building up of electrones neutralise the holes in the p-type material and hence the whole region becomes intrinsic. More electrones cause the substrate to turn to n type material at the surface.

Thus we have a n channel connecting the drain and source. So now a short circuit occurs between drain and source terminals to ground. So the output becomes zero. So we have turned the transistor on by applying a +ve gate voltage. The amount of voltage needed to turn the transistor on is called the threshold voltage. Since our transistor is normally off, and since we have to force it on by actively doing something to it, it is called an enhancement mode device.

Note:

1. Input is always open circuit since gate lead goes only to a capacitor hence no I/P current needed.
2. When the transistor turns on, it is simply a solid bar of material or a plain resister.

APPENDIX - A

The construction, biasing and equivalent circuits of the P channel mosfet is shown in the figures above. The only difference between P-channel and n-channel mosfets are that they are exactly the opposite in operation.

Here a grounded gate produces a low voltage at the output (transistor on). A +ue voltage applied to the gate produces a high voltage at the output (transistor off). Here the substrate and drain are tied together and the source is grounded through the load resistor.

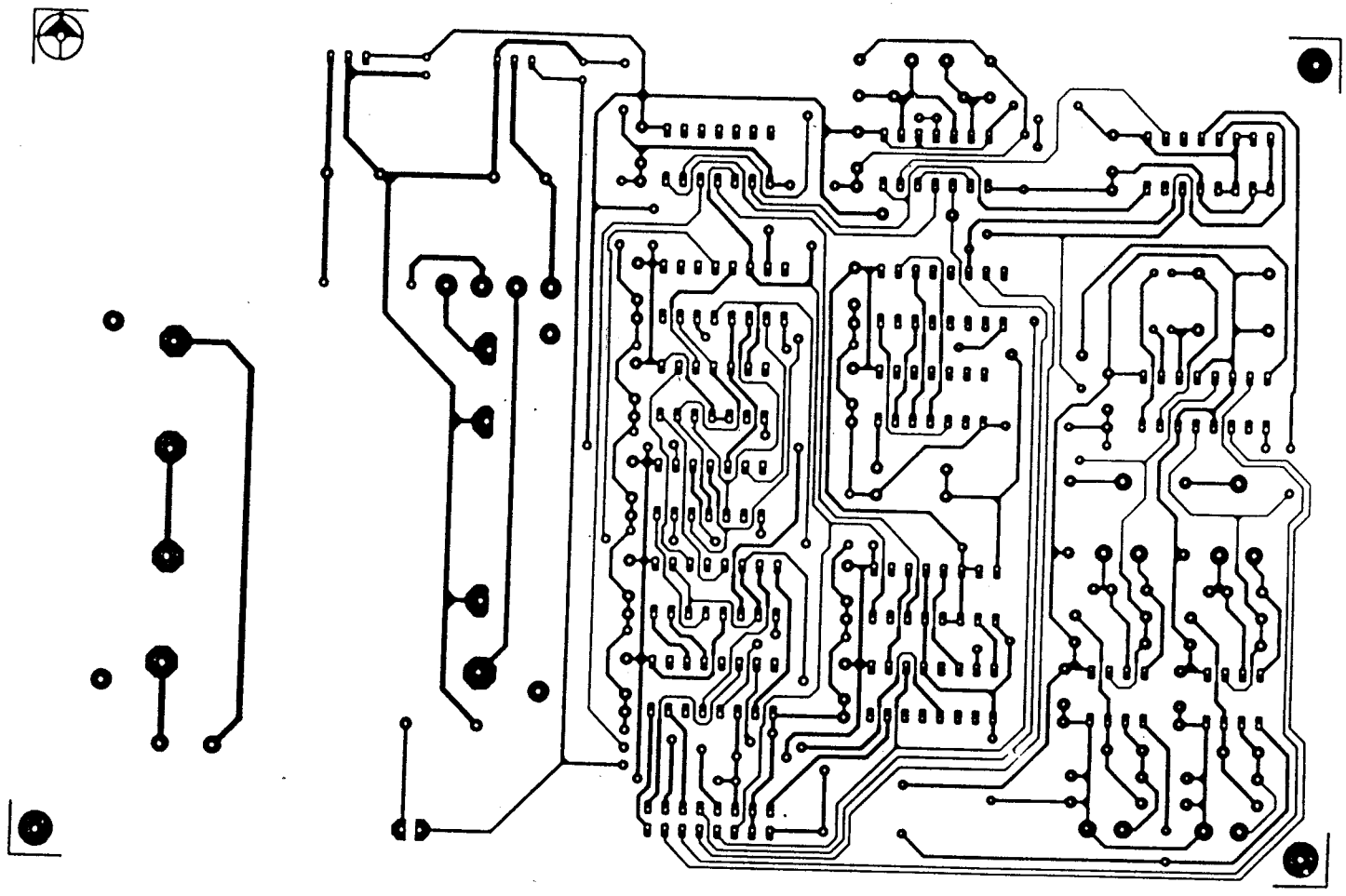


FIG. B-1 TRACK SIDE LAYOUT OF THE MOTHER BOARD

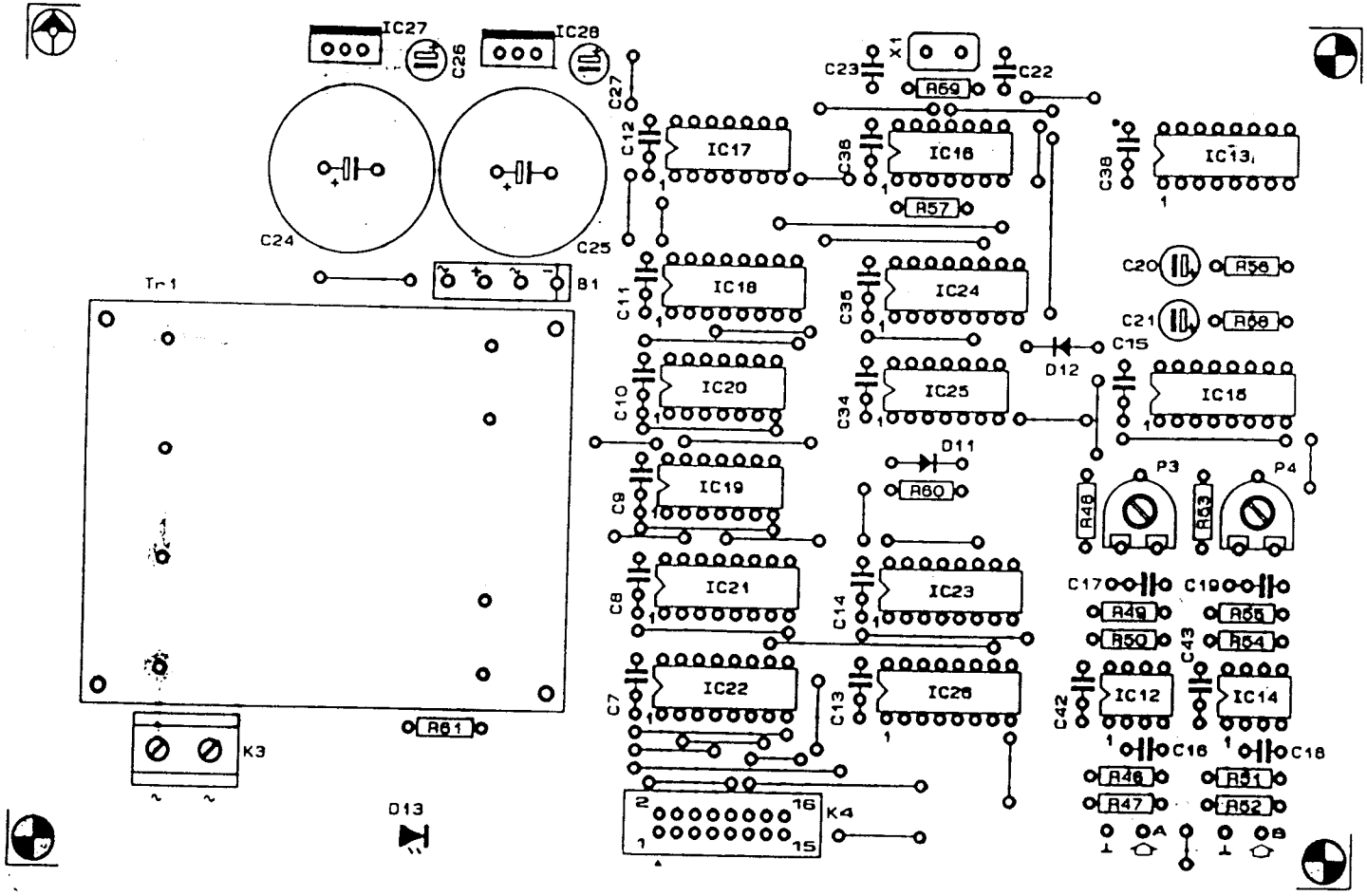


FIG. B-2 COMPONENT SIDE LAYOUT OF THE MOTHER BOARD

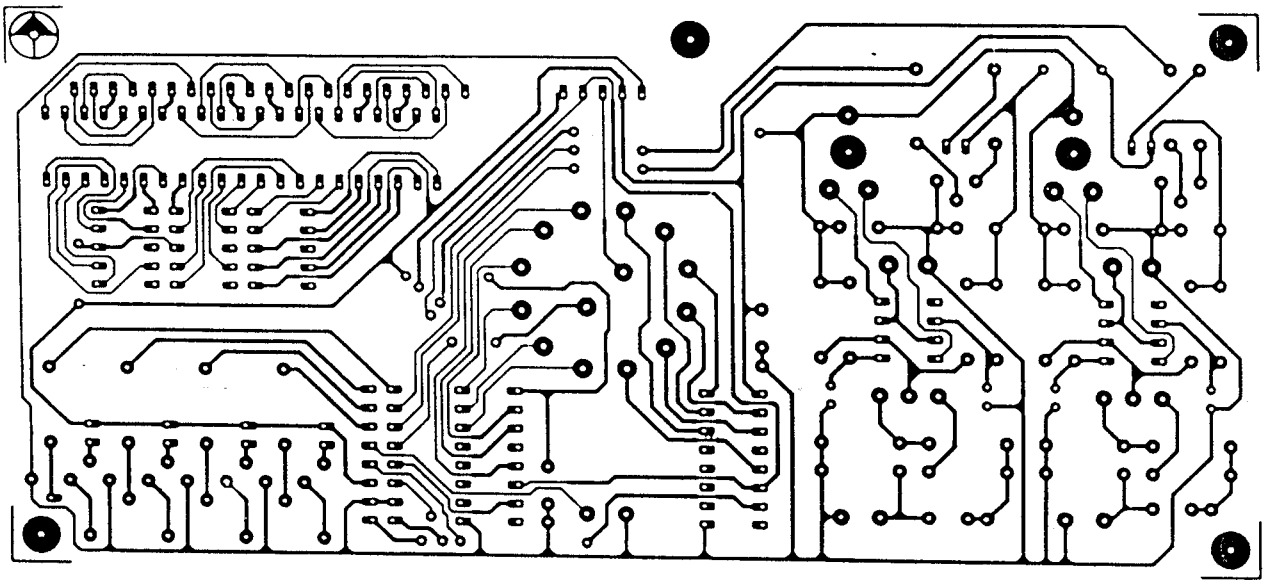


FIG. B-3 TRACK SIDE LAYOUT FOR THE DISPLAYS, INPUT STAGES AND SELECTOR SWITCHES.

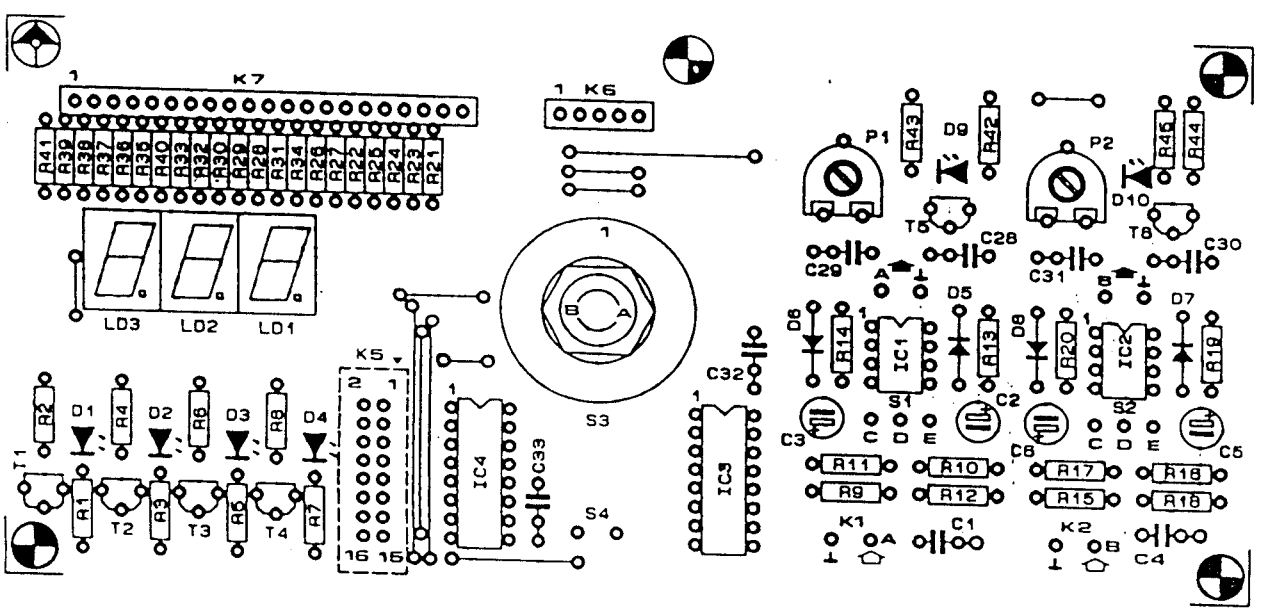


FIG. B-4 COMPONENT SIDE LAYOUT FOR THE DISPLAYS, INPUT STAGES AND SELECTOR SWITCHES.

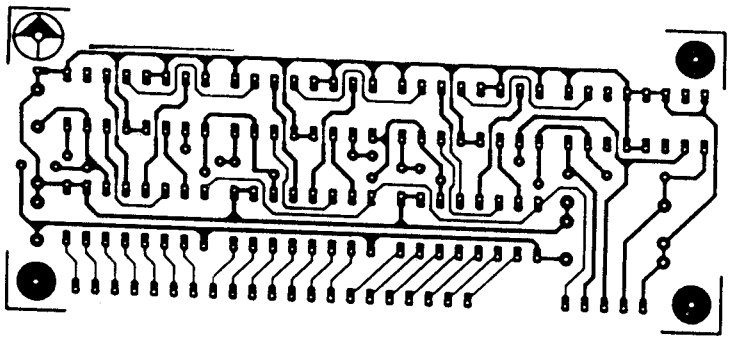


FIG. B-5 TRACK SIDE LAYOUT FOR THE LOGIC CIRCUITS FOR THE LED DISPLAYS

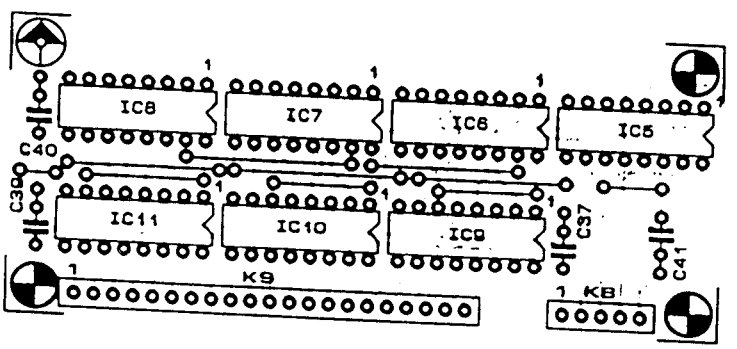


FIG. B-6 COMPONENT SIDE LAYOUT FOR THE LOGIC CIRCUITS FOR THE LED DISPLAYS

RCA

BiMOS Operational Amplifiers

With MOS/FET input, bipolar output

The CA3140B, CA3140A, and CA 3140 are integrated-circuit operational amplifiers that combine the advantages of high-voltage PMOS transistors with high-voltage bipolar transitors on a single monolithic chip. Because of this unique combination of technologies, this device can now provide designers, for the first time, with the special performance features of the CA 3130 COS/MOS operational amplifiers and the versatility of the 741 series of industry-standard operational amplifiers.

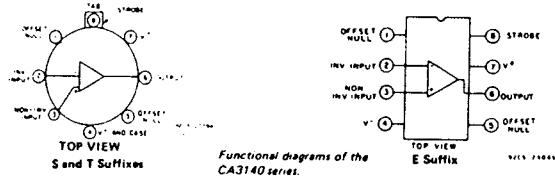
The CA 3140, CA 3140A, and CA 3140 BiMOS operational amplifiers feature gate-protected MOS/FET (PMOS) transistors in the input circuit to provide very-high-input impedance, very-low-input current, and high-speed performance. The CA 3140B operates at supply voltages from 4 to 44 volts; the CA 3140A and CA 3140 from 4 to 36 volts (either single or dual supply). These operational amplifiers are internally phase-compensated to achieve stable operation in unity-gain follower operation, and, additionally, have access terminals for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset-voltage nulling. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute for single-supply applications. The output stage uses bipolar transistors and includes built-in protection against damage from load terminal short-circuiting to either supply-rail or to ground.

The CA 3140 series has the same 8-lead terminal pin-out used for the '741' and other industry-standard operational amplifiers. They are supplied in either the standard 8-lead TO-5 style package (T suffix), or in the 8-lead dual-in-line formed-lead TO-5 style package 'DIL-CAN' (S suffix). The CA 3140 is available in chip form (H suffix). The CA3140A and CA 3140 are also available in an 8-lead dual-in-line plastic package (Mini-DIP-E suffix). The CA 3140B is intended for operation at supply voltages ranging from 4 to 44 volts, for applications requiring premium-grade specifications and with electrical limits established for operations over the range from −55°C to +125°C. The CA 3140A and CA 3140 are for operation at supply voltages up to 36 volts (± 18 volts). All types can be operated safely over the temperature range from −55°C to +125°C.

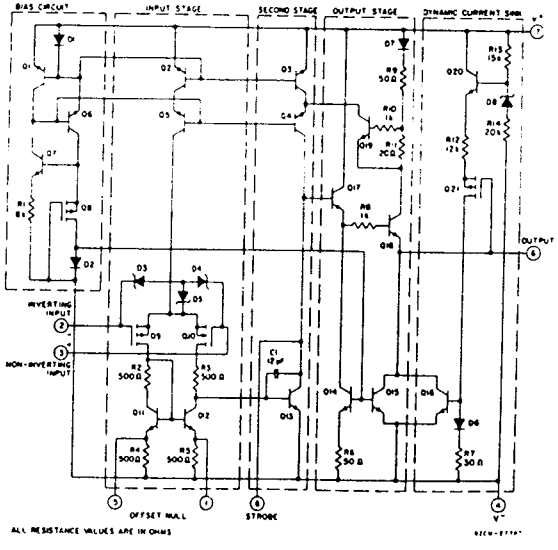
Maximum ratings, *absolute-maximum values:*

	CA 3140, CA 3140A	CA 3140B
DC supply voltage (Between V^+ and V^- terminals)	36 V	44 V
Differential-mode input voltage	± 8 V	± 8 V
Common-mode DC input voltage	(V^+ +8 V) to (V^- −0.5 V)	
Input-terminal current		1 mA
Device dissipation:		
without heatsink:		
up to 55°C		630 mW
above 55°C		derate linearly 6.67 mW/°C
with heat sink:		
up to 55°C		1 W
above 55°C		derate linearly 16.7 mW/°C
Temperature range:		
Operating (all types)		−55 to +125°C
storage (all types)		−65 to +150°C
Output short-circuit duration*		Indefinite
Lead temperature (during soldering): at distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.:		+265°C

* Short circuit may be applied to ground or to either supply.



Functional diagrams of the CA3140 series.



Schematic diagram of CA3140 series.

TYPICAL ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS V^+ = +15 V, V^- = −15 V, T_A = 25°C		CA3140B (T,S)	CA3140A (T,S,E)	CA3140 (T,S,E)	UNITS
Input Offset Voltage Adjustment Resistor		Typ. Value of Resistor Between Term. 4 and 5 or 4 and 1 to Adjust Max. V_{IO}		43	18	4.7	kΩ
Input Resistance	R_I			1.5	1.5	1.5	TΩ
Input Capacitance	C_i			4	4	4	pF
Output Resistance	R_O			60	60	60	Ω
Equivalent Wideband Input Noise Voltage	e_n	BW = 140 kHz, R_S = 1 MΩ		48	48	48	μV
Equivalent Inout Noise Voltage	e_n	f = 1 kHz	R_S = 100 Ω	40	40	40	nV/√Hz
		f = 10 kHz		12	12	12	
Short-Circuit Current to Opposite Supply	Source I_{OM^+}			40	40	40	mA
	Sink I_{OM^-}			18	18	18	mA
Gain-Bandwidth Product	f_T			4.5	4.5	4.5	MHz
Slew Rate	SR			9	9	9	V/μs
Sink Current From Terminal 8 To Terminal 4 to Swing Output Low				220	220	220	μA
Transient Response: Rise Time	t_r	R_L = 2 kΩ, C_L = 100 pF		0.08	0.08	0.08	μs
Overshoot				10	10	10	%
Settling Time at 10 V_{p-p}	1 mV	t_s	R_L = 2 kΩ, C_L = 100 pF, Voltage Follower	4.5	4.5	4.5	μs
	10 mV			1.4	1.4	1.4	

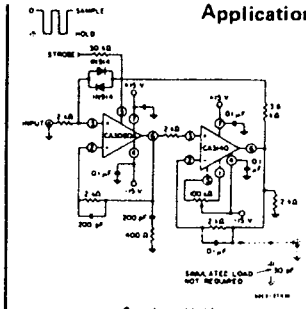
Features:

- MOS/FET input stage
  a. very high input impedance (Z_{IN}) — 1.5 TΩ typ.
  b. Very low input current (I_I) — 10 pA typ. at ± 15 V
  c. Low input-offset voltage (V_{IO}) — to 2 mV max.
  d. Wide common-mode input-voltage range (V_{ICR}) — can be swung 0.5 volt below negative supply-voltage rail
  e. Output swing complements input common-mode range
  f. Rugged input stage — bipolar diode protected
- Directly replaces industry type 741 in most applications
- Includes numerous industry operational amplifier categories such as general-purpose, FET input, wideband (high slew rate)
- Operation from 4-to-44 volts single or dual supplies
- Internally compensated
- Characterised from ± 15-volt operation and for TTL supply systems with operation down to 4 volts
- Wide bandwidth — 4.5 MHz unity gain at ± 15 V or 30 V; 3.7 MHz at 5 V
- High voltage-follower slew rate — 9 V/μs
- Fast settling time — 1.4 μs typ. to 10 mV with a 10-V_{p-p} signal
- Output swings to within 0.2 volt of negative sypply
- Strobable output stage

Applications:

- Ground-referenced single-supply amplifiers in automobile and portable instrumentation
- Sample and hold amplifiers
- Long-duration timers/multivibrators (micro-seconds-minutes-hours)
- Photocurrent instrumentation
- Peak detectors
- Active filters
- Comparators
- Interface in 5 V TTL systems & other low-supply voltage systems
- All standard operational amplifier applications
- Function generator
- Tone controls
- Power supplies
- Portable instruments
- Intrusion alarm systems

Application



Sample- and hold circuit.

National Semiconductor

LM 79XXC

3-terminal negative voltage regulators

The LM 79XXC series of 3-terminal regulators is available with fixed output voltages. These devices need only one external component – a compensation capacitor at the output. The LM 79XX series is packaged in the TO-220 power package and is capable of supplying 1.5 A of output current.

These regulators employ internal current limiting safe area protection and thermal shutdown for protection against all overload conditions.

Low ground pin current of the LM 79XXC series allows output voltage to be easily boosted above the preset value with a resistor divider. The low quiescent current drain of these devices with a specified maximum change with line and load ensures good regulation in the voltage boosted mode.

Features

- Thermal, short circuit and safe area protection
- High ripple rejection
- 1.5 A output current
- 4% preset output voltage

National only the 5 V, 12 V and 15 V types.

LM 79LXX

The LM 79LXXAC series of 3-terminal negative voltage regulators features fixed output voltages and with output current capabilities in excess of 100 mA. These devices were designed using the latest computer techniques for optimising the packaged IC thermal/electrical performance. The LM 79LXXAC series, even when combined with a minimum output compensation capacitor of 0.1 μF, exhibits an excellent transient response, a maximum line regulation of 0.07% V_O/V, and a maximum load regulation of 0.01% V_O/mA.

The LM 79LXXAC series also includes, as self-protection circuitry: safe operating area circuitry for output transistor power dissipation limiting, a temperature independent short circuit current limit for peak output current limiting, and a thermal shutdown circuit to prevent excessive junction temperature. Although designed primarily as fixed voltage regulators, these devices may be combined with simple external circuitry for boosted and/or adjustable voltages and currents. The LM 79LXXAC series is available in the 3-lead TO-92 package.

Features

- Preset output voltage error is less than ± 5% over load, line and temperature
- Specified at an output current of 100 mA
- Easily compensated with a small 0.1 μF output capacitor
- Internal short-circuit, thermal and safe operating area protection
- Easily adjustable to higher output voltages
- Maximum line regulation less than 0.07% V_{OUT}/V
- Maximum load regulation less than 0.01% V_{OUT}/mA
- TO-92 package

LM 79MXX

The LM 79MXX series of 3-terminal regulators is available with fixed output voltages and these devices need only one external component – a compensation capacitor at the output. The LM 79MXX series is packaged in the TO-202 power package and TO-39 metal can and is capable of supplying 0.5 A output current.

These regulators employ internal current limiting safe area protection and thermal shutdown for protection against virtually all overload conditions.

Low ground pin current of the LM 79MXX series allows output voltage to be easily boosted above the preset value with a resistor divider. The low quiescent current drain of these devices with a specified maximum change with line and load ensures good regulation in the voltage boosted mode.

Features

- Thermal, short circuit and safe area protection
- High ripple rejection
- 0.5 A output current
- 4% preset output voltage

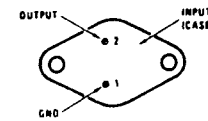
National Semiconductor

Electrical characteristics

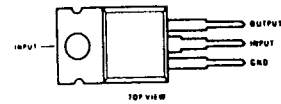
Type	U_{out} (V)	I_{out} (A) 79XXC	79LXX	79MXX	U_{in} (V) min.	max.
7905	–5	1,5	0,1	0,5	–20	– 7,5
7905,2	–5,2	1,5	–	–	–20,5	– 7,5
7906	–6	1,5	–	0,5	–21	– 8
7908	–8	1,5	–	0,5	–23	–10,5
7909	–9	1,5	–	–	–24	–11,5
7912	–12	1,5	0,1	0,5	–27	–14,5
7915	–15	1,5	0,1	0,5	–30	–18
7918	–18	1,5	0,1	–	–33	–21
7924	–24	1,5	0,1	0,5	–38	–24

Connection Diagrams

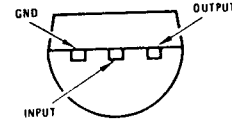
TO-3 Package (K)



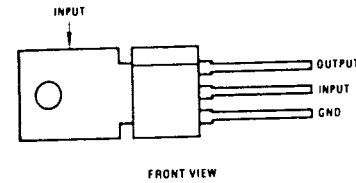
TO-220 Package (T)



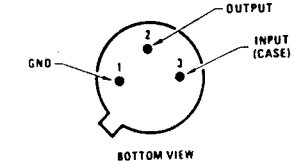
TO-92 Plastic Package (Z)



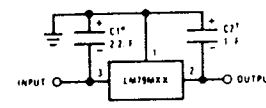
Power Package TO-202 (P)



Metal Can Package TO-39 (H)
Order Number:



Fixed Regulator



*Required if regulator is separated from filter capacitor by more than 3". For value given, capacitor must be solid tantalum. 25μF aluminum electrolytic may be substituted.

†Required for stability. For value given, capacitor must be solid tantalum. 25μF aluminum electrolytic may be substituted. Values given may be increased without limit.

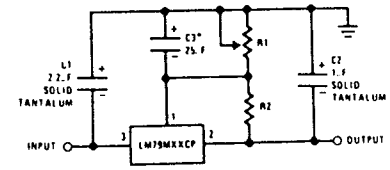
For output capacitance in excess of 100μF, a high current diode from input to output (1N4001, etc.) will protect the regulator from momentary input shorts.

$$V_{OUT} = V_{SET}\left(\frac{R1 + R2}{R2}\right)$$

Select R2 as follows:

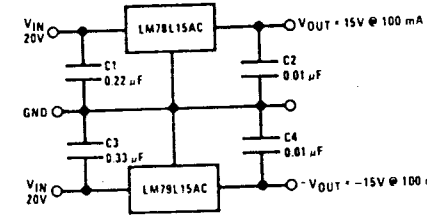
LM79M05CP	300Ω
LM79M06CP	300Ω
LM79M08CP	470Ω
LM79M12CP	750Ω
LM79M15CP	1k
LM79M24CP	2.5k

Variable Output



*Improves transient response and ripple rejection. Do not increase beyond 50μF.

±15V, 100 mA Dual Power Supply



National Semiconductor

3-terminal positive voltage regulator

The LM 78XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

National only the 5 V, 12 V and 15 V types.

LM 78XXC

The LM 78XX series is available in an aluminium TO-3 package wich will allow over 1.0 A load current if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.
Considerable effort was expended to make the LM 78XX series of regulators easy to use and minimise the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

Features

- Output current in excess of 1 A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in the aluminium TO-3 package

LM 78LXX

The LM 78LXX is available in the metal three lead TO-39 (H) and the plastic TO-92 (Z) With adequate heat sinking the regulator can deliver 100 mA output current. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Features

- Output voltage tolerances of ± 5% (LM 78LXXAC) and ± 10% (LM 78LXXC) over the temperature range
- Output current of 100 mA
- Internal thermal overload protection
- Output transistor safe area protection
- Internal short circuit current limit
- Available in plastic TO-92 and metal TO-39 low profile packages

Electrical characteristics

Type	U_{out} (V)	I_{out} (A) 78XXC	78LXX	78MXX	U_{in} (V) min.	max.
7805	5	1	0,1	0,5	7,5	20
7806	6	1	0,1	0,5	8,6	21
7808	8	1	0,1	0,5	10,6	23
7810	10	1	0,1	0,5	12,7	25
7812	12	1	0,1	0,5	14,8	27
7815	15	1	0,1	0,5	18	30
7818	18	1	0,1	0,5	21	33
7824	24	1	0,1	0,5	27,3	38

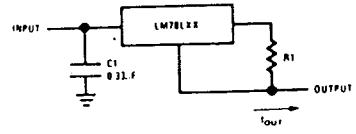
National Semiconductor

LM 78MXX

The LM 78MXX series is available in the plastic TO-202 package. This package allows these regulators to deliver over 0,5 A if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.
Considerable effort was expended to make the LM-78MXX series of regulators easy to use and minimise the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

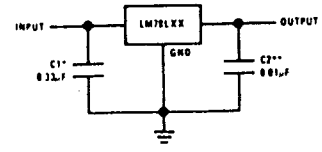
Features

- Output current in excess of 0.5 A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in plastic TO-202 package
- Special circuitry allows start-up even if output is pulled to negative voltage (± supplies)



$I_{out} = (V_{33}/R1) + I_Q$
$\geq I_Q + 1.5$ mA over line and load changes

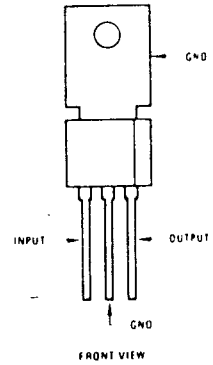
Current Regulator



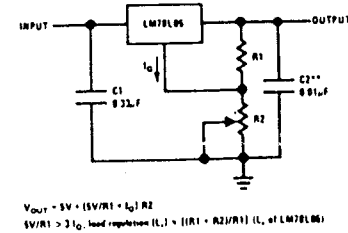
*Required if the regulator is located far from the power supply filter
**See Note 3 on the electrical characteristics table

Fixed Output Regulator

Plastic Package



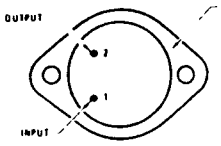
FRONT VIEW



$V_{OUT} = 5V + (5V/R1 + I_Q) R2$
$5V/R1 > 3\,I_Q$, load regulation (L_r) = $(R1 + R2)/R1$ (L_r of LM78L05)

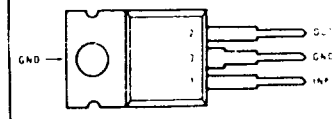
Adjustable Output Regulator

Metal Can Package
TO-3 (K)
Aluminum



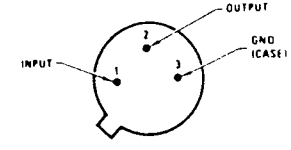
BOTTOM VIEW

Plastic Package
TO-220 (T)



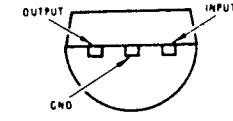
TOP VIEW

Metal Can Package



BOTTOM VIEW

Plastic Package



BOTTOM VIEW

5-STAGE JOHNSON COUNTER

The HEF4017B is a 5-stage Johnson decade counter with ten spike-free decoded active HIGH outputs (O_0 to O_9), an active LOW output from the most significant flip-flop ($\overline{O}_{5-9}$), active HIGH and active LOW clock inputs (CP_0, $\overline{CP}_1$) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW to HIGH transition at CP_0 while $\overline{CP}_1$ is LOW or a HIGH to LOW transition at $\overline{CP}_1$ while CP_0 is HIGH (see also function table).

When cascading counters, the $\overline{O}_{5-9}$ output, which is LOW while the counter is in states 5, 6, 7, 8 and 9, can be used to drive the CP_0 input of the next counter.

A HIGH on MR resets the counter to zero ($O_0 = \overline{O}_{5-9}$ = HIGH; O_1 to O_9 = LOW) independent of the clock inputs (CP_0, $\overline{CP}_1$).

Automatic code correction of the counter is provided by an internal circuit: following any illegal code the counter returns to a proper counting mode within 11 clock pulses.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

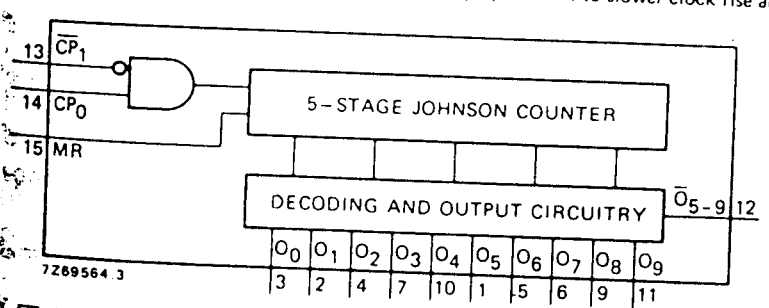


Fig. 1 Functional diagram.

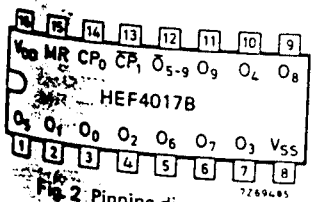


Fig. 2 Pinning diagram.

HEF4017BP : 16-lead DIL; plastic (SOT-38Z).
HEF4017BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4017BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

Pinning

CP_0: clock input (LOW to HIGH triggered)
$\overline{CP}_1$: clock input (HIGH to LOW triggered)
MR: master reset input
O_0 to O_9: decoded outputs
$\overline{O}_{5-9}$: carry output (active LOW)

FUNCTION TABLE

MR	CP_0	$\overline{CP}_1$	operation
H	X	X	$O_0 = \overline{O}_{5\text{-}9} = H$; O_1 to $O_9 = L$
L	H	↘	Counter advances
L	↗	L	Counter advances
L	L	X	No change
L	X	H	No change
L	H	↗	No change
L	↘	L	No change

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
↗ = positive-going transition
↘ = negative-going transition

A.C. CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
$CP_0, \overline{CP}_1 \rightarrow O_0$ to O_9 HIGH to LOW	5	t_{PHL}		140	280	ns	113 ns + (0,55 ns/pF) C_L
	10			55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
LOW to HIGH	5	t_{PLH}		125	250	ns	98 ns + (0,55 ns/pF) C_L
	10			50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
$CP_0, \overline{CP}_1 \rightarrow \overline{O}_{5\text{-}9}$ HIGH to LOW	5	t_{PHL}		145	290	ns	118 ns + (0,55 ns/pF) C_L
	10			55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
LOW to HIGH	5	t_{PLH}		125	250	ns	98 ns + (0,55 ns/pF) C_L
	10			50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
$MR \rightarrow O_1$ to O_9 HIGH to LOW	5	t_{PHL}		115	230	ns	88 ns + (0,55 ns/pF) C_L
	10			50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
$MR \rightarrow \overline{O}_{5\text{-}9}$ LOW to HIGH	5	t_{PLH}		110	220	ns	83 ns + (0,55 ns/pF) C_L
	10			45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
$MR \rightarrow O_0$ LOW to HIGH	5	t_{PLH}		130	260	ns	103 ns + (0,55 ns/pF) C_L
	10			55	105	ns	44 ns + (0,23 ns/pF) C_L
	15			40	75	ns	32 ns + (0,16 ns/pF) C_L
Output transition times							
HIGH to LOW	5	t_{THL}		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10			30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
LOW to HIGH	5	t_{TLH}		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10			30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

14-STAGE BINARY COUNTER

The HEF4020B is a 14-stage binary ripple counter with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve fully buffered outputs (O_0, O_3 to O_{13}). The counter advances on the HIGH to LOW transition of $\overline{CP}$. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$. Each counter stage is a static toggle flip-flop. A feature of the HEF4020B is: high speed (typ. 35 MHz at V_{DD} = 15 V).

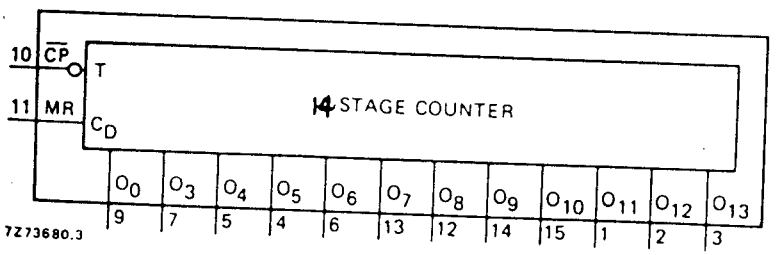


Fig. 1 Functional diagram.

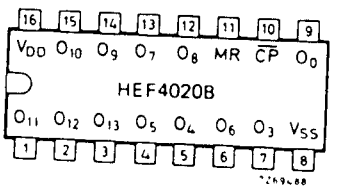


Fig. 2 Pinning diagram.

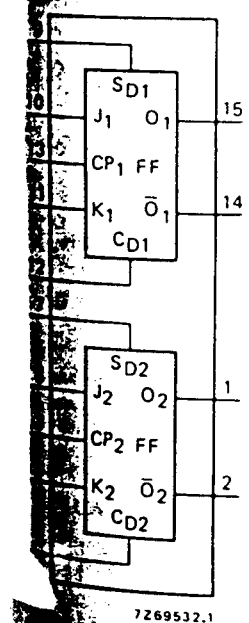
HEF4020BP : 16-lead DIL; plastic (SOT-38Z).
HEF4020BD : 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4020BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

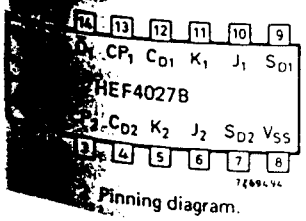
O_3 to O_{13} parallel outputs

DUAL JK FLIP-FLOP

The HEF4027B is a dual JK flip-flop which is edge-triggered and features indepedent set direct (S_D), clear direct (C_D), clock (CP) inputs and outputs (O,$\bar{O}$). Data is accepted when CP is LOW, and transferred to the output on the positive-going edge of the clock. The active HIGH asynchronous clear-direct (C_D) and set-direct (S_D) are independent and override the J, K, and CP inputs. The outputs are buffered for best system performance. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.



Functional diagram.



Pinning diagram.

FUNCTION TABLES

inputs					outputs	
S_D	C_D	CP	J	K	O	$\bar{O}$
H	L	X	X	X	H	L
L	H	X	X	X	L	H
H	H	X	X	X	H	H

inputs					outputs	
S_D	C_D	CP	J	K	O_{n+1}	$\bar{O}_{n+1}$
L	L	∫	L	L	no change	
L	L	∫	H	L	H	L
L	L	∫	L	H	L	H
L	L	∫	H	H	$\bar{O}_n$	O_n

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
O_{n+1} = state after clock positive transition

PINNING

J,K synchronous inputs
CP clock input (L to H edge-triggered)
S_D asynchronous set-direct input (active HIGH)
C_D asynchronous clear-direct input (active HIGH)
O true output
$\bar{O}$ complement output

HEF4027BP : 16-lead DIL; plastic (SOT-38Z).
HEF4027BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4027BT : 16-lead mini-pack; plastic

12-STAGE BINARY COUNTER

4040B is a 12-stage binary ripple counter with a clock input ($\overline{CP}$), an overriding asynchronous **set input** (MR) and twelve fully buffered outputs (O_0 to O_{11}). The counter advances on the **LOW** transition of $\overline{CP}$. A HIGH on MR clears all counter stages and forces all outputs LOW, **dent of** $\overline{CP}$. Each counter stage is a static toggle flip-flop. Schmitt-trigger action in the clock **kes** the circuit highly tolerant to slower clock rise and fall times.

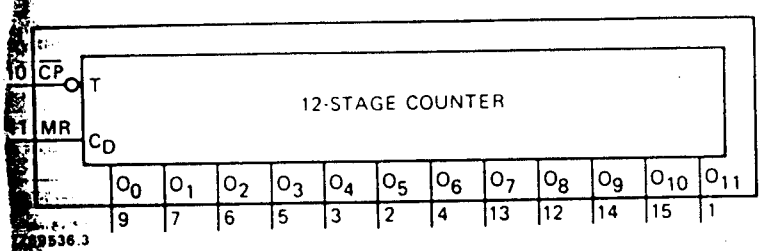


Fig. 1 Functional diagram.

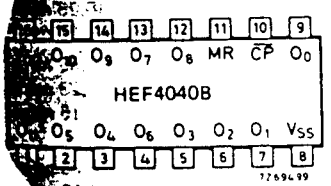


Fig. 2 Pinning diagram.

HEF4040BP : 16-lead DIL; plastic (SOT-38Z);
HEF4040BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4040BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

clock input (HIGH to LOW edge-triggered)
master reset input (active HIGH)
parallel outputs

TION INFORMATION

mples of applications for the HEF4040B are:

ncy dividing circuits
lay circuits
counters

QUADRUPLE D-LATCH

The HEF4042B is a 4-bit latch with four data inputs (D_0 to D_3), four buffered latch outputs (O_0 to O_3), four buffered complementary latch outputs ($\bar{O}_0$ to $\bar{O}_3$) and two common enable inputs (E_0 and E_1). Information on D_0 to D_3 is transferred to O_0 to O_3 while both E_0 and E_1 are in the same state, either HIGH or LOW. O_0 to O_3 follow D_0 to D_3 as long as both E_0 and E_1 remain in the same state. When E_0 and E_1 are different, D_0 to D_3 do not affect O_0 to O_3 and the information in the latch is stored.

$\bar{O}_0$ to $\bar{O}_3$ are always the complement of O_0 to O_3. The exclusive-OR input structure allows the choice of either polarity for E_0 and E_1. With one enable input HIGH, the other enable input is active HIGH; with one enable input LOW, the other enable input is active LOW.

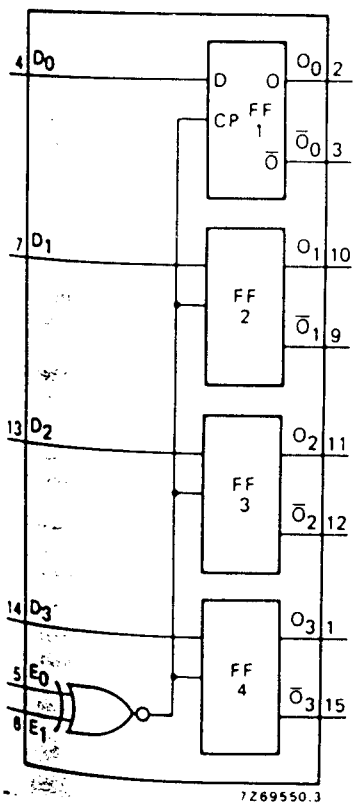


Fig. 1 Functional diagram.

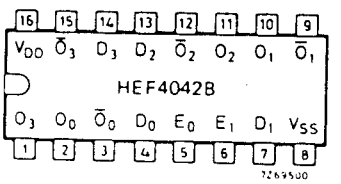


Fig. 2 Pinning diagram.

HEF4042BP: 16-lead DIL; plastic (SOT-38Z).
HEF4042BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4042BT: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

D_0 to D_3	data inputs
E_0 and E_1	enable inputs
O_0 to O_3	parallel latch outputs
$\bar{O}_0$ to $\bar{O}_3$	complementary parallel latch outputs

APPLICATION INFORMATION

Some examples of applications for the HEF4042B are:

- Buffer storage
- Holding register

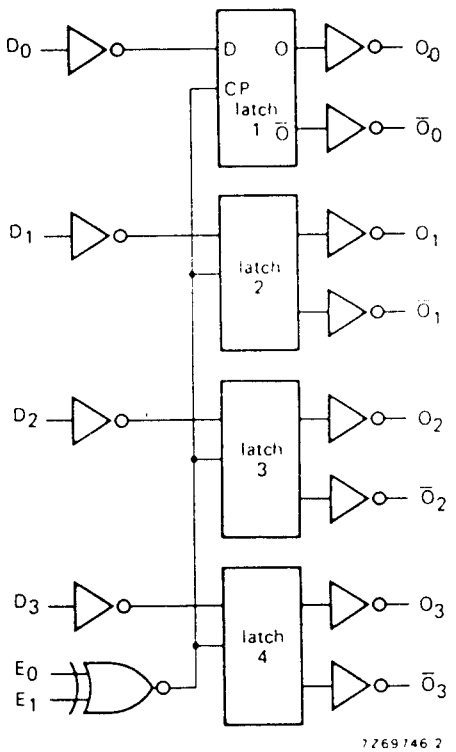


Fig. 3 Logic diagram.

FUNCTION TABLE

E_0	E_1	output O_n
L	L	D_n
L	H	latched
H	L	latched
H	H	D_n

H = HIGH state (the more positive
L = LOW state (the less positive

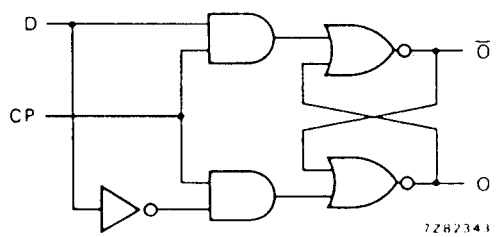


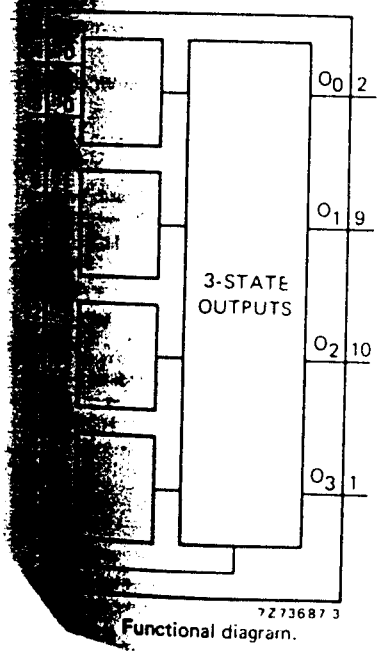
Fig. 4 Logic diagram (one latch).

QUADRUPLE R/S LATCH WITH 3-STATE OUTPUTS

HEF4043B is a quadruple R/S latch with 3-state outputs with a common output enable input (EO). Each latch has an active HIGH set input (S_0 to S_3), an active HIGH reset input (R_0 to R_3) and an active HIGH 3-state output (O_0 to O_3).

When EO is HIGH, the state of the latch output (O_n) can be determined from the function table below. When EO is LOW, the latch outputs are in the high impedance OFF-state. EO does not affect the state of the latch.

The high impedance off-state feature allows common busing of the outputs.



Functional diagram.

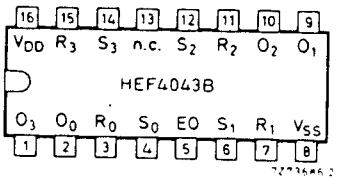


Fig. 2 Pinning diagram.

HEF4043BP : 16-lead DIL; plastic (SOT-38Z).
HEF4043BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4043BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

EO	common output enable input
S_0 to S_3	set inputs (active HIGH)
R_0 to R_3	reset inputs (active HIGH)
O_0 to O_3	3-state buffered latch outputs

FUNCTION TABLE

inputs			output
EO	S_n	R_n	O_n
L	X	X	Z
H	L	H	L
H	H	X	H
H	L	L	latched

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state immaterial
Z = high impedance state

...ogory MSI | see Family Specifications

QUADRUPLE EXCLUSIVE-OR GATE

The HEF4070B provides the positive quadruple exclusive-OR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

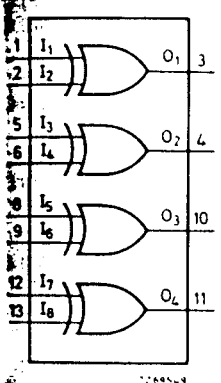


Fig. 1 Functional diagram.

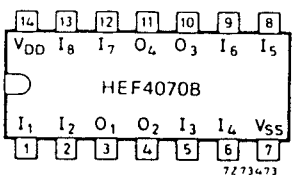


Fig. 2 Pinning diagram.

HEF4070BP : 14-lead DIL; plastic (SOT-27K, M, T).
HEF4070BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4070BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

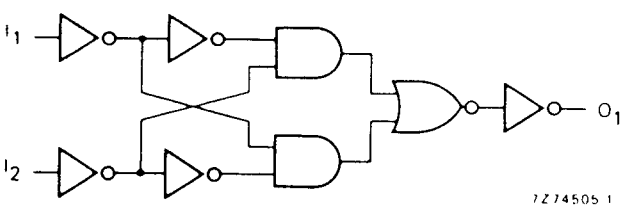


Fig. 3 Logic diagram (one gate).

APPLICATION INFORMATION

Some examples of applications for the HEF4070B are:
- Digital comparators
- Parity checkers and generators

TRUTH TABLE

I_1	I_2	O_1
L	L	L
H	L	H
L	H	H
H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

QUADRUPLE 2-INPUT AND GATE

HEF4081B provides the positive quadruple 2-input AND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

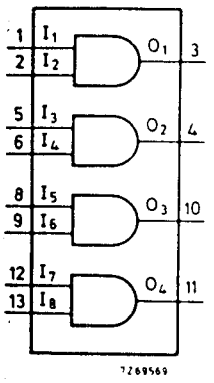


Fig.1 Functional diagram.

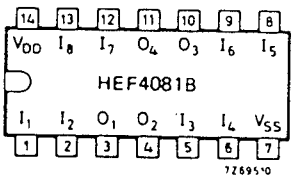
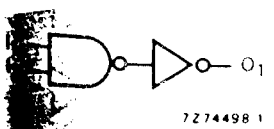


Fig.2 Pinning diagram.

HEF4081BP : 14-lead DIL; plastic (SOT-27K, M, T).
HEF4081BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4081BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).



Logic diagram (one gate).

DUAL 4-INPUT AND GATE

HEF4082B provides the positive dual 4-input AND function. The outputs are fully buffered for best noise immunity and pattern insensitivity of output impedance.

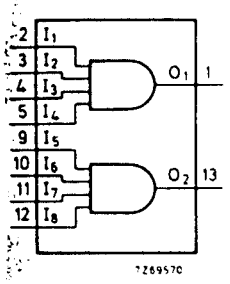


Fig. 1 Functional diagram.

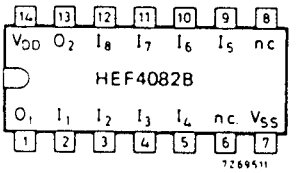


Fig. 2 Pinning diagram.

HEF4082BP : 14-lead DIL; plastic (SOT-27K, M, T).
HEF4082BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4082BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

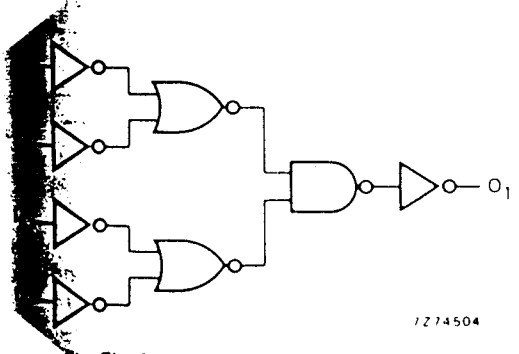


Fig. 3 Logic diagram (one gate).

BCD UP/DOWN COUNTER

The HEF4510B is an edge-triggered synchronous up/down BCD counter with a clock input (CP), an up/down count control input (UP/$\overline{DN}$), an active LOW count enable input ($\overline{CE}$), an asynchronous active HIGH parallel load input (PL), four parallel inputs (P_0 to P_3), four parallel outputs (O_0 to O_3), an active LOW terminal count output ($\overline{TC}$), and an overriding asynchronous master reset input (MR).

Information on P_0 to P_3 is loaded into the counter while PL is HIGH, independent of all other input conditions except the MR input, which must be LOW. With PL LOW, the counter changes on the LOW to HIGH transition of CP if $\overline{CE}$ is LOW. UP/$\overline{DN}$ determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, $\overline{TC}$ is LOW when O_0 and O_3 are HIGH and $\overline{CE}$ is LOW. When counting down, $\overline{TC}$ is LOW when O_0 to O_3 and $\overline{CE}$ are LOW. A HIGH on MR resets the counter (O_0 to O_3 = LOW) independent of all other input conditions.

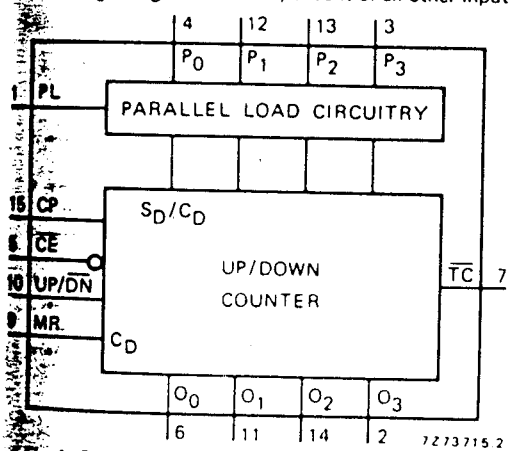


Fig. 1 Functional diagram.

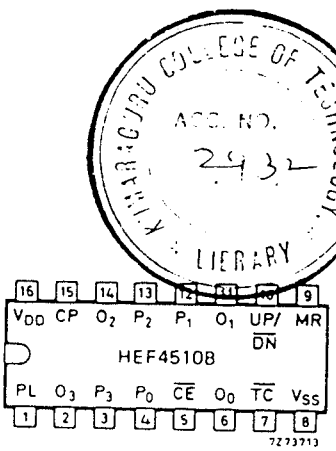


Fig. 2 Pinning diagram.

HEF4510BP: 16-lead DIL; plastic (SOT-38Z).
HEF4510BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4510BT: 16-lead mini-pack; plastic (SO-16L; SOT-162A).

PINNING

PL	parallel load input (active HIGH)	UP/$\overline{DN}$	up/down count control input
P_0 to P_3	parallel inputs	MR	master reset input
$\overline{CE}$	count enable input (active LOW)	$\overline{TC}$	terminal count output (active LOW)
CP	clock pulse input (LOW to HIGH, edge triggered)	O_0 to O_3	parallel outputs

FUNCTION TABLE

MR	PL	UP/$\overline{DN}$	$\overline{CE}$	CP	mode
L	H	X	X	X	parallel load
L	L	X	H	X	no change
L	L	L	L	∫	count down
L	L	H	L	∫	count up
H	X	X	X	X	reset

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition

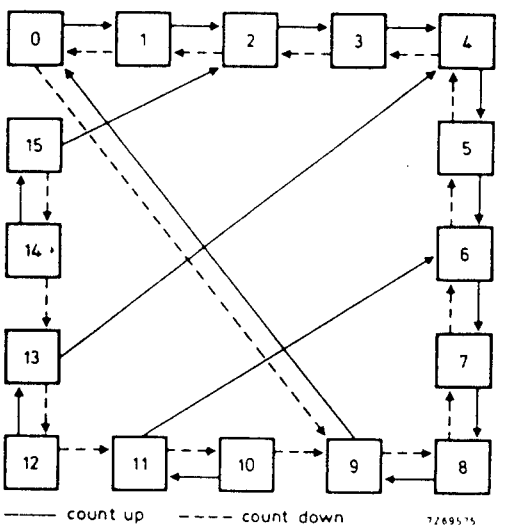


Fig. 4 State diagram.

Logic equation for terminal count:

$$\overline{TC} = \overline{\overline{CE} \cdot \{ (UP/\overline{DN}) \cdot O_0 \cdot O_3 + \overline{(UP/\overline{DN})} \cdot \overline{O}_0 \cdot \overline{O}_1 \cdot \overline{O}_2 \cdot \overline{O}_3 \}}$$

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1000 f_i + Σ($f_o C_L$) × V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) Σ($f_o C_L$) = sum of outputs V_{DD} = supply voltage (V)
	10	4500 f_i + Σ($f_o C_L$) × V_{DD}^2	
	15	11 200 f_i + Σ($f_o C_L$) × V_{DD}^2	

DUAL MONOSTABLE MULTIVIBRATOR

The HEF4528B is a dual retriggerable-resettable monostable multivibrator. Each multivibrator has an active LOW input ($\overline{I}_0$), and active HIGH input (I_1), an active LOW clear direct input ($\overline{C}_D$), an output (O) and its complement ($\overline{O}$), and two pins for connecting the external timing components (C_{TC}, RC_{TC}).

An external timing capacitor (C_t) must be connected between C_{TC} and RC_{TC} and an external resistor (R_t) must be connected between RC_{TC} and V_{DD}. The duration of the output pulse is determined by the external timing components C_t and R_t.

A HIGH to LOW transition on $\overline{I}_0$ when I_1 is LOW or a LOW to HIGH transition on I_1 when $\overline{I}_0$ is HIGH produces a positive pulse (LOW-HIGH-LOW) on O and a negative pulse (HIGH-LOW-HIGH) on $\overline{O}$ if the $\overline{C}_D$ is HIGH. A LOW on $\overline{C}_D$ forces O LOW, $\overline{O}$ HIGH and inhibits any further pulses until $\overline{C}_D$ is HIGH.

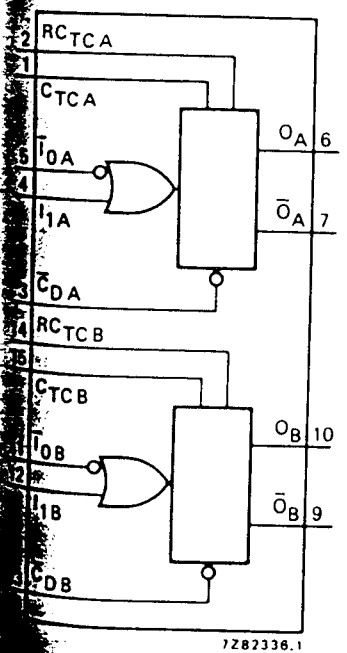


Fig. 1 Functional diagram.

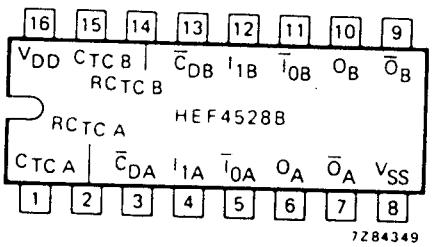


Fig. 2 Pinning diagram.

HEF4528BP : 16-lead DIL; plastic (SOT-38Z).
HEF4528BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4528BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

$\overline{I}_{0A}$, $\overline{I}_{0B}$	input (HIGH to LOW triggered)
I_{1A}, I_{1B}	input (LOW to HIGH triggered)
$\overline{C}_{DA}$, $\overline{C}_{DB}$	clear direct input (active LOW)
O_A, O_B	output
$\overline{O}_A$, $\overline{O}_B$	complementary output (active LOW)
$C_{TC\,A}$, $C_{TC\,B}$	external capacitor connections
$RC_{TC\,A}$, $RC_{TC\,B}$	external capacitor/ resistor connections

FUNCTION TABLE

inputs			outputs	
$\overline{T}_0$	I_1	C_D	O	$\overline{O}$
⎍	L	H	⎍	⎎
H	⎍	H	⎍	⎎
X	X	L	L	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
⎍ = positive-going transition
⎎ = negative-going transition
⎍⎎ = positive or negative output pulse; width is determined by C_t and R_t

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF, input transition times ≤ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
$\overline{T}_0$, I_1 → $\overline{O}$	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
$\overline{T}_0$, I_1 → O	5			155	305	ns	128 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	115	ns	49 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
$\overline{C}_D$ → O	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	85	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
$\overline{C}_D$ → $\overline{O}$	5			120	240	ns	93 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	105	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns; R_t = 5 kΩ; C_t = 15 pF

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	4000 f_i + Σ($f_o C_L$) × V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) Σ($f_o C_L$) = sum of outputs V_{DD} = supply voltage (V)
	10	20 000 f_i + Σ($f_o C_L$) × V_{DD}^2	
	15	59 000 f_i + Σ($f_o C_L$) × V_{DD}^2	

BCD TO 7-SEGMENT LATCH/DECODER/DRIVER

The HEF4543B is a BCD to 7-segment latch/decoder/driver for liquid crystal and LED displays. It has four address inputs (D_A to D_D), an active HIGH latch disable input (LD), an active HIGH blanking input (BI), an active HIGH phase input (PH) and seven buffered segment outputs (O_a to O_g).

The circuit provides the function of a 4-bit storage latch and an 8-4-2-1 BCD to 7-segment decoder/driver. It can invert the logic levels of the output combination. The phase (PH), blanking (BI) and latch disable (LD) inputs are used to reverse the function table phase, blank the display and store a BCD code, respectively.

For liquid crystal displays a square-wave is applied to PH and the electrical common back-plane of the display. The outputs of the device are directly connected to the segments of the liquid crystal.

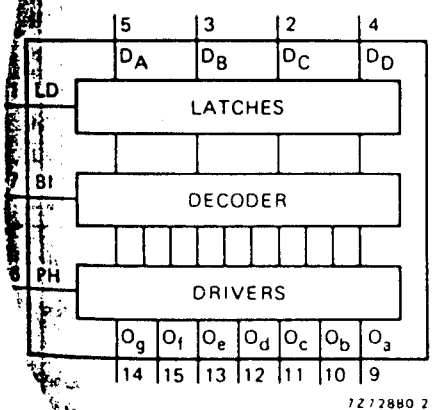


Fig. 1 Functional diagram.

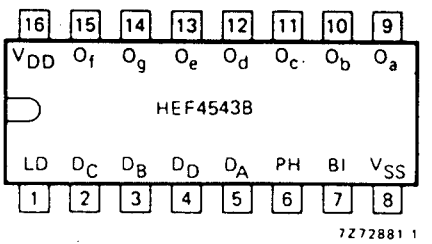


Fig. 2 Pinning diagram.

HEF4543BP : 16-lead-DIL; plastic (SOT-38Z).
HEF4543BD : 16-lead-DIL; ceramic (cerdip) (SOT-74).
HEF4543BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

D_A to D_D address (data) inputs
PH phase input (active HIGH)
BI blanking input (active HIGH)
LD latch disable input (active HIGH)
O_a to O_g segment outputs

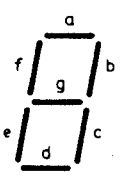


Fig. 3 Segment designation.

FUNCTION TABLE

inputs							outputs							
LD	BI	PH *	D_D	D_C	D_B	D_A	O_a	O_b	O_c	O_d	O_e	O_f	O_g	display
X	H	L	X	X	X	X	L	L	L	L	L	L	L	blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	blank
H	L	L	H	H	L	H	L	L	L	L	L	L	L	blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	blank
L	L	L	X	X	X	X				• •				• •
as above		H	as above				inverse of above							as above

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

* For liquid crystal displays, apply a square wave to PH.
For common cathode LED displays, select PH = LOW.
For common anode LED displays, select PH = HIGH.

• • Depends upon the BCD code previously applied when LD = HIGH.

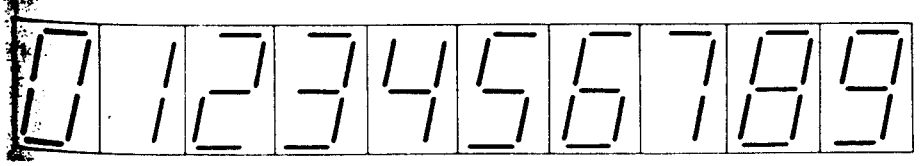


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Fig. 5 Display.

APPLICATION INFORMATION

Some examples of applications for the HEF4543B are:

- Driving LCD displays.
- Driving LED displays.
- Driving fluorescent displays
- Driving incandescent displays.
- Driving gas discharge displays.

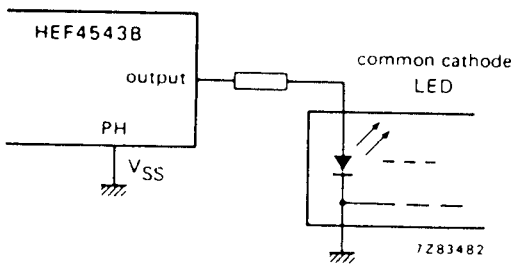

Fig. 6 Connection to common cathode LED display readout.

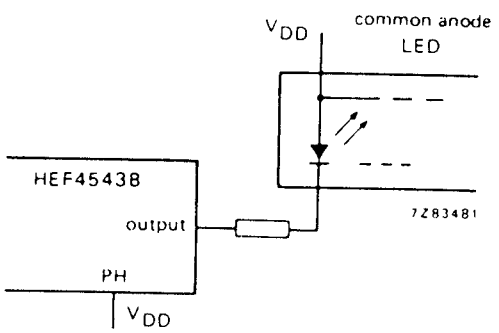

Fig. 7 Connection to common anode LED display readout.

Note to Figs 6 and 7: bipolar transistors may be added for gain where $V_{DD} \leqslant 10$ V or $I_{out} \geqslant 10$ mA.

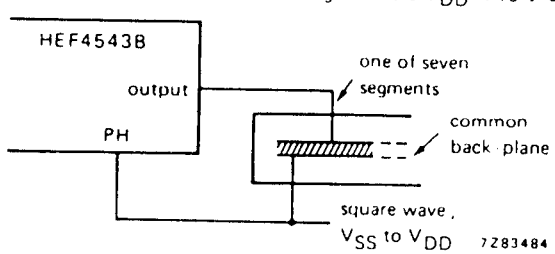

Fig. 8 Connection to liquid crystal (LCD) display readout.

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(AUTHORS)

SYNOPSIS

This project titled "Digital Phase Meter" primarily aims at measuring the phase difference between any two sinusoidal signals of same frequencies in the audio range, without going for different 'Connections or Strenuous calculations'.

The phase difference between two sinusoidal signals are of great importance in most branches of Electronic Engineering, but more particularly in Audio Engineering. In all circuits containing capacitors or inductors or both, frequency dependant phase shifts will occur and these will affect the operation of many a circuit. There are, of course, circuits such as filters, where phase shift is one of the design parameters.

We have, in this project, dealt in depth about the system, the various blocks' that has been associated with the system, their mode of working and their characteristics. We have explained the materials required in such a way that a layman can understand the utility of the project. We have also shown the clear block schematic structure of the system and also the circuit diagram related to each block separately. We feel that although we have tried to incorporate the latest trends available in the field of Electronics there is always scope for future development in this topic.

CHAPTER 10

CONCLUSION

The various building blocks of the Digital phase meter is rigged up on a bread board in stages. These stages were tested for its output signals. It gave satisfactory results. After testing the entire circuits, the printed circuit boards were designed and the various components were mounted on these boards.

The Digital phase meter was found to have a very good accuracy in the audio range. It was found to have an error rate of only 0.5 per cent. It indicated any phase difference between 0^{o} and 360^{o} accurately with a resolution of 1^{o}.

The main advantage of our project is to give directly the phase difference between two signals without going in for different connections or streneous calculations. However, at low signal frequencies, the measurement period is more. That is, however, the prize to be paid for accuracy at these frequencies.

This project can be further developed to have high speed at low frequencies, while maintaining the same degree of acuracy.