Microprocessor Based Electronic Telephone Directory

Project Report

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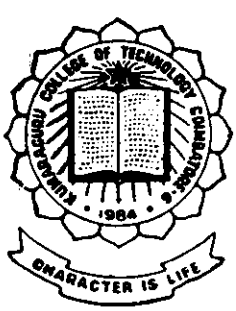
SUBMITTED IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE AWARD OF THE DEGREE OF BACHELOR OF ENGINEERING IN ELECTRONICS AND COMMUNICATION ENGINEERING OF THE BHARATHIAR UNIVERSITY



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

KUMARAGURU COLLEGE OF TECHNIOLOGY

COIMBATORE - 641 006

CERTIFICATE

Name ..... Roll No. .....

Register No. .....

This is to bonofide award of the project work titled MICRO **PROCESSOR BASED ELECTRONIC TELEPHONE DIRECTORY**

Done By

Mr. .....

In partial fulfilment of the requirements of the award of the Degree of Bachelor of Engineering in Electronics and Communication Engineering Branch of Bharathiar University Coimbatore, During the year 1992 - 1993.

Station : Coimbatore

Date : 2/4/93

....

Guide Head of the Department

Submitted for University Exam held on .....

....

Internal Examiner External Examiner

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We also thank one and all who helped us tc complete this project.

Date: 22.3.1993

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SYNOPSIS

This project has introduced the prototype electronic telephone directory to keep in touch with the advancement in technology.

This electronic telephone directory has got the facility to store the name and corresponding number of a particular person, company etc. The purpose of building this gadget is to make the process of storing and retrieving the number of a person easier. Directory is built around the 8085 Microprocessor because of facilities provided in this chip. The electronic memory is used for storing just as paper in book.

This project will be of use for person or company handling large amount of telephone numbers, which makes retrieval easier without any wear and tear or damage and saves valuable time.

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CHAPTER

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CHAPTER 1

INTRODUCTION

1.1 General Introduction

It is long since the telephone has been introduced into the society. From then on the numbers have been stored or written down on a piece of paper or a book.

The directory is a small book which is always prone to getting misplaced, lost or getting torn in due course of time.

The electronic telephones and exchanges have been introduced and to keep in pace with the development we have introduced electronic telephone directory. This makes things much easier to saves valuable time. The user does not have to refer to the number he wants to dial. With the push of a button, the required number is obtained.

The electronic telephone directory is built around the 8085 Microprocessor because the chip provides facilities suitable for this application.

1.2 Key Board

The Electronic telephone directory is provided with 30 keys, A.....Z, Read (Rd), Write (WR), load and digits (0.....9). The names and numbers are loaded in and read whenever needed by using these keys. Two multiplexers (74150) are used to multiplex 15 keys each to scan for key pressing.

1.3 Display

Eight seven segment displays (dynamic type) are used for displaying the number retrieved while reading. In order to drive the seven segment display, BCD to seven segment decoder (4511) is used. Decoder uses latch enable pin to store and blanking pin to turnoff the display. The display is achieved by the phenomenon of persistance of vision.

1.4 Computer Peripheral Connections

The input-output port is provided by 8155. 8155 has a static RAM, TIMER and three ports for input and output for interfacing keyboard & display.

Other peripheral connections are the EPROM 2732 with 4K memory and a 2K RAM 6116. The latch is provided by 74373 for latching the lower order address available on the multiplexed data bus.

1.5 Project functioning

Circuit is made to function by connecting the power supply. The program looks for load key to be pressed. Upon pressing this key, the scan code is send to the microprocessor and the program waits for alphabatical input. This is indicated by display of 'S'.

When the alphabet characters are keyed in two 'S' are displayed. Now the corresponding number of the person is keyed in. The end of numerical character input denotes a tripple 'S'. Now the load key has to be pressed in order to perform the next desired operation.

CHAPTER 2

8085 MICROPROCESSOR AND PERIPHERALS

2.1 Introduction

This chapter deals with the 8085 microprocessor and its peripheral connections. 8085 is an eight bit general purpose microprocessor capable of addressing 64K of memory.

The peripheral connections include memory chips.

EPROM 2732 is a 24 pin chip with 32K i.e. 4K x 3 bit memory. It is completely static and operates at 5 volts power supply.

RAM 6116: This is 2K RAM capable of working at high speeds. This RAM is a 2048 x 8 bit (CMOS). It needs 5 volts power supply.

Octal Latch 74373 is to provide latched address to RAM and EPROM.

8155 is a programmable I/O device which is used by the 8085 microprocessor to access key board and display. It acts as programmable I/O interface.

Multiplexer 74150 is a 16 line multiplexing unit. It is also supplied with 4 line scan input signal.

BCD to seven segment decder 4511: It is a 16 pin chip with 4 pin input for BCD. It converts the BCD signal into seven segment code for the display.

2.2 Microprocessor 8085

8085 microprocessor is an 8 bit general purpose microprocessor capable of addressing 64K of memory. The device has 40 pins, requires a +5V single power supply and a clock signal of 3.072 MHz. The clock is generated internally in the microprocessor by connecting a 6.144 MHz crystal at the pins X1, X2.

The signals are classified into 6 groups (Fig. 2.1)

1. Address bus
2. Data bus
3. Control and status signals
4. Power supply and frequency signals
5. Interrupts and peripheral initiated signals and
6. Serial I/O Ports.

The address bus comprises of 8 signal lines A_8 - A_{15} which are unidirectional, used as high order address bus.

The multiplexed address/data bus is also a set of 8 signal lines AD_0 - AD_7 which are bidirectional, they serve a

8085 - PIN CONNECTIONS

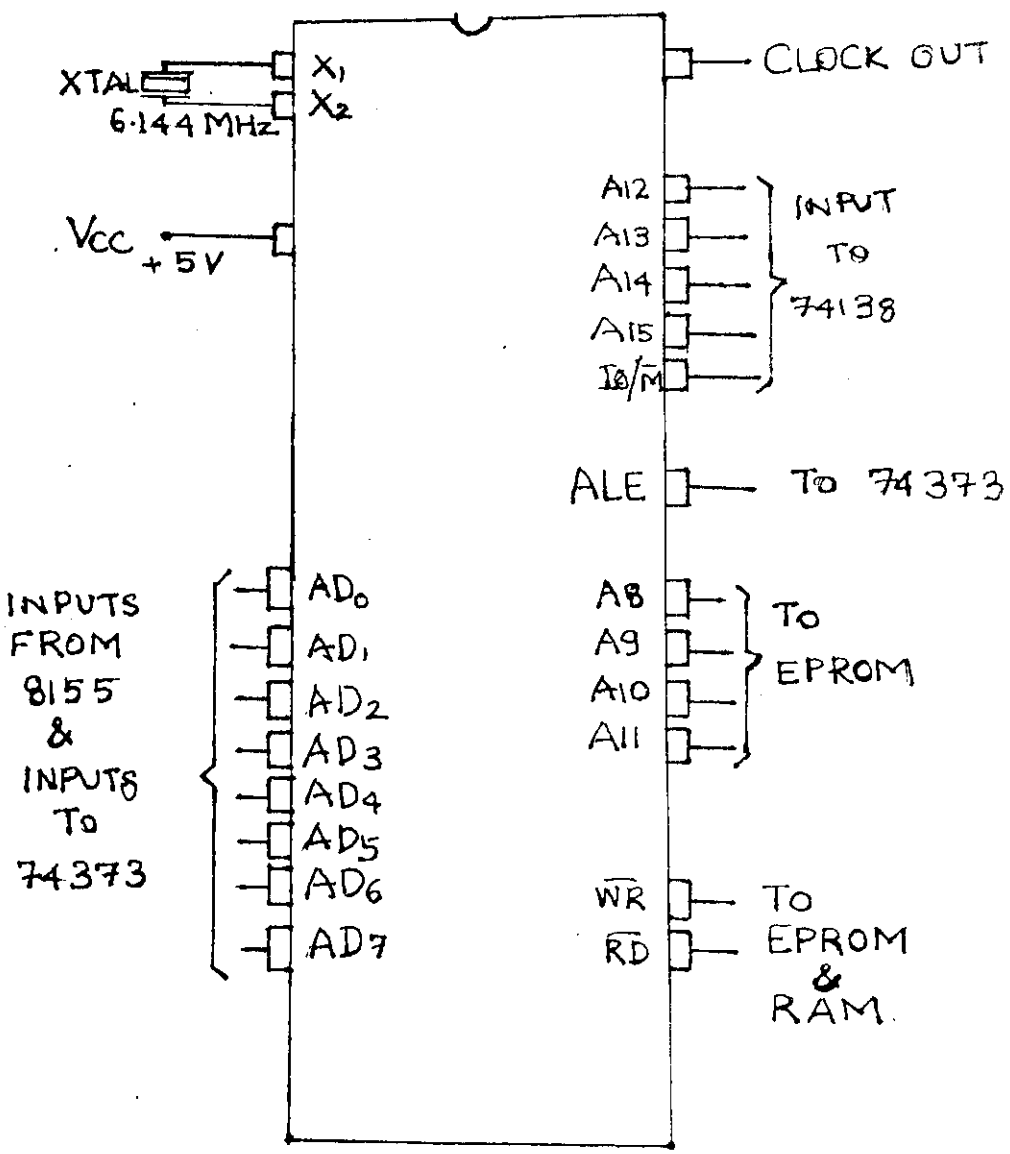


fig 2.1

dual purpose. They are used as the low-order address bus as well as the data bus. In an instruction execution, during the earlier part of the cycle, these lines are used as low-order address bus. During the later part of the cycle, these lines are used as the data bus. The process is known as multiplexing of the bus. They can be seperated using a latch.

The control and status signals include 2 control signals $\overline{RD}$ and $\overline{WR}$, 3 status signals IO/$\overline{M}$, S_1 and S_0 to identify the name of operation and one special signal ALE to latch the low order address bits.

Power supply and clock frequency:

Vcc	:	+ 5 Volts
Vss	:	Ground Reference
X1 & X2	:	A crystal (or RC, LC network) is connected between these 2 pins. The frequency is internally divided by 2. To operate the system at 3.072 MHz, the crystal should have 6.144 Mhz.
CLK (OUT)	:	Clock output. This can be used as a clock to clock other devices.

Interrupts and Externally initiated operation:

It has 5 interrupt signals.

INTR - Interrupt Request - Input

INTA - Interrupt Acknowledge - Output

Externally initiated:

HOLD - Input

READY - Input

RESET - Input

RESTART Interrupt Signals

RST 5.5]-

RST 6.5]- Inputs

RST 7.5]-

HLDA - Hold Acknowledge - Output

Serial I/o Ports:

For serial transmission implementation,

SID - Serial Input Data

SOD - Serial Output Data

2.3 Input-Output Port

8155 Programmable Input-Output device:

The circuit uses the 8155 programmable input-output device which is used between the 8085 microprocessor and the keyboard and display set up. The 8155 acts as the programmable interface between the microprocessor and the I/O section.

8155 is used between the 8085 microprocessor and the external devices. These external devices in this case are the keyboard and the 7 segment display unit. The interface is done with the help of the ports of 8155.

The 3 different sets of lines are classified as the ports of 8155. They are:

PORT A - PA_0 - PA_7 - I/O
PORT B - PB_0 - PB_7 - I/O
PORT C - PC_0 - PC_5 - I/O

Thus we see all the 3 ports can be used either as input or as output port. The control word determines, which port should be input and which one should be the output

8155 - PROGRAMMABLE I/O INTERFACE

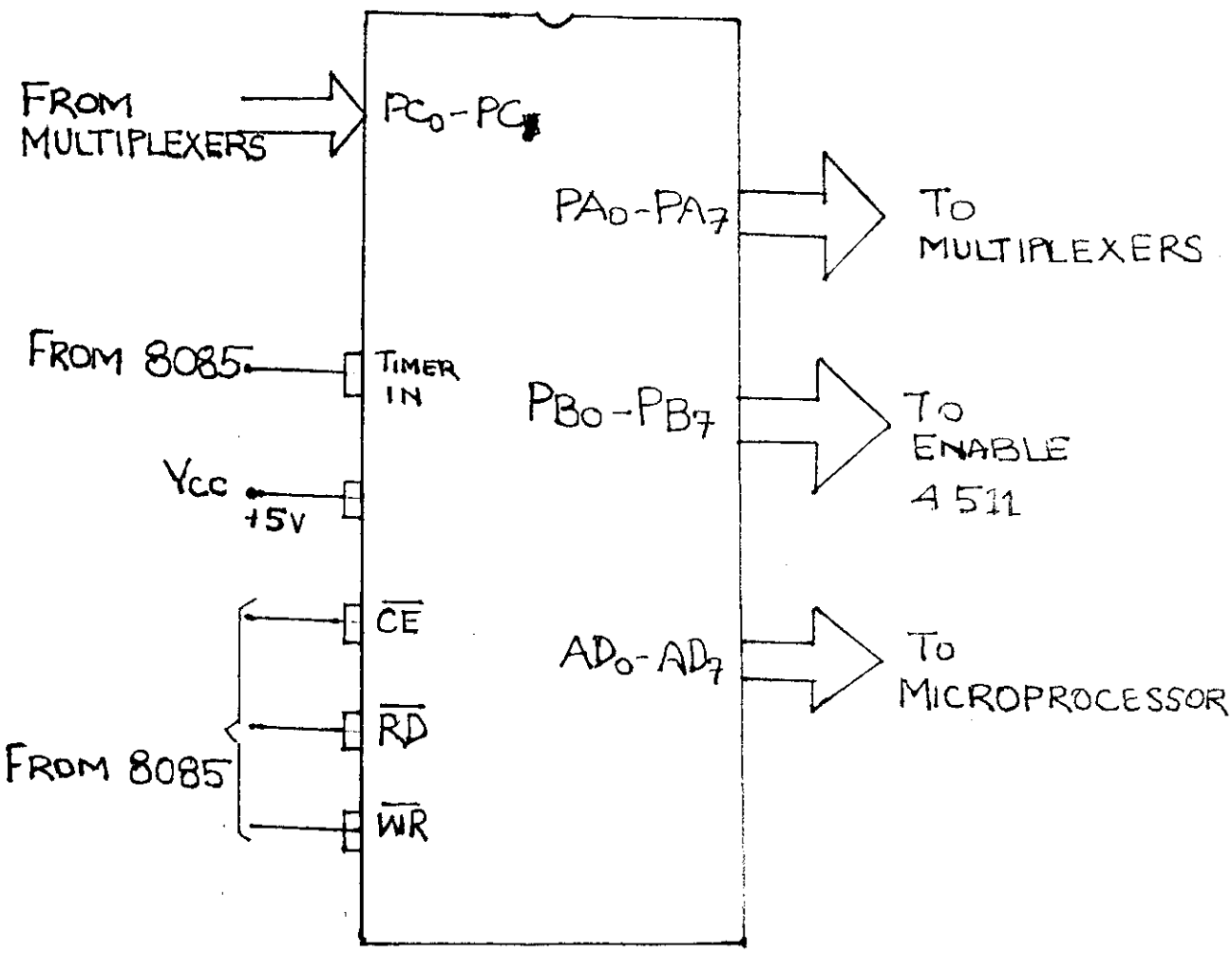


fig 2.2

port. After defining the control word, it is also possible for us to change the definition by just giving another control word.

The 8155 as shown in the figure 2.2 , has 40 pins. Among these 8 are Address/Data lines defined by AD_0 - AD_7. These lines take care of the key press scan line signals' defined by the software. These 8 lines are connected with the AD_0 - AD_7 lines of the microprocessor.

Here we have used the ports in the following manner.

Port A - O/P

Port B - O/P

Port C - I/P

The Port B used as the output port is used to enable the 7 segment display drivers (8 in number). The port A is used for the scan code delivery. The Port C is used to look for which of the key press code appears through the Z pin of the 74150 multiplexers. Since only 2 multiplexers are being used only PC_0 and PC_1 lines are used for this purpose.

The Port B output signals are accordingly set with respect to which of the 8 seven segment displays should be driven to display the particular digit. This being determined by the 4 bit 8241 code sent to the 4511 BCD - 7 segment driver.

2.4 Memory

The peripheral connections include two memory chips.

2.4.1 EPROM 2732 (Fig. 2.3)

This is a 24 pin, 32K i.e. (4K x 8 bit) Ultraviolet Erasable PROM. It is completely static, operating at +5V single power supply. It has simple programming requirements of

1. Single location programming
2. Programs with one 50 ms Pulse

In this circuit, to store the software this EPROM is being used. The fast access time capability of this EPROM is also of mentionable importance.

Upon switching ON the system, the EPROM chip is enabled and the execution of the stored software takes place.

Upon each and every step of execution, the EPROM is addressed to and it takes care of whatever is to be done according to the different parameters, say flags etc. Say when in the read operation, a non existing name is asked for, the software in EPROM takes care of blanking out the display.

2732- UV - ERASABLE EPROM

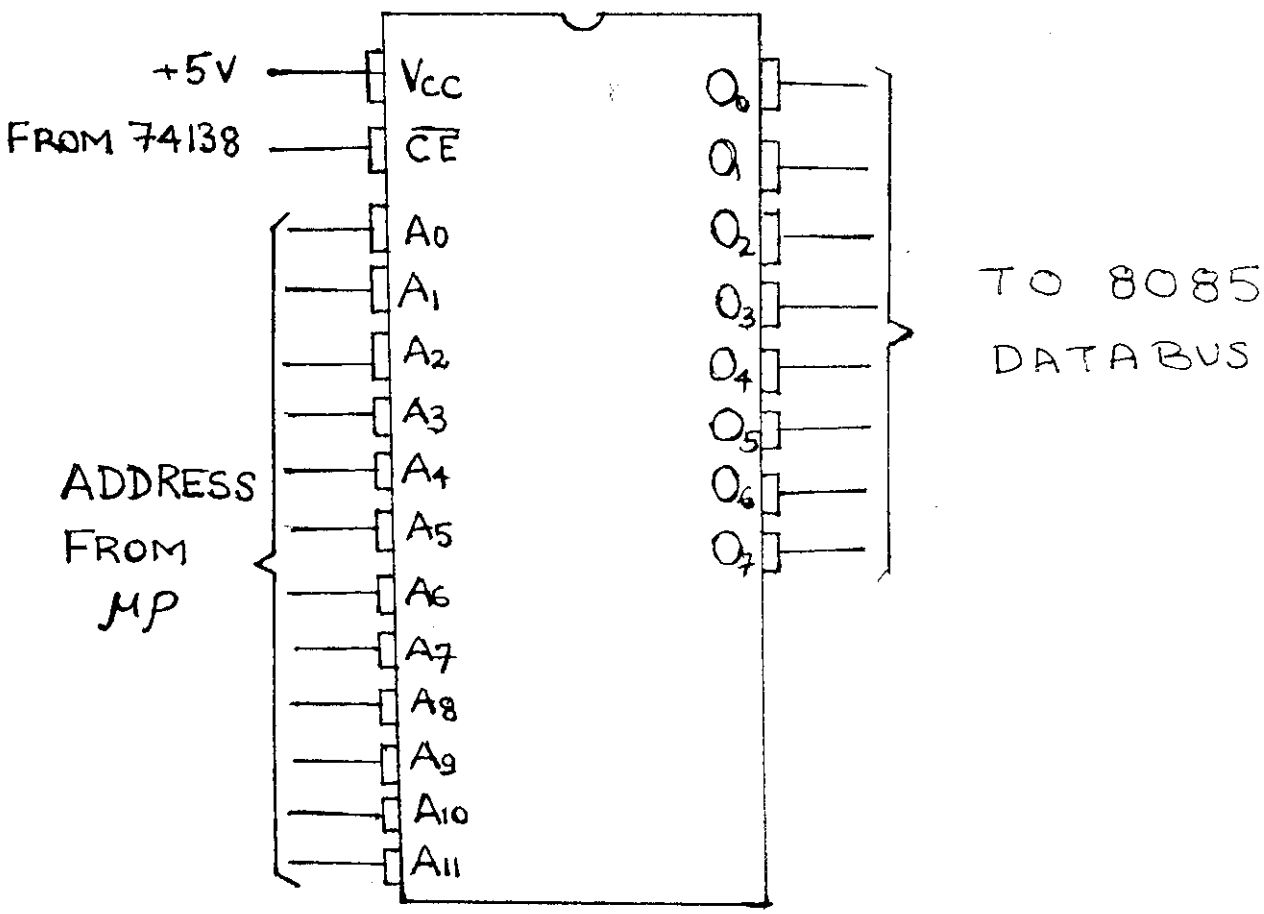


fig 2.3

2.4.2 The RAM 6116

This is a 2K RAM capable of working at high speeds. The fastest access time are 120 ns/150 ns/200 ns (Max.). 6116 RAM is a 2048 word x 8 bit CMOS RAM. The Vcc supply is of +5 V single power supply. (fig 2.4)

The output lines of the octal latch is connected to the A_0 - A_7 and the A_8, A_9, A_{10} of 8085 are connected to A_8 - A_{10} of 6116 RAM. Thus a 11 line address can accomodate a 2K address location. So according to the location being addressed, the RAM registers the data while a write operation and takes data and passes the data if present on to the data lines via the I/o lines.

The operation of this RAM is enabled by the CS (Chip Select) line. Given to this is a low signal, from the 1 of 8 decoder output.

6116 - 2K STATIC RAM

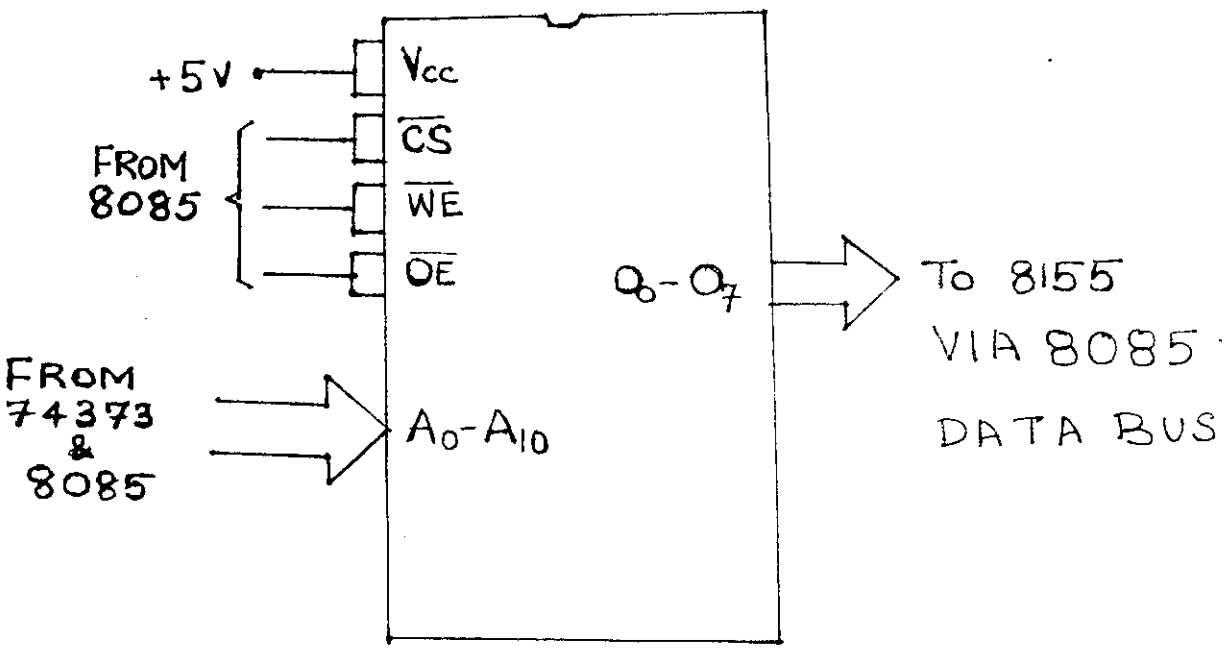


fig 2.4

Octal Latch: 74373

This chip is used to pass on the address to the RAM and EPROM. Whenever a key press is encountered the address lines AD_0 - AD_7 of Microprocessor are set with the particular address. On being a valid address, the microprocessor enables the latch enable signal ie output enable ($\overline{OE}$) an active low (fig 2.5).

When this is activated, the input and the output lines are connected virtually and the address on the lines I_0 - I_7 are transferred on to O_0 - O_7 of the latch. After this, the enable signal is taken off ie., $\overline{OE}$ is made 1. Thus any other address won't be transferred until the next enable signal is given by the microprocessor.

This transferred address is made available at the A_0 - A_7 of the RAM 6116.

Internally these latches have D flip-flops.

74373 - OCTAL LATCH

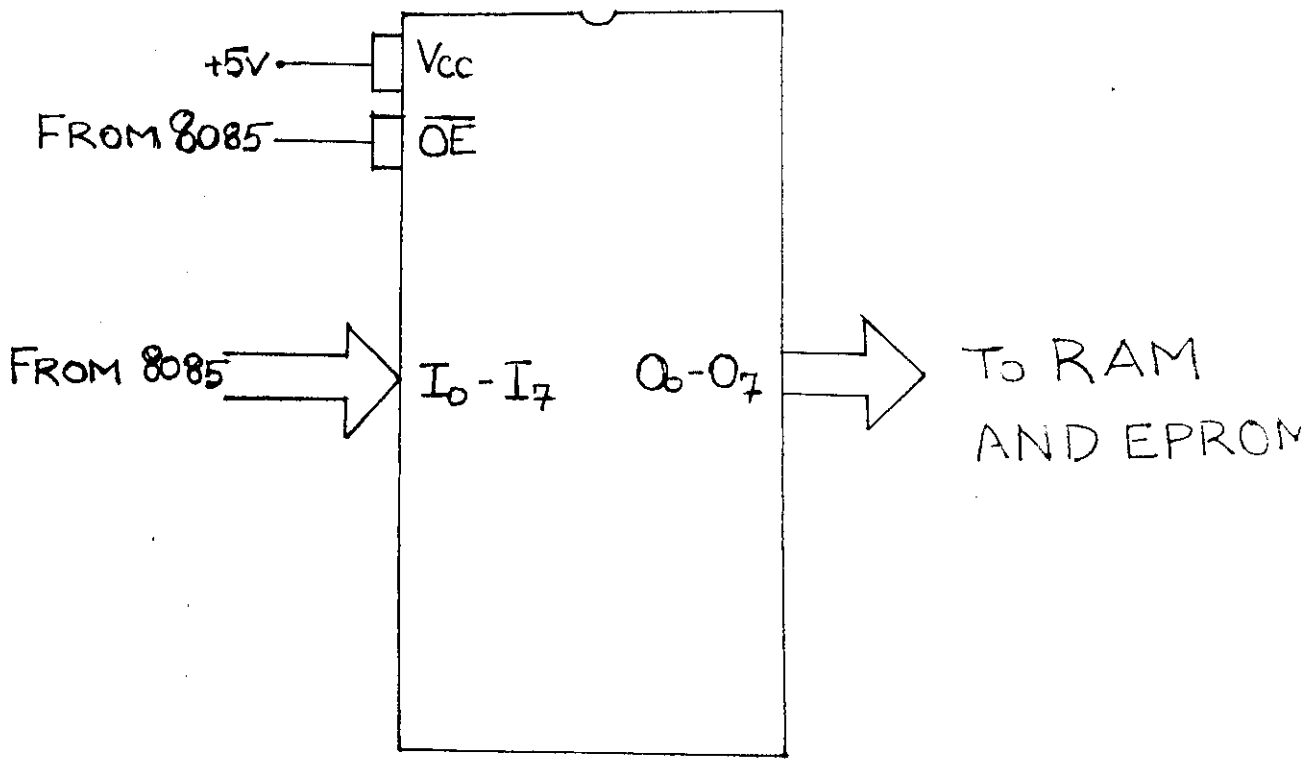


fig 2.5

2.4.3. 74138 - 1 of 8 Decoder

This is used to generate chip enable signals to the EPROM, RAM etc. According to the inputs provided to this, we have either a high or a low at the pins O_0 to O_7. The inputs are at pins A_0, A_1 & A_2 and to E_1 and E_2 (fig 2.6).

Chip enable signals given are O_0 to 2732 and O_1 to 6116.

This chip enable of 8155 is also a low signal. The A_{15} line of microprocessor 8085 is 'NOT' - ed and given to $\overline{CS}$ of 8155 (2.6.2)

74138 - 1-OF-8 DECODER.

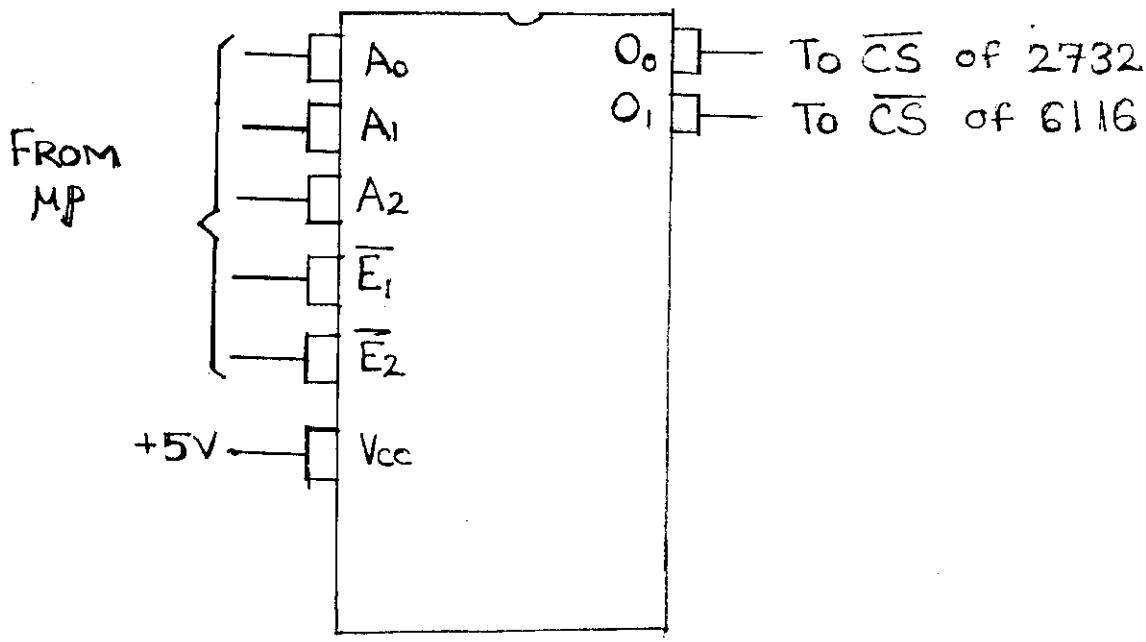


fig 2.6.1

7404 - HEX INVERTER

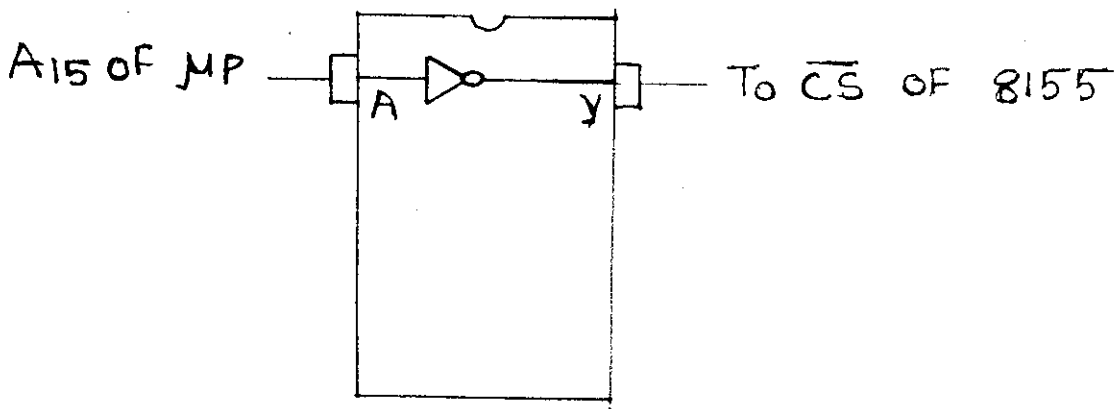


fig 2.6.2

2.5 Input section

The keyboard section comprises of 30 different keys and the multiplexer unit. The keys are "press to ON" type. The multiplexer unit has two 74150 chips.

2.5.1 Multiplexer

These 74150 multiplexer are sixteen line multiplexing units. So a maximum of 16 keys can be connected to a single multiplexer. The actual circuit uses only 28 keys. To the first multiplexer are connected a set of 16 keys. The rest 12 are connected to the second multiplexer (fig 2.7)

The multiplexer also is supplied with a 4 line, scan input signal. It ranges from 0000 to 1111. These are connected to lines S_0 - S_3. These are connected to lines S_0 - S_3 of each multiplexer. Thus a total of 8 line scanning is given by the 8155 through its Port A of which PA_0 - PA_3 are connected to Multiplexer-1 and PA_4 - PA_7 to the multiplexer - 2.

The scanning code actually follows the sequence. When a scan signal scans the first multiplexer, the other multiplexer's scan signal is kept constant. That is:

74150 - MULTIPLEXER

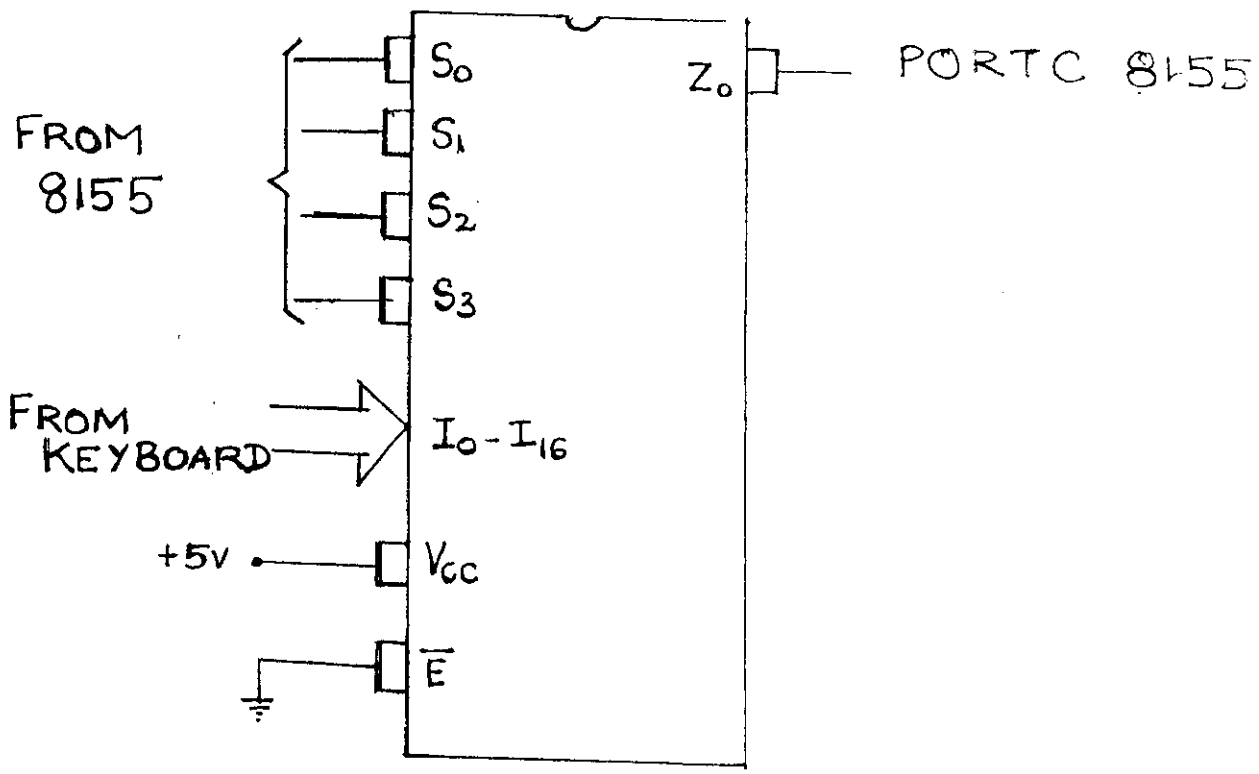


fig 2.7

Initially the lines PA_0 - PA_3 are made 1111 and the other 4 lines are PA_4 - PA_7 are continuously varied from 0000 to 1100. This scans the rest of the keys (12) connected to the 2nd multiplexer. The above procedure is repeated until a key press is met with.

2.6 4511 BCD to seven segment decoder

The chip 4511 has 4 pin input for BCD which is fed to pins 7,1,2 and 6. The chip converts the BCD and makes the corresponding display segments glow. It functions like 4 bit storage latch, a 8421 BCD to seven segment decoder, and an output drive with capability to source upto 25 mA. Latch enable pin of 4511 stores BCD code and blanking turns of the display(fig 2.8).

Its application includes counter, display drivers, seven segment decimal display and various clock, watch and timer users.

4511 - BCD To 7 SEGMENT

LATCH/DECODER/DRIVER

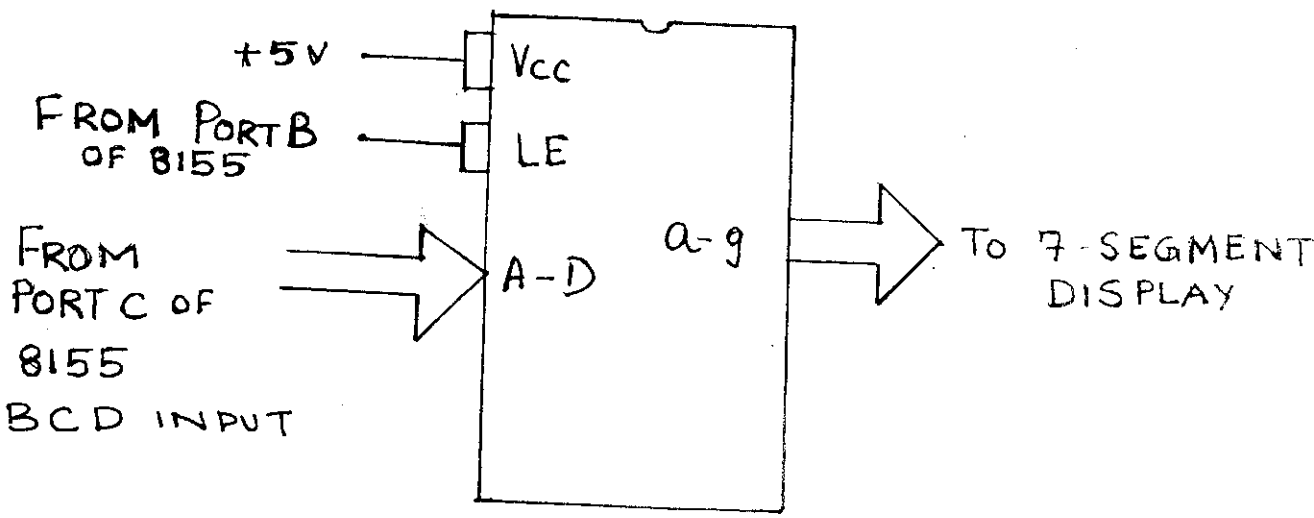


fig 2.8

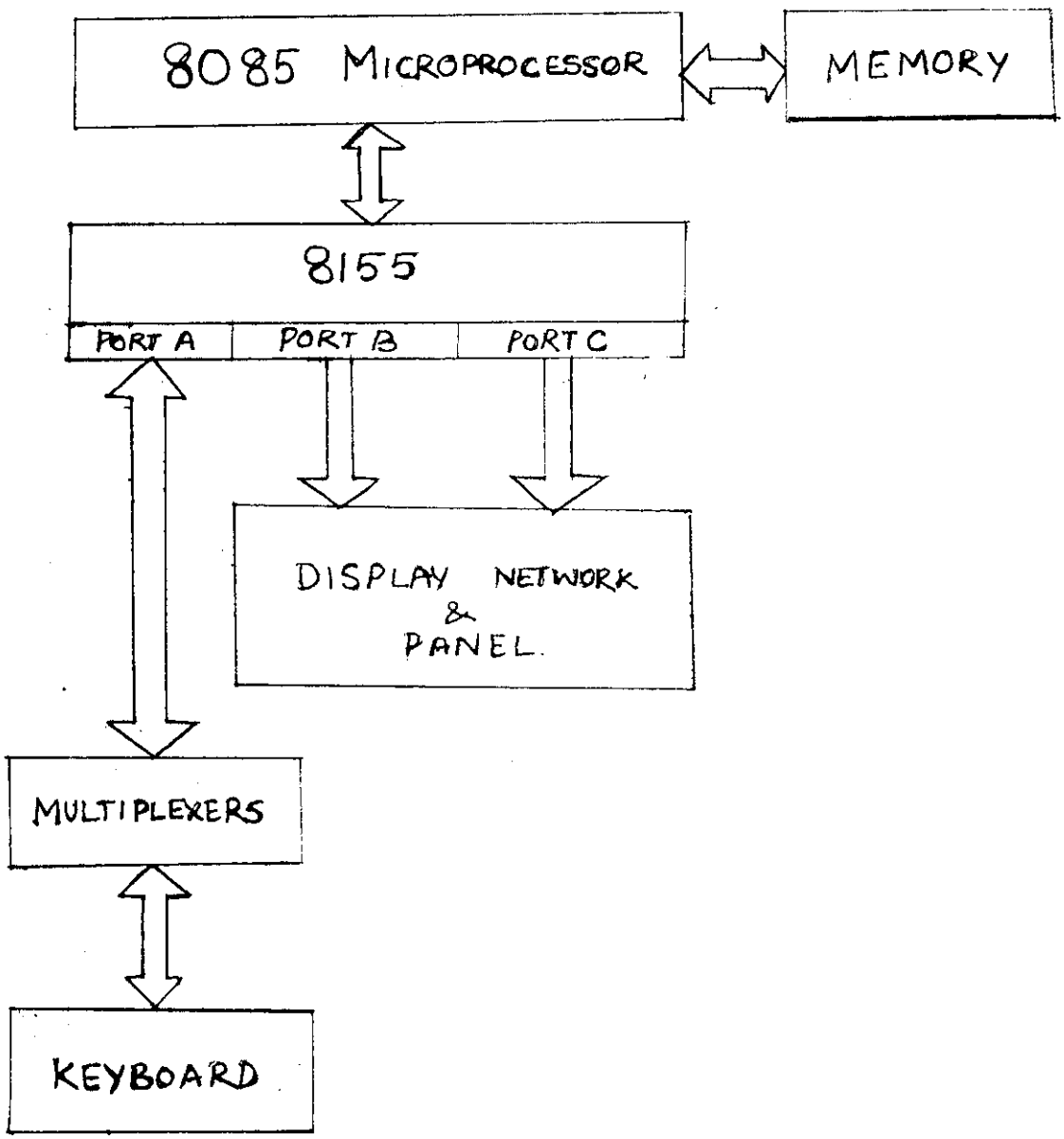
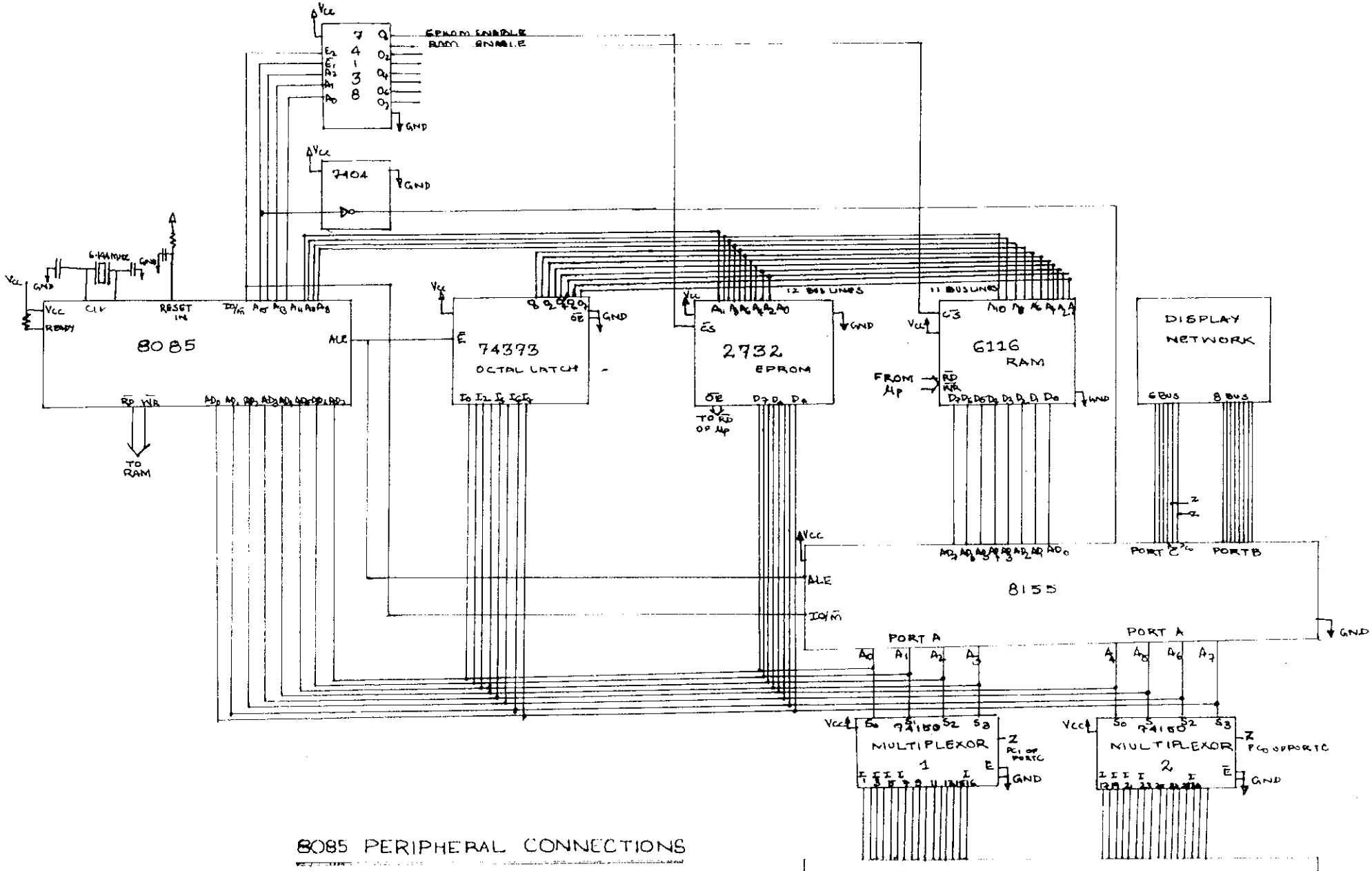
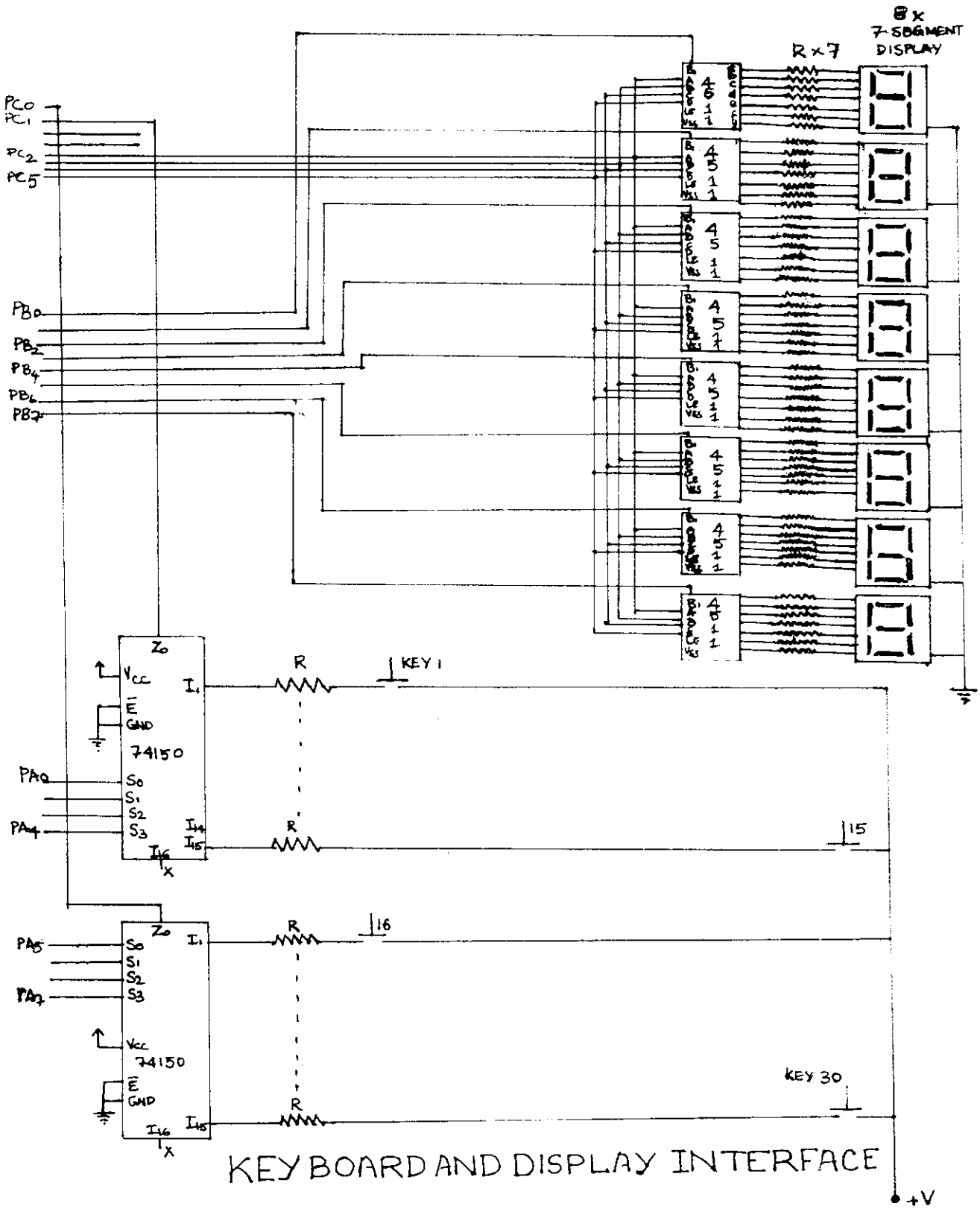


fig 3. BLOCK DIAGRAM



8085 PERIPHERAL CONNECTIONS

KEY BOARD



KEY BOARD AND DISPLAY INTERFACE

CHAPTER 3

GENERAL CIRCUIT DESCRIPTION

3.3.1 Keyboard Description

In the circuit of this project we have a key board which contains thirty keys. These keys are connected to two multiplexers (74150). Each multiplexer is connected to 16 switches. The output of the multiplexer are connected to the Port A low of 8155 which acts as an input to the microprocessor.

The Port A of 8155 is connected to the select lines of the multiplexers the lines PA_0 - PA_3 is connected to one multiplexer and the lines PA_4 - PA_7 is connected to next multiplexer.

Now the data from the key board is taken as follows: The lines PA_0 - PA_3 are made 1111 and the next four lines PA_4 - PA_7 are varied continuously from 0000 to 111C. These act as the address of the first fifteen keys. The address of the next fifteen keys is taken by interchanging the process. That is first four lines are varied continuously from 0000

to 1110 and the next four lines are kept constantly at 1111. This process is repeated continuously with the help of a software programme. The output of the multiplexer which are connected to the Port C low of 8155 is checked. If the output (i.e. PC_0 and PC_1) is not zero that means the key corresponding to the address which is correctly on port A is not pressed. If it is zero that means it is pressed.

If the process of changing the addresses of both multiplexers is finished and no key is pressed the process of address generation is repeated continuously till any of the thirty keys is pressed.

If in between the cycle of address generation any key is pressed the cycle terminated and it stores the address of the key as its corresponding code.

3.3.2 Display Description :

The display of the telephone number is done by the seven segment display. This display is a dynamic type of display. The data available on the lines of Port C PC_4 - PC_7. This data is given on the input lines of all the 4511 decoder drivers at a time parallely.

The display is done as follows: The addressing of the decoders is controlled by the eight lines of Port B of 8155. At a particular given time only on 4511 chip is enabled which gives the data on the seven segment display. Now this chip is disabled and the data is changed and the next 4511 is enabled sequentially. This procedure is repeated using the Port B output.

The process is repeated so fast that due to human persistance of vision. The display on the seven segment displays looks as if it is constantly glowing. This process is repeated till the key load is pressed.

CHAPTER 4

PROJECT FUNCTIONING

The circuit begins to function with the connection of power supply. The circuit scans the key board which makes all operations stand still. If the system is to be used the load key is pressed. The software initially looks for this key press, until this key is pressed system shows no response if other keys are pressed. When load key is pressed a 0 is displayed expecting a name entry. The load key press sends corresponding scan code to the microprocessor for eg. keys from 0 to 15 will have varying scan code starting from

0000	0000
0000	0001
	: :
0000	1111

Always the circuit will be scanning these codes. From 16th key to 30th key will have code like given below:

0001	1111
0010	1111
: :	: :
: :	: :
1111	1111

When the load key is pressed the corresponding code of the key is passed on to the microprocessor through peripheral connections.

After this the scan code of this key is send to the microprocessor and the program waits for the alphabetical input. This is indicated by the display of a single 'S'.

If the alphabets (names) are fed in, one by one the character count is shown on the display, while the characters are being stored temporarily. Once when this feeding is over, it displays a double 'S', indicating end of name feed.

Now it waits for either a write or read key press. If it is write key, the number feed is expected one by one the number is fed in simultaneously, the number of numerical input being counted. Once that is completed, the name & number are passed on the input bus of RAM and are stored. This is indicated by a triple 'S'.

When the write key is pressed, inside the circuit the WR line is enabled and location is addressed to microprocessor In the display when name is given the character inputs are counted. In present condition four alphabets can be fed in. These alphabets may be a short form of a person's name. After the fourth alphabet is keyed in two 'S' are displayed which indicates the alphabet entry is completed. Once the corresponding number of the person is keyed in triple 'S' is displayed indicuting the end of numerical character input.

With the end of numerical character key input the name and number from static memory of 8085 is passed onto the 6116 (RAM) bit by bit serially and thus is written in the RAM.

During a write operation the number is written to that location where it is addressed to. When the number is being given a one is displayed showing numeric input. In case if bit by bit matching is found during write operation, it over write the data previously stored.

During read key press, the $\overline{RD}$ line is enabled and program commands the microprocessor to pass on the address to the checking sequence. When the bit by bit matching meets with a 100% match then the program makes the transfer of the number from that location on to microprocessor. This data is then passed on to 8155 to be displayed on the display network. If a match is not obtained the circuit blanks of the display.

After all these operations the circuit expects the press of the load key. Now the circuit is ready for read or write operation. If another number is to be fed into the circuit above procedures are repeated. If the user is interested in finding out a number of a person the read routine is performed.

CHAPTER 5

CONCLUSION

Electronic Telephone Directory is a handy device which can be operated easily. This proto type can store about 200 numbers. The memory capacity can be increased, if desired. There are many limitations to the project. While writing or reading, the name will not be displayed, only the number of characters in the name is displayed. The solutions to this limitations is the use of 14 segment display.

No battery back up is given which makes data erased when power supply is switched off.

Overcoming these limitations will make this project a grand success.

```
0000 310081          MAIN:  LXI SP, 8100H
0003 AF                     XRA A
0004 320980                   STA 8009H
                    ;
0007 CD4100        BEGIN:  CALL BLKDISPTBL
000A CD5A01                CALL DISPLAY
000D 3E05                       MVI A, 05H
000F 320080                     STA 8000H
0012 CD5A01                     CALL DISPLAY
0015 CD4F00                     CALL SCANSTART
0018 3E05                     MVI A, 05H
001A 320180                     STA 8001H
001D CD5A01                     CALL DISPLAY
0020 CD6A00                     CALL SCANAME
0023 3E05                       MVI A, 05H
0025 320280                     STA 8002H
0028 CD5A01                     CALL DISPLAY
002B CDDB00                     CALL SCANRW
002E 3A0880                     LDA 8008H
0031 FEB0                       CPI 0B0H
0033 CC0601                     CZ READ
0036 3A0880                   LDA 8008H
0039 FEC0                       CPI 0C0H
003B CC9B01                     CZ WRITE
003E C30700                     JMP BEGIN
                    ;
0041 210080     BLKDISPTBL:  LXI H, 8000H
0044 3E0A                    MVI A, 0AH
0046 0608                         MVI B, 08H
0048 77               XXX1:  MOV M,A
0049 23                      INX H
004A 05                           DCR B
004B C24800                       JNZ XXX1
004E C9                           RET
                    ;
004F 3E03         SCANSTART:  MVI A, 03H
0051 D380                     OUT 80H
0053 3EE0             XXX2:  MVI A, 0E0H

0055 D382                        OUT 82H
0057 DB83                        IN 83H
0059 E620                     ANI 00100000B
005B CA5300                   JZ XXX2
005E 3EE0                   LOOP:  MVI A, 0E0H
0060 D382                        OUT 82H
0062 DB83                        IN 83H
0064 E620                     ANI 00100000B
0066 C25E00                       JNZ LOOP
0069 C9                           RET
                    ;
006A F5              SCANAME:  PUSH PSW
006B C5                      PUSH B
006C D5                           PUSH D
006D E5                           PUSH H
006E 0E04                         MVI C, 04H
0070 1600                         MVI D, 00H
0072 1E11             XXX5:  MVI E, 11H
0074 0610                    MVI B, 10H
0076 211080                     LXI H, 8010H
0079 3E03                  XXX3:  MVI A, 03H
007B D380                         OUT 80H
```

```
007D 05                DCR B
007E 1D                DCR E
007F CA8F00            JZ XXX4
0082 78                MOV A,B
0083 D382              OUT 82H
0085 DB83              IN 83H
0087 E610              ANI 00010000B
0089 CA7900            JZ XXZ
008C C37800            JMP LOOP1
008F 1E05      XXX4:   MVI E, 05H
0091 060A              MVI B, 0AH
0093 05        XXY:    DCR B
0094 1D                DCR E
0095 CA?200            JZ XXX2
0098 78                MOV A,B
0099 87                ADD A
009A 87                ADD A
009B 80                ADD B
009C 87                ADD A
009D D382              OUT 82H
009F DB83              IN 83H
00A1 E620              ANI 00100000B
00A3 CA?300            [illegible]
00A6 78        LOOP3:  MOV A,B
00A7 87                ADD A
00A8 87                ADD A
00A9 80                ADD B
00AA 87                ADD A
00AB 47                MOV B,A
00AC D382              OUT 82H
00AE DB83              IN 83H
00B0 E620              ANI 00100000B
00B2 C2A600            JNZ LOOP3
00B5 C3C100            JMP XXY
00B8 78        LOOP2:  MOV A,B
00B9 D382              OUT 82H
00BB DB83              IN 83H
00BD E610              ANI 00010000B
00BF C2B800            JNZ LOOP2
00C2 7D        XX2:    MOV A,L
00C3 91                SUB C
00C4 6F                MOV L,A
00C5 78                MOV A.B
00C6 77                MOV M,A
00C7 14                INR D
00C8 7A                MOV A,D
00C9 320780            STA 8007H
00CC CD5A01            CALL DISPLAY
00CF CD5502            CALL DELAY
00D2 0D                DCR C
00D3 C27200            JNZ XX5
00D6 E1                POP H
00D7 D1                POP D
00D8 C1                POP B
00D9 F1                POP PSW
00DA C9                RET

00DB 3E03      SCANKW: MVI A, 03H
00DD D380              OUT 80H
00DF 3EB0      XXX6:   MVI A, 0B0H
00E1 47                MOV B,A
00E2 D382              OUT 82H
00E4 DB83              IN 83H
00E6 E620              ANI 00100000B
00E8 C2F700            JNZ LOOP4
00EB 3EC0              MVI A, 0C0H
00ED 47                MOV B,A
00EE D382              OUT 82H
00F0 DB83              IN 83H
00F2 E620              ANI 00100000B
00F4 CADF00            JZ XXX6
00F7 78        LOOP4:  MOV A,B
```

```
00F8 D382                                   OUT 82H
00FA DB83                                   IN 83H
00FC E620                                   ANI 00100000B
00FE CAF700                                 JZ LOOP
0101 78                                     MOV A,B
0102 320880                                 STA 8008H
0105 C9                                     RET
               ;
0106 CD4100            [illegible]:   CALL DISPTH
0109 3E00                             MVI A, 00H
010B 320080                           STA 8000H
010E CD5A01                                 CALL DISPLAY
0111 3A0980                           LDA 8009H
0114 4F                               MOV C,A
0115 FE00                                   CPI 00H
0117 CA8A01                                 JZ ERROR1
011A 210040                                 LXI H, 4000H
011D 79                XXX:   MOV A,C
011E 320680                           STA 8006H
0121 CD5A01                                 CALL DISPLAY
0124 110C80                           LXI D, 800CH
0127 0604                             MVI B, 04H
0129 EB                YYY:   XCHG
012A 7E                               MOV A,M
012B EB                                     XCHG
012C BE                                     CMP M
012D C23901                                 JNZ NEXT
0130 23                                     INX H
0131 13                                     INX D
0132 05                                     DCR B
0133 CA4B01                                 JZ PREDISPLAY
0136 C22901                                 JNZ YYY
0139 0D                NEXT:  DCR C
013A CA8A01                           JZ ERROR1
013D 110800                                 LXI D, 0008H
0140 19                                     DAD D
0141 7D                                     MOV A,L
0142 80                                     ADD B
0143 6F                                     MOV L,A
0144 7C                                     MOV A,H
0145 CE00                                   ACI 00H
0147 67                                     MOV H,A
0148 C31D01                                 JMP XXX
               ;
014B 0608        PREDISPLAY:  MVI B, 08H
014D 111780                       LXI D, 8017H
0150 7E                    YYY3:            MOV A,M
0151 EB                                     XCHG
0152 77                                     MOV M,A
0153 EB                                     XCHG
0154 1B                                     DCX D
0155 23                                     INX H
0156 05                                     DCR B
0157 C25001                                 JNZ YYY3
015A F5                  DISPLAY:     PUSH PSW
015B C5                               PUSH B
015C D5                                     PUSH D
015D E5                                     PUSH H
015E 3E0F                             MVI A, 0FH
0160 D380                             OUT 80H
0162 117F00                       LXI D, 007FH
0165 210080            [illegible]:   LXI H, 8000H
0168 1B                               DCX D
0169 7B                                     MOV A,E
016A B2                                     ORA D
016B CA8501                                 JZ YYYY
016E 0E09                                   MVI C, 09H
0170 0601                                   MVI B, 01H
0172 7E                    XXX9:      MOV A,M
0173 D383                             OUT 83H
0175 78                               MOV A,B
0176 D381                             OUT 81H
0178 87                                     ADD A
```

```
0179 47                            MOV [illegible]
017A 0D                          DCR [illegible]
017B CA6501                         JZ XXX[illegible]
017E 23                             [illegible]
017F CD5502                 CALL [illegible]
0182 C37201                        JMP XXX[illegible]
0185 E1              [illegible]Y:   POP H
0[illegible] D1                          [illegible]
01[illegible] C1                             [illegible]
[illegible]8 [illegible]                             POP PSW
[illegible]9 C9                             RET
[illegible]8A 0608           [illegible]DR1:   MVI B, [illegible]H
[illegible]8C 210080                       LXI H, 80[illegible]0H
018F 3E00                           MVI A, [illegible]H
[illegible]91 77                 XXX:  MOV M,A
[illegible]92 23                       INX H
[illegible]93 05                            DCR B
[illegible]94 C29101                        JNZ XXX
[illegible]97 CD5A01                      CALL DISPL[illegible]
[illegible]9A C9                            RET

[illegible]9B CD4100    WR[illegible]:   CALL [illegible]DISPTE[illegible]
019E 3E01                          MVI A, 01H
01A0 320080                        STA 800[illegible]H
01A3 CD5A01                          CALL DISPL[illegible]
01A6 CDE301                        CALL SCANUM
01A9 3A0980              LDA 8[illegible]
01AC 4F                              MOV C,A
01AD FE00                CPI 00H
01AF CA2302                          JZ FIRST
01B2 210040                          LXI H, 400[illegible]
01B5 110C80             [illegible]:   LXI D, 800CH
01B8 0604                          MVI B, 04H
01BA EB                 XXXC:   XCHG
01BB 7E                            MOV A,M
01BC EB                              XCHG
01BD BE                              CMP M
01BE C2CA01                          JNZ NEXT1
01C1 23                              INX H
01C2 13                              INX D
01C3 05                              DCR B
01C4 CA3D02                          JZ STORE
01C7 C3BA01                          JMP XXXC
01CA 0D                  NEXT1:   DCR C
01CB CA2C02                       JZ STORE1
01CE 79                              MOV A,C
01CF 320680                          STA 8006H
01D2 CD5[illegible]01              CALL DISPLAY
01D5 110800                          LXI D, 0008H
01D8 19                              DAD D
01D9 7D                              MOV A,L
01DA 80                              ADD B
01DB 6F                              MOV L,A
01DC 7C                              MOV A,H
01DD CE00                            ACI 00H
01DF 67                              MOV H,A
01E0 C3B501                          JMP XXXD
                     ;
01E3 F5              SCANUM:   PUSH PSW
01E4 C5                             PUSH B
01E5 D5                             PUSH D
01E6 E5                                PUSH H
01E7 211080                          LXI H, 8010H
01EA 0E08                            MVI C, 08H

01EC 110780                           LXI D, 8007H
01EF CD5A01               SCAN1:   [illegible] DISPLAY
01F2 3E03                   MVI A, 03H
01F4 D380                               OUT 80H
01F6 060A                 SCAN2:  MVI B, 0AH
01F8 78                    SCAN:  MOV A,B
01F9 FE00                         CPI 00H
```

```
[illegible]                          [illegible]
01FE 06                              OUT [illegible]
01FF 78                              MOV A,B
0200 D382                            OUT 82H
0202 DB83                            IN 83H
0204 E610                            ANI 00010000B
0206 CAF801                          JZ [illegible]
0209 78                   LOOP?:     MOV A,B
020A D382                            OUT 82H
020C DB83                            IN 83H
020E E610                            ANI 00010000B
0210 C20902                          JNZ LOOP?
                                     CALL DELAY

0213 7E                              MOV A,M
0214 77                              MOV [illegible]
0215 EB                              XCHG
0216 [illegible]                     MOV M,A
0217 EB                              XCHG
0218 23                              INX H
0219 1B                              DCX D
021A 0D                              DCR C
021B C2EF01                          JNZ SCAN1
021E E1                   [illegible]
021F D1                              POP D
0220 C1                              POP B
0221 F1                              POP PSW
0222 C9                              RET

0223 CD4100               FIRST:     CALL BLKDISPTBL
0226 210440                          LXI H, 4004H
0229 C33002                          JMP STORE2
022C 011000               STORE1:    LXI B, 0010H
022F 09                              DAD B
0230 3A0980               STORE2:    LDA 8009H
0233 320680                          STA 8006H
0236 CD5A01                          CALL DISPLAY
0239 3C                              INR A
023A 320980                          STA 8009H
023D 7D                   STORE:     MOV A,L
023E D604                            SUI 04H
0240 6F                              MOV L,A
0241 7C                              MOV A,H
0242 DE00                            SBI 00H
0244 67                              MOV H,A
0245 060C                            MVI B, 0CH
0247 110C80                          LXI D, 800CH
024A EB                   STORE3:    XCHG
024B 7E                              MOV A,M
024C EB                              XCHG
024D 77                              MOV M,A
024E 23                              INX H
024F 13                              INX D
0250 05                              DCR B
0251 C24A02                          JNZ STORE3
0254 C9                              RET

0255 F5                   DELAY:     PUSH PSW
0256 C5                              PUSH B
0257 D5                              PUSH D
0258 E5                              PUSH H
0259 21FF00                          LXI H, 00FFH
025C 2B                   XXYY:      DCX H
025D 7C                              MOV A,H
025E B5                              ORA L
025F C25C02                          JNZ XXYY
0262 E1                              POP H
0263 D1                              POP D
0264 C1                              POP B
0265 F1                              POP PSW
0266 C9                              RET

                                     END
```

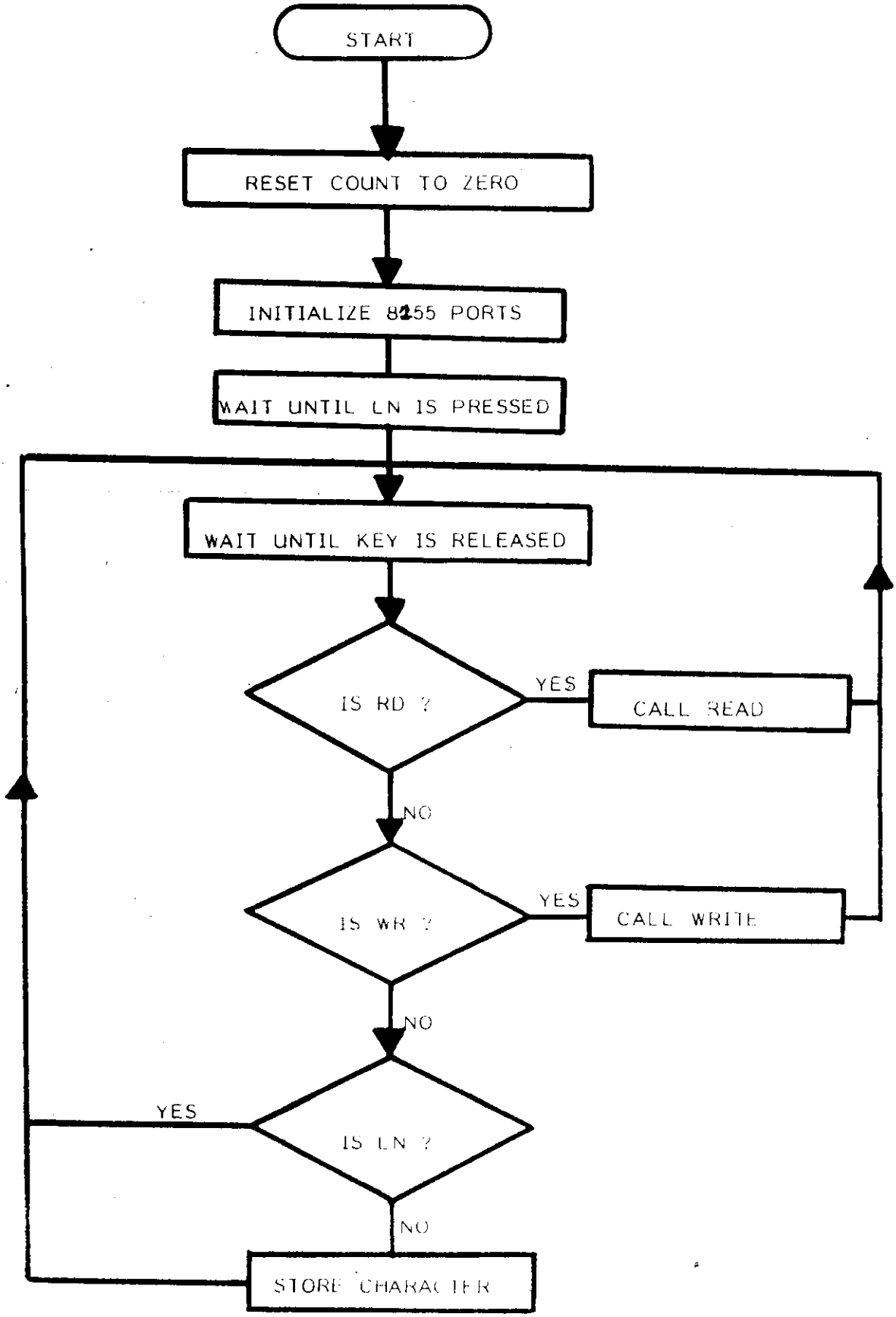
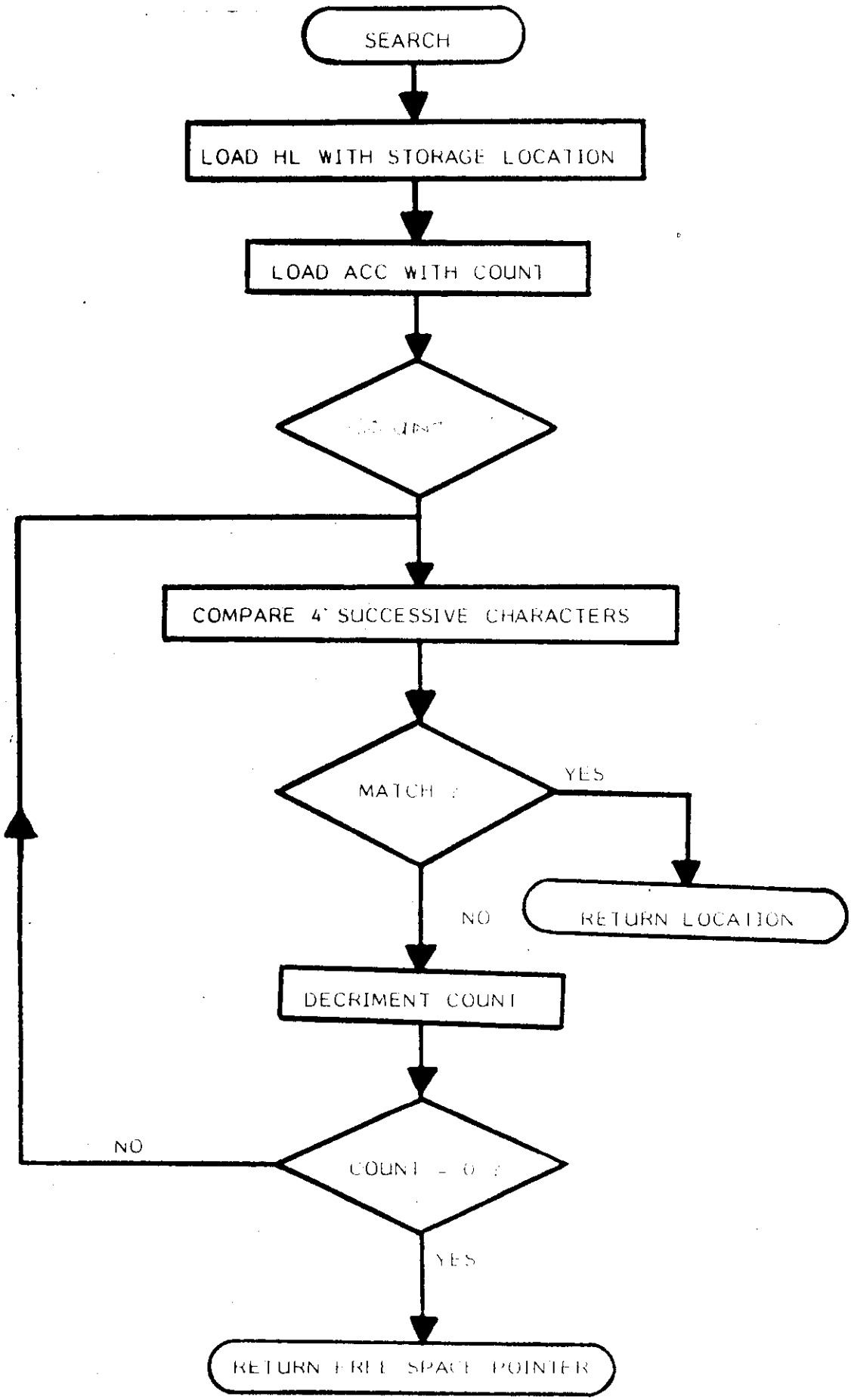


fig 6.1. MAIN ROUTINE.


SEARCH
LOAD HL WITH STORAGE LOCATION
LOAD ACC WITH COUNT
COMPARE 4 SUCCESSIVE CHARACTERS
MATCH ?
YES
RETURN LOCATION
NO
DECRIMENT COUNT
COUNT - 0 ?
NO
YES
RETURN FREE SPACE POINTER

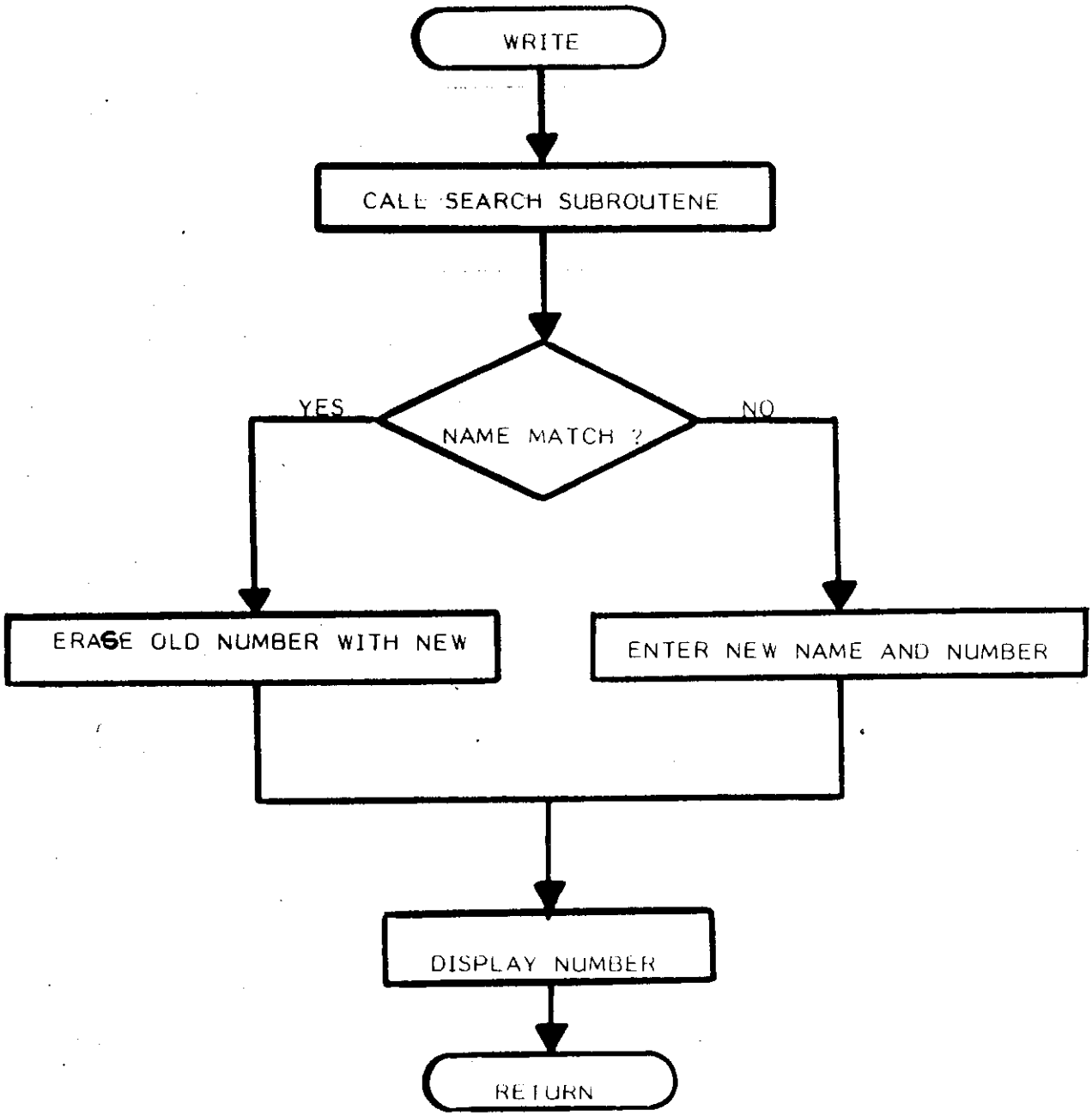


fig 6.2. WRITE SUBROUTINE.

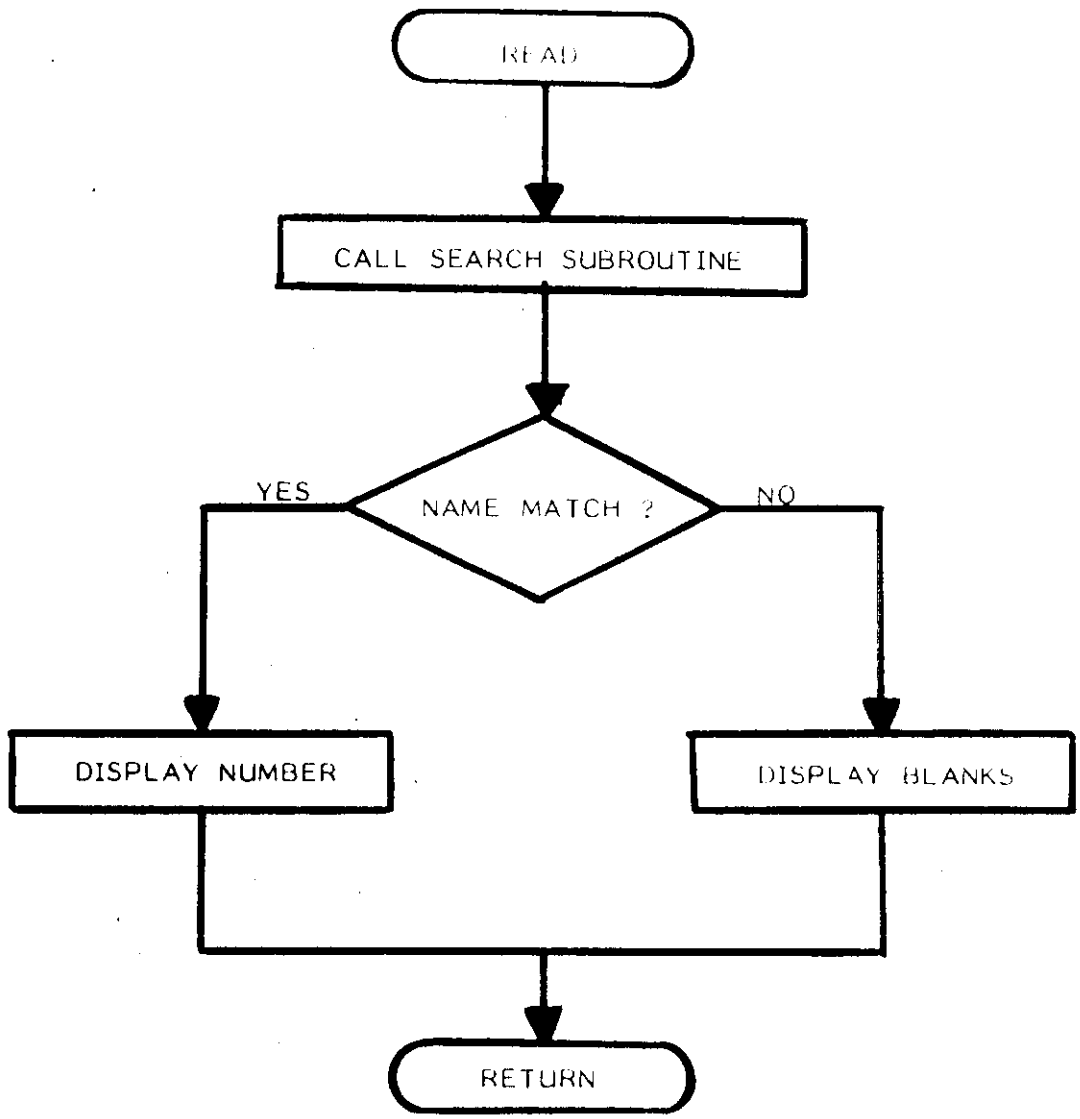


fig 6.3. READ SUBROUTINE.

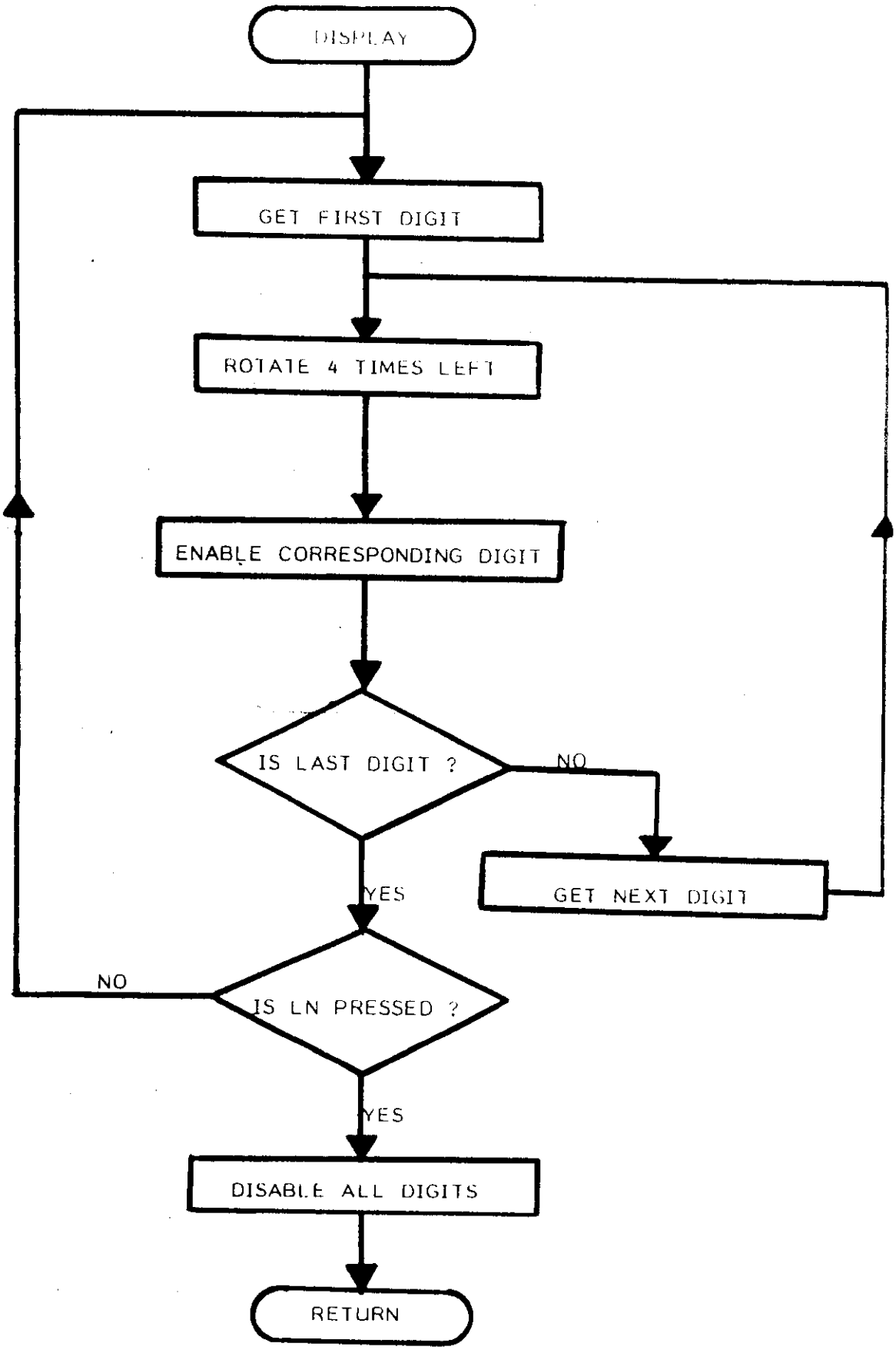


fig 6.4. DISPLAY SUBROUTINE

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Microprocessor Data Hand Book.

intel

8085AH/8085AH-2/8085AH-1
8-BIT HMOS MICROPROCESSORS

- Single +5V Power Supply with 10% Voltage Margins
- 3 MHz, 5 MHz and 6 MHz Selections Available
- 20% Lower Power Consumption than 8085A for 3 MHz and 5 MHz
- 1.3 μs Instruction Cycle (8085AH); 0.8 μs (8085AH-2); 0.67 μs (8085AH-1)
- 100% Compatible with 8085A
- 100% Software Compatible with 8080A
- On-Chip Clock Generator (with External Crystal, LC or RC Network)
- On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control
- Four Vectored Interrupt Inputs (One is Non-Maskable) Plus an 8080A-Compatible Interrupt
- Serial In/Serial Out Port
- Decimal, Binary and Double Precision Arithmetic
- Direct Addressing Capability to 64K Bytes of Memory
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range

The Intel* 8085AH is a complete 8 bit parallel Central Processing Unit (CPU) implemented in N-channel, depletion load, silicon gate technology (HMOS). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's (8085AH (CPU), 8156H (RAM/IO) and 8355/8755A (ROM/PROM/IO)) while maintaining total system expandability. The 8085AH-2 and 8085AH-1 are faster versions of the 8085AH.

The 8085AH incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A, thereby offering a high level of system integration.

The 8085AH uses a multiplexed data bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of 8155H/8156H/8355/8755A memory products allow a direct interface with the 8085AH.

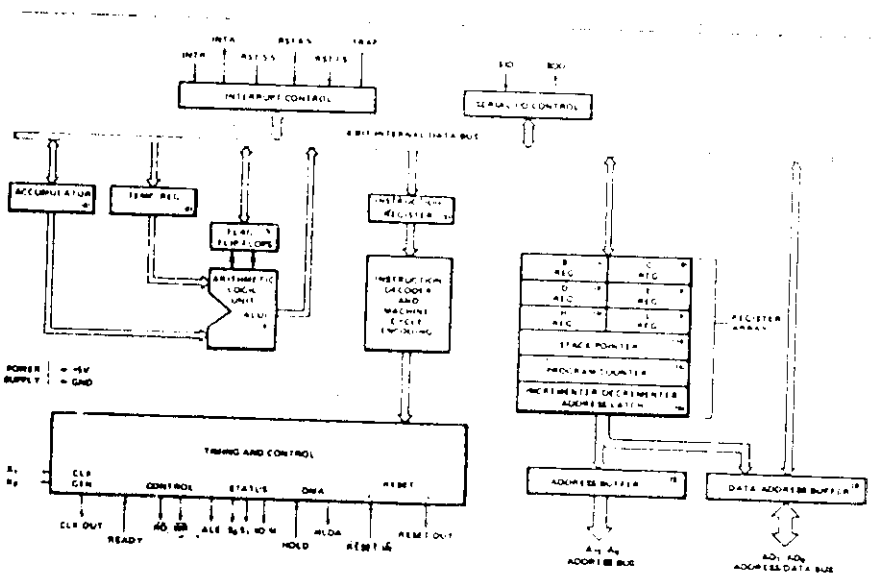


Figure 1. 8085AH CPU Functional Block Diagram

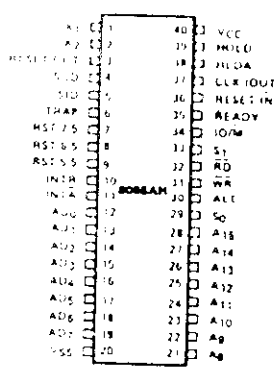


Figure 2. 8085AH Pin Configuration

Table 1. Pin Description

Symbol	Type	Name and Function
A_8–A_{15}	O	**Address Bus:** The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET
AD_0–$_7$	I/O	**Multiplexed Address/Data Bus:** Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles
ALE	O	**Address Latch Enable:** It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated
S_0, S_1, and IO/$\overline{M}$	O	**Machine Cycle Status:** IO/$\overline{M}$ S_1 S_0 Status 0 0 1 Memory write 0 1 0 Memory read 1 0 1 I/O write 1 1 0 I/O read 0 1 1 Opcode fetch 1 1 1 Interrupt Acknowledge · 0 0 Halt · X X Hold · X X Reset · = 3-state (high impedance) X = unspecified S_1 can be used as an advanced R/$\overline{W}$ status. IO/$\overline{M}$, S_0 and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines
$\overline{RD}$	O	**Read Control:** A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer. 3-stated during Hold and Halt modes and during RESET
$\overline{WR}$	O	**Write Control:** A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$. 3-stated during Hold and Halt modes and during RESET

Symbol	Type	Name and Function
READY	I	**Ready:** If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the CPU will wait an integral number of clock cycles for READY to go high before completing the read or write cycle. READY must conform to specified setup and hold times
HOLD	I	**Hold:** Indicates that another master is requesting the use of the address and data buses. The CPU, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data, $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated
HLDA	O	**Hold Acknowledge:** Indicates that the CPU has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The CPU takes the bus one half clock cycle after HLDA goes low
INTR	I	**Interrupt Request:** Is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted
$\overline{INTA}$	O	**Interrupt Acknowledge:** Is used instead of (and has the same timing as) $\overline{RD}$ during the instruction cycle after an INTR is accepted. It can be used to activate an 8259A Interrupt chip or some other interrupt port
RST 5.5 RST 6.5 RST 7.5	I	**Restart Interrupts:** These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in Table 2. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction

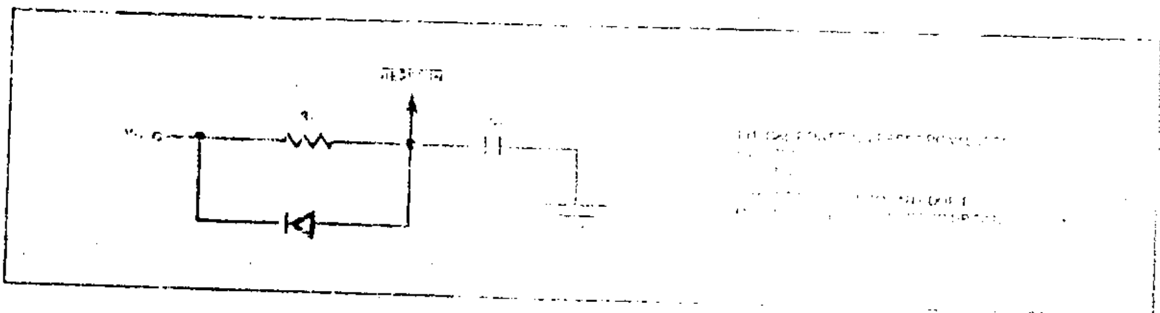
Table 1. [illegible]

Symbol	Type	Name and Function
[illegible]	I	[illegible] interrupt [illegible] maskable RESTART interrupt [illegible] at the same time as INTR [illegible] 5.5-7.5 [illegible] by any mask or Interrupt Enable. It has the highest priority of any interrupt. (See Table 2.)
RESET IN	I	**Reset In:** Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. RESET IN is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay (see Figure 3). Upon power-up, $\overline{RESET\ IN}$ must remain low for at least 10 ms after minimum V_{CC} has been reached. For proper reset operation after the power-up duration, $\overline{RESET\ IN}$ should be kept low a minimum of three clock periods. The CPU is held in the reset condition as long as $\overline{RESET\ IN}$ is applied.
[illegible]	[illegible]	[illegible] being [illegible]. Can be used [illegible]. The signal is synchronized [illegible] processor clock and lasts an integral number of clock periods.
X_1, X_2	I	**X_1 and X_2:** Are connected to a crystal, LC, or RC network to drive the internal clock generator. X_1 can [illegible] frequency is divided by 2 to give the [illegible] internal operating frequency.
[illegible]	[illegible]	[illegible] The period of [illegible] X_1, X_2 input [illegible]
SID	I	**Serial Input Data Line:** The data on this line is loaded into accumulator [illegible] whenever a RIM instruction is [illegible]
SOD	O	**Serial Output Data Line:** The output SOD is set or reset as specified by the SIM instruction.
V_{CC}		**Power:** +5 volt supply.
V_{SS}		**Ground:** Reference.

Table 2. Interrupt Priority, Restart Address, and Sensitivity

Name	Priority	Address Branched To (1) When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge AND [illegible]
RST 7.5	2	3CH	Rising edge [illegible]
RST 6.5	3	34H	High level until sampled
RST 5.5	4	2CH	High level until sampled
INTR	5	See Note 2	High level until sampled

NOTES:
1. The processor pushes the PC on the stack before branching to the indicated address.
2. The address branched to depends on the instruction provided to the cpu when the interrupt is acknowledged.



FUNCTIONAL DESCRIPTION

The 8085AH is a complete 8-bit parallel central processor. It is designed with N-channel, depletion load, silicon gate technology (HMOS), and requires a single +5 volt supply. Its basic clock speed is 3 MHz (8085AH), 5 MHz (8085AH-2), or 6 MHz (8085AH-1), thus improving on the present 8080A's performance with higher system speed. Also it is designed to fit into a minimum system of three IC's: The CPU (8085AH), a RAM/IO (8156H), and a ROM or EPROM/IO chip (8355 or 8755A).

The 8085AH has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or as 16-bit register pairs. The 8085AH register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8 bits
PC	Program Counter	16-bit address
BC,DE,HL	General-Purpose Registers; data pointer (HL)	8 bits x 6 or 16 bits x 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flags (8-bit space)

The 8085AH uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data bus. These lower 8 bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

The 8085AH provides $\overline{RD}$, $\overline{WR}$, S_0, S_1, and IO/$\overline{M}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{INTA}$) is also provided. HOLD and all interrupts are synchronized with the processor's internal clock. The 8085AH also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for simple serial interface.

In addition to these features, the 8085AH has three maskable, vector interrupt pins, one nonmaskable TRAP interrupt, and a bus vectored interrupt, INTR.

INTERRUPT AND SERIAL I/O

The 8085AH has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the 8080A INT. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks. (See Table 2.)

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are *high level-sensitive* like INTR (and INT on the 8080) and are recognized with the same timing as INTR. RST 7.5 is *rising edge-sensitive*.

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request (a normally high level signal with a low going pulse is recommended for highest system noise immunity). The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a $\overline{RESET\ IN}$ to the 8085AH. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and $\overline{RESET\ IN}$. (See SIM, Chapter 5 of the MCS-80/85 User's Manual.)

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP—highest priority, RST 7.5, RST 6.5, RST 5.5, INTR—lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both *edge and level sensitive*. The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. Figure 4 illustrates the TRAP interrupt request circuitry within the 8085AH. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

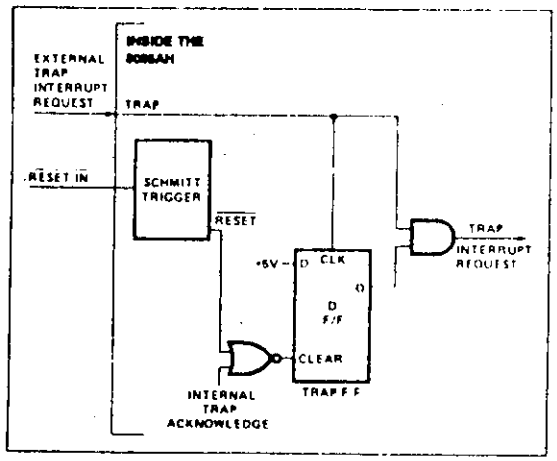


Figure 4. TRAP and RESET IN Circuit

The TRAP interrupt is special in that it disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR, or RST 5.5–7.5 will provide current interrupt Enable status, revealing that interrupts are disabled. See the description of the RIM instruction in the MCS-80/85 Family User's Manual.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

DRIVING THE X_1 AND X_2 INPUTS

You may drive the clock inputs of the 8085AH, 8085AH-2, or 8085AH-1 with a crystal, an LC tuned circuit, an RC network, or an external clock source. The crystal frequency must be at least 1 MHz, and must be twice the desired internal clock frequency; hence, the 8085AH is operated with a 6 MHz crystal (for 3 MHz clock), the 8085AH-2 operated with a 10 MHz crystal (for 5 MHz clock), and the 8085AH-1 can be operated with a 12 MHz crystal (for 6 MHz clock). If a crystal is used, it must have the following characteristics:

Parallel resonance at twice the clock frequency desired
C_L (load capacitance) ≤ 30 pF
C_S (shunt capacitance) ≤ 7 pF
R_S (equivalent shunt resistance) ≤ 75 Ohms
Drive level: 10 mW
Frequency tolerance: ±.005% (suggested)

Note the use of the 20 pF capacitor between X_2 and ground. This capacitor is required with crystal frequencies below 4 MHz to assure oscillator startup at the correct frequency. A parallel-resonant LC circuit may be used as the frequency-determining network for the 8085AH, providing that its frequency tolerance of approximately ±10% is acceptable. The components are chosen from the formula:

$$f = \frac{1}{2\pi\sqrt{L(C_{ext} + C_{int})}}$$

To minimize variations in frequency, it is recommended that you choose a value for C_{ext} that is at least twice that of C_{int}, or 30 pF. The use of an LC circuit is not recommended for frequencies higher than approximately 5 MHz.

An RC circuit may be used as the frequency-determining network for the 8085AH if maintaining a precise clock frequency is of no importance. Variations in the on-chip timing generation can cause a wide variation in frequency when using the RC mode. Its advantage is its low component cost. The driving frequency generated by the circuit shown is approximately 3 MHz. It is not recommended that frequencies greatly higher or lower than this be attempted.

Figure 5 shows the recommended clock driver circuits. Note in D and E that pullup resistors are required to assure that the high level voltage of the input is at least 4V and maximum low level voltage of 0.8V.

For driving frequencies up to and including 6 MHz you may supply the driving signal to X_1 and leave X_2 open-circuited (Figure 5D). If the driving frequency is from 6 MHz to 12 MHz, stability of the clock generator will be improved by driving both X_1 and X_2 with a push-pull source (Figure 5E). To prevent self-oscillation of the 8085AH, be sure that X_2 is not coupled back to X_1 through the driving circuit.

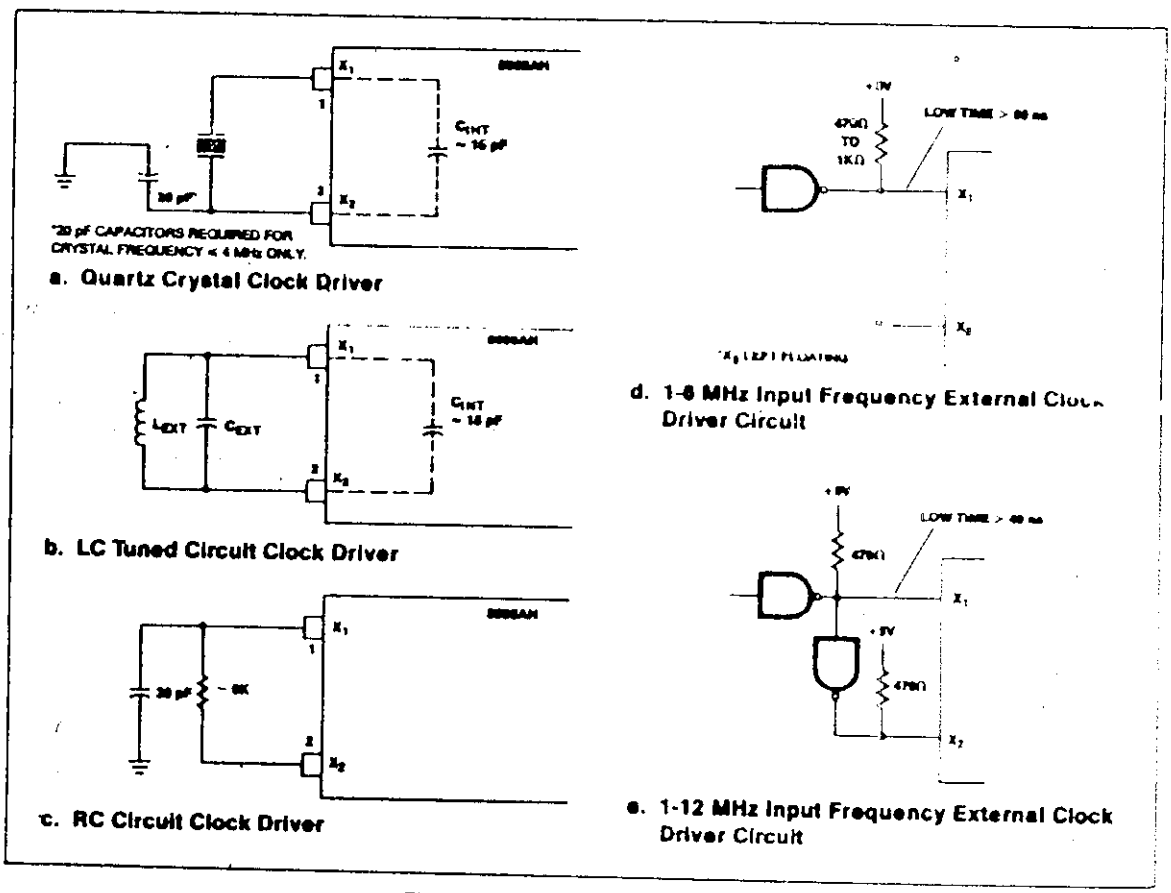


Figure 5. Clock Driver Circuits

GENERATING AN 8085AH WAIT STATE

If your system requirements are such that slow memories or peripheral devices are being used, the circuit shown in Figure 6 may be used to insert one WAIT state in each 8085AH machine cycle.

The D flip-flops should be chosen so that
- CLK is rising edge-triggered
- CLEAR is low-level active.

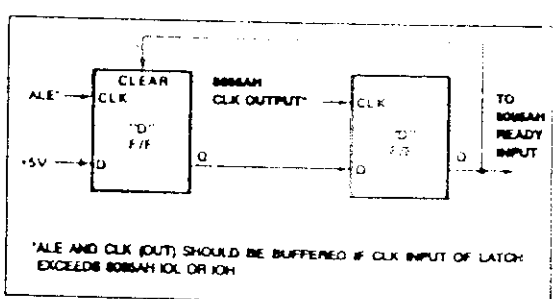


Figure 6. Generation of a Wait State for 8085AH CPU

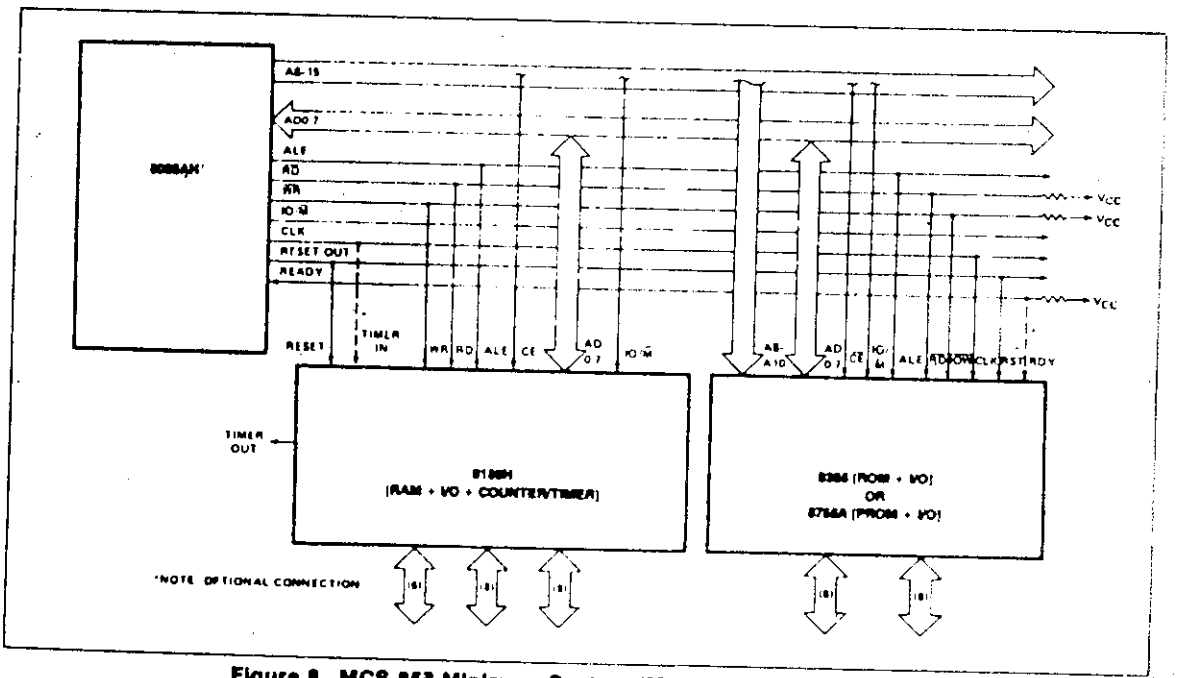


Figure 8. MCS-85® Minimum System (Memory Mapped I/O)

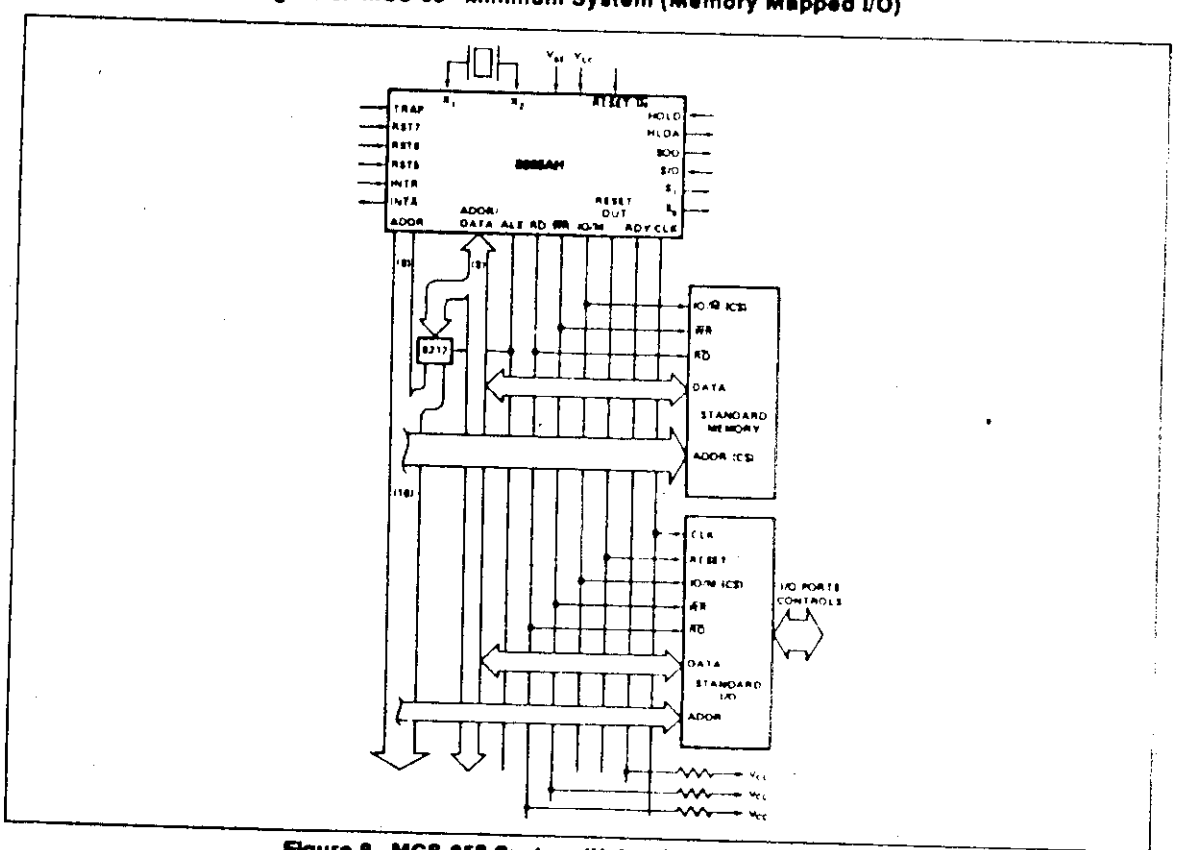


Figure 9. MCS-85® System (Using Standard Memories)

As in the 8080, the READY line is used to extend the read and write pulse lengths so that the 8085AH can be used with slow memory. HOLD causes the CPU to relinquish the bus when it is through with it by floating the Address and Data Buses.

SYSTEM INTERFACE

The 8085AH family includes memory components, which are directly compatible to the 8085AH CPU. For example, a system consisting of the three chips, 8085AH, 8156H, and 8355 will have the following features:

- 2K Bytes ROM
- 256 Bytes RAM
- 1 Timer/Counter
- 4 8-bit I/O Ports
- 1 6-bit I/O Port
- 4 Interrupt Levels
- Serial In/Serial Out Ports

This minimum system, using the standard I/O technique is as shown in Figure 7.

In addition to standard I/O, the memory mapped I/O offers an efficient I/O addressing technique. With this technique, an area of memory address space is assigned for I/O address, thereby, using the memory address for I/O manipulation. Figure 8 shows the system configuration of Memory Mapped I/O using 8085AH.

The 8085AH CPU can also interface with the standard memory that does *not* have the multiplexed address/data bus. It will require a simple 8212 (8-bit latch) as shown in Figure 9.

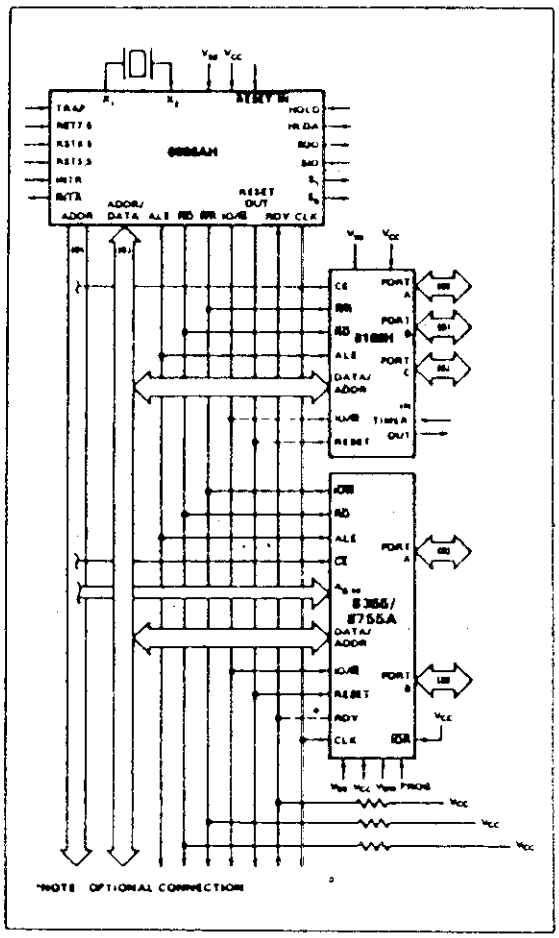


Figure 7. 8085AH Minimum System (Standard I/O Technique)

BASIC SYSTEM TIMING

The 8085AH has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Figure 10 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines ($IO/\overline{M}$, S_1, S_0) and the three control signals ($\overline{RD}$, $\overline{WR}$, and $\overline{INTA}$). (See Table 3.) The status lines can be used as advanced controls (for device selection, for example), since they become active at the T_1 state, at the outset of each machine cycle. Control lines $\overline{RD}$ and $\overline{WR}$ become active later, at the time when the transfer of data is to take place, so are used as command lines.

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless WAIT or HOLD states are forced by the receipt of $\overline{READY}$ or HOLD inputs). Any T state must be one of ten possible states, shown in Table 4.

Table 3. 8085AH Machine Cycle Chart

MACHINE CYCLE			STATUS			CONTROL		
			$IO/\overline{M}$	S_1	S_0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
OPCODE FETCH	(OF)		0	1	1	0	1	1
MEMORY READ	(MR)		0	1	0	0	1	1
MEMORY WRITE	(MW)		0	0	1	1	0	1
I/O READ	(IOR)		1	1	0	0	1	1
I/O WRITE	(IOW)		1	0	1	1	0	1
ACKNOWLEDGE OF INTR	(INA)		1	1	1	1	1	0
BUS IDLE	(BI)	DAD	0	1	0	1	1	1
		ACK OF RST TRAP	1	1	1	1	1	1
		HALT	TS	0	0	TS	TS	1

Table 4. 8085AH Mecnine State Chart

Machine State	Status & Buses				Control			
	S_1, S_0	$IO/\overline{M}$	A_8-A_{15}	AD_0-AD_7	$\overline{RD}$, $\overline{WR}$		$\overline{INTA}$	ALE
T_1	X	X	X	X	1	1	1	1*
T_2	X	X	X	X	X	X	1	0
T_{WAIT}	X	X	X	X	X	X	1	0
T_3	X	X	X	X	X	X	1	0
T_4	1	0†	X	TS	1	1	1	0
T_5	1	0†	X	TS	1	1	1	0
T_6	1	0†	X	TS	1	1	1	0
T_{RESET}	X	TS	TS	TS	TS	TS	1	0
T_{HALT}	0	TS	TS	TS	TS	TS	1	0
T_{HOLD}	X	TS	TS	TS	TS	TS	1	0

0 = Logic "0" TS = High Impedance
1 = Logic "1" X = Unspecified

* ALE not generated during 2nd and 3rd machine cycles of DAD instruction
† IO/M = 1 during T_4-T_6 of INA machine cycle

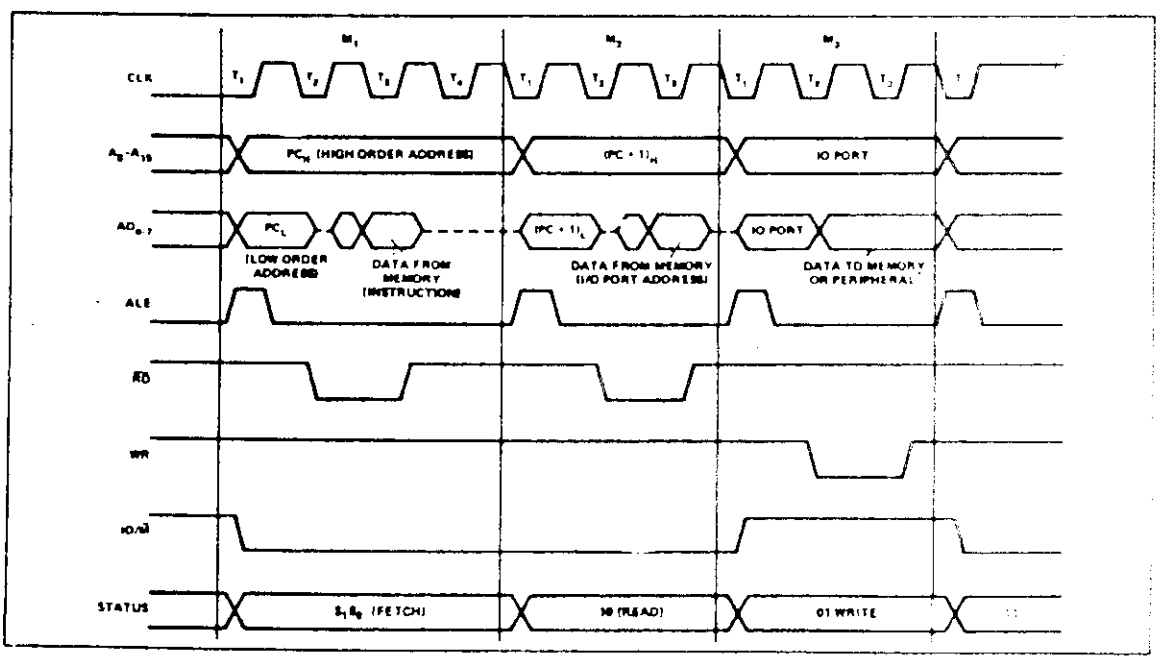


Figure 10. 8085AH Basic System Timing

Table 6. Instruction Set Summary

Mnemonic	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Operations Description
MOVE, LOAD, AND STORE									
MOV r1 r2	0	1	D	D	D	S	S	S	Move register to register
MOV M r	0	1	1	1	0	S	S	S	Move register to memory
MOV r M	0	1	D	D	D	1	1	0	Move memory to register
MVI r	0	0	D	D	D	1	1	0	Move immediate register
MVI M	0	0	1	1	0	1	1	0	Move immediate memory
LXI B	0	0	0	0	0	0	0	1	Load immediate register Pair B & C
LXI D	0	0	0	1	0	0	0	1	Load immediate register Pair D & E
LXI H	0	0	1	0	0	0	0	1	Load immediate register Pair H & L
STAX B	0	0	0	0	0	0	1	0	Store A indirect
STAX D	0	0	0	1	0	0	1	0	Store A indirect
LDAX B	0	0	0	0	1	0	1	0	Load A indirect
LDAX D	0	0	0	1	1	0	1	0	Load A indirect
STA	0	0	1	1	0	0	1	0	Store A direct
LDA	0	0	1	1	1	0	1	0	Load A direct
SHLD	0	0	1	0	0	0	1	0	Store H & L direct
LHLD	0	0	1	0	1	0	1	0	Load H & L direct
XCHG	1	1	1	0	1	0	1	1	Exchange D & E, H & L Registers
STACK OPS									
PUSH B	1	1	0	0	0	1	0	1	Push register Pair B & C on stack
PUSH D	1	1	0	1	0	1	0	1	Push register Pair D & E on stack
PUSH H	1	1	1	0	0	1	0	1	Push register Pair H & L on stack
PUSH PSW	1	1	1	1	0	1	0	1	Push A and Flags on stack
POP B	1	1	0	0	0	0	0	1	Pop register Pair B & C off stack
POP D	1	1	0	1	0	0	0	1	Pop register Pair D & E off stack
POP H	1	1	1	0	0	0	0	1	Pop register Pair H & L off stack
POP PSW	1	1	1	1	0	0	0	1	Pop A and Flags off stack
XTHL	1	1	1	0	0	0	1	1	Exchange top of stack, H & L
SPHL	1	1	1	1	1	0	0	1	H & L to stack pointer
LXI SP	0	0	1	1	0	0	0	1	Load immediate stack pointer
INX SP	0	0	1	1	0	0	1	1	Increment stack pointer
DCX SP	0	0	1	1	1	0	1	1	Decrement stack pointer
JUMP									
JMP	1	1	0	0	0	0	1	1	Jump unconditional
JC	1	1	0	1	1	0	1	0	Jump on carry
JNC	1	1	0	1	0	0	1	0	Jump on no carry
JZ	1	1	0	0	1	0	1	0	Jump on zero
JNZ	1	1	0	0	0	0	1	0	Jump on no zero
JP	1	1	1	1	0	0	1	0	Jump on positive
JM	1	1	1	1	1	0	1	0	Jump on minus
JPE	1	1	1	0	1	0	1	0	Jump on parity even
JPO	1	1	1	0	0	0	1	0	Jump on parity odd
PCHL	1	1	1	0	1	0	0	1	H & L to program counter
CALL									
CALL	1	1	0	0	1	1	0	1	Call unconditional
CC	1	1	0	1	1	1	0	0	Call on carry
CNC	1	1	0	1	0	1	0	0	Call on no carry
CZ	1	1	0	0	1	1	0	0	Call on zero
CNZ	1	1	0	0	0	1	0	0	Call on no zero
CP	1	1	1	1	0	1	0	0	Call on positive
CM	1	1	1	1	1	1	0	0	Call on minus
CPE	1	1	1	0	1	1	0	0	Call on parity even
CPO	1	1	1	0	0	1	0	0	Call on parity odd
RETURN									
RET	1	1	0	0	1	0	0	1	Return
RC	1	1	0	1	1	0	0	0	Return on carry
RNC	1	1	0	1	0	0	0	0	Return on no carry
RZ	1	1	0	0	1	0	0	0	Return on zero
RNZ	1	1	0	0	0	0	0	0	Return on no zero
RP	1	1	1	1	0	0	0	0	Return on positive
RM	1	1	1	1	1	0	0	0	Return on minus
RPE	1	1	1	0	1	0	0	0	Return on parity even
RPO	1	1	1	0	0	0	0	0	Return on parity odd
RESTART									
RST	1	1	A	A	A	1	1	1	Restart
INPUT/OUTPUT									
IN	1	1	0	1	1	0	1	1	Input
OUT	1	1	0	1	0	0	1	1	Output
INCREMENT AND DECREMENT									
INR r	0	0	D	D	D	1	0	0	Increment register
DCR r	0	0	D	D	D	1	0	1	Decrement register
INR M	0	0	1	1	0	1	0	0	Increment memory
DCR M	0	0	1	1	0	1	0	1	Decrement memory
INX B	0	0	0	0	0	0	1	1	Increment B & C registers
INX D	0	0	0	1	0	0	1	1	Increment D & E registers
INX H	0	0	1	0	0	0	1	1	Increment H & L registers
DCX B	0	0	0	0	1	0	1	1	Decrement B & C
DCX D	0	0	0	1	1	0	1	1	Decrement D & E
DCX H	0	0	1	0	1	0	1	1	Decrement H & L
ADD									
ADD r	1	0	0	0	0	S	S	S	Add register to A
ADC r	1	0	0	0	1	S	S	S	Add register to A with carry
ADD M	1	0	0	0	0	1	1	0	Add memory to A
ADC M	1	0	0	0	1	1	1	0	Add memory to A with carry
ADI	1	1	0	0	0	1	1	0	Add immediate to A
ACI	1	1	0	0	1	1	1	0	Add immediate to A with carry
DAD B	0	0	0	0	1	0	0	1	Add B & C to H & L
DAD D	0	0	0	1	1	0	0	1	Add D & E to H & L
DAD H	0	0	1	0	1	0	0	1	Add H & L to H & L
DAD SP	0	0	1	1	1	0	0	1	Add stack pointer to H & L
SUBTRACT									
SUB r	1	0	0	1	0	S	S	S	Subtract register from A
SBB r	1	0	0	1	1	S	S	S	Subtract register from A with borrow
SUB M	1	0	0	1	0	1	1	0	Subtract memory from A
SBB M	1	0	0	1	1	1	1	0	Subtract memory from A with borrow
SUI	1	1	0	1	0	1	1	0	Subtract immediate from A
SBI	1	1	0	1	1	1	1	0	Subtract immediate from A with borrow

Table 6. Instruction Set Summary (Continued)

Mnemonic	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Operations Description
LOGICAL									
ANA r	1	0	1	0	0	S	S	S	And register with A
XRA r	1	0	1	0	1	S	S	S	Exclusive OR register with A
ORA r	1	0	1	1	0	S	S	S	OR register with A
CMP r	1	0	1	1	1	S	S	S	Compare register with A
ANA M	1	0	1	0	0	1	1	0	And memory with A
XRA M	1	0	1	0	1	1	1	0	Exclusive OR memory with A
ORA M	1	0	1	1	0	1	1	0	OR memory with A
CMP M	1	0	1	1	1	1	1	0	Compare memory with A
ANI	1	1	1	0	0	1	1	0	And immediate with A
XRI	1	1	1	0	1	1	1	0	Exclusive OR immediate with A
ORI	1	1	1	1	0	1	1	0	OR immediate with A
CPI	1	1	1	1	1	1	1	0	Compare immediate with A
ROTATE									
RLC	0	0	0	0	0	1	1	1	Rotate A left
RRC	0	0	0	0	1	1	1	1	Rotate A right
RAL	0	0	0	1	0	1	1	1	Rotate A left through carry
RAR	0	0	0	1	1	1	1	1	Rotate A right through carry

Mnemonic	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Operations Description
SPECIALS									
CMA	0	0	1	0	1	1	1	1	Complement A
STC	0	0	1	1	0	1	1	1	Set carry
CMC	0	0	1	1	1	1	1	1	Complement carry
DAA	0	0	1	0	0	1	1	1	Decimal adjust A
CONTROL									
EI	1	1	1	1	1	0	1	1	Enable interrupts
DI	1	1	1	1	0	0	1	1	Disable interrupt
NOP	0	0	0	0	0	0	0	0	No-operation
HLT	0	1	1	1	0	1	1	0	Halt
NEW 8085A INSTRUCTIONS									
RIM	0	0	1	0	0	0	0	0	Read Interrupt Mask
SIM	0	0	1	1	0	0	0	0	Set Interrupt Mask

NOTES:

1. DDS or SSS: B 000, C 001, D 010, E 011, H 100, L 101, Memory 110, A 111
2. Two possible cycle times (6/12) indicate instruction cycles dependent on condition flags

Unspecified 8085A Op Codes

NEW 8085 INSTRUCTIONS

NEW CONDITION CODES

X5 = bit 5

Condition code format							
S	Z	X5	AC	0	P	V	C

2's complement overflow
Underflow (DLX), or overflow (IVX)
X5 = 01·02 + 01·R + 02·R, where
01 = sign of operand 1, 02 = sign of operand 2
R = sign of result. For subtraction and comparisons replace 02 with $\overline{02}$

DSUB (double subtraction)

(H) (L) = (H) (L) - (B) (C)
The contents of register pair B and C are subtracted from the contents of register pair H and L. The result is placed in register pair H and L. All condition flags are affected.

0 0 0 0 1 0 0 0

(08)

cycles	3
states	10
addressing	register
flags	Z, S, P, CY, AC, X5, V

ARHL (arithmetic shift of H and L to the right)

(H7=H7), (Hn-1) = (Hn)
(L7=H0), (Ln-1) = (Ln), (CY) = (L0)
The contents of register pair H and L are shifted right one bit. The uppermost bit is duplicated and the lowest bit is shifted into the carry bit. The result is placed in register pair H and L. Note: only the CY flag is affected.

0 0 0 1 0 0 0 0

(10)

cycles	2
states	7
addressing	register
flags	CY

RDEL (rotate D and E left through carry)

(Dn+1) = (Dn), (D0) = (E7)
(CY) = (D7), (En+1) = (En), (E0) = (CY)
The contents of register pair D and E are rotated left one position through the carry flag. The low order bit is set equal to the CY flag and the CY flag is set to the value shifted out of the high order bit. Only the CY and the V flags are affected.

0 0 0 1 1 0 0 0

(18)

cycles	3
states	10
addressing	register
flags	CY, V

LDHI (load D and E with H and L plus immediate byte)

(D) (E) = (H) (L) + (byte 2)
The contents of register pair H and L are added to the immediate byte. The result is placed in register pair D and E. Note: no condition flags are affected.

0 0 1 0 1 0 0 0
data

(28)

cycles	3
states	10
addressing	immediate register
flags	none

LDSI (load D and E with SP plus immediate byte)

(D) (E) = (SPH) (SPL) + (byte 2)
The contents of register pair SP are added to the immediate byte. The result is placed in register pair D and E. Note: no condition flags are affected.

0 0 1 1 1 0 0 0
data

(38)

cycles	3
states	10
addressing	immediate register
flags	none

RSTV (restart on overflow)

IF (V)
((SP)-1) = (PCH)
((SP)-2) = (PCL)
(SP) = (SP)-2
(PC) = 40 hex

If the overflow flag V is set, the actions specified above are performed; otherwise control continues sequentially.

1 1 0 0 1 0 1 1

(CB)

cycles	1 or 3
states	6 or 12
addressing	register indirect
flags	none

SHLX (store H and L indirect through D and E)

((D)(E)) = (L)
((D)(E)+1) = (H)
The contents of register L are moved to the memory location whose address is in register pair D and E. The contents of register H are moved to the succeeding memory location.

1 1 0 1 1 0 0 1

(D9)

cycles	3
states	10
addressing	register indirect
flags	none

JNX5 (jump on not X5)

IF (not X5)
(PC) = (byte 3) (byte 2)
If the X5 flag is reset, control is transferred to the instruction whose address is specified in byte 3 and byte 2 of the current instruction; otherwise control continues sequentially.

1 1 0 1 1 1 0 1
low order address
high order address

(DD)

cycles	2 or 3
states	7 or 10
addressing	immediate
flags	none

LHLX (load H and L indirect through D and E)

(L) = ((D)(E))
(H) = ((D)(E)+1)
The content of the memory location whose address is in D and E are moved to register L. The contents of the succeeding memory location are moved to register H.

1 1 1 0 1 1 0 1

(ED)

cycles	3
states	10
addressing	register indirect
flags	none

JX5 (jump on X5)

IF (X5)
(PC) = (byte 3) (byte 2)
If the X5 flag is reset, control is transferred to the instruction whose address is specified in byte 3 and byte 2 of the current instruction; otherwise control continues sequentially.

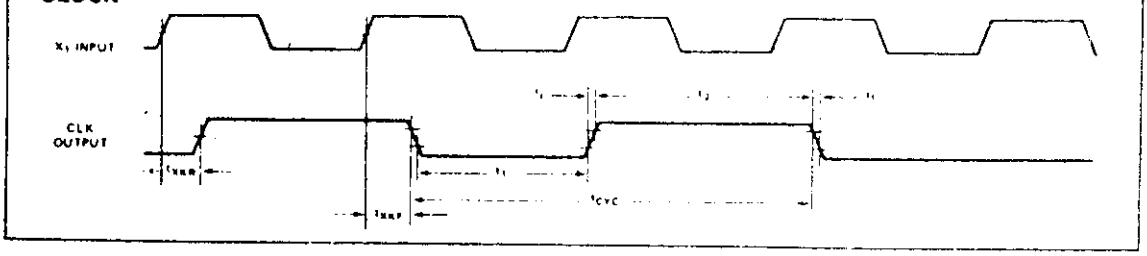
1 1 1 1 1 1 0 1
low order address
high order address

(FD)

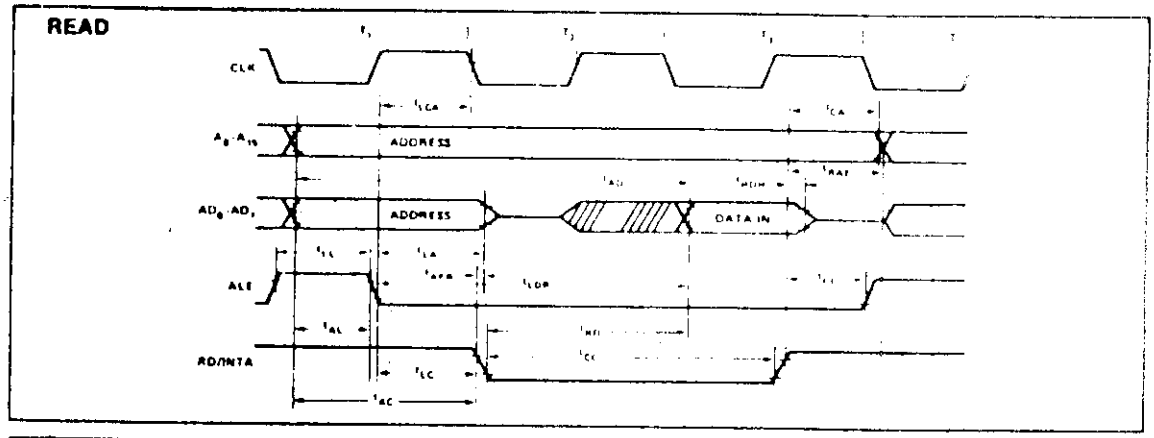
cycles	2 or 3
states	7 or 10
addressing	immediate
flags	none

WAVEFORMS

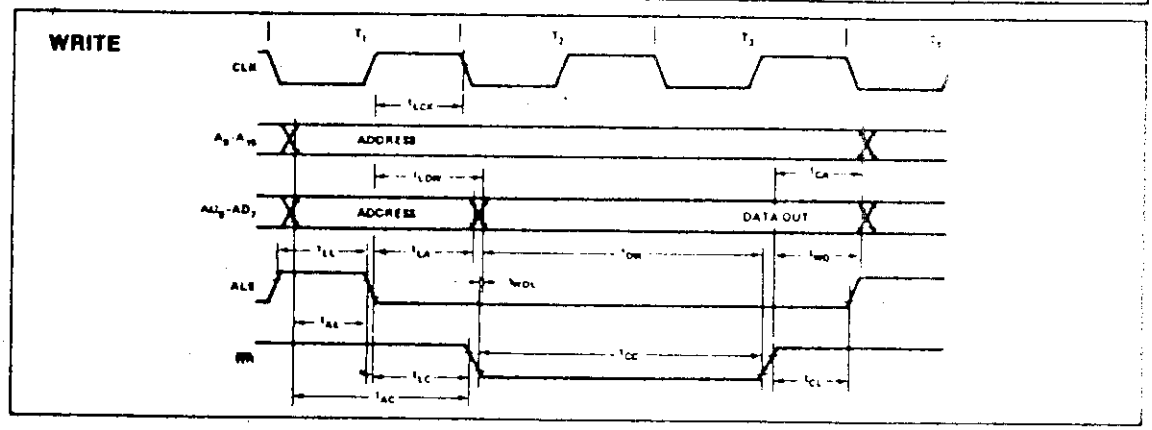
CLOCK



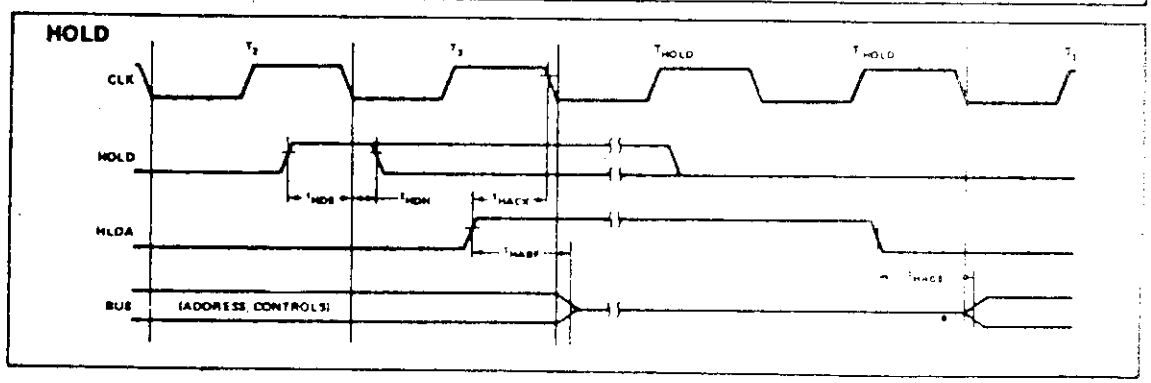
READ



WRITE



HOLD



intel

8155H/8156H/8155H-2/8156H-2
2048-BIT STATIC HMOS RAM WITH I/O PORTS AND TIMER

- Single +5V Power Supply with 10% Voltage Margins
- 30% Lower Power Consumption than the 8155 and 8156
- 100% Compatible with 8155 and 8156
- 256 Word x 8 Bits
- Completely Static Operation
- Internal Address Latch
- 2 Programmable 8-Bit I/O Ports
- 1 Programmable 6-Bit I/O Port
- Programmable 14-Bit Binary Counter/ Timer
- Compatible with 8085AH, 8085A and 8088 CPU
- Multiplexed Address and Data Bus
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range

The Intel® 8155H and 8156H are RAM and I/O chips implemented in N-Channel, depletion load, silicon gate technology (HMOS), to be used in the 8085AH and 8088 microprocessor systems. The RAM portion is designed with 2048 static cells organized as 256 x 8. They have a maximum access time of 400 ns to permit use with no wait states in 8085AH CPU. The 8155H-2 and 8156H-2 have maximum access times of 330 ns for use with the 8085AH-2 and the 5 MHz 8088 CPU.

The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.

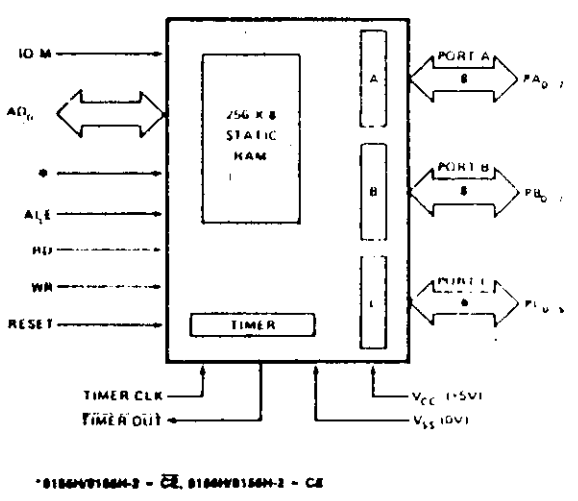


Figure 1. Block Diagram

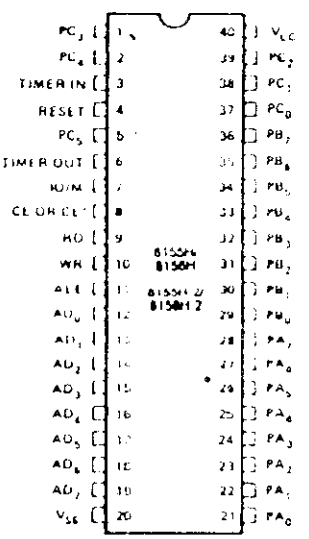


Figure 2. Pin Configuration

Table 1. Pin Description

Symbol	Type	Name and Function
RESET	I	**Reset:** Pulse provided by the 8085AH to initialize the system (connect to 8085AH RESET OUT). Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two 8085AH clock cycle times
AD_{0-7}	I/O	**Address/Data:** 3-state Address/Data lines that interface with the CPU lower 8 bit Address/Data Bus. The 8-bit address is latched into the address latch inside the 8155H/5BH on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/$\overline{M}$ input. The 8-bit data is either written into the chip or read from the chip, depending on the $\overline{WR}$ or $\overline{RD}$ input signal.
CE or $\overline{CE}$	I	**Chip Enable:** On the 8155H, this pin is $\overline{CE}$ and is ACTIVE LOW. On the 8156H, this pin is CE and is ACTIVE HIGH.
$\overline{RD}$	I	**Read Control:** Input low on this line with the Chip Enable active enables and AD_{0-7} buffers. If IO/$\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command status registers will be read to the AD bus.
$\overline{WR}$	I	**Write Control:** Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register, depending on IO/$\overline{M}$
ALE	I	**Address Latch Enable:** This control signal latches both the address on the AD_{0-7} lines and the state of the Chip Enable and IO/$\overline{M}$ into the chip at the falling edge of ALE.
IO/$\overline{M}$	I	**I/O Memory:** Selects memory if low and I/O and command/status registers if high.
PA_{0-7}(8)	I/O	**Port A:** These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PB_{0-7}(8)	I/O	**Port B:** These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PC_{0-5}(6)	I/O	**Port C:** These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When PC_{0-5} are used as control signals, they will provide the following: PC_0 — A INTR (Port A Interrupt) PC_1 — ABF (Port A Buffer Full) PC_2 — $\overline{A\ STB}$ (Port A Strobe) PC_3 — B INTR (Port B Interrupt) PC_4 — $\overline{B}$ BF (Port B Buffer Full) PC_5 — $\overline{B\ STB}$ (Port B Strobe)
TIMER IN	I	**Timer Input:** Input to the counter-timer.
$\overline{TIMER\ OUT}$	O	**Timer Output:** This output can be either a square wave or a pulse, depending on the timer mode.
V_{CC}		**Voltage:** +5 volt supply
V_{SS}		**Ground:** Ground reference

FUNCTIONAL DESCRIPTION

The 8155H/8156H contains the following:

- 2k Bit Static RAM organized as 256 x 8
- Two 8-bit I/O ports (PA & PB) and one 6-bit I/O port (PC)
- 14-bit timer/counter

The IO/$\overline{M}$ (IO/Memory Select) pin selects either the five registers (Command, Status, PA_{0-7}, PB_{0-7}, PC_{0-5}) or the memory (RAM) portion.

The 8-bit address on the Address/Data lines, Chip Enable input CE or $\overline{CE}$, and IO/$\overline{M}$ are all latched on-chip at the falling edge of ALE.

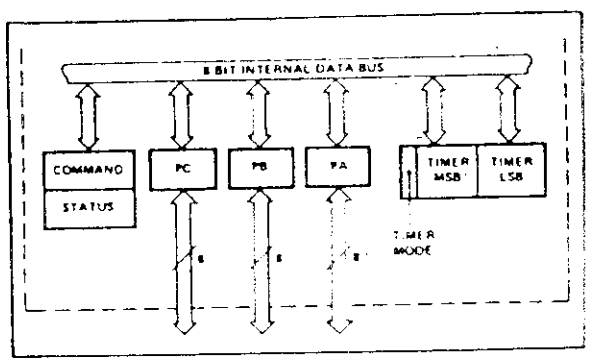


Figure 3. 8155H/8156H Internal Registers

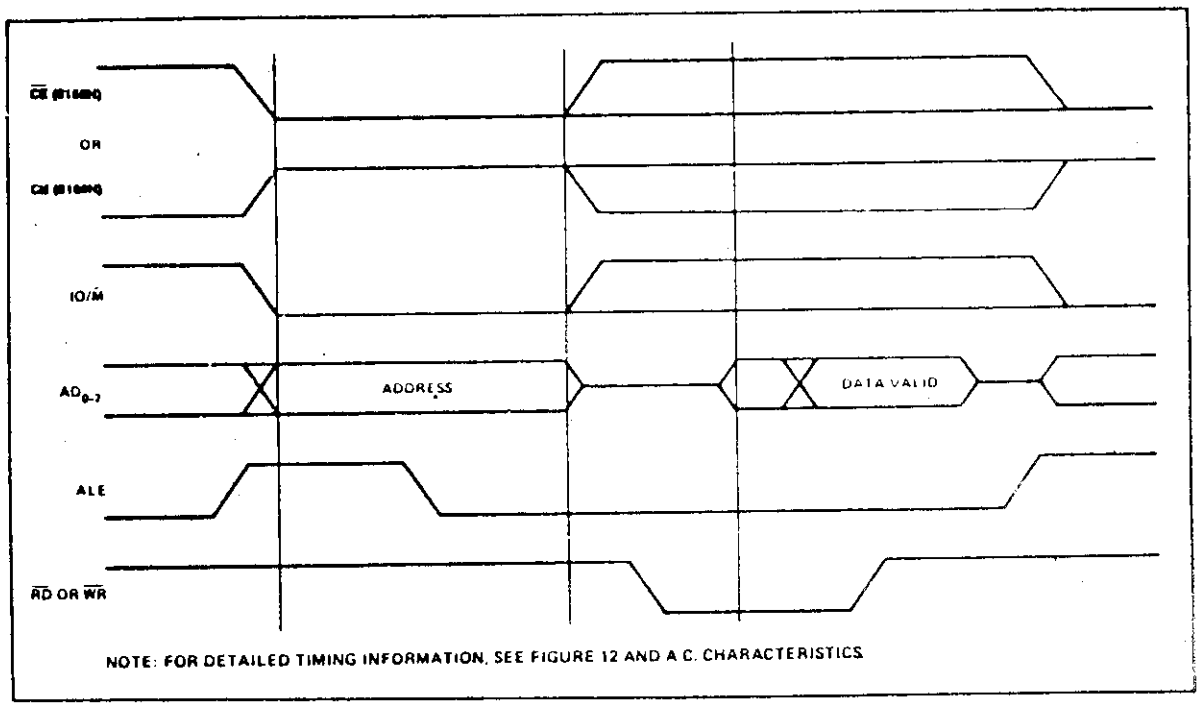


Figure 4. 8155H/8156H On-Board Memory Read/Write Cycle

PROGRAMMING OF THE COMMAND REGISTER

The command register consists of eight latches. Four bits (0-3) define the mode of the ports, two bits (4-5) enable or disable the interrupt from port C when it acts as control port, and the last two bits (6-7) are for the timer.

The command register contents can be altered at any time by using the I/O address XXXXX000 during a WRITE operation with the Chip Enable active and IO/$\overline{M}$ = 1. The meaning of each bit of the command byte is defined in Figure 5. The contents of the command register may never be read.

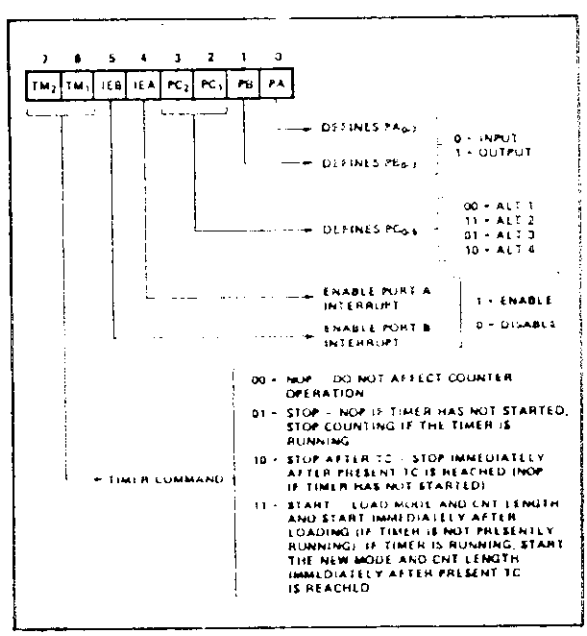


Figure 5. Command Register Bit Assignment

READING THE STATUS REGISTER

The status register consists of seven latches, one for each bit: six (0-5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polled by reading the Status Register (Address XXXXX000). Status word format is shown in Figure 6. Note that you may never write to the status register since the command register shares the same I/O address and the command register is selected when a write to that address is issued.

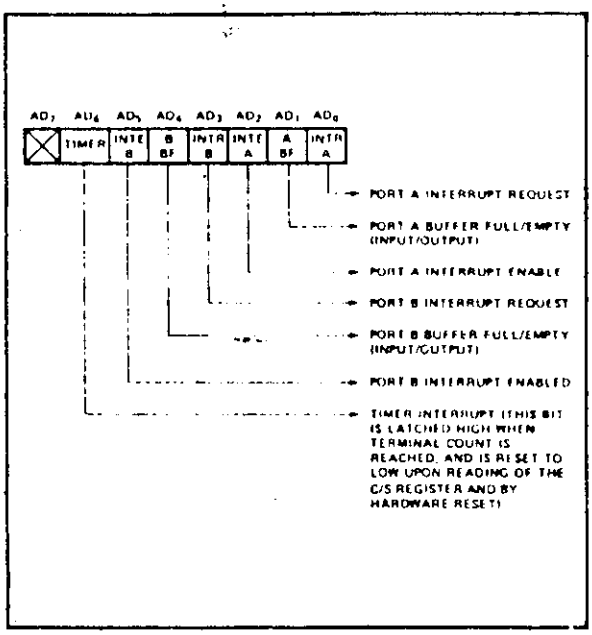


Figure 6. Status Register Bit Assignment

INPUT/OUTPUT SECTION

The I/O section of the 8155H/8156H consists of five registers: (See Figure 7.)

- **Command/Status Register (C/S)** — Both registers are assigned the address XXXXX000. The C/S address serves the dual purpose.

  When the C/S registers are selected during WRITE operation, a command is written into the command register. The contents of this register are *not* accessible through the pins

  When the C/S (XXXXX000) is selected during a READ operation, the status information of the I/O ports and the timer becomes available on the AD_{0-7} lines

- **PA Register** — This register can be programmed to be either input or output ports depending on the status of the contents of the C/S Register. Also depending on the command, this port can operate in either the basic mode or the strobed mode (See timing diagram). The I/O pins assigned in relation to this register are PA_{0-7}. The address of this register is XXXXX001.

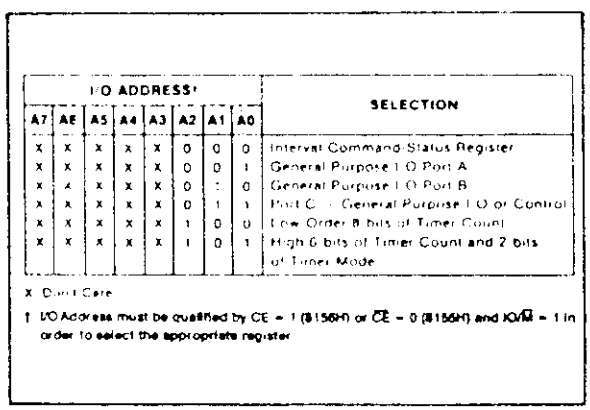
- **PB Register** — This register functions the same as PA Register. The I/O pins assigned are PB_{0-7}. The address of this register is XXXXX010

- **PC Register** — This register has the address XXXXX011 and contains only 6 bits. The 6 bits can be programmed to be either input ports, output ports or as control signals for PA and PB by properly programming the AD_2 and AD_3 bits of the C/S register.

  When PC_{0-5} is used as a control port, 3 bits are assigned for Port A and 3 for Port B. The first bit is an interrupt that the 8155H sends out. The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode. (See Table 2.)

When the 'C' port is programmed to either ALT3 or ALT4, the control signals for PA and PB are initialized as follows:

CONTROL	INPUT MODE	OUTPUT MODE
BF	Low	Low
INTR	Low	High
STB	Input Control	Input Control



I/O ADDRESS†								SELECTION
A7	A6	A5	A4	A3	A2	A1	A0	
X	X	X	X	X	0	0	0	Interval Command/Status Register
X	X	X	X	X	0	0	1	General Purpose I/O Port A
X	X	X	X	X	0	1	0	General Purpose I/O Port B
X	X	X	X	X	0	1	1	Port C — General Purpose I/O or Control
X	X	X	X	X	1	0	0	Low Order 8 bits of Timer Count
X	X	X	X	X	1	0	1	High 6 bits of Timer Count and 2 bits of Timer Mode

X Don't Care

† I/O Address must be qualified by CE = 1 (8156H) or $\overline{CE}$ = 0 (8156H) and IO/$\overline{M}$ = 1 in order to select the appropriate register

Figure 7. I/O Port and Timer Addressing Scheme

Figure 8 shows how I/O PORTS A and B are structured within the 8155H and 8156H:

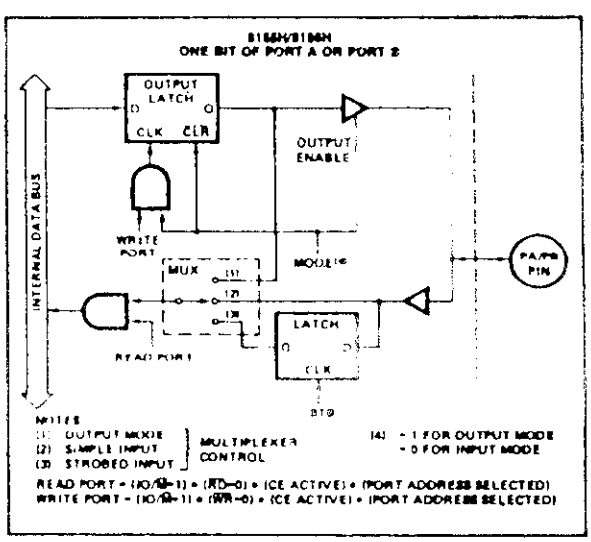


Figure 8. 8155H/8156H Port Functions

Bits 6-7 (TM_2 and TM_1) of command register contents are used to start and stop the counter. There are four commands to choose from:

TM_2	TM_1	
0	0	NOP — Do not affect counter operation.
0	1	STOP — NOP if timer has not started; stop counting if the timer is running.
1	0	STOP AFTER TC — Stop immediately after present TC is reached (NOP if timer has not started).
1	1	START — Load mode and CNT length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and CNT length immediately after present TC is reached.

Note that while the counter is counting, you may load a new count and mode into the count length registers. Before the new count and mode will be used by the counter, you must issue a START command to the counter. This applies even though you may only want to change the count and use the previous mode.

In case of an odd-numbered count, the first half-cycle of the squarewave output, which is high, is one count longer than the second (low) half-cycle, as shown in Figure 12.

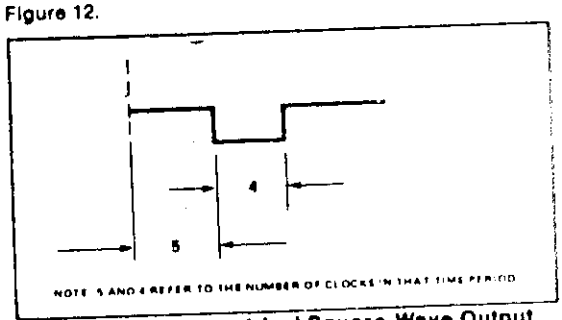


Figure 12. Asymmetrical Square-Wave Output Resulting from Count of 9

The counter in the 8155H is not initialized to any particular mode or count when hardware RESET occurs, but RESET does *stop* the counting. Therefore, counting cannot begin following RESET until a START command is issued via the C/S register.

Please note that the timer circuit on the 8155H/8156H chip is designed to be a square-wave timer, not an event counter. To achieve this, it counts down by twos twice in completing one cycle. Thus, its registers do not contain values directly representing the number of TIMER IN pulses received. You cannot load an initial value of 1 into the count register and cause the timer to operate, as its terminal count value is 10 (binary) or 2 (decimal). (For the detection of single pulses, it is suggested that one of the hardware interrupt pins on the 8085AH be used.) After the timer has started counting down, the values residing in the count registers can be used to calculate the actual number of TIMER IN pulses required to complete the timer cycle if desired. To obtain the remaining count, perform the following operations in order:

1. Stop the count
2. Read in the 16-bit value from the count length registers
3. Reset the upper two mode bits
4. Reset the carry and rotate right one position all 16 bits through carry
5. If carry is set, add 1/2 of the full original count (1/2 full count — 1 if full count is odd).

Note: If you started with an odd count and you read the count length register before the third count pulse occurs, you will not be able to discern whether one or two counts has occurred. Regardless of this, the 8155H/56H always counts out the right number of pulses in generating the $\overline{\text{TIMER OUT}}$ waveforms.

8085A MINIMUM SYSTEM CONFIGURATION

Figure 13a shows a minimum system using three chips, containing:

- 256 Bytes RAM
- 2K Bytes ROM
- 38 I/O Pins
- 1 Interval Timer
- 4 Interrupt Levels

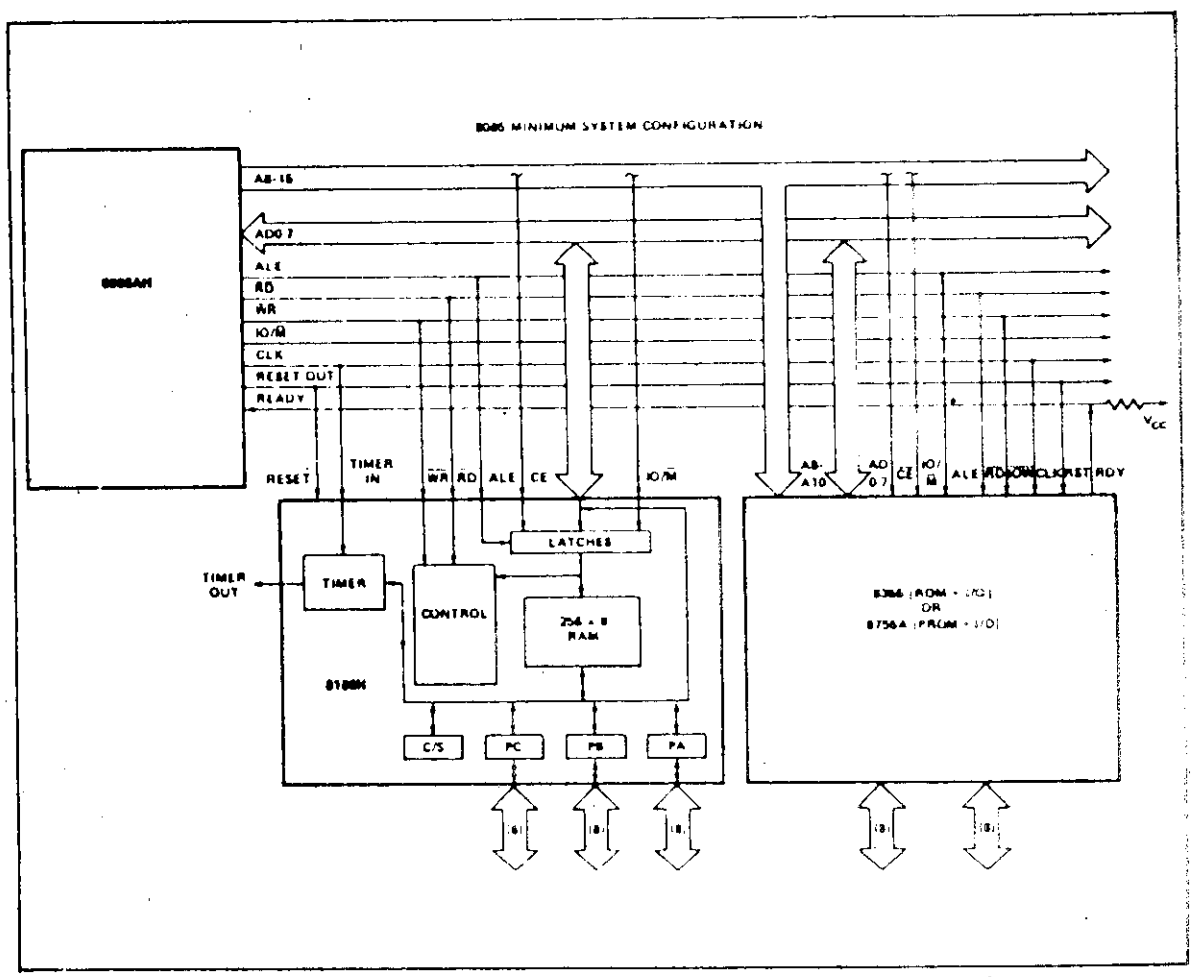


Figure 13a. 8085AH Minimum System Configuration (Memory Mapped I/O)

8088 FIVE CHIP SYSTEM

Figure 13b shows a five chip system containing:

- 1.25K Bytes RAM
- 2K Bytes ROM
- 38 I/O Pins
- 1 Interval Timer
- 2 Interrupt Levels

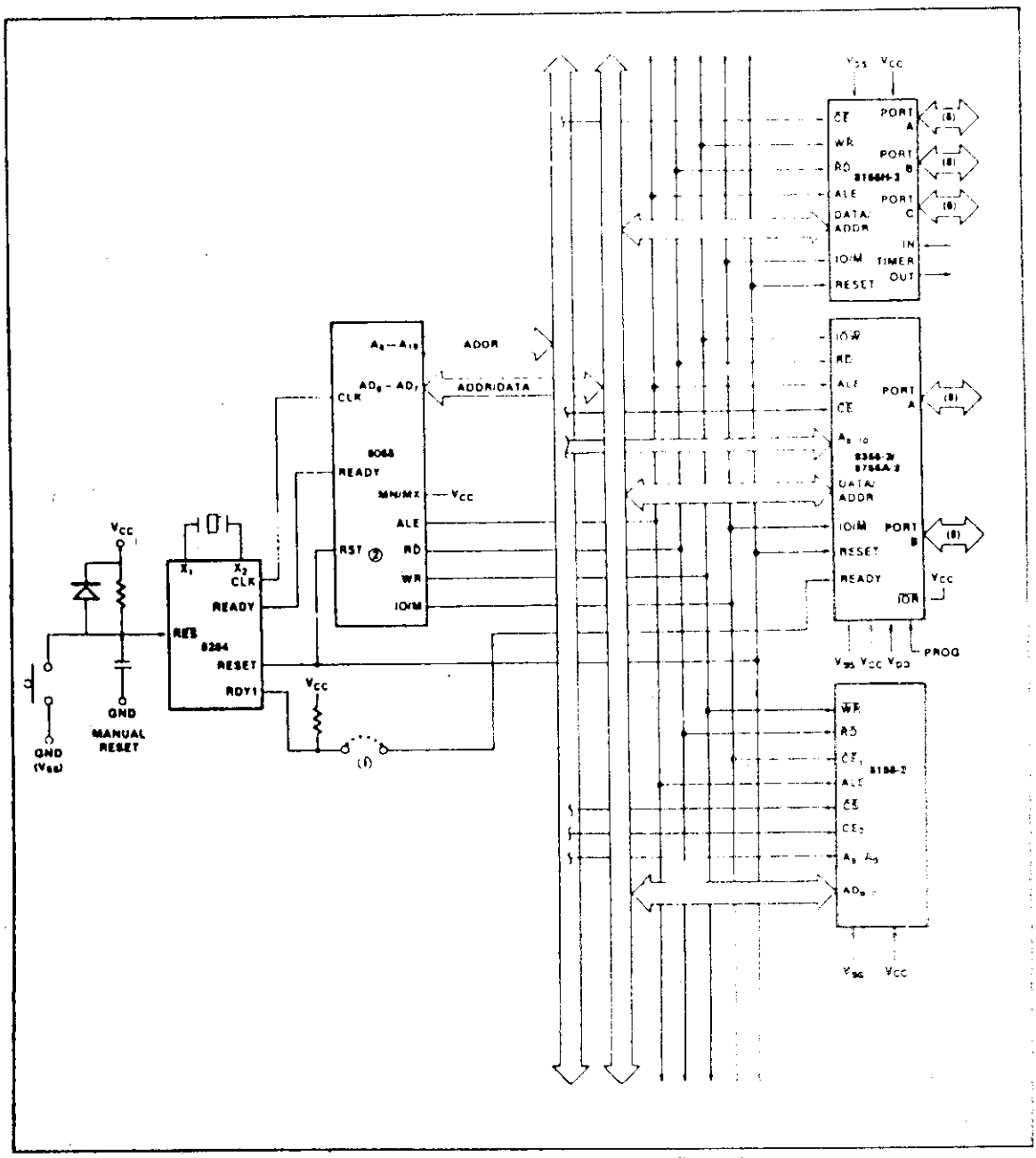


Figure 13b. 8088 Five Chip System Configuration

intel

2732
32K (4K x 8) UV ERASABLE PROM

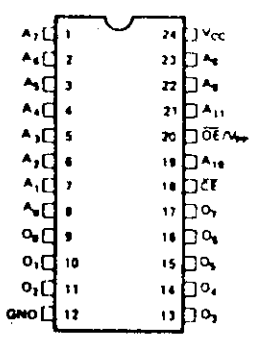
- **Fast Access Time:**
  - **— 450 ns Max. 2732**
  - **— 550 ns Max. 2732-6**
- **Single +5V ± 5% Power Supply**
- **Output Enable for MCS-85™ and MCS-86™ Compatibility**
- **Low Power Dissipation:**
  150mA Max. Active Current
  30mA Max. Standby Current
- **Pin Compatible to Intel® 2716 EPROM**
- **Completely Static**
- **Simple Programming Requirements**
  - **— Single Location Programming**
  - **— Programs with One 50ms Pulse**
- **Three-State Output for Direct Bus Interface**

The Intel® 2732 is a 32,768-bit ultraviolet erasable and electrically programmable read only memory (EPROM). The 2732 operates from a single 5-volt power supply, has a standby mode, and features an output enable control. The total programming time for all bits is three and a half minutes. All these features make designing with the 2732 in microcomputer systems faster, easier, and more economical.

An important 2732 feature is the separate output control, Output Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems. Intel's Application Note AP-72 describes the microprocessor system implementation of the $\overline{OE}$ and $\overline{CE}$ controls on Intel's 2716 and 2732 EPROMs. AP-72 is available from Intel's Literature Department.

The 2732 has a standby mode which reduces the power dissipation without increasing access time. The maximum active current is 150mA, while the maximum standby current is only 30mA, an 80% savings. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input.

PIN CONFIGURATION



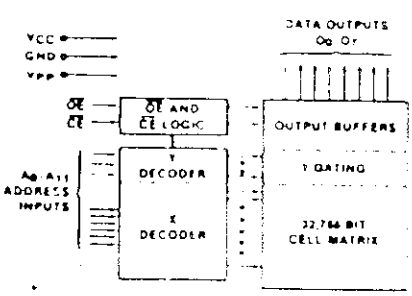
PIN NAMES

A_0-A_{11}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS

MODE SELECTION

MODE \ PINS	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	OUTPUTS (9-11,13-17)
Read	V_{IL}	V_{IL}	+5	O_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	O_{OUT}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

BLOCK DIAGRAM

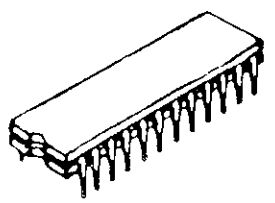


2048-word×8-bit High Speed Static CMOS RAM

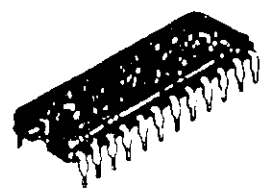
■FEATURES

- Single 5V Supply and High Density 24 Pin Package
- High speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation Standby: 100μW (typ.) Operation: 180mW (typ.)
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

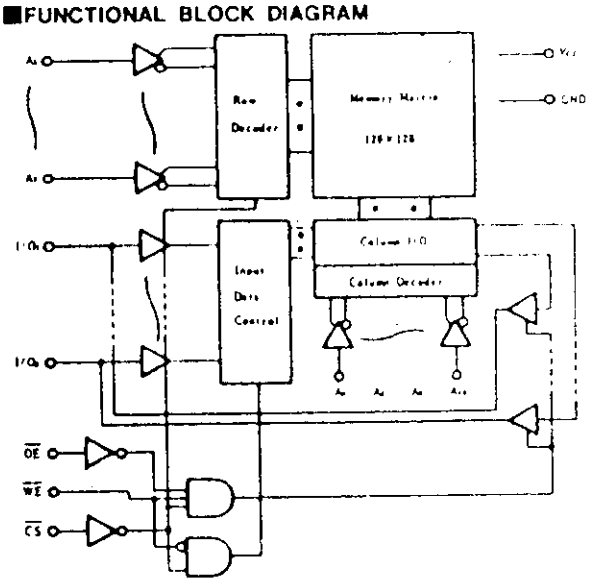
HM6116-2, HM6116-3, HM6116-4



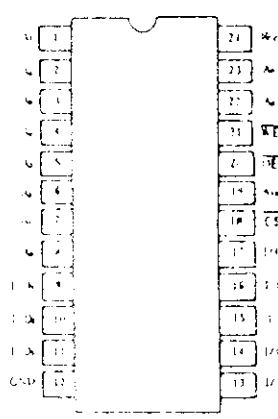
HM6116P-2, HM6116P-3, HM6116P-4



■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	−0.5* to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (Plastic)	T_{stg}	−55 to +125	°C
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

* Pulse Width 50ns: −1.5 V

■TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

74150
Multiplexer

16-Input Multiplexer
Product Specification

Logic Products

FEATURES

- **Select data from 16 sources**
- **Demultiplexing capability**
- **Active-LOW enable or strobe**
- **Inverting data output**

DESCRIPTION

The '150 is a logical implementation of a single-pole, 16-position switch with the switch position controlled by the state of four Select inputs. S_0, S_1, S_2, S_3. The Multiplexer output ($\overline{Y}$) inverts the selected data. The Enable input ($\overline{E}$) is active-LOW. When $\overline{E}$ is HIGH the $\overline{Y}$ output is HIGH regardless of all other inputs. In one package the '150 provides the ability to select from 16 sources of data or control information.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74150	17ns	40mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74150N

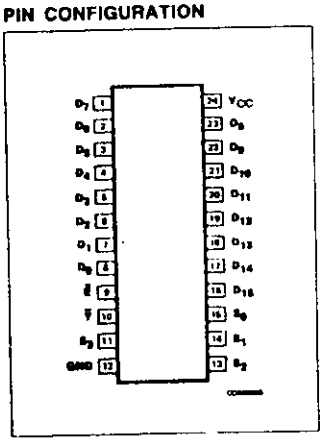
NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

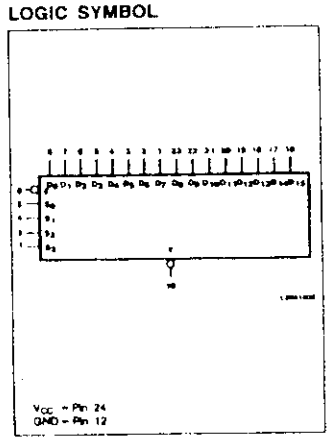
PINS	DESCRIPTION	74
All	Inputs	1ul
$\overline{Y}$	Output	10ul

NOTE
A 74 unit load (ul) is understood to be 40µA I_{IH} and −1.6mA I_{IL}

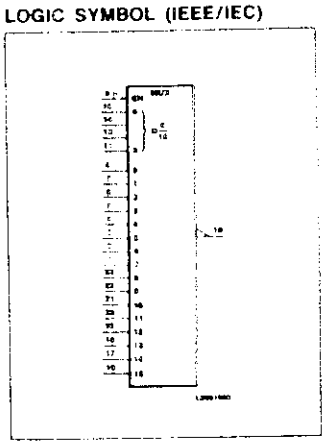
PIN CONFIGURATION



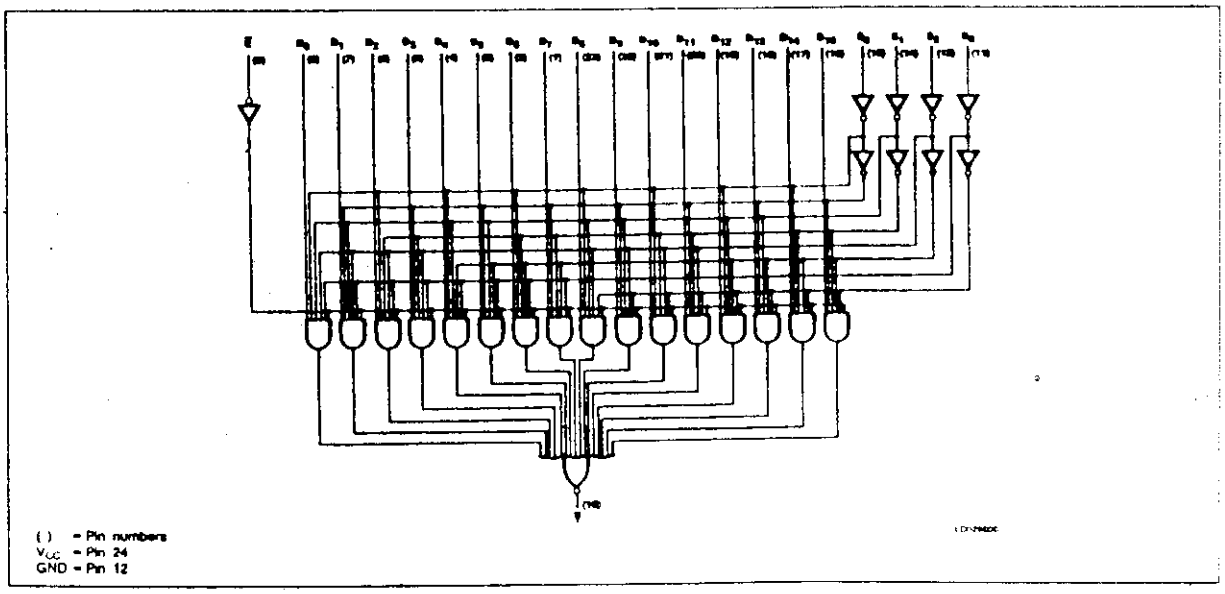
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS																		OUTPUT
S_3	S_2	S_1	S_0	$\overline{E}$	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}	$\overline{Y}$
X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	L	L	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	L	H	L	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	H	L	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	H	L	L	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	H	L	L	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	H	H	L	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	H	H	L	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	L
L	H	L	L	L	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	H
L	H	L	L	L	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	L
L	H	L	H	L	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	H
L	H	L	H	L	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	L
L	H	H	L	L	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	H
L	H	H	L	L	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	L
L	H	H	H	L	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	H
L	H	H	H	L	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	L
H	L	L	L	L	X	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	H
H	L	L	L	L	X	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	L
H	L	L	H	L	X	X	X	X	X	X	X	X	X	L	X	X	X	X	X	X	H
H	L	L	H	L	X	X	X	X	X	X	X	X	X	H	X	X	X	X	X	X	L
H	L	H	L	L	X	X	X	X	X	X	X	X	X	X	L	X	X	X	X	X	H
H	L	H	L	L	X	X	X	X	X	X	X	X	X	X	H	X	X	X	X	X	L
H	L	H	H	L	X	X	X	X	X	X	X	X	X	X	X	L	X	X	X	X	H
H	L	H	H	L	X	X	X	X	X	X	X	X	X	X	X	H	X	X	X	X	L
H	H	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	X	H
H	H	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	H	X	X	X	L
H	H	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	H
H	H	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	H	X	X	L
H	H	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	H
H	H	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	X	L
H	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	H
H	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

SCL4511B

CMOS BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

FEATURES

- High-Current Sourcing Bipolar Outputs (Up to 25 mA)
- Latched Storage of Input Code
- Blanking Input for Display Intensity Modulation
- Lamp Test Provision
- Readout Blanking for Illegal Input Combinations

DESCRIPTION

The SCL4511B provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability to source up to 25 mA of current. Lamp Test, Blanking, and Latch Enable inputs are used to test the display, turn off the display, and store a BCD code, respectively. It can be used with LED, incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include counter display drivers, seven-segment decimal display, and various clock, watch, and timer uses.

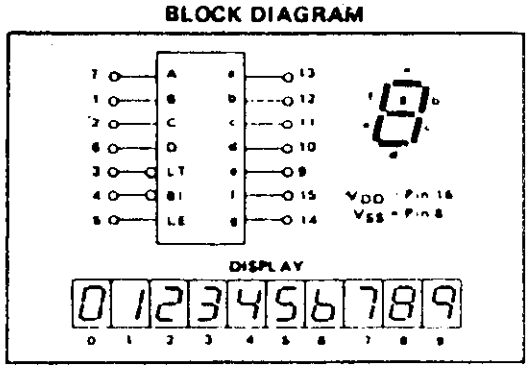
TRUTH TABLE

LE	BI	LT	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X				*				*

X = Don't care

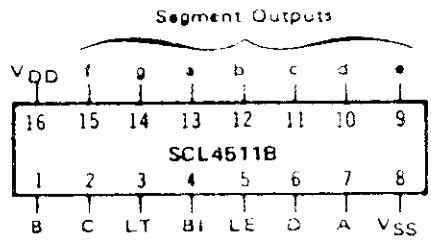
* Depends upon the BCD code applied during the 0 to 1 transition of LE

BLOCK DIAGRAM



CONNECTION DIAGRAM

(all packages)



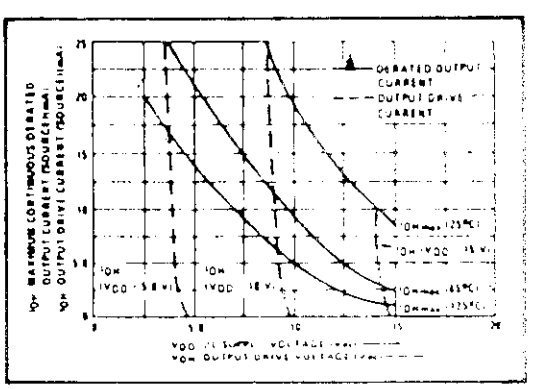
Add suffix for package:

- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C



Typical P-Channel Source Current Characteristics

The maximum continuous (worst case) derated output drive current applies to a single output with all other outputs sourcing an equal amount of current. Operation above the derating curve at a given temperature is not recommended.

74LS373, 74LS374, S373, S374
Latches/Flip-Flops

'373 Octal Transparent Latch With 3-State Outputs
'374 Octal D Flip-Flop With 3-State Outputs
Product Specification

Logic Products

FEATURES
- **8-bit transparent latch — '373**
- **8-bit positive, edge-triggered register — '374**
- **3-State output buffers**
- **Common 3-State Output Enable**
- **Independent register and 3-State buffer operation**

DESCRIPTION
The '373 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable ($\overline{OE}$) control gates.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS373	19ns	24mA
74S373	10ns	135mA
74LS374	19ns	27mA
74S374	8ns	116mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74LS373N, N74S373N, N74LS374N, N74S374N
Plastic SOL-20	N74LS373D, N74S373D, N74LS374D, N74S374D

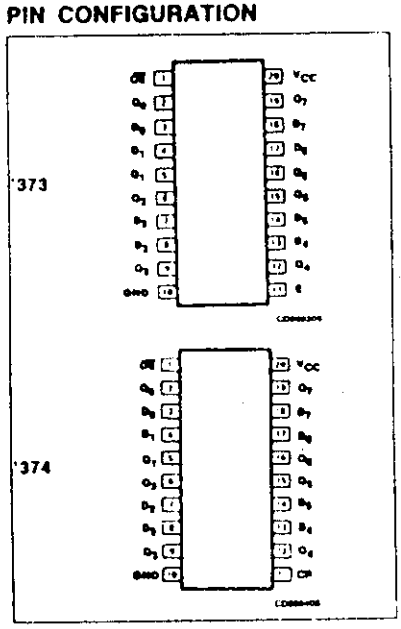
NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

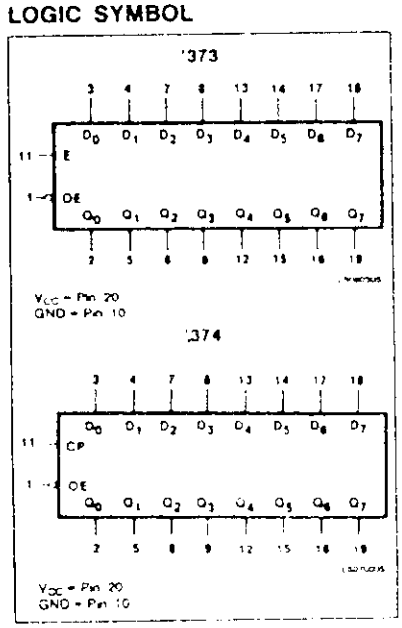
PINS	DESCRIPTION	74S	74LS
All	Inputs	1Sul	1LSul
All	Outputs	10Sul	30LSul

NOTE:
Where a 74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and a 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

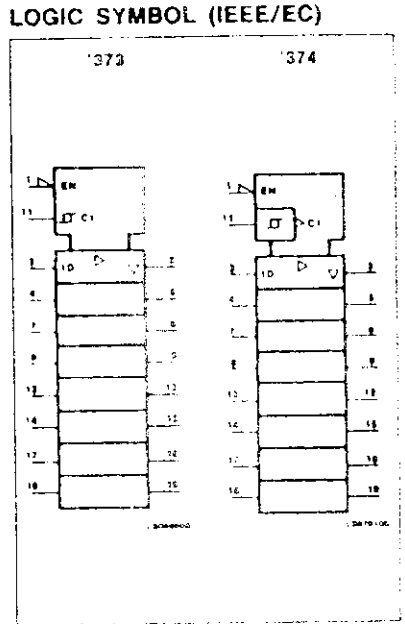
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/EC)



Latches/Flip-Flops

74LS373, 74LS374, S373, S374

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one set-up time before the HIGH-to-LOW enable transition. The enable gate has hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

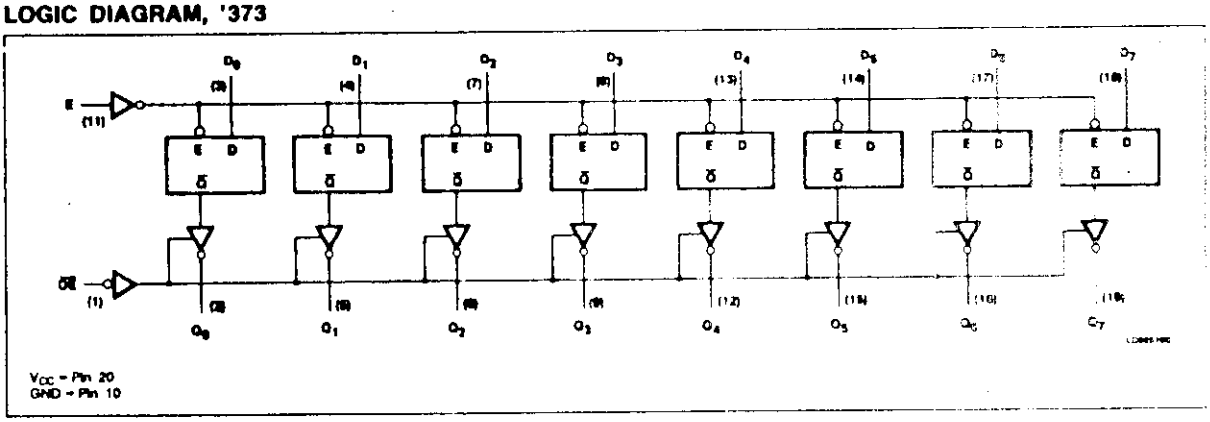
The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is LOW, the latched or transparent data appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

The '374 is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

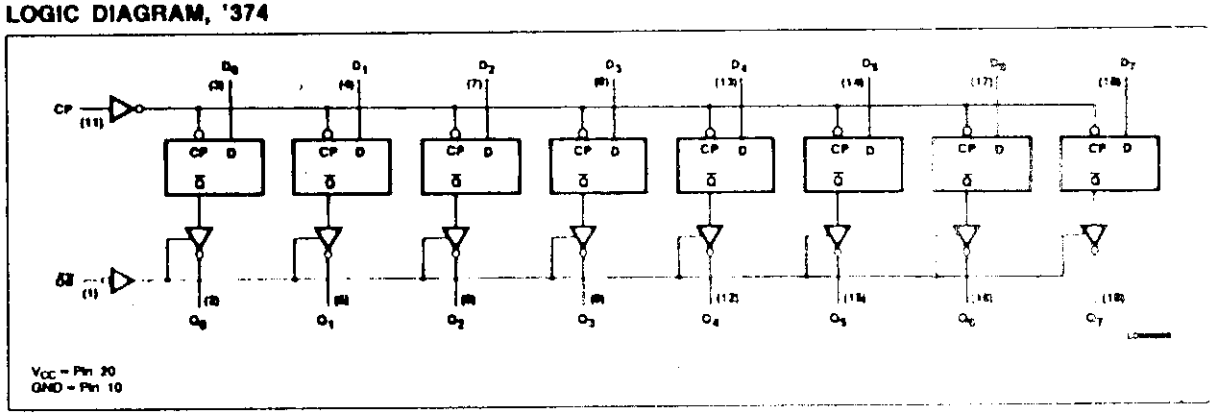
The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The clock buffer has hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is LOW, the data in the register appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, '373



LOGIC DIAGRAM, '374



MODE SELECT — FUNCTION TABLE '373

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		$Q_0 - Q_7$
Enable and read register	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	(Z)
	H	L	h	H	(Z)

74LS138, S138
Decoders/Demultiplexers

1-Of-8 Decoder/Demultiplexer
Product Specification

Logic Products

FEATURES
- **Demultiplexing capability**
- **Multiple input enable for easy expansion**
- **Ideal for memory chip select decoding**
- **Direct replacement for Intel 3205**

DESCRIPTION
The '138 decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled, provides eight mutually exclusive, active LOW outputs ($\overline{0}-\overline{7}$). The device features three Enable inputs: two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). Every output will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four '138s and one invertor.

The device can be used as an eight output demultiplexer by using one of the active LOW Enable inputs as the Data input and the remaining Enable inputs as strobes. Enable inputs not used must be permanently tied to their appropriate active HIGH or active LOW state.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS138	20ns	6.3mA
74S138	7ns	49mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74S138N, N74LS138N
Plastic SO	N74LS138D, N74S138D

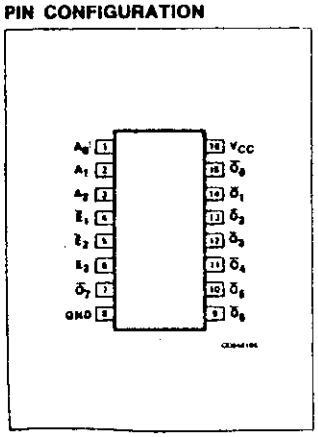
NOTE:
For information regarding devices processed to Military Specifications see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

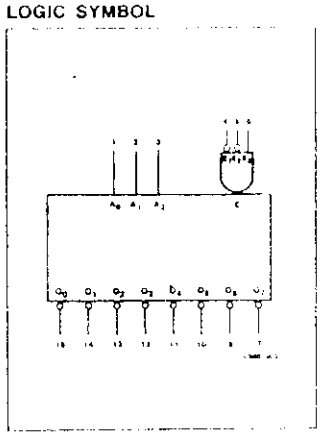
PINS	DESCRIPTION	74S	74LS
All	Inputs	1.0 U.L.	1.0 U.L.
All	Outputs	100 U.L.	10 U.L.

NOTE:
Where a 74S unit load (U.L.) is 50μA I_{IH} and −2.0mA I_{IL}, and a 74LS unit load (U.L.) is 20μA I_{IH} and −0.4mA I_{IL}.

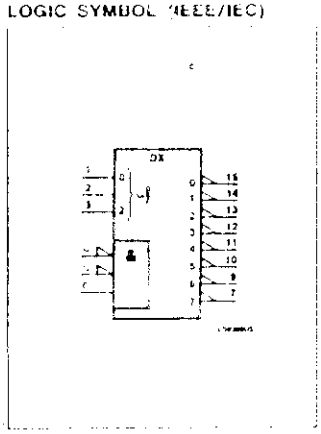
PIN CONFIGURATION



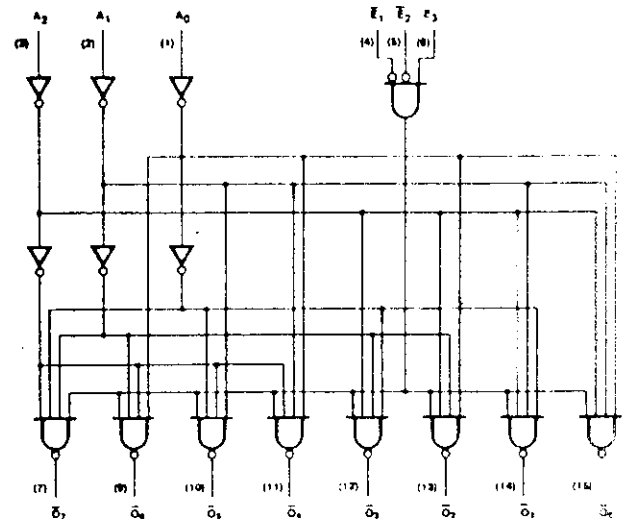
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



( ) = Pin number
V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

7404, LS04, S04
Inverters

Hex Inverter
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7404	10ns	12mA
74LS04	9.5ns	2.4mA
74S04	3ns	22mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N7404N, N74LS04N, N74S04N
Plastic SO	N74LS04D, N74S04D

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

FUNCTION TABLE

INPUT	OUTPUT
A	Y
L	H
H	L

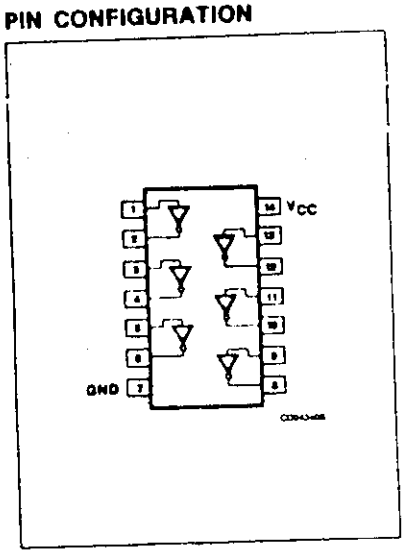
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

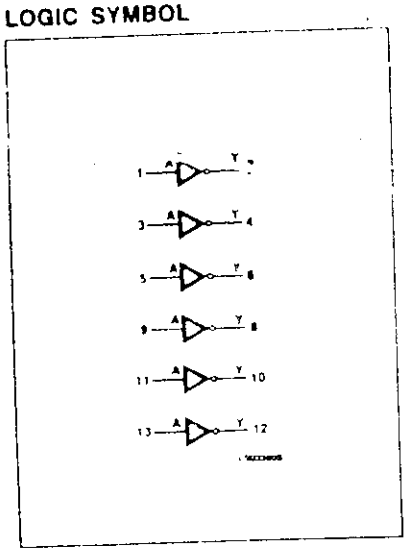
PINS	DESCRIPTION	74	74S	74LS
A	Input	1ul	1Sul	1LSul
Y	Output	10u	10Sul	10LSul

NOTE:
Where a 74 unit load (ul) is understood to be 40µA I_{IH} and −1.6mA I_{IL}, a 74S unit load (Sul) is 50µA I_{IH} and −2.0mA I_{IL}, and 74LS unit load (LSul) is 20µA I_{IH} and −0.4mA I_{IL}.

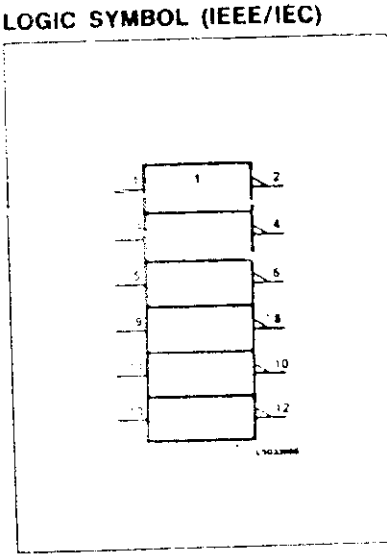
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



In addition to the standard application of multiplexers in data conversion techniques, these circuits can also be used in generating logic

select inputs as the first three variables, any combination of A, B, and C will select a data input (assuming the output is enabled). For each combi-