# Microprocessor Based Rotor Analyser for Universal Motors

## Project Report



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## CERTIFICATE

This is to certify that the report entitled

**Microprocessor Based Rotor Analyser for Universal Motors**

has been submitted by

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In partial fulfilment for the award of

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during the academic year 1992-93

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Guide Head of the Department

Certified that the candidate was examined by us in the Project work Viva-Voce Examination held on _____ and the University Register Number was _____

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Internal Examiner External Examiner

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## SYNOPSIS

This project aims at testing the rotor automatically (universal motor's) during the course of production. The testing of rotors presently employed is cumbersome and time consuming and hence a completely automatic machine is developed. The rotor to be tested is placed and the output analog signal is processed and the display is made. The company at present tests the rotor manually which takes more time and the new machine proves to be useful interms of money and time. The project can be extended by interfacing the system to computer for assembly line production.

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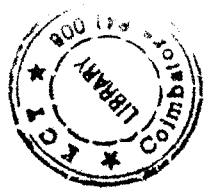



# INTRODUCTION

Automation of the industry at all levels is as important as its existence. The various parts of prime movers that are used should undergo testing before they are assembled into units for consumption.

Conventional methods are used in most industries to test the various parts of motors. The conventional methods turn out to be cumbersome and time consuming which inturn will affect productivity and economy. With the advent of digital electronic, integrated circuits and computers, "Automatic Testing Machines" can be made which are highly reliable, more precise and fast responding.

The microprocessor based rotor analyser developed can be used to test the rotor for faults, such as inter-turn short, welding resistance, coil resistance etc. The rotor to be tested is placed, by transformer principle a field is generated and the rotor excited. The 24 analog signals obtained from the commutator are given to a system where the data is being processed. The fault is verified from the LED display.

# 1. UNIVERSAL MOTORS

## 1.1 INTRODUCTION

With its ability to operate on ac or on dc over a wide range of frequencies, the universal motor is an essential part of much domestic and industrial equipment.

Their characteristics make them suitable for many domestic appliance application and while dc supplies are becoming fewer, these motors can be used over a wide range of frequencies on ac supplies.

They are an essential part of equipment, both domestic and industrial, with a production worth millions a year in every country.

## 1.2 GENERAL ASPECTS

The universal motor is characterized by its ability to operate with substantially the same performance on direct as well as alternating currents of frequency up to 60 Hz. It develops more horsepower than other ac motors, principally because of its high speed.

These motors are series wound and have series characteristics on both ac and dc.

No load speeds are high some times well over 20,000 rpm but the armatures are designed so that they will not be damaged at these speeds.

They are usually designed for full load operating speeds of 4,000 to 16,000 rpm in large horse power ratings and upto 20,000 or more in smaller power ratings.

The universal motor is at its best as a high speed machine ie. when running at about three times synchronous speed when the power factor is near to unity and the performance is similar on both ac and dc supplies.

Depending on the windings universal motors are classified into two types.

1. Compensated
2. Non compensated

The first type has now all but disappeared, the non compensated is usually built with concentrated or salient poles. The non compensated motor is less expensive and simpler in construction.

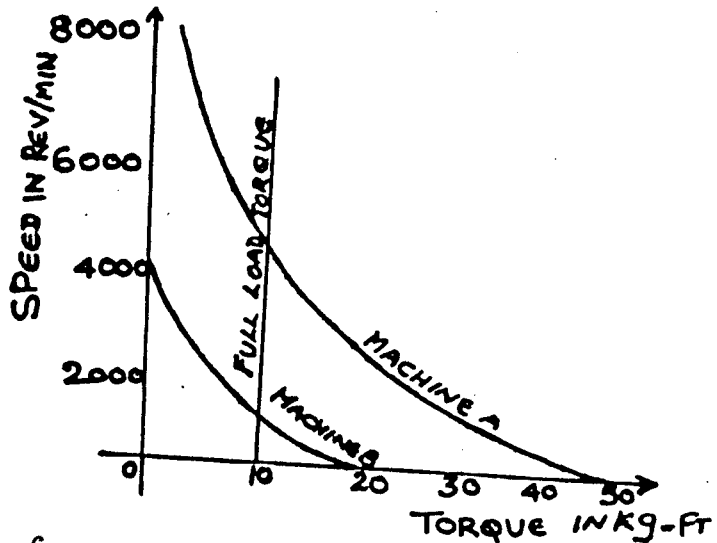



fig 2.1. SPEED-TORQUE CURVES FOR

(i) MACHINE A

10kg - 5,000 rev/min

(ii) MACHINE B

10kg - 1,000 rev/min

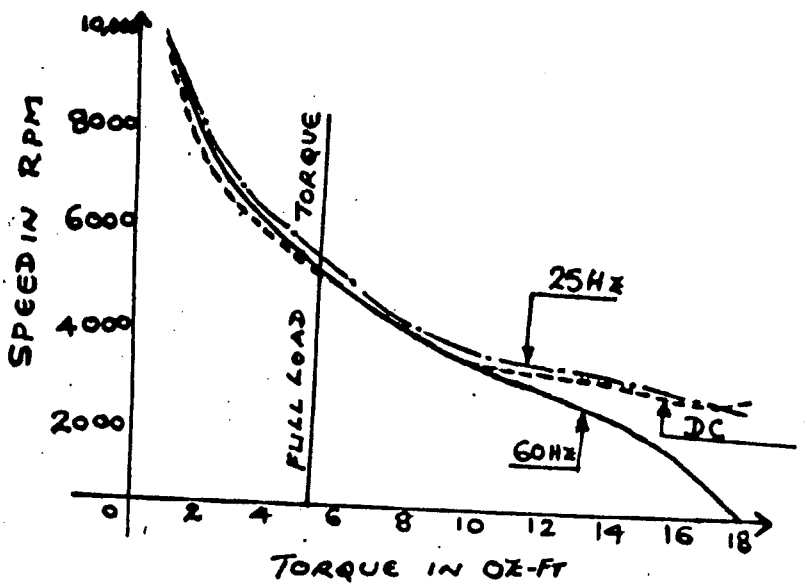



fig 2.2 speed torque curves for a compensated motors

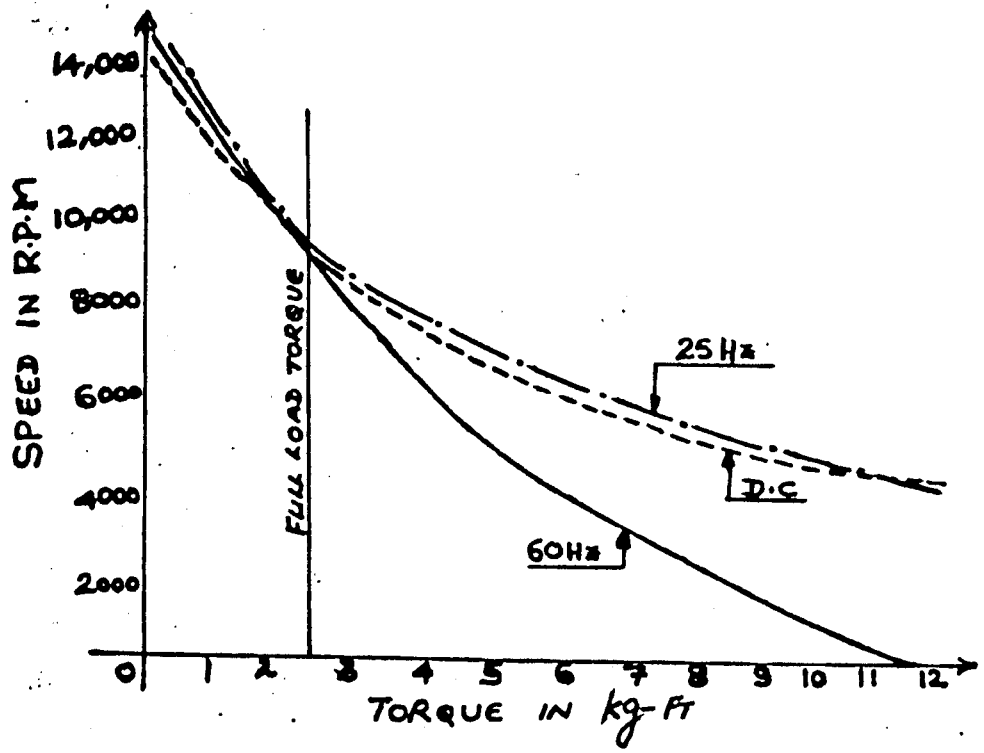



fig 2.3 Speed torque curves of a non compensated universal motors rated at 1/4 LP and 8,000 rpm.

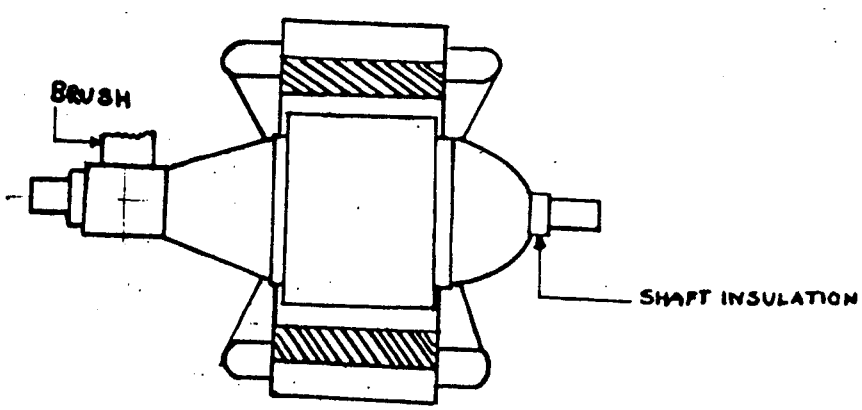



fig 2.4 CROSSECTIONAL VIEW OF UNIVERSAL MOTOR.

It is to be noted that with either type; the speed drops off rapidly with an increase in load and increase with decrease in load.

The difficulty in the low speeds is due to the rapid drop in torque/speed characteristic resulting from the highly inductive winding required for low speed working as both field and armature have a large number of turns. From the speed torque characteristics, it is noticed that only a slight increase in load can cause a large fall in speed.

Please to be noted that the compensated universal motor has better universal characteristics.

No industry wide standards of horse power and speed ratings have been established for universal motors, because these motors are often sold as sets of parts, because the choice of possible full load operating speed is virtually unlimited and most of their applications are specialized.

## 1.3 CONSTRUCTIONAL FEATURES

In general universal motors consist of three parts.

1. Stator
2. Rotor
3. Brushes

## STATOR

The stator consist of field windings according to the application. In case of mixie it consists of two poles. There is a difference in the stator punching and that of the complete wound stator of the non compensated to that of the compensated. The compensated stator looks very much like that of for a two pole induction motor. In some of the application the speed of the motor is varied by using one set of windings of the stator. This is done by properly tapping them at calculated or desired speed levels.

The stator for the field system, through having salient poles, must be built of laminations to suit alternating flux conditions. Many of these stators are now suitable for machine winding of the field coils and this must be borne in mind when shaping the pole shanks.

## ROTORS

As commutation is one of the most difficult aspects of this type of motor, every effort must be directed to making conditions as easy as possible. To do this the number of turns per coil under commutation is made as small as possible, which means having a large number of segments.

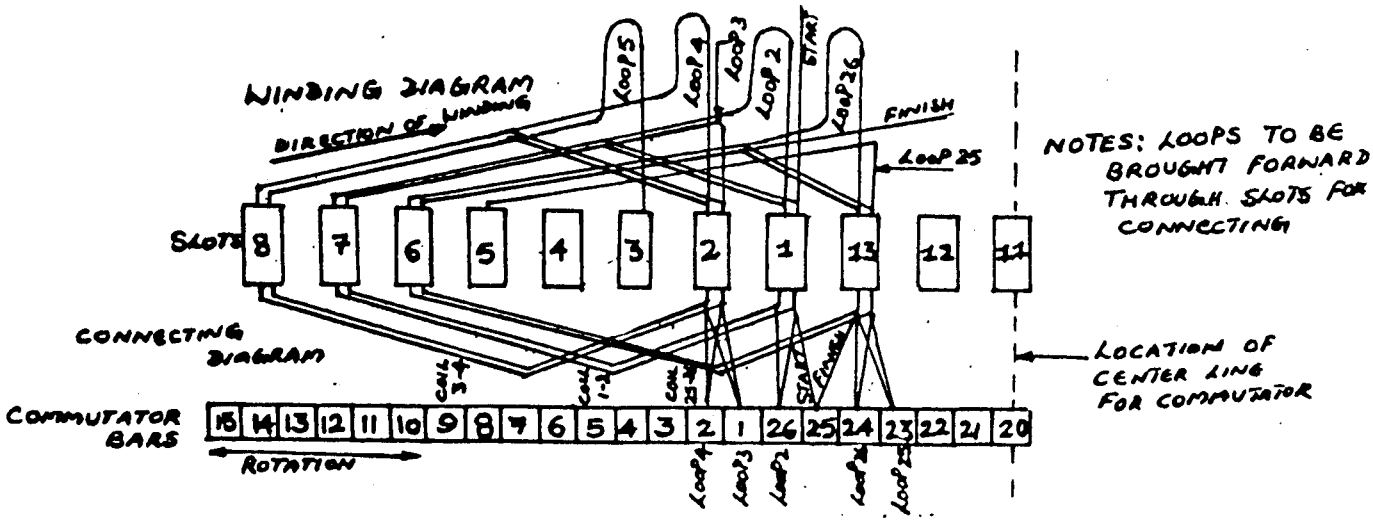



fig 2.5. ARMATURE WINDING

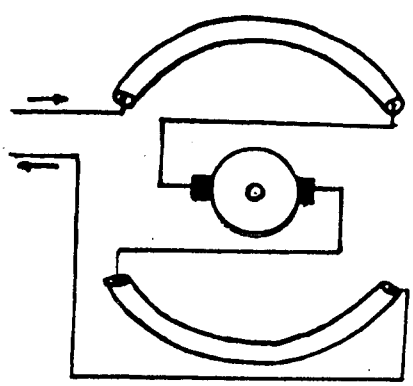


fig 2.6(a) CONNECTION DIAGRAM SHOWING BRUSH-HOLDER CONNECTIONS

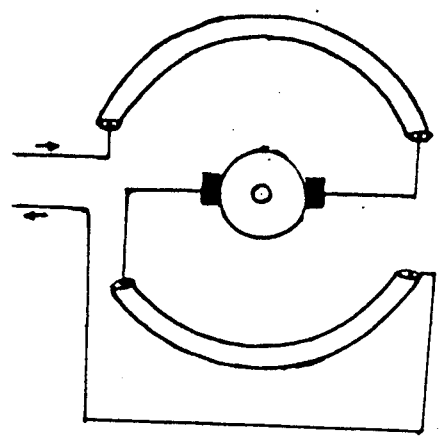


fig 2.6(b) BRUSH-HOLDER CONNECTIONS REVERSED

The design of the armature is similar to a normal dc type. The armature core stampings are usually assembled so that the slots are skewed about 1 slot pitch. This tends to reduce the variation of reluctance of the main flux circuit through the armature and reduces noise which could easily be caused by sudden changes of magnetic flux.

Universal motors are wound for two poles, the winding share the same as the windings used in dc motor. The two types are winding are:

a. Front lead windings
b. Back lead windings

a) FRONT LEAD WINDING

In front lead windings, the commutator connections from the armature coils are brought out in front of the armature ie, on the commutator side of the laminations.

Roughly speaking there are three main types of connections.

i) On Centre
ii) Thrown left
iii) Thrown right

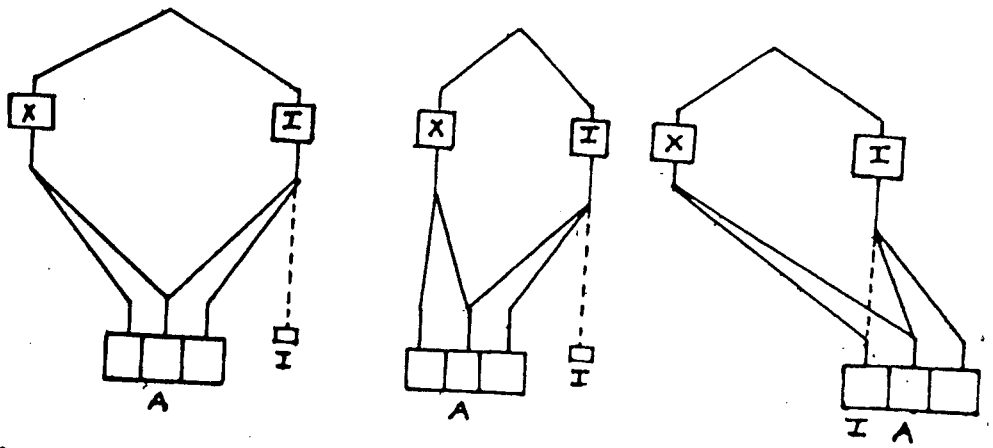



fig 2·7 (a) ON CENTRE (b) THROWN LEFT (c) THROWN RIGHT

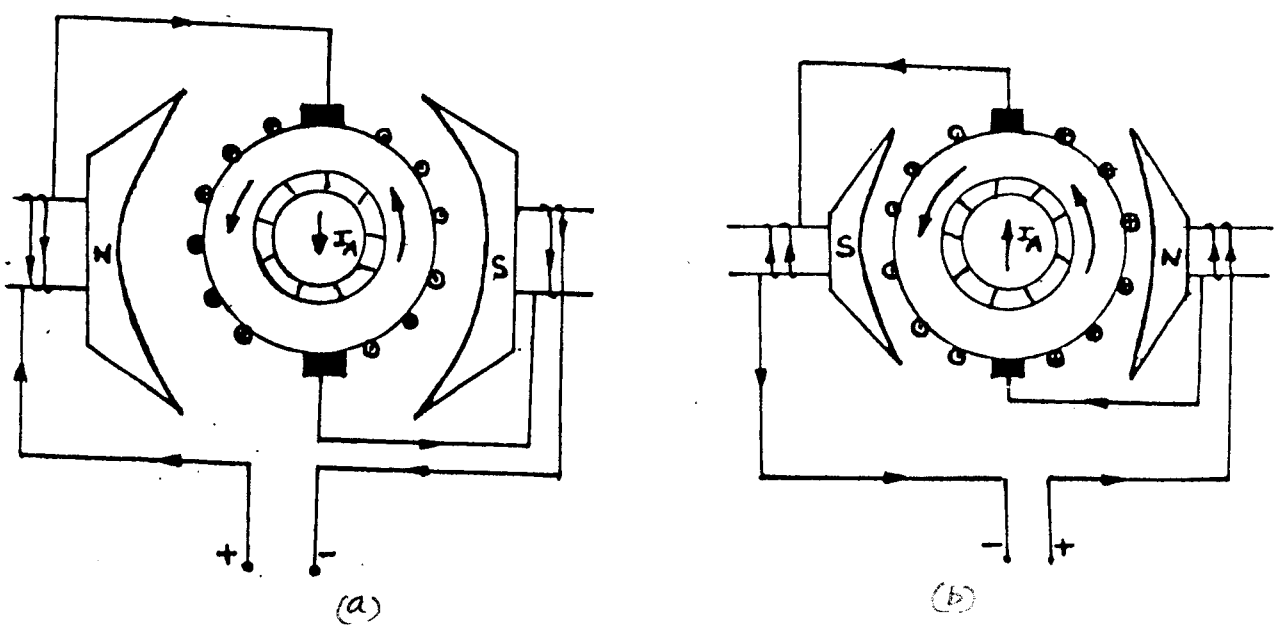



fig 2·8. UNI-DIRECTIONAL TORQUE PRODUCTION

When the connections are either thrown left and thrown right the neutral position for the brushes falls between the poles. When the connections are 'on Centre', the brushes will fall opposite the centres of the poles.

b) BACK-LEAD WINDINGS

In back lead windings, the wires is started at the back of the armature and all commutator connections are brought out at the end.

3) BRUSHES

Brushes are used to collect the current from the armature coil through the commutator.

The section should be chosen bearing in mind the full current in the brush due to theinput current and the commutating current.

The width of the brush should be such that commutation does not take place while the coil is under the pole. The brush width is narrow on this type of machine and although it reduces the time of commutation and hence keeps the reactance voltage up on that account.

As these machines usually rotate at fairly high speeds and brushes require 6 lb per sq.inch or so pressure, there should not be high coefficient of friction between brush and commutator over heating may occur.

The stator and brush-holder connections of a simple too lead non reversible concentrated pole non compensated universal motor is given in figure.

It should be noted that the brushes are located half way between the centres of stator coils. When the brushes are so located, the connections from the armature coils to the commutator cannot be connected on centre but they must be either thrown left or thrown right.

The excellance of the carbon brush manufacturers product is a big factor in the success of universal motors careful selection of the right brush for the job is most essential.

With undercut micas noise can be a nuisance and in many cases flush micas are used, but again care is required as micas must wear with copper or they will become proud, causing destructive sparking from a bouncing brush. The brush must, in these conditions, be capable of wearing down the mica.

## 1.4 PRINCIPLE OF OPERATION

Regardless of whether they operate on dc or ac supply, series motors developed unidirection torque. However the torque developed for ac supply is not of constant magnitude but pulsates between zero to maximum value each half cycle.

The production of unidirectional torque when the motor runs on ac supply is easily understood from the figure.

As the figure shows, the armature conductors under north pole current downwards and those under south pole carry current upwards. By applying Fleming's left hand rule, the direction of force on each conductor is found. It is seen the each conductor experiences a force which tends to rotate the armature in the anticlockwise direction. These forces collectively produce a driving torque which sets the armature rotating. The principle is true for current in both directions, hence true for alternating current and direct current.

## 1.5 ADVANTAGES

Universal motors have three outstanding advantages.

1. It can be used on both dc and ac supplies of frequencies upto 60 Hz.
2. They can be made for operation at any speed within very limits.
3. They are suitable for a wide range of speed control.

## 1.6 APPLICATIONS

Very popular applications for universal motors are:

a. Food Mixers
b. Blenders
c. Vacuum cleaners
d. Portable drills
e. Saws
f. Sewing machines
g. Routers etc.

## 2.1 ROTOR SPECIFICATION

| MOTOR | TYPE |
|---|---|
| UNIVERSAL MOTOR | NON-COMPENSATED |

SPECIFICATION - ARMATURE

| | | |
|---|---|---|
| a) | No. of slots | 12 |
| b) | No. of Commutator segments | 24 |
| c) | No. of turns b/w two Commutator segments | 40 |
| d) | No. of lead wires from each slot | 02 |
| e) | No. of turns/slot | 160 |
| f) | Maximum speed | 17200 rpm |
| g) | Welding provided - Spot welding | |

STANDARD COMMUTATOR SEGMENT VOLTAGES WHEN STANDARD ARMATURE IS PLACED IN FIELD GENERATOR.

Input Voltage - 230 V

Input Current - 2 Amps

Reference Segment - 24

Voltage between reference segment and the other segments

| Commutator segment | Voltage |
|---|---|
| 1 | 3.5 V |
| 2 | 8 V |
| 3 | 12.5 V |
| 4 | 16.5 V |
| 5 | 1.9 V |
| 6 | 22 V |
| 7 | 22.5 V |
| 8 | 23 V |
| 9 | 21.5 V |
| 10 | 19.5 V |
| 11 | 15.7 V |
| 12 | 12.1 V |
| 13 | 7.5 V |
| 14 | 2.5 V |
| 15 | .5 V |

| Commutator segment | Voltage |
|---|---|
| 16 | 3.5 V |
| 17 | 5.5 V |
| 18 | 8 V |
| 19 | 8.5 V |
| 20 | 8.7 V |
| 21 | 7.1 V |
| 22 | 5.5 V |
| 23 | 2.5 V |

## 2.2 POSSIBLE FAULTS AND DETECTION

This paper has been prepared to assist in developing apprehensive test methods to the users of electrical equipment in industrial environments and thei r asociated repair facilities. Some of the information presented here is as old as the use of such equipment itself, and some is relatively new. It will benefit those most who wish to identify, clarify, and establish comprehensive test methods and preventive maintenance programs in their shops and plans.

### 1. INSULATION

Insultation, or the ability to isolate electrical conductors in an electric circuit, is that critical factor in the ability of the circuit or mechanism to function; yet it is often considered the weakest like in the chain which harnesses electricity as man's servant.

The fundamental properties of any given insulating material are dielectric strength, or the ability to withstand high voltages without breakdown; Ohmic resistance, or the ability to prevent leakage of small currents; and thermal conductivity, or the ability to dissipate electrical energy that is transformed into heat. The ideal insulator is one having the maximum dielectric strength and resistance, good ther mal conductivity, and also mechanical strength and chemical stability.

A. Dielectric Strength

The dielectric strength of an insulating material is usually expressed in terms of a voltage gradient, common units being volts per mil. volts per millimeter, and kilovolts per centimeter. The dielectric strength of an insulating material is that quality of the material to resist high voltage puncture or rupture, not only at normal operating levels, but also as might occur in a power surge. Once a high voltage puncture or rupture has occurred in an insulation system, the dielectric strength of the insulating system may be completely destroyed of severely reduced, depending upon the severity of the rupture.

B. Insulation Resistance

The insulation resistance of an insulating material is usualy expressed in megohms (M$\Omega$.10ohms) per centimeter, and is proportional to the thickness of the material and inversely proportional to the area under rest. Insulation resistance is the quality of an insulating material that prevents the leakage of current through the material and creeppage of current among the surface of the material when subject to a direct voltage.

Insulation resistance and dielectric strength are two fundamental and distinct properties of insulation and no dintinct relationship between then has been found.

## II INSULATING SYSTEM

An insulating system is an assembly of insulating materials in association with the conductors and supporting structural parts of an electrical apparatus. Thus, the insulation on the mager wire, the insulation separating phases, slot liner, and varnish all compose the insulating system of a stator winding. An isulation system may be classied A,B,G, or H according to its temperature rating, as designated by the National Electrical Manufacturer Association (NEMA).

Insulation system Limiting Temperatures

| Insulation System Classification | Limiting Temperature,C |
|---|---|
| Class A | 105 |
| Class B | 130 |
| Class F | 155 |
| Class H | 180 |

## III. CAUSES OF INSULATION FAILURE

### A. Temperature

The temperature coefficient of resistance of an insulating material is a negative value and relatively large. Therefore, even a small increase in temperaturer will cause a large decrease in insulation resistance. The thermal theory of dielectric breakdown postulates that the current distribution over a given

insulation sample is not uniform. The weak part carries more current and is heated more than other parts. As long as the insulation or adjacent structure can conduct the heat away as fast as it is generated, the temperature will remain stable and no failure will occur. However, if the heat is not become increasingly hotter until thermal.

B. Thermal Aging

The temperature at which an insulattion operates determines its useful life. Insulation does not always fail when reaching some critical temperature, but by gradual mechanical deterioration with time at an elevated temperature. The time-temperature relationship determines the rate at which the mechaniical strength of organic material decreases. Thereafter, electrical failure may occur because of physical disintegration of the insulation. An approximate rule of thumb states that the thermal life of instalation halves for each 10 degrees C increase in termperature.

C. Dielectric Breakdown Due to Voltage Surges

A physical measure of an insulation with the destructicn of moiecular bonds might occur during momentary overpotential stresses the molecular of the insulating material, causing mzation and failure of the material itself.

D. Mechanical Damage

Insulation can available damaged by mechanical vibration and expansion/contraction. When current is applied, the end turns of a motor winding are fixed. If this twisting force is strong enough to break the bond of the insulating varnish, the turns of magnet wire can wear against each other. This wire-to or coil-to-coil wear abraids the enamel layer of the magnet wire. Eventually the wires can come into direct contact, creating a turn-a-turn short. Once the turns are shorted, localized heating is caused by the current induced onto the closesd loop. This closed circuit behaves like the secondary of a transformer, which when closed dissipates all the induced power as heat. This heat rapidly degrades the surrounding insulation of eventually destroys the ground wall. When the ground wall fails, so much current passes through the fault that all the surrounding insulation is charred. This destroys the evidence of the turn-to-turn short which caused the failure.

Industrial duty motor windings are often bonded, braided, or encapsulated in an attempt to prevent this wire-to-wire wear. In large motors, surge rings are installed to brace the end turns and minimize coil-or-coil shifting. New motor designs, particularly the energy efficient motors, require very right spacing of turns and coils. This compacting of the wire and operation at higher temperature may cause the turn insulation to fail ever sooner.

## IV TESTING OF INSULATION SYSTEMS

Various means of electrical testing have come into use over the years. Registar of continuity, megohmmeter, high potential, are surge testing are the most common. Each has its own merit, yet none are all-inclusive. Hoever, when used in conjunction with one another, they can and do provide very accurate and detailed information concerning the condition of an electrical apparatus.

Tools are only as good as the user, consequently adequate instruction and training are necessary to make the most effective use of them. Additionally, with proper instruction, knowledge of test methods, and maintenance of accurate rest recordsm the maintenance, engineering, and repair staff can become an efficient team capable of handling most any problem that might arise.

### A. The Multimeter

Multimeter tests are the most frequently ussed preliminary test on any peice of electrical apparatus. Very few people working in the electrical environment have never used a multimeter. It is probably the most useful and versatile piece of equipment an electrician owns.

Multimeters derive their name from the many functions they perform. Most will measure both AC and DC potential differences up to 600volts. AC and DC current up to 12 amps, and resistance from perhaps 2K ohms to 20K ohms, all on one meter movement. Many have additional features as well, making them a very valuable, portable, and versatile too.

## 1. **Test Methods**

### a. VOLTAGE TESTS

Voltage tests are made across the line of a piece of equipment in service, at various pointss in a circuit, or simply to check for a voltage potential prior to working on a piece of equipment. Voltage tests are made by setting the select switch to the highest level and stepping the switch down until the meter movements reads mid-scale. This procedure is used to avoid damaging the meter movement and care should be taken in all such tests to assure th select switch is in the proper position for the type of testing being performed.

### b. CURRENT TESTS

Current tests are run in the same manner as voltage tests, except that the current must pass through the meter and the continuity of the circuitry must be broken to do so. Care should be taken not to exceed the limits of the instrument. For large current tests, clamp-on or some other type ammeter is employed.

c. RESISTANCE AND CONTINUITY TESTS

Resistance values are measured by passing a small current through that resistance from batteries within the instrument. Care should be taken to maintain the batteries in good condition and to zero the meter movement prior to making resistance measurements. Avoid contacting live circuits when in the resistance position of the meter.

Continuity tests are simply an extension of a resistance check to verify the continuity, or lack of, in a circuit. This is most useful when checking and making electrical connections.

B. Millohmmeters

Milliohmmeters measure low resistances. They are often employed to check the quality of electrical connections that would go undetected with megohmmeter, hipot, or surge testing. Winding resistance checks can also be made with milliohmmeters to assure proper wire gauges. Motor control contacts can be checked for arcing damage.

C. Megohmmeter Testing

Insulation resistance is a quantity that can be measured without damaging the insulation and furnishes a highly useful

guide for determining the general condition of insulation but is, by itself, not entirely conclusive.

The megohmmeter is an instrument designed specifically to measure insulation resistance directly in megohms ( $M\Omega$ 106 ohms). Megohmmeter testing may be used to test the insulation resistance between conductors of separate circuits or between the conductors and ground. Remember that the megohmmeter tests only insulation resistance and not the dielectric strength of an insulation.

Test measurements have shown that insulation resistance measurements at moderate voltages may actually increase after the insulation has been punctured by AC hipot tests. Clean, dry insulation having cracks or other faults may show a high value of insulation resistance, but obviously is not suitable for use. These limitations of isulation resistance values must be fully realized when the condition of insulation is appraised by such measurements.

Various types of megohmmeters are available to the user: hand crank operated, battery powered, and modern driven. They may cithet generate or supply a DC voltage output of 500 of 1000 volts at a very low current level. This current passes through an unknown resistance and through the meter movement. The resistance value is then read directly on the meter in megohms. These instruments have ranges up to several thousand megohms.

## 2.3 **TEST PARAMETERS**

The Test parameters under consideration are

(1) Interturn short

(2) Insulation Resistance

(3) Coil resistance

(4) Welding resistance

(5) Discontinuity

(6) Rise in temperature

1. **Interturn short** :

It is due to the short between two coils (or ) between coil and body.

2. **Insulation resistance** :

It is the resistance of the insulating material to prevent short-circuiting of wires. It comes in the order of magohms.

3. **Coil resistance** :

It is the resistance of the copper wire of the entire windings. It comes in the order of few ohms. The coil resistance can be measured between any two commutator segments.

4. **Welding resistance** :

In universal motors welding provided is spot welding. Welding is done, to connect the lead wires from the armeture slot and commutator segments. The value of welding resistance comes around milliohms. Welding resistance normally changes with rise

in temperature. Thus its value is measured with full load current.

5. **Discontinuity ;**

This arises, when there is a break in the winding. Due to this, there will be open circuit and the characteristics of the motor is changed. This is the very important parameter that ha to be considered, when motors are tested.

## 2.4 FAULT DETECTION

Fault are detected by making a comparative study. This is mae possible by taping the induced voltage from the rotor. The signals are processed and a comparison is made with the available standard values. The tolerence values are also accounted for during comparison. For example the inter turnshort if any or if the number of windings are less the induced enof will be less than the specified value.

## 2.5 FIELD GENERATOR

To obtain 20 analog signals from the rotor a field generator is required which resembeles the stator of the prime mover.

The basic principle involved is much simiilar to that of a single phase transformer. The single phase transformer has two set of windings primary and secondary which works on the

# FIELD GENERATOR

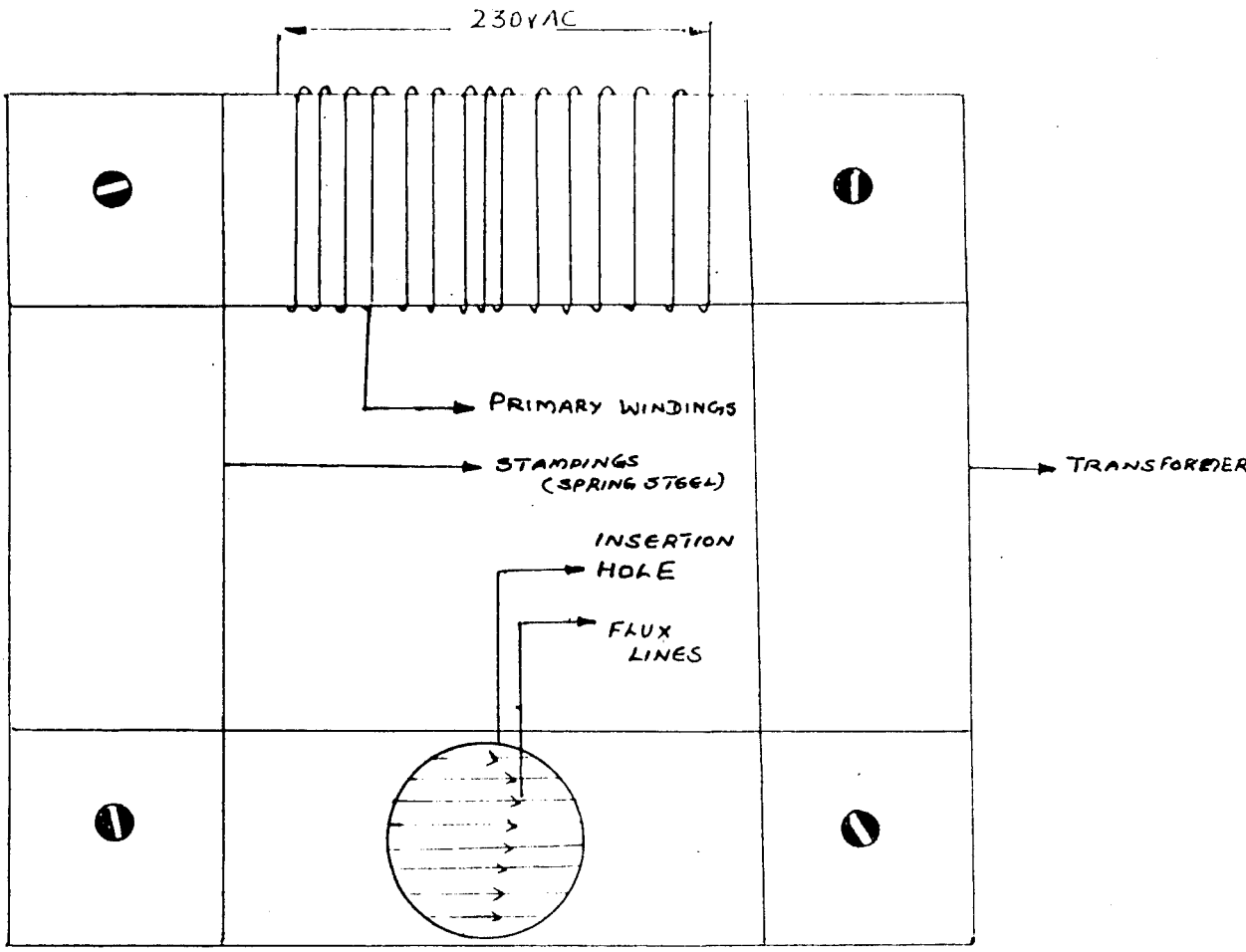



fig 2.9. TOP VIEW

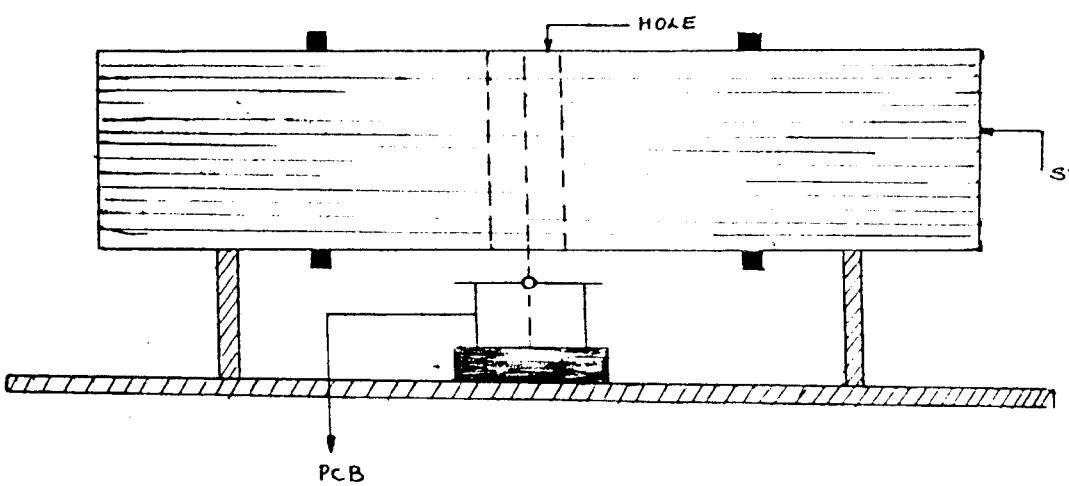



fig 2.10. FRONT VIEW

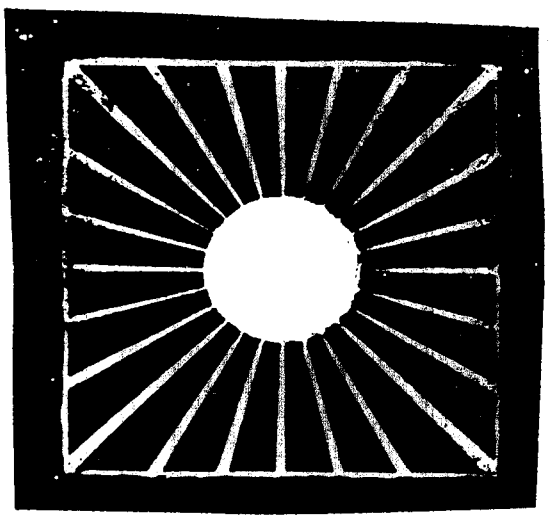


fig 2.11. PCB NEGATIVE

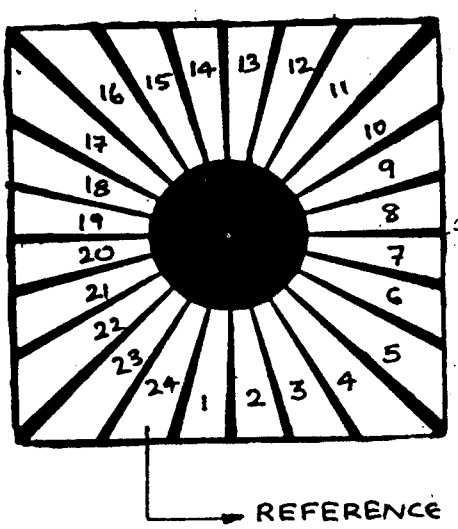



fig 2.12 24 SEGMENT PCB

principle of Favadays electromagnetic induction.

The transformer core is made of spring steel. The primary windings are excited from a 230v A.C. mains the number of windings are 450 turns. In place of the secondary windings a hole of suitable diameter (40.5mm) is drilled the hole is drilled such that the direction of the fluse lies perpendicular to the axis of the hole.

The excitation voltage is alternating and hence the flux direction will vary.

The rotor which is placed inside will have its conductors aligned perpendicular to the flux. Hence a varying flux will induce a voltage in the conductors.

A printed circuit board is designed to collect the voltages induced from the 24 commutator segments. Brange brushes are carefully rivetted on to the PCB for the purpose. Lead wires are taken out from the segments which gives the twenty four analog signals.

## INTRODUCTION

The hardware part gives the physical analogy of the project in a nutshell. This includes the functional block diagram. The functional block diagram encompases mainly of three sections.

i) The analog to digital interface unit.
ii) The processing unit
iii) The display unit

Each of the units involved is described in detail under the heading "HARDWARE".

The functional block diagram of the rotor analyser is shown in figure. As shown the 24 analog signals is rectified before they are given to the "ANALOG TO DIGITAL CONVERTER". The system incorporates two 8255 PPI's to interface the ADC with the central processor and another one to interface the processor with the display units. The central processing unit used is Zilog-80 processor.

The storage facility is provided by one unit of RAM and EPROM each. The display is shown on a seven segment display.

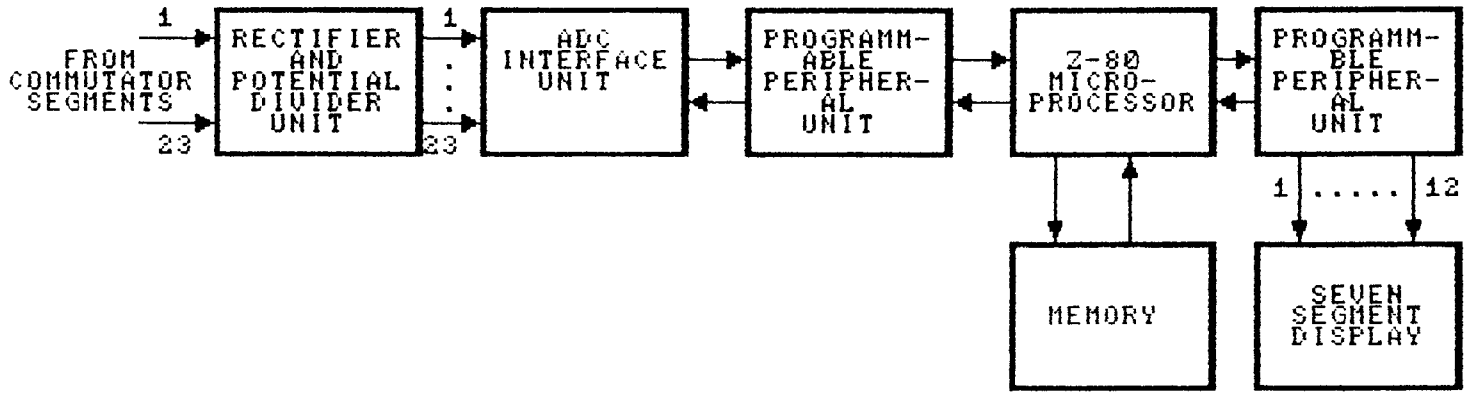



Fig 3.1. FUNCTIONAL BLOCK DIAGRAM

## 3.1 ANALOG TO DIGITAL INTERFACE UNIT

### a) Filters

In order to have uniform sampling points from a set of analog ac signal it has to be rectified and filtered. The output from the filter is a dc signal.

The arbitrary segment is chosen as the reference and the voltages are measured with reference to this segment. The reference segment is grounded along with the system. It is ensured that the ADC receives voltages not exceeding the +Vcc voltage.

The rectifier circuit is necessary to convert a signal having a zero average value to one that has a non-zero average. The output of the rectifier contain ripple and has to be removed, using filter. A simple resistor-capacitor filter (RC filter) circuit is used where the capacitor is connected across the rectifier output and the dc output voltage is available across the capacitor. CD 4040 is a 12 stage ripple carry binary counter is used to ensure the proper value not exceeding +Vcc.

b) Analog to digital conversion

The dc analog signal from the filter forms the inputs to the ADC. The A/D conversion is a quantizing process whereby an analog signal is represented by equivalent binary states for compatibility with the processor.

The ADC 0808 is a typical example of an A/D converter using the successive approximation technique. They contain an 8 bit A/D converter, 8 channel multiplexer with address input latch and associated control logic. They operate using 640 KHz clock.

They can be functionally divided into

i) Analog multiplexer

ii) A/D converter

The analog multiplexer selects upto 8 analog inputs and the A/D converter, transforms the analog output to the multiplexer to an 8 bit digital word.

The ADC 0808 converters were designed to interface to most standard microprocessors with very little external logic. Here the interface is made feasible by the use of 8255 A PPI.

A counter CD 4040 is used to provide the clock frequency of 640 KHz. Since three ADC's are used and for selecting the required chip, the output enable line (OE) on the chip is made use of.

When the conversion cycle is complete, the resulting data is loaded into tristate output latch. The data in the output latch can be read by the host system by activating the output enable line.

c) Programmable peripheral interface unit

The 8255 A is a very powerful tool for interfacing peripheral equipment to the system. It can be programmed to transfer data under various conditions.

Each peripheral device in a system has a service routine. The routine manages the software interface between the device of the CPU.

The 8255 A has 24 I/O pins that can be grouped primarily in two 8 bit parallel ports. A and B with the remaining eight bits as port 'C'.

Here the chip is used in mode '0' condition. Port A being selected as the input port and port B as output port. The eight bits of the port is grouped in two 4-bit port, $C_{upper}$ being used as input port and $C_{lower}$ as the output port.

The datas from the ADC reaches the 8255 A through Port 'A'. The other input port takes the end of conversion signal from the ADC to the 8255 A.

Port B takes address of the input line to be selected the start signal and address latch enable signal (ALE) from 8255 A to ADC. The $C_{lower}$ which acts as the O/P port selects the particular chip.

## 3.2 PROCESSING UNIT

The basic components in the processing unit are Z80 CPU, EPROM (27256) and RAM (6264). The 5V supply is provided to the unit from an external circuitry using 7805 regulator. A crystal of 8 MHz is used to generate the clock signal. Schmitt Triggers are used for wave shapping.

In our case Z80 CPU is made work in the memory mapped I/O. The maximum capacity of the memory chip used is less than 8 Kilo bytes. This means that 2 address lines $A_{14}$ and $A_{15}$ are free. A 2 x 4 decoder (74LS139) is being used by the Z80 CPU to select the memory chips and peripheral interface chips.

EPROM is loaded with the programs that is used to execute the entire process. First of all the data from the commutator segments are filtered and is given to the ADC card. The O/P from the ADC is taken and placed in the RAM by the processor. Then the signal from the next segment is now taken and placed in the RAM and so on. Like this all the values from the 23 segments is placed sequentially in the RAM.

Now the test values started in the RAM is compared with the standard value in the EPROM. If the test value lies within the ± tolerance range, then the rotor is good. If it is out of the limit the rotor is a bad one.

If the test value is less than the standard value the problem is that there is some interturn short or the number of turns is less. If the test value is more than the standard value the problem like open circuit is occured.

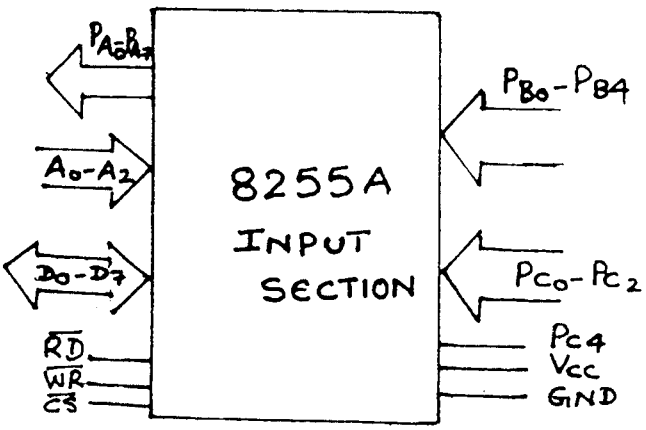



Fig 3.2 (a)

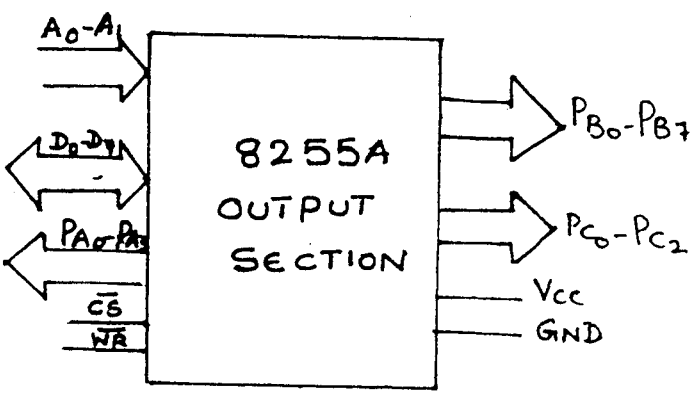



Fig 3.2 (b)

BLOCK DIAGRAMS OF PPI - I/O SECTIONS (8255A)

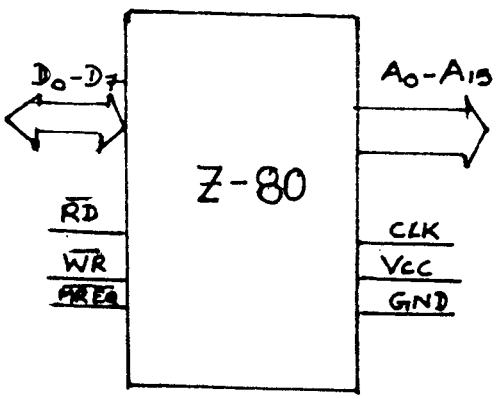



Fig 3.3

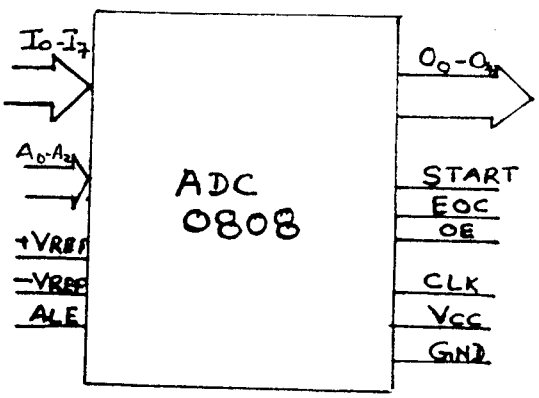



Fig 3.4

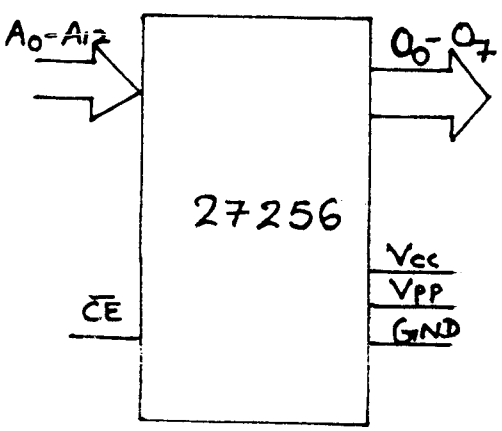



Fig 3.5

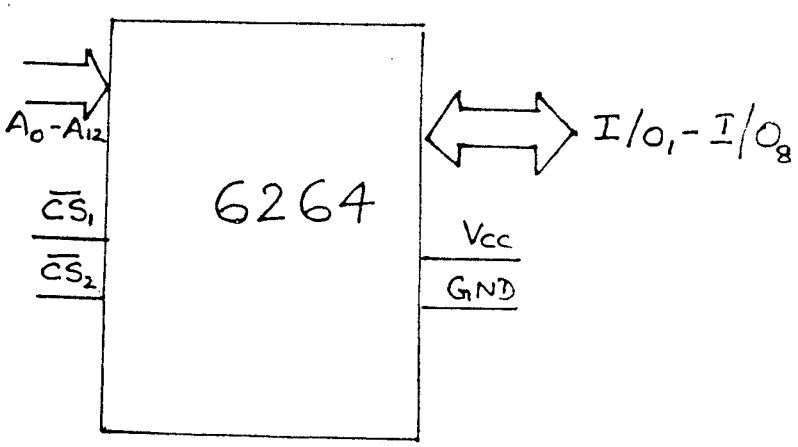



Fig 3.6

BLOCK DIAGRAMS OF Z-80, A/D CONVERTER (0808), EPROM (27256) & RAM (6264).

## 3.3 DISPLAY UNIT

To display the data processed twelve 7 segment LED's are used. The seven segment display used is LT 573.

The signal processed in the Z80 are interfaced to the display LED's using 8255 A PPI. The datas are received from the data bus. To display the BCD data to the 7 segment display a BCD to 7 segment Decoder is used.

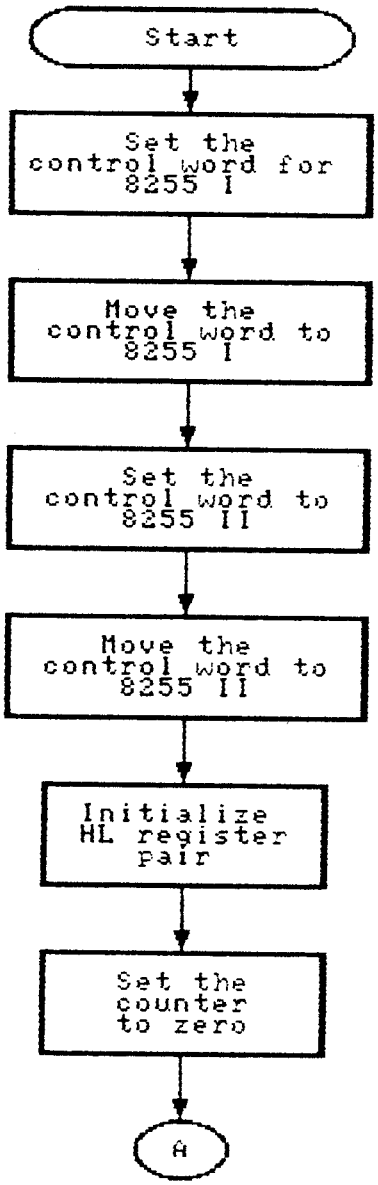
8255 A uses the least four bits of Port A as the data bus to the decoder. The control bits to the decoder are provided through Port C and B. Using the 4 bits of Port A the BCD to seven segment conversion is done. The twelve LED units are arranged such a way that only one letter can be displayed at a time.

The particular chip is selected by activating the latch enable (LE) signal through any one of the 12 port lines which forms the control bits.

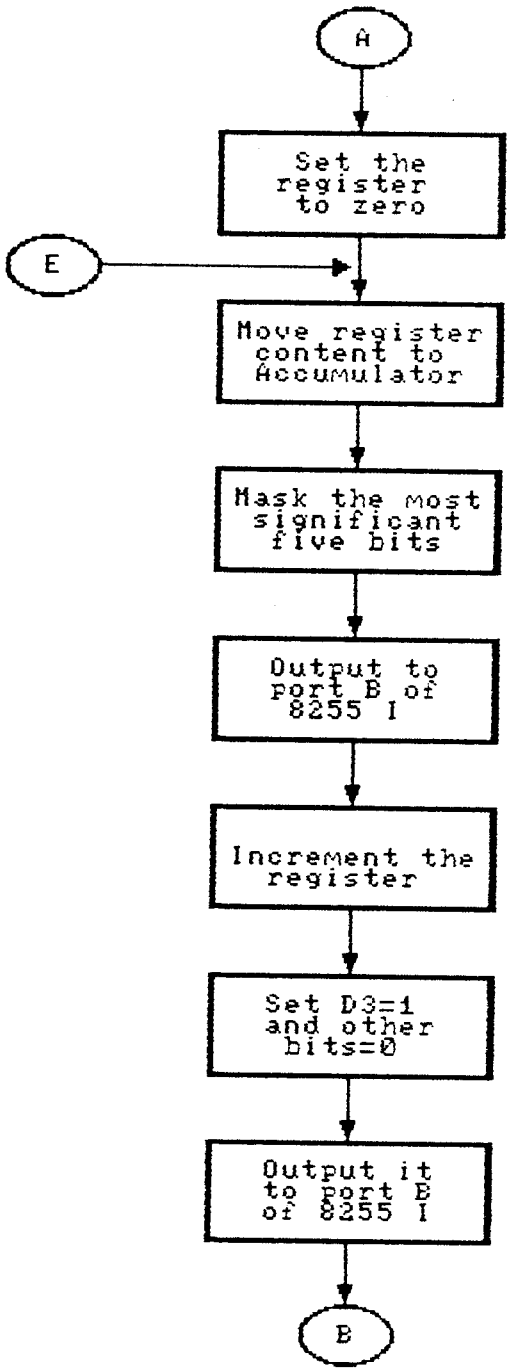
Since the operation takes place fast in GHZ and due to persistance of vision a word say "IT IS GOOD" can be identified.

## 3.1 ALGORITHM

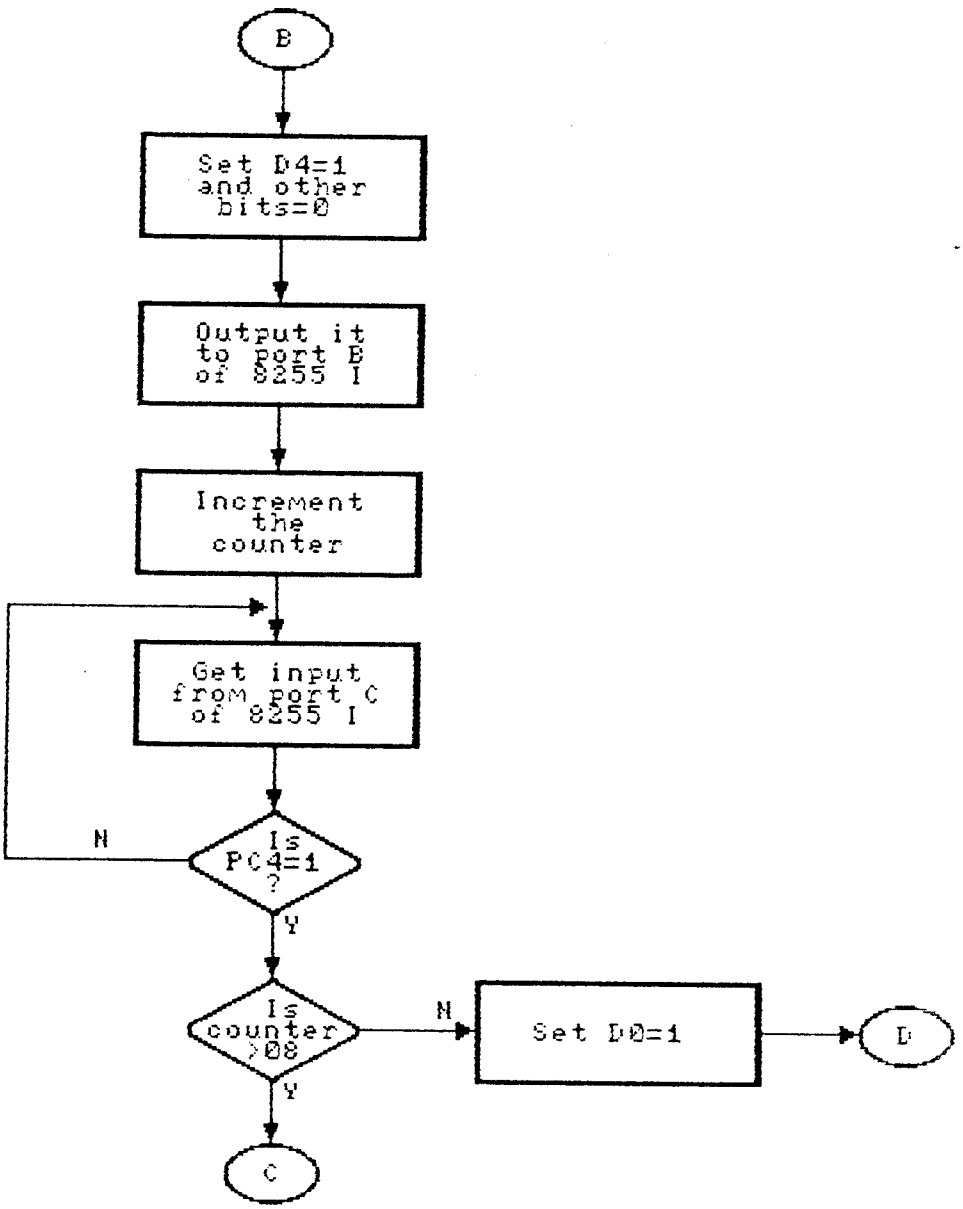
1.Initialising the peripherals
Both the 8255's are initialised by giving their control words to their corresponding control registers.
2.Getting the data from AD card
i)Check for the input signal until there is any.
ii)Give the address for the input channel.
iii)Give the address latch enable signal.
iv)Give the start signal.
v)Get the end of conversion signal.
vi)Give the output enable signal.
vii)Get the data bits.
3.Arranging the data
i)The data from the first segment is stored in a specified location in RAM.
ii)Increment the address for the next segment through 8255 I.
iii)Get the data and store in the next memory location.
iv)Repeat the above two steps until all the data are received.
4.Comparing the data
i)Standard values including their tolerence are stored in the EPROM. The test values are compared with these standard values.
ii)If there is any deviation from the standard value then the rotor is displayed bad.
iii)If all the values coincide then the rotor is displayed good.



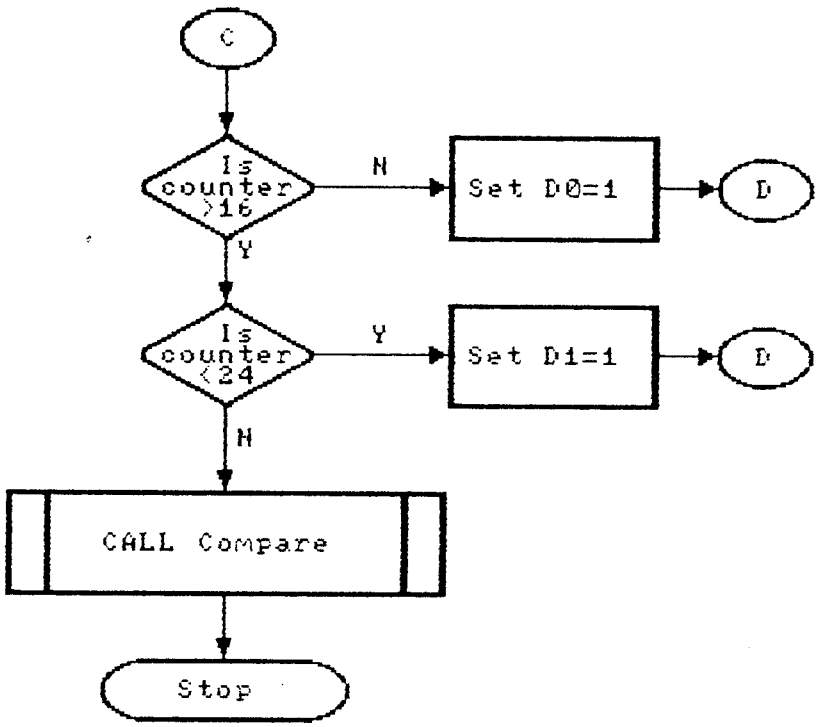

FLOW CHART 1(a)



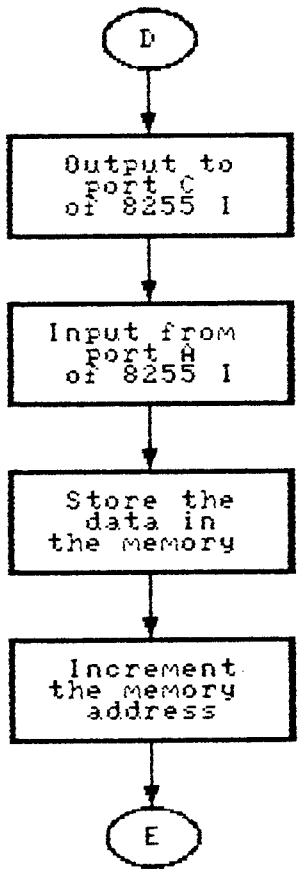

FLOW CHART 1(b)



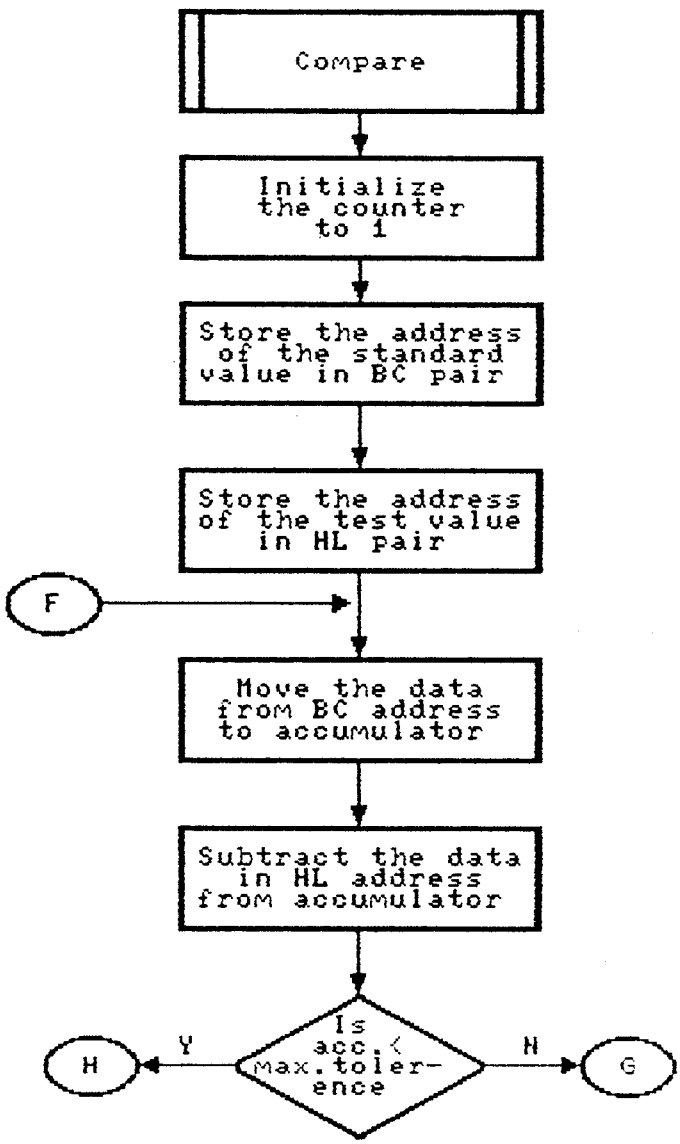

FLOW CHART 1 (c)



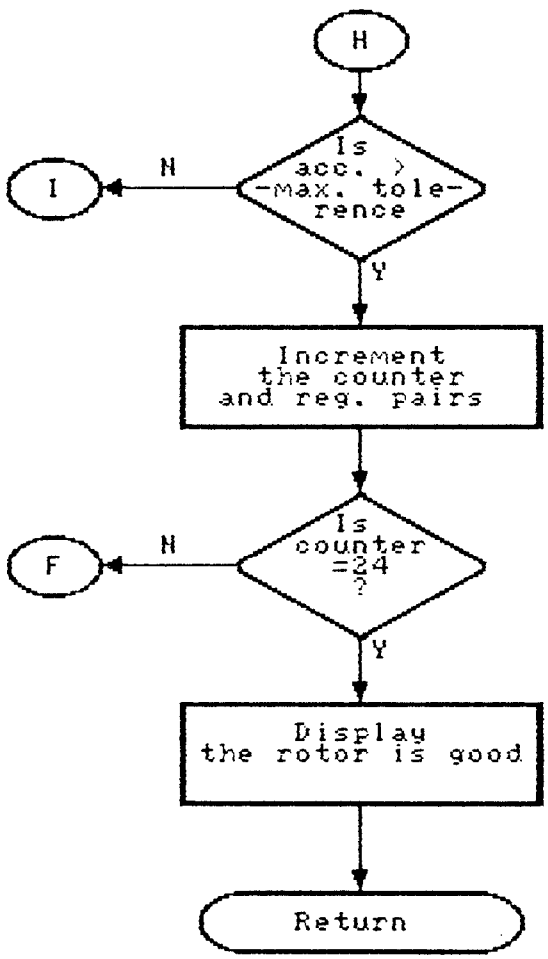

FLOW CHART 1(d)



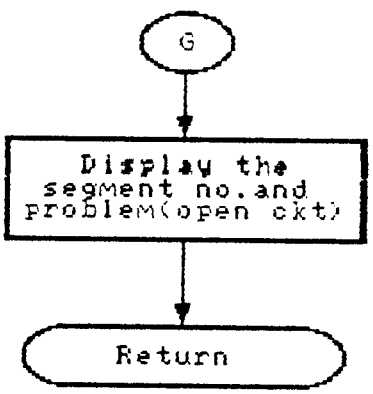

FLOW CHART 1(e)

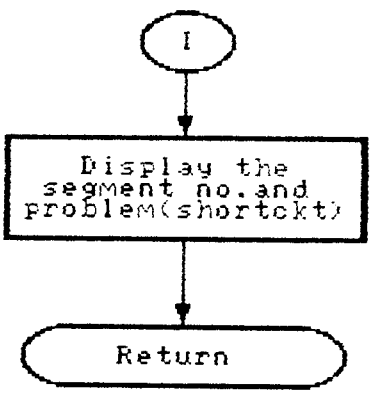



FLOW CHART 2 (a)




FLOW CHART 2(b)




FLOW CHART 2 (c)

### 3.3 PROGRAM

| ADDRESS | OPCODE | LABLE | MNEMONIC |
|---|---|---|---|
| 0000 | 3E 98 | | LD A,98 |
| 0002 | 32 FF FF | | LD FFFF,A |
| 0005 | 3E 80 | | LD A,80 |
| 0007 | 32 FF 7F | | LD 7FFF,A |
| 000A | 21 00 81 | | LD HL,8100 |
| 000D | 00 00 00 | | NOP |
| 0010 | 06 00 | | LD B,00 |
| 0012 | 0E 00 | | LD C,00 |
| 0014 | 79 | LOOP2: | LD A,C |
| 0015 | A6 07 | | AND 07 |
| 0017 | 32 FD FF | | LD FFFD,A |
| 001A | 0C | | INC C |
| 001B | 3E 08 | | LD A,08 |
| 001D | 32 FD FF | | LD FFFD,A |
| 0020 | 3E 10 | | LD A,10 |
| 0022 | 32 FE FF | | LD FFFD,A |
| 0025 | 04 | | INC B |
| 0026 | 3A FE FF | | LD A,FFFE |
| 0029 | A6 10 | | AND 10 |
| 002B | D6 10 | | SUB 10 |
| 002D | 20 F9 | | JRNZ F9 |
| 002F | 78 | | LD A,B |
| 0030 | D6 09 | | SUB 09 |
| 0032 | 30 1D | | JRNC 1D |

```
0034    D6  08              SUB 08
0036    30  1E              JRNC 1E
0038    D6  07              SUB 06
003A    20  1F              JRNZ 1F
003C    CD  00  01          CALL COMPARE
003F    76                  HALT

0050    3E  01              LD A,01
0052    C3  5C  00          JP LOC1
0055    3E  02              LD A,02
0057    C3  5C  00          JP LOC1
005A    3E  04              LD A,04
005C    32  FE  FF  LOC1:   LD FFFE,A
005F    3A  FC  FF          LD A,FFFC
0062    77                  LD (HL),A
0063    23                  INC HL
0064    C3  14  00          JP LOOP2
```

```
0100    1E  01          COMPARE: LD E,01
0102    21  00  81               LD HL,8100
0105    01  00  10               LD BC,1000
0108    0A               CON:    LD A,(BC)
0109    96                       SUB A,(HL)
010A    FA  00  06               JPM BAD1
010D    03                       INC DC
010E    0A                       LD A,(BC)
010F    96                       SUB A,(HL)
0110    F2  00  07               JPP BAD2
0113    23                       INC HL
0114    03                       INC BC
0115    1C                       INC E
0116    3E  24                   LD A,24
0118    93                       SUB A,E
0119    CA  00  50               JPZ GOOD
012C    C3  08  01               JP CON
```

```
0500    21  00  15    GOOD:   LD HL,1500
0053    C3  00  08            JP DISPLAY
0600    21  00  16    BAD1:   LD HL,1600
0603    C3  00  08            JP DISPLAY
0700    21  00  17    BAD2:   LD HL,1700
0703    C3  00  08            JP DISPLAY
```

```
0800    06  FF        DISPLAY: LD B,FF
0802    2E  00                 LD L,00
0804    0E  FE                 LD C,FE
0806    78             LOC2:   LD A,B
0807    32  FD  7F             LD 7FFD,D
080A    79                     LD A,C
080B    32  FE  7F             LD 7FFE,A
080E    2D                     INC L
080F    7D                     LD A,L
0810    D6  04                 SUB 04
0812    CA  1E  08             JPZ LOC3
0815    FA  22  08             JPM LOC4
0818    79                     LD A,C
0819    07                     RLC A
081A    4F                     LD C,A
081B    C3  06  08             JP LOC2
081E    0E  FF         LOC3:   LD C,FF
0820    06  7F                 LD B,7F
0822    7D             LOC4:   LD A,L
0823    D6  0C                 SUB 0C
0825    CA  00  08             JPZ DISPLAY
0828    78                     LD A,B
0829    07                     RLC A
082A    47                     LD B,A
082B    C3  06  08             JP LOC2
```

| | |
|---|---|
| 1500 | 60 |
| 1501 | 87 |
| 1502 | 00 |
| 1503 | 00 |
| 1504 | 60 |
| 1505 | D5 |
| 1506 | 00 |
| 1507 | 00 |
| 1508 | D7 |
| 1509 | F2 |
| 150A | F2 |
| 150B | E6 |

| | |
|---|---|
| 1600 | 92 |
| 1601 | 67 |
| 1602 | 97 |
| 1603 | 92 |
| 1604 | 00 |
| 1607 | 00 |
| 1608 | F2 |
| 1609 | 27 |
| 160A | 92 |
| 160B | 87 |

| | |
|---|---|
| 1700 | 92 |
| 1701 | 67 |
| 1702 | 97 |
| 1703 | 92 |
| 1704 | 00 |
| 1707 | 00 |
| 1708 | D5 |
| 1709 | 67 |
| 170A | 92 |
| 170B | 87 |

# CONCLUSION

"MICROPROCESSOR BASED ROTOR ANALYSER" (MBRA) used for industrial automation is a powerful tool used in the production line. The equipment is constructed and tested. The hardware has been interfaced with the microprocessor.

MBRA when used in the on line production, it would be better to interface the system with a Computer.

# Z8400
# Z80® CPU Central Processing Unit

# Zilog

## Product Specification

September 1983



**Features**

- The instruction set contains 158 instructions. The 78 instructions of the 8080A are included as a subset; 8080A software compatibility is maintained.
- Eight MHz, 6 MHz, 4 MHz and 2.5 MHz clocks for the Z80H, Z80B, Z80A, and Z80 CPU result in rapid instruction execution with consequent high data throughput.
- The extensive instruction set includes string, bit, byte, and word operations. Block searches and block transfers together with indexed and relative addressing result in the most powerful data handling capabilities in the microcomputer industry.
- The Z80 microprocessors and associated family of peripheral controllers are linked by a vectored interrupt system. This system may be daisy-chained to allow implementation of a priority interrupt scheme. Little, if any, additional logic is required for daisy-chaining.
- Duplicate sets of both general-purpose and flag registers are provided, easing the design and operation of system software through single-context switching, background-foreground programming, and single-level interrupt processing. In addition, two 16-bit index registers facilitate program processing of tables and arrays.
- There are three modes of high-speed interrupt processing: 8080 similar, non-Z80 peripheral device, and Z80 Family peripheral with or without daisy chain.
- On-chip dynamic memory refresh counter.

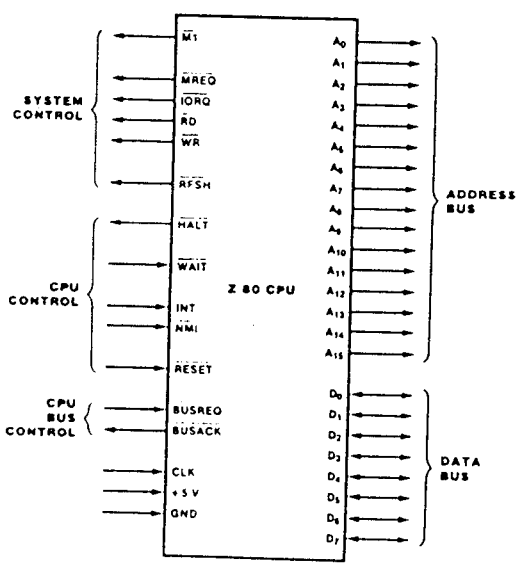



Figure 1. Pin Functions

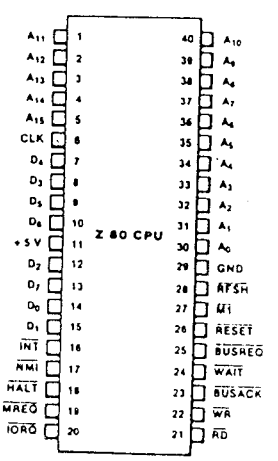



Figure 2. Pin Assignments

## General Description

The Z80, Z80A, Z80B, and Z80H CPUs are third-generation single-chip microprocessors with exceptional computational power. They offer higher system throughput and more efficient memory utilization than comparable second-and third-generation microprocessors. The internal registers contain 208 bits of read/write memory that are accessible to the programmer. These registers include two sets of six general-purpose registers which may be used individually as either 8-bit registers or as 16-bit register pairs. In addition, there are two sets of accumulator and flag registers. A group of "Exchange" instructions makes either set of main or alternate registers accessible to the programmer. The alternate set allows operation in foreground-background mode or it may be reserved for very fast interrupt response.

The Z80 also contains a Stack Pointer, Program Counter, two index registers, a Refresh register (counter), and an Interrupt register. The CPU is easy to incorporate into a system since it requires only a single +5 V power source. All output signals are fully decoded and timed to control standard memory or peripheral circuits, and it is supported by an extensive family of peripheral controllers. The internal block diagram (Figure 3) shows the primary functions of the Z80 processors. Subsequent text provides more detail on the Z80 I/O controller family, registers, instruction set, interrupts and daisy chaining, and CPU timing.

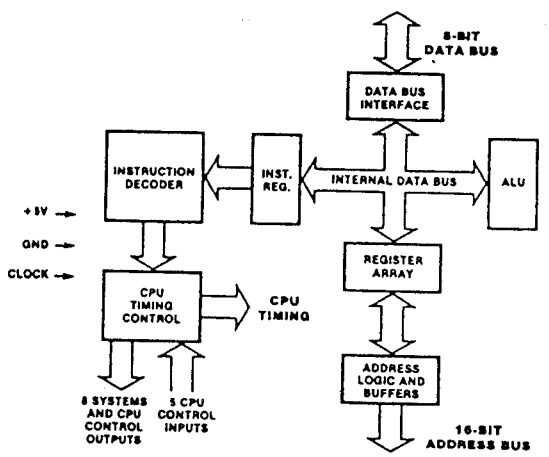



Figure 3. Z80 CPU Block Diagram

**Z80 Microprocessor Family**

The Zilog Z80 microprocessor is the central element of a comprehensive microprocessor product family. This family works together in most applications with minimum requirements for additional logic, facilitating the design of efficient and cost-effective microcomputer-based systems.

Zilog has designed five components to provide extensive support for the Z80 microprocessor. These are:

- The PIO (Parallel Input/Output) operates in both data-byte I/O transfer mode (with handshaking) and in bit mode (without handshaking). The PIO may be configured to interface with standard parallel peripheral devices such as printers, tape punches, and keyboards.
- The CTC (Counter/Timer Circuit) features four programmable 8-bit counter/timers, each of which has an 8-bit prescaler. Each of the four channels may be configured to operate in either counter or timer mode.
- The DMA (Direct Memory Access) controller provides dual port data transfer operations and the ability to terminate data transfer as a result of a pattern match.
- The SIO (Serial Input/Output) controller offers two channels. It is capable of operating in a variety of programmable modes for both synchronous and asynchronous communication, including Bi-Sync and SDLC.
- The DART (Dual Asynchronous Receiver/Transmitter) device provides low cost asynchronous serial communication. It has two channels and a full modem control interface.

**Z80 CPU Registers**

Figure 4 shows three groups of registers within the Z80 CPU. The first group consists of duplicate sets of 8-bit registers: a principal set and an alternate set (designated by ' [prime], e.g., A'). Both sets consist of the Accumulator Register, the Flag Register, and six general-purpose registers. Transfer of data between these duplicate sets of registers is accomplished by use of "Exchange" instructions. The result is faster response to interrupts and easy, efficient implementation of such versatile programming techniques as background-foreground data processing. The second set of registers consists of six registers with assigned functions. These are the I (Interrupt Register), the R (Refresh Register), the IX and IY (Index Registers), the SP (Stack Pointer), and the PC (Program Counter). The third group consists of two interrupt status flip-flops, plus an additional pair of flip-flops which assists in identifying the interrupt mode at any particular time. Table 1 provides further information on these registers.

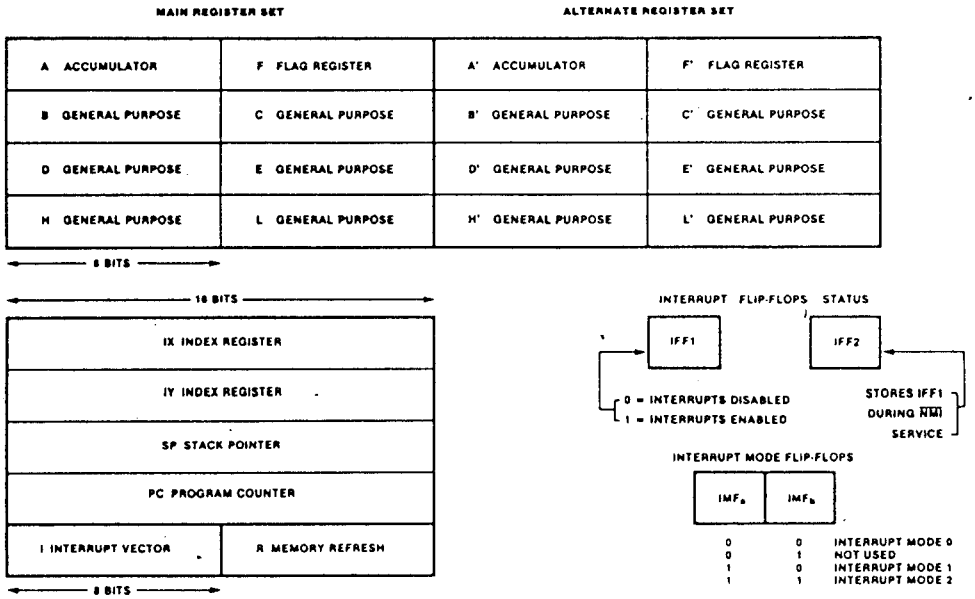



Figure 4. CPU Registers

**Z80 CPU Registers** (Continued)

| Register | | Size (Bits) | Remarks |
|---|---|---|---|
| A, A' | Accumulator | 8 | Stores an operand or the results of an operation. |
| F, F' | Flags | 8 | See Instruction Set. |
| B, B' | General Purpose | 8 | Can be used separately or as a 16-bit register with C. |
| C, C' | General Purpose | 8 | See B, above. |
| D, D' | General Purpose | 8 | Can be used separately or as a 16-bit register with E. |
| E, E' | General Purpose | 8 | See D, above. |
| H, H' | General Purpose | 8 | Can be used separately or as a 16-bit register with L. |
| L, L' | General Purpose | 8 | See H, above. |
| | | | Note: The (B,C), (D,E), and (H,L) sets are combined as follows:<br>B — High byte C — Low byte<br>D — High byte E — Low byte<br>H — High byte L — Low byte |
| I | Interrupt Register | 8 | Stores upper eight bits of memory address for vectored interrupt processing. |
| R | Refresh Register | 8 | Provides user-transparent dynamic memory refresh. Lower seven bits are automatically incremented and all eight are placed on the address bus during each instruction fetch cycle refresh time. |
| IX | Index Register | 16 | Used for indexed addressing. |
| IY | Index Register | 16 | Same as IX, above. |
| SP | Stack Pointer | 16 | Holds address of the top of the stack. See Push or Pop in instruction set. |
| PC | Program Counter | 16 | Holds address of next instruction. |
| $IFF_1$-$IFF_2$ | Interrupt Enable | Flip-Flops | Set or reset to indicate interrupt status (see Figure 4). |
| IMFa-IMFb | Interrupt Mode | Flip-Flops | Reflect Interrupt mode (see Figure 4). |

**Table 1. Z80 CPU Registers**

**Interrupts: General Operation**

The CPU accepts two interrupt input signals: $\overline{NMI}$ and $\overline{INT}$. The $\overline{NMI}$ is a non-maskable interrupt and has the highest priority. $\overline{INT}$ is a lower priority interrupt and it requires that interrupts be enabled in software in order to operate. $\overline{INT}$ can be connected to multiple peripheral devices in a wired-OR configuration.

The Z80 has a single response mode for interrupt service for the non-maskable interrupt. The maskable interrupt, $\overline{INT}$, has three programmable response modes available. These are:

- Mode 0 — similar to the 8080 microprocessor.
- Mode 1 — Peripheral Interrupt service, for use with non-8080/Z80 systems.
- Mode 2 — a vectored interrupt scheme, usually daisy-chained, for use with Z80 Family and compatible peripheral devices.

The CPU services interrupts by sampling the $\overline{NMI}$ and $\overline{INT}$ signals at the rising edge of the last clock of an instruction. Further interrupt service processing depends upon the type of interrupt that was detected. Details on interrupt responses are shown in the CPU Timing Section.

**Interrupts: General Operation** (Continued)

**Non-Maskable Interrupt ($\overline{NMI}$).** The non-maskable interrupt cannot be disabled by program control and therefore will be accepted at all times by the CPU. $\overline{NMI}$ is usually reserved for servicing only the highest priority type interrupts, such as that for orderly shutdown after power failure has been detected. After recognition of the $\overline{NMI}$ signal (providing $\overline{BUSREQ}$ is not active), the CPU jumps to restart location 0066H. Normally, software starting at this address contains the interrupt service routing.

**Maskable Interrupt ($\overline{INT}$).** Regardless of the interrupt mode set by the user, the Z80 response to a maskable interrupt input follows a common timing cycle. After the interrupt has been detected by the CPU (provided that interrupts are enabled and $\overline{BUSREQ}$ is not active) a special interrupt processing cycle begins. This is a special fetch ($\overline{M1}$) cycle in which $\overline{IORQ}$ becomes active rather than $\overline{MREQ}$, as in normal $\overline{M1}$ cycle. In addition, this special $\overline{M1}$ cycle is automatically extended by two $\overline{WAIT}$ states, to allow for the time required to acknowledge the interrupt request.

**Mode 0 Interrupt Operation.** This mode is similar to the 8080 microprocessor interrupt service procedures. The interrupting device places an instruction on the data bus. This is normally a Restart instruction, which will initiate a call to the selected one of eight restart locations in page zero of memory. Unlike the 8080, the Z80 CPU responds to the Call instruction with only one interrupt acknowledge cycle followed by two memory read cycles.

**Mode 1 Interrupt Operation.** Mode 1 operation is very similar to that for the $\overline{NMI}$. The principal difference is that the Mode 1 interrupt has a restart location of 0038H only.

**Mode 2 Interrupt Operation.** This interrupt mode has been designed to utilize most effectively the capabilities of the Z80 microprocessor and its associated peripheral family. The interrupting peripheral device selects the starting address of the interrupt service routine. It does this by placing an 8-bit vector on the data bus during the interrupt acknowledge cycle. The CPU forms a pointer using this byte as the lower 8-bits and the contents of the I register as the upper 8-bits. This points to an entry in a table of addresses for interrupt service routines. The CPU then jumps to the routine at that address. This flexibility in selecting the interrupt service routine address allows the peripheral device to use several different types of service routines. These routines may be located at any available location in memory. Since the interrupting device supplies the low-order byte of the 2-byte vector, bit 0 ($A_0$) must be a zero.

**Interrupt Priority (Daisy Chaining and Nested Interrupts).** The interrupt priority of each peripheral device is determined by its physical location within a daisy-chain configuration. Each device in the chain has an interrupt enable input line (IEI) and an interrupt enable output line (IEO), which is fed to the next lower priority device. The first device in the daisy chain has its IEI input hardwired to a High level. The first device has highest priority, while each succeeding device has a corresponding lower priority. This arrangement permits the CPU to select the highest priority interrupt from several simultaneously interrupting peripherals.

The interrupting device disables its IEO line to the next lower priority peripheral until it has been serviced. After servicing, its IEO line is raised, allowing lower priority peripherals to demand interrupt servicing.

The Z80 CPU will nest (queue) any pending interrupts or interrupts received while a selected peripheral is being serviced.

**Interrupt Enable/Disable Operation.** Two flip-flops, $IFF_1$ and $IFF_2$, referred to in the register description are used to signal the CPU interrupt status. Operation of the two flip-flops is described in Table 2. For more details, refer to the *Z80 CPU Technical Manual* and *Z80 Assembly Language Manual.*

| Action | $IFF_1$ | $IFF_2$ | Comments |
|---|---|---|---|
| CPU Reset | 0 | 0 | Maskable interrupt $\overline{INT}$ disabled |
| DI instruction execution | 0 | 0 | Maskable interrupt $\overline{INT}$ disabled |
| EI instruction execution | 1 | 1 | Maskable interrupt $\overline{INT}$ enabled |
| LD A,I instruction execution | • | • | $IFF_2$ → Parity flag |
| LD A,R instruction execution | • | • | $IFF_2$ → Parity flag |
| Accept $\overline{NMI}$ | 0 | $IFF_1$ | $IFF_1$ → $IFF_2$ (Maskable interrupt $\overline{INT}$ disabled) |
| RETN instruction execution | $IFF_2$ | • | $IFF_2$ → $IFF_1$ at completion of an $\overline{NMI}$ service routine. |

**Table 2. State of Flip-Flops**

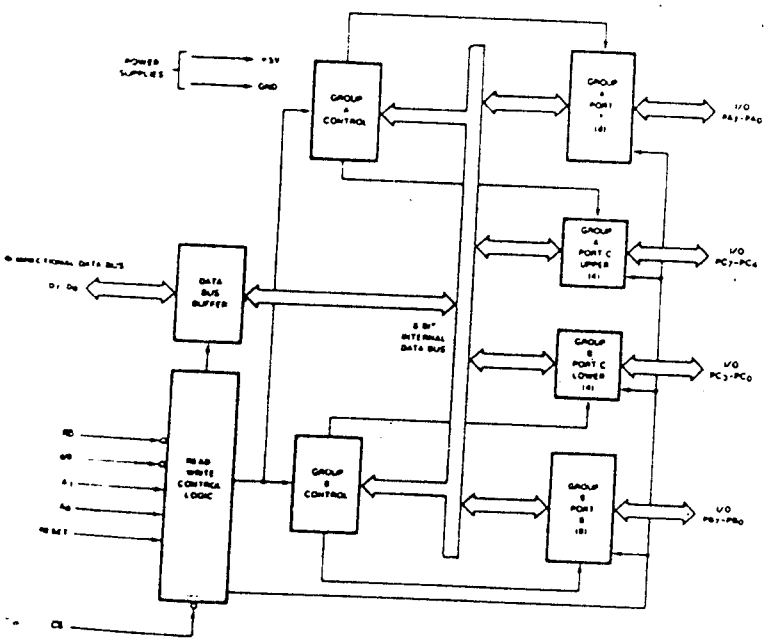
intel

# 8255A/8255A-5
# PROGRAMMABLE PERIPHERAL INTERFACE

- MCS-85™ Compatible 8255A-5
- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with Intel Microprocessor Families
- Improved Timing Characteristics
- Direct Bit Set/Reset Capability Easing Control Application Interface
- Reduces System Package Count
- Improved DC Driving Capability
- Available in EXPRESS
  - —Standard Temperature Range
  - —Extended Temperature Range
- 40 Pin DIP Package or 44 Lead PLCC

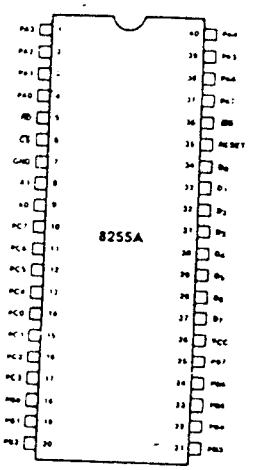
(See Intel Packaging: Order Number: 231369)

The Intel 8255A is a general purpose programmable I/O device designed for use with Intel microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.



231308-1

Figure 1. 8255A Block Diagram




231308-2

Figure 2. Pin Configuration

## 8255A FUNCTIONAL DESCRIPTION

### General

The 8255A is a programmable peripheral interface (PPI) device designed for use in Intel microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 8255A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

### Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 8255A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

### Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

### ($\overline{CS}$)

**Chip Select.** A "low" on this input pin enables the communication between the 8255A and the CPU.

### ($\overline{RD}$)

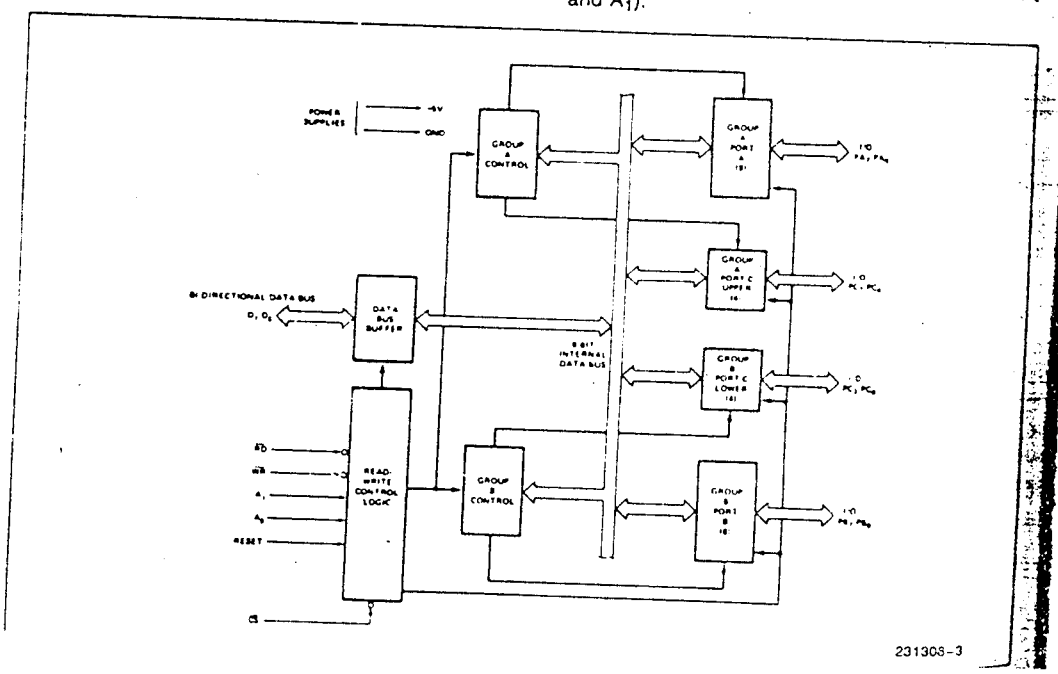
**Read.** A "low" on this input pin enables the 8255A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255A.

### ($\overline{WR}$)

**Write.** A "low" on this input pin enables the CPU to write data or control words into the 8255A.

### ($A_0$ and $A_1$)

**Port Select 0 and Port Select 1.** These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus ($A_0$ and $A_1$).




231308-3

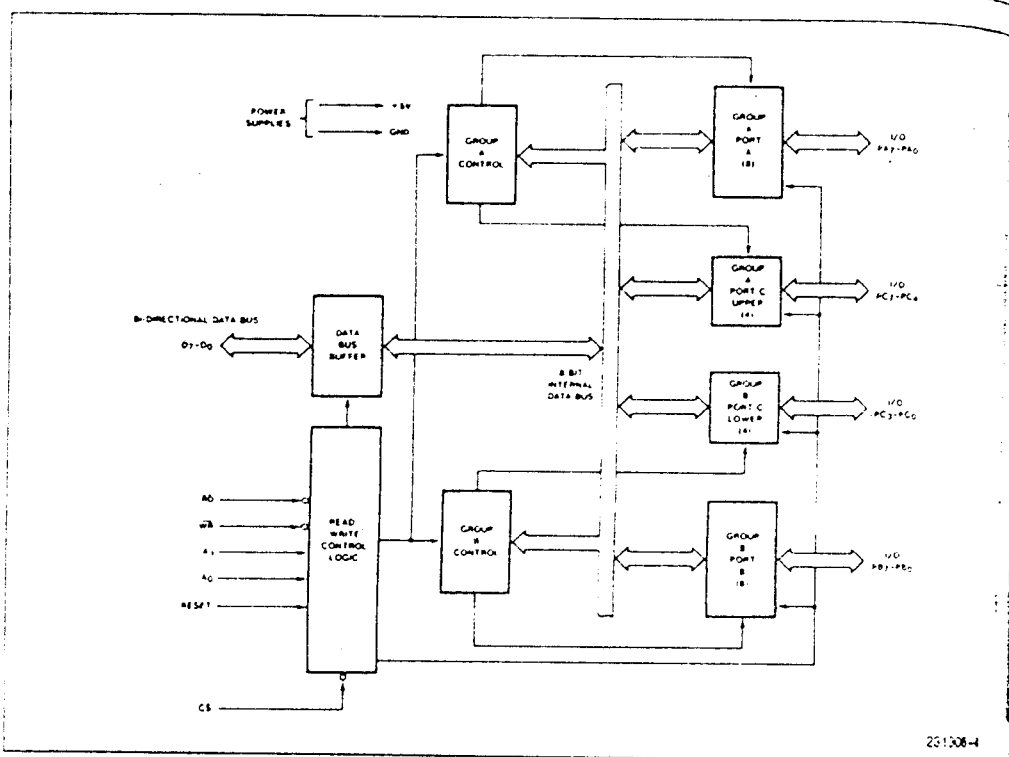
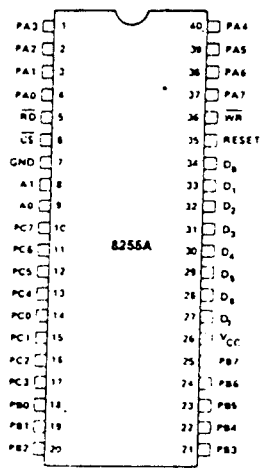



**Figure 4. 8225A Block Diagram Showing Group A and Group B Control Functions**

**Pin Configuration**




231308-5

**Pin Names**

| | |
|---|---|
| $D_7-D_0$ | Data Bus (Bi-Directional) |
| RESET | Reset Input |
| $\overline{CS}$ | Chip Select |
| $\overline{RD}$ | Read Input |
| $\overline{WR}$ | Write Input |
| A0, A1 | Port Address |
| PA7–PA0 | Port A (BIT) |
| PB7–PB0 | Port B (BIT) |
| PC7–PC0 | Port C (BIT) |
| $V_{CC}$ | +5 Volts |
| GND | 0 Volts |

## 8255A OPERATIONAL DESCRIPTION

### Mode Selection

Mode 0—Basic Input/Output

Mode 1—Strobed Input/Output

Mode 2—Bi-Directional Bus

When the reset input goes "high" all ports will be set to the input mode (i.e., all 24 lines will be in the high impedance state). After the reset is removed the 8255A can remain in the input mode with no additional initialization required. During the execution of the system program any of the other modes may be selected using a single output instruction. This allows a single 8255A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

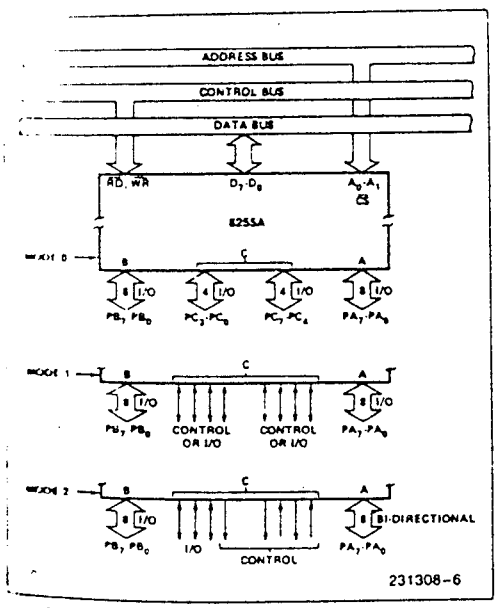



Figure 5. Basic Mode Definitions and Bus Interface

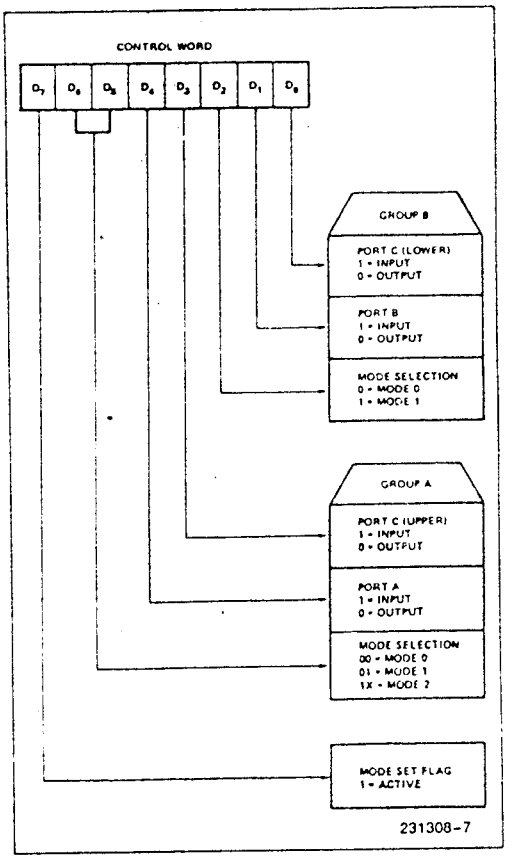



Figure 6. Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 8255A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

## Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.

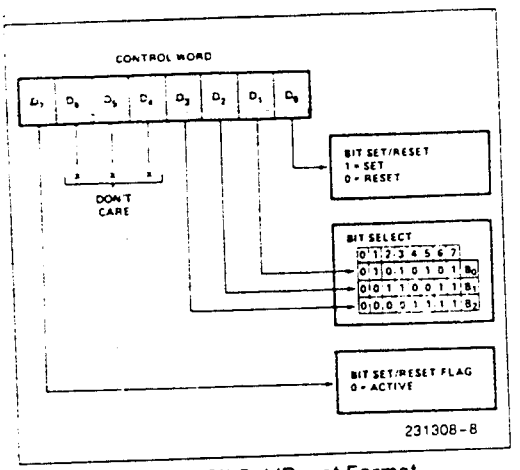



**Figure 7. Bit Set/Reset Format**

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

## Interrupt Control Functions

When the 8255A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the Programmer to disallow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET)—INTE is set—Interrupt enable

(BIT-RESET)—INTE is RESET—Interrupt disable

NOTE:
All Mask flip-flops are automatically reset during mode selection and device Reset.

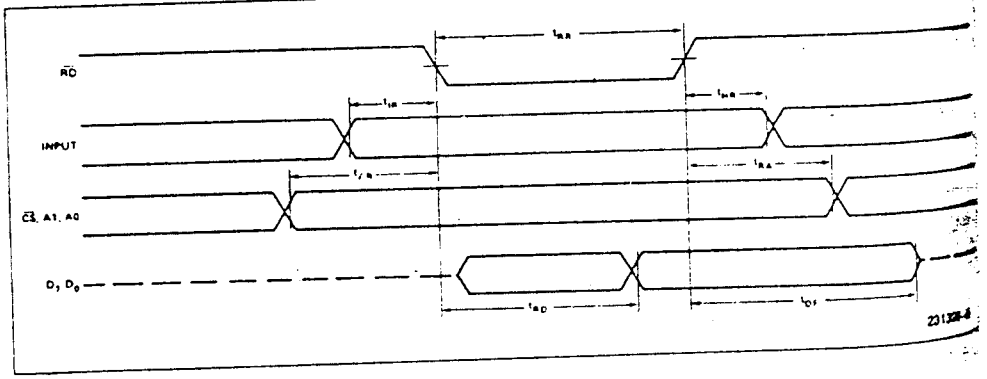
## Operating Modes

**MODE 0 (Basic Input/Output).** This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from the specified port.

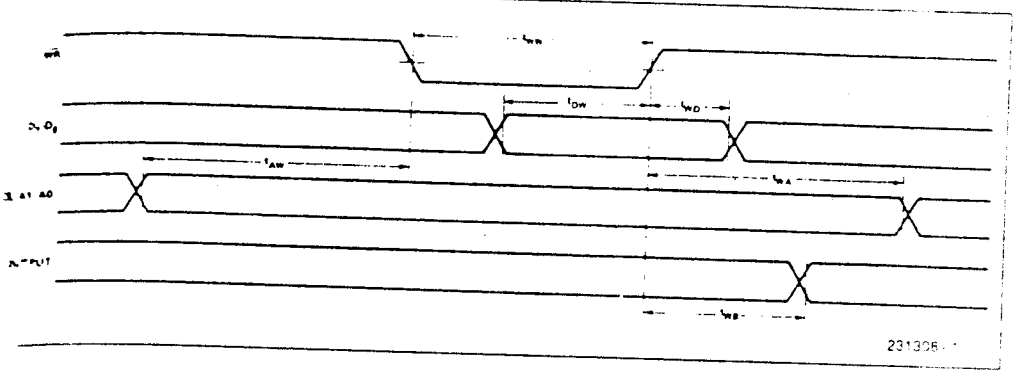
Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.

**MODE 0 (BASIC INPUT)**



## MODE 0 (BASIC OUTPUT)



## MODE 0 PORT DEFINITION

| A | | B | | Group A | | | Group B | |
|---|---|---|---|---|---|---|---|---|
| $D_4$ | $D_3$ | $D_1$ | $D_0$ | Port A | Port C (Upper) | # | Port B | Port C (Lower) |
| 0 | 0 | 0 | 0 | OUTPUT | OUTPUT | 0 | OUTPUT | OUTPUT |
| 0 | 0 | 0 | 1 | OUTPUT | OUTPUT | 1 | OUTPUT | INPUT |
| 0 | 0 | 1 | 0 | OUTPUT | OUTPUT | 2 | INPUT | OUTPUT |
| 0 | 0 | 1 | 1 | OUTPUT | OUTPUT | 3 | INPUT | INPUT |
| 0 | 1 | 0 | 0 | OUTPUT | INPUT | 4 | OUTPUT | OUTPUT |
| 0 | 1 | 0 | 1 | OUTPUT | INPUT | 5 | OUTPUT | INPUT |
| 0 | 1 | 1 | 0 | OUTPUT | INPUT | 6 | INPUT | OUTPUT |
| 0 | 1 | 1 | 1 | OUTPUT | INPUT | 7 | INPUT | INPUT |
| 1 | 0 | 0 | 0 | INPUT | OUTPUT | 8 | OUTPUT | OUTPUT |
| 1 | 0 | 0 | 1 | INPUT | OUTPUT | 9 | OUTPUT | INPUT |
| 1 | 0 | 1 | 0 | INPUT | OUTPUT | 10 | INPUT | OUTPUT |
| 1 | 0 | 1 | 1 | INPUT | OUTPUT | 11 | INPUT | INPUT |
| 1 | 1 | 0 | 0 | INPUT | INPUT | 12 | OUTPUT | OUTPUT |
| 1 | 1 | 0 | 1 | INPUT | INPUT | 13 | OUTPUT | INPUT |
| 1 | 1 | 1 | 0 | INPUT | INPUT | 14 | INPUT | OUTPUT |
| 1 | 1 | 1 | 1 | INPUT | INPUT | 15 | INPUT | INPUT |

## 8255A BASIC OPERATION

| $A_1$ | $A_0$ | $\overline{RD}$ | $\overline{WR}$ | $\overline{CS}$ | Input Operation (READ) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | Port A → Data Bus |
| 0 | 1 | 0 | 1 | 0 | Port B → Data Bus |
| 1 | 0 | 0 | 1 | 0 | Port C → Data Bus |
| | | | | | **Output Operation (WRITE)** |
| 0 | 0 | 1 | 0 | 0 | Data Bus → Port A |
| 0 | 1 | 1 | 0 | 0 | Data Bus → Port B |
| 1 | 0 | 1 | 0 | 0 | Data Bus → Port C |
| 1 | 1 | 1 | 0 | 0 | Data Bus → Control |
| | | | | | **Disable Function** |
| X | X | X | X | 1 | Data Bus → 3-State |
| 1 | 1 | 0 | 1 | 0 | Illegal Condition |
| X | X | 1 | 1 | 0 | Data Bus → 3-State |

## (RESET)

**Reset.** A "high" on this input clears the control register and all ports (A, B, C) are set to the input mode.

## Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 8255A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 8255A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A—Port A and Port C upper (C7–C4)

Control Group B—Port B and Port C lower (C3–C0)

The Control Word Register can **Only** be written into. No Read operation of the Control Word Register is allowed.

## Ports A, B, and C

The 8255A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255A.

**Port A.** One 8-bit data output latch/buffer and one 8-bit data input latch.

**Port B.** One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

**Port C.** One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

# 27256
# 256K (32K x 8) PRODUCTION AND UV ERASABLE PROMS

- New Quick-Pulse Programming™ Algorithm for Plastic P27256
  - 4 Second Programming
  - Int$_e$ligent Programming™ Algorithm Compatible
- Fast Access Time
  - 170 ns D27256-1
  - 200 ns P27256-2
- Int$_e$ligent Identifier™ Mode
- Plastic Production P27256 is Compatible with Auto-Insertion Equipment
- Moisture Resistant
- Industry Standard Pinout . . . JEDEC Approved . . . 28 Lead Cerdip and Plastic Package

(See Packaging Spec, Order #231369)

The Intel 27256 is a 5V only, 262,144-bit Ultraviolet Erasable (Cerdip)/plastic production (P27256) electrically programmable read-only memory (EPROM). Organized as 32K words by 8 bits, individual bytes can be accessed in less than 170 ns (27256-1). This is compatible with high performance microprocessors, such as the Intel iAPX 186, allowing full speed operation without the addition of performance-degrading WAIT states. The 27256 is also directly compatible with Intel's 8051 family of microcontrollers.

The Plastic P27256 is ideal for high volume production environments where code flexibility is crucial. Plastic packaging is also well-suited to auto-insertion equipment in cost-effective automated assembly lines. Intel's new Quick-Pulse Programming Algorithm enables the P27256 to be programmed within four seconds (plus programmer overhead). Programming equipment which takes advantage of this innovation will electronically identify the EPROM with the help of the int$_e$ligent Identifier and rapidly program it using a superior programming method. The int$_e$ligent Programming Algorithm may be utilized in the absence of such equipment.

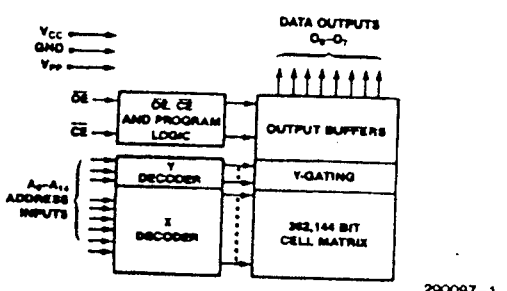
The 27256 enables implementation of new, advanced systems with firmware-intensive architectures. The combination of the 27256's high-density, cost-effective EPROM storage, and new advanced microprocessors offering megabit addressing capability provides designers with opportunities to engineer user-friendly, high capability, high-performance systems.

The 27256's large storage capability of 32 K-bytes enables it to function as a high-density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can be made in a 27256 EPROM directly on a system's memory bus. This permits immediate microprocessor access and execution of software and elminates the need for time-consuming disk accesses and downloads.

On-line control and JEDEC-approved, 28-pin packaging are standard features of all Intel high-density EPROMs. This assures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between nonvolatile memory alternatives.

The 27256 is manufactured using Intel's advanced HMOS®II-E technology.

®HMOS is a patented process of Intel Corporation.



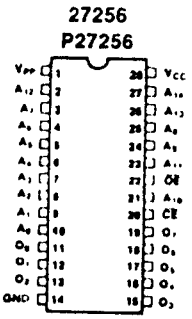

290097-1

Figure 1. Block Diagram

**Pin Names**

| | |
|---|---|
| $A_0$–$A_{14}$ | Addresses |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $O_0$–$O_7$ | Outputs |
| D.U. | Don't Use |
| $\overline{WE}$ | Write Enable |

| 27516 | 27513 | 27512 | 27128A | 2764A 27C64 | 2732A | 2716 |
|---|---|---|---|---|---|---|
| $V_{PP}$ | D.U. | $A_{15}$ | $V_{PP}$ | $V_{PP}$ | | |
| $A_{12}$ | $A_{12}$ | $A_{12}$ | $A_{12}$ | $A_{12}$ | | |
| $A_7$ | $A_7$ | $A_7$ | $A_7$ | $A_7$ | $A_7$ | $A_7$ |
| $A_6$ | $A_6$ | $A_6$ | $A_6$ | $A_6$ | $A_6$ | $A_6$ |
| $A_5$ | $A_5$ | $A_5$ | $A_5$ | $A_5$ | $A_5$ | $A_5$ |
| $A_4$ | $A_4$ | $A_4$ | $A_4$ | $A_4$ | $A_4$ | $A_4$ |
| $A_3$ | $A_3$ | $A_3$ | $A_3$ | $A_3$ | $A_3$ | $A_3$ |
| $A_2$ | $A_2$ | $A_2$ | $A_2$ | $A_2$ | $A_2$ | $A_2$ |
| $A_1$ | $A_1$ | $A_1$ | $A_1$ | $A_1$ | $A_1$ | $A_1$ |
| $A_0$ | $A_0$ | $A_0$ | $A_0$ | $A_0$ | $A_0$ | $A_0$ |
| $O_0$ | $D_0/O_0$ | $O_0$ | $O_0$ | $O_0$ | $O_0$ | $O_0$ |
| $O_1$ | $D_1/O_1$ | $O_1$ | $O_1$ | $O_1$ | $O_1$ | $O_1$ |
| $O_2$ | $O_2$ | $O_2$ | $O_2$ | $O_2$ | $O_2$ | $O_2$ |
| Gnd | Gnd | Gnd | Gnd | Gnd | Gnd | Gnd |




| 2716 | 2732A | 2764A 27C64 | 27128A | 27512 | 27513 | 27516 |
|---|---|---|---|---|---|---|
| $V_{CC}$ | $V_{CC}$ | $V_{CC}$ PGM | $V_{CC}$ PGM | $V_{CC}$ | $V_{CC}$ | |
| $A_8$ | $A_8$ | N.C. | $A_{13}$ | $A_{13}$ | $A_{13}$ | |
| $A_9$ | $A_9$ | $A_8$ | $A_8$ | $A_8$ | $A_8$ | |
| $V_{PP}$ | $A_{11}$ | $A_9$ | $A_9$ | $A_9$ | $A_9$ | |
| $\overline{OE}$ | $\overline{OE}/V_{PP}$ | $A_{11}$ | $A_{11}$ | $A_{11}$ | $A_{11}$ | |
| $A_{10}$ | $A_{10}$ | $\overline{OE}$ | $\overline{OE}$ | $\overline{OE}/V_{PP}$ | $\overline{OE}/V_{PP}$ | |
| $\overline{CE}$ | $\overline{CE}$ | $A_{10}$ | $A_{10}$ | $A_{10}$ | $A_{10}$ | |
| $O_7$ | $O_7$ | $\overline{CE}$ | $\overline{CE}$ | $\overline{CE}$ | $\overline{CE}$ | |
| $O_6$ | $O_6$ | $O_7$ | $O_7$ | $O_7$ | $O_7$ | |
| $O_5$ | $O_5$ | $O_6$ | $O_6$ | $O_6$ | $O_6$ | |
| $O_4$ | $O_4$ | $O_5$ | $O_5$ | $O_5$ | $O_5$ | |
| $O_3$ | $O_3$ | $O_4$ | $O_4$ | $O_4$ | $O_4$ | |
| | | $O_3$ | $O_3$ | $O_3$ | $O_3$ | |

**NOTE:**
Intel "Universal Site"-Compatible EPROM pin configurations are shown in the blocks adjacent to the P27256 pins.

**Figure 2. Cerdip/Plastic DIP Pin Configuration**

# Using the ADC0808/ ADC0809 8-Bit μP Compatible A/D Converters with 8-Channel Analog Multiplexer

National Semiconductor
Application Note 247
Larry Wakeman

## INTRODUCTION

The ADC0808/ADC0809 Data Acquisition Devices (DAD) implement on a single chip most the elements of the standard data acquisition system. They contain an 8-bit A/D converter, 8-channel multiplexer with an address input latch, and associated control logic. These devices provide most of the logic to interface to a variety of microprocessors with the addition of a minimum number of parts.

These circuits are implemented using a standard metal-gate CMOS process. This process is particularly suitable to applications where both analog and digital functions must be implemented on the same chip.

These two converters, the ADC0808 and ADC0809, are functionally identical except that the ADC0808 has a total unadjusted error of $\pm \frac{1}{2}$ LSB and the ADC0809 has an unadjusted error of $\pm 1$ LSB. They are also related to their big brothers, the ADC0816 and ADC0817 expandable 16 channel converters. All four converters will typically do a conversion in ~ 100 μs when using a 640 kHz clock, but can convert a single input in as little as ~ 50 μs.

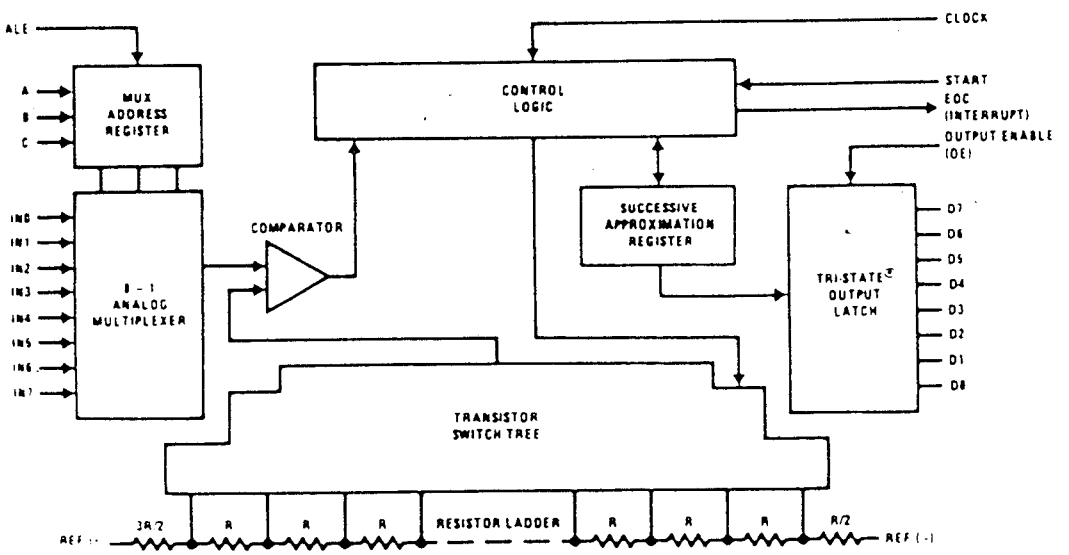
## 1.0 FUNCTIONAL DESCRIPTION

The ADC0808/ADC0809, shown in *Figure 1*, can be functionally divided into 2 basic subcircuits. These two subcircuits are an analog multiplexer and an A/D converter. The multiplexer uses 8 standard CMOS analog switches to provide for up to 8 analog inputs. The switches are selectively turned on, depending on the data latched into a 3-bit multiplexer address register.

The second function block, the successive approximation A/D converter, transforms the analog output of the multiplexer to an 8-bit digital word. The output of the multiplexer goes to one of two comparator inputs. The other input is derived from a 256R resistor ladder, which is tapped by a MOSFET transistor switch tree. The converter control logic controls the switch tree, funneling a particular tap voltage to the comparator. Based on the result of this comparison, the control logic and the successive approximation register (SAR) will decide whether the next tap to be selected should be higher or lower than the present tap on the resistor ladder. This algorithm is executed 8 times per conversion, once every 8 clock periods, yielding a total conversion time of 64 clock periods.

When the conversion cycle is complete the resulting data is loaded into the TRI-STATE® output latch. The data in the output latch can then be read by the host system any time before the end of the next conversion. The TRI-STATE capability of the latch allows easy interface to bus oriented systems.

The operation of these converters by a microprocessor or some control logic is very simple. The controlling device first selects the desired input channel. To do this, a 3-bit channel address is placed on the A, B, C input pins; and the ALE input is pulsed positively, clocking the address into the multiplexer address register. To begin the conversion, the START pin is pulsed. On the rising edge of this pulse the internal registers are cleared and on the falling edge the start conversion is initiated.




TL/H/5623-1

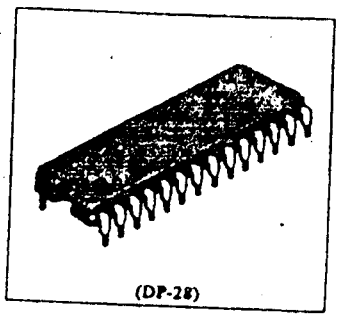
FIGURE 1. ADC0808/ADC0809 Functional Block Diagram

# HM6264P-10, HM6264P-12, HM6264P-15

8192-word x 8-bit High Speed Static CMOS RAM

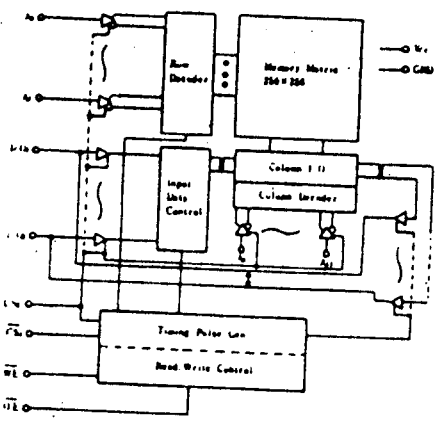
## FEATURES

- Fast access Time — 100ns/120ns/150ns (max.)
- Low Power Standby — Standby: 0.1mW (typ.)
- Low Power Operation — Operating: 200mW (typ.)
- Single +5V Supply
- Completely Static Memory..... No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output
- Standard 28pin Package Configuration
- Pin Out Compatible with 64K EPROM HN482764

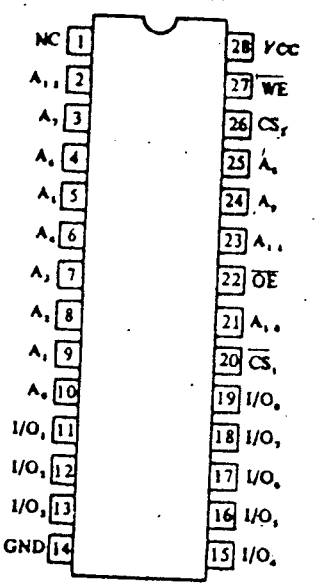


(DP-28)

## BLOCK DIAGRAM



## PIN ARRANGEMENT




(Top View)

## ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Terminal Voltage * | $V_T$ | −0.5 ** to +7.0 | V |
| Power Dissipation | $P_T$ | 1.0 | W |
| Operating Temperature | $T_{opr}$ | 0 to +70 | °C |
| Storage Temperature | $T_{stg}$ | −55 to +125 | °C |
| Storage Temperature (Under Bias) | $T_{bias}$ | −10 to +85 | °C |

* With respect to GND. ** Pulse width 50ns: −3.0V

## TRUTH TABLE

| $\overline{WE}$ | $\overline{CS_1}$ | $CS_2$ | $\overline{OE}$ | Mode | I/O Pin | $V_{CC}$ Current | Note |
|---|---|---|---|---|---|---|---|
| X | H | X | X | Not Selected (Power Down) | High Z | $I_{SB}$, $I_{SB1}$ | |
| X | X | L | X | | High Z | $I_{SB}$, $I_{SB2}$ | |
| H | L | H | H | Output Disabled | High Z | $I_{CC}$, $I_{CC1}$ | |
| H | L | H | L | Read | Dout | $I_{CC}$, $I_{CC1}$ | |
| L | L | H | H | Write | Din | $I_{CC}$, $I_{CC1}$ | Write Cycle (1) |
| L | L | H | L | | Din | $I_{CC}$, $I_{CC1}$ | Write Cycle (2) |

X : Don't care.

Signetics

# 74LS139, S139
# Decoders/Demultiplexers

**Dual 1-of-4 Decoder/Demultiplexer**
***Product Specification***

Logic Products

## FEATURES

- **Demultiplexing capability**
- **Two independent 1-of-4 decoders**
- **Multifunction capability**
- **Replaces 9321 and 93L21 for higher performance**

## DESCRIPTION

The '139 is a high-speed, dual 1-of-4 decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs ($A_0$, $A_1$) and providing four mutually exclusive active LOW outputs ($\overline{0} - \overline{3}$). Each decoder has an active LOW Enable ($\overline{E}$). When $\overline{E}$ is HIGH, every output is forced HIGH. The Enable can be used as the Data input for a 1-of-4 demultiplexer application.

| TYPE | TYPICAL PROPAGATION DELAY (ENABLE AT 2 LOGIC LEVELS) | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74LS139 | 19ns | 6.8mA |
| 74S139 | 6ns | 60mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V ±5%; $T_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | N74S139N, N74LS139N |
| Plastic SO | N74LS139D, N74S139D |

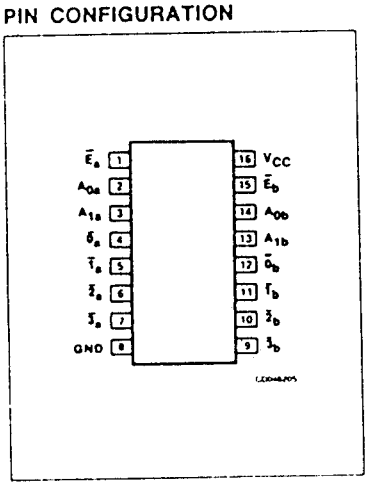
**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

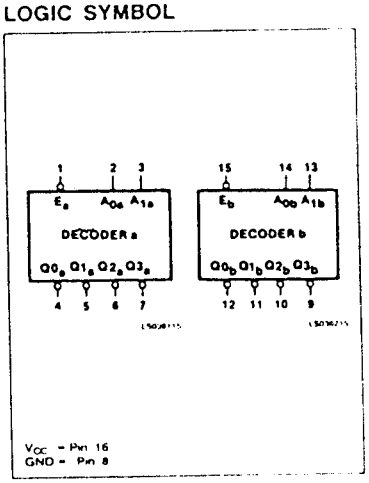
| PINS | DESCRIPTION | 74S | 74LS |
|---|---|---|---|
| All | Inputs | 1Sul | 1LSul |
| All | Outputs | 10Sul | 10LSul |

**NOTE:**
A 74S unit load (Sul) is 50μA $I_{IH}$ and −2.0mA $I_{IL}$, and a 74LS unit load (LSul) is 20μA $I_{IH}$ and −0

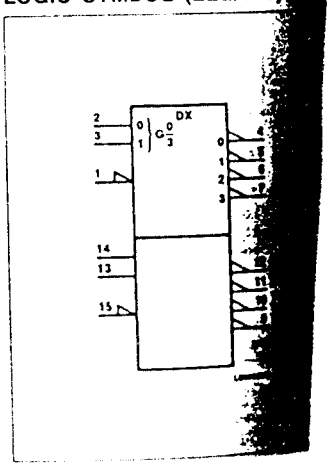
## PIN CONFIGURATION



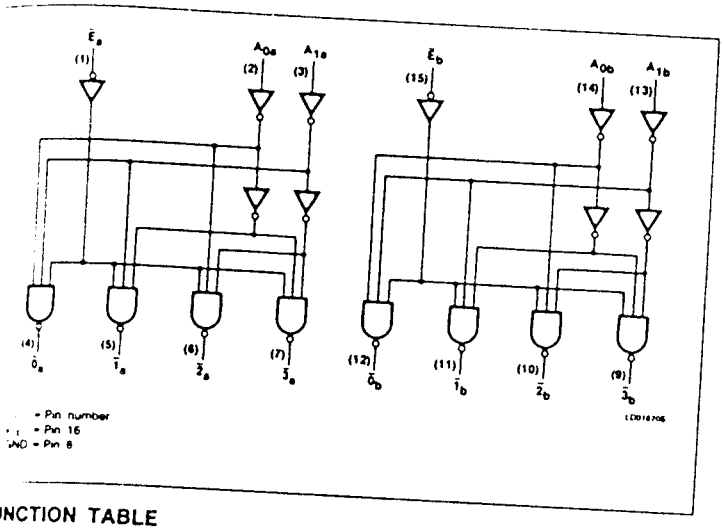

## LOGIC SYMBOL




## LOGIC SYMBOL (EEE/IEC)



## LOGIC DIAGRAM




## FUNCTION TABLE

| INPUTS | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|
| $\bar{E}$ | $A_0$ | $A_1$ | $\bar{0}$ | $\bar{1}$ | $\bar{2}$ | $\bar{3}$ |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | H | L | H | L | H | H |
| L | L | H | H | H | L | H |
| L | H | H | H | H | H | L |

= HIGH voltage level
= LOW voltage level

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| PARAMETER | 74LS | 74S | UNIT |
|---|---|---|---|
| Supply voltage | 7.0 | 7.0 | V |
| Input voltage | −0.5 to +7.0 | −0.5 to +5.5 | V |
| Input current | −30 to +1 | −30 to +5 | mA |
| Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | V |
| Operating free-air temperature range | 0 to 70 | | °C |

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | 74LS | | | 74S | | | UNIT |
|---|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max | |
| Supply voltage | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | V |
| HIGH-level input voltage | 2.0 | | | 2.0 | | | V |
| LOW-level input voltage | | | +0.8 | | | +0.8 | V |
| Input clamp current | | | −18 | | | −18 | mA |
| HIGH-level output current | | | −400 | | | −1000 | μA |
| LOW-level output current | | | 8 | | | 20 | mA |
| Operating free-air temperature | 0 | | 70 | 0 | | 70 | °C |

Signetics

# 7414, LS14
## Schmitt Triggers

**Hex Inverter Schmitt Trigger**
***Product Specification***

Logic Products

### DESCRIPTION

The '14 contains six logic inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional inverters.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transition, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7414 | 15ns | 31mA |
| 74LS14 | 15ns | 10mA |

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V ±5%; $T_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | N7414N, N74LS14N |
| Plastic SO | N74LS14D |

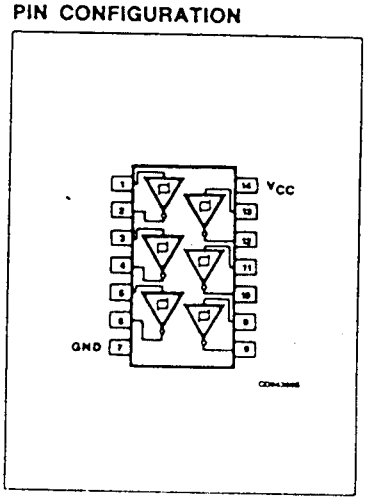
**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Produc Data Manual.

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

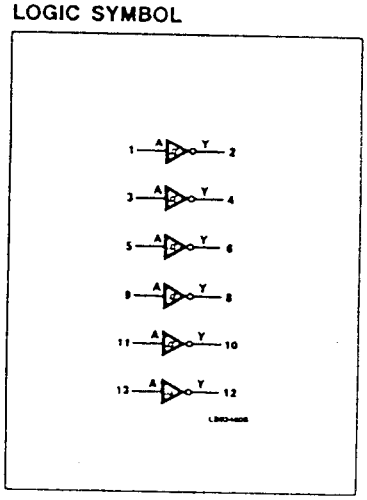
| PINS | DESCRIPTION | 74 | 74LS |
|---|---|---|---|
| A | Inputs | 1ul | 1LSui |
| Y | Output | 10ul | 10LSui |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40μA $I_{IH}$ and −1.6mA $I_{IL}$, and 74LS unit load (LSul 20μA $I_{IH}$ and −0.4mA $I_{IL}$.

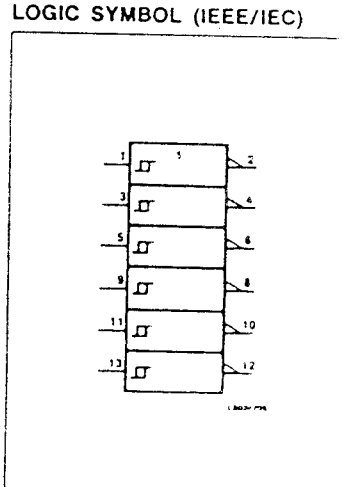
### PIN CONFIGURATION




### LOGIC SYMBOL



### LOGIC SYMBOL (IEEE/IEC)



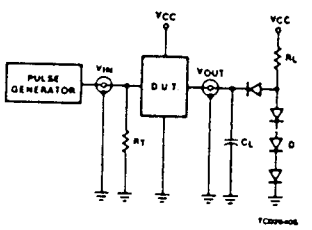
## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| PARAMETER | | 74 | 74LS | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | −0.5 to +7.0 | V |
| $I_{IN}$ | Input current | −30 to +5 | −30 to +1 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | | °C |

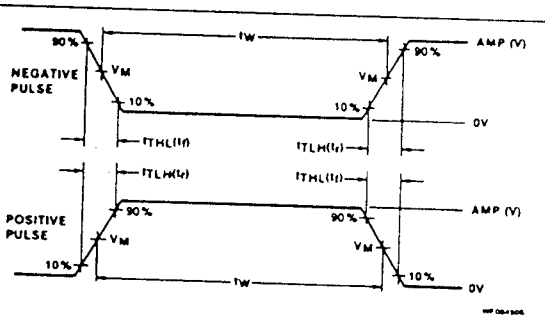
## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | 74 | | | 74LS | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | V |
| $I_{IK}$ | Input clamp current | | | −12 | | | −18 | mA |
| $I_{OH}$ | HIGH-level output current | | | −800 | | | −400 | μA |
| $I_{OL}$ | LOW-level output current | | | 16 | | | 8 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | 0 | | 70 | °C |

## TEST CIRCUITS AND WAVEFORMS




Test Circuit For 74 Totem-Pole Outputs




Input Pulse Definition

DEFINITIONS

$R_L$ = Load resistor to $V_{CC}$; see AC CHARACTERISTICS for value.
$C_L$ = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
$R_T$ = Termination resistance should be equal to $Z_{OUT}$ of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
$t_{TLH}$, $t_{THL}$ Values should be less than or equal to the table entries.

| FAMILY | INPUT PULSE REQUIREMENTS | | | | |
|---|---|---|---|---|---|
| | Amplitude | Rep. Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 74 | 3.0V | 1MHz | 500ns | 7ns | 7ns |
| 74LS | 3.0V | 1MHz | 500ns | 15ns | 6ns |
| 74S | 3.0V | 1MHz | 500ns | 2.5ns | 2.5ns |

5

Signetics

# 7474, LS74A, S74
# Flip-Flops

**Dual D-Type Flip-Flop**
***Product Specification***

**Logic Products**

## DESCRIPTION

The '74 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs; also complementary Q and $\overline{Q}$ outputs.

Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active-LOW inputs and operate independently of the Clock input. Information on the Data (D) input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation. Although the Clock input is level-sensitive, the positive transition of the clock pulse between the 0.8V and 2.0V levels should be equal to or less than the clock-to-output delay time for reliable operation.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7474 | 25MHz | 17mA |
| 74LS74A | 33MHz | 4mA |
| 74S74 | 100MHz | 30mA |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Product Data Manual.

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V ±5%; $T_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | N7474N, N74LS74AN, N74S74N |
| Plastic SO | N741S74A, N74S74D |

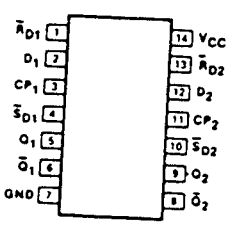
**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Product Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

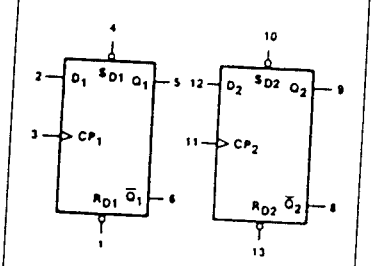
| PINS | DESCRIPTION | 74 | 74S | 74LS |
|---|---|---|---|---|
| D | Input | 1ul | 1Sul | 1LSul |
| $\overline{R}_D$ | Input | 2ul | 3Sul | 2LSul |
| $\overline{S}_D$ | Input | 1ul | 2Sul | 2LSul |
| CP | Input | 2ul | 2Sul | 1LSul |
| Q,$\overline{Q}$ | Outputs | 10ul | 10Sul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40μA $I_{IH}$ and −1.6mA $I_{IL}$, a 74S unit load (Sul) is 50μA $I_{IH}$ and −2.0mA $I_{IL}$, and 74LS unit load (LSul) is 20μA $I_{IH}$ and −0.4mA $I_{IL}$.

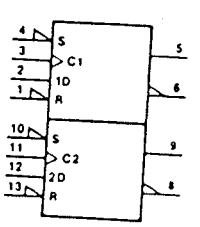
## PIN CONFIGURATION



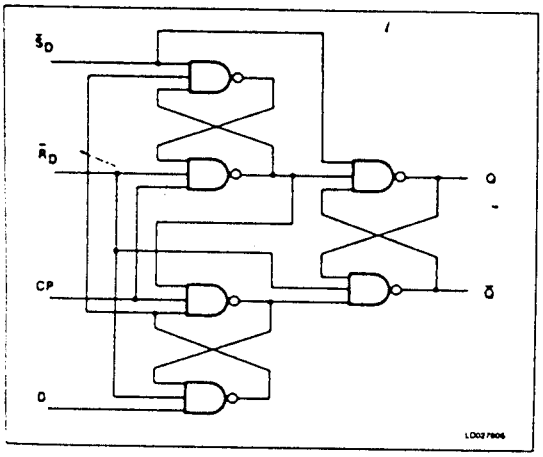

## LOGIC SYMBOL




## LOGIC SYMBOL (IEEE/IEC)



## LOGIC DIAGRAM




## MODE SELECT — FUNCTION TABLE

| OPERATING MODE | INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|---|
| | $\bar{S}_D$ | $\bar{R}_D$ | CP | D | Q | $\bar{Q}$ |
| Asynchronous Set | L | H | X | X | H | L |
| Asynchronous Reset (Clear) | H | L | X | X | L | H |
| Undetermined[1] | L | L | X | X | H | H |
| Load "1" (Set) | H | H | ↑ | h | H | L |
| Load "0" (Reset) | H | H | ↑ | l | L | H |

H = HIGH voltage level steady state.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

**NOTE:**
(1) Both outputs will be HIGH while both $\bar{S}_D$ and $\bar{R}_D$ are LOW, but the output states are unpredictable if $\bar{S}_D$ and $\bar{R}_D$ go HIGH simultaneously.

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| | PARAMETER | 74 | 74LS | 74S | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | 7.0 | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | −0.5 to +7.0 | −0.5 to +5.5 | V |
| $I_{IN}$ | Input current | −30 to +5 | −30 to +1 | −30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | | | °C |

## RECOMMENDED OPERATING CONDITIONS

| | PARAMETER | 74 | | | 74LS | | | 74S | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Nom | Max | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | V |
| $V_{IH}$ | HIGH-level input voltage | 2.0 | | | 2.0 | | | 2.0 | | | V |
| $V_{IL}$ | LOW-level input voltage | | | +0.8 | | | +0.8 | | | +0.8 | V |
| $I_{IK}$ | Input clamp current | | | −12 | | | −18 | | | −18 | mA |
| $I_{OH}$ | HIGH-level output current | | | −400 | | | −400 | | | −1000 | μA |
| $I_{OL}$ | LOW-level output current | | | 16 | | | 8 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | 0 | | 70 | 0 | | 70 | °C |

National Semiconductor

# CD4020BM/CD4020BC 14-Stage Ripple Carry Binary Counters
# CD4040BM/CD4040BC 12-Stage Ripple Carry Binary Counters
# CD4060BM/CD4060BC 14-Stage Ripple Carry Binary Counters

## General Description

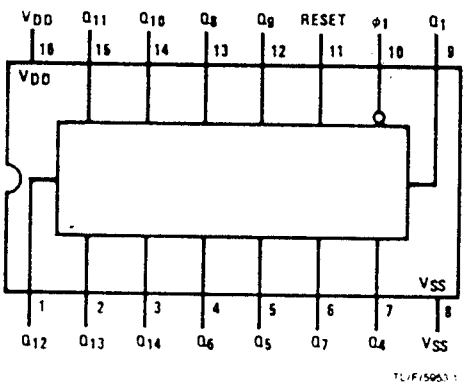
The CD4020BM/CD4020BC, CD4060BM/CD4060BC are 14-stage ripple carry binary counters, and the CD4040BM/CD4040BC is a 12-stage ripple carry binary counter. The counters are advanced one count on the negative transition of each clock pulse. The counters are reset to the zero state by a logical "1" at the reset input independent of clock.

## Features

| | |
|---|---|
| ■ Wide supply voltage range | 1.0 V to 15 V |
| ■ High noise immunity | 0.45 $V_{DD}$ (typ.) |
| ■ Low power TTL compatibility | fan out of 2 driving 74L or 1 driving 74LS |
| ■ Medium speed operation | 8 MHz typ. at $V_{DD}$ = 10 V |
| ■ Schmitt trigger clock input | |

## Connection Diagrams Dual-In-Line Packages/Top Views

CD4020BM/CD4020BC

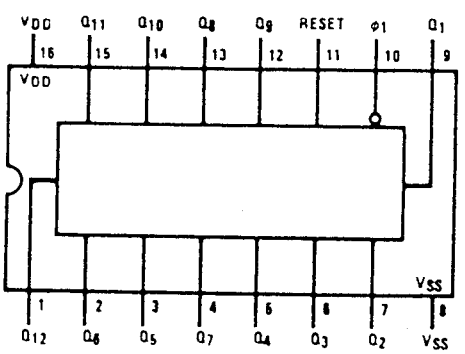



TL/F/5063-1

Order Number CD4020BMJ, CD4020BCJ, CD4040BMJ, CD4040BCJ, CD4060BMJ or CD4060BCJ
See NS Package J16A

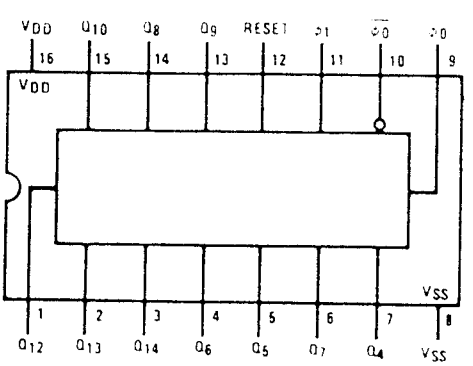
Order Number CD4020BMN, CD4020BCN, CD4040BMN, CD4040BCN, CD4060BMN or CD4060BCN
See NS Package N16E

CD4040BM/CD4040BC



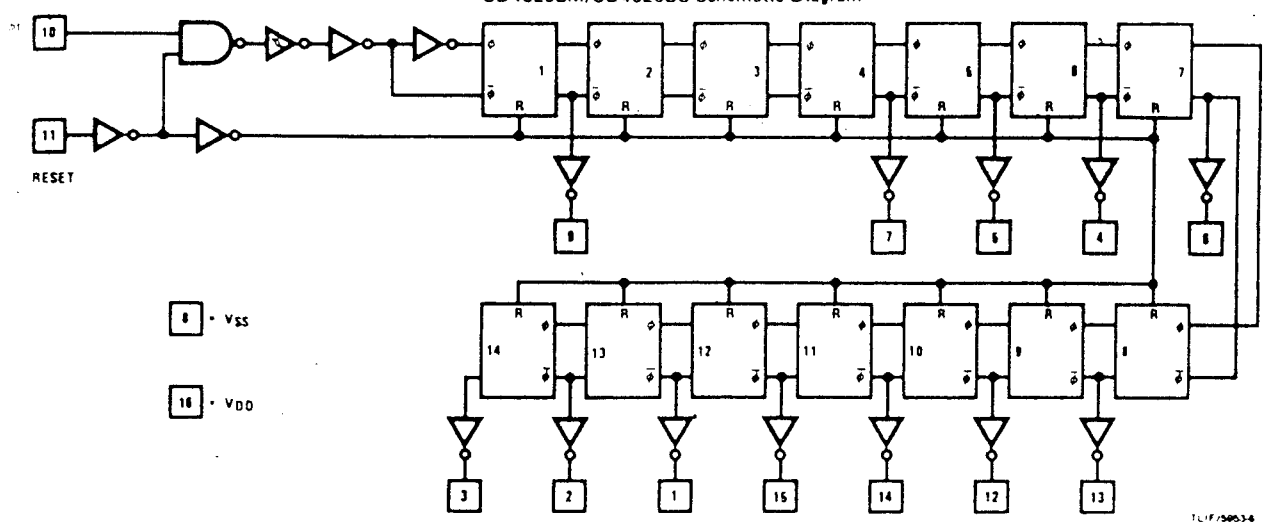

TL/F/5063-2

CD4060BM/CD4060BC

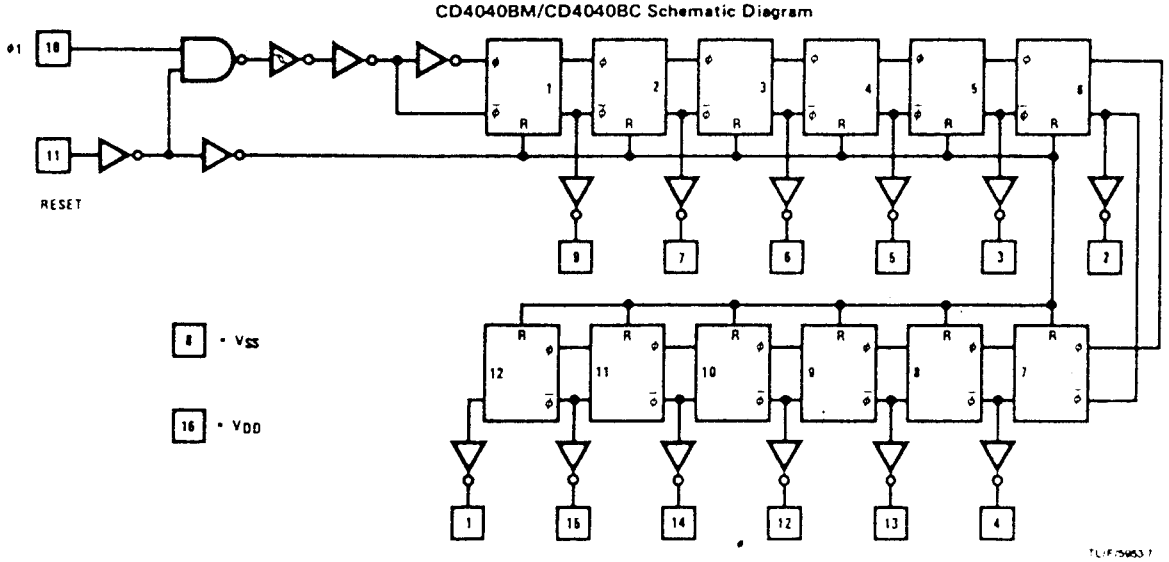


## Schematic Diagrams

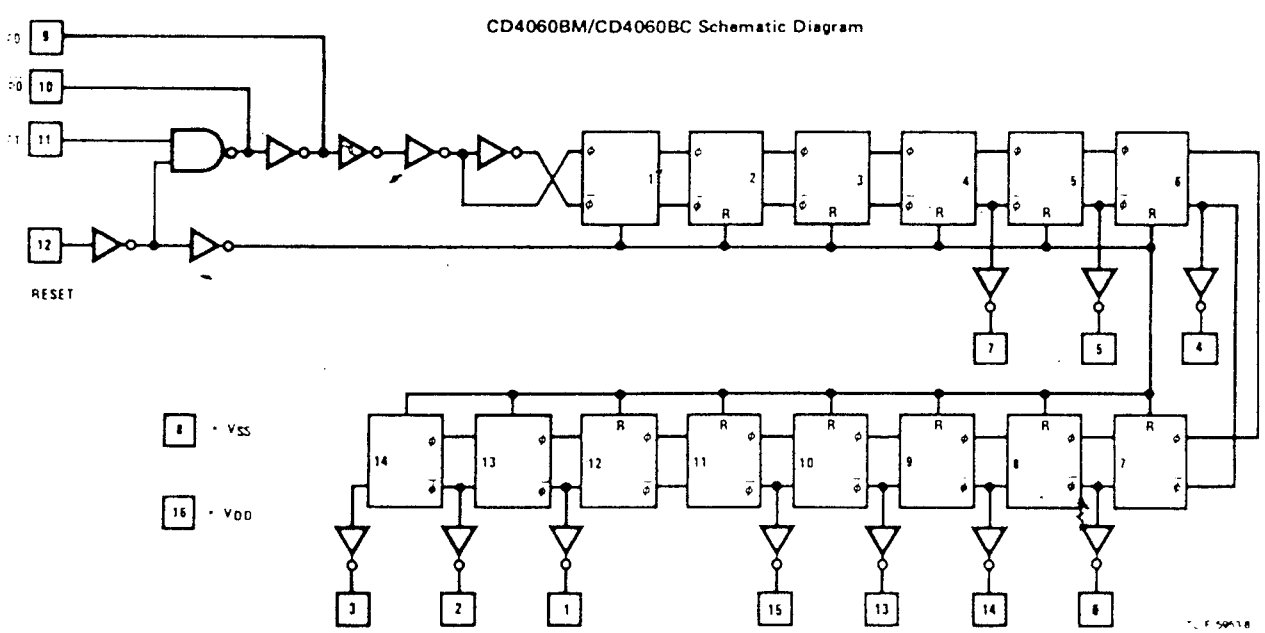
CD4020BM/CD4020BC Schematic Diagram




CD4040BM/CD4040BC Schematic Diagram




CD4060BM/CD4060BC Schematic Diagram



# BIBLIOGRAPHY


1. ZILOG 80 MICROPROCESSOR DATA BOOK
2. B.L. THEREJA, "Introduction to Electrical and Electronics Engineering"
3. Ramesh S.Goankar -"Microprocessor architecture Programming and applications"
4. ALBERT PAUL MALVINO and DONALD P. LEACH "Digital Principles and applications".
5. LED Indicators and Displays, Applications Hand book.
6. TTL Data Manual
7. Linear IC Manual
8. CMOS Data Manual
9. ADITHIYA P.MATHUR "Microprocessors & Applications"
10. Microprocessor Data Hand Book
11. THOMAS T.BARTEE "Digital Fundamentals" Mc Graw Hill Edition.