DICOLT

Digital Control System For On Load Tap Changer

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CERTIFICATE

This is to certify that the project report entitled

Dicolt - Digital Control System for On Load Tap Changer

has been submitted by

Mr......

In partial fulfilment for the Award of

Bachelor of Engineering

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During the Academic Year 1992-'93

Guide *Head of the Department*

Certified that the candidate was Examined by us in the project work Viva-Voce Examination held on..... *and the University Register No. was*.....

Internal Examiner *External Examiner*

" It is not by discoveries only, and the registration of them by learned societies, that science is advanced. The true seat of science is not in the volumes of Transactions, but in the living mind..."

James Clerk Maxwell(1831-1879)
In Grove's " Correlation of Physical Forces"

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SYNOPSIS

D I C O L T - a project sponsored by Messrs. ON LOAD GEARS, MADRAS adds a new dimension to control mechanisms for on-load tap changers.

The existing system built on hard-wired logic, controls the different modes of operation of the on-load tap changer.

The proposed design incorporates a microprocessor unit with additional circuitry for interfacing with the inputs from the system and deliver outputs after processing for system control.

The software developed using assembly language for the system allows a versatile operation of the different modes such as OFF, FOLLOWER, MASTER, and INDEPENDENT. It is a user-friendly and highly interactive system.

This application oriented project introduces processor based control of HT electrical equipment for the first time in the market.

CONTENTS

CHAPTER I

INTRODUCTION

An On Load Tap Changer is a mechanism to provide the required voltage for various loads. This is achieved by changing the tap positions relative to the required voltage. The tap positions are changed by the movement of a shaft, driven by an induction motor.

The control system currently used is electro-mechanical in nature, with logic outputs derived using hard-wiring. The system faces the drawback of not being versatile in its operation for any other additional logic requirement. Also due to hard-wiring, it becomes necessary to use large rotary switches which add up to the system cost.

The prototype designed is versatile in its operation with the processing of logic information taken over by the microprocessor. The inputs are processed through signal conditioners and latches. The information received is made binary in nature and hence makes the processing of it possible through the interfacing ports and the processor. The

processor system used is the 8085 along with its associated hardware.

The electronic control system with the addition of software proves an effective combination in controlling the system as a whole.

CHAPTER -II

TRADITIONAL SYSTEM

The existing system at present is an electro-mechanically controlled system. The description of which is given below. This explanation is to be read in conjunction with the schematic diagram.(included in the enclosure)

2.1. SUPPLY VOLTAGES :

This scheme is mainly designed for an operation of 3 phase, 3 wire system .

3 phase, 3 wire supply is fed to the Motor Circuit from Terminals H85, H86 and H87.

The Control circuit is operating on a 110V A.C. Circuit fed from an auxillary supply transformer of 250 V.A. rating 230V PY/55-0-55V and is provided in the Drive Mechanism Chamber.

The input primary voltage of 230V A.C. for this Auxillary supply Transformer will have to be given at Terminals H83 & H88.

2.2 MOTOR CIRCUIT :

The Motor M gets 3 phase power supply through tapchanger isolation switch TCSIS, set of HRC fuses, overload relay (a1), crank handle

interlock (b8) and through normally open contacts of contactor(c1), for raise directions and for lower directions through normally open contacts of contactor(c2). All the equipment and switches mentioned above are located in the Drive Mechanism.

2.3. **ACTIVATING CIRCUIT :**

The working voltage of this circuit is 110V A.C. which is derived from the Auxillary supply Transformer (AST) . The choice of remote and local operations is possible by the Control Selector Switch CSS - 1 which is housed in the Drive Mechanism Chamber. The motor contactor for raise tap nos. (c1) is energised by the push button 'b1' for local operation and 'b3' for remote operations. The motor contactor for lower tap nos. is energised by push button 'b2' for local operation and 'b4' for remote operations. The supply for the contactor b1/b3 via limit switch 'b6', normally closed contact of 'c2' and through one of the normally open contacts of the stepping contactors c3/c4. One of these stepping contactors c3/c4 will always be under energised conditions, depending on the position of the changeover switch 'b9'. The moment the main spring of the tap changer releases its stored energy,

the changeover switch b9 also changes over to the other side and thereby de-energising C1 or C2 contactors whichever is in operation. This prevents the motor running further until another tapchanging operation is effected through the respective push buttons.

2.4. **INDICATION CIRCUIT :**

During remote operation, in order to indicate the tapchanger operation is in progress a 230V A.C. bulb (TCPL) for visual indication is provided in the Control Panel (CP). This TCPL is connected between the neutral and one of the phases of the Drive Motor(M). In order to indicate the tap position , a set of dial switch is housed in the Drive Mechanism and is wired with a set of resistances. This dial with a set of resistances act like a potentiometer and is connected to a Digital Display Indicator for showing the respective tap numbers. This Digital Display Indicator is housed in the control panel.

2.5. **LOCAL ELECTRIC OPERATION:**

The tap changer can be made operational in local mode by the use of the push buttons b1 & b2 in any direction either Raise/Lower. Only one tap change is possible at a time and fresh impulse

is to be given for next tap change.

At the end of ach tap change, the witch b9 throws over, breaking the supply to the motor reversing contactor coils C1 & C2 as well as the stepping relay C3 & C4 coils. If all the operating push buttons are in the normal (non-operational) state, and if the motor reversing contactors, C1 & C2 have dropped off, then only the complementary stepping relays coil will energise restoring the continuity in the C1 & C2 coil circuit. This ensures "Stepping" which means the ability of the tapchanger to do only one tap change per initiation, irrespective of the length of time for which the initiating action persists.

2.6. REMOTE ELECTRIC OPERATION :

In this system the tap change is made from Remote tap change Control Panel(CP). For remote electric operation remove the temporary supply connection given to the Drive Mechanism Chamber for Local Electric Operation and as well as the shorting links. Keeping the control Selector switch (CSS-1) mounted on tapchanger drive mechanism on Remote' and Sequence Selector Switch' (SSS) mounted on CP on Independent position. Switch on TCSIS and a1' on

the drive mechanism. The unit is then ready for remote electric operation and tap change can be made by pressing the raise push button (b3) or lower push button (b4), as desired.

The operation of tap change takes place similarly as in case of Local Electric Operation.

2.7. PARALLEL CONTROL OPERATION :

When two or more Transformers are connected in parallel, it becomes very essential to maintain the same tapping position of the Transformers in parallel. This is being achieved by a Sequence Selector Switch (SSS) provided in the RTCC (Remote Tap Change Control). This switch has got four positions namely Independent, Off, Follower and Master. When the SSS is kept at "INDEPENDENT" position, it allows the individual tapchanger of the particular transformer to operate. For the position "OFF", it indicates that the entire control circuit of the tapchanging mechanism gets switched off. The remaining two positions, "FOLLOWER" and "MASTER" are used for parallel control of the tapchangers.

When two or more(a maximum of 4 units) Transformers are connected in parallel, it is to be ensured that all the respective tapchangers are in

the same tap number. This is done by sending the Raising or Lowering pulse initiated from the "Master" unit of the RTCC to the "Follower" also and checking up whether they are at the same tap number. Hence when a pulse is given from the "Master" unit, simultaneously all the "Follower" units also get operated.

An interlock system is provided to prevent any further tap changing operations in case the tapchangers in parallel are not in the same tap number. This switch also helps in the manual operation of the tap changer. When the switch is put ON the connections to the motor power supply are opened. When the followers are not in conjunction with the Master the Out of Step Lamp gets ON along with the Buzzer as an indication. After corrections the tapchangers can be operated as usual.

Based on the existing system the simulation board has been designed so as to incorporate every possible signal of it in the processing.

CHAPTER III

SIMULATION BOARD SPECIFICATIONS

The simulation board has been designed for the real time testing of the DICOLT system. The block diagram in figure 1 shows the various sections of the on load tap changer system from which the inputs are derived. The simulation board has the following switches and push buttons to generate the inputs for real time analysis.

PSØ1 TO PSØ3

This switch represents the power supply conditions of the motor. [3-phase supply]

ON - POWER FAILURE

O.R. :

This is to indicate the overloading of the motor.

ON - MOTOR OVERLOAD

I.L. :

It is the interlock for the crank handle which is engaged whenever the handle is inserted.

ON - INTERLOCK ENGAGED

M.T. :

This switch indicates that the current

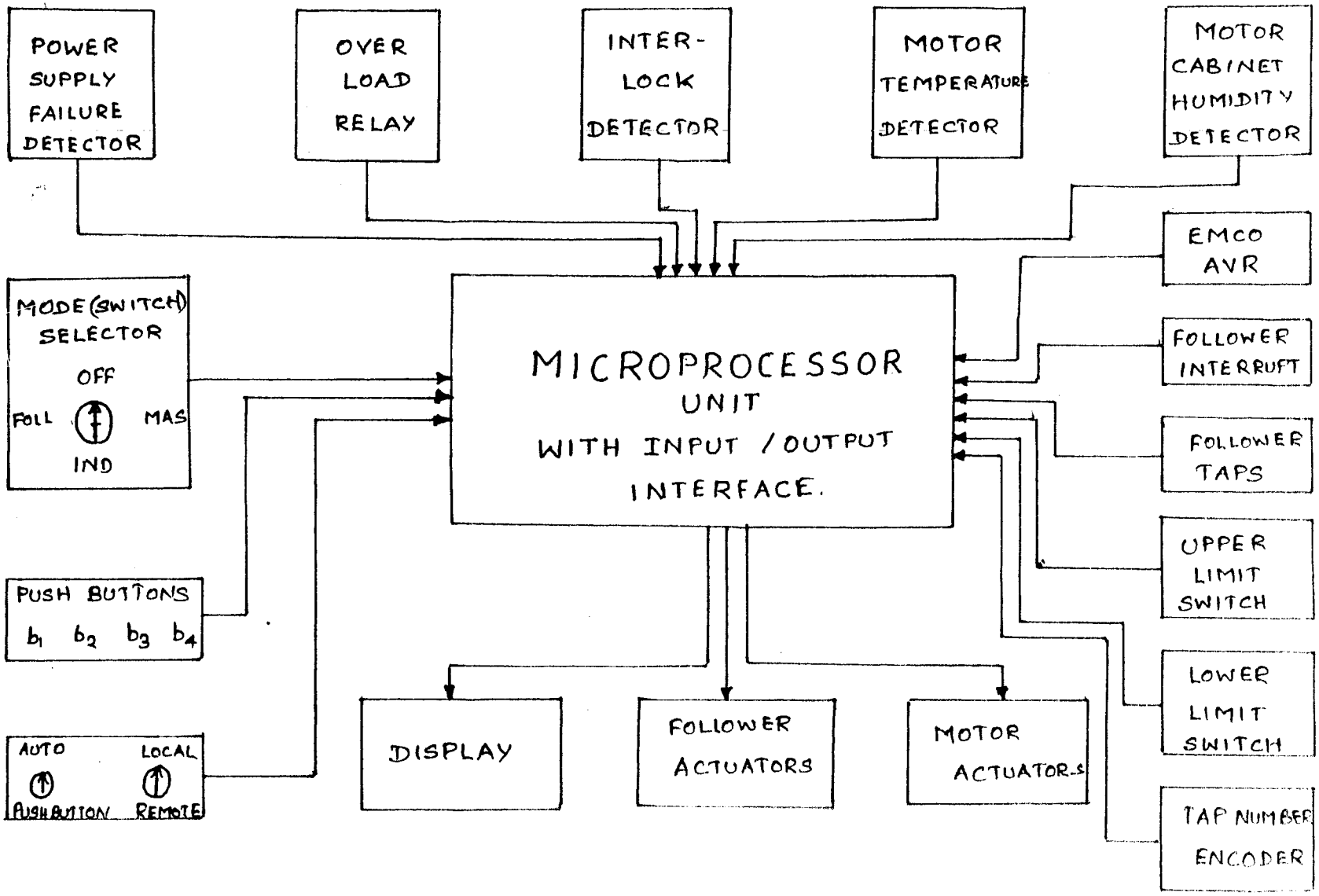

fig. 1. FUNCTIONAL BLOCK DIAGRAM - DICOLT

temperature of motor is higher than the nominal value.

ON - TEMP. HIGHER THAN SPECIFIED VALUE

M.H. :

This is to check the motor cabinet humidity level.

ON - HIGH HUMIDITY LEVEL

OFF - HUMIDITY WITHIN SAFE LIMITS

b1 - b4 :

These are the push button switches used to change the taps. b1 & b2 are used for local operation, b3 & b4 for remote operation.

PRESSED CONDITION :

b1, b3 : RAISE TAP

b2, b4 : LOWER TAP

OFF :

This denotes the OFF condition of the entire system. No operation can be performed in this mode.

ON - SYSTEM IN OFF CONDITION

FOLL :

If the system operates as a follower, it is indicated by the switch.

ON - SYSTEM AS A FOLLOWER

IND :

Master or Independent condition is shown by this switch.

ON - INDEPENDENT MODE

OFF - MASTER MODE

A/PB :

This is a mode switch indicating either the Automatic (or) Push Button mode of operation of the system.

ON - AUTOMATIC MODE

OFF - PUSH BUTTON MODE

L/R :

Local or Remote mode of operation is indicated by the switch.

ON - LOCAL MODE

OFF - REMOTE MODE

F.UP & F.DN :

The control signals for the follower tap changer is indicated through this switch.

ON CONDITION :

F.UP - FOLLOWER TAP RAISED BY 1 STEP

F.DN - FOLLOWER TAP LOWERED BY 1 STEP

E.UP & E.DN :

E denotes EMCO AVR which represents the

automatic operation of the system according to voltage requirement. The switch represents the control signals for the EMCO AVR.

ON CONDITION :

E.UP - TAPS RAISED BY 1 STEP

E.DN - TAPS LOWERED BY 1 STEP

LIMIT MAX & L.MIN :

This switch indicates the upper and lower tap positions of the system.

ON CONDITION :

LIMIT MAX - UPPER LIMIT OF TAPS

L.MIN - LOWER LIMIT OF TAPS

CF C1 & C2 :

CF indicates the contactor feedback after a tap position has been moved correctly.

C1 ON - TAPS ONE STEP HIGHER

C2 ON - TAPS ONE STEP LOWER

ADC 1 - 8 :

ADC - Analog to Digital Converter

The systems tap positions are indicated by the ADC inputs.

ADC 1-4 : Lower order packed BCD.

ADC 5-8 : Higher order packed BCD.

ON - LOGIC 1

OFF - LOGIC 0

FTN1-1 to 5 :

These switches represent the binary code of the follower's tap number.

ON - LOGICAL '1'

OFF - LOGICAL '0'

MODE :

This switch indicates the mode in which the follower tap changer is working.

ON - FOLLOWER

OFF - MASTER

CHAPTER IV

SYSTEM HARDWARE

The hardware section of DICOLT consists of three parts, one is the input interfacing section , the other is the processing section and the third is the output section. The detail of each section is explained below. The input and output section details are to be read in conjunction with the figure 2.

4.1. INPUT INTERFACE SECTION :

This section includes the different processes of signal conditioning, signal selection and noise suppression. The inputs here are derived from the simulation board . The inputs after conditioning are fed to the ports of the programmable peripheral interface chip intel 8255A. The inputs are then processed in the microprocessor.

Input Signal Conditioning

The input voltage from the simulation board though is TTL, the actual voltage from the field lines is 24V. The input voltage of 24V is attenuated to a lower voltage of 5V using a resistive network.

The TTL level voltages of either 5V or 0V are then reconstructed by feeding through inverting Schmitt Triggers (IC 74LS14). The Schmitt Trigger allows to reconstruct the signal levels if they tend to vary about the nominal signal levels. Also interferences due to noise is reduced due to the inclusion of the Schmitts. The output of the Schmitt trigger is either +5V or 0V for respective inverted inputs.

The signals that trigger the interrupt routines of RST7.5,RST6.5, and RST5.5 are fed through Schmitt Trigger circuits with decoupling capacitor connected between Vcc and Ground. The value of capacitance is about 0.01 micro Farad. This causes the inclusion of interference from the power supply to be decoupled from the circuit.

Input Signal Selection

The signals after being conditioned are connected to a latch or directly to the ports of the peripheral interface device - 8255A. The signals connected directly to the ports of 8255A-1 are as follows:

PS01, PS02, PS03	-	POWER SUPPLY FAILURE	A0,A1,A2
O.L	-	OVERLOAD	A3
I.L	-	INTERLOCK	A4

M.T	-	MOTOR TEMPERATURE	A5
M.H	-	MOTOR HUMIDITY	A6
OFF	-	OFF MODE	A7
FOLL	-	FOLLOWER MODE	B0
IND	-	INDEPENDENT MODE	B1
A/PB	-	AUTO / PUSH BUTTON	B2
L/R	-	LOCAL / REMOTE	B3
b1	-	LOCAL TAP RAISE	B4
b2	-	LOCAL TAP LOWER	B5
b3	-	REMOTE TAP RAISE	B6
b4	-	REMOTE TAP LOWER	B7
LIMIT MAX	-	UPPER TAP LIMIT	C0
L MIN	-	LOWER TAP LIMIT	C1
F.UP	-	FOLLOWER TAP RAISE	C2
F.DN	-	FOLLOWER TAP LOWER	C3
CF C1	-	CONTACTOR FEEDBACK	C4
CF C2	-	CONTACTOR FEEDBACK	C5
E.UP	-	ENCO AVR RAISE	C6
E.DN	-	ENCO AVR LOWER	C7

The inputs given to 8255A-2 are through the latches (IC 74LS373). Each of the latch is selected by enabling the data enable (pin number 1) of it. The data enable is an active low signal, i.e. we have to give a 0V signal to the pin inorder

to enable the latch. Once selected, the inputs from that particular latch is passed onto the interface port. The selection of each latch is done by using the outputs of the Decoder (IC 74LS154) .

Operation of the Decoder

The latch selection is done by feeding the outputs of the higher order bits of port C (bits 4,5,6,7) to the decoder inputs of A,B,C & D respectively. Each latch has a seperate code in hexadecimal format for its selection. When the respective selection code for a latch is fed to the decoder inputs, it outputs a low level signal to the pin connected to the data enable of the selected latch. The pins 18 and 19 of the decoder chip IC 74LS154 should be grounded inorder to enable the outputs from it.

The inputs connected to the ports of 8255A-2 are as follows :

		LATCH NO.	DECODER CODE
ADC1 - A/D CONVERTER	A0	L3	3H
ADC2	A1	L3	3H
ADC3	A2	L3	3H
ADC4	A3	L3	3H
ADC5	A4	L3	3H

ADC6	A5	L3	3H
ADC7	A6	L3	3H
ADC8	A7	L3	3H
FT1-1 - FOLLOWER TAP NO.	B0	L4	4H
FT1-2	B1	L4	4H
FT1-3	B2	L4	4H
FT1-4	B3	L4	4H
FTI-5	B4	L4	4H
MODE - FOLLOWER 1 MODE	B5	L4	4H
FT2-1 - FOLLOWER TAP NO.	B0	L5	5H
FT2-2	B1	L5	5H
FT2-3	B2	L5	5H
FT2-4	B3	L5	5H
FT2-5	B4	L5	5H
MODE - FOLLOWER 2 MODE	B5	L5	5H
FT3-1 - FOLLOWER 3 TAP NO.	B0	L6	6H
FT3-2	B1	L6	6H
FT3-3	B2	L6	6H
FT3-4	B3	L6	6H
FT3-5	B4	L6	6H
MODE - FOLLOWER 3 MODE	B5	L6	6H

NOTE : The latches used are transparent.

The Schmitts used are of inverting type.

The interrupts of the microprocessor intel 8085 are used to trigger operations in case we operate the push buttons, EMCO AVR and follower up & down switches.

The interrupts used are the RST7.5, 6.5 and RST5.5. After conditioning through the Schmitt, the inputs of b1,b2,b3 & b4 are connected to the NAND gate (IC 74LS20), the output of it is connected to RST7.5 through a noise suppressing capacitive network. The noise suppressing network is shown in figure 3 . The capacitor acts as a short circuit to the high frequency signals which is typical of noise interference signals.

The inputs of EMCO AVR up and down form the interrupt RST 6.5. The inputs of Follower up & down form the interrupt RST 5.5. These interrupts are used to trigger subroutines for tap changing.

4.2. **PROCESSING SECTION**

This section acts as a sandwich to the input and output sections. It supports the software for actuating the control system according to the inputs. This is supported by the microprocessor intel 8085 chip and its associated hardware devices. The project software has been designed using the PRI 85AD kit manufactured by Precitron, Coimbatore.

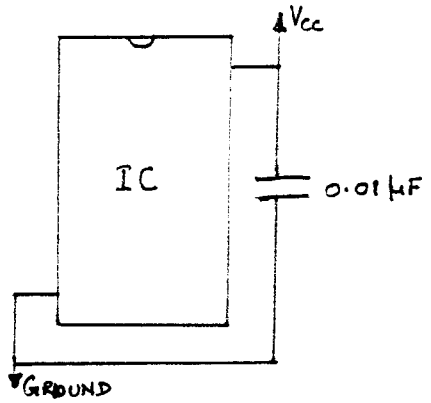

fig. 3.a.

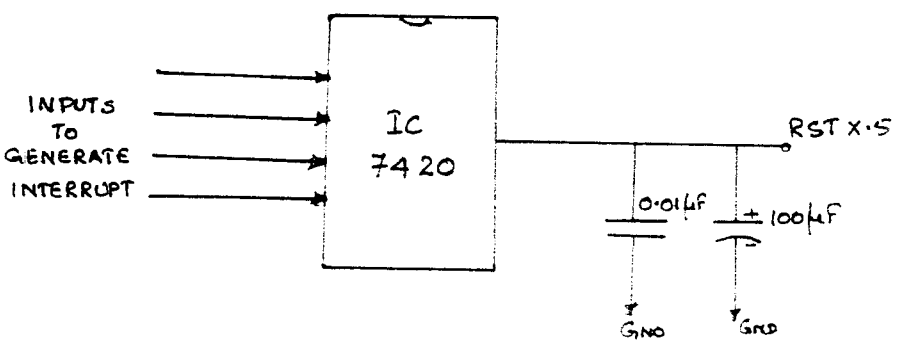

fig. 3.b.

fig. 3.a. POWER LINE DECOUPLING FOR IC.

3.b. INTERFERENCE SUPPRESSOR FOR INTERRUPT SEQUENCE GENERATOR.

The 8085 is an 8-bit general purpose microprocessor capable of addressing 64K of memory. The device has 40 pins, requires +5V single power supply, and can operate with a 3-MHz single phase clock.

Interface Device

Associated with the interfacing devices is the intel 8255A programmable interface device. It is a widely used parallel I/O device. The 8255A has 24 I/O pins that can be grouped primarily in two 8-bit parallel ports: A and B, with the remaining eight bits as port C.

Mode of Operation

The mode of operation used is the I/O mode. The I/O mode is further divided into three modes : Mode 0, Mode 1 and Mode 2. Here the Mode 0 of operation is chosen since the handshaking signals are not required in the process of controlling the tap changer.

The features of operating in Mode 0 are as follows:

1. Outputs are latched.
2. Inputs are not latched.
3. Ports do not have handshake or interrupt capability.

The interrupts obtained from the input section are connected to the respective pins on the trainer kit.

4.3. **OUTPUT SECTION :**

This section delivers the required signals to the various displays , indicators and follower tap changers if connected. It proves to be very effective in giving commands to the operator whenever the requirement arises while processing.

The outputs delivered at the ports of the 8255A 2 are as follows :

Displaying Outputs		LATCH DECODER	CODE
7 SEGMENT LED - 1	A0 to A7	L7	7H
7 SEGMENT LED - 2	A0 to A7	L8	8H
7 SEGMENT LED - 3	A0 to A7	L9	9H
7 SEGMENT LED - 4	A0 to A7	L10	AH

The connections from the output latch to the seven segment LEDs are made as given below

A7	A6	A5	A4	A3	A2	A1	A0
dp	g	f	e	d	c	b	a

The 7 segment LEDs used are of the common cathode configuration (LT 543). Also a driver unit is connected to the output of the latches and then

connected to the displays. The buffer driver used is IC 7407 which is of the open collector type. Using this type of driver, allows to obtain output voltages according to the choice within the limits specified.

The tap numbers and mode of operation is indicated by the 6 LEDs connected to port B of the 8255A -2.

		LATCH	DECODER CODE
FTN - 1	B0	L11	BH
FTN - 2	B1	L11	BH
FTN - 3	B3	L11	BH
FTN - 4	B4	L11	BH
FTN - 5	B5	L11	BH
MODE	B6	L11	BH

The mode bit signifies either Independent of OFF mode of operation of the Follower.

The remaining outputs are signals for the Buzzer, Heater, Motor Raise and Lower and Follower Raise and Lower.

The Buzzer is used to indicate alarm situations. The buzzer used is a d.c. operated buzzer.

Heater bit indicates that the heater is put on due to high humidity levels. An LED indicates that the heater bit is on.

Motor raise and lower (up and down) operate the respective relays which inturn put on the motor for a specific duration in either the Raise/Lower direction and then turnoff when the operation is completed. The raise and lower signals operate relays which in turn drive higher power relays for driving the motor.

Follower raise and lower signals are produced to indicate the Followers to be in step with the master whenever a Raise/Lower is actuated by the Master. This helps in holding the followers IN STEP with the Master.

		LATCH	DECODER CODE
BUZZER	B6	L12	CH
HEATER	B7	L12	CH
MOTOR UP	C0	L12	CH
MOTOR DN	C1	L12	CH
FOLLOWER UP	C2	L12	CH
FOLLOWER DN	C3	L12	CH

CHAPTER V

SOFTWARE EPITOME

DICOLT uses simple, module based logic. The whole logic can be divided into four parts.

(1) Initialization loop

(2) Diagnostics loop

(3) Interrupts loop

(4) Allied Routines

A brief description of the above logics are as follows:

(1) **Initialization loop:-** Here the loop initializes all the output side latches and outputs the follower tap number as 20 decimal.

(2) **Diagnostics loop :-** This loop checks succesively the input side lines i.e. power supply, overload relay, interlock, motor temperature, cabinet humidity, OFF, Master, Independent and Follower conditions, etc., and takes the appropriate action.

(3) **Interrupts loop:-** This can be further subdivided into RST 7.5 - Push button interrupt, RST 6.5 - EMCO AVR interrupt, RST 5.5 - Follower interrupt. The RST 7.5 handles all the push button requirements. The RST 6.5 handles the EMCO AVR requirements, and likewise the RST 5.5 handles follower requirements.

(4) Allied Routines:- These are the subroutines used by the above mentioned loops.

The general flow of the software is is as shown in figure 4.

FLOWCHART - DIAGNOSTIC LOOP.

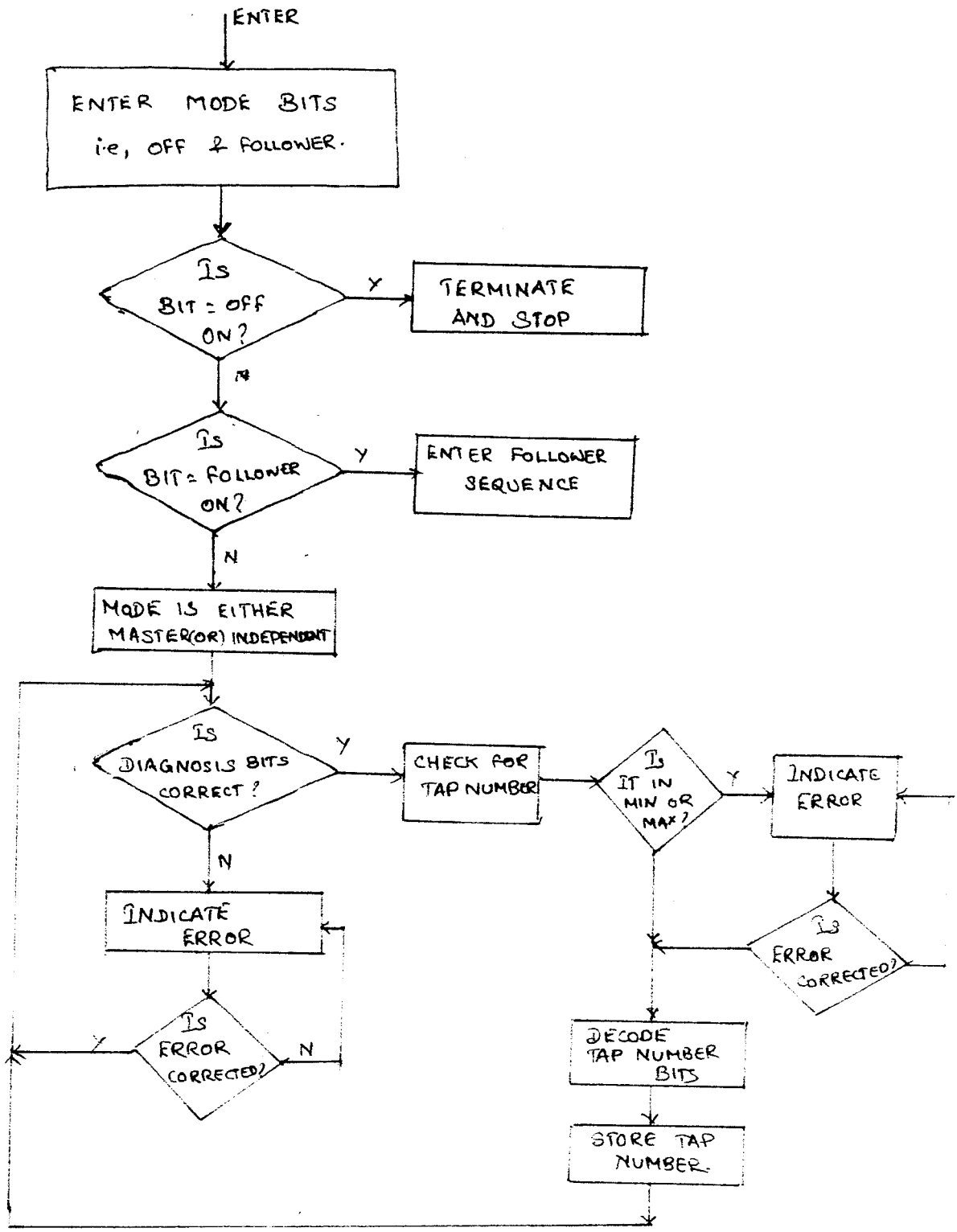

fig. 4.2 - SEQUENCE FOR DIAGNOSIS LOOP.

FLOWCHART - FOLLOWER LOOP

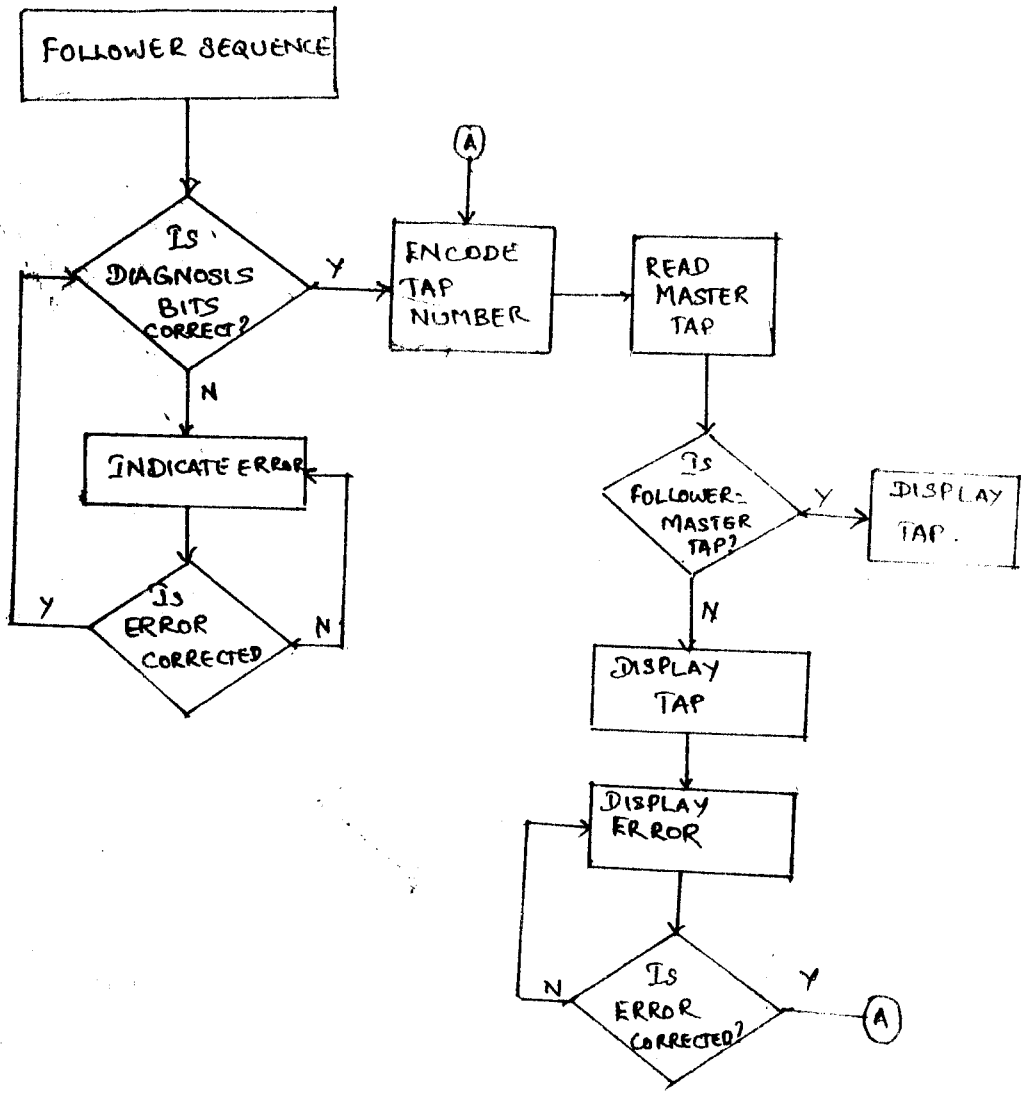

fig.4(b) SEQUENCE FOR FOLLOWER LOOP.

INTERRUPT LOOP

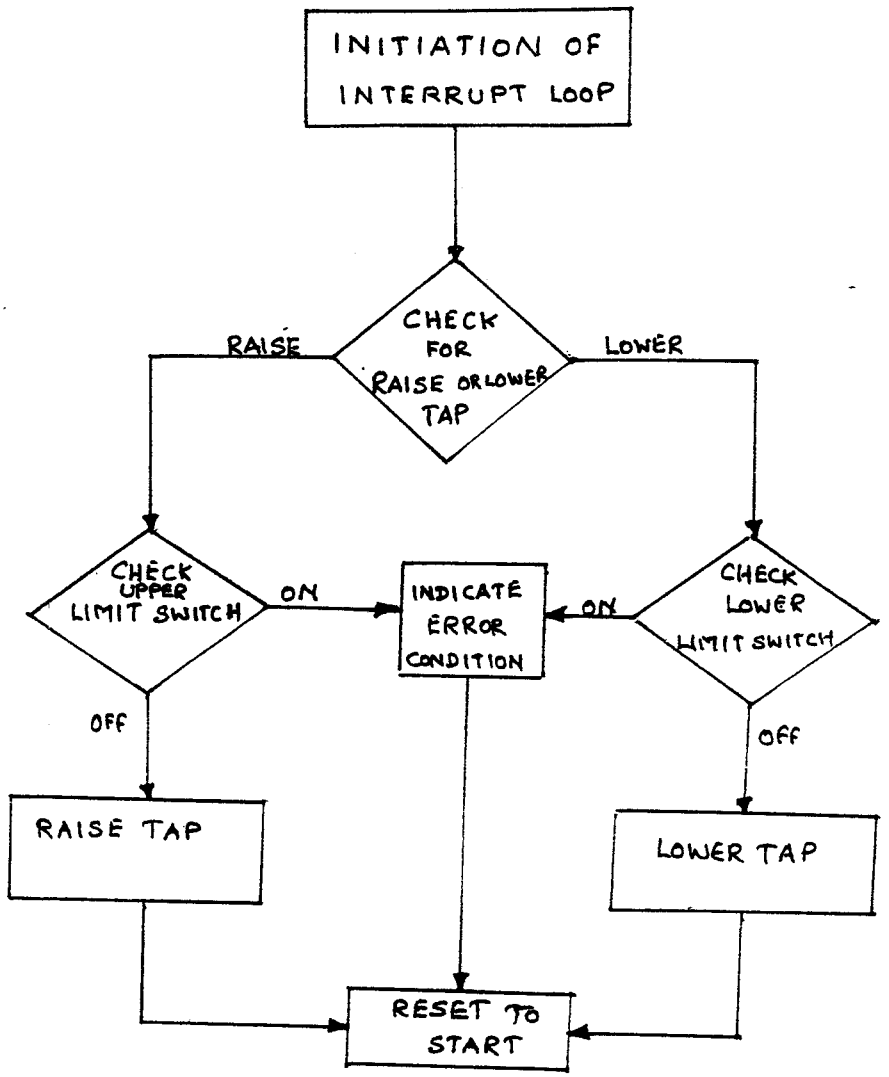

fig. 4.0 : SEQUENCE FOR INTERRUPT LOOP

CHAPTER VI

SOFTWARE DETAILS

```
0000                    CPU     "8085.TBL"    ;CPU TABLE
0000                    HOF     "INT8"        ;HEX FORMAT

8000                ORG 8000H
8000 31FFEF         STARTI:LXI SP,0EFFFH; INITIALIZATION LOOP.
8003 3E80           MVI A,80H
8005 CD0581         CALL CREGII;  SET 55II AS ALL O/P.
8008 3EC0           MVI A,0C0H
800A CD0881         CALL WRPCII; SET MUX L12
800D 3E00           MVI A,00H;RESET ALL L12 BITS
800F CD0B81         CALL WRPBII
8012 3201C0         STA 0C001H; STORE L12 STATUS
8015 3EB0           MVI A,0B0H
8017 CD0881         CALL WRPCII; SET MUX L11
801A 3E14           MVI A,14H; SET O/P TAP # AS INIT
801C CD0B81         CALL WRPBII
801F 3EFF           MVI A,0FFH; SET MUX L15
8021 CD0881         CALL WRPCII

8024 3E3F           MVI A,3FH;     START LOADING CODES
8026 3200C1         STA 0C100H
8029 3E30           MVI A,30H
802B 3201C1         STA 0C101H
802E 3E5B           MVI A,5BH
8030 3202C1         STA 0C102H
8033 3E4F           MVI A,4FH
8035 3203C1         STA 0C103H
8038 3E66           MVI A,66H
803A 3204C1         STA 0C104H
803D 3E6D           MVI A,6DH
803F 3205C1         STA 0C105H
8042 3E7D           MVI A,7DH
8044 3206C1         STA 0C106H
8047 3E07           MVI A,07H
8049 3207C1         STA 0C107H
804C 3E7F           MVI A,7FH
804E 3208C1         STA 0C108H
8051 3E67           MVI A,67H
8053 3209C1         STA 0C109H;    END LOADING CODES

8056 F3             STARTD:DI;     DIAGNOSTICS LOOP.
8057 31FFEF         LXI SP,0EFFFH
805A 3E00           MVI A,00H
805C 3200C0         STA 0C000H;  INITIALIZE STATUS REGISTER
```

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805F 3E9B      MVI A,9BH; SET 55I AS ALL I/P
8061 CD0E81    CALL CREGI
8064 CD1181    CALL RDPAI
8067 320AC0    STA 0C00AH
806A E607      ANI 07H; CHEKING PS1 PS2 PS3
806C FE00      CPI 00H
806E C42881    CNZ POWER
8071 3A0AC0    LDA 0C00AH
8074 E608      ANI 08H; CHEK OVER LOAD RELAY
8076 FE00      CPI 00H
8078 C45081    CNZ ORLOAD
807B 3A0AC0    LDA 0C00AH
807E E610      ANI 10H; CHEK INTERLOCK
8080 FE00      CPI 00H
8082 C49F81    CNZ  ILOCK
8085 3A0AC0    LDA 0C00AH
8088 E620      ANI 20H; CHEK  MOTOR TEMP
808A FE00      CPI 00H
808C C4B681    CNZ  MOTEM
808F 3A0AC0    LDA 0C00AH
8092 E640      ANI 40H; CHEK MOTOR HUMIDITY
8094 FE00      CPI 00H
8096 C4F881    CNZ MOTHUM
8099 3A0AC0    LDA 0C00AH
809C E680      ANI 80H; CHEK OFF CONDITION
809E FE00      CPI 00H
80A0 C44C82    CNZ  OFF
80A3 CD1581    CALL RDPBI; OPR ON PORT B OF 55I
80A6 320AC0    STA 0C00AH
80A9 E601      ANI 01H; CHEK FOLLOWER CONDITION
80AB FE00      CPI 00H
80AD C4EC82    CNZ  FOLLO
80B0 3A0BC0    LDA  0C00BH ; IF FOLLOWER DONT     (NOTE1)
80B3 FEFF      CPI  0FFH;  CHECK FOR
80B5 CAC580    JZ   SKIP;  MASTER OR INDEPENDANT
80B8 3A0AC0    LDA  0C00AH
80BB E602      ANI 02H; CHEK INDEP CONDITION
80BD FE00      CPI 00H
80BF C41983    CNZ  INDE
80C2 CC3283    CZ  MAST
80C5 3E00      SKIP:MVI A,00H;        REFER  NOTE1
80C7 320BC0    STA 0C00BH;            REFER  NOTE1
80CA 3A0AC0    LDA 0C00AH
80CD E604      ANI 04H; CHEK  AUTO  CONDN
80CF FE00      CPI 00H
80D1 C4F483    CNZ AUTO
80D4 3A0AC0    LDA 0C00AH
80D7 FE00      CPI 00H;      CHEK  PB CONDN.
80D9 CCFC83    CZ  PUSBOT
80DC CD1981    CALL RDPCI; OPR ON PORT C OF 55I
80DF 320AC0    STA 0C00AH
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80E2 E601       ANI 01H;  CHEK LT MAX CONDN
80E4 FE00       CPI 00H
80E6 C40484     CNZ MAXLOD
80E9 3A0AC0     LDA 0C00AH
80EC E602       ANI 02H; CHEK LT MIN CONDN
80EE FE00       CPI 00H
80F0 C41584     CNZ  MINLOD
80F3 3A0AC0     LDA 0C00AH
80F6 E603       ANI 03H    ;  CHEK  LIMITS NOT SET CONDN.
80F8 FE00       CPI 00H
80FA CC2684     CZ  NOLOAD
80FD CDA082     CALL  ADC
8100 FB         EI
8101 C35680     JMP   STARTD;   END OF DIAGNOSTICS LOOP

8104 76         HLT
8105  D343       CREGII:OUT 43H;  SUB TO WRITE CONTROL  REG
                                                        II

8107 C9         RET
8108 D342       WRPCII: OUT 42H;  SUB  WRITE  PORT C  II
810A C9         RET
810B D341       WRPBII:OUT 41H;  SUB WRITE PORT B II
810D C9         RET
810E D303       CREGI:OUT 03H;  SUB WRITE CONTROL REG I
8110 C9         RET
8111 DB00       RDPAI:IN  00H; SUB READ & COMPLIMENT PORTAI
8113 2F         CMA
8114 C9         RET
8115 DB01       RDPBI:IN 01H;  SUB READ & COMPLI PORT B I
8117 2F         CMA
8118 C9         RET
8119 DB02       RDPCI:IN 02H; SUB READ & COMPLI PORT C I
811B 2F         CMA
811C C9         RET
811D DB40       RDPAII:IN 40H; SUB READ + COMPLI PORT A II
811F 2F         CMA
8120 C9         RET
8121 DB41       RDPBII:IN 41H; SUB TO READ +  COMPLI  PORT BII
8123 2F         CMA
8124 C9         RET
8125 D340       WRPAII:OUT 40H; SUB WRITE PORT A II
8127 C9         RET
8128 00         POWER:NOP; POWER SUPPLY  CHEK  SUB
8129 0673       MVI B,73H;  O/P  'P'
812B 0E6D       MVI C,6DH;  O/P  'S'
812D 1671       MVI D,71H;  O/P  'F'
812F 1E38       MVI E,38H;  O/P  'L'
8131 CDCD81     CALL  LOADOP
8134 110100     LXI  D,0001H
8137 CD6781     CALL  BUZZ
813A 33         INX SP
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813B 33          INX SP
813C C35680      JMP STARTD


813F 00          DELAY1:NOP; DELAY  SUB. TIME  16BIT IN   DE
                                                      REG.
8140 01FFFF      LXI B,0FFFFH
8143 0B          LOOP:DCX B
8144 79          MOV A,C
8145 B0          ORA B
8146 C24381      JNZ LOOP
8149 1B          DCX D
814A 7B          MOV A,E
814B B2          ORA D
814C C23F81      JNZ  DELAY1
814F C9          RET


8150 00          ORLOAD:NOP;OVER LOAD RELAY SUB
8151 063F        MVI B,3FH; O/P 'O'
8153 0E50        MVI C,50H; O/P 'R'
8155 1671        MVI D,71H; O/P 'F'
8157 1E38        MVI E,38H; O/P 'L'
8159 CDCD81      CALL  LOADOP
815C 110100      LXI  D,0001H
815F CD6781      CALL  BUZZ
8162 33          INX SP
8163 33          INX SP
8164 C35680      JMP STARTD


8167 00          BUZZ:NOP;     BUZZER   SUB( TIMING  IN   DE
                                                   REG PAIR)
8168 3EFF        MVI A,0FFH
816A CD0881      CALL WRPCII;  DE-SELECT MUX.
816D 3A01C0      LDA 0C001H;LOAD  L12  STATUS
8170 F640        ORI 40H; SET   BUZZ   BIT
8172 3201C0      STA 0C001H
8175 CD0B81      CALL  WRPBII
8178 E60F        ANI 0FH;     RESET D- 7,6,5,4 OF ACC.
817A C6C0        ADI 0C0H; SET MUX  L12
817C CD0881      CALL WRPCII
817F 3EFF        MVI A,0FFH
8181 CD0881      CALL WRPCII; DE-SELECT MUX
8184 CD3F81      CALL DELAY1
8187 3A01C0      LDA 0C001H; LOAD L12 STATUS
818A E6BF        ANI 0BFH; RESET BUZZ BIT
818C 3201C0      STA 0C001H
818F CD0B81      CALL WRPBII
8192 E60F        ANI 0FH;  RESET D-7,6,5,4 OF ACC.
8194 C6C0        ADI 0C0H;  SET  MUX L12
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8196 CD0881     CALL  WRPCII
8199 3EFF       MVI A,0FFH
819B CD0881     CALL WRPCII
819E C9         RET


819F 00         ILOCK:NOP;  INTERLOCK  SUB
81A0 0630       MVI B,30H; O/P 'I'
81A2 0E38       MVI C,38H; O/P 'L'
81A4 1671       MVI D,71H; O/P 'F'
81A6 1E38       MVI E,38H; O/P 'L'
81A8 CDCD81     CALL LOADOP
81AB 110100     LXI  D,0001H
81AE CD6781     CALL BUZZ
81B1 33         INX SP
81B2 33         INX SP
81B3 C35680     JMP STARTD


81B6 00         MOTEM:NOP;  MOTOR  TEMP  SUB
81B7 0676       MVI B,76H; O/P 'H'
81B9 0E30       MVI C,30H; O/P 'I'
81BB 163D       MVI D,3DH; O/P 'G'
81BD 1E76       MVI E,76H; O/P 'H'
81BF CDCD81     CALL LOADOP
81C2 110100     LXI D,0001H
81C5 CD6781     CALL BUZZ
81C8 33         INX SP
81C9 33         INX SP
81CA C35680     JMP STARTD


81CD 00         LOADOP:NOP; O/P LOADER  SUB.  I/P  B,C,D,E
                                                REGISTERS
81CE 3E70       MVI A,70H
81D0 CD0881     CALL WRPCII
81D3 78         MOV A,B
81D4 CD2581     CALL WRPAII
81D7 3E80       MVI A,80H
81D9 CD0881     CALL WRPCII
81DC 79         MOV A,C
81DD CD2581     CALL WRPAII
81E0 3E90       MVI A,90H
81E2 CD0881     CALL WRPCII
81E5 7A         MOV A,D
81E6 CD2581     CALL WRPAII
81E9 3EA0       MVI A,0A0H
81EB CD0881     CALL WRPCII
81EE 7B         MOV A,E
81EF CD2581     CALL WRPAII
81F2 3EFF       MVI A,0FFH
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81F4 CD0881     CALL WRPCII
81F7 C9         RET


81F8 00         MOTHUM: NOP ; MOTOR HUM SUB
81F9 0676       MVI B,76H; O/P 'H'
81FB 0E79       MVI C,79H; O/P 'E'
81FD 1677       MVI D,77H; O/P 'A'
81FF 1E78       MVI E,78H; O/P 'T'
8201 CDCD81     CALL LOADOP
8204 110100     LXI D,0001H
8207 CD6781     CALL BUZZ
820A 3EFF       MVI A,0FFH
820C CD0881     CALL WRPCII
820F 3A01C0     LDA 0C001H
8212 F680       ORI 80H ;   SET HEATER BIT
8214 3201C0     STA 0C001H
8217 CD0B81     CALL WRPBII;  SWITCH ON HEATER
821A E60F       ANI 0FH;
821C C6C0       ADI 0C0H;
821E CD0881     CALL WRPCII;  SET MUX L12
8221 3EFF       MVI A,0FFH
8223 CD0881     CALL WRPCII
8226 CD1181     CALL RDPAI
8229 E640       ANI 40H;   CHECK IF HEATER REQD AGAIN
822B FE00       CPI 00H;
822D C2F881     JNZ MOTHUM
8230 3A01C0     LDA 0C001H
8233 E67F       ANI 7FH;    RESET HEAT BIT
8235 3201C0     STA 0C001H
8238 CD0B81     CALL WRPBII;  SWITCH OFF HEATER
823B E60F       ANI 0FH
823D C6C0       ADI 0C0H
823F CD0881     CALL WRPCII;  SET MUX L12
8242 3EFF       MVI A,0FFH
8244 CD0881     CALL WRPCII
8247 33         INX SP
8248 33         INX SP
8249 C35680     JMP STARTD


824C 00         OFF: NOP ; OFF CHECKER SUB
824D F3         DI
824E 3EB0       MVI A,0B0H
8250 CD0881     CALL WRPCII;  SET MUX L11
8253 3E13       MVI A,13H;    SET O/P TAP# AS OFF CONDN
8255 CD0B81     CALL WRPBII
8258 3EFF       MVI A,0FFH
825A CD0881     CALL WRPCII;DE-SELECT  MUX
825D 063F       MVI B,3FH;  O/P 'O'
825F 0E71       MVI C,71H;  O/P 'F'
8261 1671       MVI D,71H;  O/P 'F'
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8263 1E80       MVI E,80H;  O/P '.'
8265 CDCD81     CALL LOADOP
8268 110100     LXI  D,0001H
826B CD6781     CALL BUZZ
826E CD1181     CALL RDPAI
8271 E680       ANI 80H
8273 FE00       CPI 00H
8275 C24C82     JNZ OFF
8278 33         INX SP
8279 33         INX SP
827A C30080     JMP STARTI


827D 00         BCDBIN: NOP; BCD TO BIN CONVERT  SUB.  I/P
                                PACKED BCD ACC. O/P ACC.
827E C5         PUSH B
827F D5         PUSH D
8280 47         MOV B,A
8281 E60F       ANI 0FH
8283 4F         MOV C,A
8284 78         MOV A,B
8285 E6F0       ANI 0F0H
8287 0F         RRC
8288 0F         RRC
8289 0F         RRC
828A 0F         RRC
828B 57         MOV D,A
828C AF         XRA A
828D 1E0A       MVI E,0AH
828F 83         SUM:  ADD E
8290 15         DCR D
8291 C28F82     JNZ SUM
8294 81         ADD C
8295 D1         POP D
8296 C1         POP B
8297 C9         RET


8298 00         LEDCOD: NOP; 7SEG LED CODE GEN. SUB
8299 2100C1     LXI H,0C100H
829C 85         ADD L
829D 6F         MOV L,A
829E 7E         MOV A,M
829F C9         RET


82A0 00         ADC: NOP; ADC READER SUB
82A1 3E90       MVI A,90H ; SET PORT AII AS I/P
82A3 CD0581     CALL CREGII
82A6 3E30       MVI A,30H
82A8 CD0881     CALL WRPCII;  SET MUX L3
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82AB CD1D81     CALL RDPAII
82AE 3202C0     STA 0C002H;  STORE TAP# IN BCD FORMAT
82B1 3EFF       MVI A,0FFH
82B3 CD0881     CALL WRPCII;DE-SELECT  MUX
82B6 3E80       MVI A,80H ; SET PORT AII AS O/P
82B8 CD0581     CALL CREGII
82BB 3A02C0     LDA 0C002H
82BE E6F0       ANI 0F0H
82C0 0F         RRC
82C1 0F         RRC
82C2 0F         RRC
82C3 0F         RRC
82C4 CD9882     CALL LEDCOD
82C7 3203C0     STA 0C003H
82CA 3E80       MVI A,80H
82CC CD0881     CALL WRPCII;  SET MUX L8
82CF 3A03C0     LDA 0C003H
82D2 CD2581     CALL WRPAII; WRITE TAP# ON DISPLAY
82D5 3A02C0     LDA 0C002H
82D8 E60F       ANI 0FH
82DA CD9882     CALL LEDCOD
82DD 3203C0     STA 0C003H
82E0 3E90       MVI A,90H
82E2 CD0881     CALL WRPCII; SET MUX L9
82E5 3A03C0     LDA 0C003H
82E8 CD2581     CALL WRPAII ;     WRITE TAP# ON DISPLAY
82EB C9         RET


82EC 00         FOLLO: NOP; FOLLOWER CHECKER SUB
82ED 3E0E       MVI A, 0EH;  MASK 7.5, 6.5 ONLY
82EF 30         SIM
82F0 CDA082     CALL ADC
82F3 3A02C0     LDA 0C002H;  LOAD TAP# IN BCD FORMAT
82F6 CD7D82     CALL BCDBIN
82F9 F620       ORI 20H;      SET FOLLOWER MODE BIT
82FB 3250C0     STA 0C050H
82FE 3EB0       MVI A,0B0H
8300 CD0881     CALL WRPCII;  SET MUX L11
8303 3A50C0     LDA 0C050H
8306 CD0B81     CALL WRPBII;  WRITE FOLLOWER O/P TAP
8309 3E70       MVI A,70H
830B CD0881     CALL WRPCII; SET MUX L7
830E 3EF1       MVI A,0F1H; O/P  'F.'
8310 CD2581     CALL WRPAII
8313 3EFF       MVI A,0FFH
8315 320BC0     STA 0C00BH
8318 C9         RET
```

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8319 00        INDE:NOP; INDEPENDANT CHEKER SUB
831A 3E09      MVI A,09H; MASK 5.5 ONLY   (CHANGE 0DH  TO
                                          09H AFTER TEST)
                                                (CHANGE)
831C 30        SIM;
831D 3EB0      MVI A,0B0H
831F CD0881    CALL WRPCII; SET MUX L11
8322 3E15      MVI A,15H
8324 CD0B81    CALL WRPBII; WRITE INDEP O/P TAP
8327 3E70      MVI A,70H
8329 CD0881    CALL WRPCII; SET MUX L7
832C 3EB0      MVI A,0B0H; O/P 'I.'
832E CD2581    CALL WRPAII
8331 C9        RET


8332 00        MAST:NOP;  MASTER CHEKER  SUB
8333 3E09      MVI A,09H; MASK 5.5 ONLY (CHANGE 0DH TO 09H
                                              AFTER TEST)
                                                (CHANGE)
8335 30        SIM;
8336 3EB0      MVI A,0B0H
8338 CD0881    CALL WRPCII; SET MUX L11
833B 3E12      MVI A,12H;   LOAD TAP AS MASTER
833D CD0B81    CALL WRPBII
8340 3E70      MVI A, 70H
8342 CD0881    CALL WRPCII; SET MUX L11
8345 3EB7      MVI A,0B7H
8347 CD2581    CALL WRPAII;  O/P 'M.'
834A 3EFF      MVI A,0FFH
834C CD0881    CALL WRPCII;    DE-SELECT THE  MUX
834F  3E82      MVI A,82H;  SET PORT BII  AS  I/P   (START
                                  READING FOLL  TAP NOS)

8351 CD0581    CALL CREGII
8354 3E40      MVI A,40H;  SET MUX L4
8356 CD0881    CALL WRPCII
8359 CD2181    CALL RDPBII ; READ FT#1
835C 3204C0    STA 0C004H
835F 3E50      MVI A,50H;   SET MUX L5
8361 CD0881    CALL WRPCII
8364 CD2181    CALL RDPBII; READ FT#2
8367 3205C0    STA 0C005H
836A 3E60      MVI A,60H ; SET MUX L6
836C CD0881    CALL WRPCII
836F CD2181    CALL RDPBII;  READ FT#3
8372 3206C0    STA 0C006H
8375 3E80      MVI A,80H ; SET PORT BII AS O/P
8377 CD0581    CALL CREGII
837A 3A04C0    LDA 0C004H;  LOAD FT#1
837D 1E30      MVI E,30H;   LOAD O/P LAST SEG AS '1'
837F 2A04C0    LHLD 0C004H
8382 CD9C83    CALL CHEK
8385 3A05C0    LDA 0C005H;  LOAD FT#2
8388 1E5B      MVI E,5BH;   LOAD O/P LAST SEG AS '2'
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838A 2A05C0     LHLD 0C005H
838D CD9C83     CALL CHEK
8390 3A06C0     LDA 0C006H ; LOAD FT#3
8393 1E4F       MVI E,4FH ; LOAD O/P LAST SEG AS '3'
8395 2A06C0     LHLD 0C006H
8398 CD9C83     CALL CHEK
839B C9         RET
839C 00         CHEK:NOP;   FOLLOWER  TAP# CHEKER SUB
839D FE14       CPI 14H;  CHEK IF INIT MODE
839F C2B683     JNZ  TRIPA;  IF NOT IN INIT MODE GOTO TRIPA
83A2 0630       MVI B,30H; O/P 'I'
83A4 0E54       MVI C,54H; O/P 'N'
83A6 1630       MVI D,30H; O/P 'I'
83A8 CDCD81     CALL  LOADOP
83AB 110100     LXI  D,0001H
83AE CD6781     CALL  BUZZ
83B1 33         INX SP
83B2 33         INX SP
83B3 C35680     JMP STARTD
83B6 FE12       TRIPA:CPI 12H; CHEK IF MASTER MODE
83B8 C2CF83     JNZ  TRIPB;  IF NOT IN  MASTER  MODE  GOTO
                                                    TRIPB
83BB 0637       MVI B,37H; O/P 'M'
83BD 0E77       MVI C,77H; O/P 'A'
83BF 166D       MVI D,6DH; O/P 'S'
83C1 CDCD81     CALL LOADOP
83C4 110100     LXI  D,0001H
83C7 CD6781     CALL  BUZZ
83CA 33         INX SP
83CB 33         INX SP
83CC C35680     JMP STARTD
83CF E620       TRIPB:ANI 20H;CHEK IF FOLLOWER MODE
83D1 FE20       CPI 20H
83D3 C0         RNZ;    IF NOT FOLLOWER MODE RETURN
83D4 7D         MOV A,L;       'COMPARE THE
83D5 E61F       ANI 1FH;        MASTER  AND
83D7 6F         MOV L,A;        FOLLOWER
83D8 3A02C0     LDA 0C002H;     TAP NUMBERS.'
83DB CD7D82     CALL BCDBIN;
83DE BD         CMP L;
83DF C8         RZ;
83E0 063F       MVI B,3FH; O/P 'O'
83E2 0E3E       MVI C,3EH; O/P 'U'
83E4 1678       MVI D,78H; O/P 'T'
83E6 CDCD81     CALL LOADOP
83E9 110100     LXI  D,0001H
83EC CD6781     CALL BUZZ
83EF 33         INX SP
83F0 33         INX SP
83F1 C35680     JMP STARTD
83F4 00         AUTO:NOP; AUTOMATIC MODE CHEKER SUB
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```
83F5 20          RIM
83F6 E60F        ANI 0FH;MASK 7.5 ALONE RETAINING OLD  MASK
                                                  SETTINGS

83F8 F60C        ORI 0CH
83FA 30          SIM;       (EXCLUDE  DURING  PROBS)
83FB C9          RET
83FC 00          PUSBOT:NOP; PUSH BUTTON MODE CHEKER SUB
83FD 20          RIM
83FE E60F        ANI 0FH
8400 F60A        ORI 0AH; MASK 6.5 ALONE RETAINING OLD  MASK
                                                  SETTINGS

8402 30          SIM;    (EXCLUDE  DURING  PROBS)
8403 C9          RET
8404 00          MAXLOD:NOP; LOAD O/P WITH LT MAX CONDN
8405 3EA0        MVI A,0A0H
8407 CD0881      CALL WRPCII
840A 3E76        MVI A,76H
840C CD2581      CALL WRPAII
840F 3EFF        MVI A,0FFH
8411 CD0881      CALL WRPCII
8414 C9          RET


8415 00          MINLOD:NOP; LOAD O/P WITH LT MIN CONDN
8416 3EA0        MVI A,0A0H
8418 CD0881      CALL WRPCII
841B 3E38        MVI A,38H
841D CD2581      CALL WRPAII
8420 3EFF        MVI A,0FFH
8422 CD0881      CALL WRPCII
8425 C9          RET
8426 3EA0        NOLOAD:MVI A,0A0H;   CLEAR   LAST  DISPLAY
                                                  SEGMENT.

8428 CD0881      CALL WRPCII
842B 3E00        MVI A,00H
842D CD2581      CALL WRPAII
8430 3EFF        MVI A,0FFH
8432 CD0881      CALL WRPCII
8435 C9          RET


8436 00          RS75:NOP;      RST7.5 PUSH BUTTON INT SUB
8437 11D007      LXI D,07D0H
843A CD0087      CALL  DELAY;   CALL   16 MSEC  DELAY
843D CD1581      CALL RDPBI
8440 320FC0      STA 0C00FH;  STORE AT SOME LOCATION
8443 E6F0        ANI 0F0H; CHECK IF FALSE TRIGGER OF INT
8445 FE00        CPI 00H
8447 C24B84      JNZ TRUE75
844A C9          RET;       IF FALSE TRIGGER  RETURN
844B 3A0FC0      TRUE75:LDA 0C00FH
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```
844E 0F         RRC
844F 0F         RRC
8450 0F         RRC
8451 E61E       ANI 1EH
8453 47         MOV B,A
8454 3A00C0     LDA 0C000H; STORE THE PUSH BUTTON STATUS IN
                                                    STATUS REG
8457 B0         ORA B
8458 3200C0     STA 0C000H
845B 20         RIM
845C 1F         RAR
845D 1F         RAR
845E 1F         RAR; CHEK 7.5 MASKED OR NOT
845F D26384     JNC R7OK; IF NOT MASKED SERVICE 7.5
8462 C9         RET
8463 CD1581     R7OK:CALL RDPBI
8466 E608       ANI 08H; CHEK LOCAL OR REMOTE MODE
8468 FE08       CPI 08H
846A C29884     JNZ  REMO
846D 3A00C0     LDA 0C000H;  LOCAL / CHEKING HERE
8470 E602       ANI 02H
8472 FE02       CPI 02H; CHEK B1
8474 0637       MVI B,37H; O/P 'M'
8476 0E77       MVI C,77H; O/P 'A'
8478 163E       MVI D,3EH; O/P 'U'
847A 1E73       MVI E,73H; O/P 'P'
847C CDCD81     CALL LOADOP
847F CCC384     CZ  ACTUP
8482 3A00C0     LDA 0C000H
8485 E604       ANI 04H
8487 FE04       CPI 04H;  CHEK B2
8489 0637       MVI B,37H; O/P 'M'
848B 0E77       MVI C,77H; O/P 'A'
848D 165E       MVI D,5EH; O/P 'D'
848F 1E54       MVI E,54H; O/P 'N'
8491 CDCD81     CALL LOADOP
8494 CCD284     CZ ACTDN
8497 C9         RET
8498 3A00C0     REMO:LDA 0C000H
849B E608       ANI 08H
849D FE08       CPI 08H;   CHEK  B3
849F 0637       MVI B,37H; O/P 'M'
84A1 0E77       MVI C,77H; O/P 'A'
84A3 163E       MVI D,3EH; O/P 'U'
84A5 1E73       MVI E,73H; O/P 'P'
84A7 CDCD81     CALL LOADOP
84AA CCC384     CZ  ACTUP
84AD 3A00C0     LDA 0C000H
84B0 E610       ANI 10H
84B2 FE10       CPI 10H;  CHEK B4
84B4 0637       MVI B,37H; O/P 'M'
```

```
84B6 0E77       MVI C,77H; O/P 'A'
84B8 165E       MVI D,5EH; O/P 'D'
84BA 1E54       MVI E,54H; O/P 'N'
84BC CDCD81     CALL LOADOP
84BF CCD284     CZ  ACTDN
84C2 C9         RET


84C3 00         ACTUP:NOP; UP ACTIVATOR SUB
84C4 CD1581     CALL RDPBI
84C7 E602       ANI 02H
84C9 FE02       CPI 02H; CHEK IF IN INDEP MODE
84CB C4E184     CNZ SFOLUP; IF NOT INDEP CALL SEND FOLLOWER
                                                        UP
84CE CD4D85     CALL SMUP
84D1 C9         RET


84D2 00         ACTDN:NOP;  DOWN ACTIVATOR SUB
84D3 CD1581     CALL RDPBI
84D6 E602       ANI 02H
84D8 FE02       CPI 02H; CHEK IF IN INDEP MODE
84DA C41785     CNZ SFOLDN; IF NOT INDEP CALL SEND FOLLOWER
                                                      DOWN
84DD CDE585     CALL SMDN
84E0 C9         RET


84E1 00         SFOLUP:NOP; SEND FOLLOWER UP SUB
84E2 3A01C0     LDA 0C001H
84E5 E6C0       ANI 0C0H
84E7 CD0B81     CALL WRPBII
84EA 3A01C0     LDA 0C001H
84ED F604       ORI 04H;  SET FOLL UP BIT
84EF 3201C0     STA 0C001H
84F2 E60F       ANI 0FH
84F4 C6C0       ADI 0C0H
84F6 CD0881     CALL WRPCII
84F9 113900     LXI D,0039H; 30 SEC DELAY
84FC CD3F81     CALL DELAY1
84FF 3A01C0     LDA 0C001H
8502 E6C0       ANI 0C0H
8504 CD0B81     CALL WRPBII
8507 3A01C0     LDA 0C001H
850A E6FB       ANI 0FBH;RESET FOLL UP BIT
850C 3201C0     STA 0C001H
850F E60F       ANI 0FH
8511 C6C0       ADI 0C0H
8513 CD0881     CALL WRPCII
8516 C9         RET
```

```
8517 00          SFOLDN:NOP; SEND FOLLOWER DOWN SUB
8518 3A01C0      LDA 0C001H
851B E6C0        ANI 0C0H
851D CD0B81      CALL WRPBII
8520 3A01C0      LDA 0C001H
8523 F608        ORI 08H;    SET FOLL DN BIT
8525 3201C0      STA 0C001H
8528 E60F        ANI 0FH
852A C6C0        ADI 0C0H
852C CD0881      CALL WRPCII
852F 113900      LXI D,0039H; 30 SEC DELAY
8532 CD3F81      CALL  DELAY1
8535 3A01C0      LDA 0C001H
8538 E6C0        ANI 0C0H
853A CD0B81      CALL WRPBII
853D 3A01C0      LDA 0C001H
8540 E6F7        ANI 0F7H
8542 3201C0      STA 0C001H; RESET FOLL DN BIT
8545 E60F        ANI 0FH
8547 C6C0        ADI 0C0H
8549 CD0881      CALL WRPCII
854C C9          RET

854D 00          SMUP:NOP; SEND MOTOR UP SUB
854E CD1981      CALL RDPCI
8551 1F          RAR;        CHEK LT MAX BIT
8552 D26785      JNC ULOK;   JUMP IF LT MAX BIT NOT SET
8555 0638        MVI B,38H; O/P 'L'
8557 0E78        MVI C,78H; O/P 'T'
8559 1676        MVI D,76H; O/P 'H'
855B 1E30        MVI E,30H; O/P 'I'
855D CDCD81      CALL LOADOP
8560 117300      LXI  D,0073H;  1 MIN  BUZZ  TIME
8563 CD6781      CALL BUZZ
8566 C9          RET
8567 3A01C0      ULOK:LDA 0C001H
856A E6C0        ANI 0C0H
856C CD0B81      CALL WRPBII
856F 3A01C0      LDA 0C001H
8572 F601        ORI 01H; SET MOTOR UP BIT
8574 3201C0      STA 0C001H
8577 E60F        ANI 0FH
8579 C6C0        ADI 0C0H
857B CD0881      CALL WRPCII
857E 117300      LXI D,0073H; 1 MIN DELAY
8581 CD3F81      CALL DELAY1
8584 CD1981      LNOCON:CALL RDPCI
8587 17          RAL
8588 17          RAL
8589 17          RAL
```

```
858A 17          RAL;CHEK CF1 STATUS
858B D4BC85      CNC NOCONT
858E D28485      JNC LNOCON
8591 3A01C0      LDA 0C001H
8594 E6C0        ANI 0C0H
8596 CD0B81      CALL WRPBII
8599 3A01C0      LDA 0C001H
859C E6FE        ANI 0FEH; RESET MOTOR UP BIT
859E 3201C0      STA 0C001H
85A1 E60F        ANI 0FH
85A3 C6C0        ADI 0C0H
85A5 CD0881      CALL WRPCII
85A8 110200      LXI D,0002H
85AB CD3F81      CALL DELAY1; 5 MIN DELAY
85AE CD1981      LNOPEN:CALL RDPCI; CHEK   CF1  OPEN
85B1 17          RAL
85B2 17          RAL
85B3 17          RAL
85B4 17          RAL
85B5 DCD185      CC  NOPEN;  CALL ON CF1 NOT OPEN
85B8 DAAE85      JC LNOPEN
85BB C9          RET

85BC 00          NOCONT:NOP; CF1 NO CONTACT SUB
85BD 0639        MVI B,39H; O/P 'C'
85BF 0E3F        MVI C,3FH; O/P 'O'
85C1 1654        MVI D,54H; O/P 'N'
85C3 1E71        MVI E,71H; O/P 'F'
85C5 CDCD81      CALL LOADOP
85C8 110100      LXI  D,0001H
85CB CD6781      CALL BUZZ
85CE 37          STC
85CF 3F          CMC
85D0 C9          RET

85D1 00          NOPEN:NOP; CF1 BREAK FAIL SUB
85D2 063F        MVI B,3FH; O/P 'O'
85D4 0E73        MVI C,73H; O/P 'P'
85D6 1654        MVI D,54H; O/P 'N'
85D8 1E71        MVI E,71H; O/P 'F'
85DA CDCD81      CALL LOADOP
85DD 110100      LXI D,0001H
85E0 CD6781      CALL BUZZ
85E3 37          STC
85E4 C9          RET

85E5 00          SMDN:NOP; SEND MOTOR DOWN SUB
85E6 CD1981      CALL RDPCI
```

```
85E9 1F         RAR
85EA 1F         RAR
85EB D20086     JNC LLOK
85EE 0638       MVI B,38H; O/P 'L'
85F0 0E78       MVI C,78H; O/P 'T'
85F2 1638       MVI D,38H; O/P 'L'
85F4 1E3F       MVI E,3FH; O/P 'O'
85F6 CDCD81     CALL LOADOP
85F9 117300     LXI  D,0073H
85FC CD6781     CALL  BUZZ
85FF C9         RET
8600 3A01C0     LLOK:LDA 0C001H
8603 E6C0       ANI 0C0H
8605 CD0B81     CALL WRPBII
8608 3A01C0     LDA 0C001H
860B F602       ORI 02H
860D 3201C0     STA 0C001H
8610 E60F       ANI 0FH
8612 C6C0       ADI 0C0H
8614 CD0881     CALL WRPCII
8617 117300     LXI D,0073H
861A CD3F81     CALL DELAY1; 1MIN DELAY
861D CD1981     LINOCO:CALL RDPCI
8620 17         RAL
8621 17         RAL
8622 17         RAL
8623 D4BC85     CNC NOCONT
8626 D21D86     JNC LINOCO
8629 3A01C0     LDA 0C001H
862C E6C0       ANI 0C0H
862E CD0B81     CALL WRPBII
8631 3A01C0     LDA 0C001H
8634 E6FD       ANI 0FDH
8636 3201C0     STA 0C001H
8639 E60F       ANI 0FH
863B C6C0       ADI 0C0H
863D CD0881     CALL WRPCII
8640 110100     LXI D,0001H
8643 CD3F81     CALL DELAY1; 5 MIN DELAY
8646 CD1981     LINOPE:CALL RDPCI
8649 17         RAL
864A 17         RAL
864B 17         RAL
864C DCD185     CC  NOPEN
864F DA4686     JC  LINOPE
8652 C9         RET


8653 00         RS65:NOP;     RST6.5 EMCO AVR INT SUB
8654 01FFFF      LXI B,0FFFFH
8657 CD0087      CALL DELAY;     CALL   525 MSEC  DELAY
```

```
865A CD1981     CALL RDPCI
865D 320FC0     STA 0C00FH; STORE SOMEWHERE
8660 E6C0       ANI 0C0H; CHECK  FOR  FALSE  TRIGGER OF INT
8662 FE00       CPI 00H
8664 C26886     JNZ TRUE65
8667 C9         RET;            RETURN   IF  FALSE  TRIGGER
8668 3A0FC0     TRUE65:LDA 0C00FH
866B 0F         RRC
866C 0F         RRC
866D 0F         RRC
866E 0F         RRC
866F 0F         RRC
8670 E606       ANI 06H
8672 47         MOV B,A
8673 3A00C0     LDA 0C000H; STORE THE AVR  STATUS  IN  THE
                                          STATUS  REGISTER
8676 B0         ORA B
8677 3200C0     STA 0C000H
867A 20         RIM;            CHECK  6.5  MASKED  OR NOT
867B 1F         RAR
867C 1F         RAR
867D D28186     JNC RS6OK;  IF  6.5  NOT  MASKED   SERVICE
                                                    6.5
8680 C9         RET
8681 3A00C0     RS6OK:LDA 0C000H
8684 E602       ANI 02H
8686 FE02       CPI 02H;  CHECK   AVR   UP
8688 0677       MVI B,77H; O/P 'A'
868A 0E78       MVI C,78H; O/P 'T'
868C 163E       MVI D,3EH; O/P 'U'
868E 1E73       MVI E,73H; O/P 'P'
8690 CDCD81     CALL LOADOP
8693 CCC384     CZ  ACTUP
8696 3A00C0     LDA 0C000H
8699 E604       ANI 04H
869B FE04       CPI 04H;        CHECK    AVR   DOWN
869D 0677       MVI B,77H; O/P 'A'
869F 0E78       MVI C,78H; O/P 'T'
86A1 165E       MVI D,5EH; O/P 'D'
86A3 1E54       MVI E,54H; O/P 'N'
86A5 CDCD81     CALL LOADOP
86A8 CCD284     CZ  ACTDN
86AB C9         RET


86AC 00         RS55:NOP;  RST 5.5 FOLLOWER INT SUB
86AD 01FFFF     LXI B,0FFFFH
86B0 CD0087     CALL  DELAY;   525 MSEC  DELAY
86B3 CD1981     CALL RDPCI
86B6 320FC0     STA 0C00FH;    STORE  SOMEWHERE
86B9 E60C       ANI 0CH; CHECK  FOR  FALSE TRIGGER OF INT
```

```
86BB FE00       CPI 00
86BD C2C186     JNZ  TRUE55
86C0 C9         RET;          RETURN   ON FALSE  TRIGGER
86C1 3A0FC0     TRUE55:LDA 0C00FH
86C4 07         RLC
86C5 E618       ANI 18H
86C7 47         MOV B,A
86C8 3A00C0     LDA 0C000H
86CB B0         ORA B
86CC 3200C0     STA  0C000H; STORE   THE   FOL  STATUS  IN
                                          STATUS  REGISTER

86CF 20         RIM
86D0 1F         RAR;       CHECK  IF  5.5 MASKED OR NOT
86D1 D2D586     JNC R5OK;  IF NOT  MASKED SERVICE  5.5
86D4 C9         RET
86D5 3A00C0     R5OK:LDA 0C000H
86D8 E608       ANI 08H
86DA FE08       CPI 08H;     CHECK  FOL UP  CONDN.
86DC 0671       MVI B,71H; O/P 'F'
86DE 0E38       MVI C,38H; O/P 'L'
86E0 163E       MVI D,3EH; O/P 'U'
86E2 1E73       MVI E,73H; O/P 'P'
86E4 CDCD81     CALL LOADOP
86E7 CC4D85     CZ SMUP
86EA 3A00C0     LDA 0C000H
86ED E610       ANI 10H
86EF FE10       CPI 10H;      CHECK   FOL  DN   CONDN.
86F1 0671       MVI B,71H; O/P 'F'
86F3 0E38       MVI C,38H; O/P 'L'
86F5 165E       MVI D,5EH; O/P 'D'
86F7 1E54       MVI E,54H; O/P 'N'
86F9 CDCD81     CALL LOADOP
86FC CCE585     CZ SMDN
86FF C9         RET
8700 00         DELAY:NOP; SMALL  VAR DELAY  SUB   I/P DEL
                                    TIME IN  BC  REG. PAIR

8701 0B         LOOD:DCX B
8702 79         MOV  A,C
8703 B0         ORA  B
8704 C20187     JNZ  LOOD
8707 C9         RET


                          ; RESTART  INT  LOCATIONS
FE06            ORG  0FE06H
FE06 C3AC86     JMP  RS55
FE0C            ORG  0FE0CH
FE0C C35386     JMP  RS65
FE12            ORG  0FE12H
FE12 C33684     JMP  RS75
0000            END
```

0007	A	84D2	ACTDN	84C3	ACTUP
82A0	ADC	83F4	AUTO	0000	B
827D	BCDBIN	8167	BUZZ	0001	C
839C	CHEK	810E	CREGI	8105	CREGII
0002	D	8700	DELAY	813F	DELAY1
0003	E	82EC	FOLLO	0004	H
819F	ILOCK	8319	INDE	0005	L
8298	LEDCOD	861D	LINOCO	8646	LINOPE
8600	LLOK	8584	LNOCON	85AE	LNOPEN
81CD	LOADOP	8701	LOOD	8143	LOOP
0006	M	8332	MAST	8404	MAXLOD
8415	MINLOD	81B6	MOTEM	81F8	MOTHUM
85BC	NOCONT	8426	NOLOAD	85D1	NOPEN
824C	OFF	8150	ORLOAD	8128	POWER
83FC	PUSBOT	86D5	R5OK	8463	R7OK
8111	RDPAI	811D	RDPAII	8115	RDPBI
8121	RDPBII	8119	RDPCI	8498	REMO
86AC	RS55	8653	RS65	8681	RS6OK
8436	RS75	8517	SFOLDN	84E1	SFOLDUP
80C5	SKIP	85E5	SMDN	854D	SMUP
80C5	SKIP	85E5	SMDN	854D	SMUP
80C5	SKIP	85E5	SMDN	854D	SMUP
8056	STARTD	8000	STARTI	828F	SUM
83B6	TRIPA	83CF	TRIPB	86C1	TRUE55
8668	TRUE65	844B	TRUE75	8567	ULOK
8125	WRPAII	810B	WRPBII	8108	WRPCII

CHAPTER VII

TESTING PROCEDURE

1) SET THE TAP NUMBER FIRST

2) SET LIMIT SWITCHES ACCORDINGLY

3) CHECK PS01, PS02, PS03

4) CHECK OR

5) CHECK IL

6) CHECK MT

7) CHECK MH

8) CHECK OFF

9) CHECK FOL

10) CHECK IND

11) SET THE MODE AS MASTER

12) CHECK THE THREE FOLLOWERS FOR THE FOLLOWING MODES :

INITIALIZATION
OFF
INDEPENDANT
FOLLOWER
MASTER

13) SET THE MODE AS INDEPENDANT & CHECK CONDITIONS LISTED UNDER STEP # 12

14) SET THE MODE AS FOLLOWER & CHECK CONDITIONS LISTED UNDER STEP # 12

15) SET THE MODE AS OFF & CHECK CONDITIONS LISTED UNDER STEP # 12

16) SET THE MODE AS OFF & TEST ALL THE INTERRUPTS

17) SET THE MODE AS MASTER AND DO THE FOLLOWING:

SET TO PUSH BUTTON
SET TO LOCAL

TEST b1', b2' INCLUDING LIMITS AND CONTACTERS C1' & C2'.

SET TO REMOTE

TEST b3' & b4' INCLUDING LIMITS AND CONTACTERS
TEST FOLLOWER UP & DOWN INCLUDING LIMITS AND CONTACTERS

CHECK FOLLOWER TRIGGER OUTPUT
CHECK EMCO AVR UP & DOWN INCLUDING LIMITS AND CONTACTERS

18) SET THE MODE AS INDEPENDANT AND CHECK CONDITIONS LISTED UNDER STEP # 17

19) SET AUTO CONDITION AND REPEAT STEPS # 17 & # 18

20) SET THE MODE AS FOLLOWER AND REPEAT STEPS # 17 & # 18

END OF PROCEDURE

Project D I C O L T has been successfully tested under real time simulated conditions using the above test procedure.

CONCLUSION

A year's intriguing work, has made project D I C O L T successful. At this juncture we cannot but help cite Sir. Isaac Newton -

> Knowledge is like a shell,
> I am just a child who picks
> up some of these colourful ones,
> but when I look back there are
> millions others still lying on the
> shore of the "Ocean of knowledge".

The prototype is very much still in its premature state, as a lot of signal conditioning, noise and transient surge suppression has to be done, to make the product reliable. This we are certain that, it will be completed in a short span of time.

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APPENDIX

MICROPROCESSOR - INTEL 8085

The 8085 is an 8-bit general purpose capable of addressing 64K of memory. The device has forty pins, requires a +5V single power supply, and can operate with a 3-MHz single-phase clock. figure A shows the logic pinout of the 8085 microprocessor.

The various signals are grouped as follows: The ADDRESS BUS which has bits A15 to A8 unidirectional and bits A7 to A0 shared along with the data bus which are bidirectional.

The control and status signals are the ALE(Address Latch Enable), which is used at the start of the machine cycle, the Read(active low) and Write (active low), the IO/$\overline{M}$, which is used to differentiate between I/O and memory locations and the S1 and S0 signals, which are used for various other memory and I/O operations.

There are five Interrupt signals that can be used to interrupt a program execution. They are the following:

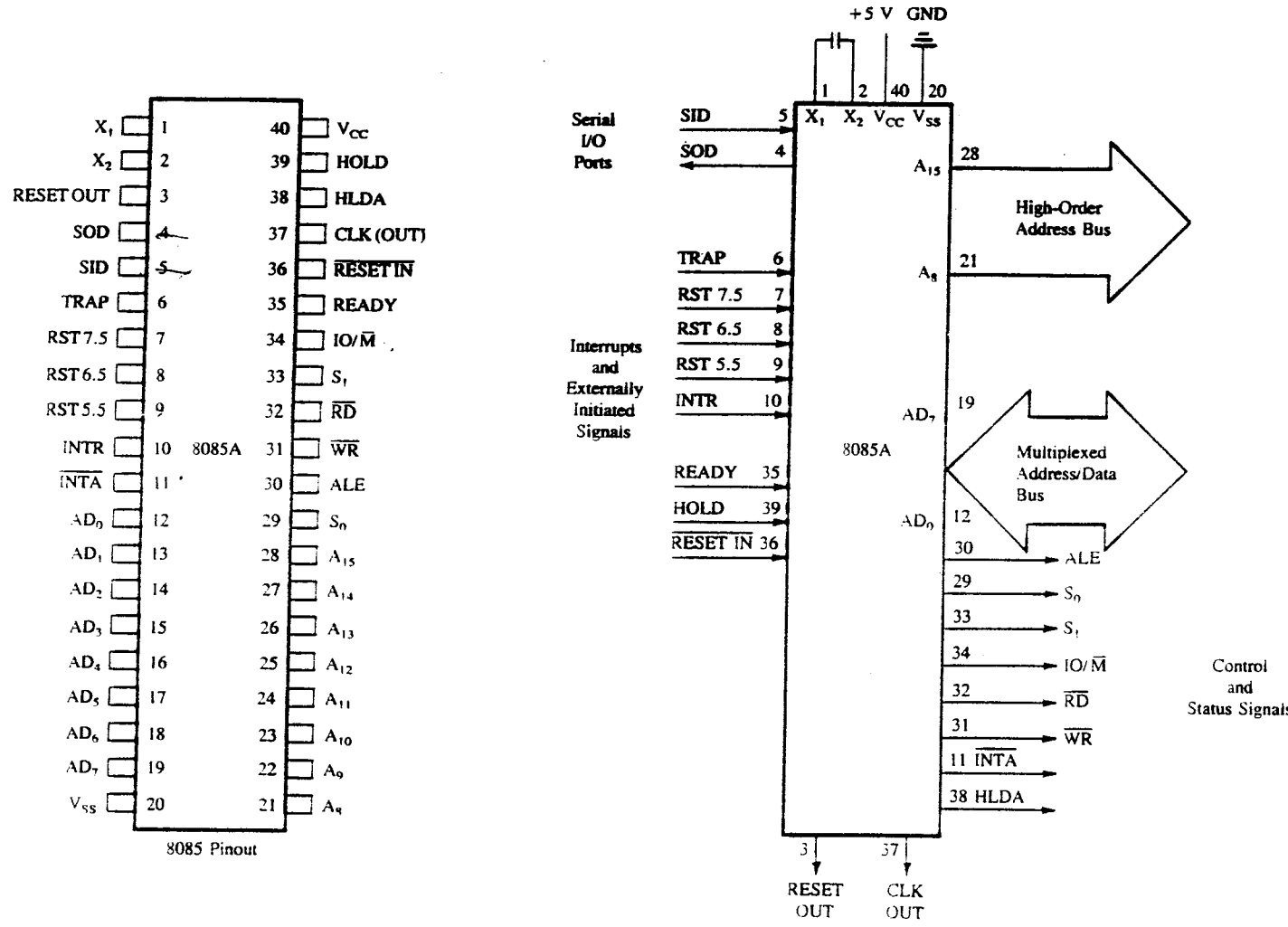


FIGURE 3.1
The 8085 Microprocessor Pinout and Signals

NOTE: The 8085A is commonly known as the 8085.
SOURCE (Pinout): Intel Corporation, *MCS — 80/85 Family User's Manual* (Santa Clara, Calif.: Author, 1979), p. 6-2.

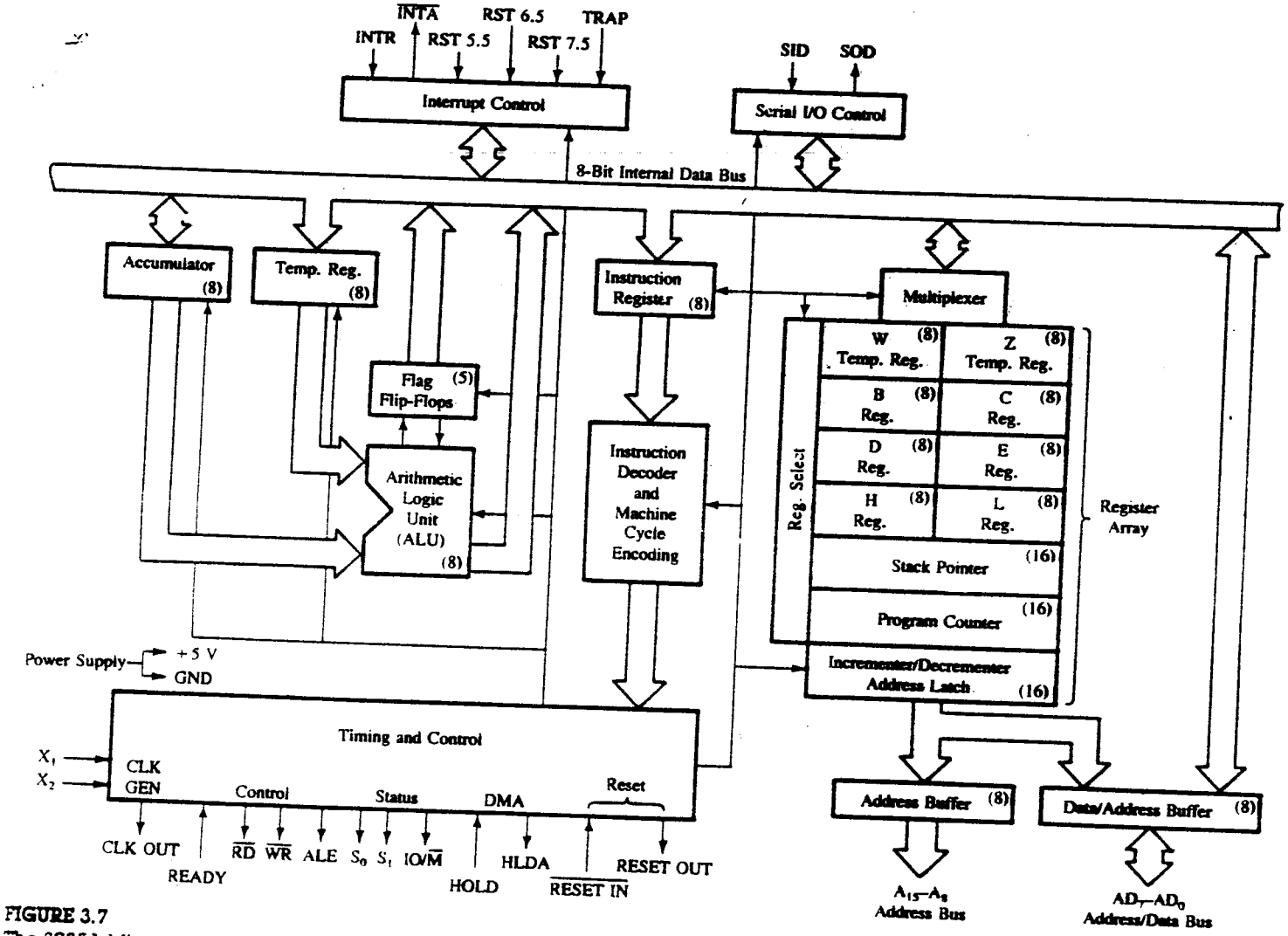


FIGURE 3.7
The 8085A Microprocessor: Functional Block Diagram

NOTE: The 8085A microprocessor is commonly known as the 8085.
SOURCE: Intel Corporation, *MCS — 80/85 Family User's Manual* (Santa Clara, Calif.: Author, 1979), p. 6-1.

* INTR(Input) : Interrupt Request
* $\overline{\text{INTA}}$(Output) : Interrupt Acknowledge
* RST 7.5(Inputs) : Restart Interrupts,
  RST 6.5 Maskable interrupts.
  RST 5.5
* TRAP(Input) : Non maskable, highest priority interrupt.
* HOLD(Input) : Used to indicate that a device such as a DMA controller is requesting the use of the address and data bus.
* HLDA(Output) : Hold Acknowledge.
* READY(Input) : Signal to delay cycles of Read or Write.

ARITHMETIC AND LOGIC UNIT (ALU) :

This unit performs the computing functions; it includes the accumulator, the temporary register, the arithmetic and logic circuits, and five flags.

The flags are affected by the arithmetic and logic operations of the ALU. The various flags are S, Z, AC, P, CY, where

S - Sign flag.

Z - Zero flag.

AC - Auxiliary flag

P - Parity flag

CY - Carry flag

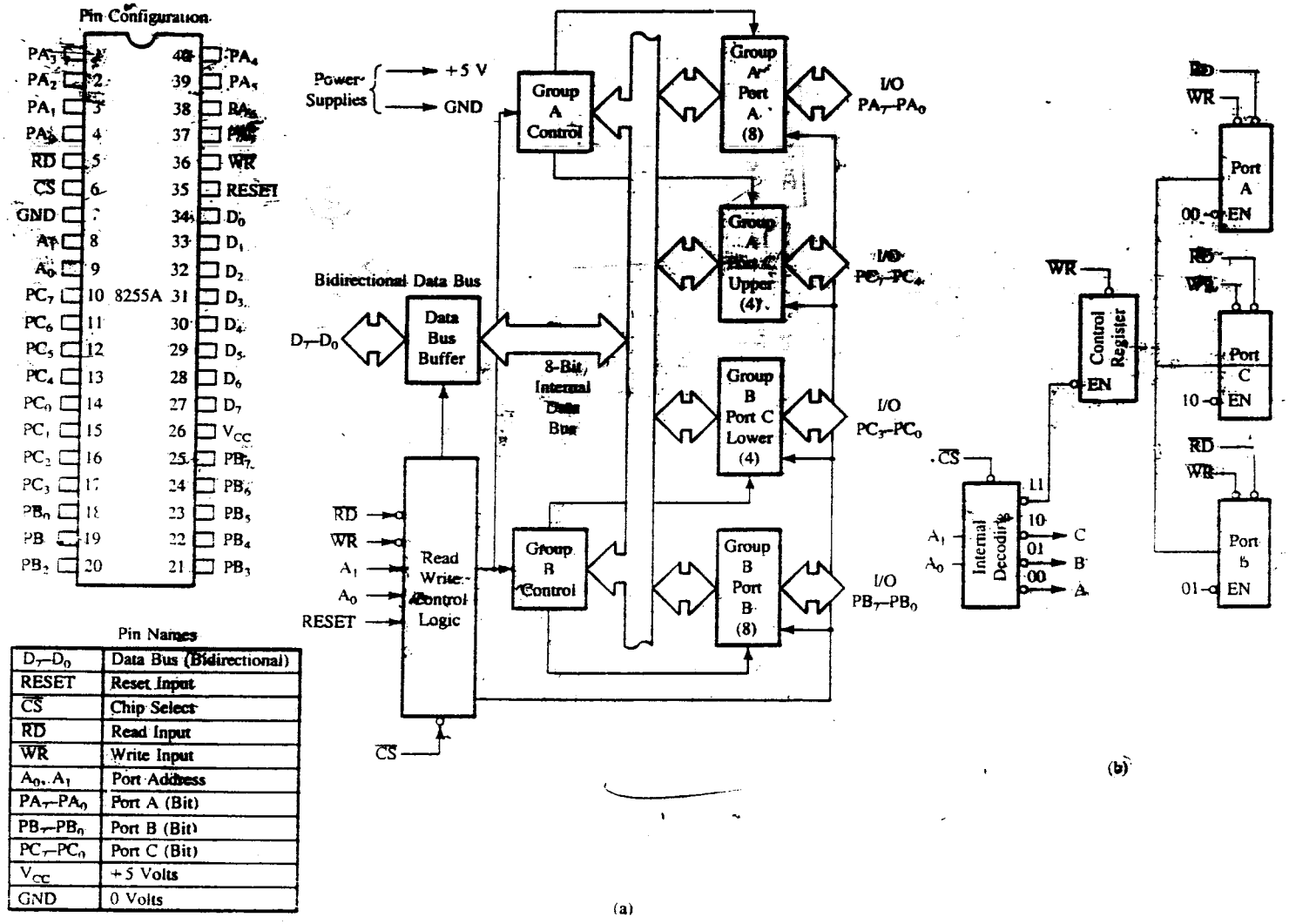
PROGRAMMABLE PERIPHERAL INTERFACE - 8255A

The 8255A widely used, programmable, parallel I/O device. It can be programmed to transfer data under various conditions, from simple I/O to interrupt I/O. It is flexible and versatile in its operation.

It has 24 I/O pins that can be grouped primarily in two 8-bit parallel ports: A and B, with the remaining 8 bits as port C.(divided into two four bit groups with C-upper and C-lower).

The different functions of peripheral interface device 8255A, are classified according to two modes: the Bit Set/Reset(BSR) mode and the I/O mode. The BSR mode is used to set or reset the bits in port C. The I/O mode is further divided into three modes: Mode 0, Mode 1 and Mode 2. In Mode 0, all ports function as simple I/O ports. Mode 1 is a handshake mode whereby ports A or B use bits from port C as handshake signals.

The block diagram in figure C shows ports A, B, C upper and C lower, the data bus buffer, and control logic.



Pin Names	
D_7–D_0	Data Bus (Bidirectional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0, A_1	Port Address
PA_7–PA_0	Port A (Bit)
PB_7–PB_0	Port B (Bit)
PC_7–PC_0	Port C (Bit)
V_{CC}	+5 Volts
GND	0 Volts

FIGURE 15.2
8255A Block Diagram (a) and an Expanded Version of the Control Logic and I/O Ports (b)

SOURCE: Adapted from Intel Corporation, *MCS—80/85 Family User's Manual* (Santa Clara, Calif.: Author, 1979), p. 6-162.

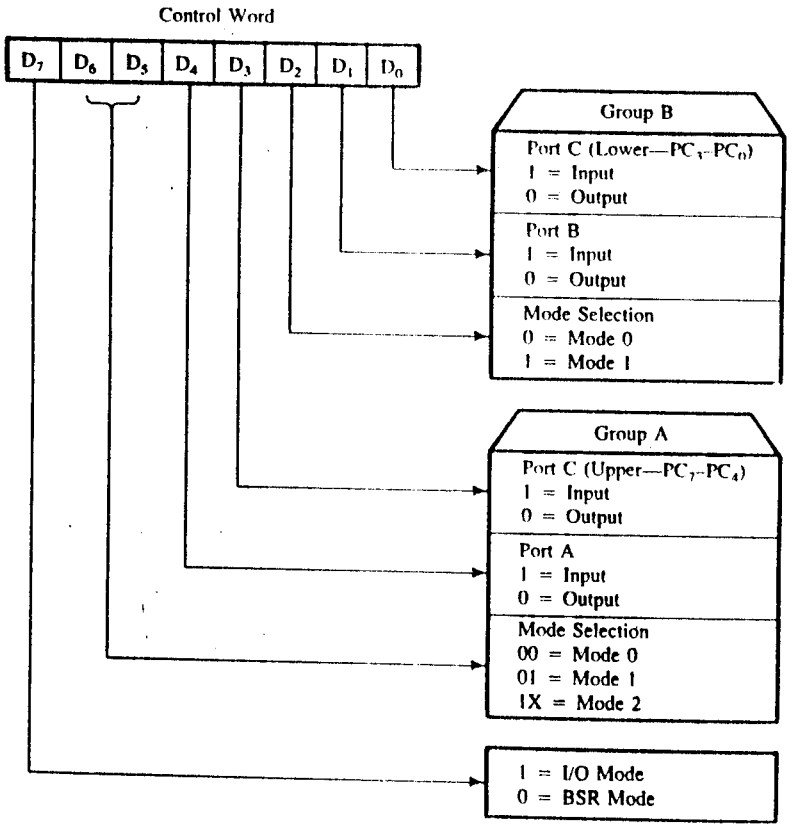


FIGURE 15.4
8255A Control Word Format for I/O Mode

SOURCE: Adapted from Intel Corporation, *Peripheral Design Handbook* (Santa Clara, Calif.: Author, 1981), p. 1-336.

3. Write a program to read the DIP switches and display the reading from port B at port A and from port C_L at port C_U.

Solution

1. Port Addresses This is a memory-mapped I/O; when the address line A_{15} is high, the Chip Select line is enabled. Assuming all don't care lines are at logic 0, the port addresses are as follows:

Port A	=	8000H ($A_1 = 0$, $A_0 = 0$)
Port B	=	8001H ($A_1 = 0$, $A_0 = 1$)
Port C	=	8002H ($A_1 = 1$, $A_0 = 0$)
Control Register	=	8003H ($A_1 = 1$, $A_0 = 1$)

The control word format for I/O mode is as shown in figure D .

The mode used here is the Mode 0 of operation. In this mode each port can be programmed to function as an input port or an output port. The features are as follows:

1. Outputs are latched.
2. Inputs are not latched.
3. Ports do not have handshaking or interrupt capability.

DETAILS OF OTHER CHIPS INCLUDED

1. 74 LS 04 - HEX INVERTER
2. 74 LS 14 - SCHMITT HEX INVERTER BUFFER
3. 74 LS 20 - DUAL 4-INPUT POSITIVE NAND GATE
4. 74 LS 07 - HEX BUFFER 30V O/P
5. 74 LS 154 - 4 TO 16 LINE DECODER
6. 74 LS 373 - OCTAL LATCH WITH 3 STATE O/P

TYPES SN5404, SN54H04, SN54L04, SN54LS04, SN54S04, SN7404, SN74H04, SN74LS04, SN74S04
HEX INVERTERS

REVISED DECEMBER 1983

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

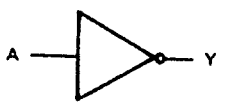
These devices contain six independent inverters.

The SN5404, SN54H04, SN54L04, SN54LS04 and SN54S04 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7404, SN74H04, SN74LS04 and SN74S04 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each inverter)

INPUTS A	OUTPUT Y
H	L
L	H

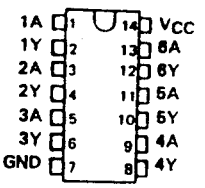
logic diagram (each inverter)



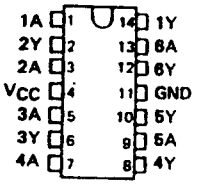
positive logic

$$Y = \overline{A}$$

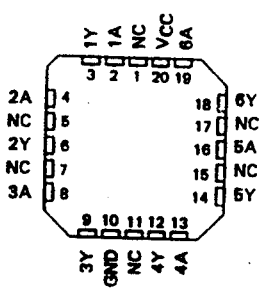
SN5404, SN54H04, SN54L04 . . . J PACKAGE
SN54LS04, SN54S04 . . . J OR W PACKAGE
SN7404, SN74H04 . . . J OR N PACKAGE
SN74LS04, SN74S04 . . . D, J OR N PACKAGE
(TOP VIEW)



SN5404, SN54H04 . . . W PACKAGE
(TOP VIEW)



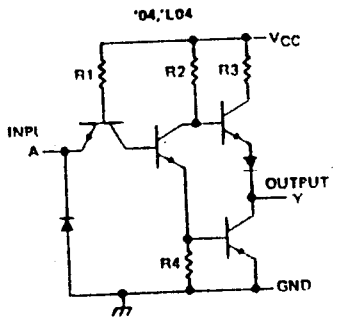
SN54LS04, SN54S04 . . . FK PACKAGE
SN74LS04, SN74S04 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

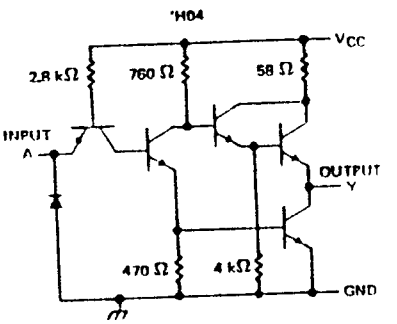
schematics (each gate)

'04,'L04

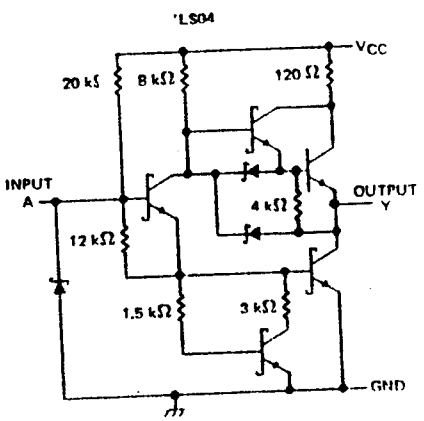


CIRCUIT	R1	R2	R3	R4
'04	4 kΩ	1.6 kΩ	130 Ω	1 kΩ
'L04	40 kΩ	20 kΩ	500 Ω	12 kΩ

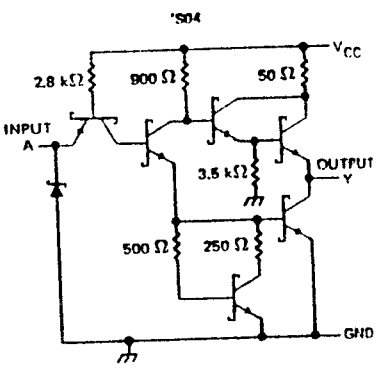
'H04



'LS04



'S04



Resistor values shown are nominal

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1): '04, 'H04, 'LS04, 'S04 . . . . . 7 V
'L04 . . . . . 5.5 V

Input voltage: '04, 'H04, 'L04, 'S04 . . . . . 5.5 V
'LS04 . . . . . 7 V

Operating free-air temperature range: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0°C to 70°C

Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal

recommended operating conditions

	SN54LS04			SN74LS04			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			−0.4			−0.4	mA
I_{OL} Low-level output current			4			8	mA
T_A Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS04			SN74LS04			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 4 mA		0.25	0.4			0.4	
	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 8 mA					0.25	0.5	
I_I	V_{CC} = MAX, V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX	−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX, V_I = 0 V		1.2	2.4		1.2	2.4	mA
I_{CCL}	V_{CC} = MAX, V_I = 4.5 V		3.6	6.6		3.6	6.6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	R_L = 2 kΩ, C_L = 15 pF		9	15	ns
t_{PHL}					10	15	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

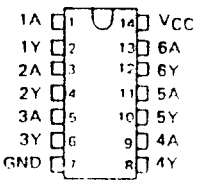
TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN5414, SN54LS14, SN7414, SN74LS14
HEX SCHMITT-TRIGGER INVERTERS

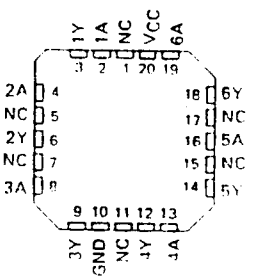
REVISED DECEMBER 1983

- **Operation from Very Slow Edges**
- **Improved Line-Receiving Characteristics**
- **High Noise Immunity**

SN5414, SN54LS14 . . . J OR W PACKAGE
SN7414 . . . J OR N PACKAGE
SN74LS14 . . . D, J OR N PACKAGE
(TOP VIEW)



SN54LS14 . . . FK PACKAGE
SN74LS14 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

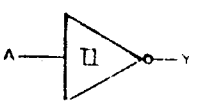
description

Each circuit functions as an inverter, but because of the Schmitt action, it has different input threshold levels for positive (V_{T+}) and for negative going (V_{T-}) signals.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

The SN5414 and SN54LS14 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7414 and the SN74LS14 are characterized for operation from 0°C to 70°C.

logic diagram

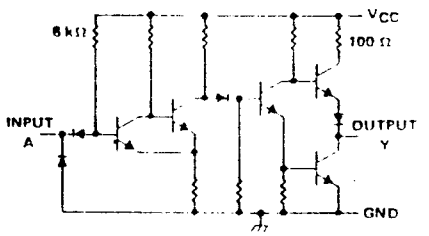


positive logic

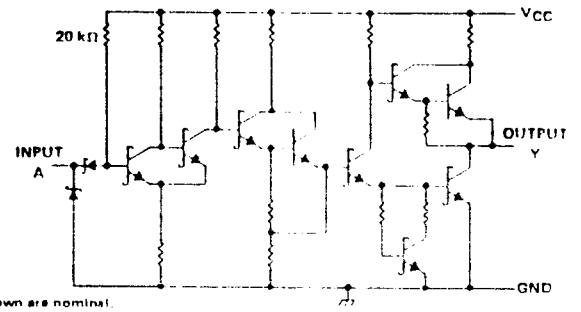
$$Y = \overline{A}$$

schematics

'14



'LS14



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage: '14		5.5 V
'LS14		7 V
Operating free-air temperature:	SN54'	−55°C to 125°C
	SN74'	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS14			SN74LS14			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH} High-level output current			−0.4			−0.4	mA
I_{OL} Low-level output current			4			8	mA
T_A Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			SN54LS14			SN74LS14			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	V_{CC} = 5 V			1.4	1.6	1.9	1.4	1.6	1.9	V
V_{T-}	V_{CC} = 5 V			0.5	0.8	1	0.5	0.8	1	V
Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 5 V			0.4	0.8		0.4	0.8		V
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	V_I = 0.5 V,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_I = 1.9 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_{T+}	V_{CC} = 5 V,	$V_I = V_{T+}$			−0.14			−0.14		mA
I_{T-}	V_{CC} = 5 V,	$V_I = V_{T-}$			−0.18			−0.18		mA
I_I	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_{IH} = 2.7 V				20			20	μA
I_{IL}	V_{CC} = MAX,	V_{IL} = 0.4 V				−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX				3.6	16		3.6	16	mA
I_{CCL}	V_{CC} = MAX				12	21		12	21	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	R_L = 2 kΩ, C_L = 15 pF		15	22	ns
t_{PHL}					15	22	ns

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS

TYPES SN5420, SN54H20, SN54L20, SN54LS20, SN54S20, SN7420, SN74H20, SN74LS20, SN74S20 DUAL 4-INPUT POSITIVE-NAND GATES

REVISED DECEMBER 1983

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

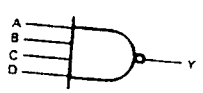
These devices contain two independent 4-input NAND gates.

The SN5420, SN54H20, SN54L20, SN54LS20 and SN54S20 are characterized for operation over the full military range of −55°C to 125°C. The SN7420, SN74H20, SN74LS20 and SN74S20 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

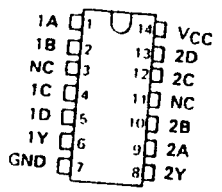
logic diagram (each gate)



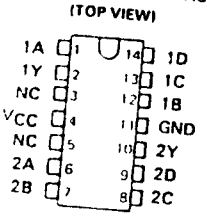
positive logic

$Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$

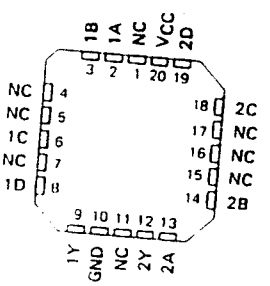
SN5420, SN54H20, SN54L20 . . . J PACKAGE
SN54LS20, SN54S20 . . . J OR W PACKAGE
SN7420, SN74H20 . . . J OR N PACKAGE
SN74LS20, SN74S20 . . . D, J OR N PACKAGE
(TOP VIEW)



SN5420, SN54H20 . . . W PACKAGE
(TOP VIEW)



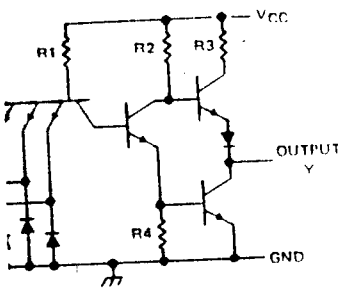
SN54LS20, SN54S20 . . . FK PACKAGE
SN74LS20, SN74S20 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

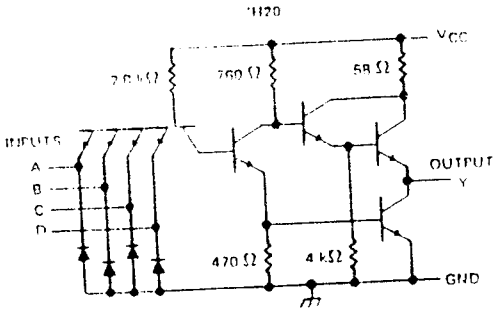
gh gate)

'20, 'L20

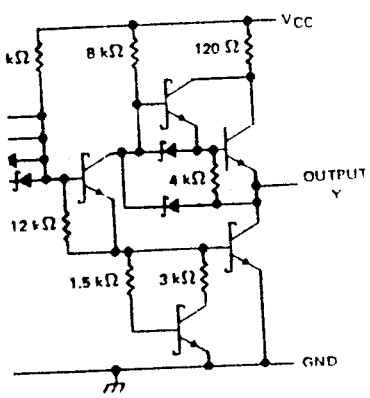


R1	R2	R3	R4
4 kΩ	1.6 kΩ	130 Ω	1 kΩ
40 kΩ	20 kΩ	500 Ω	12 k Ω

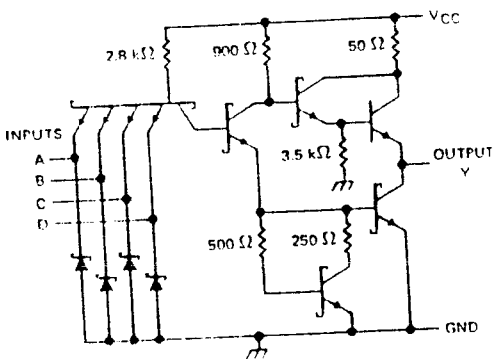
'H20



'LS20



'S20



ns shown are nominal

kimum ratings over operating free-air temperature range (unless otherwise noted)

roltage, V_{CC} (see Note 1): '20, 'H20, 'LS20, 'S20	7 V
'L20	8 V
oltage: '20, 'H20, 'L20, 'S20	5.5 V
'LS20	7 V
ng free-air temperature: SN54'	−55°C to 125°C
SN74'	0°C to 70°C
temperature range	−65°C to 150°C

age values are with respect to network ground terminal

recommended operating conditions

	SN54LS20			SN74LS20			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			−0.4			−0.4	mA
I_{OL} Low-level output current			4			8	mA
T_A Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS20			SN74LS20			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 4 mA		0.25	0.4			0.4	V
	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 8 mA					0.25	0.5	
I_I	V_{CC} = MAX, V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX	−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX, V_I = 0 V		0.4	0.8		0.4	0.8	mA
I_{CCL}	V_{CC} = MAX, V_I = 4.5 V		1.2	2.2		1.2	2.2	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	R_L = 2 kΩ, C_L = 15 pF		9	15	ns
t_{PHL}					10	15	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

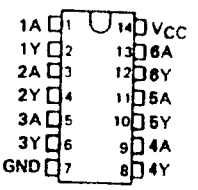
TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN5407, SN5417, SN7407, SN7417
HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

REVISED DECEMBER 1983

- **Converts TTL Voltage Levels to MOS Levels**
- **High Sink-Current Capability**
- **Input Clamping Diodes Simplify System Design**
- **Open-Collector Driver for Indicator Lamps and Relays**
- **Inputs Fully Compatible with Most TTL Circuits**

SN5407, SN5417 . . . J OR W PACKAGE
SN7407, SN7417 . . . J OR N PACKAGE
(TOP VIEW)



description

These monolithic TTL hex buffers/drivers feature high-voltage open-collector outputs for interfacing with high-level circuits (such as MOS), or for driving high-current loads (such as lamps or relays), and are also characterized for use as buffers for driving TTL inputs. The SN5407 and SN7407 have minimum breakdown voltages of 30 volts and the SN5417 and SN7417 have minimum breakdown voltages of 15 volts. The maximum sink current is 30 milliamperes for the SN5407 and SN5417, and 40 milliamperes for the SN7407 and SN7417.

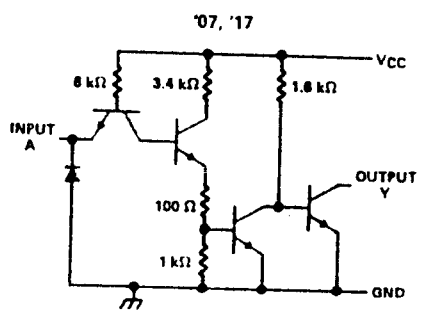
These circuits are completely compatible with most TTL families. Inputs are diode-clamped to minimize transmission-line effects which simplifies design. Typical power dissipation is 145 milliwatts and average propagation delay time is 14 nanoseconds. The SN5407 and SN5417 are characterized for operation over the full military temperature range of −55° C to 125° C; the SN7407 and SN7417 are characterized for operation from 0° C to 70° C.

logic diagram (each gate)

positive logic (each gate)

$Y = A$

schematic



Resistor values shown are nominal.

3 TTL DEVICES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Output voltage (see Notes 1 and 2): SN5407, SN7407 Circuits . . . . . 30 V
SN5417, SN7417 Circuits . . . . . 15 V
Operating free-air temperature range: SN5407, SN5417 Circuits . . . . . −55°C to 125°C
SN7407, SN7417 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

			SN5407 SN5417			SN7407 SN7417			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	'07			30			30	V
		'17			15			15	
I_{OL}	Low-level output current				30			40	mA
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN5407 SN5417			SN7407 SN7417			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5	V
I_{OH}	V_{CC} = MIN, V_{IL} = 0.8 V, V_{OH} = §				0.25			0.25	mA
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V	I_{OL} = 16 mA			0.4			0.4	V
		I_{OL} = ¶			0.7			0.7	
I_I	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX, V_{IH} = 2.4 V				40			40	mA
I_{IL}	V_{CC} = MAX, V_{IL} = 0.4 V				−1.6			−1.6	mA
I_{CCH}	V_{CC} = MAX			29	41		29	41	mA
I_{CCL}	V_{CC} = MAX			21	30		21	30	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ V_{OH} = 30 V for '07 and 15 V for '17.
¶ I_{OL} = 30 mA for SN54' and 40 mA for SN74'.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	R_L = 110 Ω, C_L = 15 pF		6	10	ns
t_{PHL}					20	30	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

National Semiconductor

DM54LS154/DM74LS154 4-Line to 16-Line Decoders/Demultiplexers

General Description

Each of these 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

Features

- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs
- Input clamping diodes simplify system design
- High fan-out, low-impedance, totem-pole outputs
- Typical propagation delay
  3 levels of logic 23 ns
  Strobe 19 ns
- Typical power dissipation 45 mW

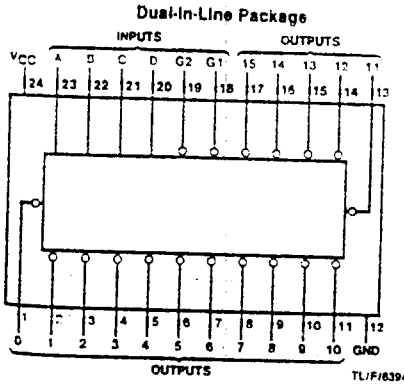
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

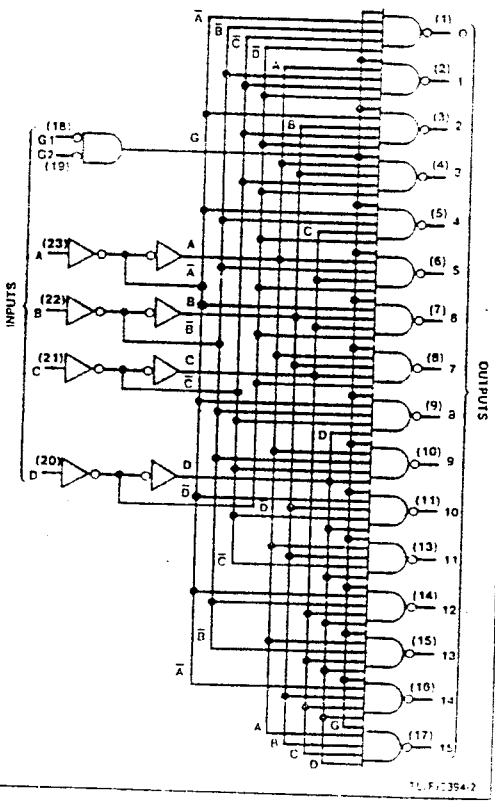
Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection and Logic Diagrams

Dual-In-Line Package



54LS154 (J) 74LS154 (N)



Recommended Operating Conditions

Symbol	Parameter	DM54LS154			DM74LS154			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.25	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			9	14	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and a [illegible]

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15\ pF$			$C_L = 50\ pF$			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Output		18	30		22	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Output		18	30		24	35	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to Output		12	20		15	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to Output		16	25		23	35	ns

Function Table

Inputs						Outputs										
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level, L = Low Level, X = Don't Care

TYPES SN54LS373, SN54LS374, SN54S373, SN54S374, SN74LS373, SN74LS374, SN74S373, SN74S374
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

OCTOBER 1975 - REVISED APRIL 1985

- **Choice of 8 Latches or 8 D-Type Flip-Flops In a Single Package**
- **3-State Bus-Driving Outputs**
- **Full Parallel-Access for Loading**
- **Buffered Control Inputs**
- **Clock/Enable Input Has Hysteresis to Improve Noise Rejection ('S373 and 'S374)**
- **P-N-P Inputs Reduce D-C Loading on Data Lines ('S373 and 'S374)**

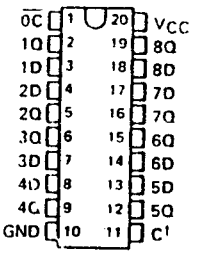
'LS373, 'S373
FUNCTION TABLE

OUTPUT ENABLE	ENABLE LATCH	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

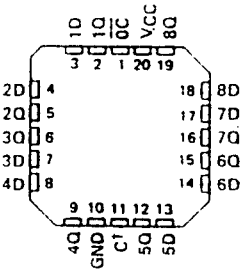
'LS374, 'S374
FUNCTION TABLE

OUTPUT ENABLE	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

SN54LS373, SN54LS374, SN54S373, SN54S374 . . . J PACKAGE
SN74LS373, SN74LS374, SN74S373, SN74S374 . . . DW, J OR N PACKAGE
(TOP VIEW)



SN54LS373, SN54LS374, SN54S373, SN54S374 . . . FK PACKAGE
SN74LS373, SN74LS374, SN74S373, SN74S374 . . . FN PACKAGE
(TOP VIEW)



'C for 'LS373 and 'S373, CLK for 'LS374 and 'S374

description

These 8-bit registers feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'LS373 and 'S373 are transparent D-type latches meaning that while the enable (C) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

description (continued)

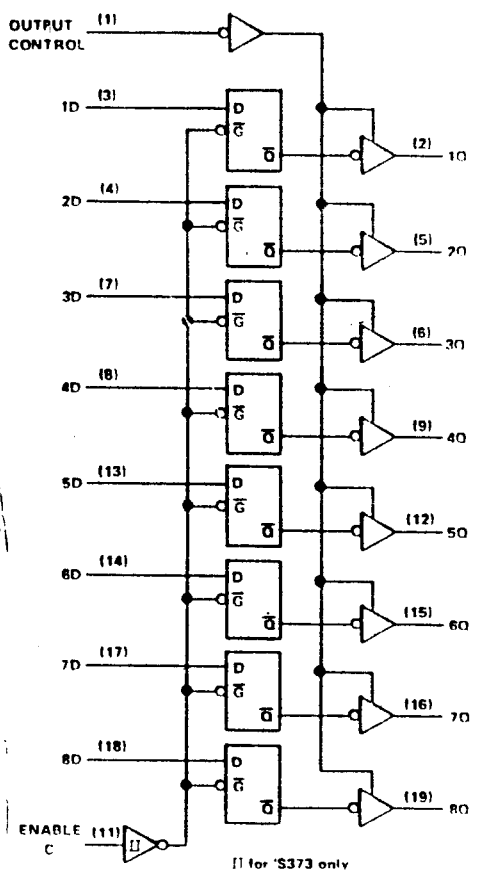
The eight flip-flops of the 'LS374 and 'S374 are edge triggered D-type flip flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were setup at the D inputs.

Schmitt-trigger buffered inputs at the enable/clock lines of the 'S373 and 'S374 devices, simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high impedance state. In the high impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

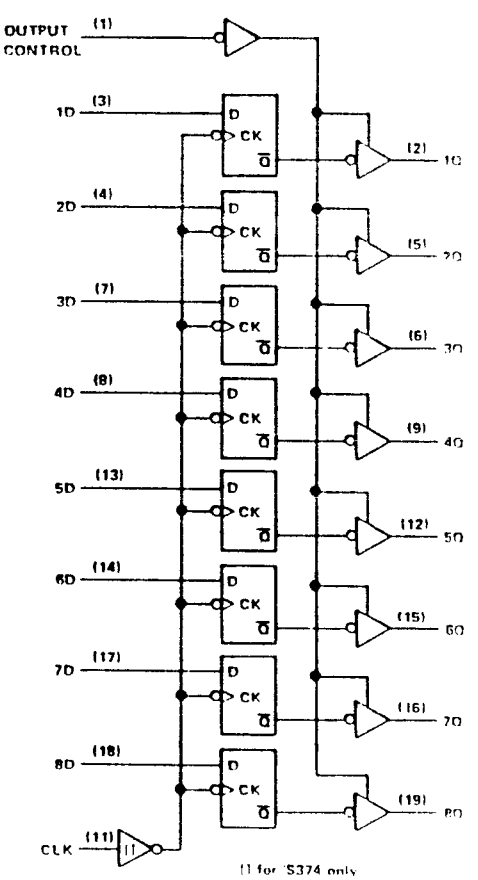
logic diagrams

'LS373, 'S373
TRANSPARENT LATCHES



[1] for 'S373 only

'LS374, 'S374
POSITIVE-EDGE-TRIGGERED FLIP-FLOPS



[1] for 'S374 only

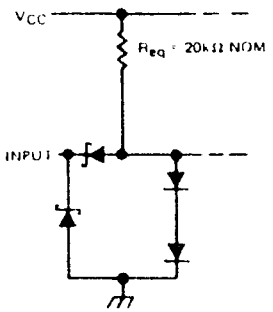
Pin numbers shown on logic notation are for DW, J or N packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

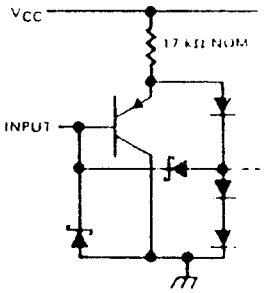
schematic of inputs and outputs

'LS373

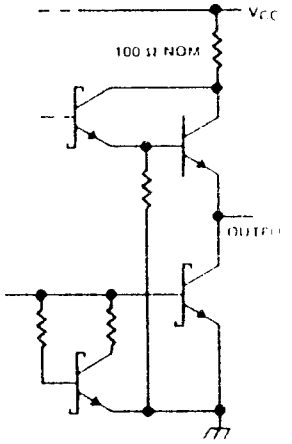
EQUIVALENT OF DATA INPUTS



EQUIVALENT OF ENABLE AND OUTPUT CONTROL INPUTS

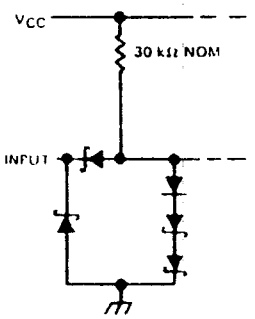


TYPICAL OF ALL OUTPUTS

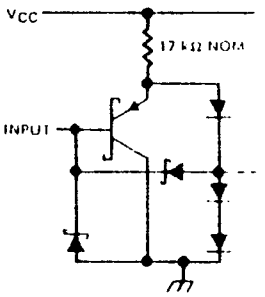


'LS374

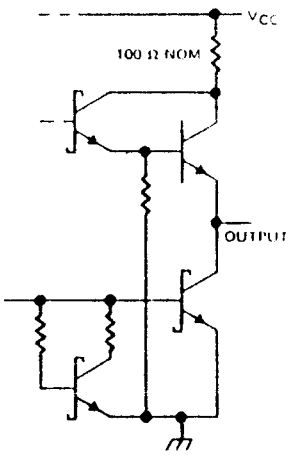
EQUIVALENT OF DATA INPUTS



EQUIVALENT OF CLOCK AND OUTPUT CONTROL INPUTS



TYPICAL OF ALL OUTPUTS



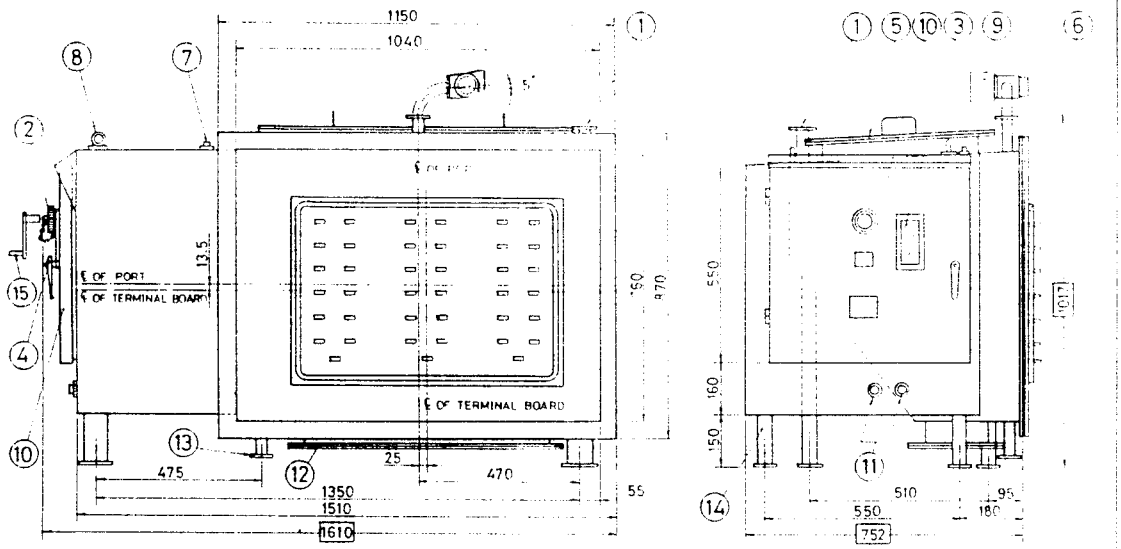
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		LS373			LS374			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			C_L = 45 pF, R_L = 667 Ω See Notes 2 and 3					35	50		MHz
t_{PLH}	Data	Any Q				12	18				ns
t_{PHL}						12	18				
t_{PLH}	Clock or enable	Any Q				20	30		15	28	ns
t_{PHL}						18	30		19	28	
t_{PZH}	Output Control	Any Q				15	28		20	26	ns
t_{PZL}						25	36		21	28	
t_{PHZ}	Output Control	Any Q	C_L = 5 pF, R_L = 667 Ω See Note 3	SN54		28	32		28	32	ns
				SN74		15	25		15	28	
t_{PLZ}	Output Control	Any Q				12	20		12	20	ns

NOTES: 2. Maximum clock frequency is tested with all outputs loaded.
3. See General Information Section for load circuits and voltage waveforms.

f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high level output
t_{PHL} = propagation delay time, high-to-low level output
t_{PZH} = output enable time to high level
t_{PZL} = output enable time to low level
t_{PHZ} = output disable time from high level
t_{PLZ} = output disable time from low level

OUT LINE DIMENSIONS



1. OIL FILLING AND FILTERING VALVE FLANGE
2. CRANK HANDLE LID
3. WINDOW FOR TAP NUMBER COUNTER
4. DOOR HANDLE
5. REMOVABLE INSPECTION COVER
6. TERMINAL BARRIER BOARD
7. AIR FILTER
8. LIFTING LUG
9. OIL SURGE BUCHHOLZ RELAY
10. DRIVING MECHANISM DOOR
11. PUSH BUTTON SWITCHES FOR RAISE AND LOWER
12. CABLE ENTRY, GLAND PLATE
13. OIL DRAIN AND FILTERING VALVE FLANGE
14. SUPPORTING LEG
15. REMOVABLE CRANK HANDLE

NOTES

1. ALL DIMENSIONS ARE IN MM
2. TRANSPORTATION DIMENSIONS ARE MARKED THUS [XXXX]
3. DIMENSIONS ARE LIABLE TO CHANGE WITHIN THE TOLERANCE (AS PER IS:2102)

TEST LEVELS :

	Power Freq. for 1 Minute (KV RMS)	Imp. Voltage of 1.2/50 Wave (KVP)
Between Phases	70	170
Between Phases and Earth	70	170
Between Adjacent Contacts	25	70
Over Fine Taps	25	70
Over Pre Selector	25	70

TESTING :

This Tapchanger has been Type Tested to IS 8468 at CPRI., and at the Division of High Voltage Engineering, Anna University, Madras.

As part of our Quality Assurance Programme, we conduct several tests at our Works, in a routine manner before despatch. The main test, which goes beyond the requirements of IS 8468, is an operation test for 5000 operations, without the contacts energised. During this test, the Motor is run at its normal voltage, and speed, and is switched on and off for each tap change. This is a very rigorous, and very practical test from the point of view of the user. Tanks are hydraulically Leak Tested at equivalent of 10ft. liquid head.

We also conduct the following Routine tests :

1. Megger
2. Contact Resistance
3. Timing of Contacts
4. Aux. Circuit Withstand

As the design and manufacture of our equipment are subject to constant improvement, the product supplied may differ in certain details from the specifications and illustrations.

ON LOAD GEARS

338 Sidco Estate Ambattur Madras 600 098
Tel : 655480, 655506 Tlx : 41-22033