Telemetry Simulation Using Direct Digital Synthesis

Project Report

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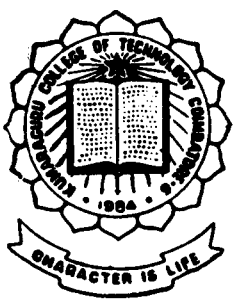
Submitted in Partial fulfilment of the Requirements for the award of Degree of Bachelor of Engineering in Electronics and Communication Engineering of the Bharathiar University



Department of Electronics and Communication Engineering

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APRIL 1994

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CERTIFICATE

This is to certify that

SHREE HARI. K, GURURAJAN. N, SAMPATH KUMAR. S, CHOLAN. K, students of VIII semester B.E., Electronics and Communication branch in KUMARAGURU COLLEGE OF TECHNOLOGY has done their project work on "TELEMETRY SIMULATION USING DIRECT DIGITAL SYNTHESIS" under my technical guidance and using the facilities available at the college.

P Angusw 18/3/94

P. ANGUSWAMY
HEAD,
SPA
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Department of Electronics and Communication Engineering

Kumaraguru College of Technology

Coimbatore - 641 006.

CERTIFICATE

This is to certify that this project entitled

TELEMETRY SIMULATION USING DIRECT DIGITAL SYNTHESIS

has been done by

K. Cholan. N. Gurukajan.

S. Sampathkumar. K. Shreehari

in partial fulfilment of the
requirement for the award of the degree of
BACHELOR OF ENGINEERING
in Electronics and Communication Engineering
Branch of the Bharathiar University, Coimbatore
During the academic year 1994

Guide

Head of the Department

Certified that the Candidate was examined by us in the Project-Work

Viva-Voce Examination held on 18th. Apl. 1994.

and the University Register Number was _____

Internal Examiner

External Examiner

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A B B R E V I A T I O N S

PCM	:	PULSE CODE MODULATION
DROPS	:	DECENTRALISED PROGRAMMABLE ON BOARD PCM SYSTEM
CCU	:	CENTRAL CONTROL UNIT
RU	:	REMOTE UNIT
IRIG	:	INTER-RANGE INSTRUMENTATION GROUP
PLL	:	PHASE LOCKED LOOP
DDS	:	DIRECT DIGITAL SYNTHESIS
EPROM	:	ERASABLE PROGRAMMABLE READ ONLY MEMORY
LTI	:	LINEAR TIME INVARIANT
EPLD	:	ERASABLE PROGRAMMABLE LOGIC DEVICES
FPGA	:	FIELD PROGRAMMABLE GATE ARRAY

SYNOPSIS

Telemetry simulator is one which simulates data which resembles the original data for the checking of Ground Station. So far various techniques have been employed to generate stable signals using RL, LC, Crystal Oscillators and PLL circuits. With the advent of high speed Digital Integrated Circuits it is possible to synthesize signals with greater accuracy. The project work deals with the simulation of signals of varying frequencies using Digital techniques.

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APPENDICES

CHAPTER 1

INTRODUCTION

The literal meaning of telemetry is measuring at a remote distance. Telemetry is used to measure parameters such as temperature, pressure, acceleration, velocity etc. Telemetry is used in many industrial and aerospace application on a day-to-day basis. Especially in the case of space applications, telemetry simulation plays a vital role.

The observed parameters from the satellite is received by the ground station and processed. Before that, the readiness of the ground station has to be checked. For that a signal corresponding to a known parameter is simulated and given to the receiver where the signal is processed and verified with

the known value. After checking the readiness, the Ground Station has to be switched back for receiving the data being transmitted from the satellite.

This project deals with the simulation of the signal using **DIRECT DIGITAL SYNTHESIS** for checking the correctness of the Ground Station.

CHAPTER 2

TELEMETRY SIMULATION

In space applications, different launch vehicles and different satellites will have different set of measurement requirements. Accordingly, the telemetry bit rate and telemetry formatting will be different for each applications. However, the Ground and on-board equipments have to be built in such a way that different mission requirements can be met with the same set of equipments so that we can minimize the time required for setting up the ground station and also to reduce the cost of mission operations. This essentially calls for designing pulse code modulation systems with very high programmability.

PCM is particularly used because of its ability to be reconstituted (pulse reshaping)

and retransmitted, using regenerative generators, with little loss of signal characteristics.

Moreover the Pulse Code Modulation has a greater immunity to noise.

Secrecy can be maintained in Pulse Code Modulation.

Hence it is more widely used despite its more complex terminal equipment requirements.

PULSE CODE MODULATION GROUND SYSTEM

A general purpose PCM ground equipment should have the facility to program the bit rate, (number of bits/second) word rate, frame rate, sub frame rate as shown in FIG (1). The DDS generates the bit stream to which is added the word rate, frame rate, sub frame rate. The Formatter a ligns the frame

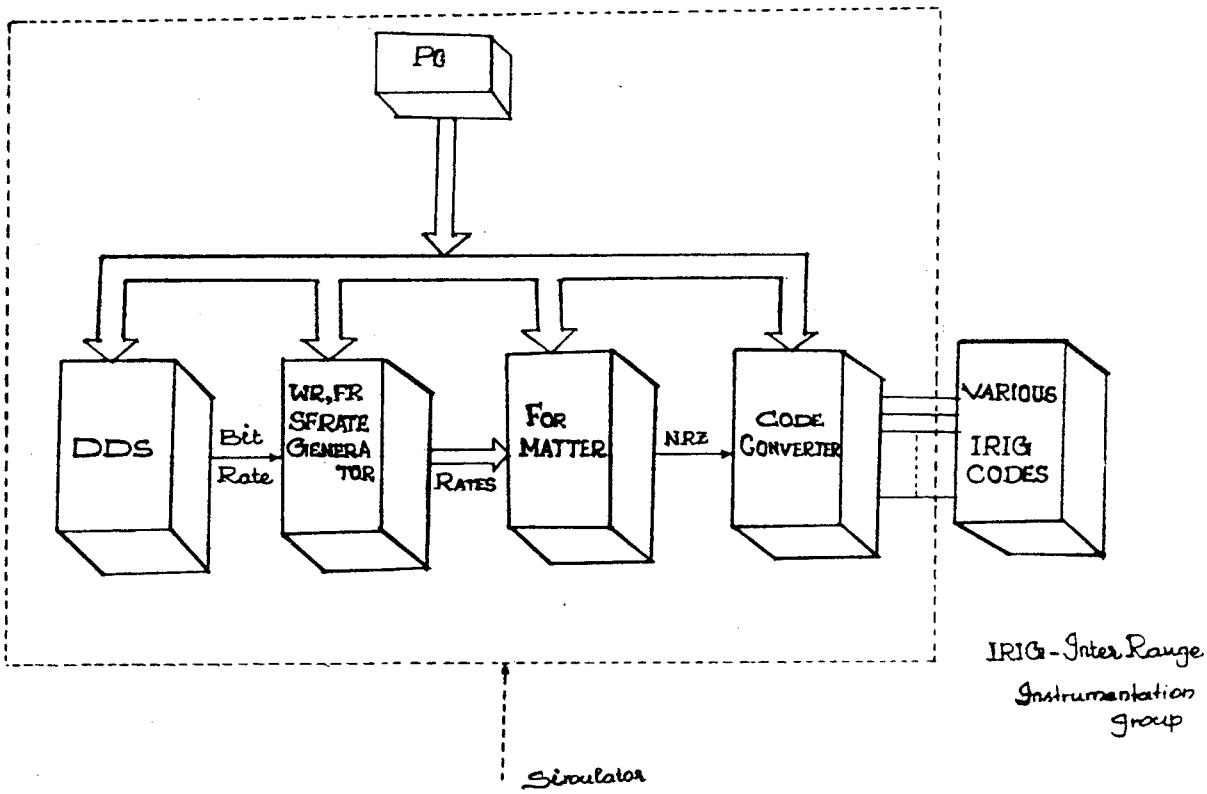


FIG.1 PCM TELEMETRY SYSTEM

sync, Sub Frame Sync and the different words in the required fashion. The output of the Formatter is a NRZ code which can be converted into the desired codes using a code converter.

The Pulse Code Modulation Ground System consists of the Pulse Code Modulation simulator, bit synchronizer, frame synchronizer, sub frame synchronizer, a display as shown in FIG (2). The PCM simulator generates the required signal which is checked for its Frame sync, Sub Frame sync and then it is brought to the required format and displayed.

PCM ENCODER

In Pulse Code Modulation Telemetry system, the different parameters to be measured are first converted into equivalent electrical signals. The output of the transducers are amplified and then fed to a Pulse Code Modulation Encoder. The Pulse Code Modu-

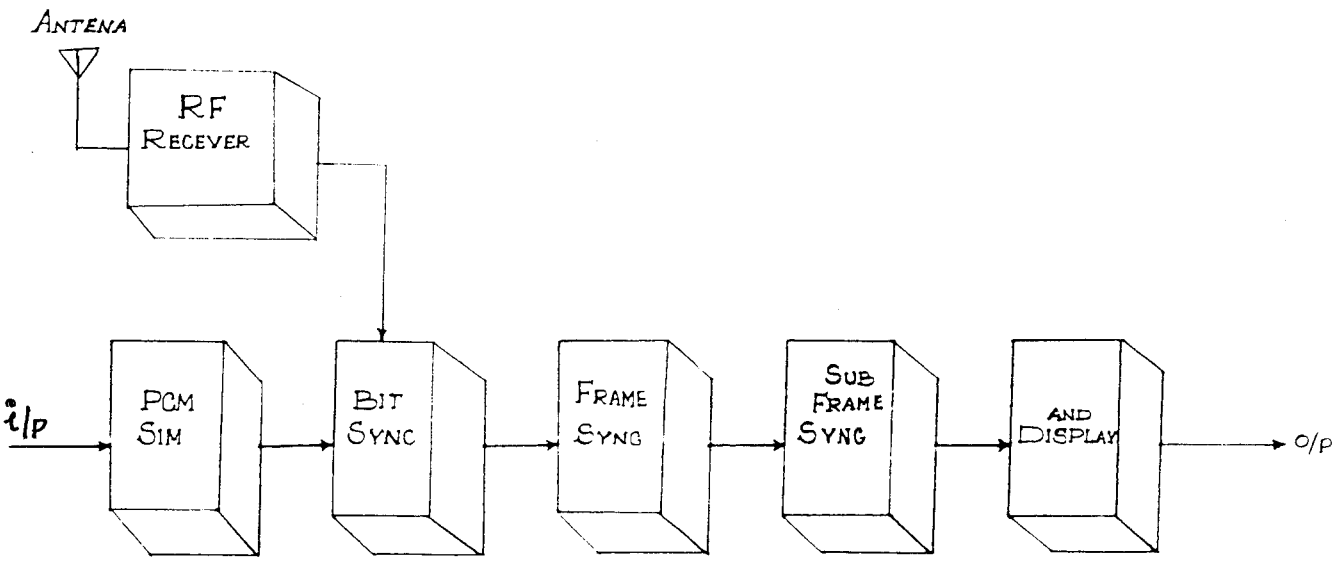


FIG 2 PCM GIROUND SYSTEM

lation Encoder consists of a Multiplexer, Sample and Hold, Analog to Digital Converter and a Pulse Code Modulation Formatter as shown in FIG(3).

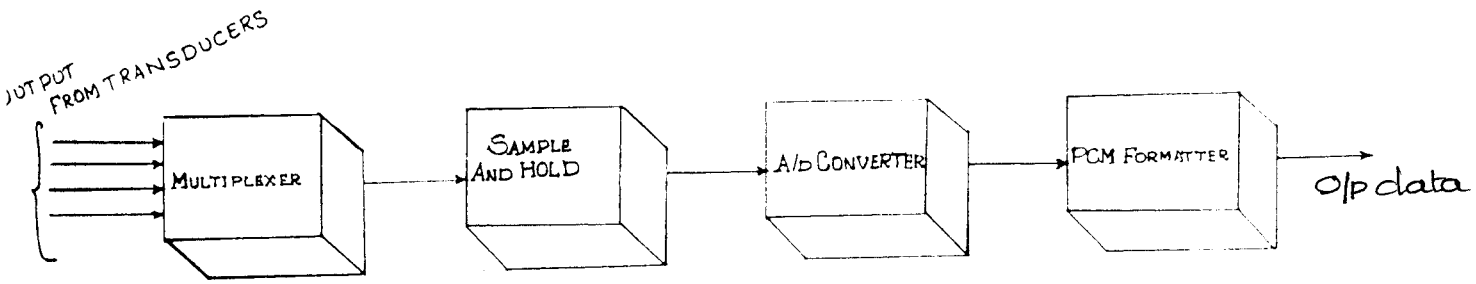


FIG 3 PCM ~~FORMATTER~~ Encoder.

CHAPTER 3

PCM FORMATTER

Telemetry formatting mainly consists of encoding these digitized samples into known approved standards, so that they can be easily decoded in the ground. The system consists of 3 major elements namely :

* Central Control Unit (CCU)
* Remote Unit (RU)
* DROPS Bus

The CCU is located near the transmitting source and the RU is located near the data source. The CCU and the RU are connected by serial communication link which is called as **DROPS BUS.** A brief discussion of each of the above three elements are given below:

CENTRAL CONTROL UNIT (CCU)

The primary functions of the CCU are

the following :-

- Generates the required PCM format

- Generates the commands to the RU's and receives the digitized data from different RU's through DROPS Bus and formats this data as required.

- Provides system level interface to the Onboard transmitting system and Ground system.

REMOTE UNIT (RU)

The primary function of the RU are the following :

- Receives the addresses from the CCU and acquires data from different sensors and signal conditioners.

- Does the multiplexing, sampling and A to D conversion wherever required.

- Transfers the digitized data to the CCU as requested.

DROPS BUS

The DROPS Bus is a vital element in the entire functioning of the DROPS. The function of the Bus is to provide communication between CCU and RU. It is basically a serial digital link with twisted shield pair wires as the communication medium.

The Bus bit rate is 1M bits per second (Max) and a telemetry word length is of eight bits.

In the case of satellite operations and launch vehicle operations, various ground networks located at various locations, throughout the globe have to receive the data from multiple launch vehicle. In order to meet such requirements, a set of guide lines and standards have been involved by various international agencies. The more popular standard is the **Inter-Range Instrumentation Group (IRIG).**

IRIG PULSE CODE FORMATTING

In this standard, each sample of data is converted into equivalent binary digits called word. The length of the word may vary anywhere between 6 - 16 bits or more. These words are assemoled into telemetry frames. Each frame consists of multiple words and a frame sync code marker. The number of words in a frame can vary upto a maximum of 512. Multiple number of frames are assembled as a sub frame and a sub frame can have a maximum of 512 frames with an appropriate sub frame sync marker. This type of arrangement is useful in accomodating varying various types of signals with varying sample rate requirements. Also, based on the number of parameters to be monitored, the telemetry bit rate may have to be varied anywhere between a few hundred bits to a few mega bits per second.

CHAPTER 4

DIRECT DIGITAL SYNTHESIS

Until recent years, all techniques for synthesizing waveforms were implemented in the frequency domain using the traditional analog oscillator phase locked loop or a Bank of Crystals to generate stable signals of controllable frequency.

The availability of fast digital circuits and accurate Digital to Analog convertors make DDS technology available to the average electronics enthusiasts who are in need of accurate frequencies.

Out of many parameters to be varied in the simulator, the programmability for a bit rate simulation needs a careful design consideration because of the fine resolution required in the bit rate values. Traditionally, various types of bit rate generators are

being used in such simulators. Some of the traditional techniques are

* Analog RC Oscillators
* Bank of Crystals
* PLL Oscillators
* Oscillators with simple dividers.

However such techniques are having many limitations such as the following :

(i) It is very difficult to get a very fine resolution over a wide bit rate variations.

(ii) The bit rate stability changes with respect to environment and age.

(iii) They are becoming more expensive and bulky.

(iv) They have limited operating speed.

Because of the above limitations and also because of the impressive developments in micro electronics, **Numerically Controlled Oscillators** using **Direct Digital Synthesis Techniques** is replacing the older circuits

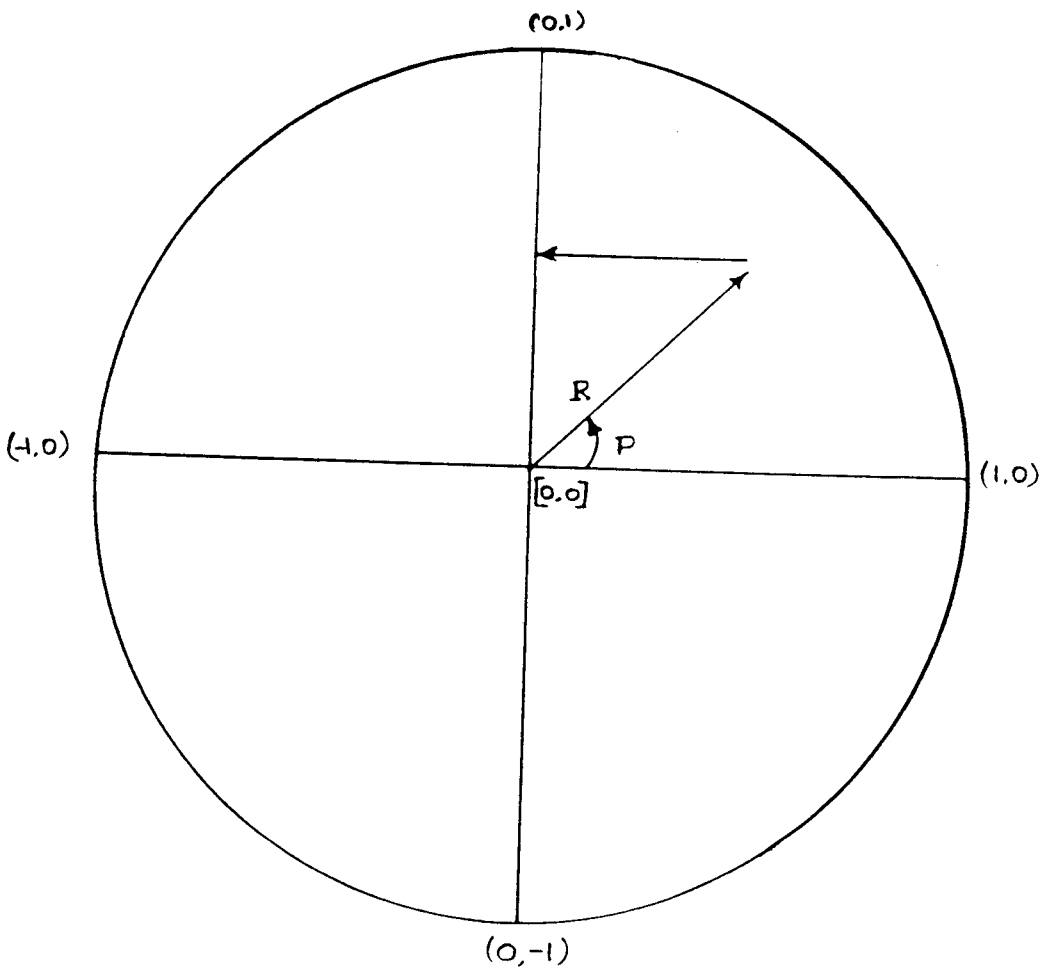


FIG 4. THIS CIRCLE HAS A RADIUS
Whose length is arbitararily set to One

and techniques in all the contemporary telemetry equipments.

Signal synthesis does not begin with an existing signal. DDS takes a small set of parameters (numbers) that describe the desired signal and generates a number sequence that represents the signal. This number sequence undergoes a digital to analog conversion to finally produce the required signal.

A review of trignometry is important to the understanding of Direct Digital Synthesis before delving into the details of the electronics. FIG(4) shows a circle with radius whose length is arbitarily set to one.

The radial line labelled R is allowed to rotate about the circle through an angle 'P', which will be referred to as the phase. Now by drawing a horizontal line from the tip of line R until it intersects

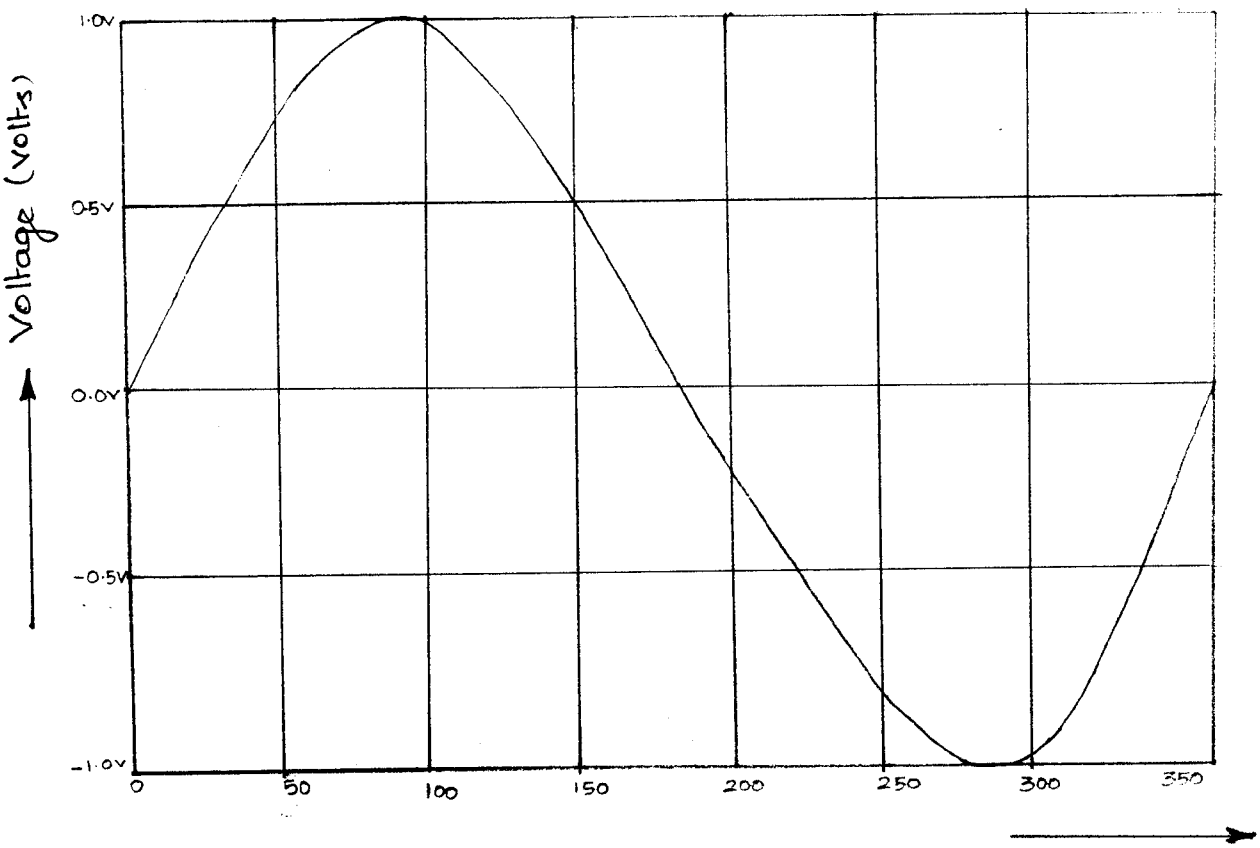


FIG: 5 THE LENGTHS. ASRROTATES. is the Sine function of P

with the vertical axis defines the length as 'S' as shown in the FIG(4). As the radius 'R' is allowed to make a complete rotation around the circle, the length of 'S' takes on all values between +1 and -1 (radius of the circle), while 'P' varies from 0 to 360 degrees. Thus the length 'S' is precisely the sine function of 'P', (i.e.) S = sin(P) as shown in FIG(5).

A popular view of this operation is based on the idea that a repetitive waveform can be visualized as rotation from point to point around a circle. The circumference of the circle (also called as phase circle) is equal to the number of values which can be represented in the phase accumulator. Phase accumulator overflow is equivalent of starting another trip around the circle. Rotation around the phase circle takes place in discrete increments at a constant clock rate such that the only variable is the size of the increment (the delta phase value).

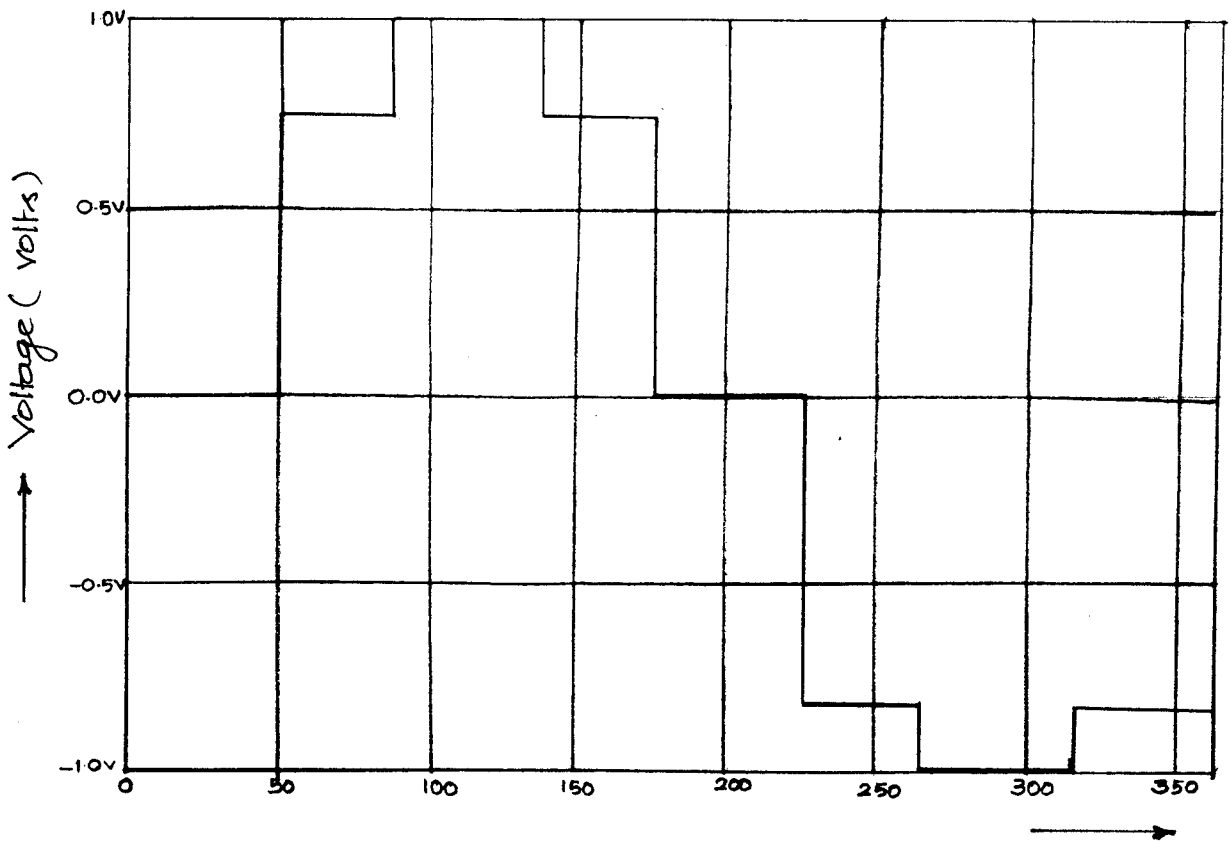


FIG 6 Stepwise approximation 8 steps

If rather than allowing R to rotate smoothly around the circle, we make eight equal steps around the circle, then the values of 'S' from the step-wise approximation as shown in FIG(6). As the number of steps is increased, the approximation becomes closer to the actual sine function with FIG(7) showing the approximation for 64 steps. Analog filtering is used to smooth out the steps to produce a perfect Sine wave.

From this simplified discussion, a method for generating a varying frequency can be derived. Assume that each step occurs at a precisely determined instant, than by varying the step size the number of steps around each circle can be varied. The fewer the steps, the faster the complete circle is covered, hence higher the frequency of the sine wave approximation. However fewer steps means a coarser approximation to the actual sine function with the output eventually

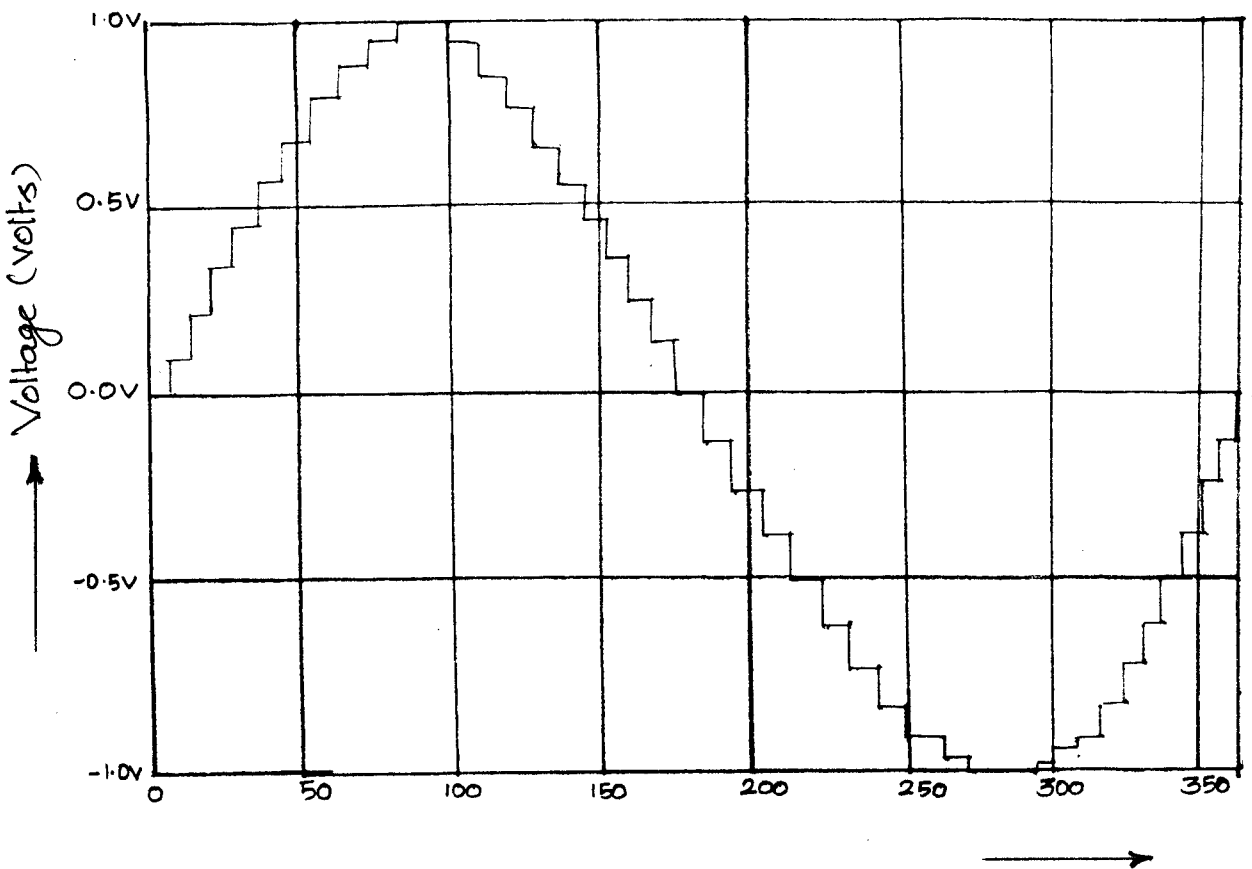


FIG 7 Stepwise approximation 64 steps

reducing to a square wave, which points out one of the limits of this technique. All we need now is a circuit that will synchronize the variable phase step to a precision clock.

Fig(8) shows the block diagram of the system. The phase accumulator basically consists of a delta phase register (or Hop register), an adder and an accumulator as shown in the complete topology. The output of the accumulator is fed to the sin(P) clock and a feedback is taken from the output of accumulator to the adder as the second set of input to the adder.

The block labelled phase accumulator repetitively adds the value set by the step size programmer to the sum performing the function of stepping the radius (R) about the circle in equal phase increments. The Phase Accumulator behaves like a simple counter, except that rather than incrementing

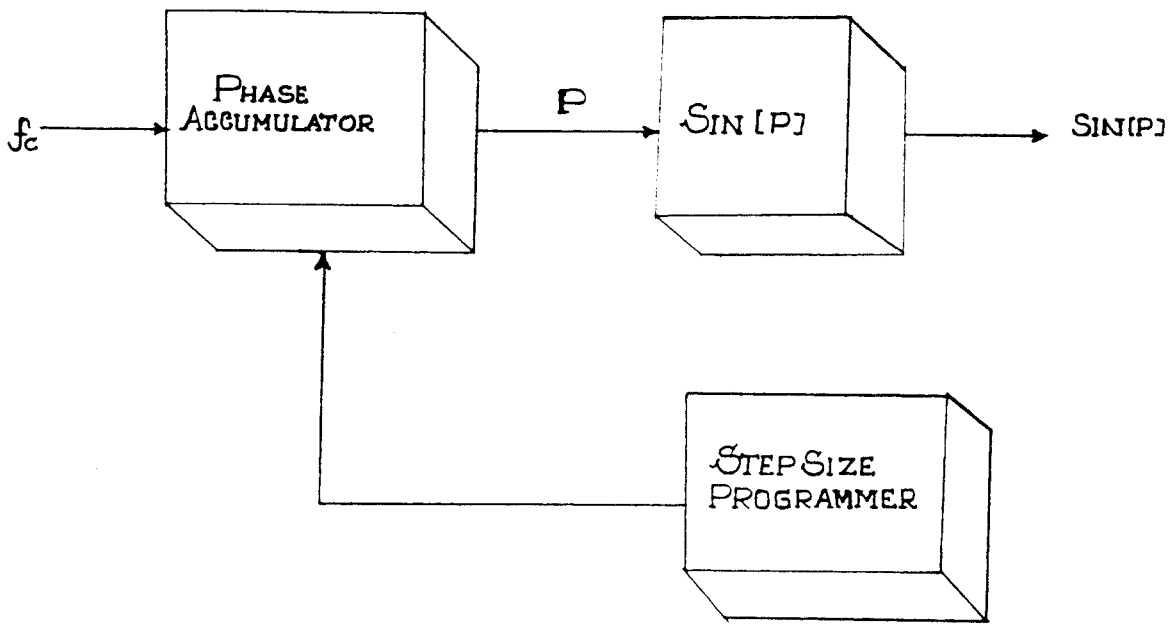


FIG 8 PHASE ACCUMULATOR and PHASE-TO-SINE CONVERTER

its output by one on each clock pulse, the output advances by the value set by the step size programmer on each clock pulse.

The block labelled sin(P) converts the value stored in the phase accumulator to a SINE amplitude approximation. The step size programmer is simply a bank of DIP switches, the phase accumulator is a series of cascaded adders, and the sin(P) block is a sine look up table contained in a memory unit.

The digital data present at the output of the sin(P) block must be converted to an analog voltage inorder to be used. A method for doing this is shown in FIG(9) which consists of a digital to analog converter, filter and an output amplifier. The filter helps to smooth out the jagged steps obtained in the sine approximation, while the output amplifier buffers the output of the digital to analog converter. In the actual implementation, the buffering and the filter-

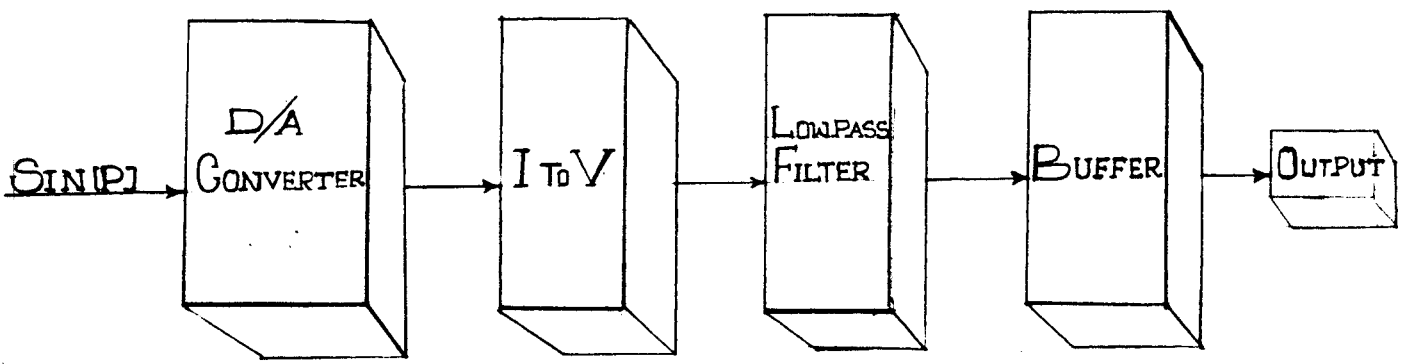


FIG:9 DIGITAL-TO-ANALOG CONVERTER and O/P STAGE

ing functions are combined.

Some writers in the field incorrectly state that a basic direct digital synthesizer can be readily constructed from a counter, a ROM OR EPROM and a DAC assembled in a straight chain. This type of device is simply a clocked waveform and not a direct digital synthesizer.

CHAPTER 5

DESIGN

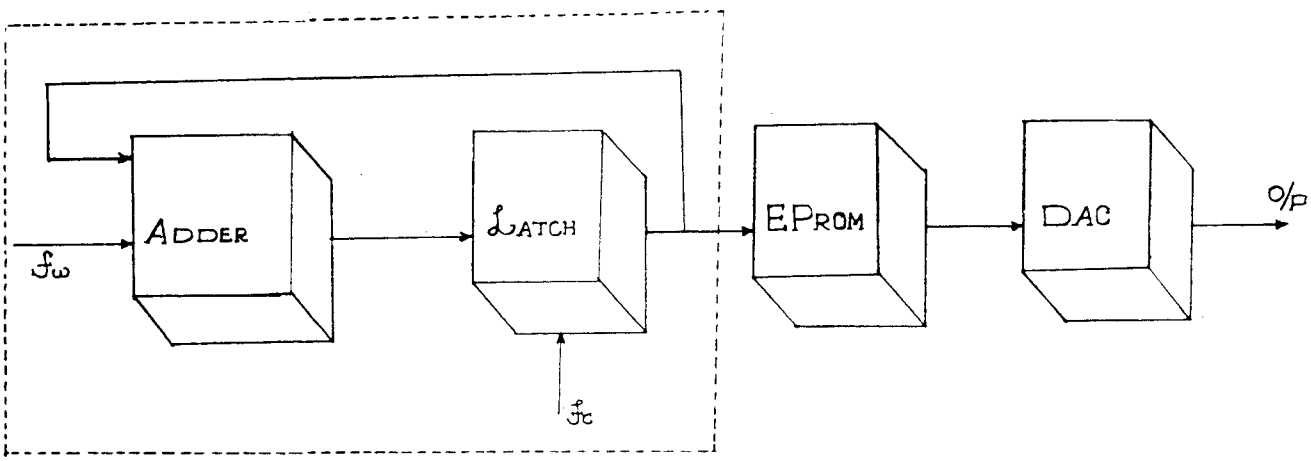


FIG 10 BLOCK DIAGRAM OF THE SYSTEM

Let fc be the clock frequency and fw be the binary input data as shown in the FIG(10).

Let the length of the Phase Accumulator be 'N'.

Consider fw = 1 (decimal) as the input to the adder.

Now the output of the latch gets incremented by one with every clock pulse.

Hence it takes 2^N clock pulses to read the complete EPROM table once and thus it takes 2^N clock pulses to complete one cycle of the sine wave.

Therefore the time taken to complete one cycle is given by,

$$Tc = \frac{1}{fc} * 2^N$$

Therefore the output frequency,

$$fo = \frac{1}{Tc}$$

$$fo = \frac{fc}{\frac{N}{2}} * l$$

where l is the value of fw.

Consider fw = 2 (decimal) as the input to the adder.

Now the output of the latch gets incremented by two with every clock pulse.

Hence it takes $\frac{2^N}{2}$ clock pulses to read the complete EPROM table once and thus it takes $\frac{2^N}{2}$ clock pulses to complete one cycle of the sine wave.

Therefore the time taken to complete one cycle is given by,

$$Tc = \frac{1}{fc} * \frac{2^N}{2}$$

Therefore the output frequency,

$$fo = \frac{1}{Tc}$$

$$fo = \frac{fc}{\frac{2^N}{2}} * 2$$

where 2 is the value of fw.

Similarly consider fw = M (decimal) as the value of the step size programmer which is the input to the adder.

Now the output of the latch gets incremented by M with every clock pulse.

Hence it takes $\frac{2^N}{M}$ clock pulses to read the complete EPROM table once and thus it takes $\frac{2^N}{M}$ clock pulses to complete

one cycle of the sine wave.

Therefore the time taken to complete one cycle is given by,

$$Tc = \frac{1}{fc} * \frac{2^N}{M}$$

Therefore the output frequency,

$$fo = \frac{1}{Tc}$$

$$fo = \frac{fc}{\frac{2^N}{M}}$$

where M is the value of fw.

Therefore

$$fo = \frac{fw * fc}{2^N}$$

The frequency resolution of a Direct Digital Synthesis system is set by a Master clock frequency fc, and the number of bits 'N', in the phase accumulator. For the binary accumulator we have here, the

resolution is then $\frac{fc}{2^N}$. If the step size programmer is set to a binary value 'M', then the output frequency is given by,

$$fo = M * \frac{fc}{2^N}$$

where,

fo - is the required frequency

M - is the value of step size programmer

fc - is the master clock frequency

N - is the length of the phase accumulator

The design presented here keeps 'M' less than $\frac{2^N}{4}$ to minimize distortion at the output. A particular frequency is synthesized by virtue of a feedback path from the accumulator to the adder, such that the step size 'M' is added to each subsequent accumulator output value to produce a new value. Eventually, the accumulator reaches overflow,

at which point a full cycle of possible phase values has been exhausted and another sequence begins. The frequency output by such a circuit is a function of the clock frequency, the length of the accumulator and the step size increment.

The tuning is accomplished by changing the size of the step taken by the phase accumulator while being clocked around the phase circle. Since the delta phase register or hop register is a separate structure from the actual accumulator portion of the circuit, the result of a change in tuning value is simply that the overall phase accumulator action continues from its current phase value to a new increment. Frequency changes therefore occur directly and in a phase continuous fashion. However, since the values output from the overall phase accumulator are used to address entries in a waveform map, the result is fundamentally a sampled data system, subject to Nyquist's

theorem. Thus the maximum output frequency which can practically be generated is something less than half of the clock frequency.

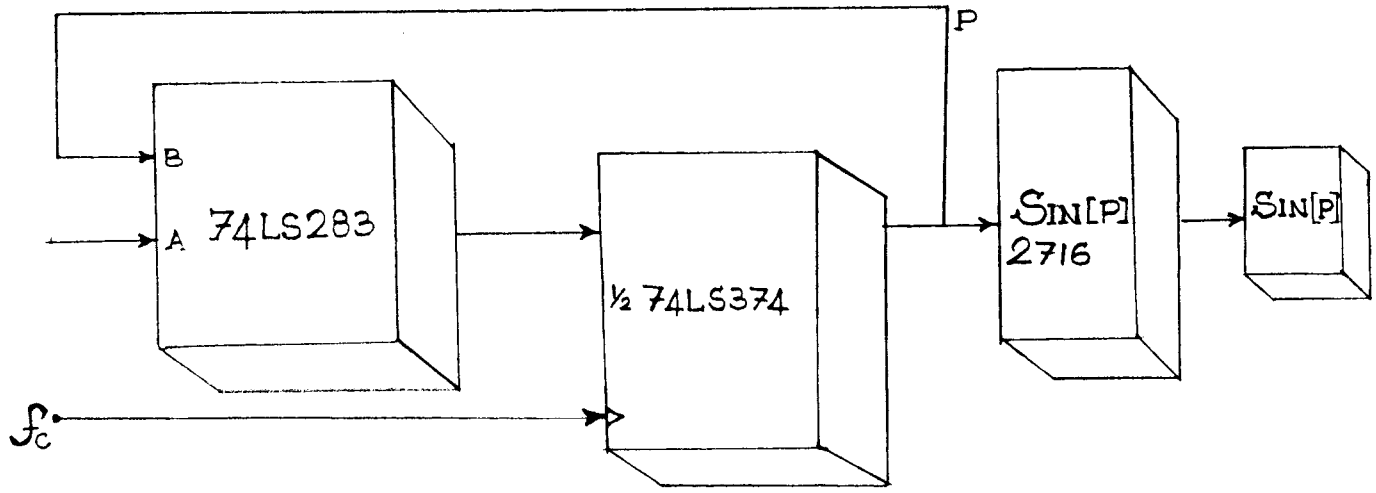


FIG 11 PARTIAL SCHEMATIC OF THE PHASE ACCUMULATOR

FIG(11) shows a partial schematic of the phase accumulator using components that are inexpensive and easy to get. FIG(12) shows the digital to analog converter block and the output stage.

The complete phase accumulator consists of six 74LS283 4 bit adders, with their outputs latched by 3 74LS374 octal D flip-flops. The outputs of the 74LS374's are fed back as the B inputs of the 74LS283, which forces the sum stored in the latches to be added to the value set by the switches on the A inputs. Since the 74LS374 stores data only at the positive edge of its clock input, the fact that the data presented to its inputs will be changing shortly after the clock causes no error.

The delay through the latch and adder guarantees a glitch free operation. At each

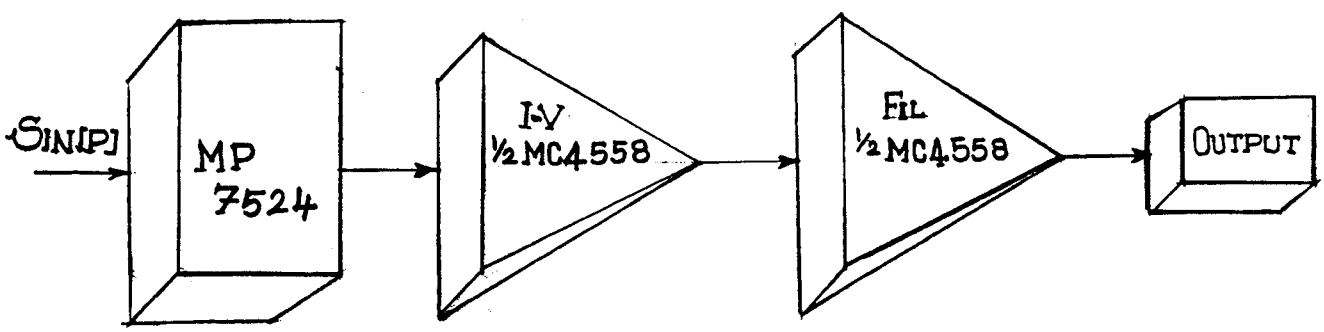


FIG 12 CONVERTER AND OUTPUT STAGE

clock pulse, a new sum is presented at the output of the latch. The output of each adder then stabilizes with the new sum allowing the cycle to repeat continuously. This sum represents the value 'P' in the theoretical discussion, while the value set by the DIP switch represent the size of each phase step.

The sine wave lookup table is contained within a single 2716 (or equivalent) EPROM providing phase to amplitude conversion. Although 24 bits are available in the phase accumulator as implemented here, only 21 bits are used to maintain compatability with readily available crystals.

The data in the EPROM represents the values generated by the mathematical function,

$$\sin(P) = 127.5 (\sin(2 \pi P/2048 - \pi /2))$$

truncated to eight bits with P taking on values from 0 to 2047, that is the address of the EPROM. The formula offsets the sine

function so that its value ranges from 0 to 255 as 'P' ranges from 0 to 2047 and avoids negative values which would complicate the next stage. This matches the function to the 2716 EPROM with its 11 bit address space and with its 8 bit output range. A C program used to generate the values in the table is shown below.

```
/* PROGRAM :-1*/
/*  THIS  PROGRAM  CALCULATES  THE  VALUE  OF  THE
SINE  FUNCTION  OFFSET  SO  THAT  THE  4th  AND  1st
QUADRANTS  CAUSE  A  CODE  FROM  0  TO  255.  CODE
IS  GENERATED  TO  FILL  A  2048  BYTE  EPROM (2716
OR  EQUIVALENT)  FOR  A  FULL  CIRCLE  OF  2*PI
RADIANS.                                          */
 #include <stdio.h>
 #include <math.h>
 main ()
 {
 double p=0;    /*PHASE INPUT TO SIN FUNCTION*/
 double S=0;    /*OUTPUT VALUE OF TRUE SIN FUNCTION*/
 int s;         /*AMPLITUDE TRUNCATED TO 8 BITS*/
 double sin()   /*TRUE SIN FUNCTION*/
 double pi=3.141592654;
 int addr =0;   /*ADDRESS OF EPROM*/
 int bytes=2048;/*SIZE OF EPROM IN BYTES*/

 printf ("        0   1   2   3   4   5   6   7   8");
 printf ("   9   A   B   C   D   E   F \n");
 while (addr < bytes)
    {
```

```
    printf ("\n%4x  ",addr);
  p = 2.0*pi*((double)addr)/((double)bytes);
  S = 127.5*(1.0+sin(p-pi/2.0));/*GIVES 0 AT -90 DEG*/
  s = ( (int) S);                    /*CONVERT TO AN INTEGER*/
  if ( S - ((double) s) > = 0.5)/*ROUNDS IF NECESSARY*/
  s++;
  printf ("   %2x",s);
  addr++;                            /*INCREMENT ADDRESS*/
  }
}
```

	0	1	2	3	4	5	6	7	8	9	a	b	c	d	e	f
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
20	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
30	1	1	1	2	2	2	2	2	2	2	2	2	2	2	2	2
40	2	3	3	3	3	3	3	3	3	3	3	3	3	4	4	4
50	4	4	4	4	4	4	4	5	5	5	5	5	5	5	5	5
60	5	6	6	6	6	6	6	6	6	7	7	7	7	7	7	7
70	7	8	8	8	8	8	8	8	9	9	9	9	9	9	9	a
80	a	a	a	a	a	a	b	b	b	b	b	b	c	c	c	c
90	c	c	d	d	d	d	d	d	e	e	e	e	e	f	f	f
a0	f	f	f	10	10	10	10	10	11	11	11	11	11	12	12	12
b0	12	12	13	13	13	13	13	14	14	14	14	14	15	15	15	15
c0	15	16	16	16	16	17	17	17	17	17	18	18	18	18	19	19
d0	19	19	1a	1a	1a	1a	1b	1b	1b	1b	1b	1c	1c	1c	1c	1d
e0	1d	1d	1d	1e	1e	1e	1e	1f	1f	1f	1f	20	20	20	21	21
f0	21	21	22	22	22	22	23	23	23	23	24	24	24	25	25	25
100	25	26	26	26	26	27	27	27	28	28	28	29	29	29	29	2a
110	2a	2a	2a	2b	2b	2b	2c	2c	2c	2d	2d	2d	2d	2e	2e	2e
120	2f	2f	2f	30	30	30	30	31	31	31	32	32	32	33	33	33
130	34	34	34	34	35	35	35	36	36	36	37	37	37	30	30	30
140	39	39	39	3a	3a	3a	3b	3b	3b	3c	3c	3c	3d	3d	3d	3e
150	3e	3e	3f	3f	3f	40	40	40	41	41	41	42	42	42	43	43
160	43	44	44	44	45	45	45	46	46	47	47	47	48	48	48	49
170	49	49	4a	4a	4a	4b	4b	4b	4c	4c	4d	4d	4d	4e	4e	4e
180	4f	4f	4f	50	50	51	51	51	52	52	52	53	53	53	54	54
190	55	55	55	56	56	56	57	57	50	50	58	59	59	59	5a	5a
1a0	5a	5b	5b	5c	5c	5c	5d	5d	5d	5e	5e	5f	5f	5f	60	60
1b0	61	61	61	62	62	62	63	63	64	64	64	65	65	65	66	66
1c0	67	67	67	68	68	69	69	69	6a	6a	6a	6b	6b	6c	6c	6c
1d0	6d	6d	6e	6c	6e	6f	6f	70	70	70	71	71	71	72	72	73
1e0	73	73	74	74	75	75	75	76	76	77	77	77	78	78	78	79
1f0	79	7a	7a	7a	7b	7b	7c	7c	7c	7d	7d	7c	7e	7c	7f	7f
200	80	80	80	81	81	81	82	82	83	83	83	84	84	85	85	85
210	86	86	87	87	87	80	88	80	89	89	8a	8a	8a	8b	8b	8c
220	8c	8c	8d	8d	8e	8e	8e	8f	8f	8f	90	90	91	91	91	92
230	92	93	93	93	94	94	95	95	95	96	96	96	97	97	90	98
240	98	99	99	9a	9a	9a	9b	9b	9b	9c	9c	9d	9d	9d	9e	9e
250	9e	9f	9f	a0	a0	a0	a1	a1	a2	a2	a2	a3	a3	a3	a4	a4
260	a5	a5	a5	a6	a6	a6	a7	a7	a7	a8	a8	a9	a9	a9	aa	aa
270	aa	ab	ab	ac	ac	ac	ad	ad	ad	ac	ac	ac	af	af	b0	b0
280	b0	b1	b1	b1	b2	b2	b2	b3	b3	b4	b4	b4	b5	b5	b5	b6
290	b6	b6	b7	b7	b7	b8	b8	b0	b9	b9	ba	ba	ba	bb	bb	bb
2a0	bc	bc	bc	bd	bd	bd	be	be	be	bf	bf	bf	c0	c0	c0	c1
2b0	c1	c1	c2	c2	c2	c3	c3	c3	c4	c4	c4	c5	c5	c5	c6	c6
2c0	c6	c7	c7	c7	c8	c8	c8	c9	c9	c9	ca	ca	ca	cb	cb	cb
2d0	cb	cc	cc	cc	cd	cd	cd	ce	ce	ce	cf	cf	cf	cf	d0	d0
2e0	d0	d1	d1	d1	d2	d2	d2	d2	d3	d3	d3	d4	d4	d4	d5	d5
2f0	d5	d5	d6	d6	d6	d7	d7	d7	d7	d8	d8	d0	d9	d9	d9	d9
300	da	da	da	da	db	db	db	dc	dc	dc	dc	dd	dd	dd	dd	de
310	de	de	dc	df	df	df	e0	e0	e0	e0	e1	e1	e1	e1	e2	e2
320	e2	e2	e3	e3	e3	e3	e4	e4	e4	e4	e4	e5	e5	e5	e5	e6
330	e0	e6	e6	e7	e7	e7	e7	e8	e8	e8	e8	e8	e9	e9	e9	e9
340	ea	ea	ea	ea	ea	eb	eb	eb	eb	eb	ec	ec	ec	ec	ec	ed

350	ed	ed	cd	cd	ce	ce	ce	ce	ee	ef	ef	ef	ef	ef	f0	f0
360	f0	f0	f0	f0	f1	f1	f1	f1	f1	f2	f2	f2	f2	f2	f2	f3
370	f3	f3	f3	f3	f3	f4	f4	f4	f4	f4	f4	f5	f5	f5	f5	f5
380	f5	f5	f6	f6	f6	f6	f6	f6	f6	f6	f7	f7	f7	f7	f7	f7
390	f8	f8	f8	f8	f8	f8	f8	f8	f9	f9	f9	f9	f9	f9	f9	f9
3a0	fa	fa	fa	fa	fa	fa	fa	fa	fa	fa	fb	fb	fb	fb	fb	fb
3b0	fb	fb	fb	fb	fc	fc	fc	fc	fc	fc	fc	fc	fc	fc	fc	fc
3c0	fd	fd	fd	fd	fd	fd	fd	fd	fd	fd	fd	fd	fd	fd	fe	fe
3d0	fe	fe	fe	fe	fe	fe	fe	fe	fe	fe	fe	fe	fe	fe	fe	fe
3e0	fe	fe	fe	fe	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff
3f0	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff
400	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff
410	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	fe	fe	fc
420	fe	fe	fe	fe	fe	fe	fe	fe	fe	fe	fe	fe	fe	fe	fe	fe
430	fe	fe	fc	fd	fd	fd	fd	fd	fd	fd	fd	fd	fd	fd	fd	fd
440	fd	fc	fc	fc	fc	fc	fc	fc	fc	fc	fc	fc	fc	fc	fb	fb	fb
450	fb	fb	fb	fb	fb	fb	fb	fa	fa	fa	fa	fa	fa	fa	fa	fa
460	fa	f9	f9	f9	f9	f9	f9	f9	f9	f8	f8	f8	f8	f8	f8	f8
470	f8	f7	f7	f7	f7	f7	f7	f7	f6	f6	f6	f6	f6	f6	f6	f5
480	f5	f5	f5	f5	f5	f5	f4	f4	f4	f4	f4	f4	f3	f3	f3	f3
490	f3	f3	f2	f2	f2	f2	f2	f2	f1	f1	f1	f1	f1	f0	f0	f0
4a0	f0	f0	f0	ef	ef	ef	ef	ef	ee	ee	ee	ee	ee	cd	ed	ed
4b0	ed	ed	ec	ec	ec	ec	ec	eb	eb	eb	eb	eb	ea	ea	ea	ea
4c0	ea	e9	e9	e9	e9	e8	e8	e8	e8	e8	e7	e7	e7	e7	e6	e6
4d0	e6	e6	e5	e5	e5	e5	e4	e4	e4	e4	e4	e3	e3	e3	e3	e2
4e0	e2	e2	e2	e1	e1	e1	e1	e0	e0	e0	e0	df	df	df	de	de
4f0	de	dc	dd	dd	dd	dd	dc	dc	dc	dc	db	db	db	da	da	da
500	da	d9	d9	d9	d9	d8	d8	d8	d7	d7	d7	d7	d6	d6	d6	d5
510	d5	d5	d5	d4	d4	d4	d3	d3	d3	d2	d2	d2	d2	d1	d1	d1
520	d0	d0	d0	cf	cf	cf	cf	ce	ce	ce	cd	cd	cd	cc	cc	cc
530	cb	cb	cb	cb	ca	ca	ca	c9	c9	c9	c8	c8	c8	c7	c7	c7
540	c6	c6	c6	c5	c5	c5	c4	c4	c4	c3	c3	c3	c2	c2	c2	c1
550	c1	c1	c0	c0	c0	bf	bf	bf	be	be	be	bd	bd	bd	bc	bc
560	bc	bb	bb	bb	ba	ba	ba	b9	b9	b8	b8	b8	b7	b7	b7	b6
570	b6	b6	b5	b5	b5	b4	b4	b4	b3	b3	b2	b2	b2	b1	b1	b1
580	b0	b0	b0	af	af	ae	ae	ae	ad	ad	ad	ac	ac	ac	ab	ab
590	aa	aa	aa	a9	a9	a9	a8	a0	a7	a7	a7	a6	a6	a6	a5	a5
5a0	a5	a4	a4	a3	a3	a3	a2	a2	a2	a1	a1	a0	a0	a0	9f	9f
5b0	9c	9e	9c	9d	9d	9d	9c	9c	9b	9b	9b	9a	9a	9a	99	99
5c0	98	98	98	97	97	96	96	96	95	95	95	94	94	93	93	93
5d0	92	92	91	91	91	90	90	8f	8f	8f	8e	8e	8e	8d	8d	8c
5e0	8c	8c	8b	8b	8a	8a	8a	89	89	88	88	88	87	87	87	86
5f0	86	85	85	85	84	84	83	83	83	82	82	81	81	81	80	80
600	7f	7f	7f	7e	7e	7e	7d	7d	7c	7c	7c	7b	7b	7a	7a	7a
610	79	79	78	78	78	77	77	77	76	76	75	75	75	74	74	73
620	73	73	72	72	71	71	71	70	70	70	6f	6f	6e	6e	6e	6d
630	6d	6c	6c	6c	6b	6b	6a	6a	6a	69	69	69	68	68	67	67
640	67	66	66	65	65	65	64	64	64	63	63	62	62	62	61	61
650	61	60	60	5f	5f	5f	5e	5e	5d	5d	5d	5c	5c	5c	5b	5b
660	5a	5a	5a	59	59	59	58	58	58	57	57	56	56	56	55	55
670	55	54	54	53	53	53	52	52	52	51	51	51	50	50	4f	4f
680	4f	4e	4e	4e	4d	4d	4d	4c	4c	4b	4b	4b	4a	4a	4a	49
690	49	49	48	48	48	47	47	47	46	46	45	45	45	44	44	44
6a0	43	43	43	42	42	42	41	41	41	40	40	40	3f	3f	3f	3e
6b0	3e	3e	3d	3d	3d	3c	3c	3c	3b	3b	3b	3a	3a	3a	39	39
6c0	39	38	38	38	37	37	37	36	36	36	35	35	35	34	34	34

6d0	34	33	33	33	32	32	32	31	31	31	30	30	30	30	2f	2f
6e0	2f	2e	2e	2e	2d	2d	2d	2d	2c	2c	2c	2b	2b	2b	2a	2a
6f0	2a	2a	29	29	29	28	28	28	28	27	27	27	26	26	26	26
700	25	25	25	25	24	24	24	23	23	23	23	22	22	22	22	21
710	21	21	21	20	20	20	1f	1f	1f	1f	1e	1e	1e	1e	1d	1d
720	1d	1d	1c	1c	1c	1c	1b	1b	1b	1b	1b	1a	1a	1a	1a	19
730	19	19	19	18	18	18	18	17	17	17	17	17	16	16	16	16
740	15	15	15	15	15	14	14	14	14	14	13	13	13	13	13	12
750	12	12	12	12	11	11	11	11	11	10	10	10	10	10	f	f
760	f	f	f	f	e	e	e	e	e	d	d	d	d	d	d	c
770	c	c	c	c	c	b	b	b	b	b	b	a	a	a	a	a
780	a	a	9	9	9	9	9	9	9	8	8	8	8	8	8	8
790	7	7	7	7	7	7	7	7	6	6	6	6	6	6	6	6
7a0	5	5	5	5	5	5	5	5	5	5	4	4	4	4	4	4
7b0	4	4	4	4	3	3	3	3	3	3	3	3	3	3	3	3
7c0	2	2	2	2	2	2	2	2	2	2	2	2	2	2	1	1
7d0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
7e0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
7f0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The values generated using the above program is shown below for different address location. Since the EPROM selected has only 11 address lines, only 11 lines from the accumulator are used in this application. The eight bits at the output of the EPROM are a digital representation of the amplitude of the sine wave and must be converted into an analog voltage before being filtered and buffered.

Since simplicity and low cost were design goals of this project, the output of the EPROM is latched by another 74LS374, which allows the full clock period for the EPROM output to settle, permitting the use of inexpensive slow EPROM's. The latch also guarantees a glitch free input to the D to A converter section.

The D to A converter is accomplisned using a MP7524 8 bit D to A converter. The output of the converter is a current propor

tional to the digital value present on its 8 bit parallel input. The current is set by resistor R8 connected between pins corresponding VR + and V + of the DAC to a maximum of 1.06mA. The digital word presented to the D to A varies from 0 to 255, forcing the current output to vary from 0 to (255/256) * 1.06mA. The current is then fed to an op-amp (ie.) IC 4-b of FIG(13) which converts it to a voltage that varies from 0 to approximately 1 Volt.

The complete circuit for the phase accumulator is shown in FIG(14) and the circuit for the analog section is shown in FIG(14).

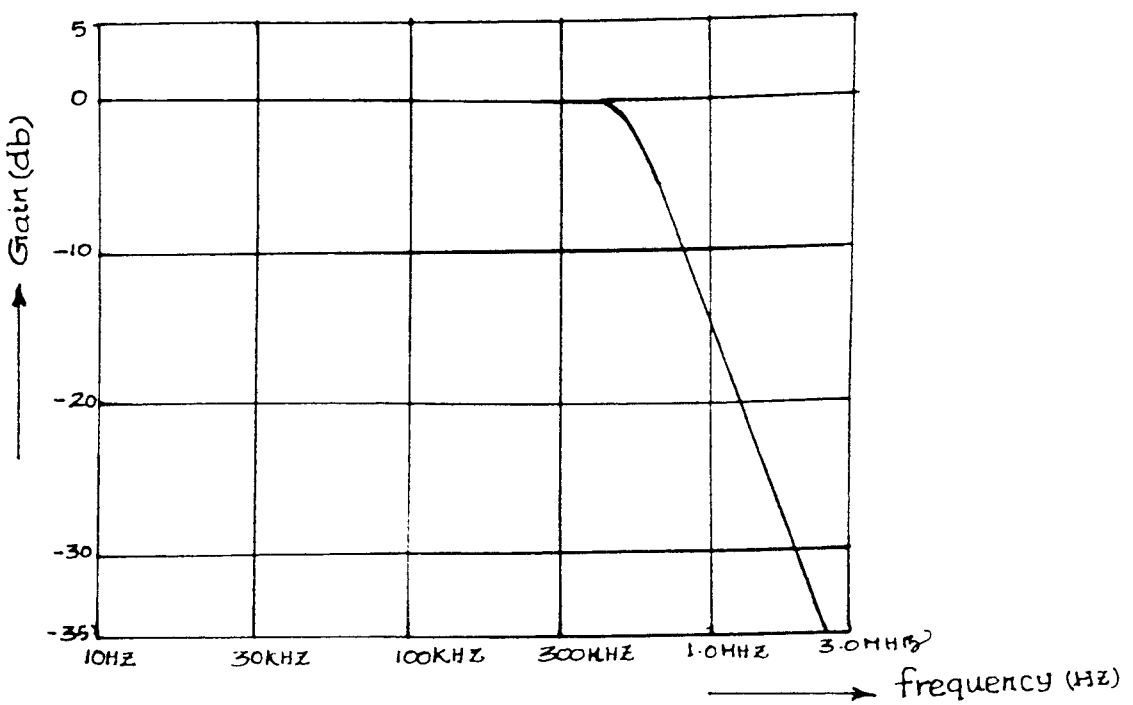
First order Filtering is accomplished by capacitor C9 in this conversion stage of IC 4-b. Op-amp IC 4 provides additional filtering to further smooth out the steps in the sine approximation. The output of this two pole filter is AC coupled to the output connection.

FIG(15) shows the relative response of the filtering, provided in the output stage. The corner frequency of the filter is set by the formula

$$fc = 1/(2 * \pi * R7 * C10 * R6 * C11)$$

which for the values assumed in the circuit is equal to 482 k Hz. A high speed op-amp is required in this stage to effectively filter the waveform. The 4558 op-amp used here is a good compramise between performance and cost.

The clock for all functions is provided by a crystal oscillator running at 4.194304 MHz, which happens to be exactly the 22nd power of 2. The clock is divided by 2 to provide the phase accumulator clock and EPROM latch clock. Additional inverters are used as delay elements to ensure that the latches are clocked at precisely the right instant to prevent glitches. With the clock and timing as such, EPROM s with access



FIG(15) Lowpass Filter Response

times as slow as 475ns can be used.

With 21 bits of the phase accumulator used and the clock frequency of 4.194304/2 MHz (fc), the output resolution is precisely 1Hz. Since 19 bits are presented as the input to the phase accumulator by the DIP switch, the output frequency is :

$$2^{19} * \frac{fc}{2^{21}} = \frac{fc}{4}$$

$$= 524.288 \text{ kHz}$$

While a DDS system can approach fc/2, fc/4 was chosen as a maximum to limit the total distortion in the output waveform. The top frequency is actually 1Hz less than that because the maximum setting is $2^{19} - 1$ for a 19 bit binary input. The filter roll off shown in FIG(15) attenuates clock-related distortion by over 30 to 1.

SPECIFICATIONS

FREQUENCY RANGE	:	1Hz TO 524.287 kHz
RESOLUTION	:	1Hz OVER COMPLETE RANGE
ACCURACY	:	DEPENDS ON CRYSTAL, TYPE, 0.005%
OUTPUT	:	LOW DISTORTION SINE WAVE
OUTPUT AMPLITUDE	:	APPROXIMATELY 1 VOLT PEAK - TO - PEAK, DECREASES AT TOP END
POWER REQUIREMENTS	:	+ 5V AT APPROX. 250mA - 5V AT APPROX. 50mA

Since the DDS is a sampled data system, an obvious source of errors is the finite quantization of a sine wave as amplitude values in the waveform map. Predictably, the final output sine wave will exhibit distortion; however, the distortion of the DDS is generally not harmonic value to the sine value itself, but rather the result of the arithmetic shifts of the original spectrum which are spaced according to the sampling frequency. This sampling effect produces image responses above and below the clock frequency, in addition to the desired fundamental. The predictable frequencies for these images may be derived from :

$$f_{img} = (N * f_{clk}) \pm f_{out}$$

where $N = 0, 1, 2, \ldots$

These images must be filtered using a low pass (or band pass) filter at the DAC output.

Properties of the waveform map relative to the DAC are another predictable source of

spurious energy in a DDS system. The basic purpose of the waveform map is to translate quantized phase values into quantized amplitude values for presentation to the DAC. Typically, a waveform map contains 180° of time-phase addressed amplitude information for a cosine function. The cosine is often used instead of the sine in order to minimize amplitude errors at zero crossings and to provide for synchronization of delta phase changes with peaks in the carrier waveform (zero slope points).

In general, DDS implementations truncate the Band width of the overall accumulator chain prior to input to the waveform map, which in turn outputs an amplitude resolution appropriate to the bit width of the DAC. The truncation of the resolution of the phase value introduces jitter in the output waveform which appears spurs in the spectrum, and the amplitude quantization of the object waveform also produces spurs. Phase truncation

errors in most DDS devices contribute spurs no greater than about -70dbc, but the behaviour of typical DAC's is likely to result in a higher figure for spurious content derived from amplitude related factors.

It is important to note that the intrinsic quantization errors of the DDS topology do not necessarily appear as uniformly distributed noise across the Nyquist band width, as conventional wisdom might imply. In general, depending upon the specific properties of the DDS, its waveform maps and D to A converter (i.e., band width of the phase accumulator vs band width of the maps vs resolution and other attributes of the DAC), quantization errors will repeat periodically at certain frequencies and produce additional spurs in the output. This occurs as a result of differential non linearity of the DAC which becomes apparent when exact phase sequence values and hence, exact amplitude values input to the DAC are repeated.

Current wisdom regarding DDS application is that the most significant source of spurious signal content is the result of DAC quantization errors. However, it would appear that essentially all currently available DDS/DAC combinations result in spurs no greater than -60dbc. In general, the so called 6db-per-DAC-bit rule (quantization SNR = 10.8db + 6db-per-bit resolution) cannot be used as a prediction of DAC spur levels for reasons cited in the preceding paragraph; and DDS/DAC combinations do not always appear to behave in strict compliance with the expected 6db slope.

Modulation basically consists of varying in the time domain one or more of the three primary signal parameters; frequency, phase, or amplitude. In order to quickly understand how Direct Digital Modulation of these signal parameters might be accomplished, consider the following general equation for a

signal.

$$s(t) = Af(wt + \phi),$$

where

A is the signal amplitude?

w is the signal frequency in radians

ϕ is the signal base phase

$f(*)$ is the signal waveshape function

Modulating this general signal consists of introducing variations in time upon the basic signal parameters, which in the general case produces the equation

$$s(t) = A(t)f(w(t)t + \phi(t))$$

where

$A(t)$ is the amplitude modulation

$w(t)$ is the frequency modulation

$\phi(t)$ is the phase modulation

CHAPTER 6

GENERATION OF SQUARE WAVE USING DDS

Many applications do not require sine waves. In timing applications, square waves are one's need. Because DDS is digital technique one would expect that a square wave output would be natural. Alas, the DDS does not produce a square wave.

The problem stems from the fact that a DDS design is a synchronous digital system. Its state will change, along with any output, only in response to a clock edge. The resolution of any output cycle is therefore limited by the clock period; the duration of any individual output cycle must be an integer number of clock periods.

Changing the output frequency by 1Hz involves a change in the output period of

far smaller than the clock period of any current DDS. Any variation from the required period is modulation, which creates side bands and spurs. Because the time quantization is too coarse to achieve the necessary signal quality, interpolation is necessary. The DDS output Low Pass Filter (LPF) performs the interpolation. Because the LPF is built from fixed components, it qualifies as an LTI (Linear Time Invariant) network. LTI networks have "a natural frequency" which is sinusoidal; one obtains the highest quality output signals by driving the filters with sinusoidal signals. This purpose underlies the cosine waveform map and the DAC. To effectively filter the phase information, one must make the LPF as perfect as possible. The LPF will then perform the required time interpolation and yield an error free signal. But it is a sine wave. To make it square, one must employ amplitude limiting, usually with a comparator of some sort.

So to generate a square waveform, a sine wave is generated first and then it is amplitude limited using a comparator of very high speed.

CHAPTER 7

CONCLUSION

Even though in the DDS prototype demonstration, Dual Input Port (DIP) switches have been used to program the required bit rate. However in actual requirements, DIP switches can be replaced and interfaced to a PC bus and the required bit rate can be programmed from the PC console.

Eventhough in this prototype, SSI, MSI digital logic devices have been used to demonstrate the concept. Same thing can be implemented using programmable logic devices like Erasable Programmable Logic Devices (EPLD), Field Programmable Gate Array (FPGA) etc. to reduce the size, power consumption and cost.

The DDS described here is an open loop circuit and does not use feedback to ensure output frequency accuracy.

Simultaneously achieving fine frequency resolution, fast switching speed and low phase noise are its Hallmark.

This is infact a Numeric method where it uses numeric means to represent quantities. It also has the advantage of being a purely digital circuit.

Because of these Hallmarks of DDS and the versatality of the circuit used, the DDS method was finally chosen for telemetry simulation.

BIBLIOGRAPHY

1. Taub and Schilling., "Principles of Communication Systems". Tata Mc Graw Hill 1991.

2. Tierney, J., Rader, C., & Gold, B., "A Digital Frequency Synthesizer", IEEE transactions on audio and electronics 1983.

3. Nossen, E., "Digital Frequency Synthesis", United States Patent 1977.

4. Gallant, J., "Direct Digital Synthesizers devices refined the art of Frequency Synthesis", EDN 1976.

5. Eisenson, H., "Frequency hopping with Direct Digital Synthesis", R.F. Design 1972.

TYPES SN54283, SN54LS283, SN54S283, SN74283, SN74LS283, SN74S283
4-BIT BINARY FULL ADDERS WITH FAST CARRY

OCTOBER 1976—REVISED DECEMBER 1983

- Full-Carry Look-Ahead Across the Four Bits
- Systems Achieve Partial Look-Ahead Performance with the Economy of Ripple Carry
- Supply Voltage and Ground on Corner Pins to Simplify P-C Board Layout

TYPICAL ADD TIMES

TYPE	TWO 8-BIT WORDS	TWO 16-BIT WORDS	TYPICAL POWER DISSIPATION PER ADDER
'283	23ns	43ns	310 mW
'LS283	25ns	46ns	95 mW
'S283	15ns	30ns	510 mW

description

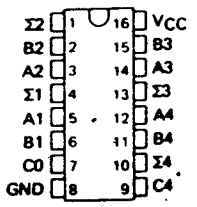
The '283 and 'LS283 adders are electrically and functionally identical to the '83A and 'LS283, respectively; only the arrangement of the terminals has been changed. The 'S283 high performance versions are also functionally identical.

These improved full adders perform the addition of two 4-bit binary words. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look-ahead across all four bits generating the carry term in ten nanoseconds, typically, for the '283 and 'LS283, and 7.5 nanoseconds for the 'S283. This capability provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

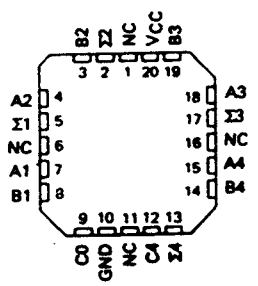
The adder logic, including the carry, is implemented in its true form. End around carry can be accomplished without the need for logic or level inversion.

Series 54, Series 54LS, and Series 54S circuits are characterized for operation over the full temperature range of −55°C to 125°C. Series 74, Series 74LS, and Series 74S circuits are characterized for 0°C to 70°C operation.

SN54283, SN54LS283 . . . J OR W PACKAGE
SN54S283 . . . J PACKAGE
SN74283 . . . J OR N PACKAGE
SN74LS283, SN74S283 . . . D, J OR N PACKAGE
(TOP VIEW)



SN54LS283, SN54S283 . . . FK PACKAGE
SN74LS283, SN74S283 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUT				OUTPUT WHEN C0 = L			OUTPUT WHEN C0 = H		
				WHEN C2 = L			WHEN C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = high level, L = low level

NOTE: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs $\Sigma 1$ and $\Sigma 2$ and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs $\Sigma 3$, $\Sigma 4$, and C4.

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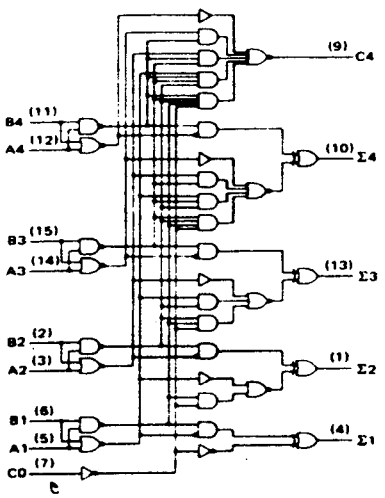
TYPES SN54283, SN54LS283, SN54S283, SN74283, SN74LS283, SN74S283
4-BIT BINARY FULL ADDERS WITH FAST CARRY

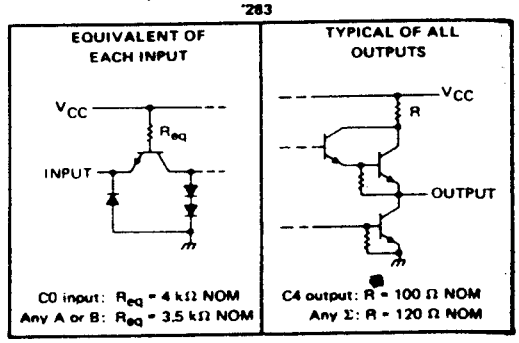
logic diagram



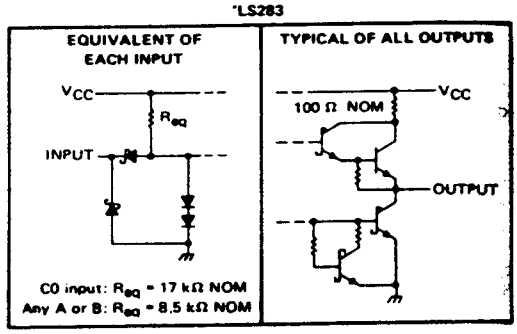
Pin numbers shown on logic notation are for D, J or N packages.

schematics of inputs and outputs

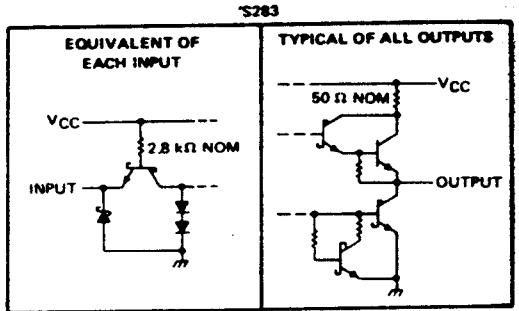
'283



'LS283



'S283



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7V
Input voltage: '283, 'S283		5.5V
'LS283		7V
Interemitter voltage (see Note 2)		5.5V
Operating free-air temperature range:	SN54283, SN54LS283, SN54S283	−55°C to 125°C
	SN74283, SN74LS283, SN74S283	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTES 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple emitter transistor. This rating applies for the '283 and 'S283 only between the following pairs: A1 and B1, A2 and B2, A3 and B3, A4 and B4.

recommended operating conditions

		SN54283			SN74283			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Any output except C4			−800			−800	μA
	Output C4			−400			−400	
Low-level output current, I_{OL}	Any output except C4			16			16	mA
	Output C4			8			8	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54283			SN74283			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.6		2.4	3.6		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX			0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.4 V				40			40	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	Any output except C4	V_{CC} = MAX		−20		−55	−18		−55	mA
		Output C4			−20		−70	−18		−70	
I_{CC}	Supply current		V_{CC} = MAX, Outputs open	All B low, other inputs at 4.5 V		56			56		mA
				All inputs at 4.5 V		66	99		66	110	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C
§ Only one output should be shorted at a time

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C0	Any Σ	C_L = 15 pF, R_L = 400 Ω, See Note 3		14	21	ns
t_{PHL}					12	21	
t_{PLH}	A_i or B_i	Σ_i			16	24	ns
t_{PHL}					16	24	
t_{PLH}	C0	C4	C_L = 15 pF, R_L = 780 Ω, See Note 3		9	14	ns
t_{PHL}					11	16	
t_{PLH}	A_i or B_i	C4			9	14	ns
t_{PHL}					11	16	

¶ t_{PLH} Propagation delay time, low to high level output
t_{PHL} Propagation delay time, high to low level output
NOTE 3 See General Information Section for load circuits and voltage waveforms

recommended operating conditions

	SN54LS283			SN74LS283			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS283			SN74LS283			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	Any A or B	V_{CC} = MAX, V_I = 7 V				0.2			0.2	mA
		C0					0.1			0.1	
I_{IH}	High-level input current	Any A or B	V_{CC} = MAX, V_I = 2.7 V				40			40	μA
		C0					20			20	
I_{IL}	Low-level input current	Any A or B	V_{CC} = MAX, V_I = 0.4 V				−0.8			−0.8	mA
		C0					−0.4			−0.4	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, Outputs open	All inputs grounded		22	39		22	39	mA
				All B low, other inputs at 4.5 V		19	34		19	34	
				All inputs at 4.5 V		19	34		19	34	

†For conditions shown as MIN or MAX, see the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Only one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C0	Any Σ	C_L = 15 pF, R_L = 2 kΩ, See Note 3		16	24	ns
t_{PHL}					15	24	
t_{PLH}	A_i or B_i	Σ_i			15	24	ns
t_{PHL}					15	24	
t_{PLH}	C0	C4			11	17	ns
t_{PHL}					11	22	
t_{PLH}	A_i or B_i	C4			11	17	ns
t_{PHL}					12	17	

¶t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output
NOTE 3: See General Information Section for load circuits and voltage waveforms.

recommended operating conditions

		SN54S283			SN74S283			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Any output except C4			−1			−1	mA
	Output C4			−500			−500	μA
Low-level output current, I_{OL}	Any output except C4			20			20	mA
	Output C4			10			10	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.2	V
V_{OH}	High-level output voltage	SN54S283	V_{CC} = MIN,	V_{IH} = 2 V,	2.5	3.4		V
		SN74S283	V_{IL} = 0.8 V,	I_{OH} = MAX	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			50	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.5 V			−2	mA
I_{OS}	Short-circuit output current§	Any output except C4	V_{CC} = MAX		−40		−100	mA
		Output C4			−20		−100	
I_{CC}	Supply current		V_{CC} = MAX, Outputs open	All S low, other inputs at 4.5 V		80		mA
				All inputs at 4.5 V		96	160	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C0	Any Σ	C_L = 15 pF, R_L = 280 Ω, See Note 3		11	18	ns
t_{PHL}					12	18	
t_{PLH}	A_i or B_i	Σ_i			12	18	ns
t_{PHL}					11.5	18	
t_{PLH}	C0	C4	C_L = 15 pF, R_L = 660 Ω, See Note 3		6	11	ns
t_{PHL}					7.5	11	
t_{PLH}	A_i or B_i	C4			7.5	12	ns
t_{PHL}					8.5	12	

¶t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output

NOTE 3: See General Information Section for load circuits and voltage waveforms

TYPES SN54LS373, SN54LS374, SN54S373, SN54S374, SN74LS373, SN74LS374, SN74S373, SN74S374
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

OCTOBER 1975 – REVISED APRIL 1985

- Choice of 8 Latches or 8 D-Type Flip-Flops In a Single Package
- 3-State Bus-Driving Outputs
- Full Parallel-Access for Loading
- Buffered Control Inputs
- Clock/Enable Input Has Hysteresis to Improve Noise Rejection ('S373 and 'S374)
- P-N-P Inputs Reduce D-C Loading on Data Lines ('S373 and 'S374)

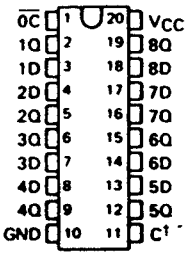
'LS373, 'S373
FUNCTION TABLE

OUTPUT ENABLE	ENABLE LATCH	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

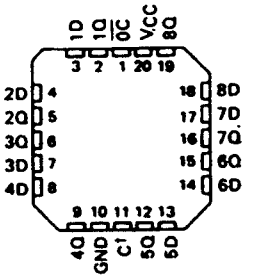
'LS374, 'S374
FUNCTION TABLE

OUTPUT ENABLE	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

SN54LS373, SN54LS374, SN54S373, SN54S374 . . . J PACKAGE
SN74LS373, SN74LS374, SN74S373, SN74S374 . . . DW, J OR N PACKAGE
(TOP VIEW)



SN54LS373, SN54LS374, SN54S373, SN54S374 . . . FK PACKAGE
SN74LS373, SN74LS374, SN74S373, SN74S374 . . . FN PACKAGE
(TOP VIEW)



'C for 'LS373 and 'S373; CLK for 'LS374 and 'S374

description

These 8-bit registers feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'LS373 and 'S373 are transparent D-type latches meaning that while the enable (C) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

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description (continued)

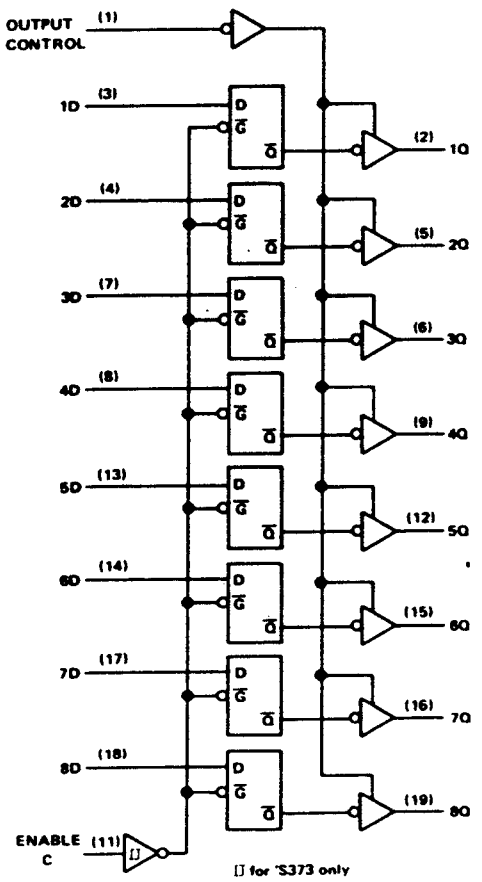
The eight flip-flops of the 'LS374 and 'S374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were setup at the D inputs.

Schmitt-trigger buffered inputs at the enable/clock lines of the 'S373 and 'S374 devices, simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high impedance state. In the high impedance state the outputs neither load nor drive the bus lines significantly.

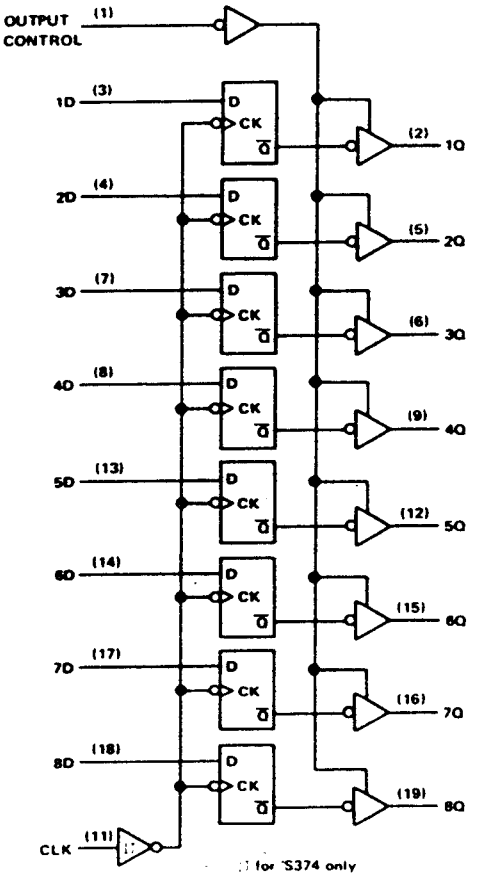
The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

logic diagrams

'LS373, 'S373
TRANSPARENT LATCHES



'LS374, 'S374
POSITIVE-EDGE-TRIGGERED FLIP-FLOPS



Pin numbers shown on logic notation are for DW, J or N packages

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS'	−55°C to 125°C
SN74LS'	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54LS'			SN74LS'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{OH}	High-level output voltage				5.5			5.5	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Pulse duration	CLK high	15			15			ns
		CLK low	15			15			
t_{su}	Data setup time	'LS373	5↓			5↓			ns
		'LS374	20↑			20↑			
t_h	Data hold time	'LS373	20↓			20↓			ns
		'LS374†	0↑			0↑			
T_A	Operating free-air temperature		−55		125	0		70	°C

† The t_h specification applies only for data frequency below 10 MHz. Designs above 10 MHz should use a minimum of 5 ns.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max, I_{OH} = MAX		2.4	3.4		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.7 V				20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.4 V				−20			−20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX, Output control at 4.5 V	'LS373		24	40		24	40	mA
			'LS374		27	40		27	40	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

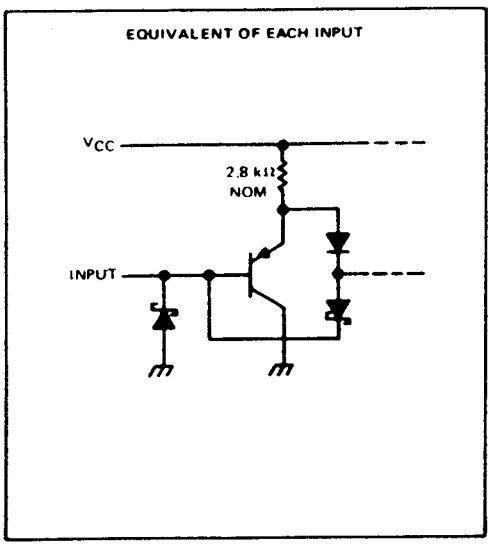
switching characteristics, V_{CC} = 5 V, T_A = 25°C

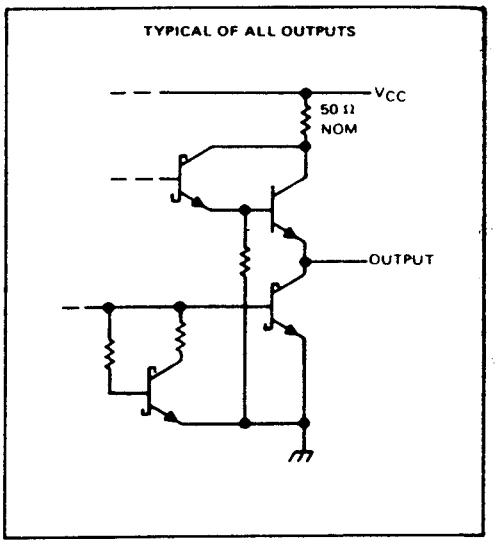
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		'LS373 MIN	'LS373 TYP	'LS373 MAX	'LS374 MIN	'LS374 TYP	'LS374 MAX	UNIT
f_{max}			C_L = 45 pF, R_L = 667 Ω See Notes 2 and 3					35	50		MHz
t_{PLH}	Data	Any Q				12	18				ns
t_{PHL}						12	18				
t_{PLH}	Clock or enable	Any Q				20	30		15	28	ns
t_{PHL}						18	30		19	28	
t_{PZH}	Output Control	Any Q				15	28		20	26	ns
t_{PZL}						25	36		21	28	
t_{PHZ}	Output Control	Any Q	C_L = 5 pF, R_L = 667 Ω See Note 3	SN54		28	32		28	32	ns
				SN74		15	25		15	28	
t_{PLZ}	Output Control	Any Q				12	20		12	20	ns

NOTES 2. Maximum clock frequency is tested with all outputs loaded.
3. See General Information Section for load circuits and voltage waveforms

f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{PZH} = output enable time to high level
t_{PZL} = output enable time to low level
t_{PHZ} = output disable time from high level
t_{PLZ} = output disable time from low level

schematic of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S' . . . . . −55°C to 125°C
SN74S' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S'			SN74S'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
High-level output current, I_{OH}				−2			−6.5	mA
Width of clock/enable pulse, t_w	High	6			6			ns
	Low	7.3			7.3			
Data setup time, t_{su}	'S373	0↓			0↓			ns
	'S374	5↑			5↑			
Data hold time, t_h	'S373	10↓			10↓			ns
	'S374	2↑			2↑			
Operating free-air temperature, T_A		−55		125	0		70	C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†					MIN	TYP‡	MAX	UNIT
V_{IH}							2			V
V_{IL}									0.8	V
V_{IK}		V_{CC} = MIN,	I_I = – 18 mA						– 1.2	V
V_{OH}	SN54S'	V_{CC} = MIN,	V_{IH} = 2 V,	V_{IL} = 0.8 V,	I_{OH} = MAX		2.4	3.4		V
	SN74S'						2.4	3.1		
V_{OL}		V_{CC} = MIN,	V_{IH} = 2 V,	V_{IL} = 0.8 V,	I_{OL} = 20 mA				0.5	V
I_{OZH}		V_{CC} = MAX,	V_{IH} = 2 V,	V_O = 2.4 V					50	μA
I_{OZL}		V_{CC} = MAX,	V_{IH} = 2 V,	V_O = 0.5 V					– 50	μA
I_I		V_{CC} = MAX,	V_I = 5.5 V						1	mA
I_{IH}		V_{CC} = MAX,	V_I = 2.7 V						50	μA
I_{IL}		V_{CC} = MAX,	V_I = 0.5 V						– 250	μA
I_{OS}§		V_{CC} = MAX					– 40		– 100	mA
I_{CC}		V_{CC} = MAX		'S373	outputs high				160	mA
					outputs low				160	
					outputs disabled				190	
				'S374	outputs high				110	
					outputs low				140	
					outputs disabled				160	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'S373			'S374			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			C_L = 15 pF, R_L = 280 Ω, See Notes 2 and 4				75	100		MHz
t_{PLH}	Data	Any Q			7	12				ns
t_{PHL}					7	12				
t_{PLH}	Clock or enable	Any Q			7	14		8	15	ns
t_{PHL}					12	18		11	17	
t_{PZH}	Output Control	Any Q			8	15		8	15	ns
t_{PZL}					11	18		11	18	
t_{PHZ}	Output Control	Any Q	C_L = 5 pF, R_L = 280 Ω, See Note 3		6	9		5	9	ns
t_{PLZ}					8	12		7	12	

NOTES 2. Maximum clock frequency is tested with all outputs loaded.
4. See General Information Section for load circuits and voltage waveforms

f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{PZH} = output enable time to high level
t_{PZL} = output enable time to low level
t_{PHZ} = output disable time from high level
t_{PLZ} = output disable time from low level

2732A
32K (4K x 8) PRODUCTION AND UV ERASABLE PROMS

- **200 ns (2732A-2) Maximum Access Time ... HMOS*-E Technology**
- **Compatible with High-Speed Microcontrollers and Microprocessors ... Zero WAIT State**
- **Two Line Control**
- **10% V_{CC} Tolerance Available**
- **Low Current Requirement**
  - **−100 mA Active**
  - **−35 mA Standby**
- **Int$_e$ligent Identifier™ Mode**
  - **−Automatic Programming Operation**
- **Industry Standard Pinout ... JEDEC Approved 24 Pin Ceramic and Plastic Package**

(See Packaging Spec. Order # 221369)

The Intel 2732A is a 5V-only, 32,768-bit ultraviolet erasable (cerdip) Electrically Programmable Read-Only Memory (EPROM). The standard 2732A access time is 250 ns with speed selection (2732A-2) available at 200 ns. The access time is compatible with high performance microprocessors such as the 8 MHz iAPX 186. In these systems, the 2732A allows the microprocessor to operate without the addition of WAIT states.

The 2732A is currently available in two different package types. Cerdip packages provide flexibility in prototyping and R & D environments where reprogrammability is required. Plastic DIP EPROMs provide optimum cost effectiveness in production environments. Inventoried in the unprogrammed state, the P2732A is programmed quickly and efficiently when the need to change code arises. Costs incurred for new ROM masks or obsoleted ROM inventories are avoided. The tight package dimensional controls, inherent non-erasability, and high reliability of the P2732A make it the ideal component for these production applications.

An important 2732A feature is Output Enable ($\overline{OE}$) which is separate from the Chip Enable ($\overline{CE}$) control. The $\overline{OE}$ control eliminates bus contention in microprocessor systems. The $\overline{CE}$ is used by the 2732A to place it in a standby mode ($\overline{CE}$ = V_{IH}) which reduces power consumption without increasing access time. The standby mode reduces the current requirement by 65%; the maximum active current is reduced from 100 mA to a standby current of 35 mA.

*HMOS is a patented process of Intel Corporation.

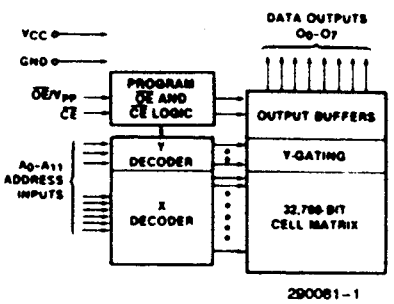
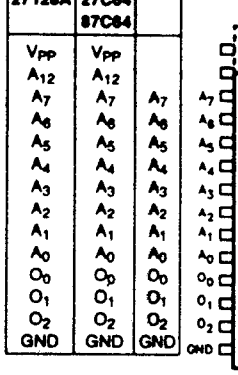


Figure 1. Block Diagram

Pin Names

A_0–A_{11}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable/V_{PP}
O_0–O_7	Outputs

27128 27128A	2764 2764A 27C64 87C64	2716
V_{PP}	V_{PP}	
A_{12}	A_{12}	
A_7	A_7	A_7
A_6	A_6	A_6
A_5	A_5	A_5
A_4	A_4	A_4
A_3	A_3	A_3
A_2	A_2	A_2
A_1	A_1	A_1
A_0	A_0	A_0
O_0	O_0	O_0
O_1	O_1	O_1
O_2	O_2	O_2
GND	GND	GND



2716	2764 2764A 27C64 87C64	27128 27128A
	V_{CC} / PGM	V_{CC} / PGM
V_{CC}	N.C.	A_{13}
A_8	A_8	A_8
A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$ / ALE/$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7
O_6	O_6	O_6
O_5	O_5	O_5
O_4	O_4	O_4
O_3	O_3	O_3

NOTE:
Intel "Universal Site" compatible EPROM configurations are shown in the blocks adjacent to the 2732A pins.

Figure 2. Cerdip/Plastic DIP Pin Configuration

Order Number: 290081-002

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

READ OPERATION

D.C. CHARACTERISTICS

Electrical Parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for:

Symbol	Parameter	TD2732A LD2732A		Test Conditions
		Min	Max	
I_{SB}	V_{CC} Standby Current (mA)		45	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC_1}(1)	V_{CC} Active Current (mA)		150	$\overline{OE} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature (mA)		125	$\overline{OE} = \overline{CE} = V_{IL}$, $V_{PP} = V_{CC}$, $T_{Ambient} = 85°C$

NOTE:
1. Maximum current value is with outputs O_0 to O_7 unloaded.

EXPRESS EPROM PRODUCT FAMILY

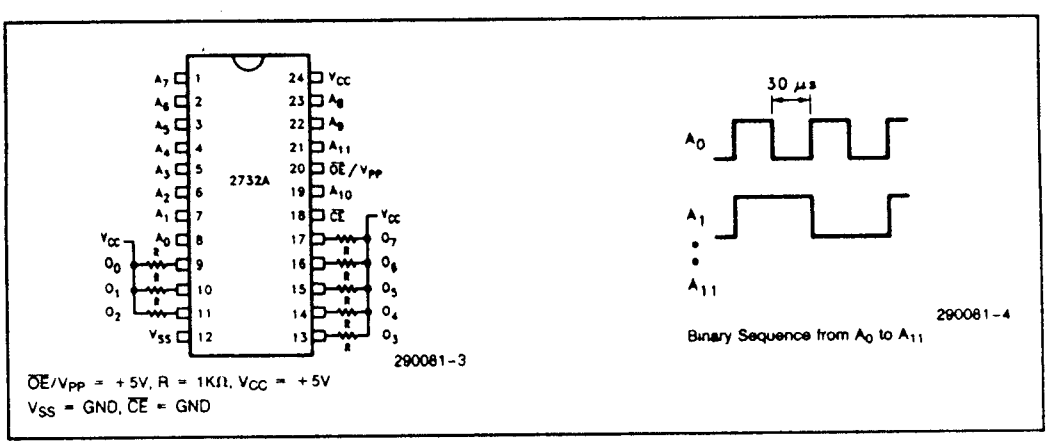
PRODUCT DEFINITONS

Type	Operating Temperature	Burn-In 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

2732A Versions

Speed Versions	Packaging Options	
	Cerdip	Plastic
−2	Q	
STD	Q, T, L	
−3	Q	
−4	Q, T, L	
−20	Q	
−25	Q, T, L	
−30	Q	
−45	Q, T, L	



Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temp. During Read .....0°C to +70°C
Temperature Under Bias .....−10°C to +80°C
Storage Temperature .....−65°C to +125°C
All Input or Output Voltages with Respect to Ground.....−0.3V to +6V
Voltage on A9 with Respect to Ground.....−0.3V to +13.5V
V_{PP} Supply Voltage with Respect to Ground During Programming .....−0.3V to +22V
V_{CC} Supply Voltage with Respect to Ground .....−0.3V to +7.0V

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

READ OPERATION

D.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ(3)	Max		
I_{LI}	Input Load Current			10	µA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current			10	µA	$V_{OUT} = 5.5V$
I_{SB}(2)	V_{CC} Current (Standby)			35	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC1}(2)	V_{CC} Current (Active)			100	mA	$\overline{OE} = \overline{CE} = V_{IL}$
V_{IL}	Input Low Voltage	−0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} + 1	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ µA

A.C. CHARACTERISTICS $0°C \le T_A \le 70°C$

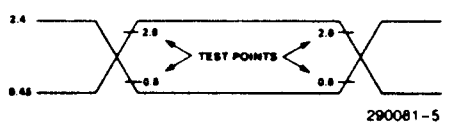
Versions	$V_{CC} \pm 5\%$	2732A-2 P2732A-2		2732A P2732A		2732A-3 P2732A-3		2732A-4 P2732A-4		Units	Test Conditions
	$V_{CC} \pm 10\%$	2732A-20		2732A-25		2732A-30		2732A-45			
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max		
t_{ACC}	Address to Output Delay		200		250		300		450	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		200		250		300		450	ns	$\overline{OE} = V_{IL}$
t_{OE}	$\overline{OE}/V_{PP}$ to Output Delay		70		100		150		150	ns	$\overline{CE} = V_{IL}$
t_{DF}(4)	$\overline{OE}/V_{PP}$ High to Output Float	0	60	0	60	0	130	0	130	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}/V_{PP}$, Whichever Occurred First	0		0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

NOTES:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. The maximum current value is with outputs O_0 to O_7 unloaded.
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.

CAPACITANCE (2) T_A = 25°C, f = 1 MHz

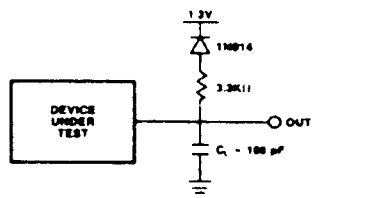
Symbol	Parameter	Typ	Max	Unit	Conditions
C_{IN1}	Input Capacitance Except $\overline{OE}/V_{PP}$	4	6	pF	V_{IN} = 0V
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance		20	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

A.C. TESTING INPUT/OUTPUT WAVEFORM



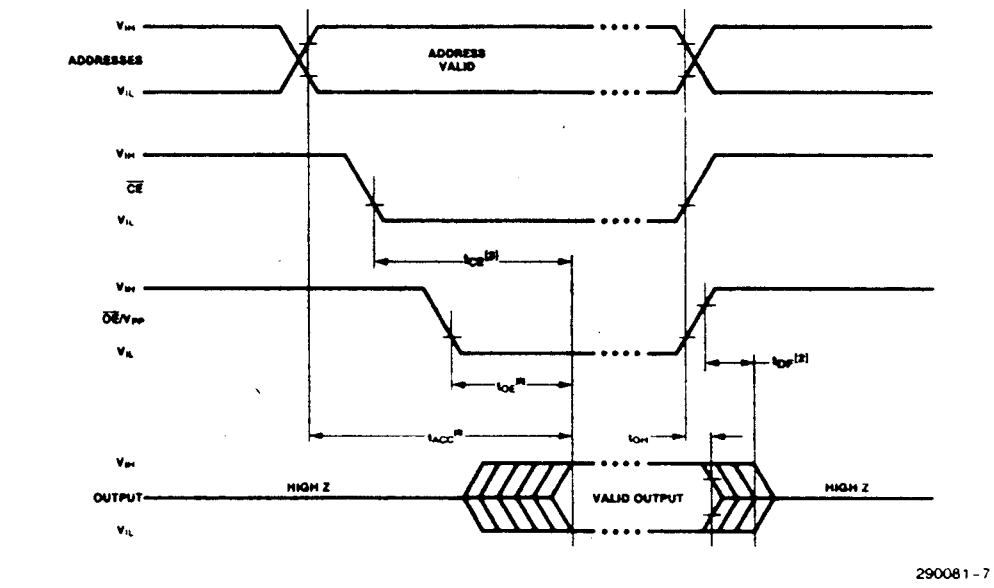
A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L Includes Jig Capacitance

A.C. WAVEFORMS



NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested. Output float is defined as the point where data is no longer driven—see timing diagram.
3. $\overline{OE}/V_{PP}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{CE}.

PLASTIC EPROM APPLICATIONS

Intel's P2732A is the result of a multi-year effort to make EPROMs more cost effective for production applications. The benefits of a plastic package enable the P2732A to be used for high volume production with lower profile boards and easier production assembly (no cover over UV transparent windows).

The reliability of plastic EPROMs is equivalent to traditional CERDIP packaging. The plastic is rugged and durable making it optimal for auto insertion and auto handling equipment. Design and testing ensures device programmability, data integrity, and impermeability to moisture.

Intel's Plastic EPROMs are designed for total compatibility with their CERDIP packaged predecessors. This encompasses quality, reliability, and programming. All Intel Plastic EPROMs have passed Intel's strict process and product reliability qualifications.

DEVICE OPERATION

The modes of operation of the 2732A are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming and 12V on A_9 for the Int$_e$ligent Identifier™ mode. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL level to 21V.

Table 1. Mode Selection

Pins / Mode	$\overline{CE}$	$\overline{OE}/V_{PP}$	A_9	A_0	V_{CC}	Outputs
Read/Program Verify	V_{IL}	V_{IL}	X	X	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC}	High Z
Standby	V_{IH}	X	X	X	V_{CC}	High Z
Program	V_{IL}	V_{PP}	X	X	V_{CC}	D_{IN}
Program Inhibit	V_{IH}	V_{PP}	X	X	V_{CC}	High Z
Int$_e$ligent Identifier[3]						
—Manufacturer	V_{IL}	V_{IL}	V_H	V_{IL}	V_{CC}	89H
—Device	V_{IL}	V_{IL}	V_H	V_{IH}	V_{CC}	01H

NOTES:
1. X can be V_{IH} or V_{IL}.
2. V_H = 12V ±0.5V.
3. A_1–A_8, A_{10}, A_{11} = V_{IL}.

Read Mode

The 2732A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}/V_{PP}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}/V_{PP}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

EPROMs can be placed in a standby mode which reduces the maximum active current of the device by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}/V_{PP}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided two control lines which accommodate this multiple memory connection. The two control lines allow for:

a) The lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}/V_{PP}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's two-line control and by use of properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for

every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PC board traces.

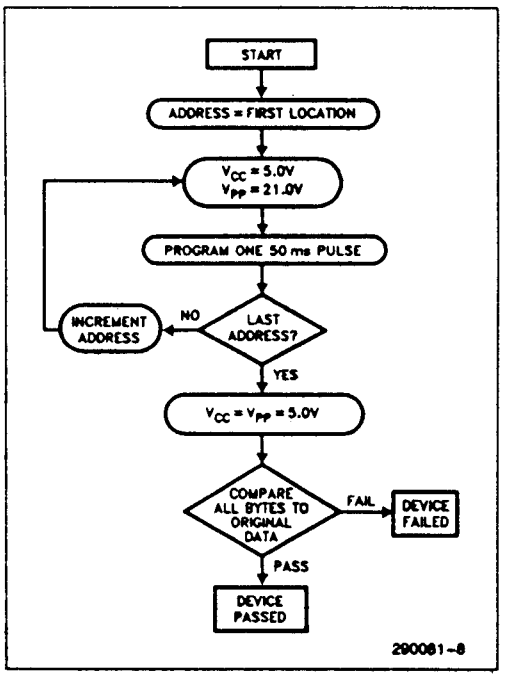


Figure 3. Standard Programming Flowchart

PROGRAMMING MODES

CAUTION: Exceeding 22V on $\overline{OE}/V_{PP}$ will permanently damage the device.

Initially, and after each erasure (cerdip EPROMs), all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" in cerdip EPROMs is by ultraviolet light erasure.

The device is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 21V. It is required that a 0.1 μF capacitor be placed across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 20 ms (50 ms typical) active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed (see Figure 3). Any location can be programmed at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 ms. The EPROM must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of multiple 2732As in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2732As may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled 2732As.

Program Inhibit

Programming of multiple EPROMs in parallel with different data is easily accomplished by using the Program Inhibit mode. A high level $\overline{CE}$ input inhibits the other EPROMs from being programmed. Except for $\overline{CE}$, all like inputs (including $\overline{OE}/V_{PP}$) of the parallel EPROMs may be common. A TTL low level pulse applied to the $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 21V will program that selected device.

Program Verify

A verify (Read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the int$_e$ligent Identifier Mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1.

INTEL EPROM PROGRAMMING SUPPORT TOOLS

Intel offers a full line of EPROM Programmers providing state-of-the-art programming for all Intel programmable devices. The modular architecture of Intel's EPROM programmers allows you to add new support as it becomes available, with very low cost add-ons. For example, even the earliest users of the iUP-FAST 27/K module may take advantage of Intel's new Quick-Pulse Programming™ Algorithm, the fastest in the industry.

Intel EPROM programmers may be controlled from a host computer using Intel's PROM Programming software (iPPS). iPPS makes programming easy for a growing list of industry standard hosts, including the IBM PC, XT, AT, and PCDOS compatibles, Intellec Development Systems, Intel's iPDS Personal Development System, and the Intel Network Development System (iNDS-II). Stand-alone operation is also available, including device previewing, editing, programming, and download of programming data from any source over an RS232C port.

For further details consult the EPROM Programming section of the Development Systems Handbook.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMS)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than aproximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for longer periods may cause permanent damage.

PROGRAMMING

D.C. PROGRAMMING CHARACTERISTICS

T_A = 25°C ±5°C, V_{CC} = 5V ±5%, V_{PP} = 21V ±0.5V

Symbol	Parameter	Limits			Units	Test Conditions (Note 1)
		Min	Typ(3)	Max		
I_{LI}	Input Current (All Inputs)			10	µA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1		0.8	V	
V_{IH}	Input High Level (All Inputs Except $\overline{OE}/V_{PP}$)	2.0		V_{CC} + 1	V	
V_{OL}	Output Low Voltage During Verify			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage During Verify	2.4			V	I_{OH} = −400 µA
I_{CC_2}(4)	V_{CC} Supply Current (Program and Verify)		85	100	mA	
I_{PP_2}(4)	V_{PP} Supply Current (Program)			30	mA	$\overline{CE} = V_{IL}$, $\overline{OE}/V_{PP} = V_{PP}$
V_{ID}	A$_9$ int$_e$ligent Identifier Voltage	11.5		12.5	V	

A.C. PROGRAMMING CHARACTERISTICS

T_A = 25°C ±5°C, V_{CC} = 5V ±5%, V_{PP} = 21V ±0.5V

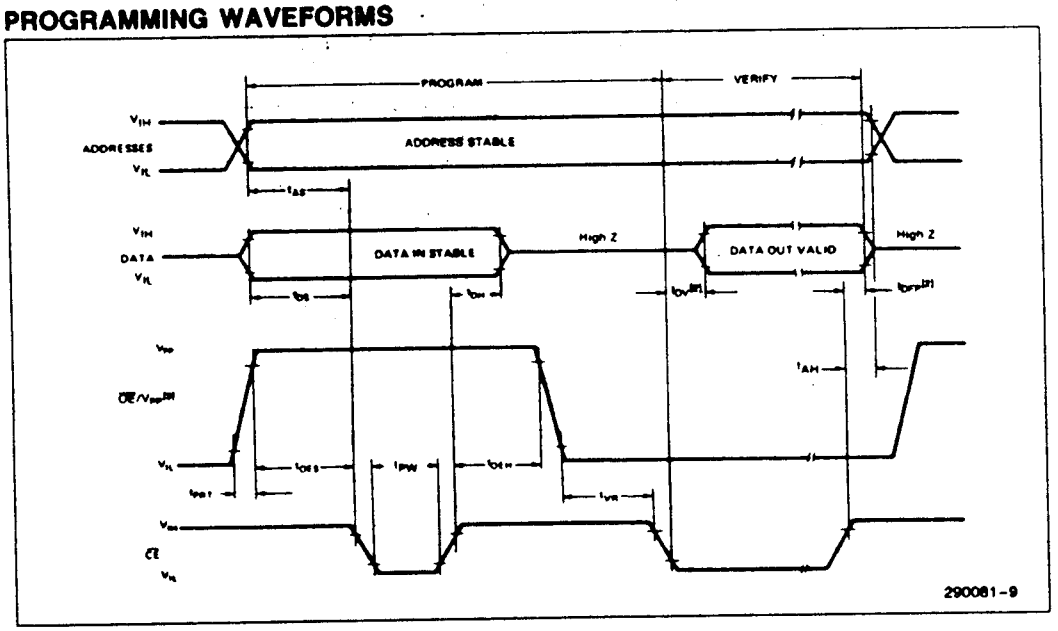
Symbol	Parameter	Limits			Units	Test Conditions* (Note 1)
		Min	Typ(3)	Max		
t_{AS}	Address Setup Time	2			µs	
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time	2			µs	
t_{DS}	Data Setup Time	2			µs	
t_{AH}	Address Hold Time	0			µs	
t_{DH}	Data Hold Time	2			µs	
t_{DFP}	$\overline{OE}/V_{PP}$ High to Output Not Driven	0		130	ns	(Note 2)
t_{PW}	$\overline{CE}$ Pulse Width During Programming	20	50	55	ms	
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time	2			µs	
t_{DV}	Data Valid from $\overline{CE}$			1	µs	$\overline{CE}$ = V_{IL}, $\overline{OE}/V_{PP}$ = V_{IL}
t_{VR}	V_{PP} Recovery Time	2			µs	
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming	50			ns	

NOTES:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. Typical values are for T_A = 25°C and nominal supply voltages.
4. The maximum current value is with outputs O_0 to O_7 unloaded.

*A.C. TEST CONDITIONS

Input Rise and Fall Time (10% to 90%) ..... ≤20 ns
Input Pulse Levels .....0.45V to 2.4V
Input Timing Reference Level .....0.8V and 2.0V
Output Timing Reference Level .....0.8V and 2.0V

PROGRAMMING WAVEFORMS



NOTES:
1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{DV} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 2732A, a 0.1μF capacitor is required across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which can damage the device.

CA741, CA747, CA748, CA1458, CA1558, LM741*, LM748*, LM1458*, LM1558*

Operational Amplifiers

High-Gain Single and Dual Operational Amplifiers
For Military, Industrial and Commerical Applications

Features:

- *Input bias current (all types)*
  500 nA max
- *Input offset current (all types)*
  200 nA max

The RCA-CA1458, CA1558 (dual types); CA741C, CA741 (single-types); CA747C, CA747 (dual types); and CA748C, CA748 (single types) are general-purpose, high-gain operational amplifiers for use in military, industrial, and commercial applications.

These monolithic silicon integrated-circuit devices provide output short-circuit protection and latch-free operation. These types also feature wide common-mode and differential-mode signal ranges and have low-offset voltage nulling capability when used with an appropriately valued potentiometer. A 5-megohm potentiometer is used for offset nulling types CA748C, CA748 (See Fig. 10); a 10-kilohm potentiometer is used for offset nulling types CA741C, CA741, CA747CE, CA747E (See Fig. 9); and types CA1458, CA1558, CA747CT, have no specific terminals for offset nulling. Each type consists of a differential-input amplifier that effectively drives a gain and level-shifting stage having a complementary emitter-follower output.

RCA's manufacturing process make it possible to produce IC operational amplifiers with low-burst ("popcorn") noise characteristics. Type CA6741, a low-noise version of the CA741, gives limit specifications for burst noise in the data bulletin, File No. 530. Contact your RCA Sales Representative for information pertinent to other operational amplifier types that meet low-burst noise specifications.

Applications:

- *Comparator*
- *DC amplifier*
- *Integrator or differentiator*
- *Multivibrator*
- *Narrow-band or band-pass filter*
- *Summing amplifier*

This operational amplifier line also offers the circuit designer the option of operation with internal or external phase compensation.

Types CA748C and CA748, which are externally phase compensated (terminals 1 and 8) permit a choice of operation for improved bandwidth and slew-rate capabilities. Unity gain with external phase compensation can be obtained with a single 30-pF capacitor. All the other types are internally phase-compensated.

RCA Type No.	No. of Ampl.	Phase Comp.	Offset Voltage Null	Min. A_{OL}	Max. V_{IO} (mV)	Operating-Temperature Range (°C)
CA1458	dual	int.	no	20k	6	0 to +70▲
CA1558	dual	int.	no	50k	5	−55 to +125
CA741C	single	int.	yes	20k	6	0 to +70▲
CA741	single	int.	yes	50k	5	−55 to +125
CA747C	dual	int.	yes*	20k	6	0 to +70▲
CA747	dual	int.	yes*	50k	5	−55 to +125
CA748C	single	ext.	yes	20k	6	0 to +70▲
CA748	single	ext.	yes	50k	5	−55 to +125

*In the 14-lead dual-in-line plastic package only.

▲All types in any package style can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to +70°C.

*Technical Data on LM Branded types is identical to the corresponding CA Branded types.

CA741, CA747, CA748, CA1458, CA1558, LM741, LM748, LM1458, LM1558

ORDERING INFORMATION

When ordering any of these types, it is important that the appropriate suffix letter for the package required be affixed to the type number. For example: If a CA1458 in a straight-lead TO-5 style package is desired, order CA1458T.

TYPE NO.	PACKAGE TYPE AND SUFFIX LETTER							FIG. NO.
	TO-5 STYLE			PLASTIC		CHIP	BEAM-LEAD	
	8L	10L	DIL-CAN	8L	14L			
CA1458	T		S	E		H		1d, 1h
CA1558	T		S	E				1d, 1h
CA741C	T		S	E		H		1a, 1e
CA741	T		S	E			L	1a, 1e
CA747C		T			E	H		1b, 1f
CA747		T			E			1b, 1f
CA748C	T		S	E		H		1c, 1g
CA748	T		S	E				1c, 1g

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^\circ C$:*

DC Supply Voltage (between V^+ and V^- terminals):
- CA741C, CA747C▲, CA748C, CA1458▲ . . . . . 36 V
- CA741, CA747▲, CA748, CA1558▲ . . . . . 44 V

Differential Input Voltage . . . . . ±30 V
DC Input Voltage* . . . . . ±15 V
Output Short-Circuit Duration . . . . . Indefinite
Device Dissipation:
- Up to 70°C (CA741C, CA748C) . . . . . 500 mW
- Up to 75°C (CA741, CA748) . . . . . 500 mW
- Up to 30°C (CA747) . . . . . 800 mW
- Up to 25°C (CA747C) . . . . . 800 mW
- Up to 30°C (CA1558) . . . . . 680 mW
- Up to 25°C (CA1458) . . . . . 680 mW

For Temperatures Indicated Above . . . . . Derate linearly 6.67 mW/°C
Voltage between Offset Null and V^- (CA741C, CA741, CA747CE) . . . . . ±0.5 V
Ambient Temperature Range:
- Operating – CA741, CA747E, CA748, CA1558 . . . . . −55 to +125 °C
- CA741C, CA747C, CA748C, CA1458 . . . . . 0 to +70 °C†
- Storage . . . . . −65 to +150 °C

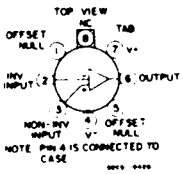
Lead Temperature (During Soldering):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . . 265 °C

* If Supply Voltage is less than ± 15 volts, the Absolute Maximum Input Voltage is equal to the Supply Voltage.

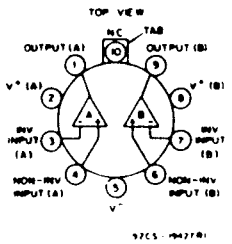
▲ Voltage values apply for each of the dual operational amplifiers.

† All types in any package style can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to +70°C.

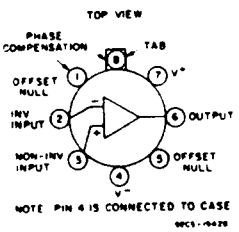
CA741, CA747, CA748, CA1458, CA1558, LM741, LM748, LM1458, LM1558



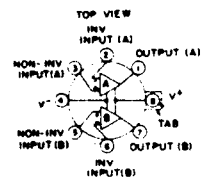
1a.–CA741CS,CA741CT,CA741S, & CA741T with internal phase compensation



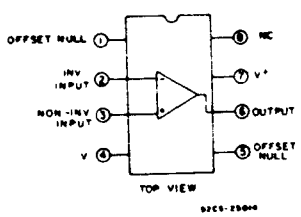
1b.–CA747CT and CA747T with internal phase compensation



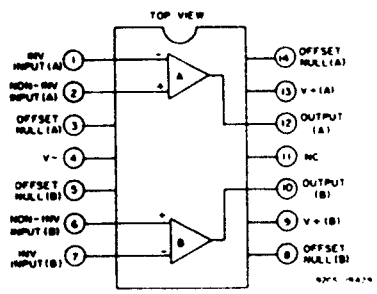
1c.–CA748CS, CA748CT,CA748S, and CA748T with external phase compensation.



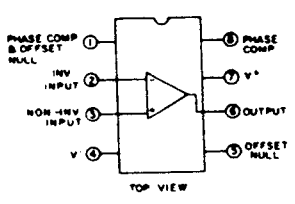
1d.–CA1458S,CA1458T,CA1558S, and CA1558T and internal phase compensation.



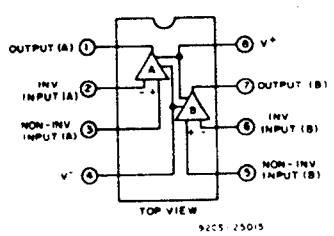
1e.–CA741C and CA741E with internal phase compensation.



1f.–CA747CE and CA747E with internal phase compensation.



1g.–CA748CE and CA748E with external phase compensation.



1h.–CA1458E and CA1558E with internal phase compensation.

Fig. 1 – Functional diagrams

CA741, CA747, CA748, CA1458, CA1558, LM741, LM748, LM1458, LM1558

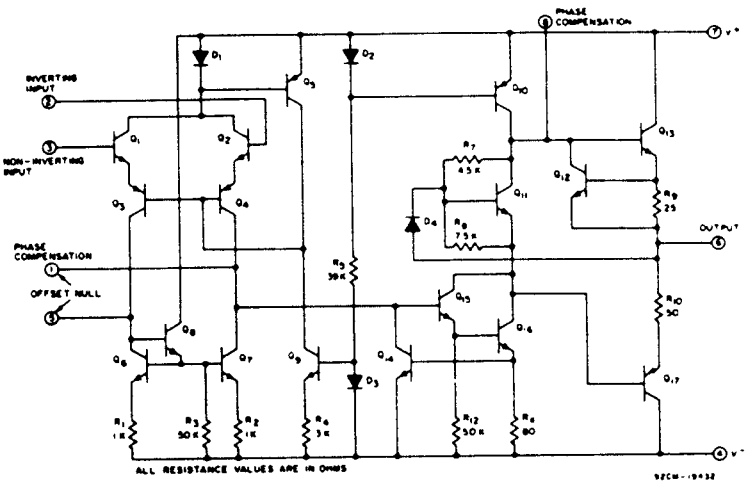


Fig. 2—Schematic diagram of operational amplifier with external phase compensation for CA748C and CA748.

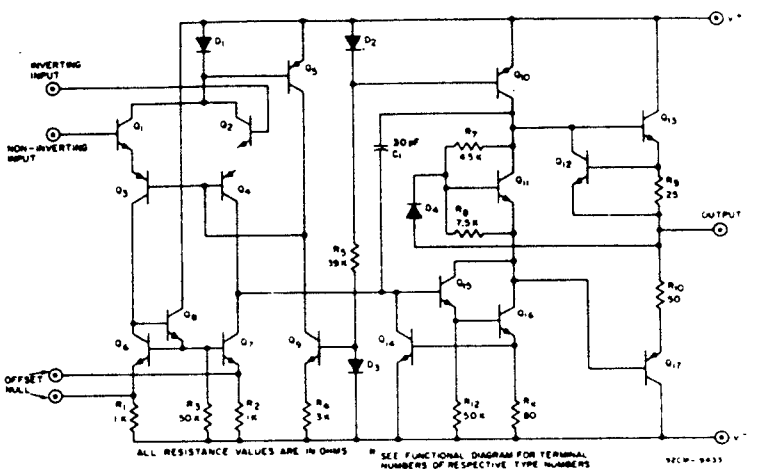


Fig. 3—Schematic diagram of operational amplifiers with internal phase compensation for CA741C, CA741, and for each amplifier of the CA747C, CA747, CA1458, and CA1558.

CA741, CA747, CA748, CA1458, CA1558, LM741, LM748, LM1458, LM1558

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

CHARACTERISTIC	TEST CONDITIONS $V\pm$ = ±15 V *	TYP. VALUES ALL TYPES	UNITS
Input Capacitance, C_I		1.4	pF
Offset Voltage Adjustment Range		±15	mV
Output Resistance, R_O		75	Ω
Output Short-Circuit Current		25	mA
Transient Response: Rise Time, t_r	Unity gain, V_I = 20 mV, R_L = 2 kΩ, $C_L \leq$ 100 pF	0.3	μs
Transient Response: Overshoot		5	%
Slew Rate, SR: Closed-loop	$R_L \geq$ 2 kΩ	0.5	V/μs
Slew Rate, SR: Open-loop▲		40	V/μs

▲ Open-loop slew rate applies only for types CA748C and CA748.

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS Supply Voltage, V^+ = 15 V, V^- = −15 V	Ambient Temperature, T_A	LIMITS CA741C, CA747C*, CA748C, CA1458* Min.	Typ.	Max.	UNITS
Input Offset Voltage, V_{IO}	$R_S \leq$ 10 kΩ	25 °C	–	2	6	mV
		0 to 70 °C	–	–	7.5	
Input Offset Current, I_{IO}		25 °C	–	20	200	nA
		0 to 70 °C	–	–	300	
Input Bias Current, I_{IB}		25 °C	–	80	500	nA
		0 to 70 °C	–	–	800	
Input Resistance, R_I			0.3	2	–	MΩ
Open-Loop Differential Voltage Gain, A_{OL}	$R_L \geq$ 2 kΩ, V_O = ±10 V	25 °C	20,000	200,000	–	
		0 to 70 °C	15,000	–	–	
Common-Mode Input Voltage Range, V_{ICR}		25 °C	±12	±13	–	V
Common-Mode Rejection Ratio, CMRR	$R_S \leq$ 10 kΩ	25 °C	70	90	–	dB
Supply-Voltage Rejection Ratio, PSRR	$R_S \leq$ 10 kΩ	25 °C	–	30	150	μV/V
Output Voltage Swing, V_{OPP}	$R_L \geq$ 10 kΩ	25 °C	±12	±14	–	V
	$R_L \geq$ 2 kΩ	25 °C	±10	±13	–	
		0 to 70 °C	±10	±13	–	
Supply Current, $I^{\pm}$		25 °C	–	1.7	2.8	mA
Device Dissipation, P_D		25 °C	–	50	85	mW

* Values apply for each section of the dual amplifiers.

CA741, CA747, CA748, CA1458, CA1558, LM741, LM748, LM1458, LM1558

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS Supply Voltage, $V^+ = 15$ V, $V^- = -15$ V	Ambient Temperature, T_A	LIMITS CA741 CA747* CA748 CA1558* Min.	Typ.	Max.	UNITS
Input Offset Voltage, V_{IO}	$R_S = \leq 10\,k\Omega$	25 °C	–	1	5	mV
		−55 to +125 °C	–	1	6	
Input Offset Current, I_{IO}		25 °C	–	20	200	nA
		−55 °C	–	85	500	
		+125 °C	–	7	200	
Input Bias Current, I_{IB}		25 °C	–	80	500	nA
		−55 °C	–	300	1500	
		+125 °C	–	30	500	
Input Resistance, R_I			0.3	2	–	MΩ
Open-Loop Differential Voltage Gain, A_{OL}	$R_L \geq 2\,k\Omega$ $V_O = \pm 10$ V	25 °C	50,000	200,000	–	
		−55 to +125 °C	25,000	–	–	
Common-Mode Input Voltage Range, V_{ICR}		−55 to +125 °C	±12	±13	–	V
Common-Mode Rejection Ratio, CMRR	$R_S \leq 10\,k\Omega$	−55 to +125 °C	70	90	–	dB
Supply Voltage Rejection Ratio, PSRR	$R_S \leq 10\,k\Omega$	−55 to +125 °C	–	30	150	μV/V
Output Voltage Swing, V_{OPP}	$R_L \geq 10\,k\Omega$	−55 to +125 °C	±12	±14	–	V
	$R_L \geq 2\,k\Omega$	−55 to +125 °C	±10	±13	–	
Supply Current, $I^{\pm}$		25 °C	–	1.7	2.8	mA
		−55 °C	–	2	3.3	
		+125 °C	–	1.5	2.5	
Device Dissipation, P_D		25 °C	–	50	85	mW
		−55 °C	–	60	100	
		+125 °C	–	45	75	

* Values apply for each section of the dual amplifiers.

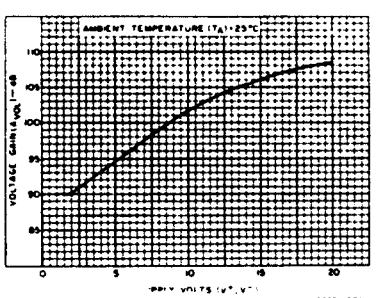


Fig.4—Open-loop voltage gain vs. supply voltage for all types except CA748 and CA748C.

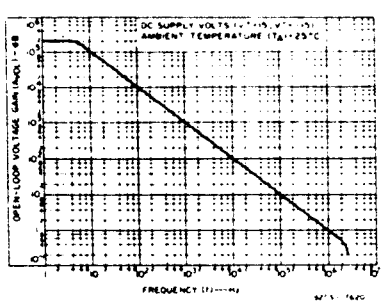


Fig.5—Open-loop voltage gain vs. frequency for all types except CA748 and CA748C.

CA741, CA747, CA748, CA1458, CA1558, LM741, LM748, LM1458, LM1558

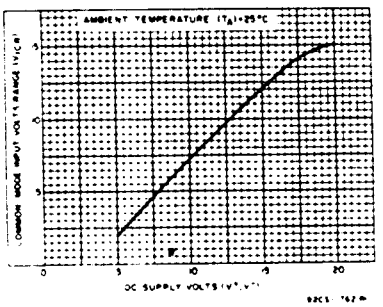


Fig.6–Common-mode input voltage range vs. supply voltage for all types.

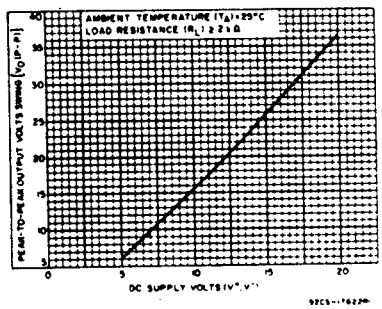


Fig.7–Peak-to-peak output voltage vs. supply voltage for all types except CA748 and CA748C

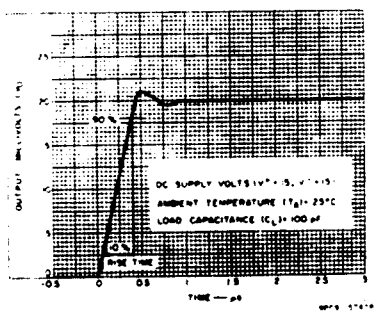


Fig.8–Output voltage vs. transient response time for CA741C and CA741.

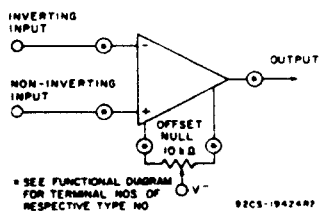


Fig.9–Voltage offset null circuit for CA741C, CA741, CA747CE, and CA747E.

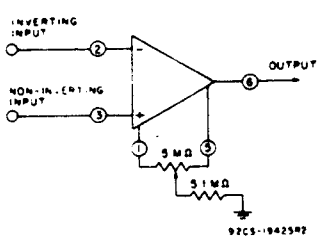


Fig.10–Voltage-offset null circuit for CA748C and CA748.

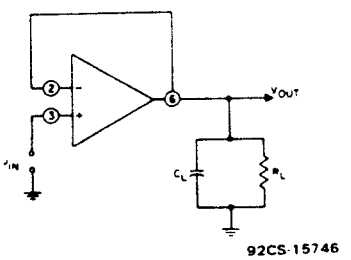


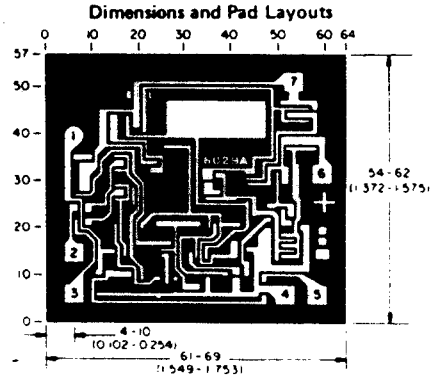
Fig.11–Transient response test circuit for all types.

CA741, CA747, CA748, CA1458, CA1558, LM741, LM748, LM1458, LM1558

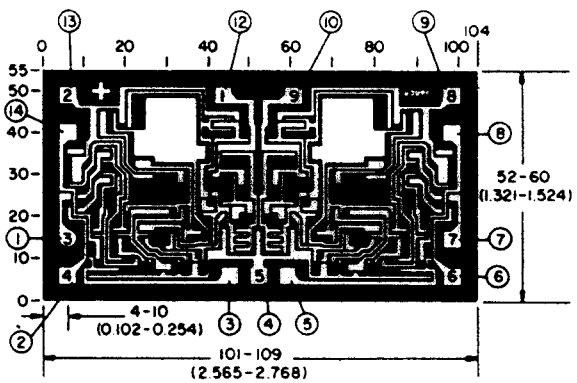
CHIP PHOTOS

Dimensions and Pad Layouts

CA741CH

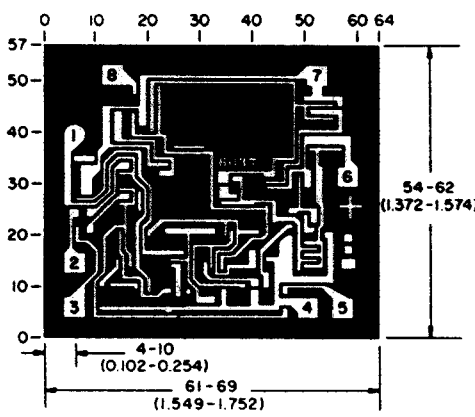


CA747CH



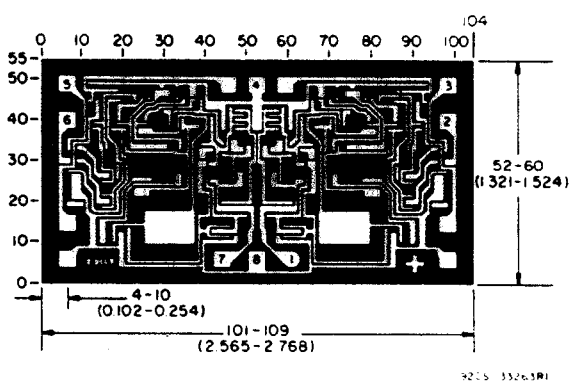
NOTE: NOS. IN PADS ARE FOR 10-LEAD TO-5
NOS. OUTSIDE OF CHIP ARE FOR 14-LEAD DIP

92CM-33260



92CS-3326

CA748CH



CA1458H

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).