DEPARTMENT OF
ELECTRONICS AND COMMUNICATION ENGINEERING

KUMARAGURU COLLEGE OF TECHNOLOGY

COIMBATORE - 641 006

CERTIFICATE

This is to Certify that the Report Entitled

MICRO CONTROLLER BASED TELEPHONE EXCHANGE

HAS BEEN SUBMITTED BY

Mr. / Miss. ______________________

in partial fulfilment for the award of the Degree of Bachelor of Engineering in Electronics and Communication Engineering Branch of the Bharathiar University, Coimbatore - 641 046 during the academic year 1993 - 94

GUIDE 30/3/94 | HEAD OF THE DEPT

Certified that the candidate was Examined by us in the project work viva-voce Examination held on ________ and the University Register Number was ________

Internal Examiner | External Examiner

PRECITRON
7/72, VALLIAMMAL STREET
RAMANATHAPURAM
COIMBATORE-641 045.

TNGST No. 227186 } Dt. 18-02-92
CST No. 626074 }

I.A.C. No. 2 | 01 | 14

Phone (Off) 21 5859
(Res) 21 2425

26/03/94

The following Electronics and Communication Engineering Branch students of Kumaraguru College of Technology have completed their project work titled **"Microcontroller Based Telephone Exchange"** in our factory.

1. Ms. Ansu Cherian
2. Ms. T.Manonmani
3. Ms. D.Suganthi
4. Mr. R.Ramesu

Yours truly,
for PRECITRON

(S.LAKSHMANAN)
Technical Director.

DEDICATED TO

OUR BELOVED PARENTS

ACKNOWLEDGEMENT

ACKNOWLEDGEMENT

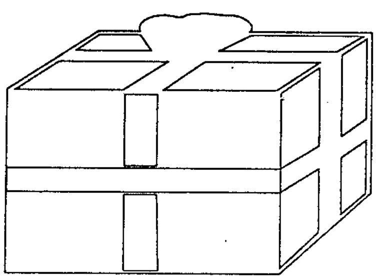
We are extremely grateful to our Principal **Dr. S. SUBRAMANIAN, MSc (Engg.), Ph.d,** for his unflinching support during the course of the project.

We are highly indepted to **PROF. K.PALANISWAMI, ME, MIEEE, MIE, MISTE, MCSI, FIETE,** Professor and Head of the Department of ELECTRONICS AND COMMUNICATION ENGINEERING for his valuable advice and timely guidance.

We are extremely thankful to our guide **Miss. H.MANGALAM, ME, MISTE,** for the moral support and the immense help she provided for the completion of this project.

Words are not enough to express our gratitude to **Mr. S.LAKSHMANAN, ME, PRECITRON** for his valuable suggestions and his timely advices during the execution of this project. We also like to extend our special thanks to him for having provided all the facilities.

Last but not the least we thank all the faculty members and our friends for their help and support.



CONTENTS

CONTENTS

SYNOPSIS

SYNOPSIS

The telephone exchange presented in this project allows upto 8 pulse telephone sets to be connected. It has options for connecting calls to or from external telephone line. This unit is controlled by 8052 based BASIC computer.

Since our telephone exchange is controlled by a BASIC interpreter, it is relatively easy to add or change certain features simply by extending or changing the control program. 8052 based computer is used because it can be programmed in BASIC, a computer language which is familiar to many. In the present application, application program is from an onboard EPROM, which has been stored after checking.

Our project comprises of some advanced features which are not present in other private exchanges. The circuit is completely designed, fabricated, and tested.

INTRODUCTION

CHAPTER ONE

INTRODUCTION

The world is witnessing an extraordinary upsurges in the development of information technology. The sweep and the range of these mini and maxi technological upsurges are both wide and far reaching in their implications generating not only new products and processes but also new global players in what has now come to be called infotelecom industry. With accelerating synthesis of telecommunication informatics and electronic media, the resulting infotelecom industry is leading the process of a new information revolution which virtually puts the world on palm.

The Indian urban areas have seen significant changes in telecommunication services in the last few years. Yet, this is only a glimpse of what is to come. On the one hand, there are definite plans to extend telecom services to our rural areas and on the otherhand the services in the cities are to become more sophisticated with the introduction of ISDN, Data networks, Mobile telephones and paging services. Yet these changes are too miniscule compared to what is happening in telecommunication around the world, with the increasing globalisation of markets, many of these new technology are likely to make an impact in our country.

Our project is a step in the direction of preparing for the future. Telecommunication to-day encompasses a large variety of speculities which requires skill and expertise. Our project **MICROCONTROLLER BASED TELEPHONE EXCHANGE** provides a glimpse of few:

SPECIAL FEATURES:

* This exchange has 8 intercomes with facility to recieve external calls with 3 DOT lines.

* **CALL INVITATION:** When the called party is not available another free intercom can invite the call.

* **TRANSFER OF CALLS:** The called party can direct the call to a free intercom.

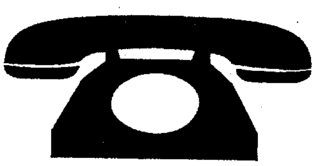
* **CALL MONITORING:** Here a record is maintained about the number of calls and the number dialled.

* **FEATURE TONE:** This tone indicates to the already engaged subscriber, that an external call is on line.

* **MUSIC ON HOLD :** This tone indicates to subscriber that he is under another subscriber's attention. This may take place during call transfer or when the subscriber waits for some information.

* **RINGING TONE:** Two seperate ringing tones are available to differentiate between the incoming external call and a call from a mutual intercom.

* **CALL CONFERENCING:** 3 party conferencing has been implemented where 3 persons can communicate at the same time. This can be between 3 intercoms or an external DOT and 2 intercoms.



T.E.L.E.P.H.O.N.E.
THE BASICS

CHAPTER TWO

TELEPHONE THE BASICS

Before discussing the operation of the telephone exchange, it is useful to look at the basic operation of the telephone system. In the following discussion, it is assumed that pulse-dialling telephone sets are used.

Figure(2-1) shows the general layout of a telephone connection. When the receiver is on the hook, the bell inside the telephone set is connected to the telephone line. When tho receiver is lifted, the voice circuit of the set is connected to the telephone network, and a direct current flows through the microphone. The telephone extensions connected to the network receive their supply voltage from the local telephone exchange. All are connected to two lines and operate free from the earth line. The use of balanced line is a simple, yet effective, way, to eliminate noise in the network. Since any noise introduced on the network is, in principle equally strong and of equal phase on the "a" and "b" lines, it is effectively inaudible.

2.1 OUTGOING CALLS :

The timing diagrams in figure(2-2) shows the switching sequences during a telephone call. Again, only the "a" and "b" lines are involved in establishing the call. Normally a voltage of 50 to 60V exists between these lines. The exchange detects that a receiver is lifted when the line voltage drops to about 10V and a microphone current of about 20mA is established. Next, the exchange sends dial tone to the calling extension to indicate that a number may be dialled. In the pulse dialling system, the current loop is interrupted repetitively. The pulse rate usually lies between 9 and 11 pulses per second. The break period is called 'pulse', and the 'connect' period is called 'pause'. The pulse length is generally defined as 61.5% + or - 3% of the period. Assuming that the period is 100ms the current is interrupted for periods of 58.5 to 64.5ms. The pause allowed between successive numbers is 0.7 to 1s.

The local exchange starts to call up the wanted extension with the aid of a ringing signal after the complete number has been received form the calling extension. When the call is answered, the exchange starts to put a cost count signal on the "a" and "b" lines. This signal is a sine-wave burst with an amplitude of about 50V. Since it is the same on the "a" and "b" line, it is inaudible to the calling as well as to the called party. A cost counter, however, is connected asymmetrically to the network to allow it to detect the pulses. When either party rings off, the voltage between the "a" and "b" line reverts to the 'standby' level of 5 to 50V.

2.2 INCOMING CALLS :

An incoming call is detected by the ringing signal produced by the telephone set. The exchange calls up the extension by putting an alternating voltage of about 50Vpp on the "a" and "b" line. The fact that the signals on "a" and "b" are in anti-phase allows the telephone to detect the ring signal and actuate a sounder device. The ringing continues until the called party lifts the receiver to answer the call. If the call is not answered after the predetermined number of rings, the connection is broken. When the called party lifts the receiver before the last ring, the previously mentioned direct current flow is established, enabling the exchange to detect that the call is answered. The telephone conversation can then begin.

2.3 DIGITISATION OF TELEPHONE NETWORKS

ARCHITECTURE:

The telephone network of today is a multilevel star network as shown in figure(2-3). At the lowest level of the network, there are local exchanges to which a number of telephone subscribers are connected using wire local loops. Any call within the local area is completed by the local exchange which circuitswitches the calling subscriber to the called subscriber . The local-exchanges are usually connected to each other directly or via a tandom exchange using two or four wire trunks. Local exchanges are also connected to trunk exchange for intercity traffic. When a subscriber calls someone outside his local exchange area the local exchange connects the subscriber to the called local exchange either using direct trunks or via tandom exchange or trunk exchange. Finally the called subscriber switches the line to the called subscriber thus completing the voice circuit. The process requires transmission of signalling data between subscriber, local exchange and also between two local exchanges or between local exchange and tandom exchange .

DIGITISATION:

The process of digitisation of telephone networks in India is well underway, with digitisation of trunks and introduction of digital switches.

Till around 70's the complete telephone network (local loop, exchange and trunks) was analog. With the development of techniques for voice digitisation and due to the advantages provided by digital transmission, this started changing. The first impact was on the trunks. With optical fibers emerging on the scene, the pace of digitisation increases and data rates moved higher. Improvement in quality of voice services, especially for long distance communication was the obvious result. Till about late 70's, all exchanges were analog. At the trunk interface, the analog voice was converted into digital stream and multiplexed before transmission. The incoming digitised voice on trunk line was converted to analog before being switched.

By late 80's, task of digitisation was almost complete. Local loop is digitised to provide an end to end digital network. Local loop carries voice, on-hook, off-hook information and number dialled from subscriber to exchange. From exchange to subscriber it carries voice, dial tone, and most importantly battery feed for telephone. All this transmission takes place on the same two wires. Let us look at two way digital transmission on pairs of wires. There are two basic techniques for transmission of digital data in both directions over the local loop.

1. Ping Pong technique.
2. Echo cancellation.

1.PING PONG TECHNIQUE:

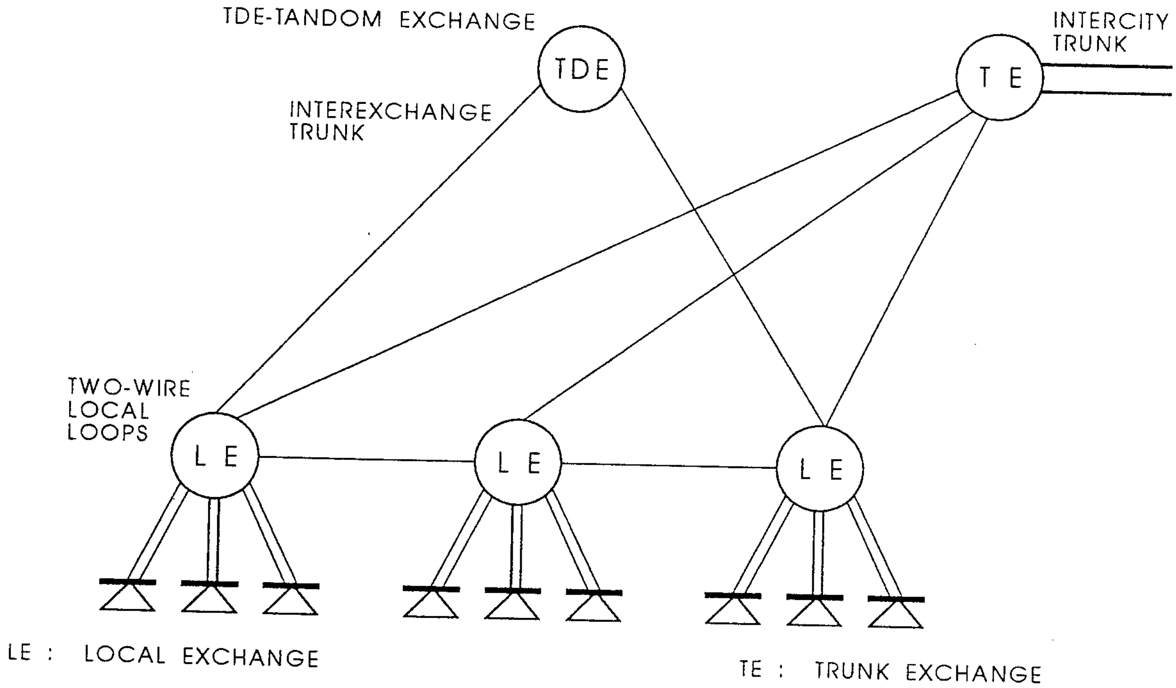
It uses a time duplex high speed data transmission link, where data is transmitted in small burst alternatively in each direction. Since it takes a finite amount of time for the data to propagate on the link, guard times are required between each burst of data as shown in figure(2-4).

It also requires a clock on two sides to be synchronous. VLSI chips existing today implements this technique.

2.ECHO CANCELLATION TECHNIQUE:

It essentially converts the combined signal on two wires to separate l's on four wires, by cancelling out the transmitted component of the signal which is transmitting on two wires referred to in figure(2-5).

The voice, tones, on-hook, off-hook information, the number dialled and the ring commands can be easily digitised and multiplexed into a two way data stream to be carried on the above described digital loops.



ARCHITECTURE OF THE TELEPHONE NETWORK

Fig : 2.3 Architecture of the Telephone Network

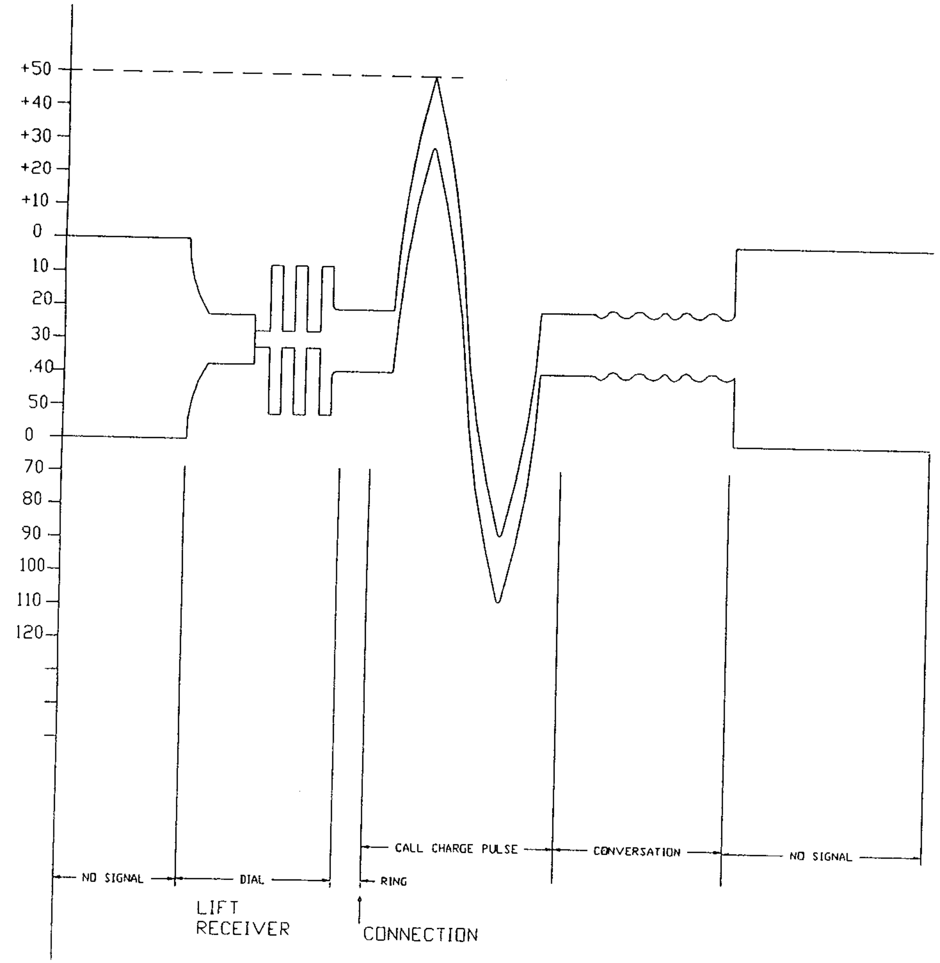


FIG 2.1

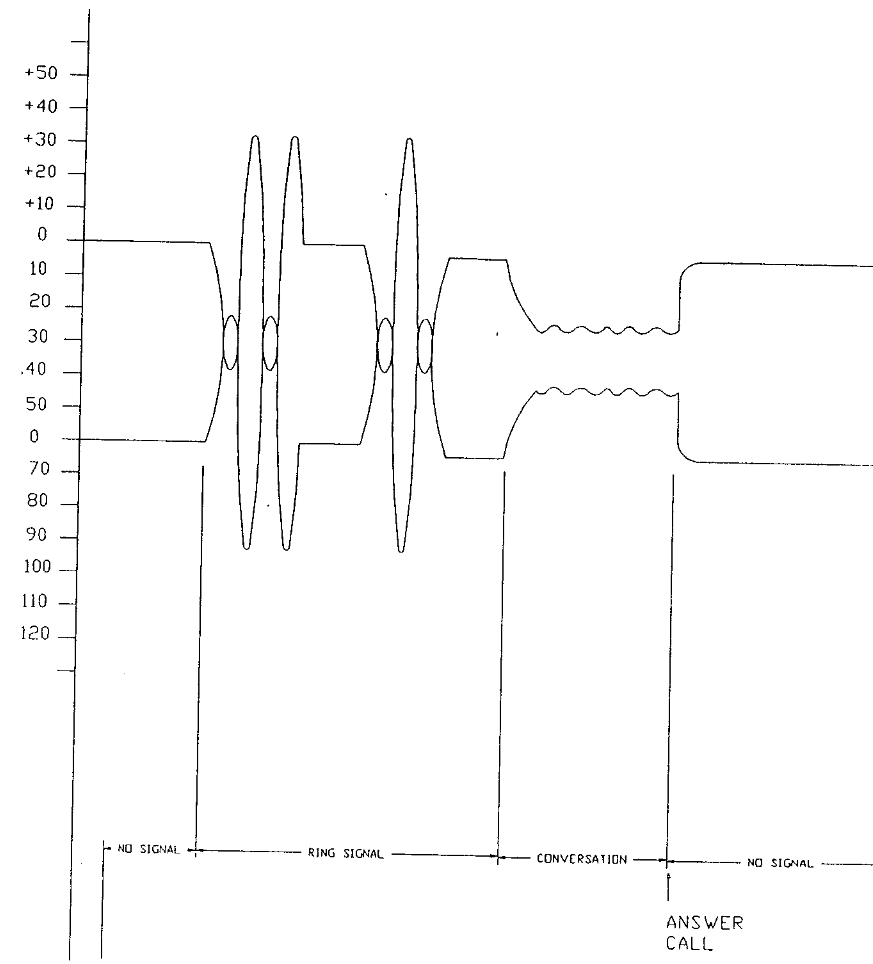


FIG 2.2

WAVEFORM SEQUENCE ON THE TELEPHONE LINES

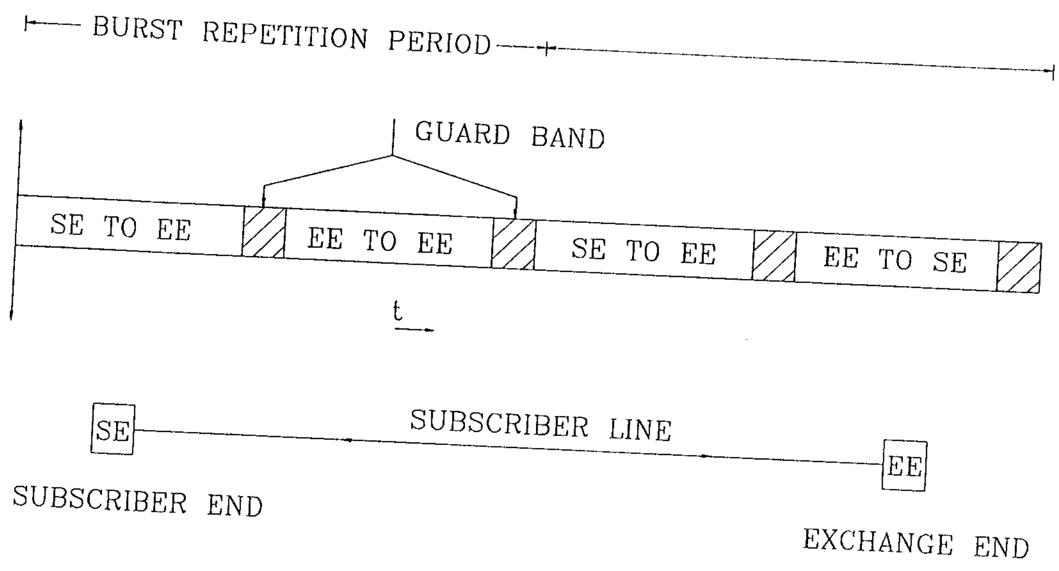


Fig: 2-4 The ping pong technique

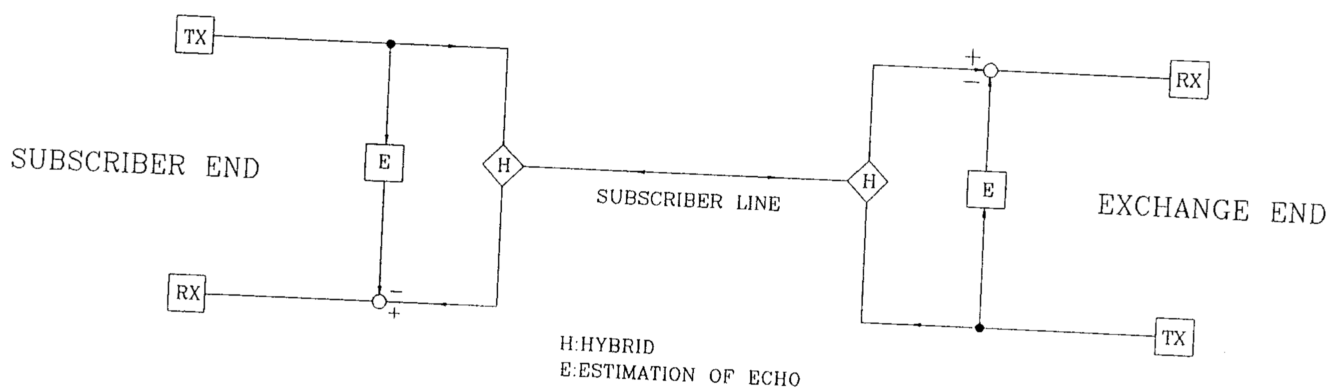


Fig: 2-5 Echo cancellation

WORKING PRINCIPLE

CHAPTER THREE

WORKING PRINCIPLE

External subscriber on dialling the number gets access to the DOT line as per availability of free lines. When a particular DOT line is selected, initially when the handset is in on hook condition the first rectifier converts the ac signal to dc signal and thus enables the optocoupler to conduct. The conduction of the optocoupler indicates the presence of an external call. The information is given to the processor through the input PORT C. The address regarding the information is sent to the switching matrix. A software routine keeps track of status of the intercoms. It keeps record of which line is free and which is engaged in conversation. Both off-hook and on-hook status of the line are sensed as follows:

1. OFF HOOK STATUS SENSING :

Subscriber off hook status is signalled by completion of the dc loop resulting in a dc current of 20 to 35 mA. The sensing is done by an optocoupler arrangement which can unambiguously detect the lowest expected loop current as well as the highest. It should not detect any dc leakage current due to poor line insulation of the cable itself. The sensor is designed to detect if current exceeds 10 mA.

2. ON-HOOK STATUS SENSING :

When the subscriber telephone is in on-hook there is only an ac path through the loop. There is no dc path. These on-hook status is interpreted when there is near zero dc current in the loop. The information given in the switching matrix dertermines which intercom is called and the software determines the status of the intercom.

3. RING FEED :

When the software senses that the desired intercom is free that is in on-hook a ringing signal is to be given to that particular intercom. To activate the ringer in the subscriber telephone set, a 25 Hz, 75 Vrms signal is fed onto the loop. This level is obviously too high for the audio circuits to handle. So the transmitter and receiver pair is switched by means of "ring feed" relay onto the another circuit that feeds this signal. The line circuit-card which provides direct interface between the exchange and subsciber is provided with the 25 Hz 75 Vrms signal. When an instruction is given to ring a given subscriber bell, the card merely activates the changeover relay in switching matrix that connects the Tip and Ring wires to this signal. Thus a ringing tone is heard by the intercom.

4. RING TRIP:

When the handset of the intercom is lifted that is in off-hook condition, the exchange should stop feeding the ringer signal. This event is called ring trip. Here again a dc loop needs to be sensed to detect off-hook status.

With the subscriber in the on-hook condition, the ac ringer waveform causes an ac current. The dc voltage is blocked by a capacitor. As soon as the subsriber goes off-hook a shifting of dc current level takes place.

The current sensor now senses an ON for a longer period in the 25 Hz waveform and this is detected by a counter and interpreted as subsciber off-hook. The current detecting element is an optocoupler and the duration measuring component is a counter which is reset to zero whenever the current goes positive (due to ac current level shifting when -48 V is superimposed). The counter reaches its terminal count only if the positive current duration has been lengthened and the occurence of this terminal count is the indication of off-hook condition having occured.

Now voice path has to be established between the external subscriber and intercom. The switching system used requires that the two way voice signal present at the Tip and Ring wires should be seperated into two unidirectional speech signals. The isolated incoming signal is then digitised and switched to the required destination subscribers circuitry, where it is again converted to an analog signal, before being sent onto the Tip and Ring wire. The analog to digital conversion is done according to PCM. The coded outputs are multiplexed to form a PCM format as per CCITT standard. This goes for switching for every channel, one CODEC is used. The LCC card interfaces 8 intercoms and each intercom subscribers voice signal is sampled 8000 times a second by the CODEC and encoded into 8 bit PCM. The bit rate is 2.048 MHz.

The carbon microphone in the subscribers handset requires a dc current of about 25-40 mA to operate at its optimal level. Furthermore the line circuit card is meant for an environment that uses dc signalling. That is information such as hook status and called subscriber member are detected solely from the dc condition of the subscriber loop.

When a subscriber telephone is on-hook there is an ac path through the loop, but not dc. Lifting the handset causes a switch to close across the capacitor in the subscriber handset establishing a dc loop. Furthermore when the subscriber is off-hook and dials a number, it results in the dc path opening and closing a number of times in accordance with the digit dialled.

On-hook status is interpreted when there is a near zero dc current in the loop and off-hook when 10-35 mA flows in the loop. The dialling of a digit by a subscriber results in a make break sequence of the loop current, which is detected and the information conveyed to the decoder to get the actual digit it represents.

The dc current used for this signalling is provided at the LCC. To introduce this current into the loop without disturbing the balance of subscriber loop, the transformer primary is wound in two halves with a break in middle through which the direct current is introduced. A capacitor across this break creates an ac path through the transformer primary. The extension is connected to the DOT when there is power failure thus providing power for the operation of the exchange.

HARDWARE DESCRIPTION

CHAPTER FOUR

HARDWARE DESCRIPTION

4.1 8031 MICRO PROCESSOR:

The term 8031 is often used generally to refer to 8051 and 8751. The 8031 is a ROMless 8051 and fetches all instructions from external memory. The architecture, memory organisation of addressing modes of 8031 are dealt in detail Chapter (5).

4.2 MEMORY COMPONENTS:

The memory components used for the project are listed below:

(a) EPROM (27C256)

(b) EEPROM (28C65)

(c) RAM (6264)

(a) EPROM (Erasable Programmable Read Only Memory):

The information stored in this memory is permanent and can be erased by exposure to UV-light. The chip can be reprogrammed again and again. The EPROM used for the project is 27C256 (UV-erasable PROMs) with a memory capacity of 32K byte. It is a CHMOS production. Some of the important feutures of thus chip are as follows:

* Micro controller and Micro processor compatible.
* High perfomance speeds (170ns maximum access time).
* Noise immunity features.
* New quick-pulse programming algorithm.

PROGRAMMING THE CHIP:

Initially, and after each erasure all bits of the EPROM are in the "1" state. Data is introduced by selectivity programming "0's" into the desired bit location. Although only "0's" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to "1" is by UV-light erasure. The device is in the programming mode when the Vpp is raised to its programming voltage and (ALE / CE) is pulsed to TTL low and OE=V1H. The data to be programmed is applied as 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

We opted this chip for the project because 87C256 was designed to reduce the hardware interface requirements when incorporated in processor systems with multiplexed address-data buses. This chip is used in the project for storing the control programs (main running program) and can also be reprogrammed according to the requirement. For more details refer to figure(4-1).

(b) EEPROM (ELECRICALLY ERASABLE PROMS):

This is fabricated with reliable n-channel floating gate MOS technology. The main features of this chip are:

* 250 ns access time.
* Fast write cycle time.
* High Reliability.
* Data Polling (A system software support scheme used to indicate the early completion of write cycle).
* Compatible with industry, standard RAM, ROM, EPROM.

DEVICE OPERATION:

1. READ:

The read operations are initiated by both OE and CE and the termimated by either CE or OE returning to high. The data bus will be in high impedence state when either of OE or CE is high.

2.WRITE:

The operations are initiated when both CE and WE are low and OE is high. This chip supports both a CE and WE controlled write cycle. That is the address is latched by falling edge of either WE or CE, whichever occurs last. Similarly, the data is latched internally by the rising edge of either CE or WE whichever occurs first. A byte write operation, once initiated, will automatically continue to completion.

EEPROM is similar to EPROM except that information can be altered using electrical signals rather than erasing all the information. For example preprogrammed priority conditions can be altered according to our needs. Also the exchange is programmed in such a way that only particular intercoms can receive or make STD/ISD calls. These type of programs are stored in EEPROM, since the user can make in it. The chip used for our project is 28C65. For more details refer to figure(4-2).

C.RAM: (RANDOM ACCESS MEMORY):

The features of RAM are:

* Fast access time.
* Low power stand-by.
* Capability of battery back-up operation.
* Completely static memory.
* No clock or strobe required.
* Equal access and cycle time.
* Common data input and output.

The memory capacity of RAM chip is 8K and the memory is volatile. The information regarding the incoming calls, outgoing calls, the data, timing can be stored in RAM. The RAM chip used is 6264. For more details refer to figure(4-3).

4.3 RECTIFIER UNIT:

The Bridge rectifier is the circuit most frequently used for full wave rectification. During the positive half cycle of the input voltage to the bridge rectifier, diodes D1 and D4 conducts as shown in figure(4-4). At the same time diodes D2 and D3 are revere biased. Figure(4-5) shows diodes D2 and D3 forward biased during the negative half cycle of the input while D1 and D4 are reverse biased. The result in that both positive and negative half cycles of the input are passed to the load resistance R . Also the negative half cycles are inverted, so that the output is a series of positive half cycles of alternating unit.

In the on-hook condition of a subscriber, there is an a.c path through the loop, but not d.c. Information such as hook status and the called subscriber number are detected solely from the d.c condition of the subscriber loop. So, a rectifier is used to convert a.c to d.c.

4.4 OPTO COUPLER:

The Optocoupler or the optical isolator is generally used in a digital interface. An optical coupler can be thought of as a circuit, which comprises of a LED and a light sensitive device such as a photo transistor as shown in the figure(4-6). The general operation of an optocoupler in a microprocessor interfacing is explained as follows:

Now, figure(4-7) shows how a single digital line of system-A may be connected to system-B using optocoupler. The driving source is the system-A and the digital signals from system-A is to be sent to system-B which is done by the optocoupler.

With the digital signal from system -A at logical-0, the LED of the optical isolator will not be forward biased. This means that the LED is OFF. The photo transistor has no base current as a result of light source being OFF. Thus the photo transistor is OFF also. With the transistor OFF, the collector is pulled up to the +5V of system-B. The collector voltage of the photo-transistor is the digital signal input to system-B. Hence when the driving signal from system-A is at logical-0, the input to the system-B is inverted to logical-1.

If digital signal from system-A is logical-1 the LED is turned ON which requires 10 to 16mA of current. To accomplish this an external pull up resistor is added. Now the photo transistor is forced into saturation, the collector voltage becomes equal to the emitter voltage. Since the emitter of the output transistor is connected directly to the system-B ground, the output voltage will be zero.

The dc signal from rectifier is fed to optocoupler-1 which enables it to conduct. The number dialled (that is ringing pulse) is sensed by this optocoupler arrangement and then sent to the processor. The optocoupler 2-9 present in intercom circuitry senses the status of its line that is during the OFF time of the ringer waveform, this optocoupler checks whether the hand set is in off-hook or on-hook condition.

4.5 INPUT AND OUTPUT PORTS:

The input and output ports used are 74245 and 74573 respectively. Here, two input ports and one output port is used. The input port is used to read the information and send it to the processor. The input port 245 reads information such as status of the intercoms, status of the DOT line, and whether the incoming call is DOT or intercom. The output port 573 is used to output data such as the dialled number and latch the line status information to the relay coils. This port is also used to display the status of the lines using LED's.

The 74245 used is an octal bus transreceiver. It is designed for synchronous two way communication between data buses and the control function implementation minimizes external timing requirement. The devices allows transmission from the A bus to B bus or viceversa. Depending on the logical level at the direction control input. The enable input G can be used to disable the device so that the bus is effectively isolated.

The 74573 used is an output latch which features tri-state outputs designed specifically for driving highly capacitive or relatively low impedance loads. Since they are particularly suitable for implementing buffer registers, output ports, bidirectional bus drivers and working registers, this IC is used. For more details refer to figure(4-8).

4.6 SWITCHING MATRIX:

This project uses IC CD22100 as a switching matrix. It is a cross point switch with control memory. The operation of the switching matrix is dealt in detail in chapter (6).

4.7 DECODER FOR CHIP SELECT:

The decoder is a logical circuit, which identifies each combination of the signals present at its input. For example, the input to the decoder has 2 binary lines which can assume 4 combination of input lines with each combination identified by the output lines 0 - 3. This process is called decoding. In addition, some decoders have active low output lines as well as enable lines.

The chip used is 74138. It is 3 to 8 line decoder and is designed specifically for high speed memory decoders and data transmission systems. It also incorporates 3 enable inputs to simplify cascading. The conditions at the binary select input and 3 enable inputs select 1 out of 3 input lines. Two active low and one active high enable input reduces the need for external gates or invertors, when expanding. Chip selection is carried out by 2 such decoders. For more details refer to figure(4-9).

4.8 LINE CIRCUIT:

The Line Circuit Card(LCC) is the direct interface between the exchange and the subscriber. The card has 8 pairs of subscriber intercom telephone wires. The function of each of these circuits is to detect the status of the corresponding subscriber telephone handset and to enable the voice of the subscriber to reach a point within the exchange from where it is sent to the called party and vice-versa. The Line Circuit Card communicates with the terminal interface network (TIC/SN) card for voice data transfer.

The analog portion of the Line Circuit-Card has been divided on the basis of its function into constituent sections.

(a) Analog line interface with A/D(and D/A) conversion.

(b) Subscriber Line Status Sensing.

(a) ANALOG LINE INTERFACE WITH A/D(and D/A) CONVERSION:

There are essentially 2 types of information flowing over the analog lines - the voice and the signalling.. The analog circuitry has to cater the both. The switching system used is the C-DOT. Digital Switching Systems(DSS) requires that the two way voice signal present at the Tip and Ring wire should be separated into two unidirectional speech signals. The isolated incoming signal is then digitized and passed on to the TIC/SN card, where it is switched in time and passed back to the required destination subscribers circuitry, where it is again connected to an analog signal, before being sent out onto the Tip and Ring wires.

The Tip and Ring wires, leading in from the subscribers loop, goes to primary of the hybrid transformer, making the voice signal available at the secondary of the transformer. The secondary of the transformer is connected to a converter which provides two unidirectional speech paths. The signal is given to CODEC which encodes it into 8 bit PCM.

For the voice signals in the direction the signals going to the subscriber communicate to the LCC from TIC/SN card in PCM form, and are converted to analog at subscribers CODEC. This passes to the secondary of the transformer and to the subscriber via Tip and Ring wires.

4.9 POWER BACK UP:

The power back up unit enable the DOT line being connected to the extension directly in case of a power failure.

During the normal conditions that when there is no power failure the voice path is established between an external call and a subscriber. Under this condition the power backup relay is in (3,4), (5,6) with extension relay in (2,3), (7,6) positions.

In case of power failure the power backup relay switches to (2,3), (6,7) position thus enabling the direct connection of DOT to the extension. Hence now the DOT line is connected to the extension through the power back up unit in the case of power failure. The relay position switchings are controlled by means of a software routine.

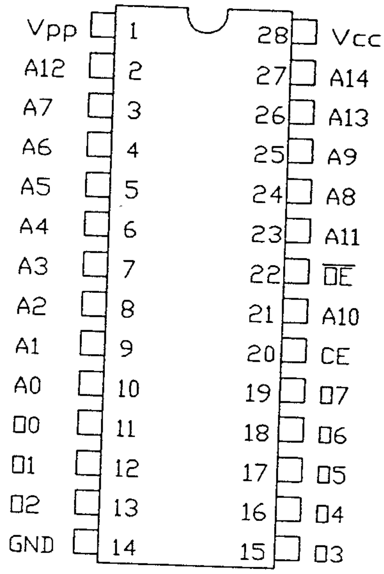


Fig: 4.1 Pin Configuration of IC 27256

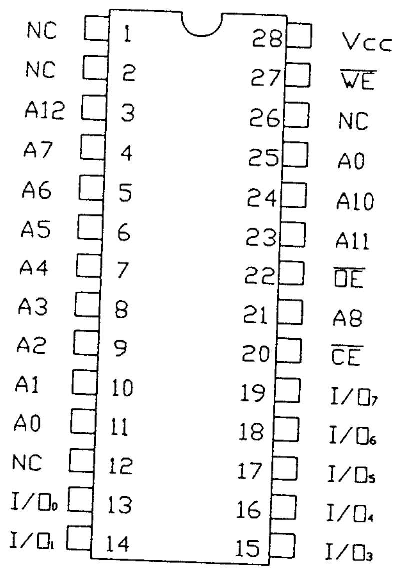


Fig: 4.2 Pin Configuration Of IC 2865

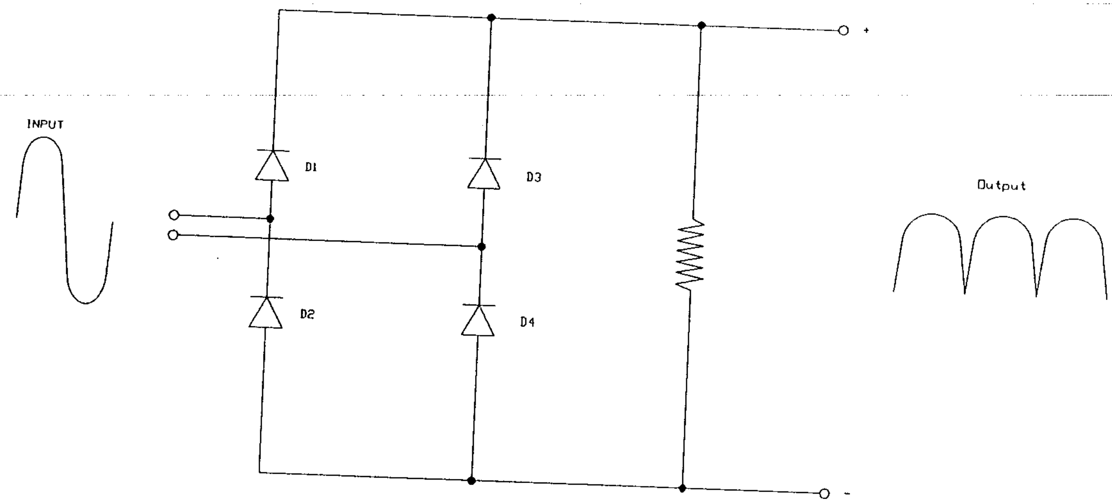


Fig 4.4

(a) Bridge Rectifier Showing Input and output

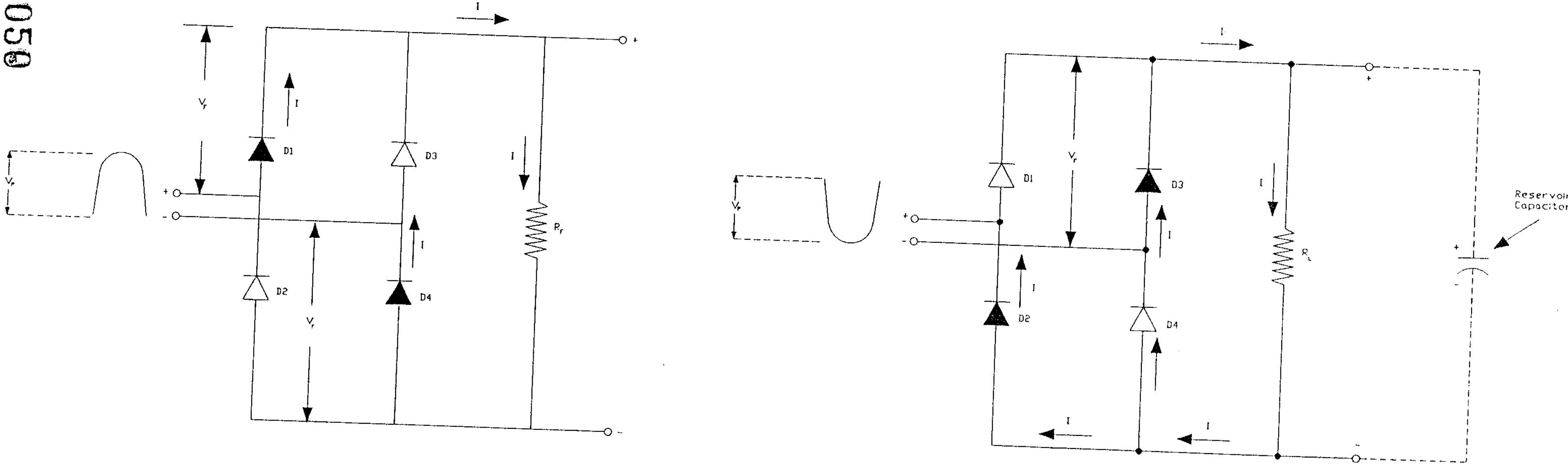
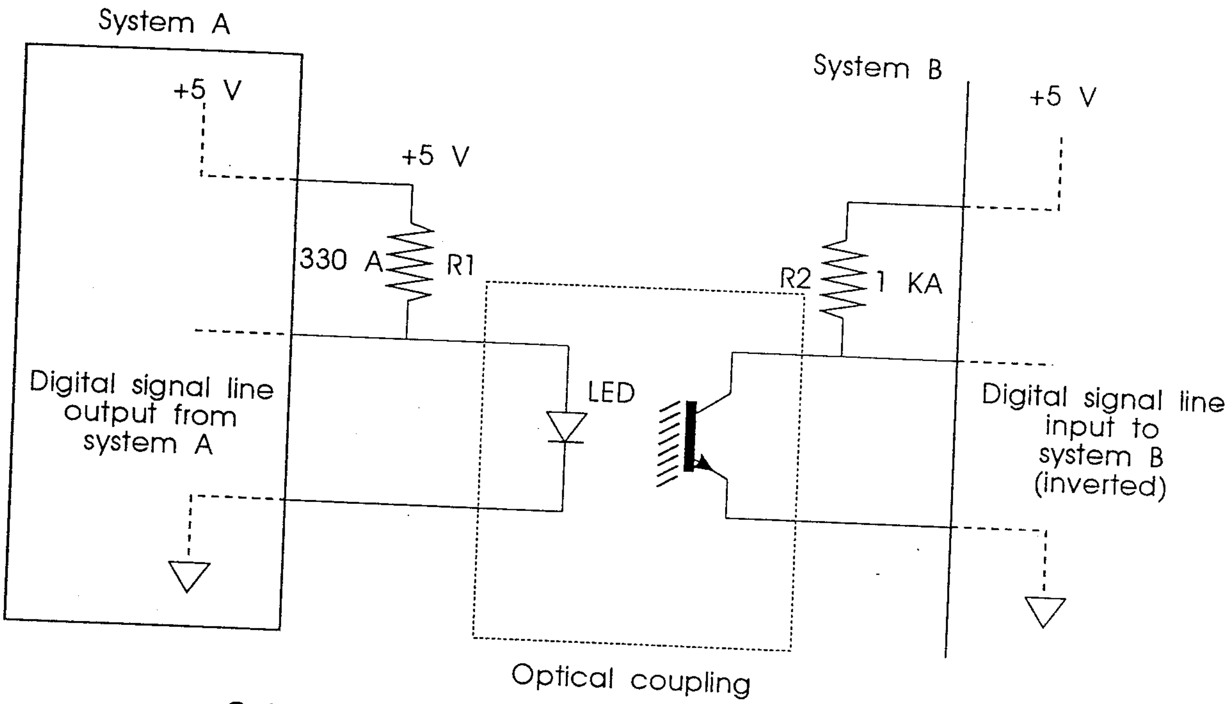


Fig 4.5

Full-Wave bridge rectifier circuit. D1 and D4 conduct during the positive half-cycle of the input. D2 and D3 conduct during the negative half-cycle



Schematic diagram showing how a single digital line may be connected using optical isolators

Fig : 4.6 Schematic diagram showing how a single digital line may be connected using optical isolators

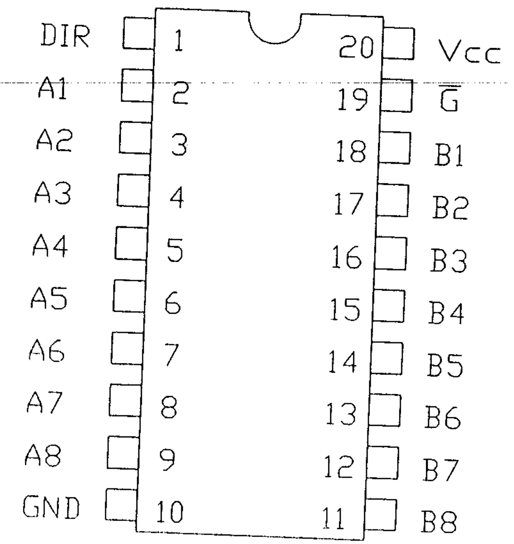


Fig: 4.8(a) Pin Configuration Of IC 74245

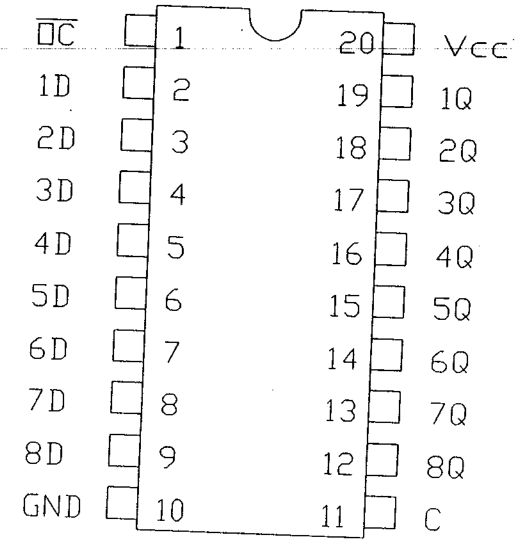


Fig: 4.8(b) Pin configuration Of IC 74573

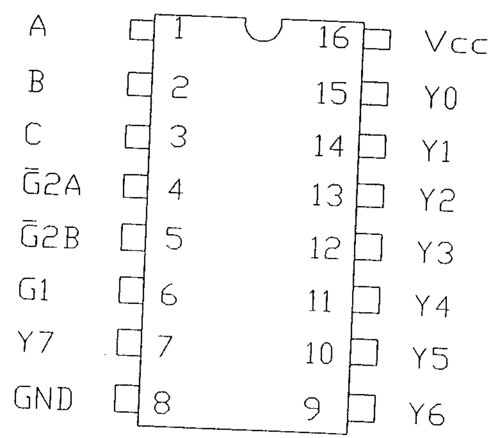


Fig: 4.9 Pin configu

ARCHITECTURE - 8031

CHAPTER FIVE

8031 ARCHITECTURE

The major features of the 8031 are :

* 8-bit CPU.
* on-chip oscillator.
* 4K bytes of ROM.
* 128 bytes of RAM.
* 21 Special Function Registers.
* 32 I/O lines.
* 64K address space for external Program Memory.
* two 16-bit timer/counters.
* a five-source interrupt structure with two priority levels.
* a full duplex serial port.
* bit addressability for Boolean processing.

The term "8051" is often used generally to refer to the 8051, the 8031, and the 8751. The 8031 is a ROMless 8051; it fetches all instructions from external memory. The 8751 is an 8051 with EPROM instead of ROM.

A block diagram of the 8051 is shown in figure(5-1).

5.1 MEMORY ORGANIZATION:

The 8051 maintains separate address spaces for program memory and data memory. The program memory can be up to 64K bytes long, of which the lowest 4K bytes are in the on-chip ROM.

The data memory consists of 128 bytes of on-chip RAM, plus 21 special function registers, in addition to which the device is capable of accessing up to 64K bytes of external data memory.

The program memory uses 16-bit addresses. The external data memory can use either 8-bit or 16-bit addresses. The internal data memory uses 8-bit addresses, which provide a 256-location address space. The lower 128 addresses access the on-chip RAM. The special function registers occupy various locations in the upper 128 bytes of the same address space.

The lowest 32 bytes in the internal RAM are divided into 4 banks of registers, each bank consisting of 8 bytes. Any one of these banks can be selected to be the "working registers" of the CPU, and can be accessed by a 3-bit address in the same byte as the opcode of an instruction.

The next higher 16 bytes of the internal RAM have individually addressable bits. These are provided for use as software flags or for one-bit (Boolean) processing. This bit-addressing capability is an important feature of the 8051. In addition to the 128 individually addressable bits in RAM, eleven of the special function registers also have individually addressable bits.

5.2 SPECIAL FUNCTION REGISTERS:

The Special Function segisters are as follows:

ACCUMULATOR

ACC is the Accumulator. The mnemonics for accumulator-specific instructions refer to the accumulator simply as A, but the register itself is named ACC.

B REGISTER

The B register is used during multiply and divide operations. For other instructions it can be treated as another scratch register.

STACK POINTER

The Stack Pointer is 8 bits wide. The stack can reside anywhere in the 128 bytes of on-chip RAM. When the 8051 is reset, the stack pointer is initialized to 07H. When executing a PUSH or a CALL, the stack pointer is incremented before data is stored, so the stack would begin at location 08H.

DATA POINTER

The data pointer is a 16 bit register consisting of a high byte (DPH) and a low byte (DPL). Its intended function is to hold a 16-bit address.

PORTS 0 THROUGH 3:

These four parallel ports provide the 32 I/O lines. Each port consists of a latch (special function registers P0 through P3), an output driver, and an input buffer.

The output drivers of ports 0 and 2 and the input buffers of port 0 are used to access the external memory. In this application, port 0 outputs the low byte of the external memory address, time-multiplexed with the byte being written or read. Port 2, meanwhile, outputs the high byte of the external memory address.

SERIAL DATA BUFFER

The serial buffer is actually two separate registers. When data is moved to SBUF, it goes to the transmit buffer where it is held for serial transmission. When data is moved from SBUF, it comes from the receive buffer.

During serial reception the incoming bits are clocked into a separate shift register. When reception of a frame is complete, and if various other conditions are satisfied, 8 received data bits are transferred from the shift register to the receive buffer. The shift register is then ready to commence reception of a second frame, while the frame already received awaits servicing.

CONTROLS AND STATUS REGISTERS

Special function registers IP, IE, TMOD, TCON, SCON, and PCON contain control and status bits for the interrupt system, the timers, and the serial port. They will be fully described in the remaining sections of this chapter.

5.3 OSCILLATOR AND CLOCK CIRCUIT:

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which is intended for use as a crystal oscilator, in the Pierce configuration, in the frequency range of 1.2MHz to 12MHz. XTAL2 is also the input to the internal clock generator.

The clock generator divides the oscillator frequency by 2, and provides a two-phase clock signal to the chip. The Phase 1 signal is active during the first half of each clock period, and the Phase 2 signal is active during the second half of each clock period.

5.3 CPU TIMING

A machine cycle consists of 6 states. Each state is divided into a phase 1 half, during which the phase 1 clock is active, and a phase 2 half, during which the phase 2 clock is active. Normally, arithmetic and logical operations take place during phase 1 and internal register-to-register transfers take place during phase 2.

5.5 PORT OPERATION:

All four ports in the 8051 are bi-directional. Ports 1, 2, and 3 have internal pull-ups. Port 0 has open-drain outputs. Figure(5-2) shows a functional diagram of a typical bit in each of the four ports.

Each I/O line can be independently used as an input or an output. For a line to be used as an input, the port latch must contain a 1, which turns off the output driver FET. Then, for Ports 1, 2, and 3, the pin is pulled high by the internal pull-up, but can be pulled low by an external source. For Port 0, a 1 in the port latch causes the output pin to float. All the port latches in the 8051 have 1's written to them by the reset function. If a 0 is subseqently written to a port latch, it can be reconfigured as an input if desired by writing a 1 to it.

Because Ports 1, 2, and 3 are pulled high when configured as inputs, they are sometimes called "quasi-bidirectional" ports. As inputs they can be driven in a normal manner by any TTL or MOS circuit. Because they do have the internal pull-ups, however, they can also be driven by open-collector or open-drain outputs without the need for additional external pull-ups.

Port 0 differs in not having internal pull-ups. The upper FET in the P0 output driver is turned OFF except when the port is being used as an ADDR/DATA bus in access to the external memory. Consequently, P0 lines that are being used as output ports have open-drain outputs. Writeing a 1 to P0 latch results in both output FET's being turned off, so the pin floats. In that condition it can be used as a high-impedance input.

READING A PORT

Notice in figure(5-3) that there are two ways to read a port: an instruction reads either the latch or the pin. In the 8051, some instructions read the latch and some read the pin. The instructions that read the latch rather than the pin are the ones that read a value, possibly change it, and then rewrite it to the latch. These are called "read-modify-wirte" instructions.

The reason that read-modify-write instructions are directed to the latch rather than the pin is to avoid a possible misinterpretation of the voltage level at the pin. For example, a port bit might be used to drive the base of a transistor. One might write a 1 to it in order to turn the transister on. If the CPU now reads the same port bit at the pin rather than the latch, it will read the base voltage of the transistor and interpret it as a 0. Reading the latch rather than the pin will return the correct value of 1. It is to avoid this type of problem that the 8051 directs read-modify-write instructions to the port latch rather than the port pin.

WRITING TO A PORT

In the execution of an instruction that changes the value in a port latch, the new value arrives at the latch during S6P2 of the final cycle of the instruction. However, port latches are in fact sampled by their output buffers only during Phase 1 of any clock period. Consequently, the new value in the port latch won't actually appear at the output pin until the next Phase 1, which will be at S1P1 of the next machine cycle.

If the change requires a 0-to-1 transition in Port 1, 2, or 3, an additional pull-up is turned on during S1P1 and S1P2 of the cycle in which the transition occurs. This is done to increase the transition speed. The extra pull-up can source about 100 times the current that the normal pull-up can.

It should be noted that the internal pull-ups are FET's, not linear resistors. The pull-up arrangement is shown in figure(5-4). The fixed part of the pull-up is a depletion-mode transistor with the gate wired to the source. If the port pin is shorted to ground, this transistor will allow about 0.25mA to exit the pin. In parallel with the fixed pull-up is an enchancement-mode transistor which is activated during S1 whenever the port bit does a 0-to-1 transition. During this interval, if the port pins shorted to ground, this extra transistor will allow an additional 30mA to exit the pin.

5.6 ACCESSING EXTERNAL MEMORY

Accesses to external memory are of two types: accesses to external program memory and accesses to external data memory. Accesses to external program memory use signal PSEN as the read strobe. Accesses to external data memory use RD or WR to strobe the memory.

Fetches from external Program Memory always use a 16-bit address. Accesses to external data memory can use either a 16-bit address or an 8-bit address.

5.7 TIMERS:

The 8051 provides two 16-bit register, Timer 0 and Timer 1, that can be used as timers or event counters. For each timer/counter register there is a control bit in Special Function Register

TMOD that selects the timer/counter function to be "timer" or "counter."

In the "timer" function the register is incremented every machine cycle. Thus one can think of it as counting machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the "counter" function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since it takes 2 machine cycles to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency.

5.8 SERIAL INTERFACE:

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. The serial port registers are both accessed at Special Function Register SBUF. A write to SBUF loads the transmit register, and a read accesses a physically separate receive register.

5.9 SERIAL PORT DATA REGISTERS:

In all serial modes a write to SBUF loads the same 9-bit shift register. The data byte goes in to the first 8 bits, with the LSB at the output bit of the register. The write to SBUF also loads the 9th bit of the shift register with either a 1 or TB8, depending on the mode. And it initiates the transmission.

The receive registers are an input shift register which is 8 bits wide in mode 0 and 9 bits wide in the other modes, plus SBUF itself, a read-only register which is loaded by the hardware with the data byte at the same time that RI is activated. In the UART modes, the 9th bit is loaded into RB8 in SCON at the same time that the data byte is loaded into SBUF. RB8 and SBUF are not changed if SM2 causes the received data to be ignored.

5.10 INTERRUPTS:

The 8051 provides five interrupt sources, each of which can be programmed to one of two priority levels. The five interrupt sources are listed below:

Source	Description
INT0	External request from P3.2 pin(sampled at S5P2 of every machine cycle).
Timer 0	Overflow from Timer 0 activates interrupt request flag TF0.
INT 1	External request from P3.3 pin (sampled at S5P2 of every machine cycle).
Timer 1	Overflow from Timer 1 activates interrupt request flag TF1.

Serial Port Completion of transmission or reception of one signal frame activates request flag Tl (on transmission) or Rl (on reception).

5.11 8051 FAMLIY PIN DESCRIPTION:

Vss : Circuit ground potential.

VCC : Supply voltage during programming, verification and normal operation.

Port 0: Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus during accesses to external memory. It also outputs instruction bytes during program verification. Port 0 can sink eight LS TTL inputs.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. It receives the low-order address byte during program verification in the 8051 or 8751. Port 1 can sink/source three LS TTL inputs. It can drive MOS inputs without external pullups.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. It emits the high-order address byte during accesses to external memory. It also receives the high-order address bits and control signals during program verification in the 8051 or 8751. Port 2 can sink/source three LS TTL inputs. It can drive MOS inputs without external pullups.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. It also serves the functions of various special features of the MCS-51 family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INT0 (external interrupt)
P3.3	INT1 (external interrupt)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)

P3.6 WR (external Data Memory wirte strobe)

P3.7 RD (external Data Memory read strobe)

Port 3 can sink/source three LS TTL inputs. It can drive MOS inputs without external pullups.

RST/VPD: A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal pulldown permits Power-On reset using only a capacitor connected to VCC.

ALE/PROG: Address Latch Enable output for latching the low byte of the address during accesses to external memory. ALE is activated though for this purpose at a constant rate of 1/6 the oscillator frequency even when external memory is not being accessed. Consequently it can be used for external clocking or timing purposes. This pin is also the program pulse input during EPROM programming.

PSEN: Program Store Enable output is the read strobe to external Program Memory PSEN is activated twice each machine cycle during fetches from external Program Memory. PSEN is not activated during fetches from internal Program Memory.

EA/VPP: When EA is held high the CPU executes out of internal Program Memory. When EA is held low the CPU executes only out of external Program Memory. In the 8031, EA must be externally wired low. In the 8751, this pin also receives the 21V programming supply voltage (VPP) during EPROM programming.

XTAL1: Input to the inverting amplifier that forms the oscilator. Should be grounded when an external oscillator is used.

XTAL2: Output of the inverting amplifier that forms the oscillator, and input to the internal clock generator.

Receives the external oscillator signal when an external oscillator is used.

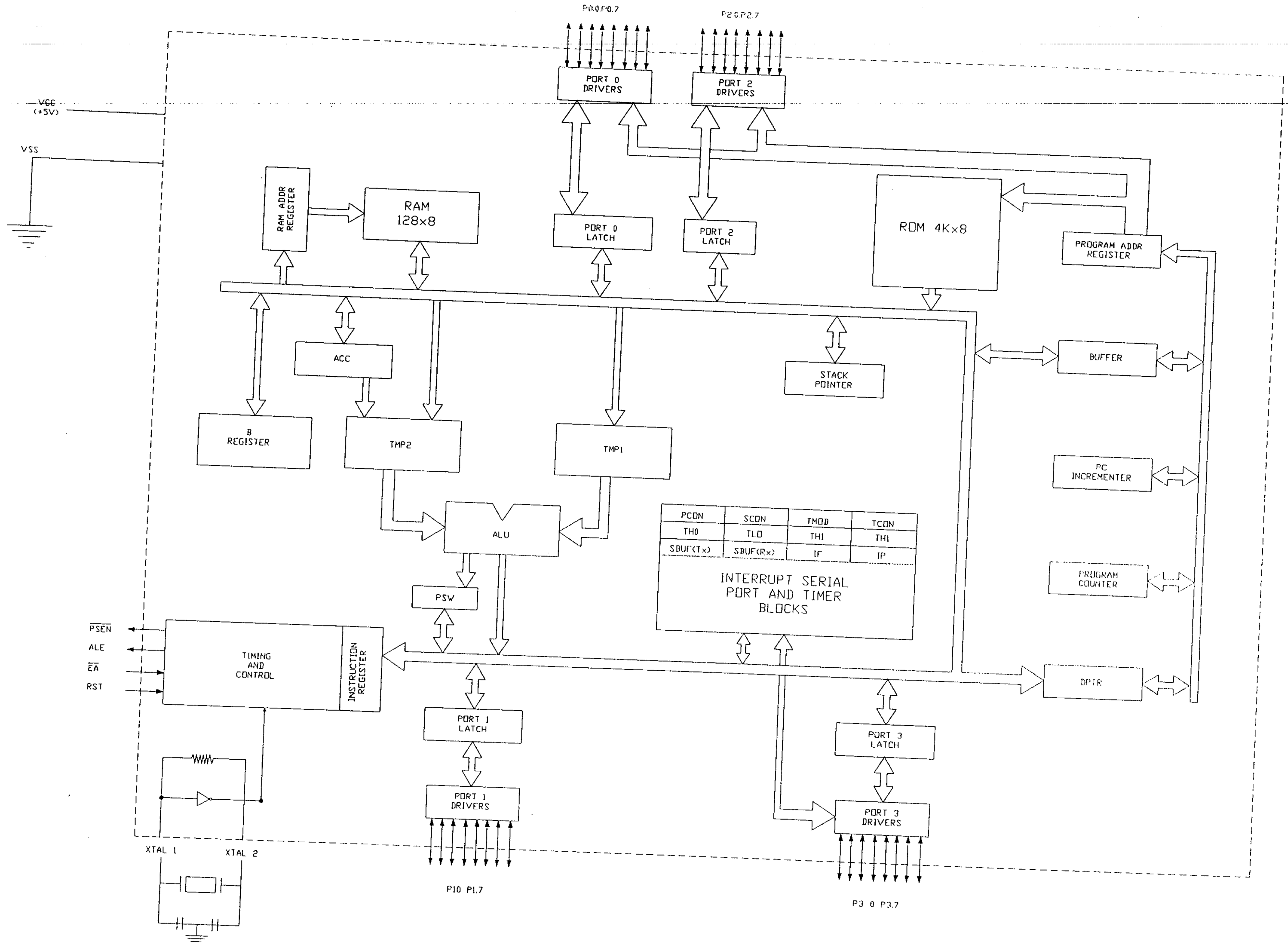


Fig 5.1
BLOCK DIAGRAM OF 8031

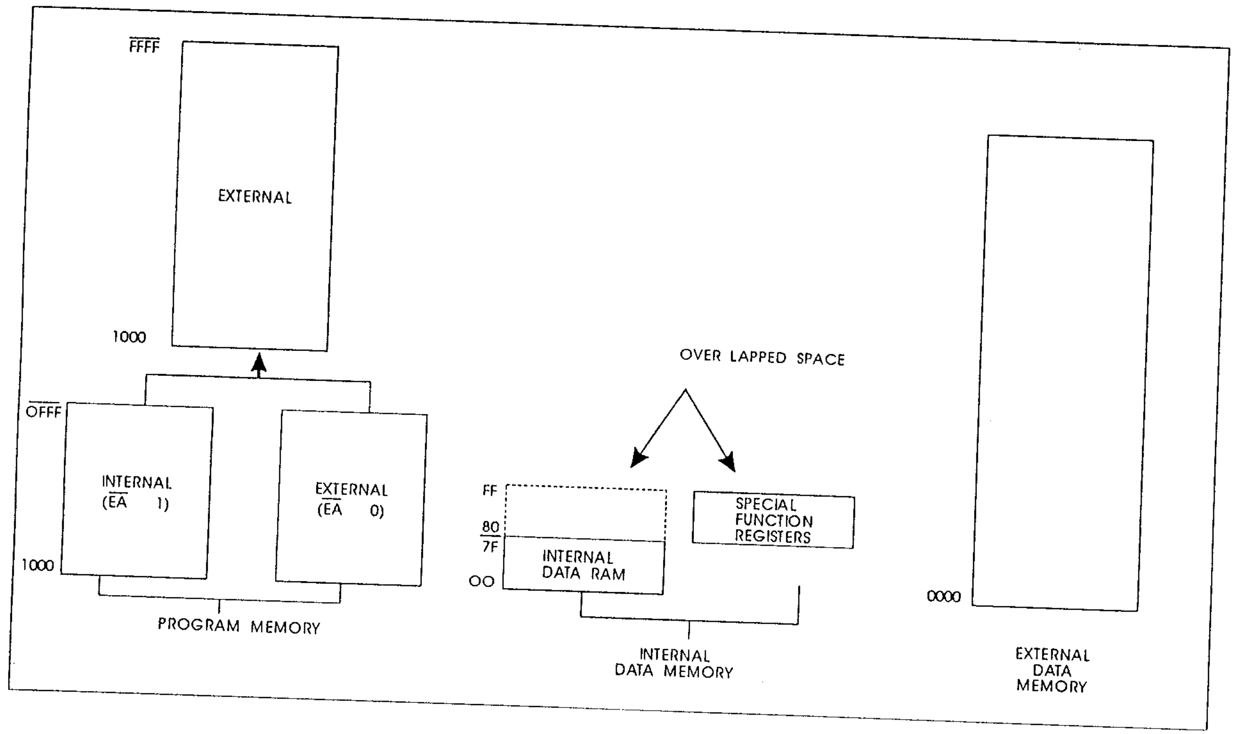


Fig : 5.2 8051 Memory Map

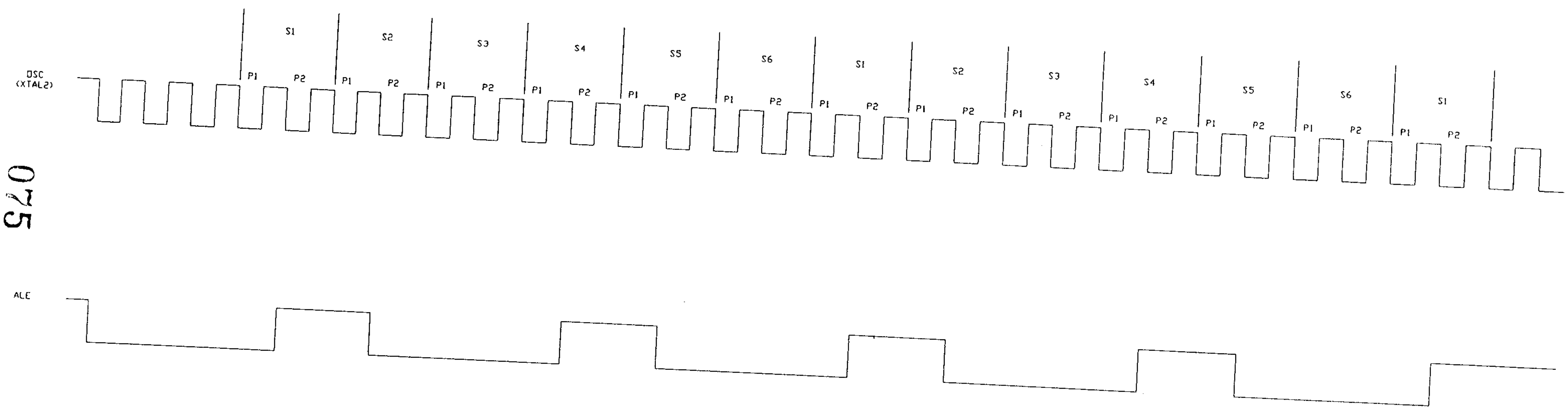


Fig 5.3
CPU Timing Diagram

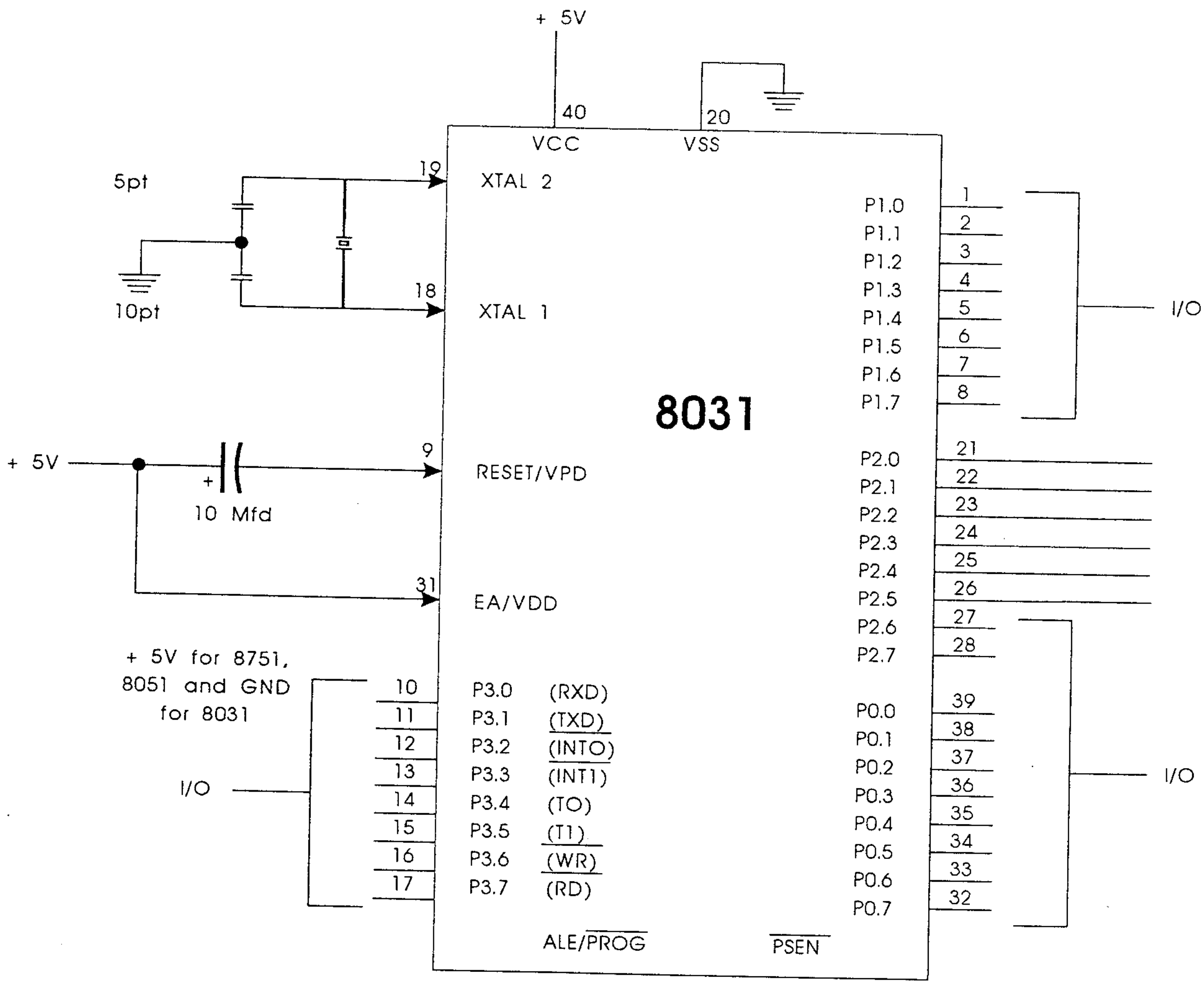


Fig 5.5 Pin Configuration of IC 8031

SWITCHING MATRIX

CHAPTER SIX

SWITCHING MATRIX

6.1 GENERAL DESCRIPTION:

The CD22100 combines a 4*4 array of cross points(transmission gates) with a 4 line to 16 line decoder and 16 latch circuits. Any one of the 16 transmission gates can be selected by applying appropriate 4 line address. The selected transmission gate can be turned ON or OFF by applying logical 1 or 0 respectively to data input and strobing the strobe input to logical 1. Any number of transmission can be ON simultaneously. For more details refer to figure(6-1).

6.2 SWITCHING MATRIX ARRANGEMENT IN THE CIRCUIT:

A single CD22100 forms a 4*4 array. For forming a 12*8 array 6 such IC's are used. The formation of 12*8 matrix is as follows. The first pair of two CD22100 IC's arranged in parallel result in a 4*8 matrix. An addition of a second such pair in series to the first pair results in a 8*8 matrix. Third such pair connected in series to the first two results in a 12*8 matrix. This forms a switching matrix with 96 cross points or transmission gates.

The lines Y0-Y7 denotes the coloumn. The 8 intercoms are connected to these coloumn lines. The lines X0-X11 forms the row. The row lines consists of 3 DOT lines, 1 MOH, 3 control lines and four tones. The four tones comprises of two ringing tones to differentiate between external and internal call, 1 feature tone, 1 busy tone or engaged tone.

6.3 OPERATION:

The 6 chips are selected by strobing the strobe input to a logical 1. Selection of cross points is done by the address bits in the line A0-A5 which comes from the microcontroller 8031. Any number of cross points can be selected according to the requirments. The various operations that are done by switching matrix, when the exchange is in the operation of implementing the following features are as follows:

(a) EXTERNAL AND AN INTERCOM COMMUNICATION:

When an external subscriber wants to establish a call in our exchange the operations that takes place in switching matrix are as follows. The address lines A0-A5 from the processor go to the switching matrix. These address lines are used in the selection of cross points. The selected DOT line which forms a row is in the enabled state. A software program monitors the intercoms and keeps record of the status of the intercoms. On receiving the address, the software program checks whether the required intercom is free or busy. When a intercom is free, contact is established between external subscriber and the intercom, otherwise engaged tone is produced.

(b) INTERCOM TO INTERCOM COMMUNICATION:

When a calling party dials the required intercom's address, the address is fed to the processor through an input port. In the processor the lower order address bytes are separated and fed to the switching matrix. This address selects the cross point. For establishing the connection between two intercoms, a control line is selected. The control line forms the row and this line is perpendicular to the two intercoms which are to be engaged in the conversation. Hence, in establishing this intercom to intercom communication two cross points are selected.

6.4 TONES:

1. RINGING TONE:

The ringing tone circuit voltage is 75V. Once the intercom is selected as explained in the previous operations, the processor supplies data to switch the relay ON and OFF. The ON and OFF period of the ringing waveform is preprogrammed. During the OFF period, the process checks whether the handset of the selected intercom is in on-hook or off-hook condition. When it is in on-hook, the ringing is continued. When it is off-hook voice path is established which is of 12V. Processor determines whether the call is external or internal and respective tone lines are selected in the switching matrix.

In the switching matrix as soon as the intercoms are selected, the corresponding ringing tones for the intercoms are enabled.

2. MUSIC ON HOLD:

When one subscriber wants another subscriber to wait, the MOH circuitry comes into action. For this, MOH line in the switching matrix has to be enabled. This happens as follows: The contacts between the subscribers are made as explained previously. The MOH line is enabled when the processor determines the waiting subscriber's address, which is fed to the switching matrix.

Thus selection of cross point is made possible. The paths established by the cross points produces MOH for the waiting subscriber.

3. ENGAGED AND FEATURE TONE:

When 2 subscribers are conversing and a third subscriber wants to communicate with an already engaged subscriber, an engaged tone is produced at the third subscriber intercom and feature tone is produced at the already engaged subscriber.

A software program monitors the intercom and finds out whether the required intercom is already engaged.

If the engaged processor enables the engaged line, the address of third party is obtained from monitoring software and is fed to switching matrix which determines the cross point. Through the established path, busy tone is sent to the third subscriber and feature tone line is enabled. The address of the engaged subscriber is got from the monitoring program and the crosspoint is related to provide the path for feature tone.

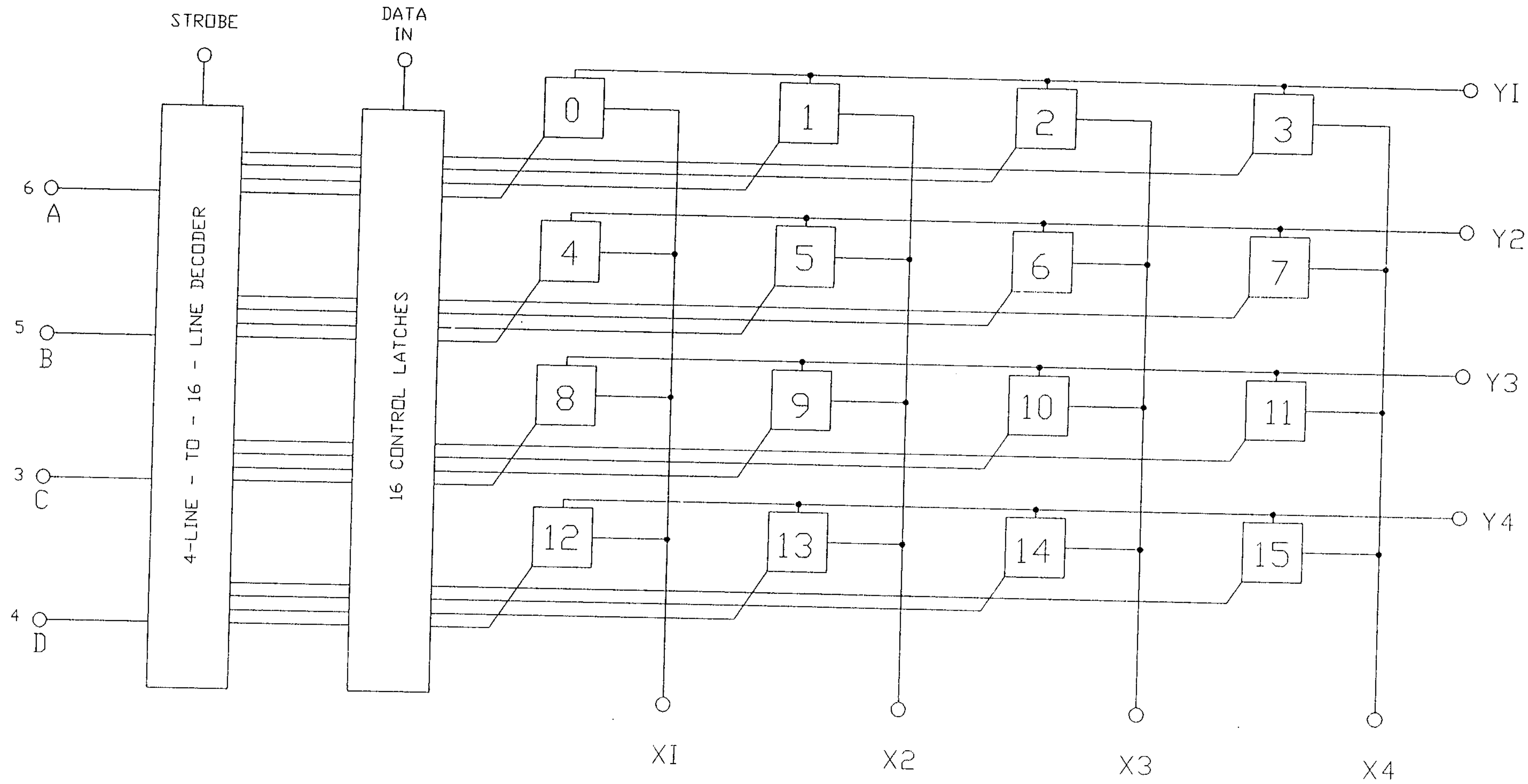


Fig 6.1 Functional Diagram of a Switching matrix

CHAPTER SEVEN

INSTRUCTION MANUAL

1. NUMBERING PLAN:

Intercom - 31-38 (8 Intercoms)

Call transfer -1

Music on hold -2

Call conferencing -5

Call invitation - 3

2. TO MAKE AN INTERCOM CALL:

(a) Lift your handset and wait for the dial tone.

(b) Dial the number of intercom you require.

3. TO MAKE A DOT LINE CALL:

(a) Lift your handset and wait for the dial tone.

(b) Dial the code number and wait for the dial tone.

(c) Dial the outside number you require.

The system selects one out of the three DOT lines for your call as follows:

* If only one line is free, the free line is selected.
* If all the lines are free, the one which was not selected for the previous call is selected.

4. TO ANSWER A CALL:

(a) Lift your handset and speak.

* The ringing cadence indicates whether the incoming call is an intercom call or a DOT line call.

5. CALL INVITATION:

(a) Lift your handset and wait for dial tone.

(b) Dial 3 and speak.

* Call pick-up is possible by dialling 3 irrespective of any station at which the ringing takes place.

6. CALL CONFERENCING:

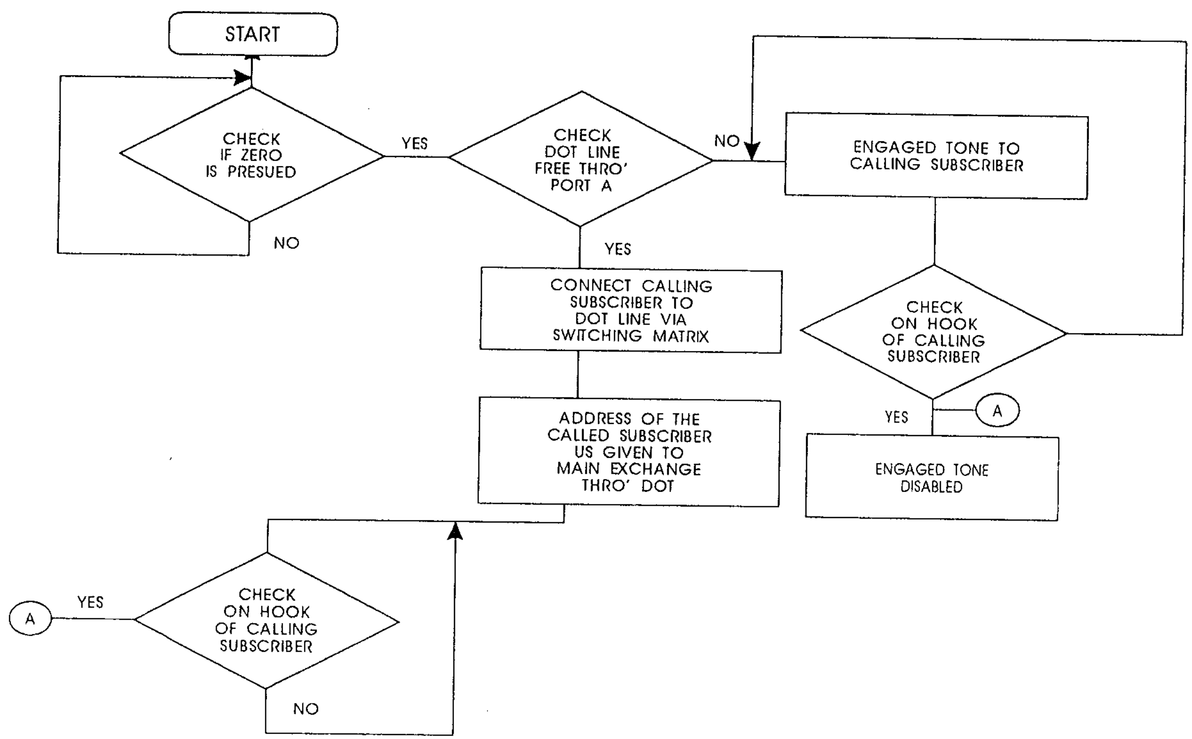
(a) Call between first two subscribers is done as explained previously.

(b) Dial 5 for call conference.

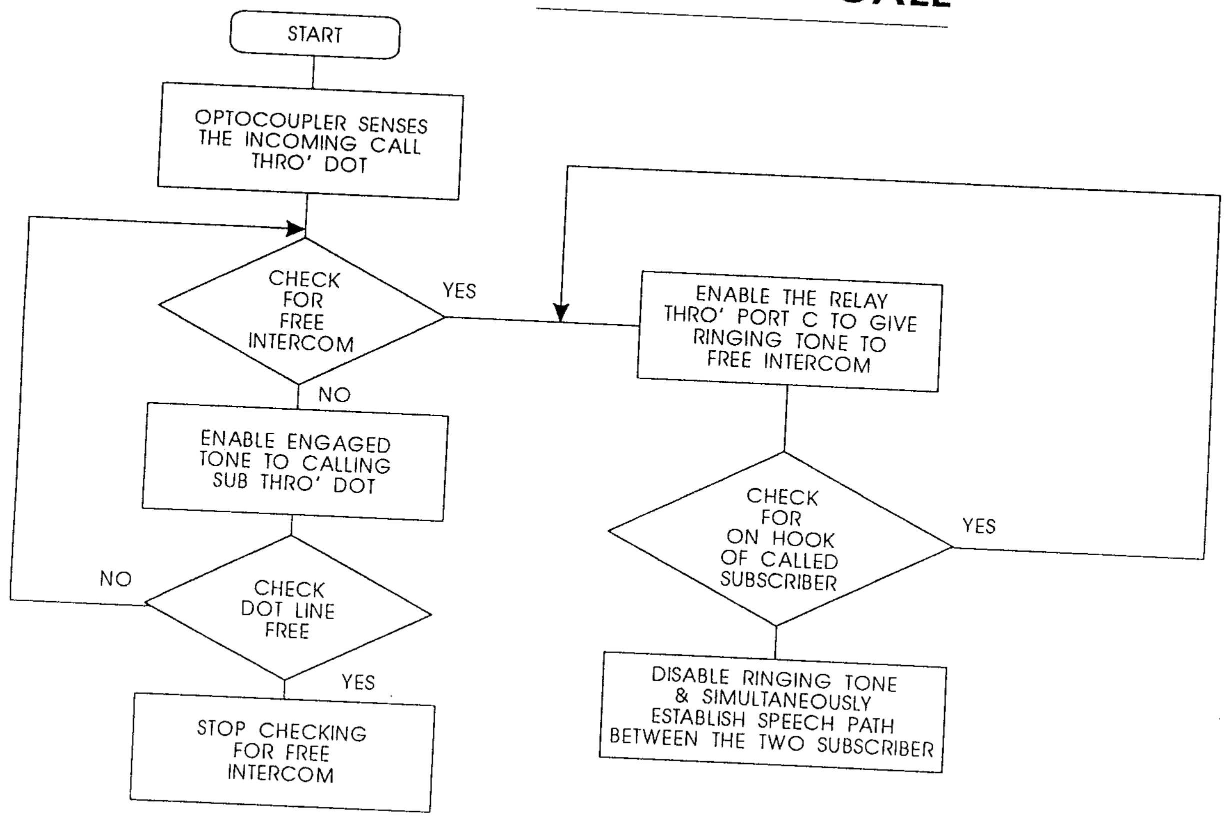
(c) Dial the number of third subscriber.

FLOW CHARTS

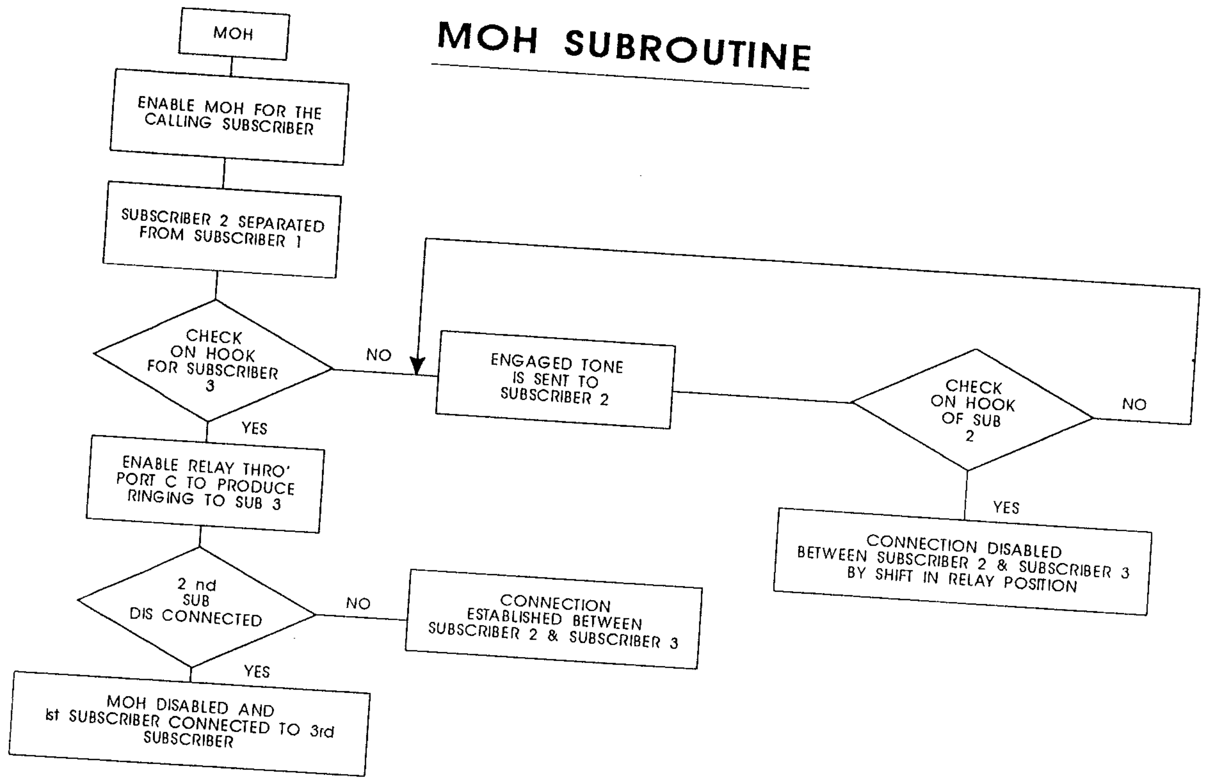
OUTGOING CALL : - INTERCOM TO DOT



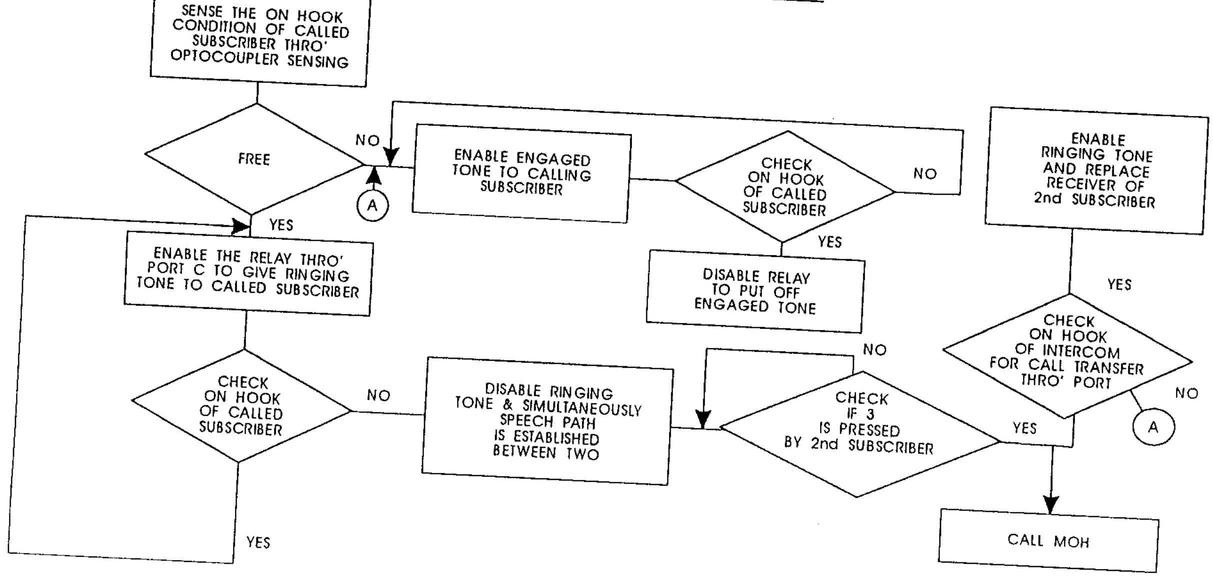
INCOMING CALL

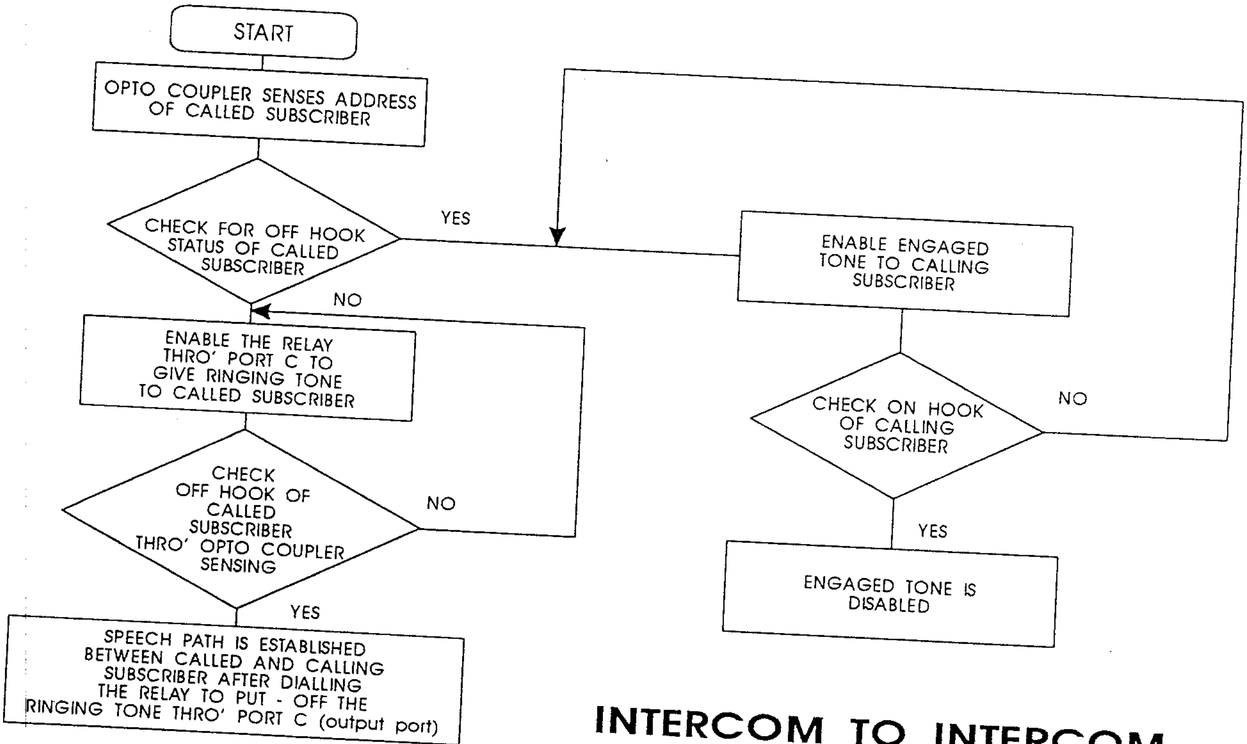


MOH SUBROUTINE



CALL TRANSFER





INTERCOM TO INTERCOM

CONCLUSION

CONCLUSION

The **'MICROCONTROLLER BASED TELEPHONE EXCHANGE'** has been designed, fabricated and tested to conform to the target specifications.

Details about the Microcontroller has been enclosed. The chips pin configuration, operational characteristics of all the chips used in implementing the hardware has also been explained.

There are also provisions for future developments such as Dual Tone Multi Frequency, which is a faster mode of operation than the pulse mode. The report also features the switching matrix principles and its role in implementing the features. What has been achieved through the project can at best be a techno-compromise to give an optimum performance.

APPENDIX

intel

PRELIMINARY

27C256/87C256 256K (32K x 8) CHMOS PRODUCTION AND UV ERASABLE PROMS

- **CHMOS/NMOS Microcontroller and Microprocessor Compatible**
  - 87C256-Integrated Address Latch
  - Universal 28 Pin Memory Site, 2-line Control
- **Low Power Consumption**
  - 100 µA Maximum Standby Current
- **High Performance Speeds**
  - 170 ns Maximum Access Time
- **Noise Immunity Features**
  - ±10% V_{CC} Tolerance
  - Maximum Latch-up Immunity Through EPI Processing
- **New Quick-Pulse Programming™ Algorithm**
  - 4 Second Programming
- **Available in 28-Pin Cerdip Package and 32-Lead PLCC Package.**
  (See Packaging Spec., Order #231369)

Intel's 27C256 and 87C256 CHMOS EPROMs are 256K bit 5V only memories organized as 32,768 words of 8 bits. They employ advanced CHMOS*II-E circuitry for systems requiring low power, high performance speeds, and immunity to noise. The 87C256 has been optimized for multiplexed bus microcontroller and microprocessor compatibility while the 27C256 has a non-multiplexed addressing interface and is plug compatible with the standard Intel 27256 (HMOS II-E).

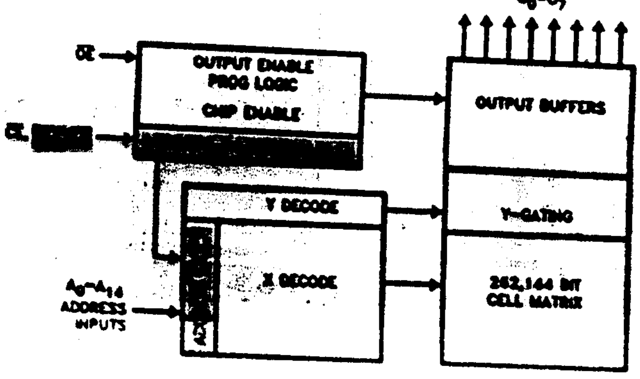
The 27C256 and 87C256(1) are offered in both a ceramic DIP and plastic leaded chip carrier (PLCC) package. Cerdip packages provide flexibility in prototyping and R&D environments, whereas, PLCC EPROMs provide optimum cost effectiveness in production environments. A new Quick-Pulse Programming Algorithm is employed on these devices which may speed up programming by as much as one hundred times. In the absence of Quick-Pulse Compatible programming equipment, the int$_e$ligent Programming™ Algorithm may be utilized.

The 87C256 incorporates an address latch on the address pins to minimize chip count in multiplexed bus systems. Designers can eliminate the address latch by tieing address and data pins of the 87C256 directly to the processor's multiplexed address/data pins. On the falling edge of the ALE input (ALE/$\overline{CE}$), address information at the address inputs (A_0–A_{14}) is latched internally. The address inputs are then ignored as data information is passed on the same bus from the EPROM O_0–O_7 Pins (ALE/$\overline{CE}$ remains low).

The highest degree of protection against latch-up is achieved through Intel's unique EPI processing. Prevention of latch-up is provided for stresses up to 100 mA on address and data pins from −1V to V_{CC} + 1V.

*HMOS and CHMOS are patented processes of Intel Corporation.

NOTE:
1. The 87C256 will be available in 1987.



290044-1

Figure 1. Block Diagram

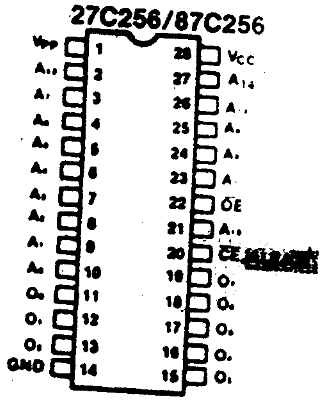
... represent the 87C256 version

Pin Names

A_0–A_{14}	ADDRESSES
O_0–O_7	OUTPUTS
$\overline{OE}$	OUTPUT ENABLE
$\overline{CE}$	CHIP ENABLE
[redacted]	
N.C.	NO CONNECT
D.U.	DON'T USE

27128	2764A	2732A	2716
V_{PP}	V_{PP}		
A_{12}	A_{12}		
A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
Gnd	Gnd	Gnd	Gnd

27C256/87C256

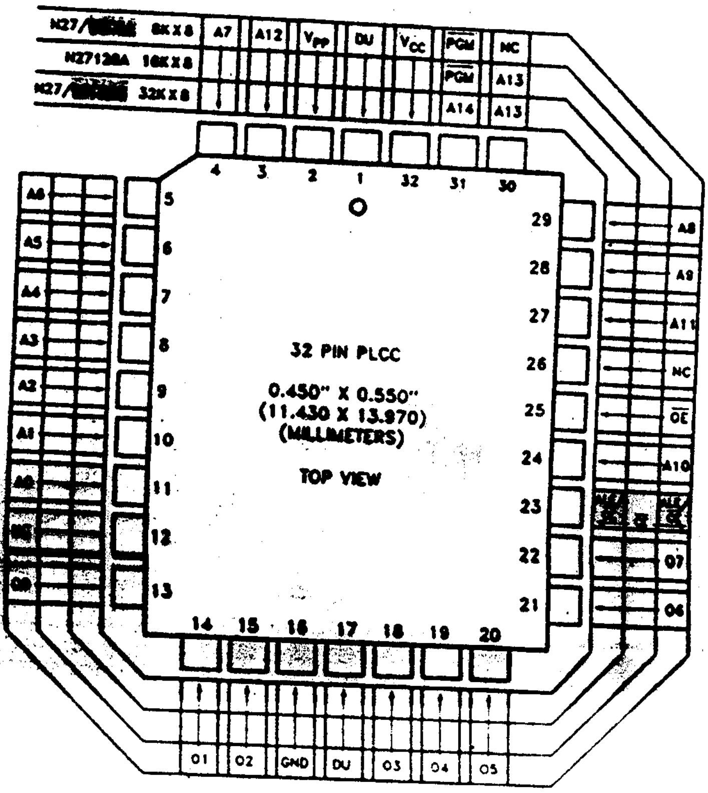


2716	2732A	2764A	27128
		V_{CC}	V_{CC}
		$\overline{PGM}$	$\overline{PGM}$
V_{CC}	V_{CC}	N.C.	A_{13}
A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3

290044-2

Figure 2. Pin Configuration

NOTE:
Intel "Universal Site" -Compatible EPROM Pin Configurations are Shown in the Blocks Adjacent.
Shaded Areas [redacted] represent the 87C256 version



290044-10

Figure 3. PLCC Lead Configuration

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS Options

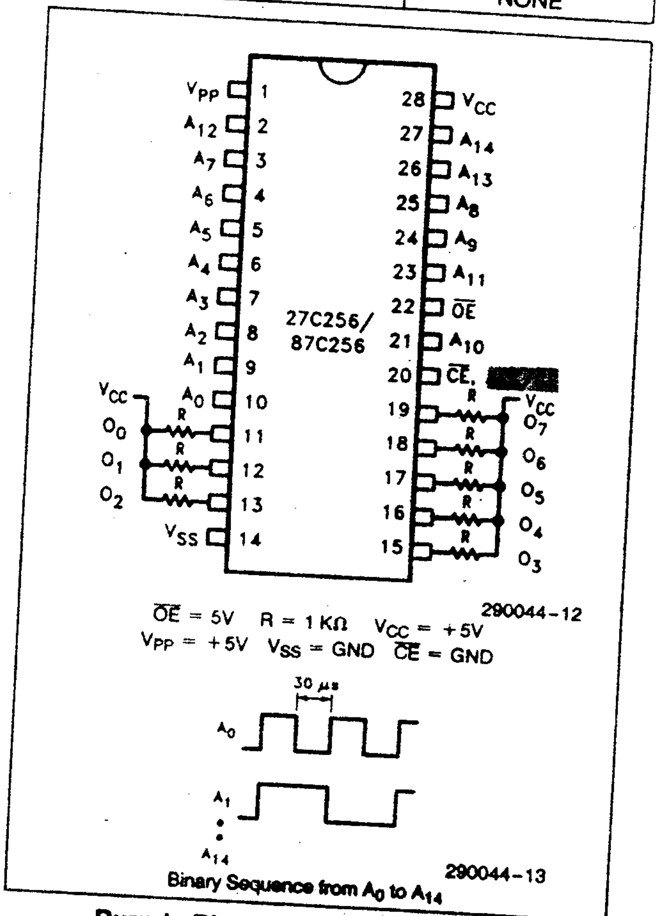
27C256 Versions

Speed Versions	Packaging Options	
	Cerdip	PLCC
−1		
−17		
−2	T, L, Q	
−20	T, L, Q	
STD	T, L, Q, A	
−25	T, L, Q, A	
−3	T, L, Q, A	
−30	T, L, Q, A	

EPROM Product Family

PRODUCT DEFINITIONS

Type	Operating Temperature (°C)	Burn-in 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	NONE
L	−40°C to +85°C	168 ±8
A	−40°C to +125°C	NONE



Burn-In Bias and Timing Diagrams

READ OPERATION

D.C. CHARACTERISTICS

Electrical Parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for:

Symbol	Parameter		27C256 Min	27C256 Max	Test Conditions
I_{SB}	V_{CC} Standby Current (ma)	CMOS		0.1	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
		TTL		1.0	
I_{CC}(1)	V_{CC} Active Current (ma)	TTL		30	$\overline{OE} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature (ma)	TTL		30	$\overline{OE} = \overline{CE} = V_{IL}$ $V_{PP} = V_{CC}$, $T_{Ambient} = 85°C$

NOTE:
1. The maximum current value is with outputs O_0 to O_7 unloaded.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature During Read .... 0°C to +70°C(2)
Temperature Under Bias .... −10°C to +80°C(2)
Storage Temperature .... −65°C to +125°C
Voltage on Any Pin with Respect to Ground .... −2V to +7V(1)
Voltage on A_9 with Respect to Ground .... −2V to +13.5V(1)
V_{PP} supply Voltage with Respect to Ground during programming .... −2V to +14.0V(1)
V_{CC} Supply Voltage with Respect to Ground .... −2V to +7.0V(1)

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

READ OPERATION

D.C. CHARACTERISTICS: 27C256/87C256

Symbol	Parameter		Notes	Min	Typ(3)	Max	Units	Test Condition
I_{LI}	Input Load Current				0.01	1.0	μA	V_{IN} = 5.5V
I_{LO}	Output Leakage Current				0.01	1.0	μA	V_{OUT} = 5.5V
I_{PP_1}	V_{PP} Read Current		5			200	μA	V_{PP} = V_{CC}
I_{SB}	V_{CC} Current Standby	CMOS	4			100	μA	$\overline{CE}$ = V_{CC}
			8			1.0	mA	$\overline{CE}$ = V_{IH}
I_{CC_1}	V_{CC} Current Active		5, 8			30	mA	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA
V_{IL}	Input Low Voltage (±10% Supply) (TTL)			−0.5		0.8	V	V_{PP} = V_{CC}
	Input Low Voltage (CMOS)			−0.2		0.2		
V_{IH}	Input High Voltage (±10% Supply) (TTL)			2.0		V_{CC} + 0.5	V	V_{PP} = V_{CC}
	Input High Voltage (CMOS)			V_{CC} − 0.2		V_{CC} + 0.2		
V_{OL}	Output Low Voltage					0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage			3.5			V	I_{OH} = −2.5 mA
I_{OS}	Output Short Circuit Current		6			100	mA	
V_{PP}	V_{PP} Read Voltage		7	V_{CC} − 0.7		V_{CC}	V	

NOTES:

1. **Minimum D.C. input voltage is −0.5V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns. Maximum D.C. voltage on output pins is V_{CC} + 0.5V which may overshoot to V_{CC} + 2V for periods less than 20 ns.**
2. Operating temperature is for commercial product defined by this specification. Extended temperature options are available in EXPRESS and Military version.
3. Typical limits are at V_{CC} = 5V, T_A = +25°C.
4. ALE/$\overline{CE}$ or $\overline{CE}$ is V_{CC} ±0.2V. All other inputs can have any value within spec.
5. **Maximum Active power usage is the sum I_{PP} + I_{CC}. The maximum current value is with outputs O_0 to O_7 unloaded.**
6. **Output shorted for no more than one second. No more than one output shorted at a time. I_{OS} is sampled but not 100% tested.**
7. V_{PP} may be one diode voltage drop below V_{CC}. It may be connected directly to V_{CC}. Also, V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
8. V_{IL}, V_{IH} levels at TTL inputs.

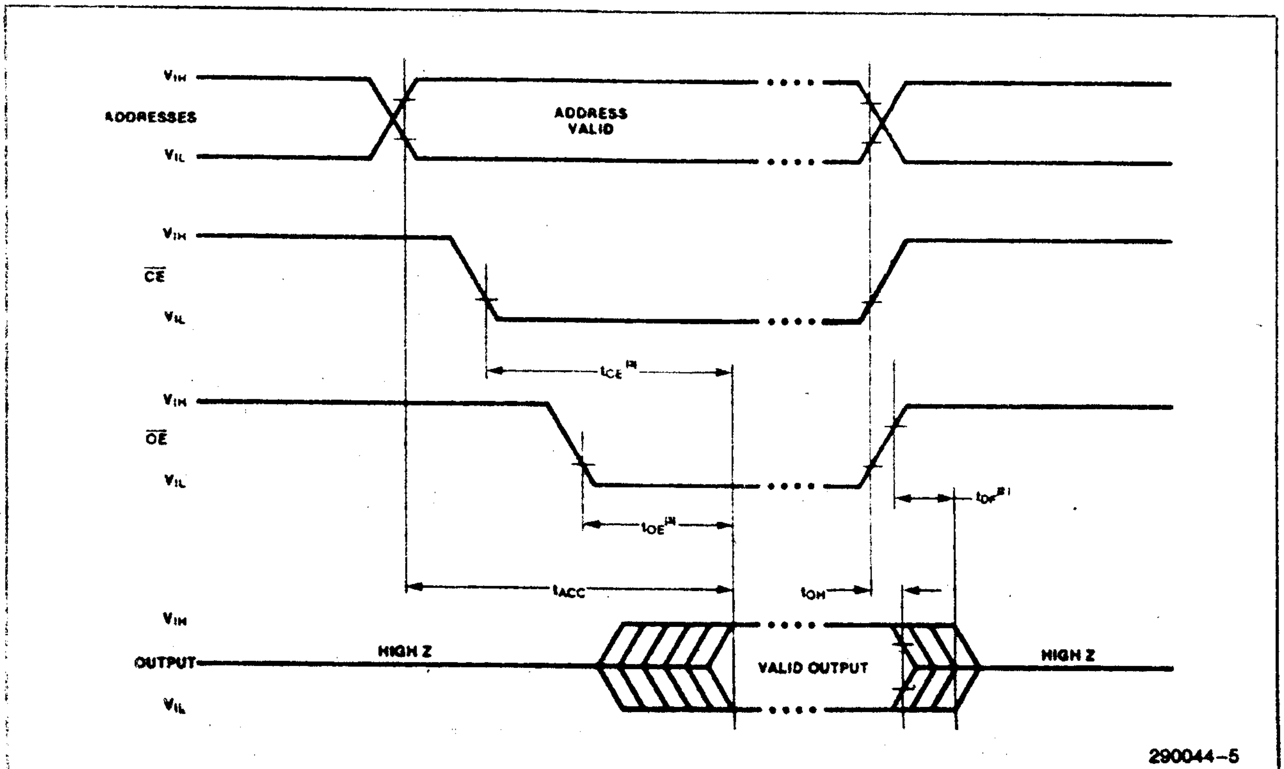
READ OPERATION

A.C. CHARACTERISTICS 27C256(1) 0°C ≤ T_A ≤ +70°C

Versions(3)		V_{CC} ±5%	27C256-1 N27C256-1		27C256-2 N27C256-2		27C256 N27C256		27C256-3 N27C256-3		Unit
		V_{CC} ±10%			27C256-20 N27C256-20		27C256-25 N27C256-25		27C256-30 N27C256-30		
Symbol	Characteristic		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay			170		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay			170		200		250		300	ns
t_{OE}	$\overline{OE}$ to Output Delay			70		75		100		120	ns
t_{DF}(2)	$\overline{OE}$ High to Output High Z			55		55		60		75	ns
t_{OH}(2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change-Whichever is First		0		0		0		0		ns

NOTES:
1. A.C. characteristics tested at V_{IH} = 2.4V and V_{IL} = 0.45V. Timing measurements made at V_{OL} = 0.8V and V_{OH} = 2.0V.
2. Guaranteed and sampled.
3. Model Number Prefixes: No Prefix = CERDIP; N = PLCC.

A.C. WAVEFORMS 27C256



NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

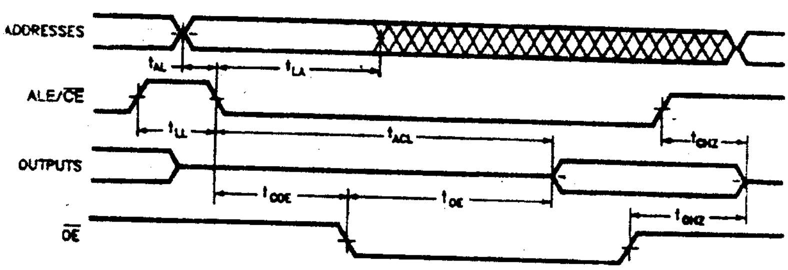
READ OPERATION

A.C. CHARACTERISTICS [redacted]

Versions[3]		V_{CC} ±5%	87C256-2 N87C256-2		87C256 N87C256		87C256-3 N87C256-3		Unit
		V_{CC} ±10%	87C256-20 N87C256-20		87C256-25 N87C256-25		87C256-30 N87C256-30		
Symbol	Parameter		Min	Max	Min	Max	Min	Max	
t_{LL}	Chip Deselect Width		50		60		75		ns
t_{AL}	Address to CE-Latch Set-up		20		25		30		ns
t_{LA}	Address Hold from CE-LATCH		45		50		60		ns
t_{ACL}	CE-Latch Access Time			200		250		300	ns
t_{OE}	Output Enable to Output Valid			75		100		120	ns
t_{COE}	ALE/$\overline{CE}$ to Output Enable		45		50		60		ns
t_{CHZ}[2]	Chip Deselect to Output in High Z			55		60		75	ns
t_{OHZ}[2]	Output Disable to Output in High Z			55		60		75	ns

NOTES:
1. A.C. characteristics tested at V_{IH} = 2.4V and V_{IL} = 0.45V. Timing measurements made at V_{OL} = 0.8V and V_{OH} = 2.0V.
2. Guaranteed and sampled.
3. Model Number Prefixes: No prefix = CERDIP; N = PLCC.

A.C. WAVEFORMS 87C256



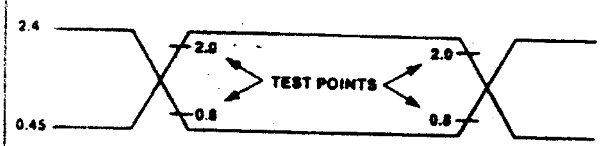
290044-6

CAPACITANCE(1) $T_A = 25°C$, f = 1.0 MHz

Symbol	Parameter	Max	Units	Conditions
C_{IN}	Address/control capacitance	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	12	pF	$V_{OUT} = 0V$

NOTE:
1. Sampled. Not 100% tested.

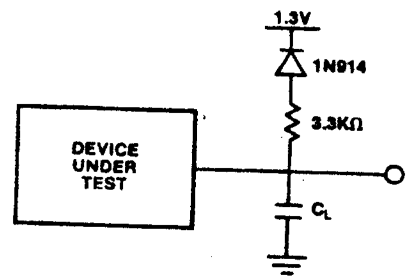
A.C. TESTING INPUT/OUTPUT WAVEFORM



290044-9

A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0" timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L Includes Jig Capacitance

290044-3

DEVICE OPERATION

The modes of operation of the 27C256/87C256 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for int$_e$ligent Identifier™ mode.

Table 1. Mode Selection for 27C256 and 87C256

Mode \ Pins	ALE/$\overline{CE}$	$\overline{OE}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X(1)	X	V_{CC}	5.0V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby	V_{IH}	X	X	X	V_{CC}	5.0V	High Z
Programming	V_{IL}	V_{IH}	X	X	(Note 4)	(Note 4)	D_{IN}
Program Verify	V_{IH}	V_{IL}	X	X	(Note 4)	(Note 4)	D_{OUT}
Optional Program Verify	V_{IL}	V_{IL}	X	X	V_{CC} (Note 4)	(Note 4)	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	X	X	(Note 4)	(Note 4)	HIGH Z
int$_e$ligent Identifier (3) -Manufacturer	V_{IL}	V_{IL}	V_H(2)	V_{IL}	V_{CC}	V_{CC}	89 H
int$_e$ligent Identifier (3) -27C256	V_{IL}	V_{IL}	V_H(2)	V_{IH}	V_{CC}	V_{CC}	8C H
int$_e$ligent Identifier (3, 5) -87C256	V_{IL}	V_{IL}	V_H(2)	V_{IH}	V_{CC}	V_{CC}	80 H

NOTES:
1. X can be V_{IL} or V_{IH}
2. V_H = 12.0V ± 0.5V.
3. A_1-A_8, $A_{10-12} = V_{IL}$.
4. See Table 2 for V_{CC} and V_{PP} voltages during programming.
5. ALE/$\overline{CE}$ has to be toggled in order to latch in the addresses and read the signature codes.

Read Mode: 27C256

The 27C256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Read Mode: 87C256

The 87C256 was designed to reduce the hardware interface requirements when incorporated in processor systems with multiplexed address-data busses. Chip count (and therefore power and board space) can be minimized when the 87C256 is designed as shown in Figure 4. The processor's multiplexed bus (AD_{0-7}) is tied to both address and data pins of the 87C256. All address inputs of the 87C256 are latched when ALE/$\overline{CE}$ is brought low thus eliminating the need for a seperate address latch.

The 87C256 internal address latch is directly enabled through the use of the ALE/$\overline{CE}$ line. As the transition occurs on the ALE/$\overline{CE}$ from the TTL high to the low state, the last address presented at the address pins is retained. Data is then enabled onto the bus from the EPROM via the $\overline{OE}$ pin.

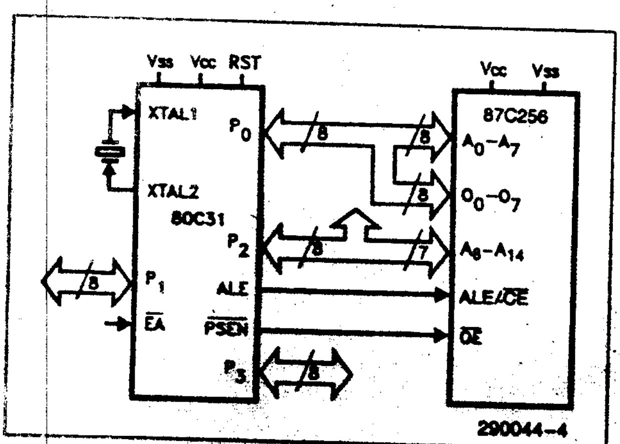


Figure 4. 80C31 with 87C256 System Configuration

Standby Mode

The 27C256 and 87C256 have Standby modes which reduce the maximum V_{CC} current to 100 μA. Both are placed in the Standby mode when $\overline{CE}$ or ALE/$\overline{CE}$ is in the CMOS-high state. When the Standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ (or ALE/$\overline{CE}$) should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control, and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor for low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effect of PC board-traces.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The device is in the programming mode when V_{PP} is raised to its programming voltage (See Table 2) and $\overline{CE}$ (or ALE/$\overline{CE}$) is pulsed to TTL low and $\overline{OE}$ = V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple EPROMS in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ (or ALE/$\overline{CE}$) input inhibits the other devices from being programmed.

Except for $\overline{CE}$ (or ALE/$\overline{CE}$) and $\overline{OE}$ all like inputs of the parallel EPROMs may be common. A TTL low-level pulse applied to the $\overline{CE}$ (or ALE/$\overline{CE}$) input with V_{PP} at its programming voltage will program the selected device.

Program Verify

A verify should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ at V_{IL} and $\overline{CE}$ (or ALE/$\overline{CE}$) at V_{IH}, and V_{PP} and V_{CC} at their programming voltages. Data should be verified a minimum of t_{OE} after the falling edge of $\overline{OE}$.

Optional Program Verify

All 27C256s with V_{PP} = 12.75V (12.5V int$_e$ligent programming) and $\overline{OE}$ = V_{IL} will present data on the bus independent of the $\overline{CE}$ state. The optional verify may be used in place of the verify mode to allow parallel programming where several devices share a common bus. It is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ = V_{IL} (as opposed to the standard verify which has $\overline{CE}$ at V_{IH}), and V_{PP} = V_{CC} = 6.25V (6.0V int$_e$ligent programming). The outputs will then tri-state according to the signals presented to $\overline{OE}$ and $\overline{CE}$. With V_{PP} lowered to V_{CC} (= 6.25V/6.0V—See Table 2), the normal read mode may be used to execute a program verify.

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A_9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the int$_e$ligent Identifier Mode.

Byte 0 (A_0 = V_{IL}) represents the manufacturer code and byte 1 (A_0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1. ALE/$\overline{CE}$ of the 87C256 has to be toggled in order to latch in the addresses and read the signature codes.

INTEL EPROM PROGRAMMING SUPPORT TOOLS

Intel offers a full line of EPROM Programmers providing state-of-the-art programming for Intel programmable devices. The modular architecture of Intel's EPROM programmers allows you to add new suport as it becomes available, with very low cost add-ons. For example, even the earliest users of the iUP-FAST 27/K module may take advantage of Intel's new Quick-Pulse Programming Algorithm, the fastest in the industry.

Intel EPROM programmers may be controlled from a host computer using Intel's PROM Programming software (iPPS). iPPS makes programming easy for a growing list of industry standard hosts, including the IBM PC, XT, AT, and PCDOS compatibles, Intellec Development Systems. Intel's iPDS Personal Development Systems, and the Intel Network Development System (iNDS-II). Stand-alone operation is also available, including device previewing, editing, programming, and download of programming data from any source over an RS232C port.

For further details consult the EPROM Programming section of the Development Systems Handbook.

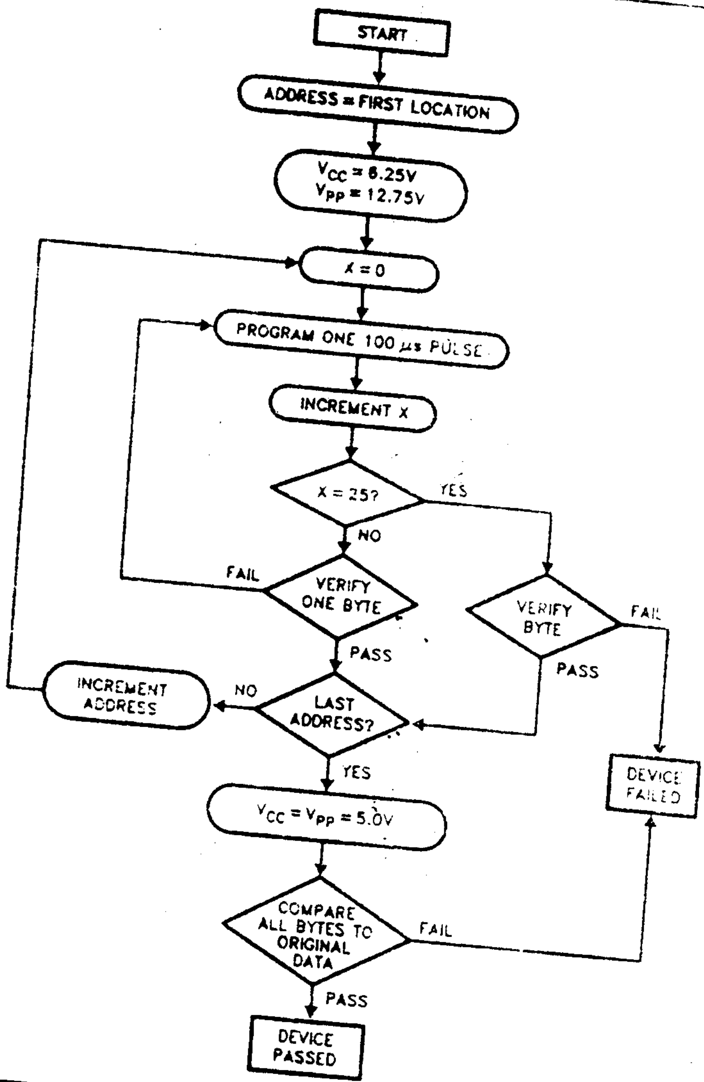


Figure 5. Quick-Pulse Programming™ Algorithm

ERASURE CHARACTERISTICS (FOR CERDIP EPROMS)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum inte-

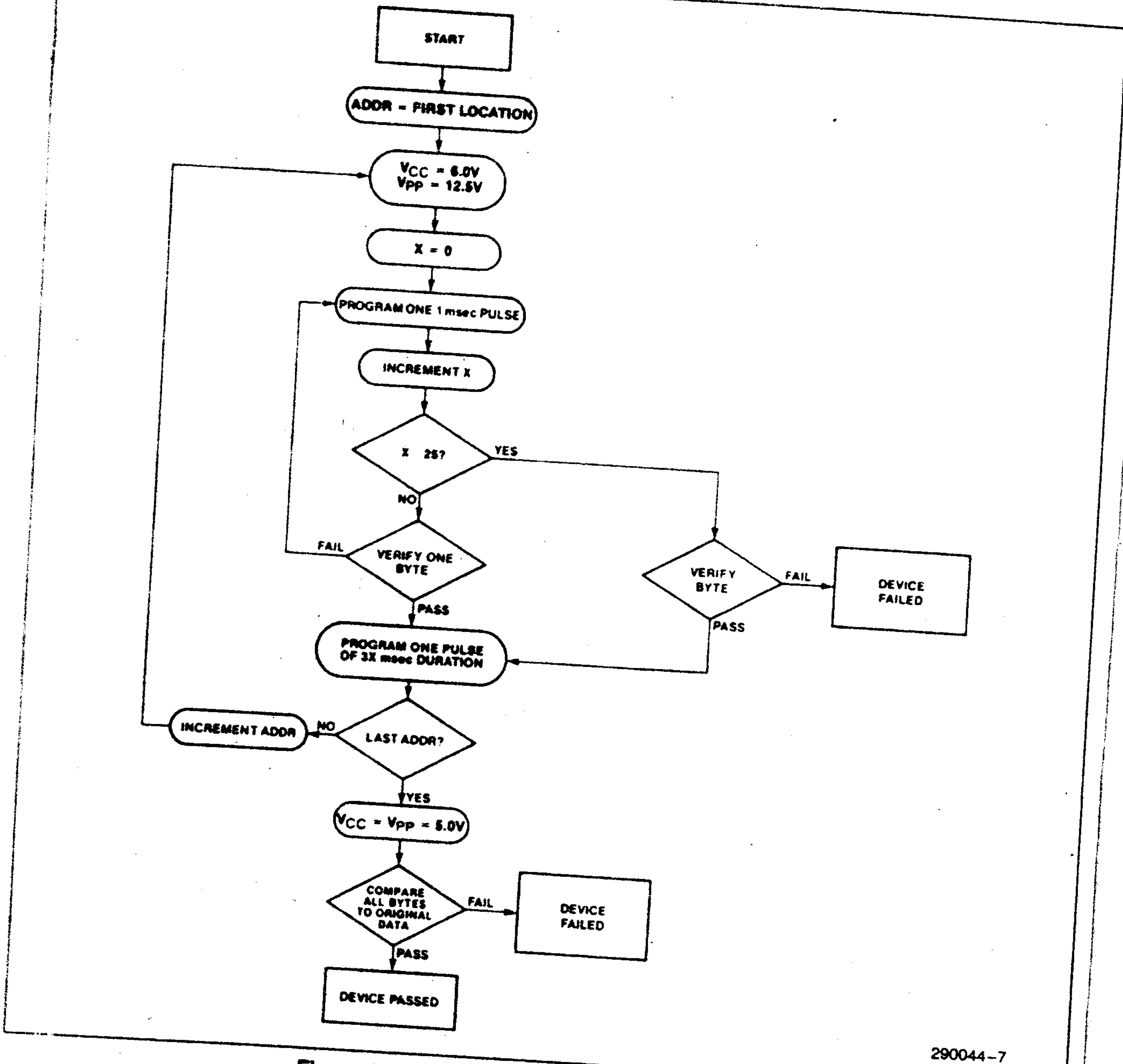


Figure 6. Int$_e$ligent Programming™ Flowchart

grated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for longer periods may cause permanent damage.

CHMOS NOISE CHARACTERISTICS

Special EPI processing techniques have enabled Intel to build CHMOS with features adding to system reliability. These include input/output protection to latch-up. Each of the data and address pins will not latch-up with currents up to 100 mA and voltages from −1V to V_{CC} + 1V.

Additionally, the V_{PP} (programming) pin is designed to resist latch-up to the 14V maximum device limit.

Quick-Pulse Programming™ Algorithm

Intel's 27C256 EPROMs can now be programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production programming environment. This algorithm allows 27C256s to be programmed in under four seconds, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 microseconds followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25 100 μs pulses per byte are provided before a failure is recognized. A flowchart of the Quick-Pulse Programming Algorithm is shown in Figure 5.

For the Quick-Pulse Programming Algorithm, the entire sequence of programming pulses and byte verifications is preformed at V_{CC} = 6.25V and V_{PP} at 12.75V. When programming of the EPROM has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP}$ = 5.0V.

In addition to the Quick-Pulse Programming Algorithm, the 27C256 is also compatible with Intel's Inteligent Programming Algorithm.

Inteligent Programming™ Algorithm

The Inteligent Programming Algorithm has been a standard in the industry for the past few years. A flow-chart of the inteligent Programming Algorithm is shown in Figure 6.

The inteligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial pulse(s) is one millisecond, which will then be followed by a larger overprogram pulse of length 3X msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V and V_{PP} = 12.5V. When the inteligent Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP}$ = 5.0V.

TABLE 2. D.C. PROGRAMMING CHARACTERISTICS 27C256/87C256
T_A = 25°C ±5°C

Symbol	Parameter	Limits Min	Limits Max	Limits Unit	Test Conditions
I_{LI}	Input Current (All Inputs)		1.0	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage During Verify	3.5		V	I_{OH} = −2.5 mA
I_{CC2}(4)	V_{CC} Supply Current		30	mA	
I_{PP2}(4)	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = V_{IL}$
V_{ID}	A_9 inteligent Identifier Voltage	11.5	12.5	V	
V_{PP}	inteligent Programming Algorithm	12.0	13.0	V	
	Quick-Pulse Programming Algorithm	12.5	13.0	V	
V_{CC}	inteligent Programming Algorithm	5.75	6.25	V	
	Quick-Pulse Programming Algorithm	6.0	6.5	V	

A.C. PROGRAMMING CHARACTERISTICS 87C256/87C256
$T_A = 25°C \pm 5°C$; see Table 2 for V_{CC} and V_{PP} Voltages.

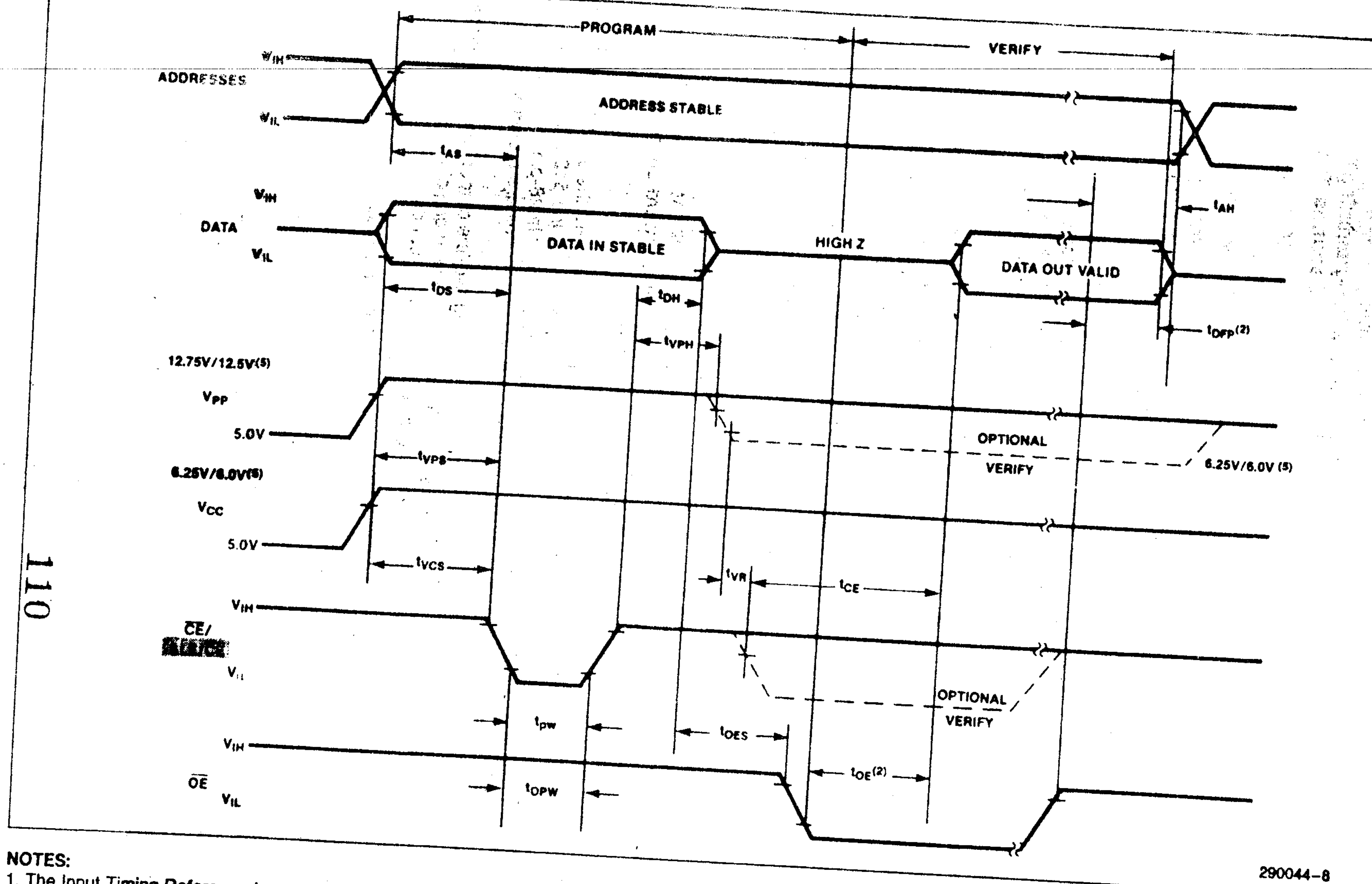
Symbol	Parameter	Limits				Conditions
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			µs	
t_{OES}	$\overline{OE}$ Setup Time	2			µs	
t_{DS}	Data Setup Time	2			µs	
t_{AH}	Address Hold Time	0			µs	
t_{DH}	Data Hold Time	2			µs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(See Note 3)
t_{VPS}	V_{PP} Setup Time	2			µs	
t_{VCS}	V_{CC} Setup Time	2			µs	
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	95	100	105	µs	Quick-Pulse
		0.95	1.0	1.05	ms	int$_e$ligent
t_{OPW}	$\overline{CE}$ Overprogram Pulse Width	2.85		78.75	ms	(See Note 2)
t_{OE}	Data Valid from $\overline{OE}$			150	ns	
t_{CE}	$\overline{CE}$ to Output Delay			500	ns	Optional Verify
t_{VR}	V_{PP} Recovery Time	2			µs	Optional Verify
t_{VPH}	V_{PP} Hold Time	2			µs	Optional Verify

A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) ...... 20 ns
Input Pulse Levels .... 0.45V to 2.4V
Input Timing Reference Level .... 0.8V and 2.0V
Output Timing Reference Level ...... 0.8V and 3.5V

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse (Intelligent Programming Algorithm) may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. The maximum current value is with outputs O_0 to O_7 unloaded.

PROGRAMMING WAVEFORMS 27C256/87C256



NOTES:
1. The Input Timing Reference Level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 27C256/87C256, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.
4. When programming the 87C256, the address latch function is bypassed with V_{PP} at 12.5V. The device will function just like the 27C256 during read or write. When V_{PP} is at 5.0V during the read mode, the address latch function is enabled and $\overline{CE}$ needs to be toggled to latch in the addresses.
5. 12.75V V_{PP} & 6.25V V_{CC} for Quick-Pulse Programming Algorithm; 12.5V V_{PP} & 6.0V V_{CC} for int$_e$ligent Programming Algorithm.

64K Commercial Industrial X2864A X2864AI 8192 x 8 Bit

Electrically Erasable PROM

FEATURES

- 250 ns Access Time
- Fast Write Cycle Times
  - —16-Byte Page Write Operation
  - —Byte or Page Write Cycle: 5 ms Typical
  - —Complete Memory Rewrite: 2.6 Sec. Typical
  - —Effective Byte Write Cycle Time of 300 μs Typical
- $\overline{\text{DATA}}$ Polling
  - —Allows User to Minimize Write Cycle Time
- High Reliability
  - —Endurance: 10,000 Writes Per Byte
  - —Data Retention: 100 Years
- Simple Byte and Page Write
  - —Single TTL Level $\overline{\text{WE}}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- JEDEC Approved Byte-Wide Pinout

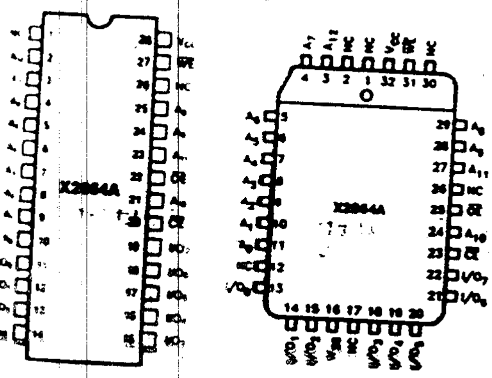
DESCRIPTION

The Xicor X2864A is a 8K x 8 E²PROM, fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V programmable nonvolatile memories. The X2864A features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

The X2864A supports a 16-byte page write operation, effectively providing a 300 μs/byte write and enabling the entire memory to be written in less than 2.6 seconds. The X2864A also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E²PROMs are designed and tested for applications requiring extended endurance and data retention. Endurance is specified as 10,000 cycles per byte minimum and data retention is specified as 100 years minimum. Refer to Xicor reliability reports RR-520 and RR-515 for details of endurance and data retention characteristics.

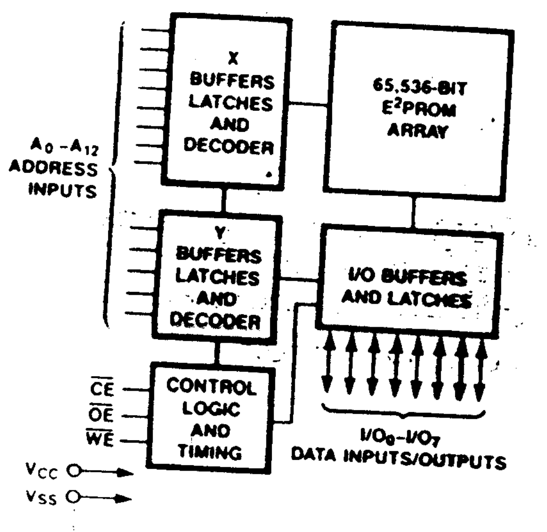
PIN CONFIGURATIONS



0070-

0070-2

FUNCTIONAL DIAGRAM



0070-3

N NAMES

A_0-A_{12}	Address Inputs
$I/O_0-I/O_7$	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

ANCE AND DATA RETENTION

'arameter	Min.	Max.	Units	Conditions
durance	10,000		Cycles/Byte	Xicor Reliability Report RR-520
ta Retention	100		Years	Xicor Reliability Report RR-515

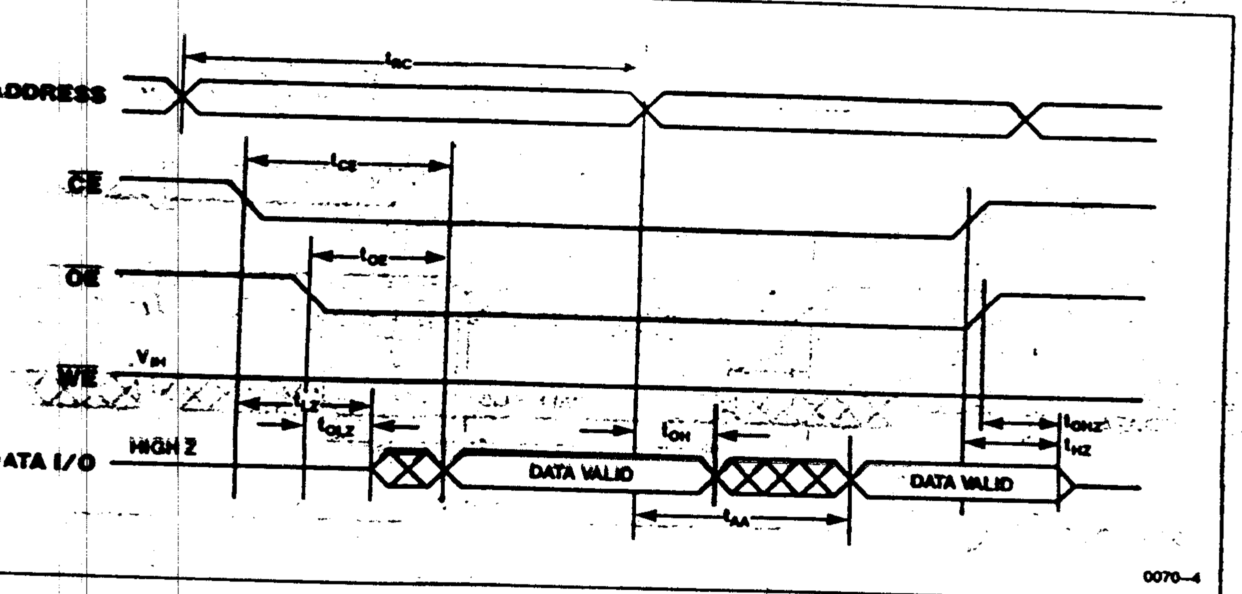
HARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$, unless otherwise specified.
$T_A = -40°C$ to $+85°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.

Cycle Limits

ol	Parameter	X2864A-25 X2864AI-25		X2864A X2864AI		X2864A-35 X2864AI-35		X2864A-45 X2864AI-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
	Read Cycle Time	250		300		350		450		ns
	Chip Enable Access Time		250		300		350		450	ns
	Address Access Time		250		300		350		450	ns
	Output Enable Access Time		100		100		100		100	ns
	Chip Enable to Output in Low Z	10		10		10		10		ns
	Chip Disable to Output in High Z	10	60	10	80	10	80	10	100	ns
4)	Output Enable to Output in Low Z	10		10		10		10		ns
4)	Output Disable to Output in High Z	10	60	10	80	10	80	10	100	ns
	Output Hold from Address Change	10		10		10		10		ns

Cycle



t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven. t_{HZ} min., t_{OHZ} min., t_{LZ} min. and t_{OLZ} min. are periodically sampled and are not 100% tested.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X2864A .... −10°C to +85°C
X2864AI .... −65°C to +135°C
Storage Temperature .... −65°C to +150°C
Voltage on any Pin with Respect to Ground .... −1.0V to +7V
D.C. Output Current .... 5 mA
Lead Temperature (Soldering, 10 Seconds) .... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X2864A T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2864AI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	X2864A Limits		X2864AI Limits		Units	Test Conditions
		Min.	Max.	Min.	Max.		
I_{CC}	V_{CC} Current (Active)		140		140	mA	$\overline{CE} = \overline{OE} = V_{IL}$; All I/O's = Open; Other Inputs = V_{CC}
I_{SB}	V_{CC} Current (Standby)		60		70	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$; All I/O's = Open; Other Inputs = V_{CC}
I_{LI}	Input Leakage Current		10		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10		10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V
V_{IL}(3)	Input Low Voltage	−1.0	0.8	−1.0	0.8	V	
V_{IH}(3)	Input High Voltage	2.0	V_{CC} +0.5	2.0	V_{CC} +1.0	V	
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		2.4		V	I_{OH} = −400 µA

TYPICAL POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
t_{PUR}(2)	Power-Up to Read Operation	1	ms
t_{PUW}(2)	Power-Up to Write Operation	5	ms

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(2)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

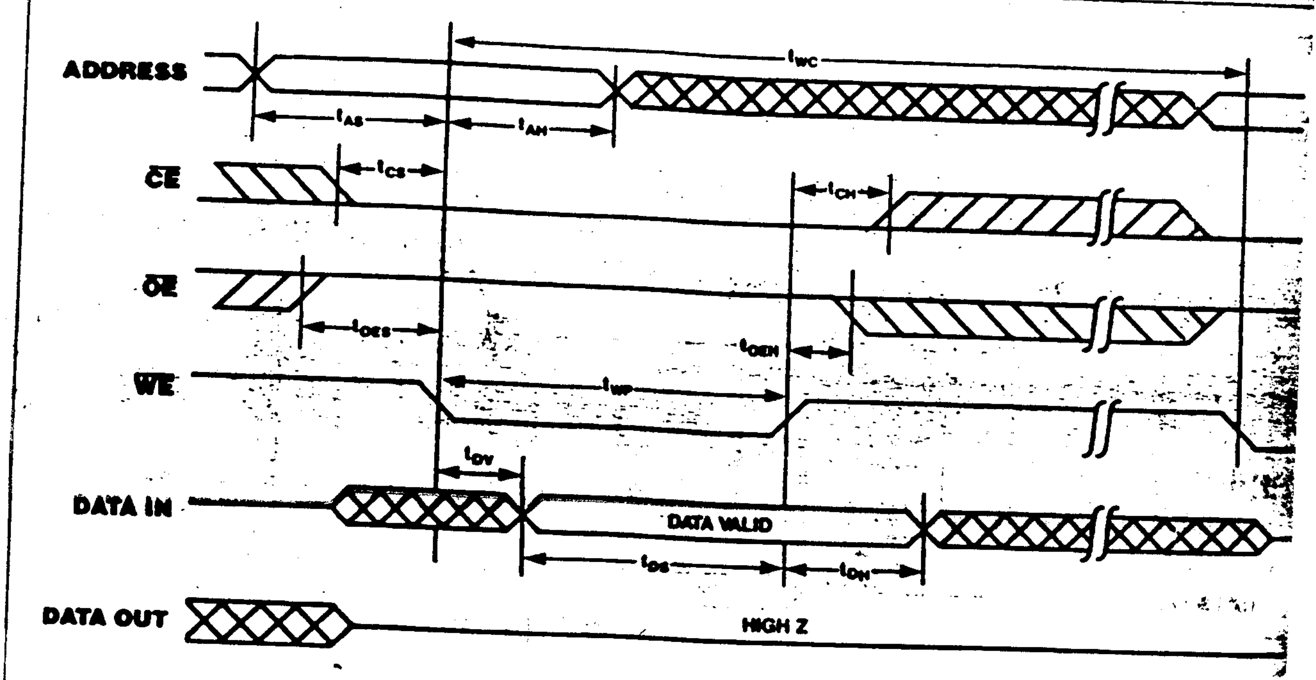
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Pow
L	L	H	Read	D_{OUT}	Activ
L	H	L	Write	D_{IN}	Activ
H	X	X	Standby and Write Inhibit	High Z	Stan
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) This parameter is periodically sampled and not 100% tested.
(3) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

Write Cycle Limits

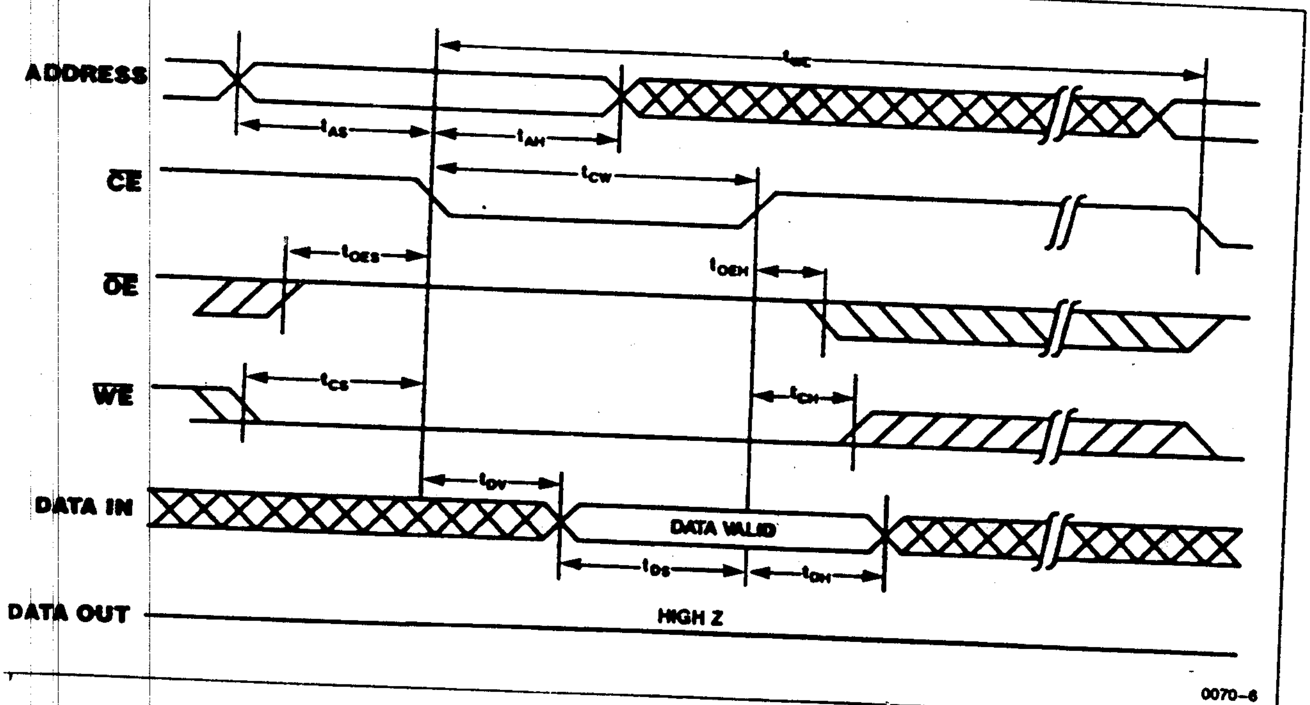
Symbol	Parameter	Min.	Max.	Units
t_{WC}(5)	Write Cycle Time		10	ms
t_{AS}	Address Setup Time	10		ns
t_{AH}	Address Hold Time	200		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}	$\overline{CE}$ Pulse Width	150		ns
t_{OES}	$\overline{OE}$ High Setup Time	10		ns
t_{OEH}	$\overline{OE}$ High Hold Time	10		ns
t_{WP}	$\overline{WE}$ Pulse Width	150		ns
t_{WPH}	$\overline{WE}$ High Recovery	50		ns
t_{DV}	Data Valid		300	ns
t_{DS}	Data Setup	100		ns
t_{DH}	Data Hold	20		ns
t_{DW}	Delay to Next Write	500		µs
t_{BLC}	Byte Load Cycle	3	40	µs

$\overline{WE}$ Controlled Write Cycle



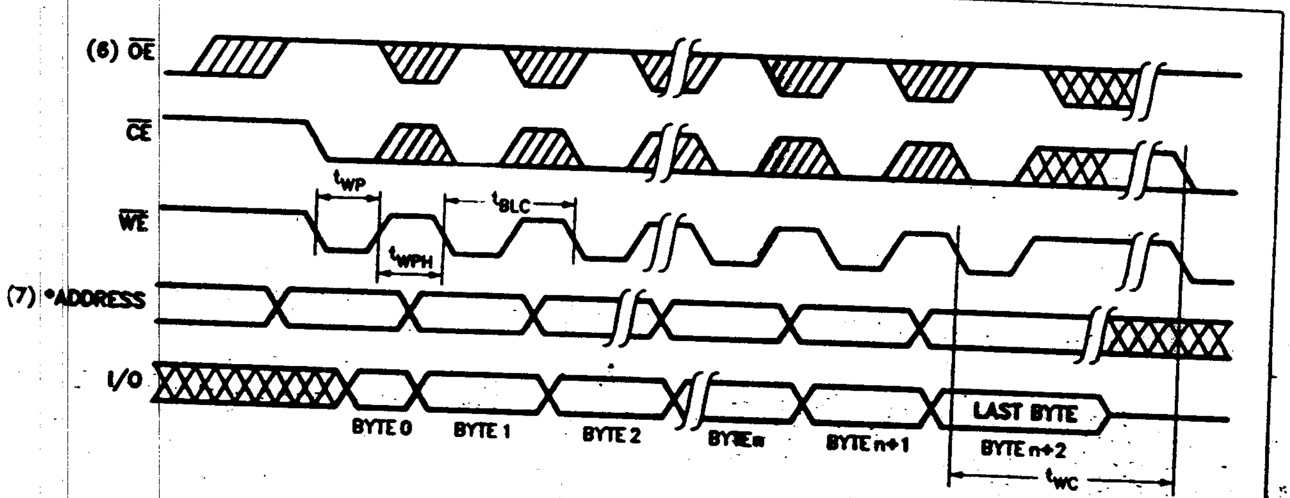
Note: (5) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

E Controlled Write Cycle



0070-6

ge Mode Write Cycle



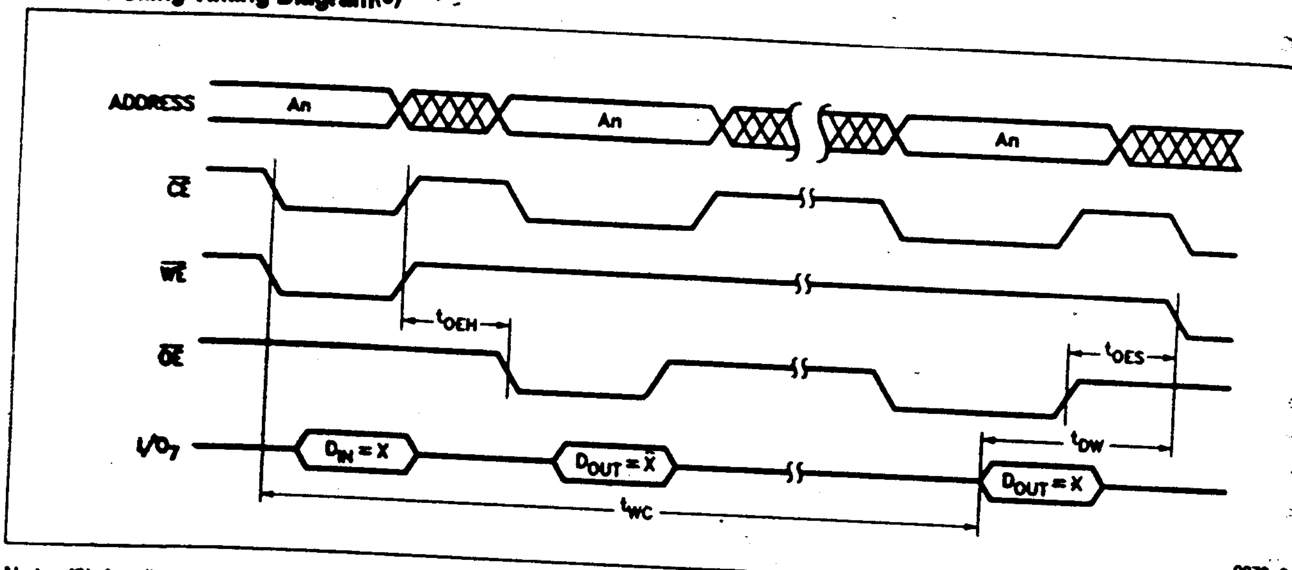
*For each successive write within the page write operation, A_4–A_{12} should be the same or writes to an unknown address could occur.

0070-7

s: (6) Between successive byte writes within a page write operation, OE can be strobed LOW: e.g. this can be done with CE and WE HIGH to fetch data from another memory device within the system for the next write; or with WE HIGH and CE LOW effectively performing a polling operation.

(7) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the CE or WE controlled write cycle timing.

DATA Polling Timing Diagram(8)



Note: (8) A polling operation by definition is a read cycle and therefore subject to read cycle timings.

PIN DESCRIPTIONS

Addresses (A_0–A_{12})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X2864A through the I/O pins.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the X2864A.

DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The X2864A supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Write Operation

The page write feature of the X2864A allows the entire memory to be written in 2.6 seconds. Page write allows two to sixteen bytes of data to be consecutively written to the X2864A prior to the commencement of the internal programming cycle. The destination addresses for a page write operation must reside on the same page; that is, A_4 through A_{12} must not change.

The page write mode can be entered during any write operation. Following the initial byte write cycle, the host can write an additional one to fifteen bytes in the same manner as the first byte was written. Each successive byte write cycle must begin within 20 μs of the falling edge of $\overline{WE}$ of the preceding cycle. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 20 μs the internal automatic programming cycle will commence.

$\overline{DATA}$ Polling

The X2864A features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X2864A, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

WRITE PROTECTION

There are three features that protect the nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse of less than 20 ns will not initiate a write cycle.
- V_{CC} Sense—All functions are inhibited when V_{CC} is ≤3V, typically.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH or $\overline{CE}$ HIGH during power-on and power-off, will inhibit inadvertent writes.

SYSTEM CONSIDERATIONS

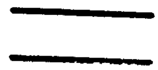
Because the X2864A is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

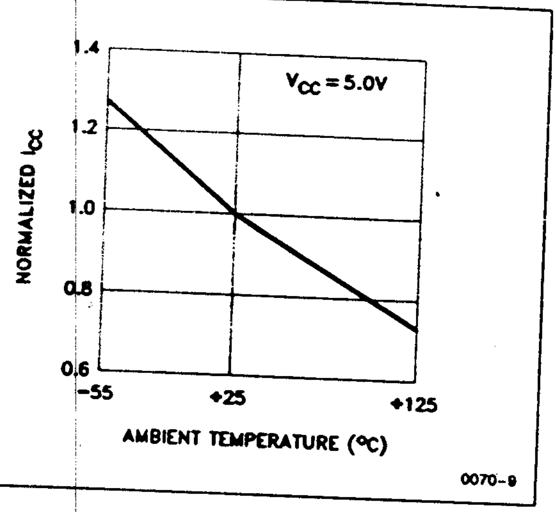
Because the X2864A has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 µF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 µF electrolytic bulk capacitor be placed between V_{CC} and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

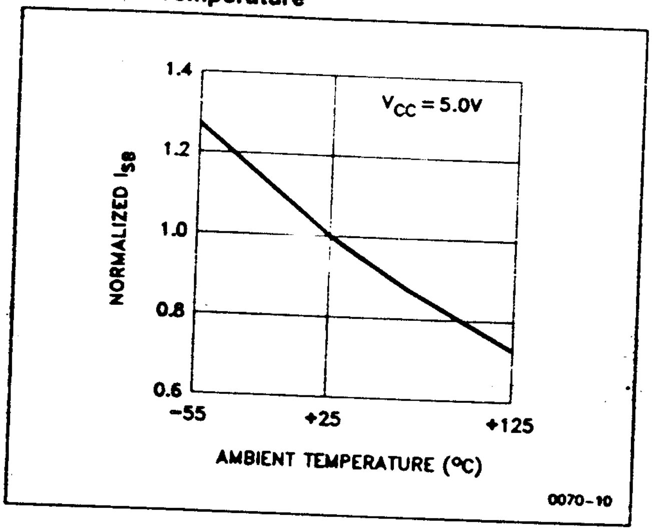
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

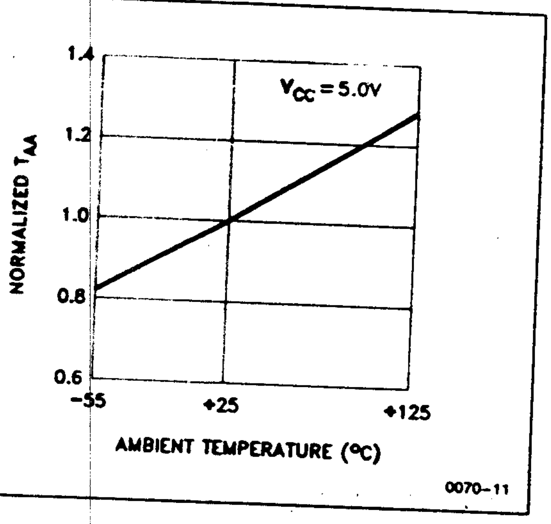
Normalized Active Supply Current vs. Ambient Temperature



Normalized Standby Supply Current vs. Ambient Temperature



Normalized Access Time vs. Ambient Temperature



3

QUADRUPLE 2-INPUT POSITIVE-AND GATES

D2661, APRIL 1982—REVISED DECEMBER 1983

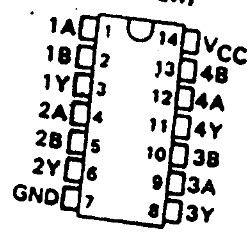
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

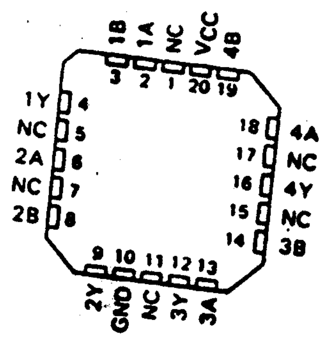
These devices contain four independent 2-input AND gates. They perform the Boolean functions Y = A·B or Y = $\overline{\overline{A}+\overline{B}}$ in positive logic.

The SN54ALS08 and SN54AS08 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS08 and SN74AS08 are characterized for operation from 0°C to 70°C.

SN54ALS08, SN54AS08 . . . J PACKAGE
SN74ALS08, SN74AS08 . . . N PACKAGE
(TOP VIEW)



SN54ALS08, SN54AS08 . . . FH PACKAGE
SN74ALS08, SN74AS08 . . . FN PACKAGE
(TOP VIEW)

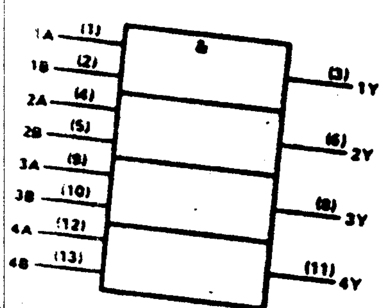


NC—No internal connection

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . 7 V
Input voltage . . . . 7 V
Operating free-air temperature range: SN54ALS08 . . . . −55 °C to 125 °C
SN74ALS08 . . . . 0 °C to 70 °C
Storage temperature range . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS08			SN74ALS08			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS08			SN74ALS08			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2						V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.3	2.4		1.3	2.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		2.2	4		2.2	4	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS08		SN74ALS08		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	4	16	4	14	ns
t_{PHL}	A or B	Y	3	12	3	10	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

2

ALS AND AS CIRCUITS

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Operating free-air temperature range: SN54AS08	−55 °C to 125 °C
SN74AS08	0 °C to 70 °C
Storage temperature range	−65 °C to 150 °C

recommended operating conditions

		SN54AS08			SN74AS08			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS08			SN74AS08			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		5.8	9.3		5.8	9.3	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		14.9	24		14.9	24	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS08		SN74AS08		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	6.5	1	5.5	ns
t_{PHL}	A or B	Y	1	6.5	1	5.5	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, APRIL 1982 – REVISED DECEMBER 1983

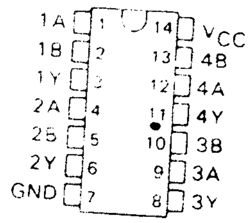
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain four independent 2-input OR gates. They perform the Boolean functions Y = A + B or Y = $\overline{\overline{A} \cdot \overline{B}}$ in positive logic.

The SN54ALS32 and SN54AS32 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS32 and SN74AS32 are characterized for operation from 0 °C to 70 °C.

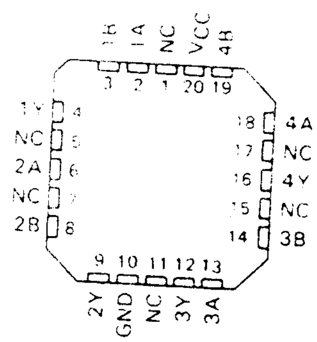
SN54ALS32, SN54AS32 . . . J PACKAGE
SN74ALS32, SN74AS32 . . . N PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each gate)

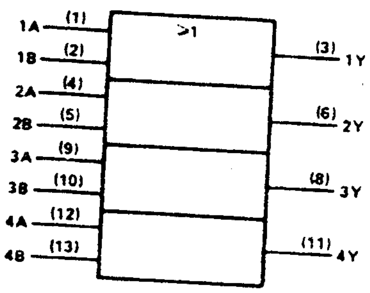
INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

SN54ALS32, SN54AS32 . . . FH PACKAGE
SN74ALS32, SN74AS32 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}		7 V
Input voltage		7 V
Operating free-air temperature range:	SN54AS32	−55 °C to 125 °C
	SN74AS32	0 °C to 70 °C
Storage temperature range		−65 °C to 150 °C

recommended operating conditions

		SN54AS32			SN74AS32			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS32			SN74AS32			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		7.3	12		7.3	12	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		16.5	26.6		16.5	26.6	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS32		SN74AS32		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	7.5	1	5.8	ns
t_{PHL}	A or B	Y	1	6.5	1	5.8	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

2

ALS AND AS CIRCUITS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . 7 V
Input voltage . . . . 7 V
Operating free-air temperature range: SN54ALS32 . . . . −55 °C to 125 °C
SN74ALS32 . . . . 0 °C to 70 °C
Storage temperature range . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS32			SN74ALS32			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS32			SN74ALS32			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.9	4		1.9	4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		2.6	4.9		2.6	4.9	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS32		SN74ALS32		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	3	16	3	14	ns
t_{PHL}	A or B	Y	3	13	3	12	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

2

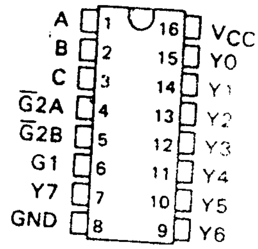
ALS AND AS CIRCUITS

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

D2661, APRIL 1982—REVISED DECEMBER 1983

- Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems
- Incorporates 3 Enable Inputs to Simplify Cascading and/or Data Reception
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS138, SN54AS138 . . . J PACKAGE
SN74ALS138, SN74AS138 . . . N PACKAGE
(TOP VIEW)



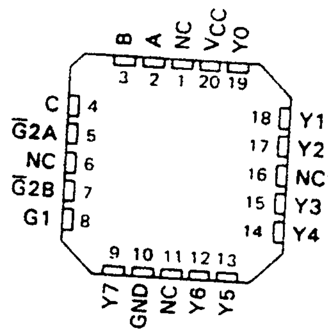
description

The 'ALS138 and 'AS138 circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decorders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

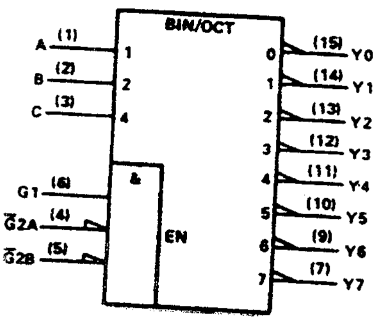
The SN54ALS138 and SN54AS138 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS138 and SN74AS138 are characterized for operation from 0°C to 70°C.

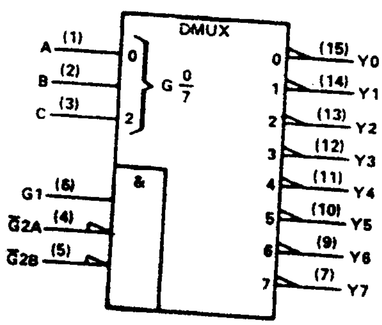
SN54ALS138, SN54AS138 . . . FH PACKAGE
SN74ALS138, SN74AS138 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

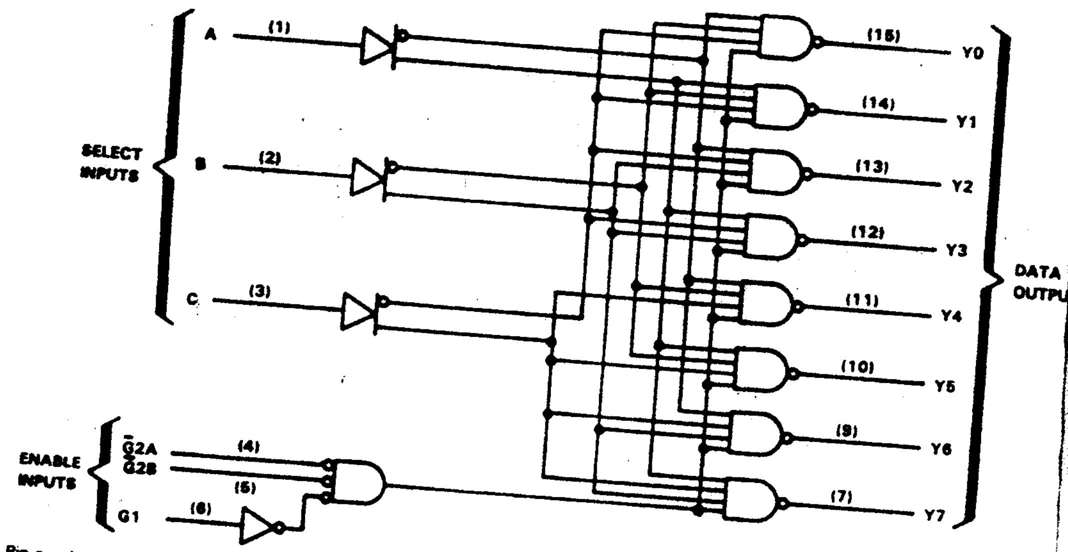
logic symbols (alternatives)





Pin numbers shown are for J and N packages.

logic diagram (positive logic)



Pin numbers shown are for J and N packages.

FUNCTION TABLE

ENABLE INPUTS		SELECT INPUTS			OUTPUTS							
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*$\overline{G2} = \overline{G2A} + \overline{G2B}$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ....

Input voltage ....

Operating free-air temperature range: SN54ALS138, SN54AS138 .... −55°C to

SN74ALS138, SN74AS138 .... 0°C to

Storage temperature range .... −65°C to

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

		SN54ALS138 MIN	SN54ALS138 NOM	SN54ALS138 MAX	SN74ALS138 MIN	SN74ALS138 NOM	SN74ALS138 MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS138 MIN	SN54ALS138 TYP†	SN54ALS138 MAX	SN74ALS138 MIN	SN74ALS138 TYP†	SN74ALS138 MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	$V_{CC}-2$			$V_{CC}-2$			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			5	10		5	10	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALS138 MIN	SN54ALS138 MAX	SN74ALS138 MIN	SN74ALS138 MAX	UNIT
			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				
t_{PLH}	A, B, C	Any Y	6	27	6	22	ns
t_{PHL}			6	22	6	18	
t_{PLH}	Enable	Any Y	4	20	4	17	ns
t_{PHL}			5	20	5	17	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

2

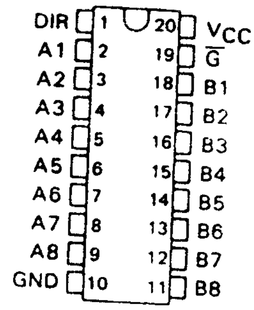
ALS AND AS CIRCUITS

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982 – REVISED DECEMBER 1983

- **3-State Outputs Drive Bus Lines Directly**
- **P-N-P Inputs Reduce Dc Loading**
- **'AS Version in Development. Data Will Be Provided As It Becomes Available. Contact the Factory for Latest Information**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS245A, SN54AS245 . . . J PACKAGE
SN74ALS245A, SN74AS245 . . . N PACKAGE
(TOP VIEW)



description

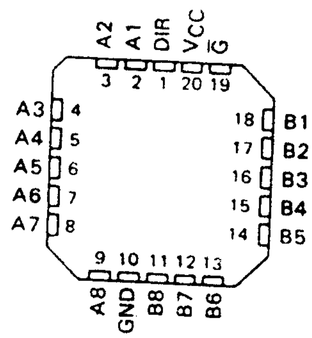
These octal bus transceivers are designed for synchronous two-way communication between data buses The control function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

The -1 version of the SN74ALS245A is identical to the standard version except that the recommended maximum I_{OL} is increased to 48 milliamperes. There is no – 1 version of the SN54ALS245A.

The SN54ALS245A and SN54AS245 are characterized for operation over the full military temperature range of – 55 °C to 125 °C. The SN74ALS245A and SN74AS245 are characterized for operation from 0 °C to 70 °C.

SN54ALS245A, SN54AS245 . . . FH PACKAGE
SN74ALS245A, SN74AS245 . . . FN PACKAGE
(TOP VIEW)



FUNCTION TABLE

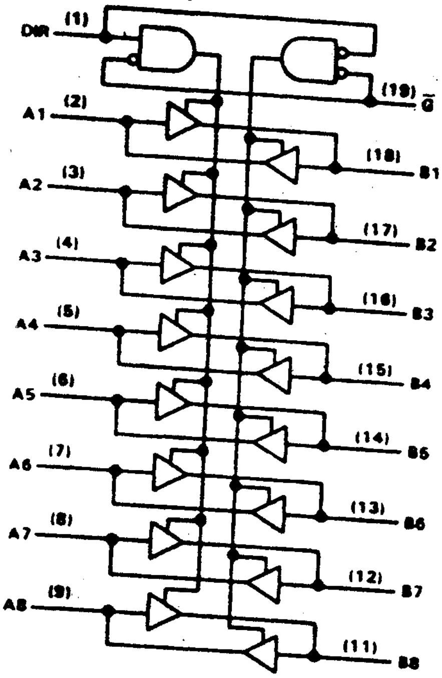
ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

2

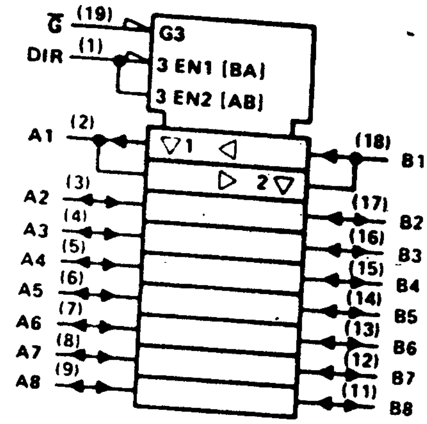
ALS AND AS CIRCUITS

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

logic diagram (positive logic)



logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . 7 V
Input voltage: All inputs . . . . 7 V
I/O ports . . . . 5.5 V
Operating free-air temperature range: SN54ALS245A . . . . −55°C to 125°C
SN74ALS245A . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS245A			SN74ALS245A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24 48†	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
† The 48-mA limit applies for the SN74ALS245A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS245A MIN	SN54ALS245A TYP†	SN54ALS245A MAX	SN74ALS245A MIN	SN74ALS245A TYP†	SN74ALS245A MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports‡					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		30	48		30	45	mA
			Outputs low		36	60		36	55	
			Outputs disabled		38	63		38	58	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}

switching characteristics (see Note 1)

V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALS245A MIN	SN54ALS245A MAX	SN74ALS245A MIN	SN74ALS245A MAX	UNIT
t_{PLH}	A or B	B or A	3	15	3	10	ns
t_{PHL}			3	13	3	10	
t_{PZH}	$\overline{G}$	A or B	5	25	5	20	ns
t_{PZL}			5	25	5	20	
t_{PHZ}	$\overline{G}$	A or B	2	12	2	10	ns
t_{PLZ}			4	18	4	15	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . 7 V
Input voltage: All inputs . . . . 7 V
I/O ports . . . . 5.5 V
Operating free-air temperature range: SN54AS245 . . . . −55 °C to 125 °C
SN74AS245 . . . . 0 °C to 70 °C
Storage temperature range . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS245			SN74AS245			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			32			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS245			SN74AS245			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					50			50	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports‡					−0.75			−0.75	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		62			62		mA
			Outputs low		95			95		
			Outputs disabled		79			79		

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

2 ALS AND AS CIRCUITS

PRODUCT PREVIEW

This page contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS245			SN74AS245			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A or B	B or A		6			6		ns
t_{PHL}				5			5		
t_{PZH}	$\overline{G}$	A or B		8			8		ns
t_{PZL}				8			8		
t_{PHZ}	$\overline{G}$	A or B		4.5			4.5		ns
t_{PLZ}				5			5		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

2

ALS AND AS CIRCUITS

PRODUCT PREVIEW

This page contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

National Semiconductor

PRELIMINARY

DM54ALS14/DM74ALS14 Hex Inverters with Schmitt Trigger Inputs

General Description

This device contains six independent gates, each of which performs the logic INVERT function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter-free output.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and low power Schottky TTL counterparts
- Improved AC performance over Schottky and low power Schottky counterparts

Absolute Maximum Ratings (Note 1)

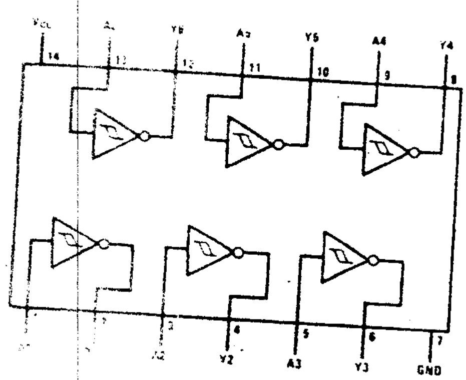
Supply Voltage	7V
Input Voltage	7V
Storage Temperature	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

2

Connection Diagram

Dual-In-Line Package



TL/F/6183-1

DM54ALS14 (J) **DM74ALS14 (N)**

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = high logic level
L = low logic level

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Recommended Operating Conditions

Symbol	Parameter	DM54ALS14			DM74ALS14			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 1)	1.4		2	1.4		2	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 1)	0.7		1.2	0.8		1.2	V
Hys	Input Hysteresis (Note 1)	0.5			0.5			V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	$V_{CC}-2$	3.4		V
			DM74	$V_{CC}-2$	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	V
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, $V_I = V_{T+}$			0.03		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, $V_I = V_{T-}$			0.034		mA
I_I	Input Current at Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max				12	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max				12	mA

Note 1: V_{CC} = 5V

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	DM54ALS14			DM74ALS14			Units
			Min	Typ (Note 3)	Max	Min	Typ (Note 3)	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 2kΩ, C_L = 50 pF		8			8		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output			8			8		ns

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C

DM54ALS14

4ALS14

Recommended Operating Conditions

Symbol	Parameter	DM54ALS13			DM74ALS13			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 1)	1.4		2	1.4		2	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 1)	0.7		1.2	0.8		1.2	V
Hys	Input Hysteresis (Note 1)	0.5			0.5			V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, $V_I = V_{T-Min}$	DM54	$V_{CC}-2$	3.4		V
			DM74	$V_{CC}-2$	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, $V_I = V_{T+Max}$	DM54		0.25	0.4	V
			DM74		0.35	0.5	V
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, $V_I = V_{T+}$			0.03		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, $V_I = V_{T-}$			0.034		mA
I_I	Input Current at Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max				4	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max				4	mA

Switching Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	DM54ALS13			DM74ALS13			Units
			Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 2 kΩ, C_L = 50 pF		8			8		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output			13			13		ns

Note 1: V_{CC} = 5V

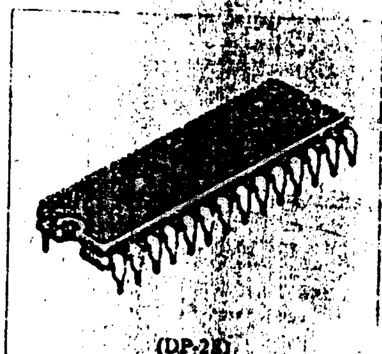
Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

HM6264LP-10, HM6264LP-12, HM6264LP-15

8192-word x 8-bit High Speed Static CMOS RAM

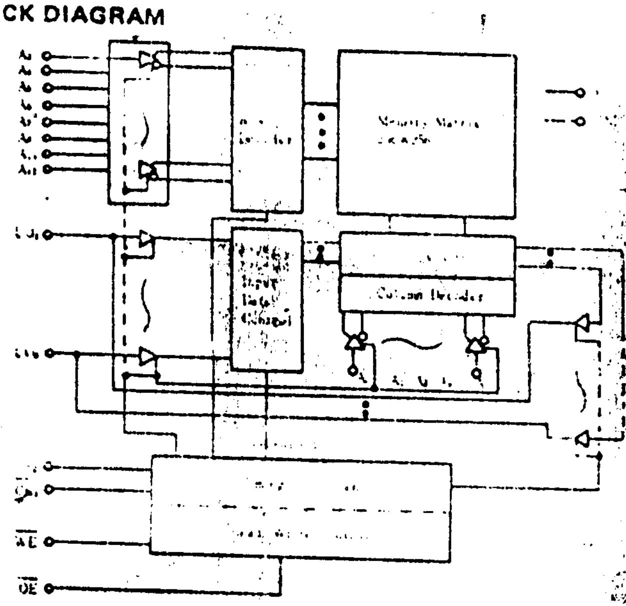
■ FEATURES

- Fast access Time — 100ns/120ns/150ns (max.)
- Low Power Standby — Standby: 0.01mW (typ.)
  Low Power Operation — Operating: 200mW (typ.)
- Capability of Battery Back-up Operation
- Single +5V Supply
- Completely Static Memory..... No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output
- Standard 28pin Package Configuration
- Pin Out Compatible with 64K EPROM HN482764

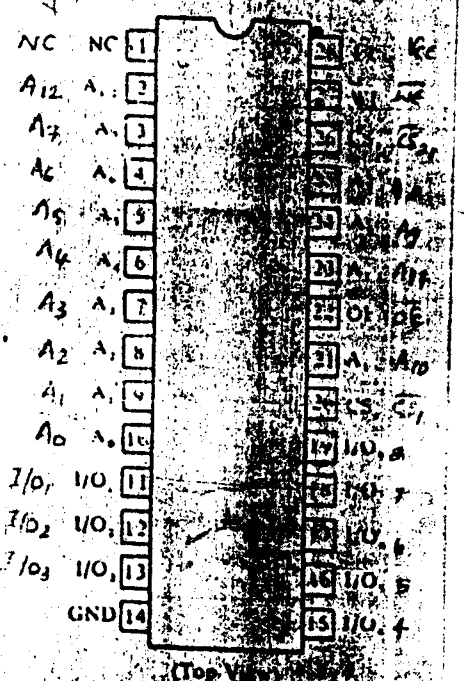


(DP-28)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage *	V_T	−0.5 ** to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	−10 to +85	°C

* With respect to GND. ** Pulse width 50ns: −3.0V

■ TRUTH TABLE

$\overline{WE}$	$\overline{CS}_1$	CS_2	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current	
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB}, I_{SB1}	
X	X	L	X		High Z	I_{SB}, I_{SB2}	
H	L	H	H	Output Disabled	High Z	I_{CC}, I_{CC1}	
H	L	H	L	Read	Dout	I_{CC}, I_{CC1}	
L	L	H	H	Write	Din	I_{CC}, I_{CC1}	Write Cycle (1)
	L	H	L		Din	I_{CC}, I_{CC1}	Write Cycle (2)

X: H or L

OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

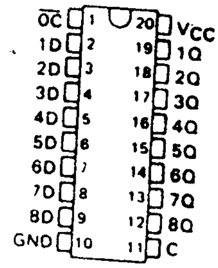
D2661, DECEMBER 1982 – REVISED DECEMBER 1983

- 3-State Buffer-Type Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- Choice of True or Inverting Logic

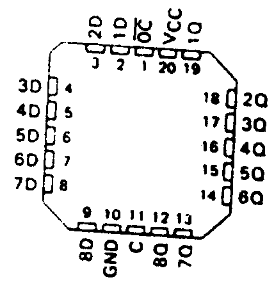
'ALS573, 'AS573	True Outputs
'ALS580, 'AS580	Inverting Outputs

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

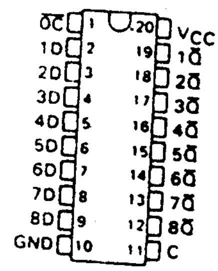
SN54ALS573, SN54AS573 . . . J PACKAGE
SN74ALS573, SN74AS573 . . . N PACKAGE
(TOP VIEW)



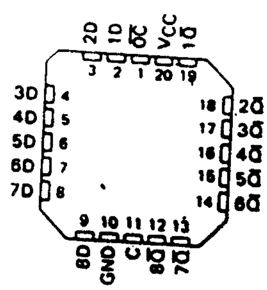
SN54ALS573, SN54AS573 . . . FH PACKAGE
SN74ALS573, SN74AS573 . . . FN PACKAGE
(TOP VIEW)



SN54ALS580, SN54AS580 . . . J PACKAGE
SN74ALS580, SN74AS580 . . . N PACKAGE
(TOP VIEW)



SN54ALS580, SN54AS580 . . . FH PACKAGE
SN74ALS580, SN74AS580 . . . FN PACKAGE
(TOP VIEW)



description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type latches. While the enable (C) is high the outputs (Q or $\overline{Q}$) will respond to the data (D) inputs. When the enable is taken low the outputs will be latched to retain the data that was set up.

A buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control ($\overline{OC}$) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are at high impedance.

The SN54ALS573, SN54AS573, SN54ALS580 and SN54AS580 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS573, SN74AS573, SN74ALS580, and SN74AS580 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLES

'ALS573, 'AS573
(EACH LATCH)

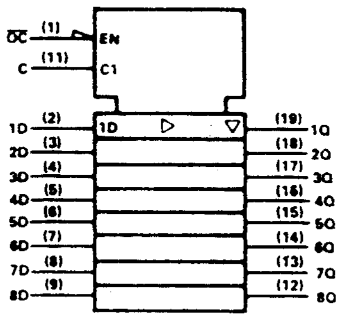
INPUTS			OUTPUT
ENABLE			Q
$\overline{OC}$	C	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

'ALS580, 'AS580
(EACH LATCH)

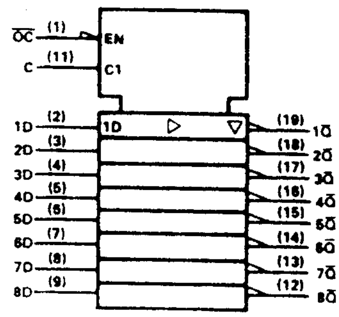
INPUTS			OUTPUT
ENABLE			$\overline{Q}$
$\overline{OC}$	C	D	
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

logic symbols

'ALS573, 'AS573

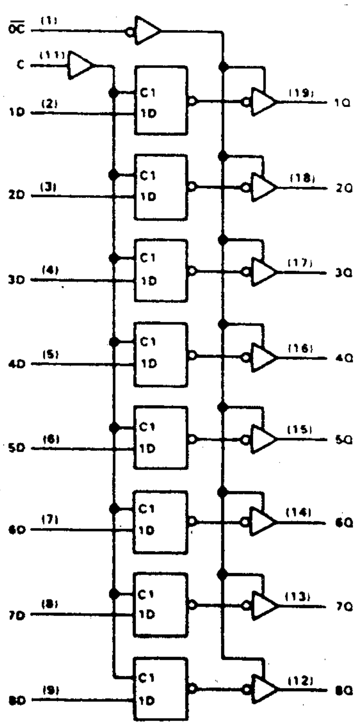


'ALS580, 'AS580

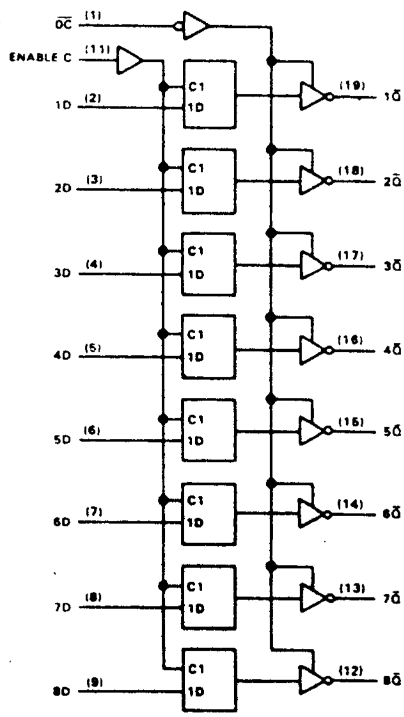


logic diagram (positive logic)

'ALS573, 'AS573



'ALS580, 'AS580



Pin numbers shown are for J and N packages.

...olute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} .... 7 V
Input voltage .... 7 V
Voltage applied to a disabled 3-state output .... 5.5 V
Operating free-air temperature range: SN54AS573, SN54AS580 .... −55 °C to 125 °C
SN74AS573, SN74AS580 .... 0 °C to 70 °C
Storage temperature range .... −65 °C to 150 °C

...mmended operating conditions

		SN54AS573 SN54AS580 MIN	NOM	MAX	SN74AS573 SN74AS580 MIN	NOM	MAX	UNIT
Supply voltage		4.5	5	5.5	4.5	5	5.5	V
High-level input voltage		2			2			V
Low level input voltage				0.8			0.8	V
High-level output current				−12			−15	mA
Low-level output current				32			48	mA
Pulse duration, enable C high	'AS573	5.5			4.5			ns
	'AS580	3			2			
Setup time, data before enable C↑		2			2			ns
Hold time, data after enable C↑		3			3			ns
Operating free-air temperature		−55		125	0		70	°C

...ical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS573 SN54AS580 MIN	TYP†	MAX	SN74AS573 SN74AS580 MIN	TYP†	MAX	UNIT
	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.28	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.33	0.5	
	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	µA
	V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	µA
	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
AS573	V_{CC} = 5.5 V	Outputs high		56	93		56	93	mA
		Outputs low		55	90		55	90	
		Outputs disabled		65	106		65	106	
AS580		Outputs high		62	100		62	100	
		Outputs low		65	106		65	106	
		Outputs disabled		71	115		71	115	

...al values are at V_{CC} = 5 V, T_A = 25 °C.
...put conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

ALS AND AS CIRCUITS

'ALS573 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS573		SN74ALS573		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	2	15	2	14	ns
t_{PHL}			2	15	2	14	
t_{PLH}	C	Q	8	27	8	20	ns
t_{PHL}			8	20	8	19	
t_{PZH}	$\overline{OC}$	Q	4	21	4	18	ns
t_{PZL}			4	21	4	18	
t_{PHZ}	$\overline{OC}$	Q	2	10	2	8	ns
t_{PLZ}			3	15	3	13	

'ALS580 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS580		SN74ALS580		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$	3	21	3	18	ns
t_{PHL}			3	15	3	14	
t_{PLH}	C	$\overline{Q}$	8	29	8	22	ns
t_{PHL}			8	22	8	21	
t_{PZH}	$\overline{OC}$	$\overline{Q}$	4	21	4	18	ns
t_{PZL}			4	21	4	18	
t_{PHZ}	$\overline{OC}$	$\overline{Q}$	2	10	2	8	ns
t_{PLZ}			3	15	3	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . 7 V
Input voltage . . . . 7 V
Voltage applied to a disabled 3-state output . . . . 5.5 V
Operating free-air temperature range: SN54ALS573, SN54ALS580 . . . . −55 °C to 125 °C
SN74ALS573, SN74ALS580 . . . . 0 °C to 70 °C
Storage temperature range . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS573 SN54ALS580			SN74ALS573 SN74ALS580			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Pulse duration, enable C high	'ALS573	10			10			ns
		'ALS580	15			15			
t_{su}	Setup time, data before enable C↓		10			10			ns
t_h	Hold time, data after enable C↓	'ALS573	7			7			ns
		'ALS580	10			10			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS573 SN54ALS580			SN74ALS573 SN74ALS580			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V,			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	'ALS573	V_{CC} = 5.5 V	Outputs high		10	17		10	17	mA
			Outputs low		15	24		15	24	
			Outputs disabled		16	27		16	27	
	'ALS580		Outputs high		10	17		10	17	
			Outputs low		15	24		15	24	
			Outputs disabled		16	27		16	27	

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

2 ALS AND AS CIRCUITS

'AS573 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS573		SN74AS573		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	3	9	3	6	
t_{PHL}			3	7	3	6	ns
t_{PLH}	C	Q	6	14	6	11.5	
t_{PHL}			4	9	4	7.5	ns
t_{PZH}	$\overline{OC}$	Q	2	8	2	6.5	
t_{PZL}			4	11	4	9.5	ns
t_{PHZ}	$\overline{OC}$	Q	2	8	2	6.5	
t_{PLZ}			2	8	2	7	ns

'AS580 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS580		SN74AS580		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$	3	10	3	7.5	
t_{PHL}			3	7.5	3	7	ns
t_{PLH}	C	$\overline{Q}$	5	12	5	9	
t_{PHL}			4	8.5	4	8	ns
t_{PZH}	$\overline{OC}$	$\overline{Q}$	2	7.5	2	6.5	
t_{PZL}			4	10.5	4	9.5	ns
t_{PHZ}	$\overline{OC}$	$\overline{Q}$	2	7.5	2	6.5	
t_{PLZ}			2	8	2	7	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS05A . . . . . −55 °C to 125 °C
SN74ALS05A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS05A			SN74ALS05A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS05A			SN74ALS05A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.65	1.1		0.65	1.1	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.9	4.2		2.9	4.2	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			SN54ALS05A		SN74ALS05A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	23	59	23	54	ns
t_{PHL}	A or B	Y	4	19	4	14	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

		SN54AS137			SN74AS137			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
t_w	Pulse duration, $\overline{GL}$ low							ns
t_{su}	Setup times at A, B, and C before $\overline{GL}$↑							ns
t_h	Hold time at A, B, and C after $\overline{GL}$↑							ns
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS137			SN74AS137			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} −2			V_{CC} −2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	Enable	V_{CC} = 5.5 V,	V_I = 7 V							mA
	A, B, C									
I_{IH}	Enable	V_{CC} = 5.5 V,	V_I = 2.7 V							μA
	A, B, C									
I_{IL}	Enable	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.05			−0.05		mA
	A, B, C				−0.05			−0.05		
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			16			16		mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS137			SN74AS137			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A, B, C	Y		6.6			6.6		ns
t_{PHL}				7.1			7.1		
t_{PLH}	$\overline{G2}$	Y		5.4			5.4		ns
t_{PHL}				5.3			5.3		
t_{PLH}	G1	Y		6.2			6.2		ns
t_{PHL}				5.6			5.6		
t_{PLH}	$\overline{GL}$	Y		5.4			5.4		ns
t_{PHL}				5.3			5.3		

† All typical values are at V_{CC} 5 V, T_A = 25°C
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

2

ALS AND AS CIRCUITS

PRODUCT PREVIEW

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

		SN54AS137			SN74AS137			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-2			-2	mA
I_{OL}	Low-level output current			20			20	mA
t_w	Pulse duration, $\overline{GL}$ low							ns
t_{su}	Setup times at A, B, and C before $\overline{GL}$↑							ns
t_h	Hold time at A, B, and C after $\overline{GL}$↑							ns
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS137			SN74AS137			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = -18 mA			-1.2			-1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = -2 mA	V_{CC} - 2			V_{CC} - 2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	Enable	V_{CC} = 5.5 V,	V_I = 7 V							mA
	A, B, C									
I_{IH}	Enable	V_{CC} = 5.5 V,	V_I = 2.7 V							μA
	A, B, C									
I_{IL}	Enable	V_{CC} = 5.5 V,	V_I = 0.4 V		0.05			-0.05		mA
	A, B, C				0.05			-0.05		
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	-30		-112	-30		-112	mA
I_{CC}		V_{CC} = 5.5 V			16			16		mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS137			SN74AS137			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A, B, C	Y		6.6			6.6		ns
t_{PHL}				7.1			7.1		
t_{PLH}	$\overline{G2}$	Y		5.4			5.4		ns
t_{PHL}				5.3			5.3		
t_{PLH}	G1	Y		6.2			6.2		ns
t_{PHL}				5.6			5.6		
t_{PLH}	$\overline{GL}$	Y		5.4			5.4		ns
t_{PHL}				5.3			5.3		

† All typical values are at V_{CC} = 5 V, T_A = 25°C
NOTE 1: For load circuit and voltage waveforms, see page 1-12

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

BIBLIOGRAPHY

BIBLIOGRAPHY

1. Dr. P.N.DAS, "An Introduction to automatic telephony", Modern book Agency Private Ltd., 1991.

2. DAVID BELL, "Electronic Devices and Circuits", Prentice - Hall International Editions, 1990.

3. Telecommunications Magazine, March, 1976.

4. WILLIAM SINNEMA, "Digital, Analog and Data Communication", Restron publishing company, Prentice-Hall Company, Restron, Virginia.

5. Electronics for you, Journal, April, 1990.

6. Electro Electronics India, Journal, October, 1990.

7. PRI 51 Manual.