Eight Channel Digital Voice Communication Through Fiber and Software for Link Simulation

P-1297

Project Report

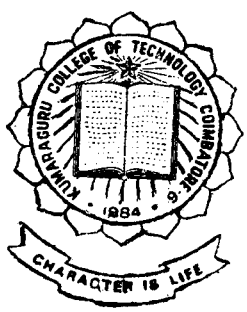
Submitted by

Apu John Joseph
George. N. Eldo
Muthumanickam .C
Padmakumar .K

Under the Guidance of

Prof. K. Palaniswami, ME,MIEEE,MIE,MISTE,MCSI,FIETE,
Head of the Department, Dept. of ECE.

Submitted in partial fulfilment of the requirements for the award of the degree of
BACHELOR OF ENGINEERING
in Electronics and Communication Engineering
of the Bharathiar University



1994

Department of Electronics and Communication Engineering

Kumaraguru College of Technology

Coimbatore - 641 006

Department of Electronics and Communication Engineering

Kumaraguru College of Technology

(Affiliated to Bharathiar University)

Coimbatore - 641 006

CERTIFICATE

This is to certify that the project report entitled

EIGHT CHANNEL DIGITAL VOICE COMMUNICATION THROUGH FIBER AND SOFTWARE FOR LINK SIMULATION

is bonafide work done by

APU JOHN JOSEPH

GEORGE .N. ELDO

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During the academic year 1994

.....
Faculty Guide

.....
Head of the Department

Certified that the Candidate was examined by us in the Project - Work.

Viva-Voce Examination held on.....
and the University Register Number was .....

.....
Internal Examiner

.....
External Examiner

DEDICATED TO OUR
BELOVED PARENTS

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ACKNOWLEDGEMENT

ACKNOWLEDGEMENT

First of all we wish to thank our Principal PROF.S.SUBRAMANIAN for his support and encouragement for completion of this project.

With due resects, we wish to thank our guide and Head Of The Department PROF.K.PALANISWAMI ME,MIEEE,MIE,MISTE,MCSI,FIETE for his valuable guidance and facilities provided for the successful completion of the project.

We are very grateful to PROF.P.SHANMUGAM for his keen interest and untiring efforts towards the completion of the project.

We would like to thank all the faculty members of the ECE department who had lent their helping hands for the completion of this project. We also thank the lab technicians for their kind co-operation.

SYNOPSIS

SYNOPSIS

An eight channel fiber optic digital audio link operating at a bit rate of 512KHz has been designed and implemented in this project and also we have developed a software for fiber optic link simulation.

The system uses LED(HFBR 1402) of 850nm wavelength as the light source, and PIN diode(HFBR 2402) as the detector. The voice signals are multiplexed using an analog multiplexer and is fed to an A/D converter for digitisation. The output of the A/D converter is manchester coded and this signal intensity modulates the light source. the optical signal is sent through the fiber and detected at the other end using the PIN diode. It is then decoded, demodulated, demultiplexed and fed to the loudspeaker for voice reproduction.

A software for fiber optic link simulation has also been developed in this project. This software helps the designer to select the LED, detector and to design the system using them. The variables related to the fiber, LED and detector are stored in an array. The software does both power budget analysis and rise time budget analysis. It outputs whether repeaters are required or not and how many numbers are required. It also specifies whether communication is possible in NRZ format or not.

CHAPTER I

INTRODUCTION

CHAPTER 1

INTRODUCTION

Many forms of communication systems have appeared over the years. The principal motivations were to improve the transmission fidelity, to increase the data rate and to increase the transmission distance. Data is usually transferred over the communication channel by superimposing the information signal on to a sinusoidally varying electromagnetic wave which is known as the carrier. At the destination the information is removed from the carrier and then processed to get back the original signal. Since the amount of information that can be transmitted is directly related to the frequency range over which the carrier operates, the need to go to the optical frequencies were imparative as the frequencies were of the order of 5×10^{14} Hz. Thus the information capacity of optical systems exceeded the microwave systems by a factor of 10^{5} which has led to the developement of economically feasible optical fiber. Communication systems that can carry live telephone, cable TV and other types of telecommunication traffic.

1.1 PRINCIPLE OF OPERATION OF FIBER OPTIC SYSTEMS

The key sections of a optical fiber transmission link are a transmitter consisting of the light source and its associated drive circuitry, a optical cable containing several hair thin glass fibers and a receiver

consisting of a photodetector plus amplification and signal restoring circuitry. (Fig.1.1) A light source either LED or LASER diodes, which is dimensionally compatible with the optical fiber is used to launch optical power into the fiber. An optical source is a square law device. i.e. a linear variation in drive current results in a corresponding linear change in optical power output.

At the receiver, the attenuated and distorted modulated optical power emerging from the fiber end will be detected by a Photodetector which can be PIN or APD depending on the application. The principle figure of merit for a receiver is the minimum optical power necessary to maintain a given error probability for digital systems or a specified S/N ratio for an analog system. The optical signal thus received is converted to its electrial form, the detector also being a square law device.

1.2 BASICS OF OPTICS

The working of optical fibers depend on basic principles of optics and the interaction of light with matter. From physical stand point, light can be seen either as electromagnetic waves or as photons,quanta of electromagnetic energy. Both view points are valid, but the most useful view point for optics often is to consider light rays travelling in straight lines between optical elements, which can reflect or refract them.

1.2.1 REFRACTIVE INDEX

The most important optical measurement for any transparent material is its refractive index (n). The refractive index is the ratio of the speed of light in vaccum to the speed of light in the medium.

$$n = Cvac/Cmat$$

1.2.2 SNELL'S LAW

Although light rays travel in straight lines through optical materials, something different happens at the surface. Light is bent as it passes through a surface where the refractive index changes. The amount of bending depends on the refractive index of the two media and the angle between them. This relation ship is known as Snell's law.

$$ni \text{ Sin } (\theta i) = nr \text{ Sin } (\theta r)$$

where,

ni and nr are refractive indices of the initial and the final medium into which light is refracted and I and R are the angles of incidence and refraction respectively. According to this law refraction cannot take place when the angle of incidence is too large i.e. if the angle of incidence exeeds a critical value, called the critical angle , where Sin r = 1 (i.e r = 90^{o}). At this angle of incidence light undegoes total internal reflection. It is this phenmenon that keeps light confined in optical fiber. The critical angle decided by SNELL'S law is given as

$$\text{critical angle} = \text{arc Sin}(nr/ni).$$

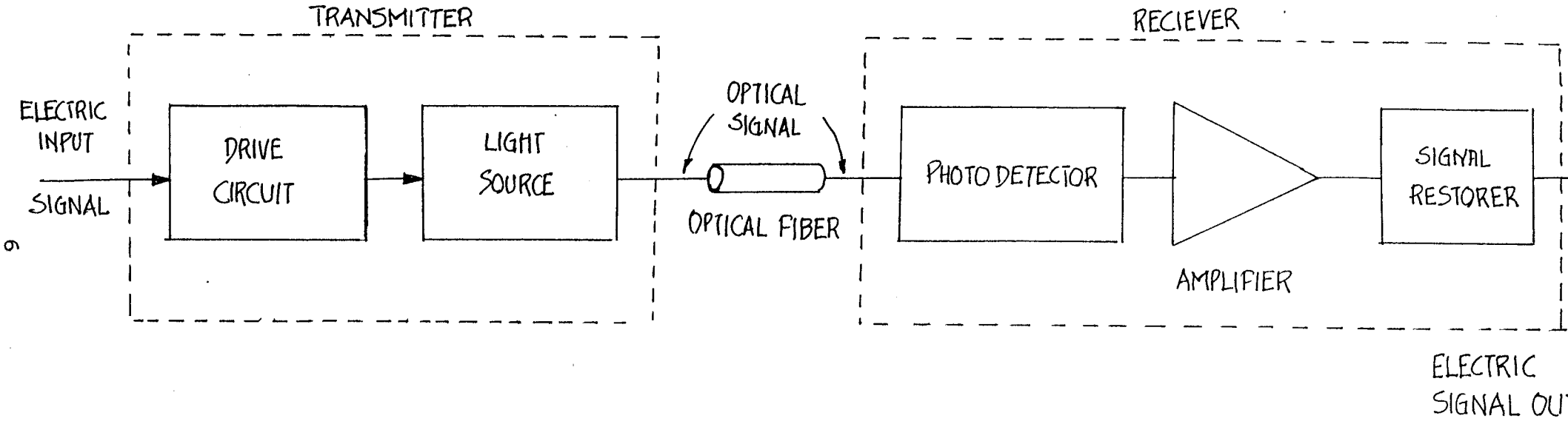


Fig 1.1. BASIC ELEMENTS OF AN OPTICAL FIBER TRANSMISSION LINK.

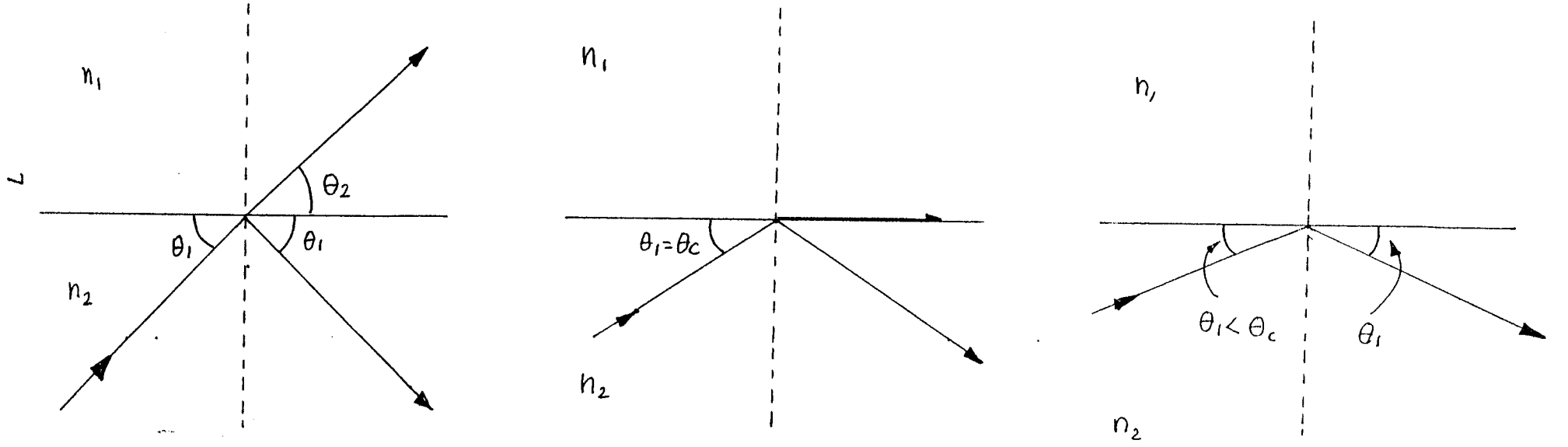


Fig. 1.2. REPRESENTATION OF THE CRITICAL ANGLE AND TOTAL INTERNAL REFLECTION AT A GLASS-AIR INTERFACE.

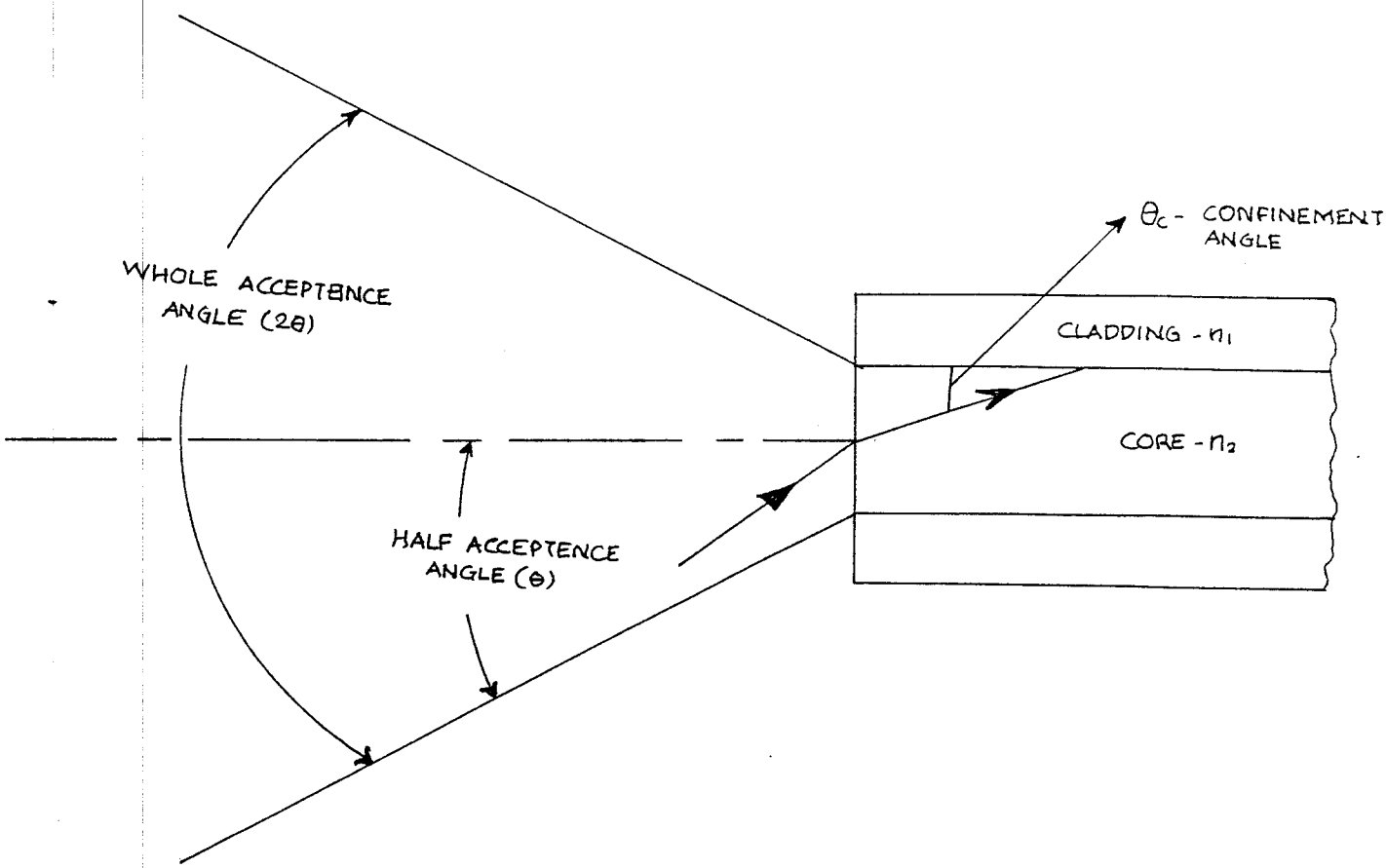


Fig. 1.3. LIGHT GUIDING IN AN OPTICAL FIBER.

CHAPTER II

ELEMENTS OF FIBER OPTICS

CHAPTER 2

ELEMENTS OF FIBER OPTICS

2.1 Introduction

The ensuring developement of fiber optical transmission systems has resulted in the implementation of a transmission link, which has inherent advantages over the conventional electrical systems in the field of telecommunications. An optic fiber transmission link comprises the basic elements,

a) a transmitter

b) optical fiber

c) a receiver

2.2 Optical fiber

The optical fiber consists of a central dielectric cylinder 'core' surrounded by another dielectric cylinder called 'cladding' (figure2.1). The refractive index of the cladding is less than that of the core. so the cladding keeps the light within the core the cladding is surrounded by a jacket which protects the fiber from moisture, abrasion and other external contamination. The fiber can be made either of glass or plastic.

2.2.1 Types of fibers

Variations in the material, composition of the core give rise to the two commonly used fiber types. The

types and their characteristics are discussed below.

a) Multimode step index fiber

b) Monomode step index fiber

c) Multimode graded index fiber

a) Multimode step index fiber

This fiber has a larger core diameter. Here the incident light takes several modes. This leads to intermodal dispersion. The numerical aperture of multimode fibers is larger than monomode fiber and hence LED's can be used as light sources to couple light into the fiber.

b) Monomode step index fiber

The refractive index of the core of the step index fiber is uniform throughout and undergoes an abrupt change or step at the cladding boundary. There is only a single mode of propagation and the core diameter is less. Hence it must be excited with laser diodes. It has a wide band width , less dispersion and low loss ; but the cost is high.

c) Multimode graded index fiber

In this fiber , the core refractive index is made to vary as a function of the radial distance from the center of the fiber. Here also there are many modes of propogation, but all the rays reach the other end at the same time. As the ray travels from the center of the core to the sides , the refractive index decreases.

As the refractive index decreases , the velocity of the wave increases and so even though the light rays take different paths , they reach the receiver at the same time. This type of fiber has small dispersion , larger band width and low loss.

The various types of fiber with their core and cladding is illustrated in figure 2.2.

2.2.2 FIBER CHARACTERISTICS

Band width

Optical fibers have a higher band width , when compared to conventional cables. The band width is inversely proportional to the length of the fiber for distances upto 1Km and is inversely proportional to the square of the length for greater distances. A band width upto 18GHz.Km is possible , but is limited by pulse dispersion.

Bidirectionality

This is accomplished by transmitting two different wavelengths simultaneously in opposite directions through one fiber.

Transmission loss or fiber loss

The attenuation of a light signal as it

propagates along the fiber is useful in determining the maximum transmission distance between repeaters and also the type of transmitter and receiver used. The basic attenuation occurs as absorption , scattering and radiative losses of energy occurs in the fiber.

Absorption is caused by three different mechanisms

1. Absorption by atomic defects in the glass composition.
2. Extrinsic absorption by impurity atoms in the glass material of the fiber.
3. Intrinsic absorption by the basic constituent atoms of the fiber material.

Scattering losses in the fibers arise from microscopic variations in the material density from compositional fluctuations and structure inhomogenities or defects occuring during fiber manufacture.

Radiative losses occur whenever an optical fiber undergoes a bend of finite radius of curvature. The bends may be microscopic or macroscopic. The attenuation specturm of a fiber is shown in figure 2.3.

Signal distortion

An optical signal may become distorted as it travels along a fiber. This distortion is a consequence of intermodal dispersion and intermodal delay effects.

Intermodal dispersion is pulse spreading that occurs within a single mode. Pulse spreading is depicted in figure 2.4 .

The two main causes of intermodal dispersion are

1. Material dispersion that arises from variation of refractive index of the core material as a function of wavelength.

2. Wavelength dispersion occurs because of variable modal propagation constant.

Pulse spreading and intersymbol interference is also due to intermodal delay which arises due to the differences in group velocities of a signal mode at each frequency. As a pulse spreads due to dispersion along the fiber , these dispersive properties determine the limit to the information capacity of an optical wave guide , usually specified by the bandwidth distance product in MHz.Km . The dispersion spectrum of the fiber is shown in figure 2.5 .

2.3 Choice of wavelength

For glass fibers , the small loss between 800 and 900 nm makes this region practial even for long distance links. This region is called first transmission window. In the range 1300 to 1600 nm , glass losses are lower. This region is divided into two parts by the OH absorption peak that occurs just below 1400 nm. In this range we have the second transmission window around 1550 nm. The total chromatic dispersion of a single mode step index fiber is zero at 1300 nm and hence

useful for long distance transmission. The total attenuation is around 0.4 - 0.5 db/Km at 1300 nm and it is much lower at 0.16 db/Km at 1500 nm. Hence for long distance transmission higher bandwidth fibers are used. The plastic clad silica fibers generally have more attenuation than glass fibers. Operation on these fibers is possible in the infrared and in the visible spectrum over moderate path lengths. Losses for all plastic fiber are quite high. Only short transmission paths are possible with these fibers. The performance characteristics of commercial fibers is shown in **table 2.1.**

2.4 Optical sources

An optical source converts the input electrical signal to changes in light if the drive current varies accordingly. An optical source is square law device as a linear change in drive current results in corresponding linear change in the optical output power. The principal light source used are heterojunction structure semiconductor laser diodes and light emitting diodes.

2.4.1 Light emitting diodes

To be useful in fiber transmission application a light emitting diode(LED) must have a high radiance output , a fast emission response time and a high quantum efficiency. To achieve this , the configuration most widely used is a double-heterostructure device.

The two basic LED configurations are surface emitters and edge emitters. Their structures are shown in figure 2.6. In the surface emitter the plane of the active light emitting region is oriented perpendicular to the axis of the fiber. The edge emitter is source of incoherent light and two guiding layers. This structure forms a wave guide channel that directs the optional radiation towards the fiber.

2.4.2 Laser diode

For optical fiber systems the laser sources used exclusively are semiconductor laser diodes shown in figure 2.7 . The output radiation is highly monochromatic and the light beam is very directional. The lasing action is a result of photon absorption , spontaneous emission and stimulated emission. For high speed long distance communications , single mode lasers are used whose spectral density of the optical emission is very narrow. The basic limitation on the modulation rate of laser diodes depends on the carrier and photon lifetime parameters associated with the operation of laser.

2.4.3 Comparison

The spatially directed coherent optical output from a laser diode can be coupled into either single mode or multimode fibers where as LED's are used with multimode fibers.

For bit rates less than 100-200 Mbits/sec LED's are usually the best light source choice as it requires less complex drive circuitry than laser. For bit rates higher than 200 Mbits/sec laser diode is prefered, which has response time less than 1 ns. They have optical bandwidths of 2 nm or less and in general are capable of coupling several milliwatts of power into small core. the typical characteristics of diode light source is shown in table 2.2 .

2.5 Optical detectors

At the receiver , the light energy is converted into electrical energy which is then amplified and processed to recover the original information. This is done by light sensors like PIN photo diodes and avalanche photo diodes (APD). The photo detector converts the received optical power directly to electrical current output and makes it suitable for processing.

2.5.1 PIN photodiode

The most common semiconductor is the PIN photo diode shown in figure 2.8. This operates under reverse bias condition. When light energy falls on the surface of the diode it penetrates the N layer and is absorbed exponentially through the PN device. As the photons are absorbed , electron-hole pairs are generated. Thus the resulting current flow due to the recombination of

electrons and holes is known as photo current .

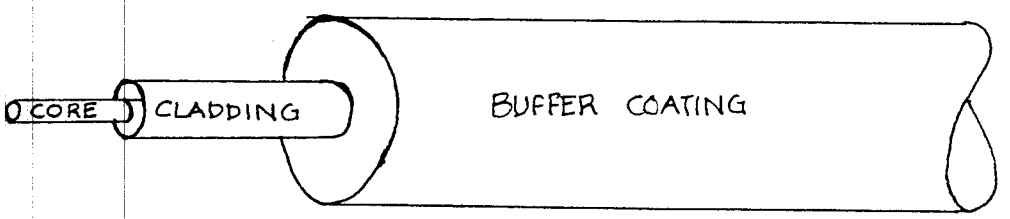
The two important characteristics of the photo diode are the quantum efficiency and responsivity which depend on the material band gap and operating wavelength , the doping and the thickness of the P , I and N region.

2.5.2 Avalanche photo diode

Avalanche photo diode multiply the primary photo current internally due to impact ionisation which results in increased photo sensitivity. It needs a high reverse bias voltage. Electrons released by the photons bombard the nearby atom to release more electrons. This is known as avalanche mechanism. The reach through construction is the commonly used structure and carrier multiplication is achieved with very little noise (fig 2.9).

2.5.3 Comparison

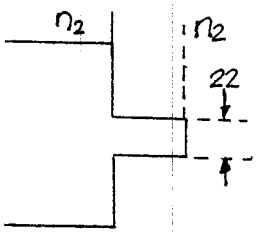
A PIN photo diode receiver is simpler , more stable with changes in temperature and also it is less expensive than an APD receiver. In addition , PIN photo diode bias voltage are normally less than 50 volts , whereas those of APD are several hundred volts. If low optical power levels are to be detected , then APD's are used because of their higher sensitivity. The typical characteristics of junction photo detectors is shown in table 2.3 .

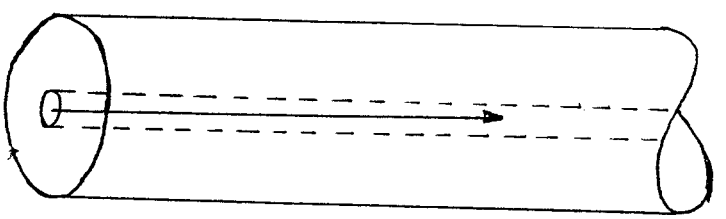


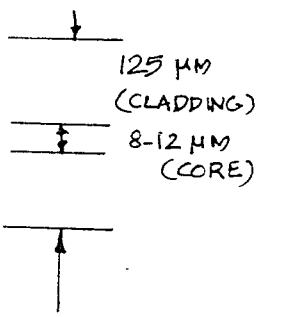
FIBER CROSS SECTION AND RAY PATHS

DEX PROFILE

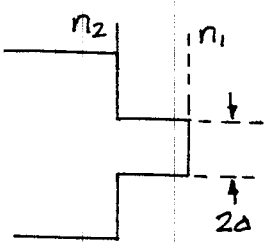
TYPICAL DIMENSION

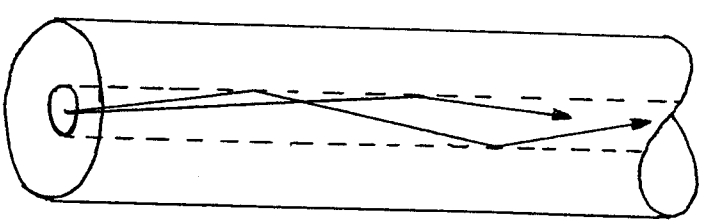


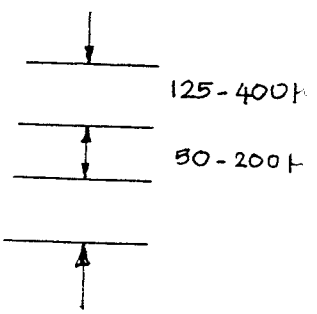




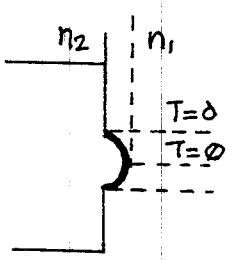
MONOMODE STEP-INDEX FIBER

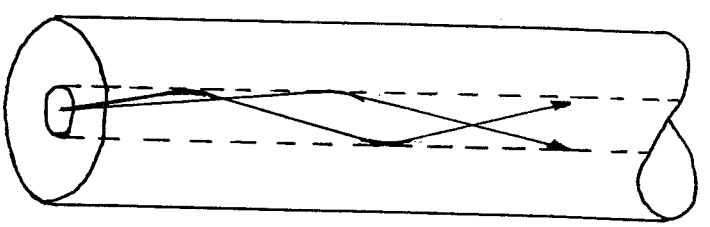


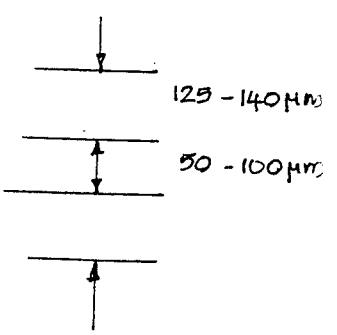




MULTIMODE STEP-INDEX FIBER

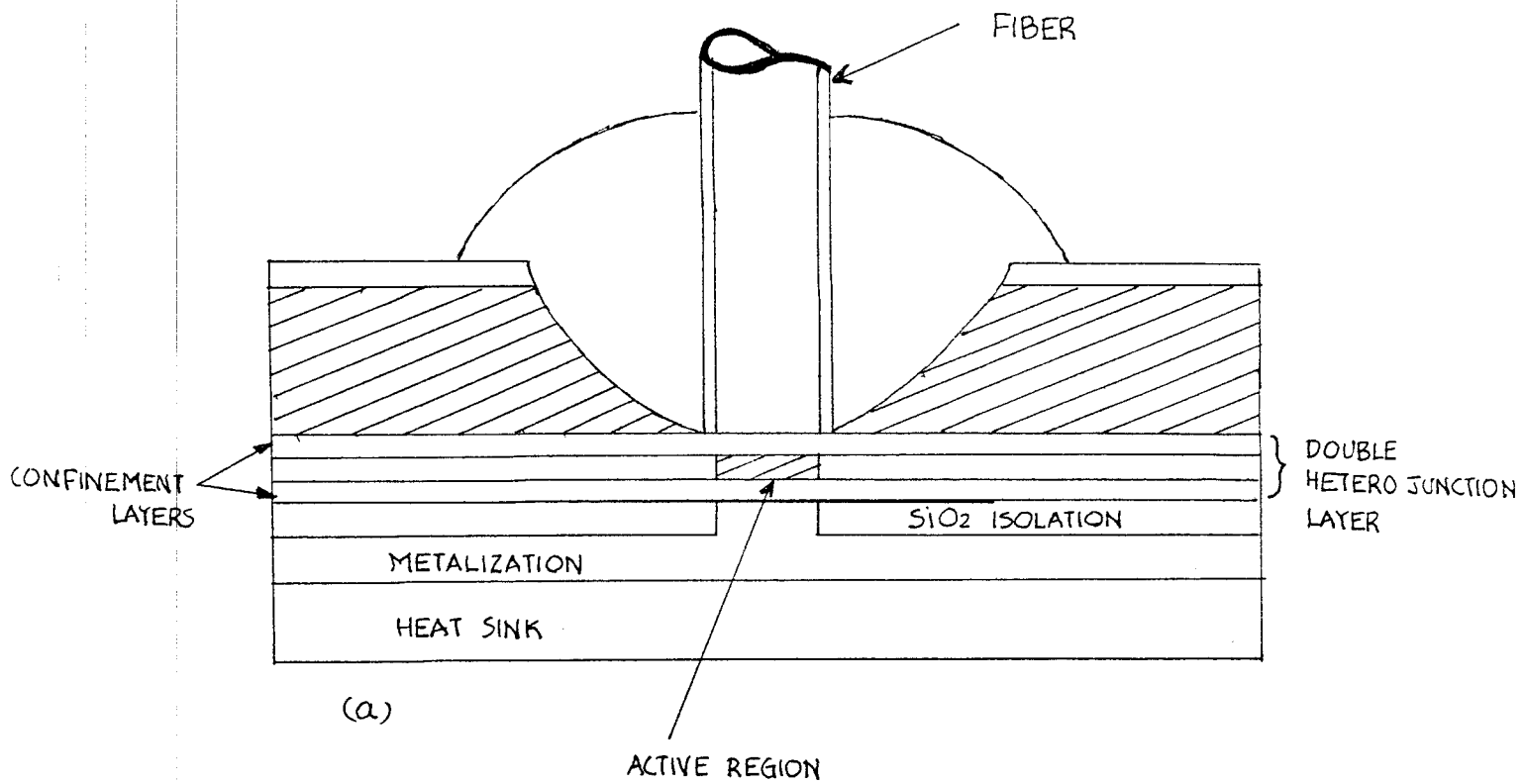






MULTI MODE GRADED INDEX FIBER

Fig. 2.1 FIBER CONFIGURATION AND TYPES



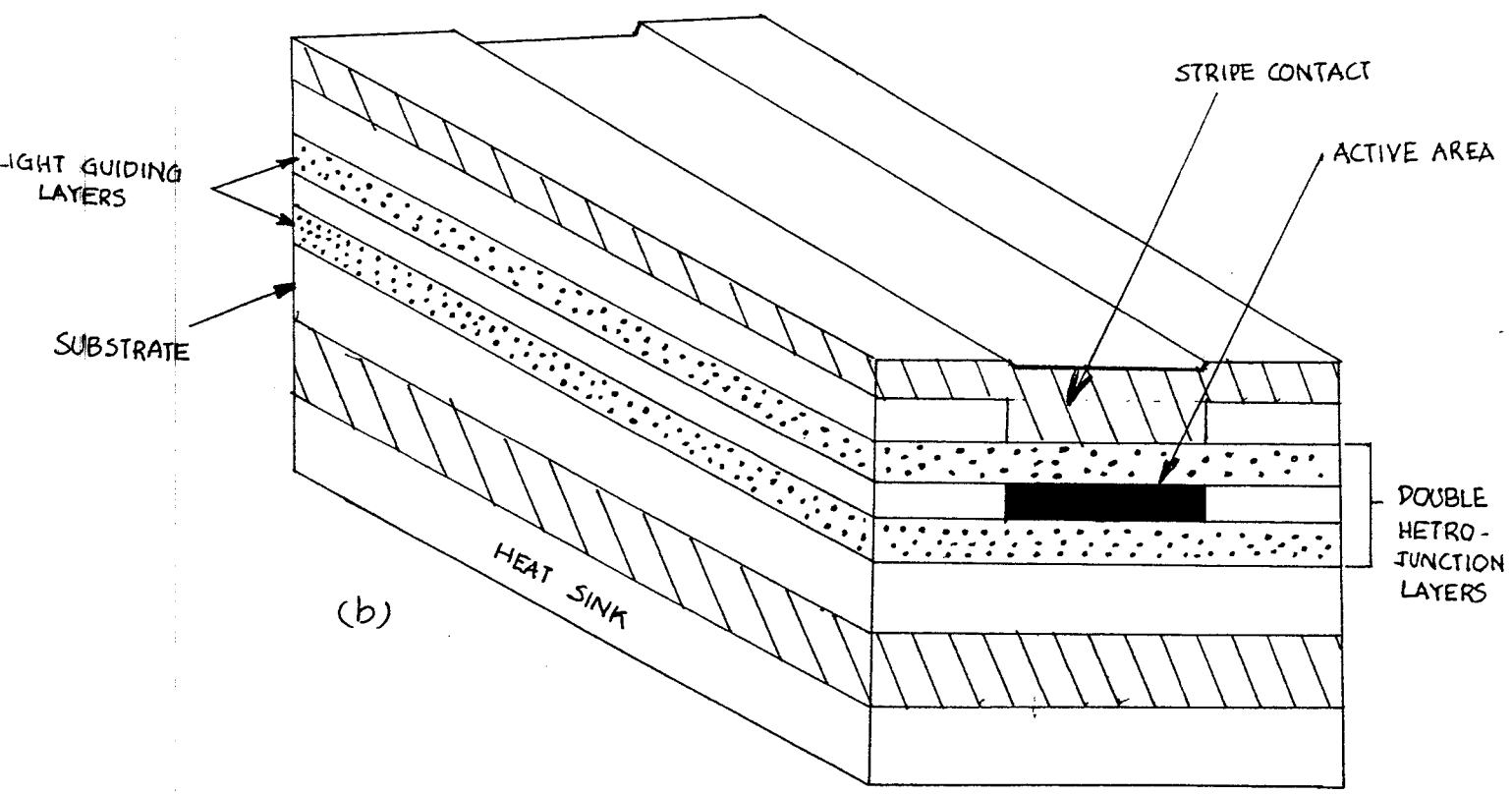


Fig. 2.6(a). SURFACE EMITTING LED

Fig 2.6(b) EDGE EMITTING LED

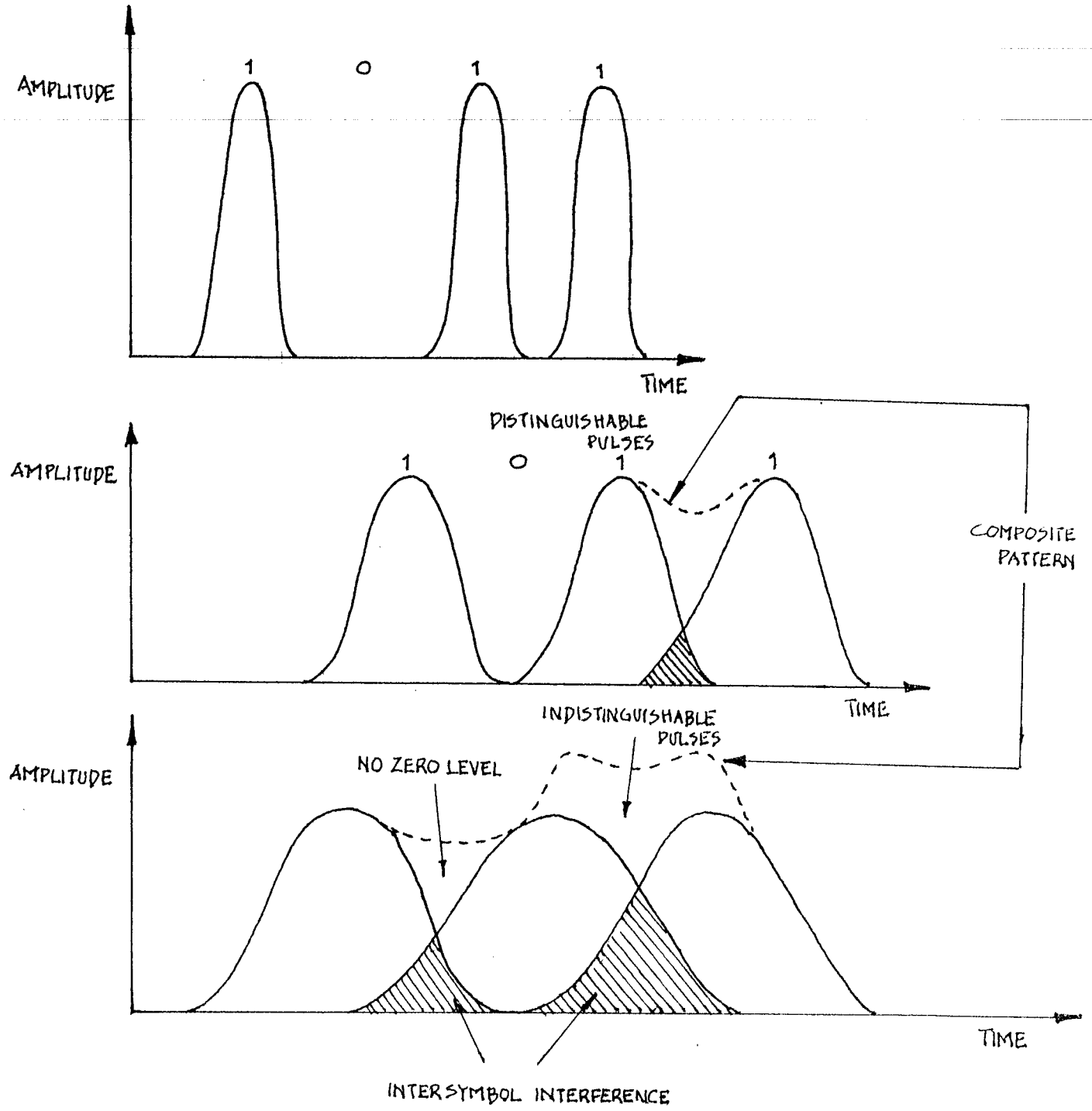


Fig 2.4. PULSE SPREADING IN OPTIC FIBER

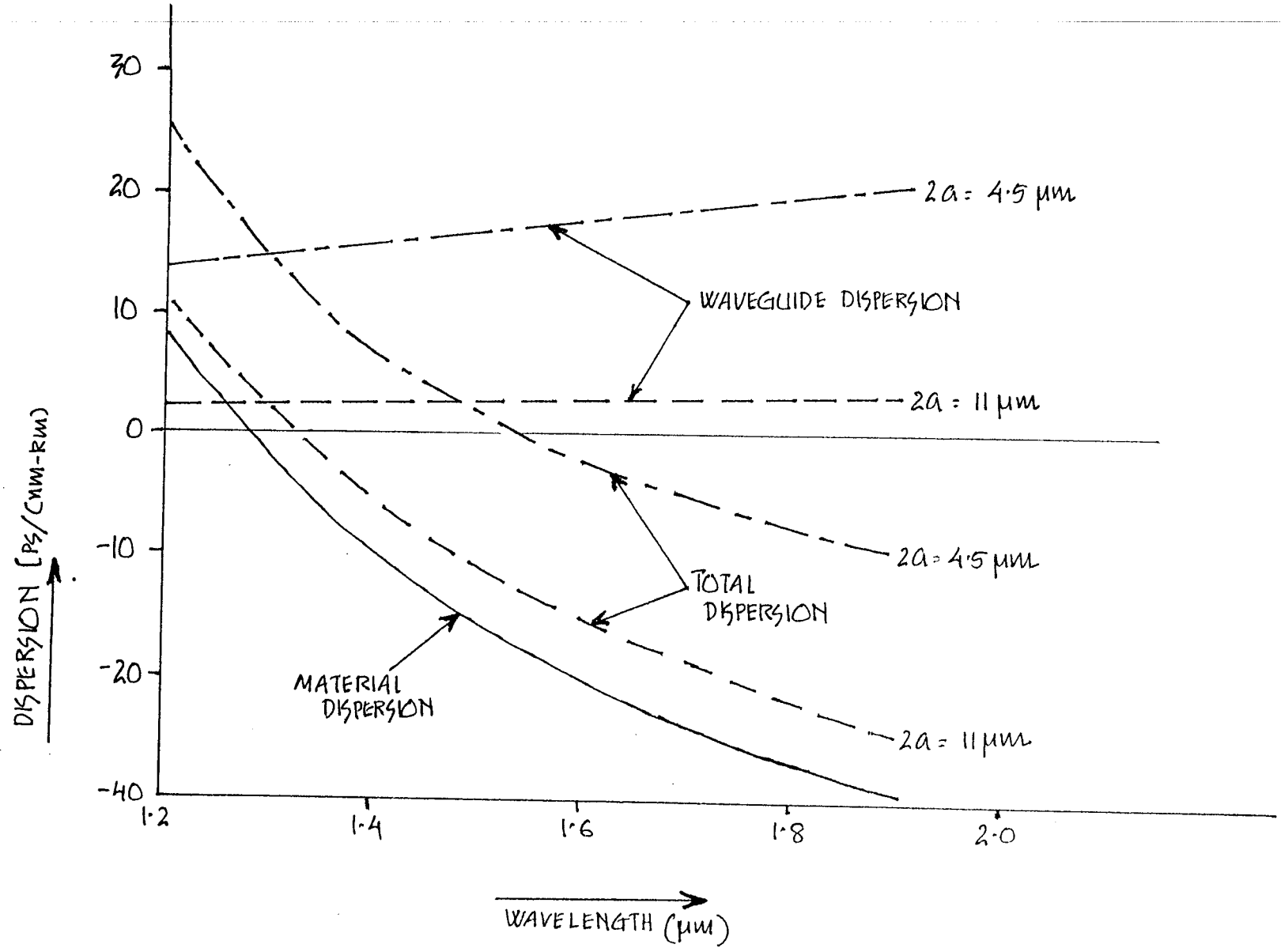


Fig 2.5: DISPERSION CHARACTERISTICS OF A SINGLE-MODE FIBER.

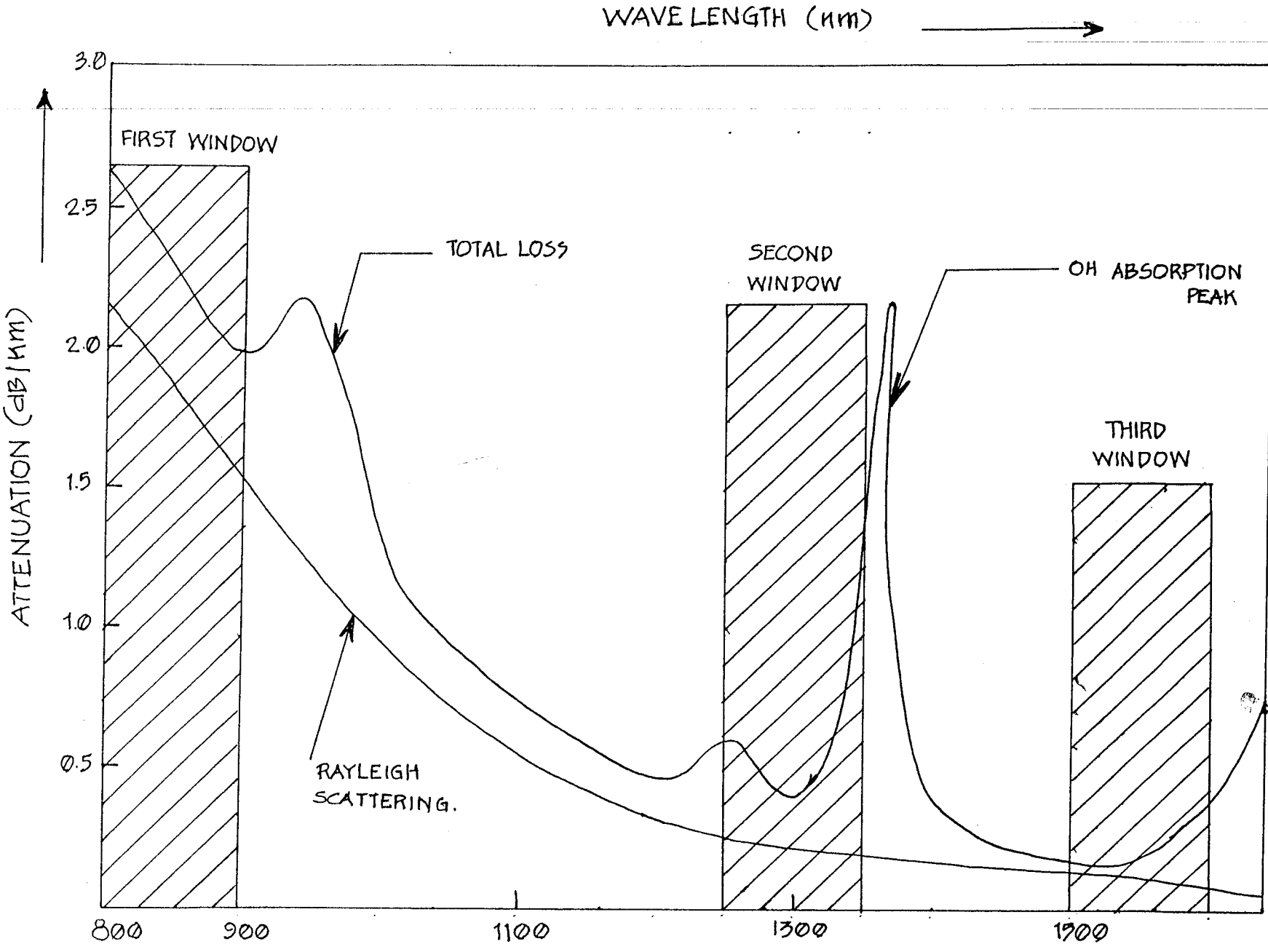


Fig. 2.2. ATTENUATION SPECTRUM.

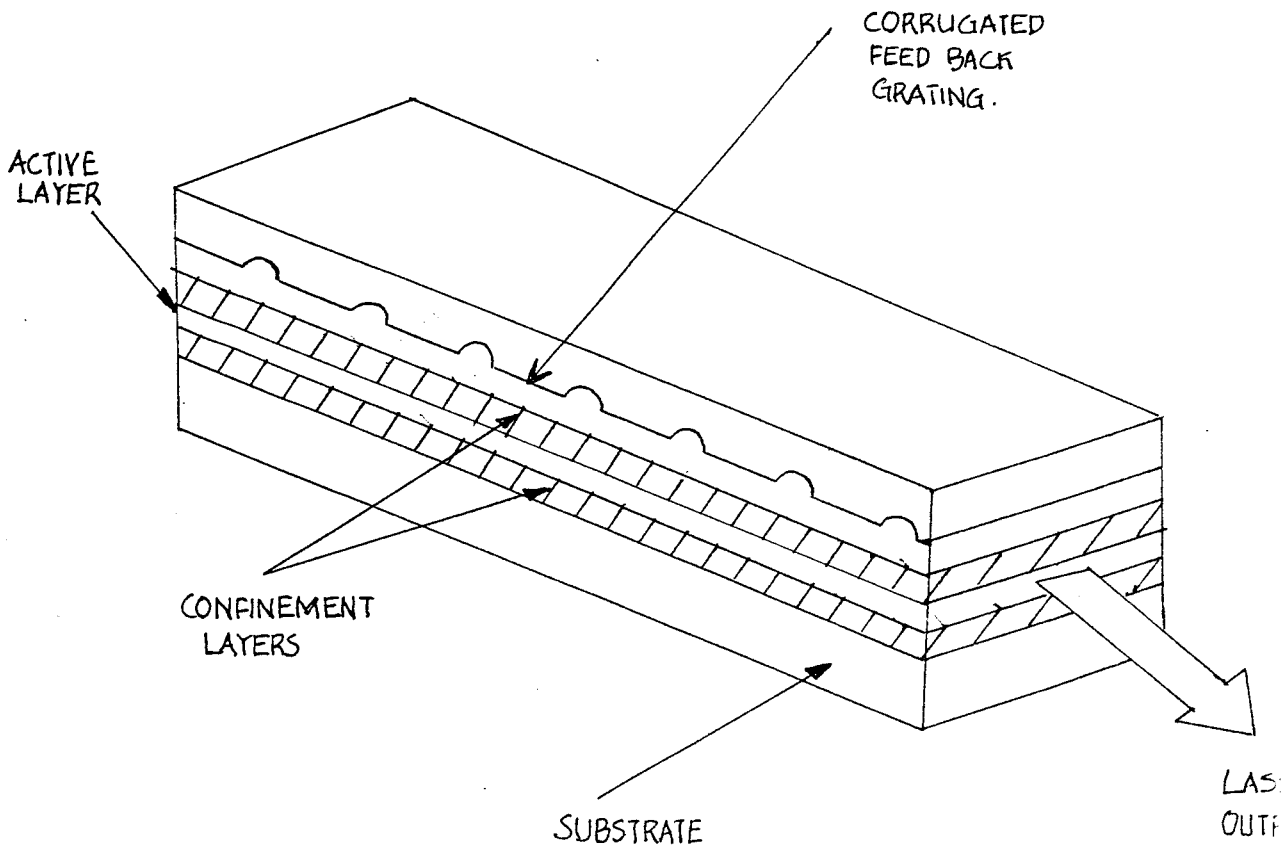


Fig. 2.7 LASER DIODE

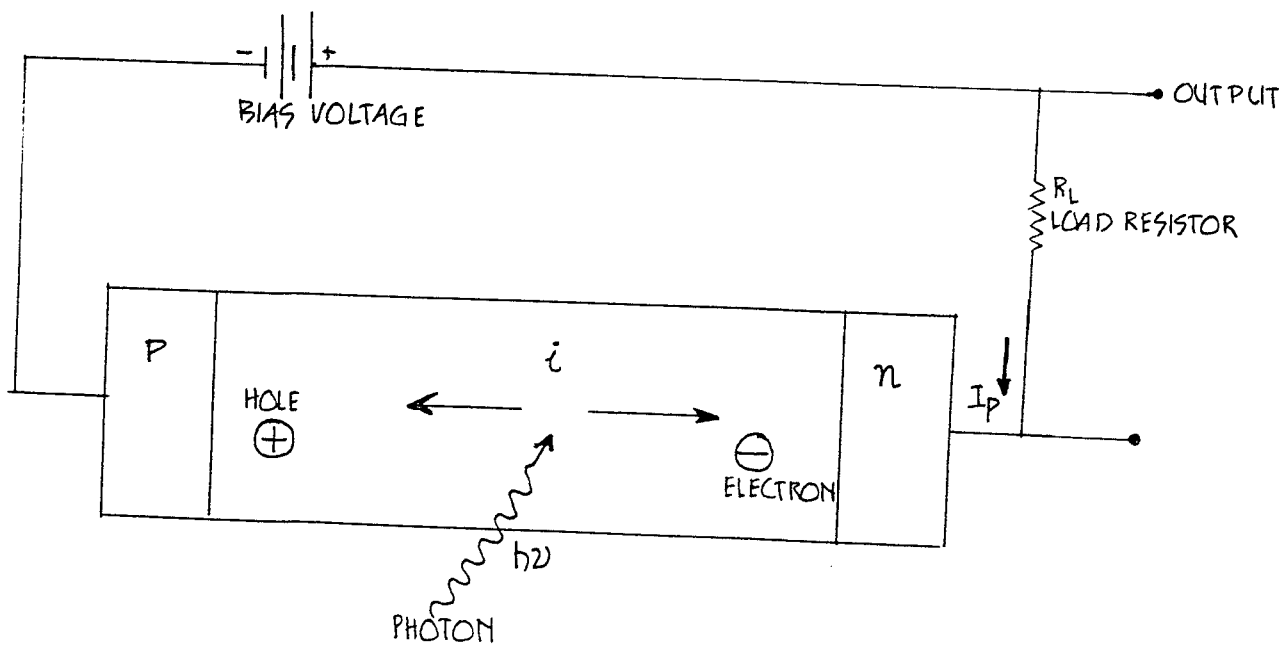


Fig 2.8. PIN DIODE

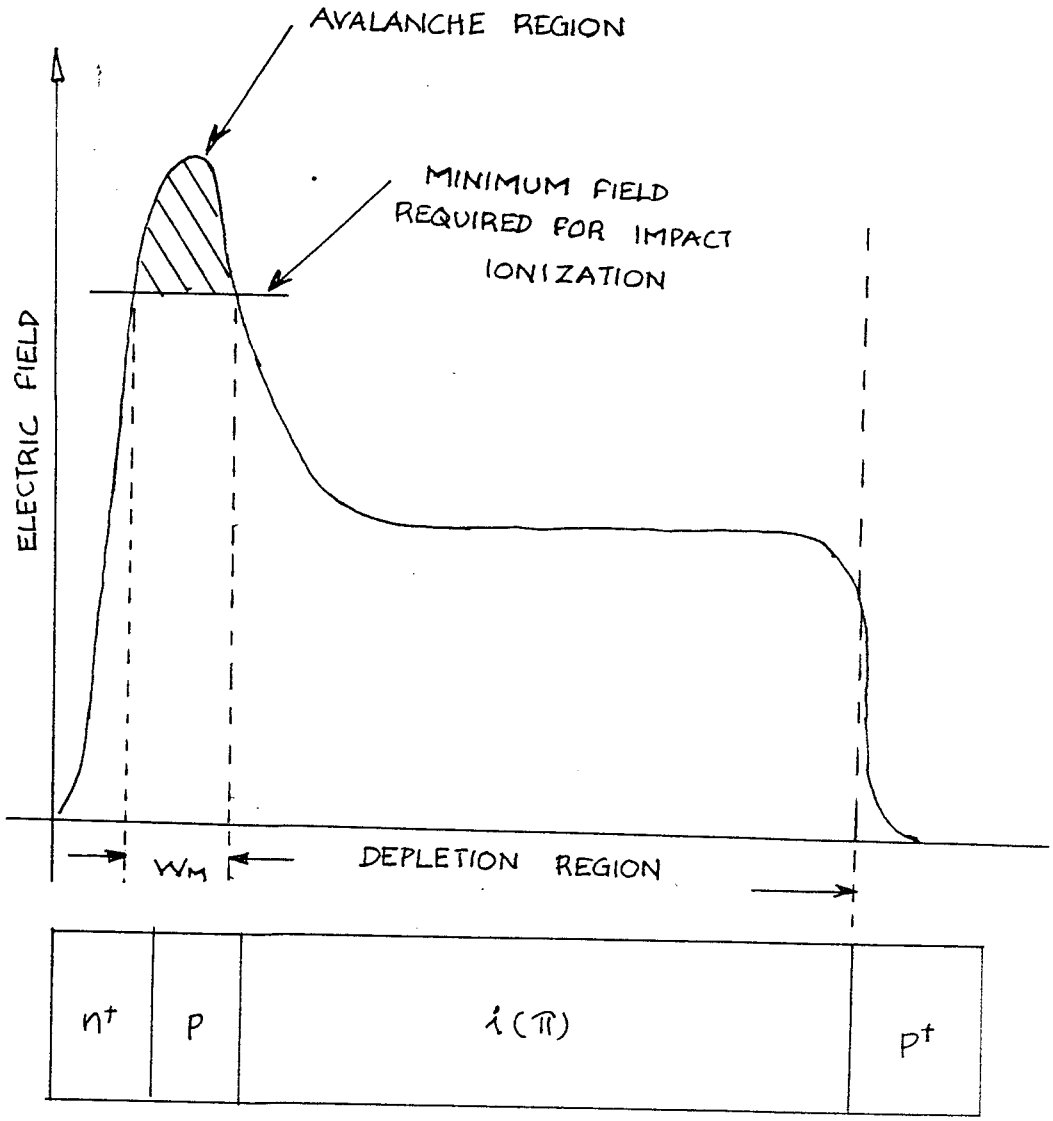


Fig. 2.8. REACH THROUGH STRUCTURE AND CARRIER MULTIPLICATION

TABLE 2.1 REPRESENTATIVE CHARACTERISTICS OF COMMERCIAL FIBRE

DESCRIPTION	CORE DIA (MIC.)	NA	LOSS (db/km)	(T/L) (ns/km)	$F_{3db}{}^{xL}$ (MHz x km)	SOURCE	WAVELENGTH (nm)
MULTI MODE							
GLASS							
SI	50	0.24	5	15	33	LED	850
GRIN	50	0.224	5	1	500	LD	850
GRIN	50	0.20	1	0.5	1000	LED, LD	1300
PCS							
SI	200	0.41	8	50	10	LED	800
PLASTIC	1000	0.48	200	-	-	LED	580
SI							
SINGLE MODE							
GLASS	5	0.1	4	0.5	1000	LD	850
GLASS	10	0.1	0.5	0.006	83000	LD	1300
GLASS	10	0.1	0.2	0.006	83000	LD	1550

TABLE 2.2 TYPICAL CHARACTERISTICS OF DIODE LIGHT SOURCES

PROPERTY	LED	LASER DIODE	SINGLE MODE LASER DIODE
SPECTRAL WIDTH (nm)	20-100	1-5	0.2
RISE TIME (nm)	2-250	0.1-1	0.05-1
MODULATION BANDWIDTH	300	2000	6000
COUPLING EFFICIENCY	VERY LOW	MODERATE	HIGH
COMPATIBLE FIBER	MULTIMODE SI MULTIMODE GRIN	MULTIMODEGRIN SINGLE MODE	SINGLE MODE
TEMPERATURE SENSITIVITY	LOW	HIGH	HIGH
CIRCUIT COMPLEXITY	SIMPLE	COMPLEX	COMPLEX
LIFE TIME (HOURS)	10^5	$10^4 - 10^5$	$10^4 - 10^5$
COSTS	LOW	HIGH	VERY HIGH
APPLICATIONS	MODERATE PATHS MODERATE DATA RATES	LONG PATHS HIGH DATA RATES	VERY LONG PATHS VERY HIGH RATES

TABLE 2.3 TYPICAL CHARACTERISTICS OF JUNCTION PHOTO DETECTORS:

MATERIAL	STRUCTURE	RISE TIME (ns)	WAVELENGTH (nm)	RESPONSIVITY (A/W)	PARK CURRENT (na)	GAIN (dB)
SILICON	PIN	0.5	300-1100	0.5	1	1
GERMANIUM	PIN	0.1	500-1800	0.7	200	1
In Ga As	PIN	0.3	900-1700	0.6	10	1
SILICON	APD	0.5	400-1000	75	15	150
GERMANIUM	APD	1	1000-1600	35	700	50
In Ga As	APD	0.25	1000-1700	12	100	20

CHAPTER III

ADVANTAGES OF DIGITAL TRANSMISSION SYSTEM

CHAPTER 3

ADVANTAGES OF DIGITAL TRANSMISSION SYSTEMS

3.1 Introduction

In this chapter first we deal with the advantages of digital voice transmission and then about the advantages and drawbacks of digital communication systems in general.

3.2 Advantages of Digital Transmission

In analog voice transmission, the effect of noise and interference is most apparent during speech pauses when the signal amplitude is nearely zero. Even relatively low noise levels can be quite annoying to a listner during speech pauses. The same levels of noise may be unnoticeable when speech is present hence, it is the absolute noise level of an idle channel that determines the analog speech quality.

Digital Speech transmission overcomes many of the problems faced in the analog systems. In a digital system, speech and speech pauses are encoded with data pattern and transmitted at a constant power level. Signal regeneration at regular interval bringing the signal to the original level virtually eliminating all noise due to the transmission medium. Thus, the idle channel noise is determined by the encoding process and not by the transmission link in digital systems.

The ability of digital transmission to reject crosstalk is superior to that of an analog system. First, low level crosstalks are eliminated because of the constant amplitude signals. Second, high amplitude crosstalks result in detection errors and such are unintelligible. Intelligible crosstalks that occur in analog systems are particularly undesirable since it violates privacy.

Other advantages of digital transmission systems include the ability to support non - voice services, easy data encryption and performance monitoring. The signal structure in a digital system is independent of the nature of the traffic and therefore the quality of the received signal can be accertained with our knowledge of the traffic type.

Some advantages of digital communication systems are given below.

1. Errors often can often corrected.
2. Signal manipulation (eg. encryption) is simple to perform.
3. Greater dynamic range (difference between largest and smallest value) is often possible

We may now expand these advantages. The major advantage of digital communication lies in its error correcting capability. This concept is critical. As long as possible signal waveforms are not being

transmitted, the receiver can often recognise when an error has ben made. Sometimes this recognition is enough, but often the error is also corrected automatically at the receiver.

Fig 3.1 Contrasts an analog communication system to a digital system. Note that in the analog system, amplifiers appear along the transmission path. Each amplifier introduces gain, but it amplifies both the signal and any additive noise that exists along the transmission path. The lower part of Fig 3.1 shows the digital communication system. Note that the amplifiers of the analog system has been replaced by regenerative repeaters. The repeaters not only perform the function of amplification but also "clean up" the signal. The input signal can take on only one of the two possible values, zeros or ones. Then, the repeater must only decide which of these two values is present in any particular interval, then reproduce that exact value for transmission over the next log of the channel.

The second advantage of digital communication relates to the fact that we are dealing with numbers rather than waveforms. These numbers can be manipulated by microprocessors. Complex operations can be easily performed in order to accomplish signal - processing functions or security in transmission. Comparable analog operations would require complex hardware.

The third advantage relates to dynamic range. This can be illustrated with an example. Traditional analog

phonograph disc recording suffers from limited dynamic range. Very loud sounds require extreme variations in the shape of the groove on a record, and it is difficult for the needle to follow the variations. Digital recording do not suffer from this problem, since all amplitude values, whether very small or very large, are transmitted using the same limited set of signals.

3.3 Disadvantages Of Digital Communication

All is not ideal. There are disadvantages to digital communication when compared to analog communication. They are,

1. It generally requires more bandwidth than analog.
2. Synchronisation is required.

Digital systems generally require more bandwidth than as analog systems. For example a voice channel can be transmitted using single - sideband AM with a bandwidth of less than 5KHz. Transmitting the same signal using digital techniques can require at least four times this bandwidth.

An additional disadvantage is the need to provide synchronization throughout the digital communication system. It is important for the system to know when each symbol is starting and stopping, and to properly associate each symbol with the correct transmission.

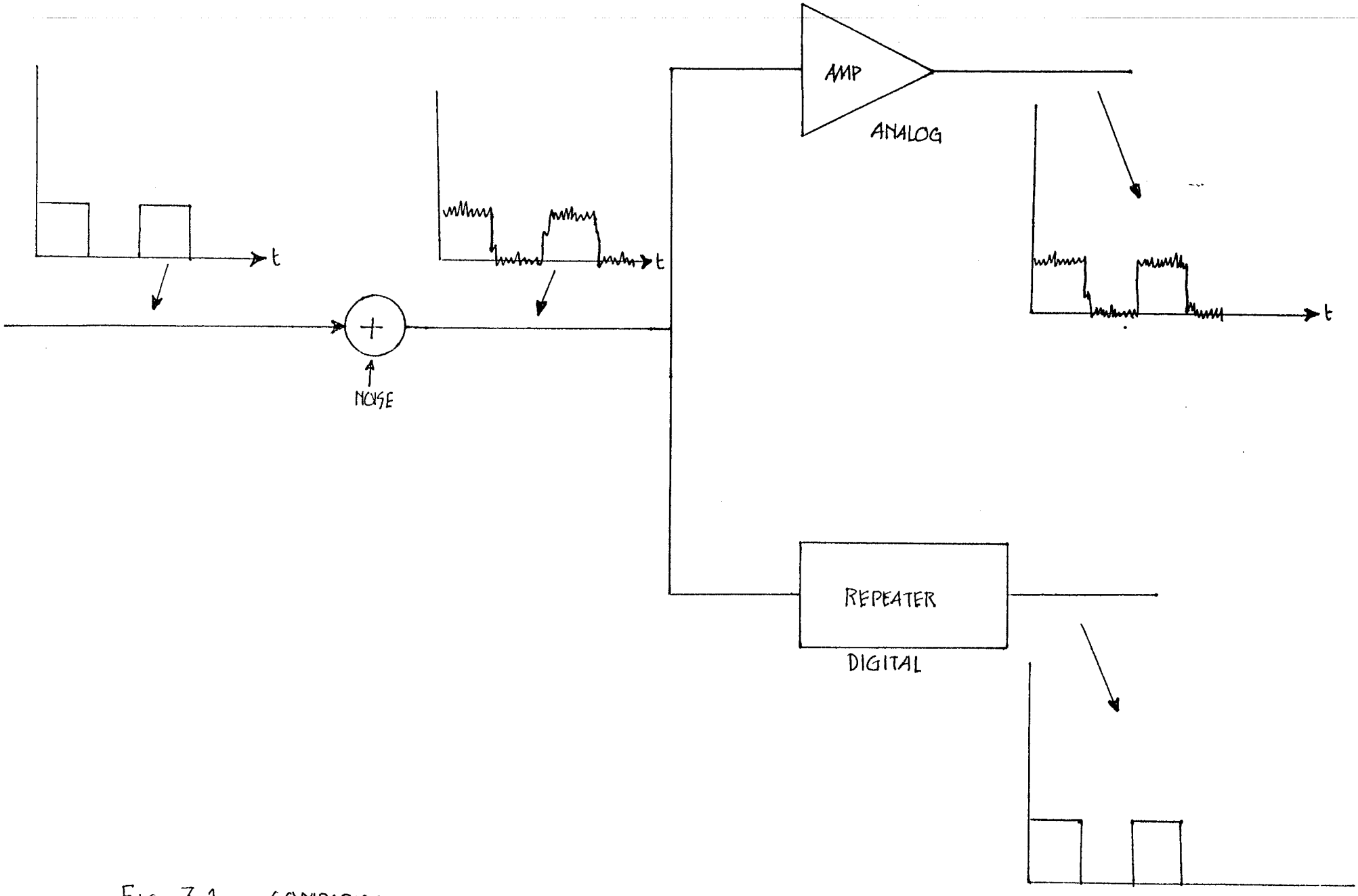


FIG 3.1 COMPARISON OF ANALOG TO DIGITAL COMMUNICATION

CHAPTER IV

DESIGN ASPECTS OF AUDIO LINK

CHAPTER 4

DESIGN ASPECTS OF DIGITAL AUDIO LINK

4.1 Introduction

The simplest transmission link is a point to point link having a transmitter on one end and receiver on the other. An optical fiber communication system is similar in basic concept to any type of communication system. A block schematic of a general communication system and that of the optical fiber communication system is given in Fig 4.1.

Here in this project we have developed an **Eight Channel Digital Audio Link** using easily available components. The audio link designed here is highly different from the system presently used by TELECOM. Economically our system is more preferable. In TELECOM they are using digital multiplexing while here we are using analog multiplexing. It gives the same quality signal which a digitally multiplexed signal provides. The main advantage is that here we have to use only one A/D converter.

The block diagram of the eight channel fibre optic digital audio link is shown in the figure.The output from the microphone is bandlimited to 4KHz. Using a low pass filter. The output of the filter are then given to an analog multiplexer.

The output of the analog multiplexer is then digitized using an A/D converter. Parallel to serial converter serialises the output of the A/D converter. The serial output is then given to the line coder. The coder data is fed to the LED driver.

The optical receiver at the end reconverts the signal back to its electrical form. Manchester decoder circuit extracts the clock from the data stream. The data ouptput is then fed to the serial to parallel converter. The parallel data output is given to the D/A converter which gives the analog output of the multiplexed audio which is given to the analog demultiplexer. The output of the demultiplexer is sharped out using a low pass filter and then fed to the loudspeaker for voice reproduction.

In this chapter the circuit details of the transmitter and receiver are discussed in detail.

4.2 Transmitter Design

Fig 4.2 shows the block schematic of the transmitter of audio fiber optic communication system.

4.2.1. Microphone

Microphone is an electro acoustic transducer used to convert acoustic energy into electrical energy. The carbon microphone is widely used for telephone and radio communication purposes. Its high electrical output, low cost and durability are of greater significance than

fidelity of response.

4.2 Filter

The human ear is capable of perceiving frequencies in the range 16Hz to 20KHz which is the audio range. Speech produces an narrow band of frequencies 100Hz to 10KHz in the audio range. If all the frequencies present in speech waveform is transmitted, the received speech is almost natural. However, the speech remains intelligible even if some upper and lower frequencies of the speech spectrum are rejected. A reduction in bandwidth is desirable as it reduces the cost of the communication systems. An acceptable level of intelligibility of speech is obtained by transmitting frequencies in the range of 300 - 3400Hz.

So here the signal from the microphone is band limited to 4KHz using a butterworth low pass filter with a cutoff frequency 4KHz. A second order butterworth filter is preferred as it provides a slope of 40db per decade. This signal is fed to the modulator for further processing.

4.2.3. Analog Multiplexer

Use of analog multiplexer reduces the cost in multichannel communication systems as we have to use only one digitizer. The IC chip used for this purpose is MC 14051B which can be used both as a multiplexer and demultiplexer. This device contains eight bidirectional analog switches each with one side connected to

independent input/output and the other side connected to a common Input/Output. With the enable input low one of the eight switches is selected by the address inputs to the chip. Four bit binary counter chip 74LS163 is used to provide the address inputs. The clock input to the counter determines the sampling rate. The sampling is done at a rate of 64KHz. This is derived from a 512KHz clock by dividing it by using a counter.

4.2.4 Analog To Digital Converter(Digitizer)

ADC 0800 is used to digitize the audio signal. It is an 8-bit monolithic A/D converter. It contains a high input impedance comparator, 256 series resistors and analog switches, control logic and output latches. Conversion is performed using a successive approximation technique where the unknown analog voltage is compared to the resistor tie points using analog switches. It can handle analog input voltages in the range +5V or -5V.

Simply tying the EOC output to the start conversion input will allow continuous conversions, but an oscillation on this line will exist during the first 4 - clock periods after EOC goes high. Adding a D flip-flop between EOC and start conversion will prevent the oscillations and will allow a stop/continuous control Via the clear input. The circuit details for the continuous operation on a A/D converter is shown in the figure. The input clock frequency to the A/D converter is 64KHz.

4.2.5 Parallel To Serial Converter

The 8-bit parallel output of the A/D converter has to be made serial for transmitting the coded data through fiber. The IC chip used for parallel to serial conversion is 74LS166 which is an 8-bit parallel load shift resister. All the inputs are buffered to lower the drive requirements to one normalized load, and input damping diodes minimizes switching transients to sampling system design. The load mode is established by the shift/load input. When high this input enables the serial data input and couples the 8-flip flops for serial shifting with each clock pulse. When low the parallel data inputs are enabled and synchronous loading occurs on the next clock pulse.

4.2.6 Line Coding

A recovery of a synchronous clock, synchronous both in terms of phase and freqency, at the receiver is a must for any synchronous digital link. A long string of zeros and ones, in lack of transitions in data could make the receiver clock lose synchronization. Line coding introduces sufficient transitions in the data for case of clock recovery. Also a certain pattern of data, like long strings of zero's and one's, would result in a strong dc component in the transmitted signal. Such a dc component is often not desirable, line coding shifts the spectrum and avoids the dc component.

Here in this project, the simplest line coding scheme is used namely manchester coding. Here each zeros is transmitted as a zero followed by a one and each one is transmitted as a one followed by a zero as shown in Fig 4.3. Thus a transmission is introduced at the middle of each data bit, which can be used to easily recover the clock at the receiver. This is realized using a D flip - flop 7474 and an X-OR gate 7486.

4.3 Receiver Design

Fig 4.7 shows the block schematic and Fig 4.5 shows the detailed circuit diagram of the audio fiber optic communication system.

4.3.1 Optical Receiver

The optical data through the fiber is coupled to the optical receiver consisting of a photodiode. The output of this optical receiver is then passed to the manchester decoder circuitry.

The HFBR 2402 fiber optic receiver incorporate a monolithic photo IC which contains a photodetector and a dc amplifier. An open collector schottky transistor on the IC provides compatibility with TTL and CMOS logic. The maximum data rate it can handle is 5Mbits/sec with a BER of 10^{-9}. The wavelength handled is 820nm.

4.3.2 Optical Transmitter

The HFBR 1402 fiber optic transmitter contains a 820nm LED. The cathode lead and three anode leads of the light emitting diode are available allowing the

drive circuit configuration shown in fig 4.6

The source is capable of operating under a BW of 5Mbits/sec. The emitter drive current from the transistor 2N2222 has to be 20mA minimum to drive the LED. 2N2222 is a high speed switching transistor and the drive circuitry has ben designed such that it accepts an input that is TTL compatible.

4.3.3 Manchester Decoder

Manchester decoder is realised using a monostable multivibrator, a flip - flop and X-OR gates. The chips used are 74221, 7474 and 7486. The clock is recovered from the data by means of the monostable multivibrator. This recovered clock is used as receiver clock. The $\overline{Q}$ output of the 7474 is the manchester decoded data which is fed to lthe demultiplexer. Decoder circuitry is shown in fig 4.4.

4.3.4 Serial To Parallel Converter

The input to D/A should be in the parallel form. The output of manchester decoder has to be made parallel by using a serial to parallel converter. The IC used for this is 74LS165.This has a serial load 8 bit shift register. The output of serial to parallel converter is applied to the D/A converter.

4.3.5 Digital To Analog Converter

DAC 0800 is used to convert the digital signal to analog. It is a monolithic 8-bit high speed current output digital to analog converter featuring typical settling times of 100ns. The noise immune inputs of the DAC0800 will accept TTL levels with the logic threshold pin, VLC pinl is grounded. Power dissipation is only 33mW with +5V or -5V supplies and is independent of the logic input states.

4.3.6 Analog Demultiplexer

MC 14051B is used as the analog demultiplexer. It is an 8 channel analog multiplexer/demultiplexer with three address inputs, an active low enable input, eight independent inputs/outputs and a common input/output. The address inputs are provided by a 4-bit binary counter 74LS163, is supplied with a clock which is desired from the main clock recovered using manchester decoder. The clock recovered using the manchester decoder is divided by "8" and is provided as the input clock to the counter.

4.3.7 Shaping Circuit

The shaping circuit used here is a low pass filter. The filter is a second order low pass butterworth filter using LM741. It has cutoff frequency of 4KHz. The output of the D/A converter has lot of ripples in the output. They have to be smoothened out to get the original analog output. This is done by the low pass butterworth filter.

4.3.8 Loudspeaker

Loudspeaker is an electro acoustic transducer that converts electrical variations to sound variations. Its impedance is 8-ohms and it gives an output of 5 watts.

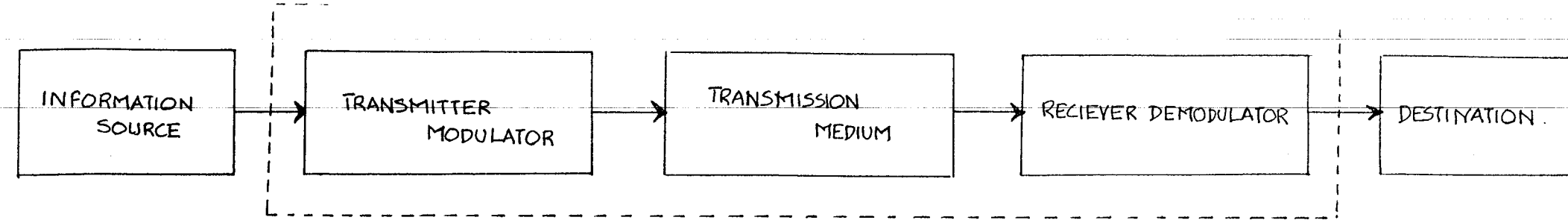


Fig 4.1. a. GENERAL COMMUNICATION SYSTEM.

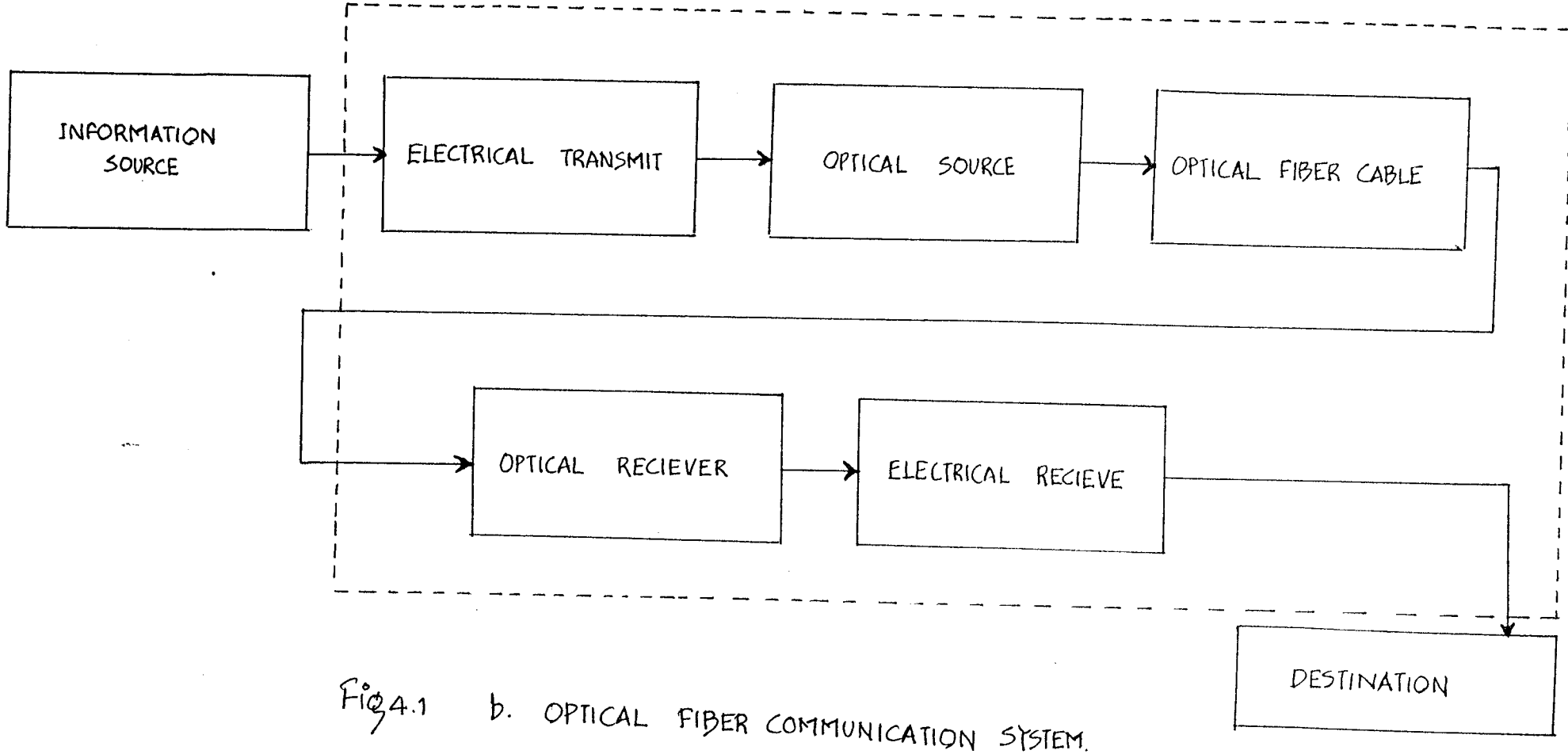


Fig 4.1 b. OPTICAL FIBER COMMUNICATION SYSTEM.

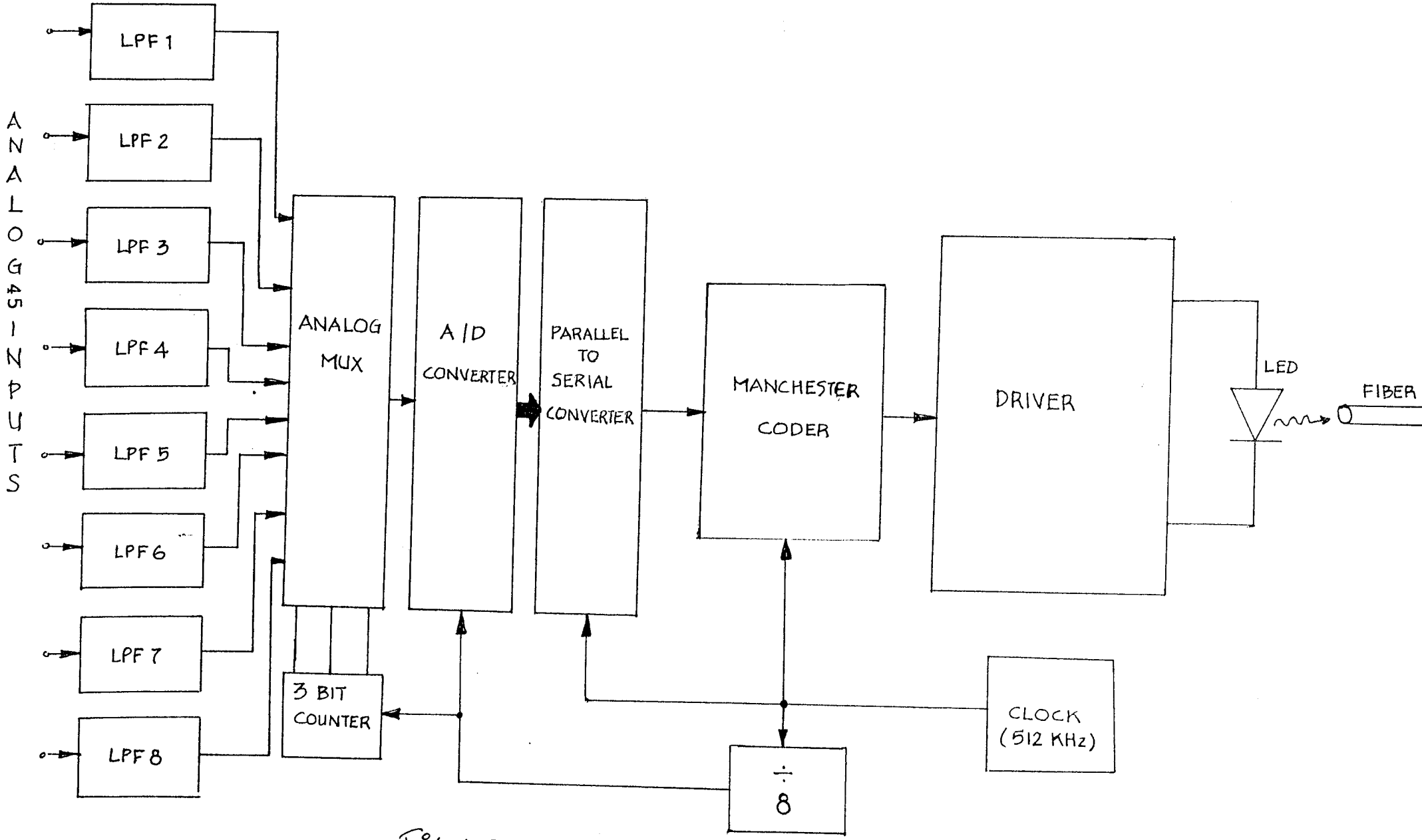


Fig 4.2. BLOCK DIAGRAM OF TRANSMITTER

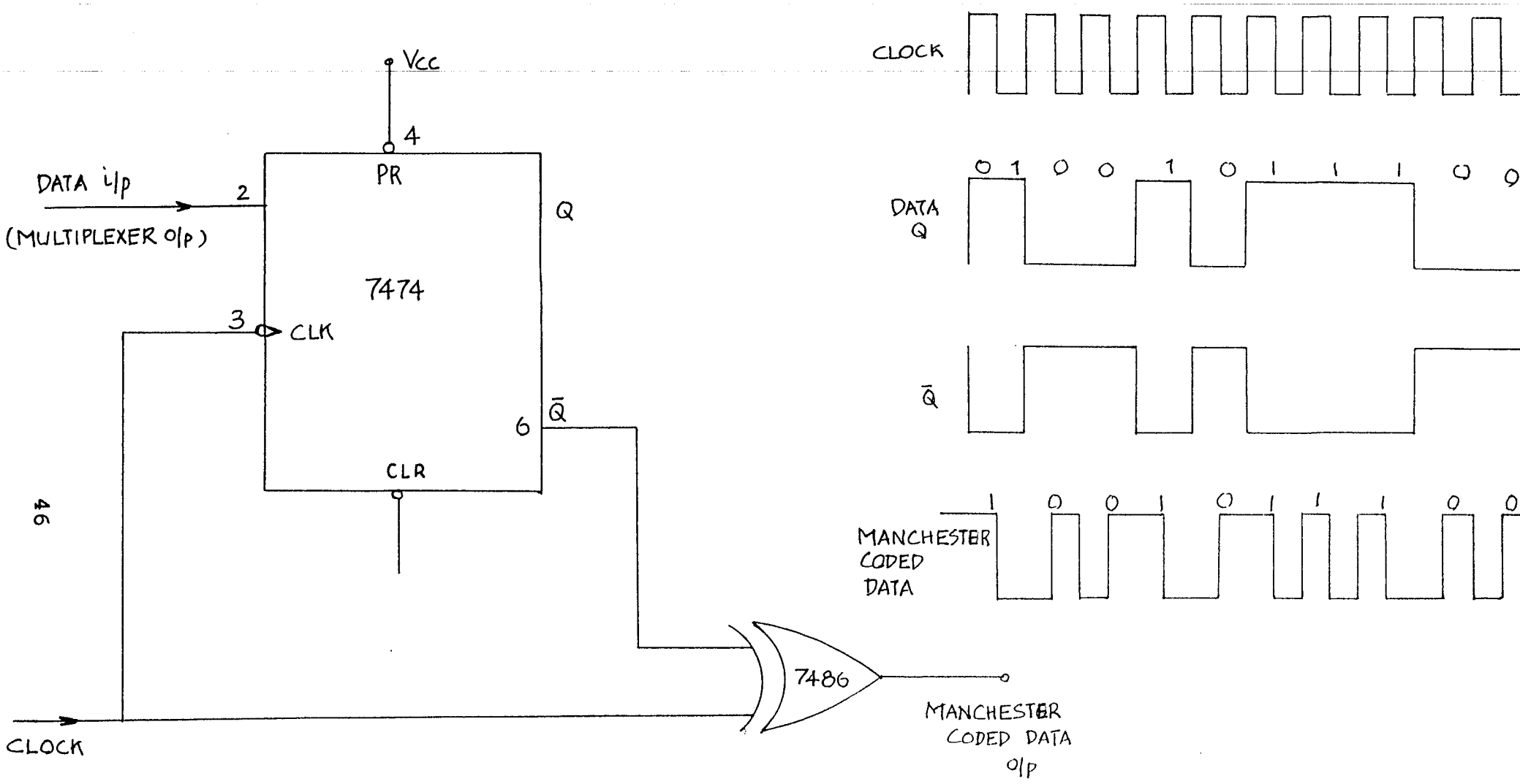


Fig. 4.3 MANCHESTER ENCODER.

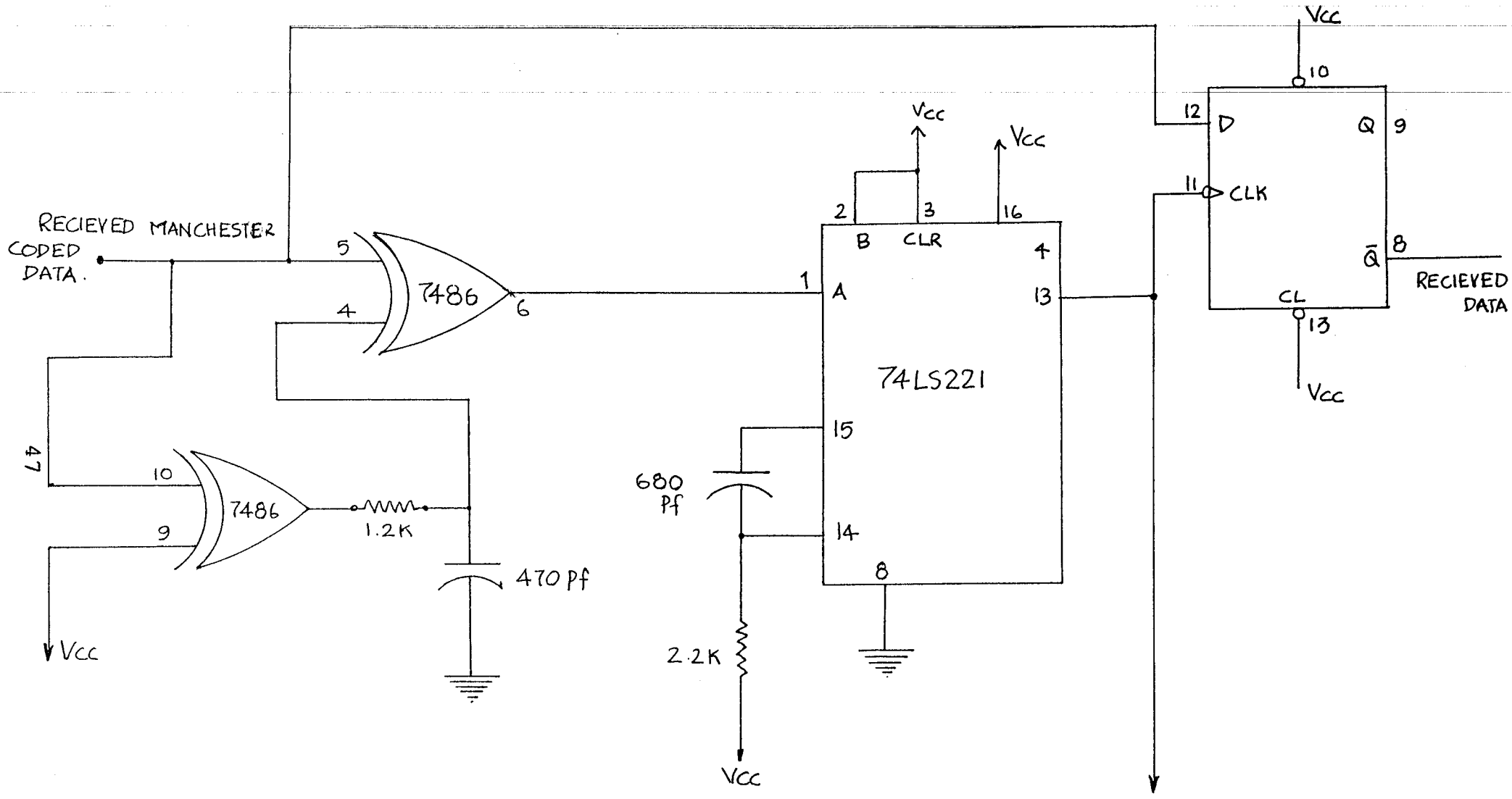


Fig 4.4. MANCHESTER DECODER

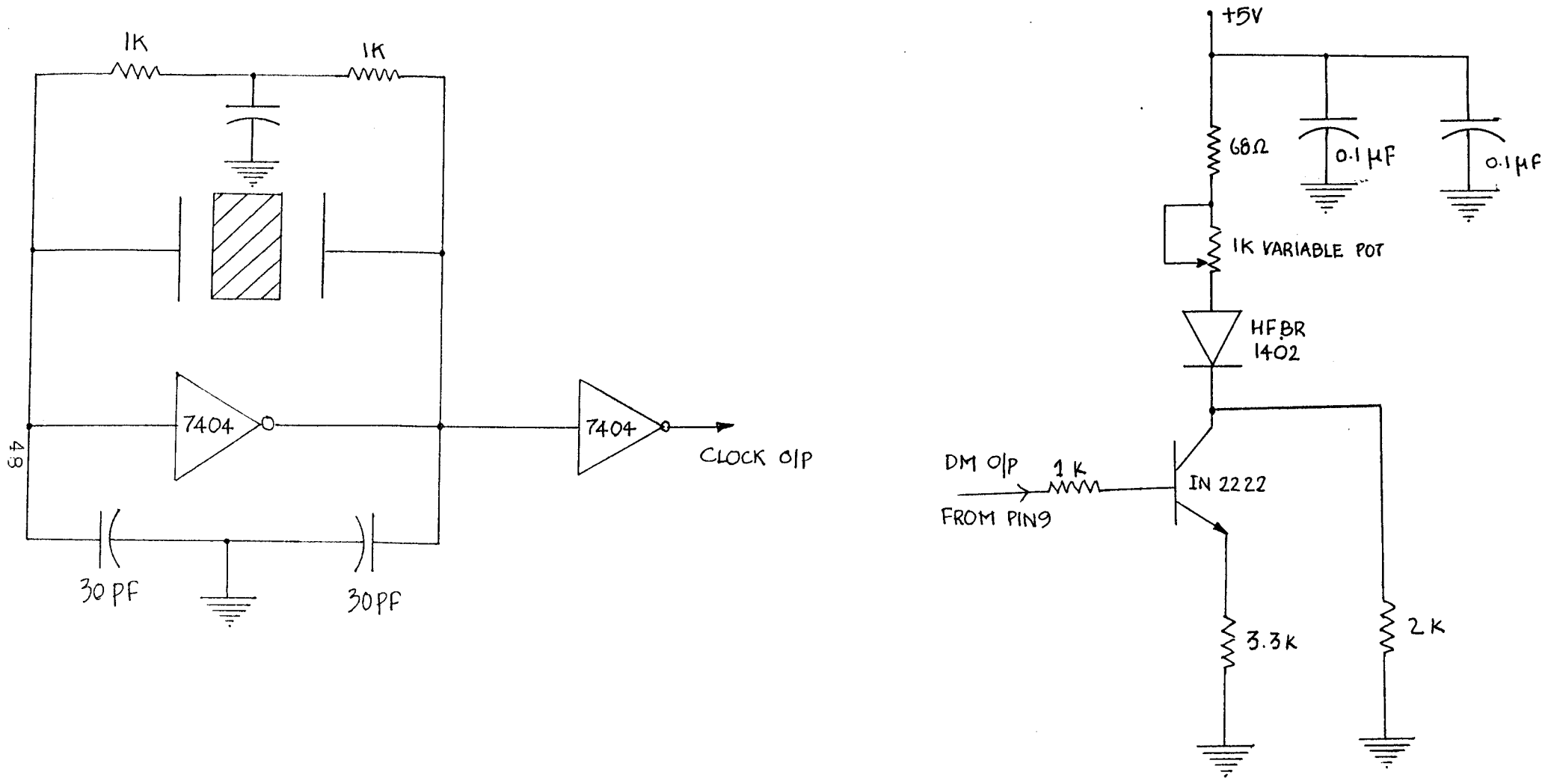


Fig. 4.6 CLOCK GENERATION & DRIVE CIRCUITRY

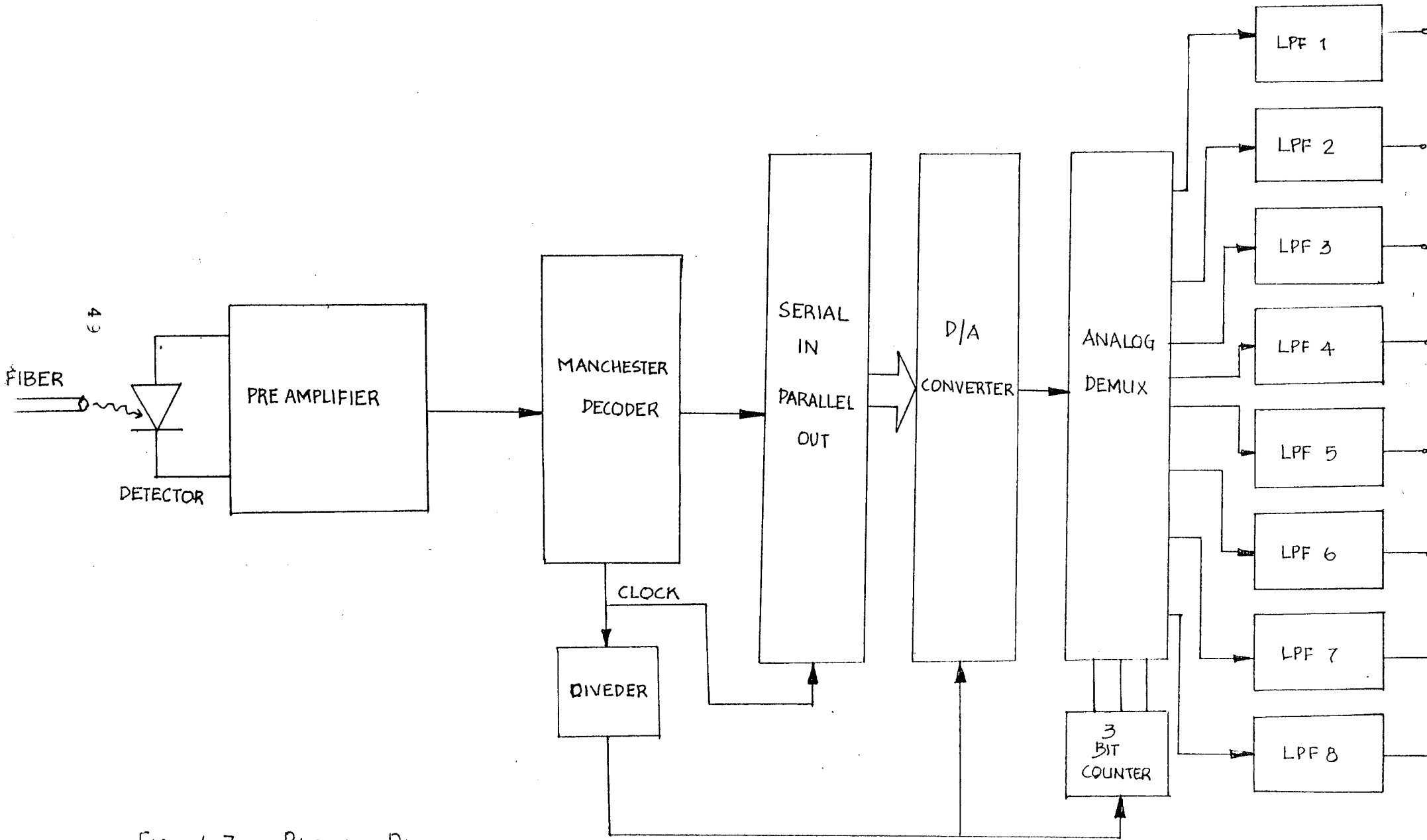


FIG 4.7. BLOCK DIAGRAM OF RECIEVER.

CHAPTER V

FIBER OPTIC LINK SIMULATION

CHAPTER 5

FIBER OPTIC LINK SIMULATION

5.1 Introduction

In this chapteer we discuss the details to develop a software in order to simulate a filter optic link, satisfying the speed, distance and bit error rate requirements of the user. The design of an optical link involves many interrelated variables among the fiber, source and detector operating characteristics so that the actual link design and analysis may require several iterations before they are completed satisfactorily. The key system requirements needed to simulate a link are.

1. The bit error rate(BER).
2. The desired transmission distance.
3. The data rate or channel Bandwidth.

In order to satisfy the above mentioned requirements we have a choice of step index or graded index fibers, LED, Laser diode or single mode laser diode as transmiters, PIN diode or avalanche photo diode as detectors.

5.2 Specifications and system considerations

In the link power budget, a decision on the wavelength at which transmison should take place is chosen, on basis of transmission distance. If the distance over which the data is transmitted is less, then the wavelength range 800-900nm can be used. But if the distance is larger, we take advantage of lower attenuation and dispersion occuring at wavelength around 1300nm.

Once we have decided the wavelength, we interrelate the performance of the receiver, transmitter and the optical fiber. The procedure we follow is to select the photo detector first . Then choose an optical source and see how far the data can be transmitted over a particular fiber before a repeater is needed in the line to boost up the power level of the optical signal. In choosing the photo detector, we mainly need to determine the minimum optical power that must fall on the photo detector to satisfy the BER requirment at the specified data rate. The design cost and complexity constraints can also be taken into consideration. The PIN diode is more simple, stable with temperature changes and less expensive. Also the bias voltage needed are less than 50V. But the increased sensitivity of APD overrules all other disadvantages it has.

The parameter involved in deciding between the use of LED or laser diode are signal dispersion, data rate, transmission distance and cost. The spectral width of the laser output is much narrower than that of LED. This is important in the range 800-900nm, where spectral width of an LED and the dispersion characteristics of fibers limit the data rate - distance product to around 150(Mb/s) Km. For higher values up to 2500(Mb/s)Km the laser is the only alternative at these wavelengths. At 1300nm wavelength signal dispersion is very low, and a bitrate-distance product of atleast 1500(Mb/s)Km is achievable with LED's.

Since laser diodes typically couple 10 to 15dbm more optical power than an LED into a fiber, greater repeaterless transmission distance is possible with a laser. This advantage and the lower dispersion capability of laser diodes may be offset by cost constraints.

For optical fiber we have a choice between single mode, multimode glass and plastic fiber, either of which has a step or graded index core. This choice depends upon the type of light source used and on the amount of dispersion than can be tolerated. For, multimode fibers, LED sources are used. .The optical power that can be coupled into a fiber depends on the core cladding index difference, which in turn is related to the numerical aperture, of the fiber.

The single mode or multimode fiber can be used with a laser diode. A single mode fiber can provide the alternate bit rate distance product (30Gb/s.Km). But their small core size makes fiber splicing more difficult and critical than for multimode fibers with 50 micro meter core diameters.

For plastic fibers LED sources are used. But this plastic fibers are not advisable for large distance transmission because of high loss.

5.3 Detector Selection

There are two classes of detectors available to us. They are PIN diode and avalanche photo diode(APD). The characteristics associated with these components which are to be taken into consideration when selecting them are,

a. Responsivity.

b. Operating Wavelength.

c. Speed.

d. Sensitivity.

5.4 Optical Source Selection

The different optical sources at our disposal are single mode laser diode, light emitting diode(LED) and laser diode. Their different characteristics to be taken into account for a link design process are.

a. Emission wavelength.

b. Special line width.

c. Output power.

d. Effective radiating area.

e. Emission pattern.

Fiber Selection

Based on the type of receiver and transmitter selected earlier, step index fiber or graded index fiber is selected to complete the link design process. The factors to be considered for choosing a fiber are.

a. Core size.

b. Core refractive index profile.

c. Band width.

d. Attenuation.

e. Numerical aperture.

5.5 Link Power Budget

An optical power loss model for a point-to-point link is shown in Fig 5.1. Theoptical power recieved at the photo detector depends on the amount of light coupled into fiber and the losses in the fiber, connectors and splices. The link loss budget is derived from the sequential loss contribution of each element in the link. Each of these loss elements are expressed as.

$$\text{Loss} = 10 \log_{10} (\text{Pout}/\text{Pin}) \text{ db}$$

where,

Pout = Optical power output

Pin = Optical power input

A link margin of 6 to 8 db is generally used for systems that are not expected to have future expansions.

The link loss budget considers the total optical power loss 'P', that is allowed betwen the light sources and photo detector and allocates this loss to cable attenuation, connector splice loss and system margin.

$$P_T = P_S - P_R$$

where,

P_R - Receiver sensitivity.

P_S - Power emerging from the fiber end attached to light source.

$$P_T = 2*l_c + \alpha_f *L + \text{System margin}$$

where,

l_c - Connector loss.

α_f - Fiber attenuation (db/Km).

L - Transmission distance.

The splice loss can be incorporated into the cable loss for simplicity. The link power budget can be graphically represented as shown in **Fig 5.2**

5.6 Rise Time Budget

A rise time budget analysis is a convenient method for determining the dispersion limitation of an optical fiber link. In these analysis,

$$t = (t_{sys}^2 + t_{tx}^2 + t_{rx}^2 + t_{mat}^2)^{1/2}$$

where,

t_{tx} - Transmitter rise time.

t_{rx} - Receiver rise time.

t_{mat} - Material dispersion time

t_{mod} - Modal dispersion time

Generally the total transition time degradation should not exceed 70% of a NRZ bit period or 35% of the bit period for RZ data, where one bit period is defined as the reciprocal of the data rate.

The rise time of transmitter and receiver arde generally known to the designer. The transmitter rise time is attribuitable primarily to the light source and its drive circuitry. The receiver rise time results from the photodetector responce and the 3-db electric band width of the receiver in MHz, then the receiver front end rise time is,

$$t_{rx} = 350/B_{rx} .$$

For multimode fibers the rise time depends on the model and material dispersions. It's analysis is more complicated since it is a function of the fiber length, the type of optical source, used and the operating wavelength. Material dispersion effects can be neglected for laser sources at both short and long wavelengths and for LED's at long wavelength's. In the wavelength range

of 800 - 900 nm, material dispersion adds about 0.07 nm/Km to the rise time.

For long continuous fiber which has no joints, the fiber band width decreases linearly with distance for lengths less than model equilibrium length 'L'. For lengths greater than 'L' a steady state equilibrium condition has been established and the bandwidth decreases as 'L' increases. Practically an optical fiber link seldom consists of a continuous jointless fiber. Several fibers are concatenated to form a long link, which complicates the situation because modal redistribution occurs at the fiber to fiber joints in the cable.

This is a result of misaligned joints, different degrees of mode mixing in individual fibers and the most important being the different core index profiles. The core index profile influences the degree of modal dispersion - induced pulse spreading in a fiber and depending on the wavelength minimises the pulse dispersion. The bandwidth $B_M(L)$ in a link of length 'L' is,

$$B_M(L) = B_0 / L^q$$

where,

B_0 - Bandwidth of a 1Km length of cable.

q - A parameter ranging between 0.5 and 1.

A reasonable estimate for q is 0.7

$$f_{3\text{-db}} = B_{3\text{-db}} = 0.44/t_{FWHM}$$

where,

t_{FWHM} - Full pulse width at its half minimum value

$$t_{FWHM} = 2*t_{1/2} = 26(2*\ln 2)^{1/2}$$

Letting t_{FWHM} to be the rise time resulting from model dispersion, then

$$t_{mod} = 0.44/B_M = 0.44*L^q / B_0 = 440*L^q / B_0 \text{ ns.}$$

All these finally gives a total system rise time of

$$t_{sys} = [t_{tx}^2 + D_{mat}^2 * \sigma_{lam}^2 * L^2 + (440*L^q/B_0)^2 + (350/B_{rx})^2]^{1/2}$$

where,

σ_{lam} - is the spectral width of the optical source

D_{mat} - Material dispersion factor of the fiber (given in ns/nm.Km)

And all times are given in nano seconds. In 800-900nm region the value of D is about 0.07ns/nm.Km and is negligible around 1300nm..lm 10

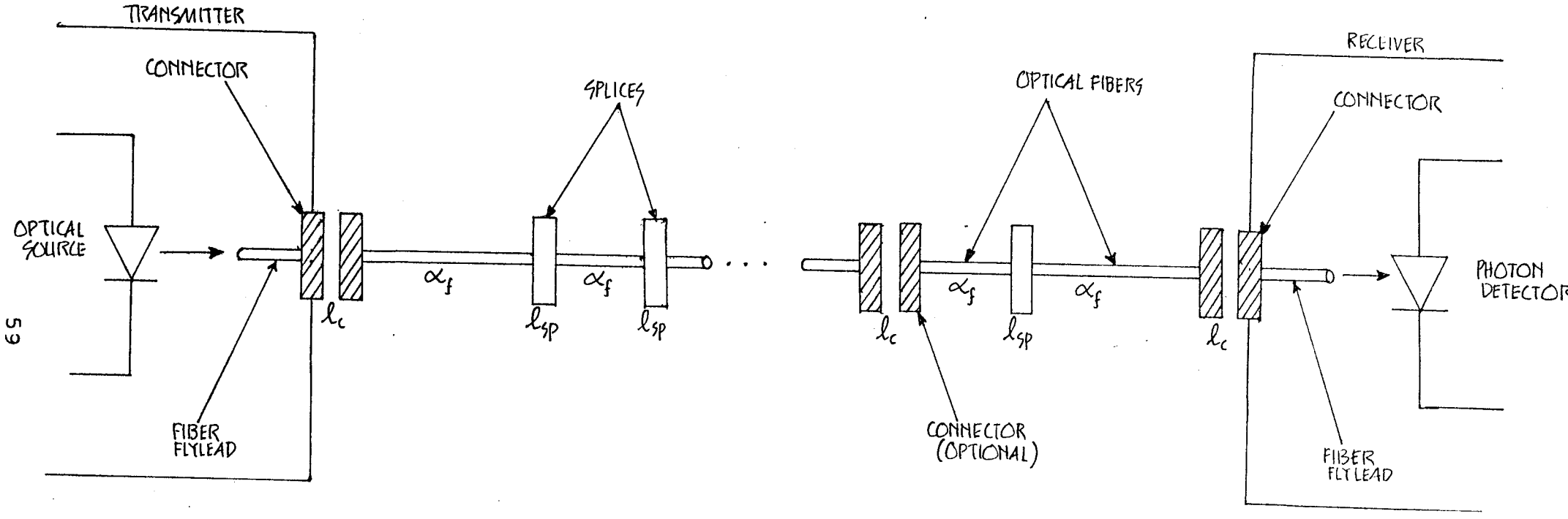


Fig 5.1: OPTICAL POWER LOSS MODEL FOR A POINT-TO-POINT LINK

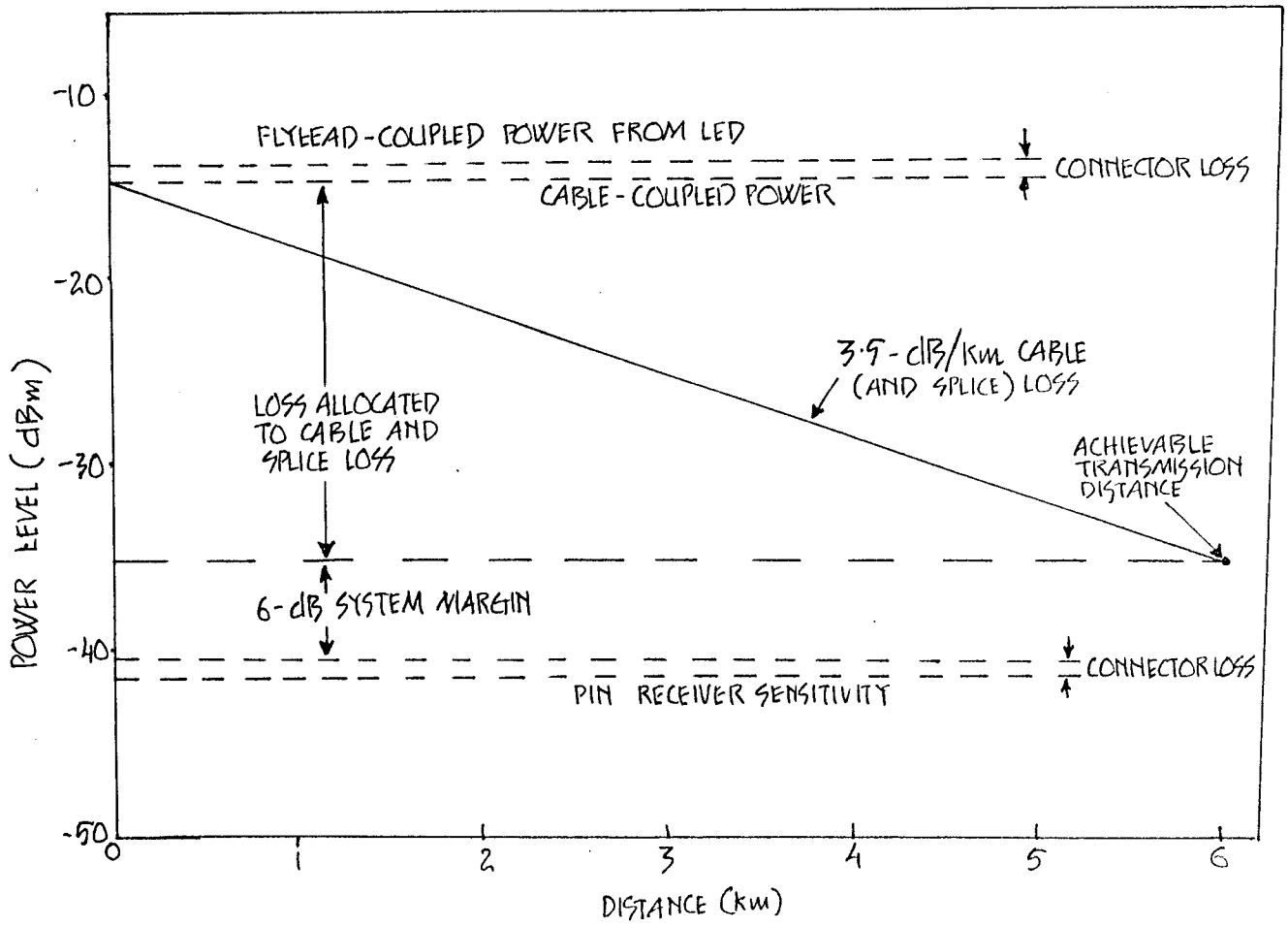


Fig 5.2: GRAPHICAL REPRESENTATION OF A LINK LOSS BUDGET

CHAPTER VI

SOFTWARE DETAILS

CHAPTER 6

SOFTWARE DETAILS

This software allows the user to select the fiber, transmitter and receiver at a particular wavelength. The software outputs whether repeaters are required or not and how many repeaters are needed. It also tells whether transmission is possible in NRZ or RZ format. Finally the programme outputs the general characterstics of the system. For which the analysis has been performed.

ALGORITHM

First of all the user has to select the fiber. He has 8-Choises from which we can select any one. Next the source is selected there we have two choises viz, LED and LASER. The wavelength available are also displayed alongwith the types of sources. Next the detector is selected. Here we have six choices from which the one required is selected.

Next the user has to input the following details:

1. System margin (db)
2. Data rate (M.Bits/sec)
3. Length of the link (Km)
4. Source coupling power (db)
5. Receiver sensitivity (db)
6. Connector loss (db)

All the parameters related to the fiber, source and detector are stored in any array. Now all the data required for link power budget analysis and system rise time budget analysis are available.

The link power budget analysis is performed first. Here the maximum repeaterless transmission distance is found using the formula

$$L = \frac{Ps - Pr - 2 * lc - Sm}{\alpha_f}$$

where,

Ps - Source coupling power (db)

Pr - Receiver sensitivity (db)

lc - Connector loss (db)

Sm - System margin (db)

f - Attenuation of the fibre (db/Km)

From the value of 'L' we can calculate the number of repeater required and is displayed.

In system rise time budget analysis the total system rise time is calculated using the formula

$$tsys = [ttx^2 + D_{mat}^2 \sigma_{lam}^2 L^2 + (440 * L_0^q /B)^2 + (350/B)_{rx}^2]^{1/2}$$

Where,

ttx - transmission rise time (ns)

Dmat - material dispersion factor of the fiber (ns/nm/km)

δ_{lam} - Spectral width of the optical source (nm)

L - Length of the link (km)

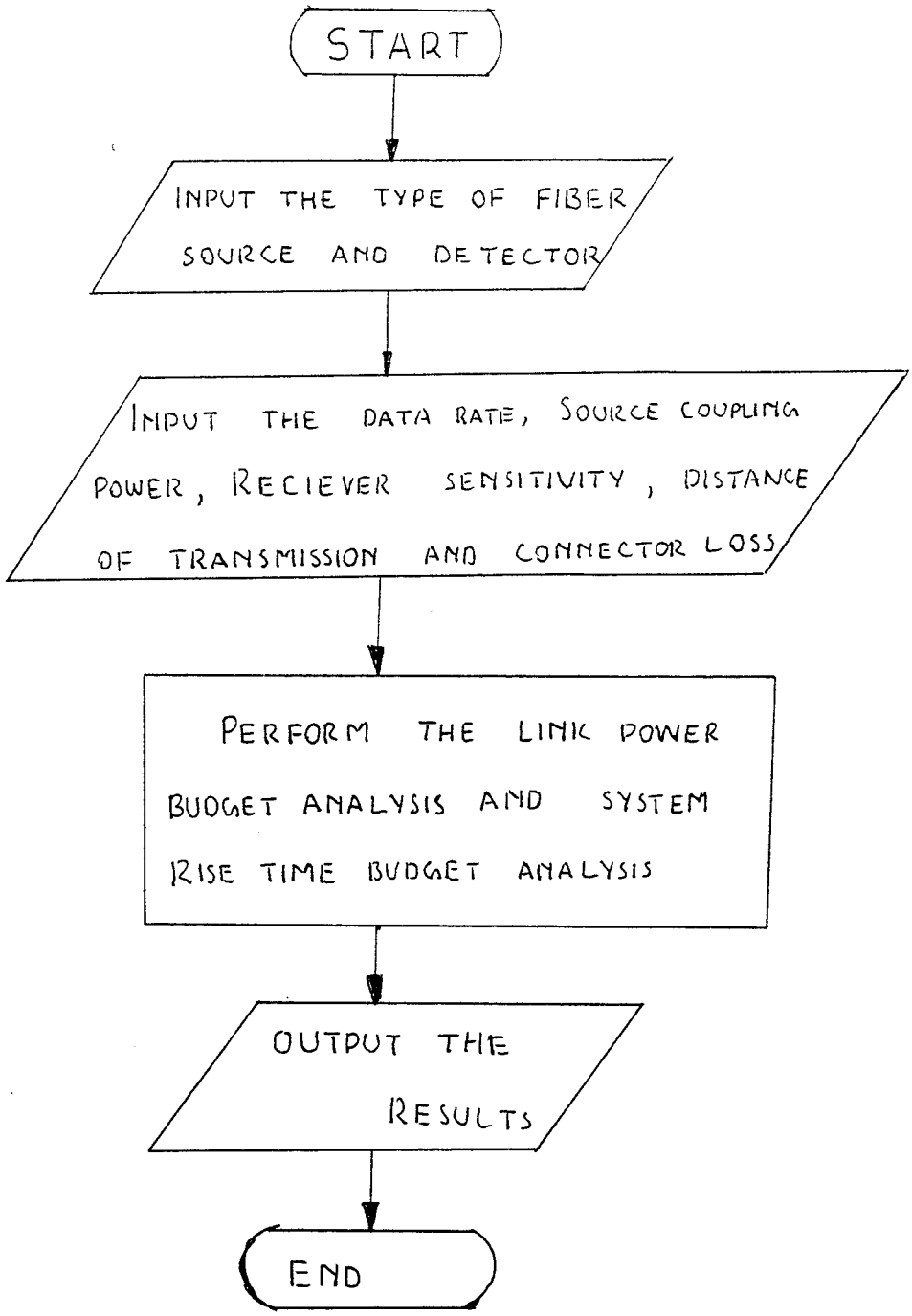
q - Constant whose value is 0.7

B_0 - Band width of a 1km length of the cable (MHz)

Brx - 3db electric bandwidth of the receiver (1MHz)

If the total transition time degradation of the digital link exceeds 70% of an NRZ bit period (or) 35% of a bit period for RZ data, then transmission is not possible. After performing the system rise time budget analysis the feasibility of transmission is displayed.

FLOWCHART


START
INPUT THE TYPE OF FIBER SOURCE AND DETECTOR
INPUT THE DATA RATE, SOURCE COUPLING POWER, RECIEVER SENSITIVITY, DISTANCE OF TRANSMISSION AND CONNECTOR LOSS
PERFORM THE LINK POWER BUDGET ANALYSIS AND SYSTEM RISE TIME BUDGET ANALYSIS
OUTPUT THE RESULTS
END

```
#include <stdio.h>
#include <conio.h>
#include <string.h>
#include <math.h>
main()
{
int ch,ch1,wl,fdl,i;
int ch2,ch3,ch4,nr,c;
/*char fib[4][40];*/
char sc[20],fbr[40],dt[30];
/*char sou[3][20],det[6][30];*/
float l,sm,tt,tr;
float ln,ps,pr,lc,s,f;
float lo,n,dm,bo,q;
float tsys,t;
/* l-- attenuation;
   wl-- wavelength;
   tsys-- system rise time;
   tt-- trnsmitter rise time;
   c-- number of repeaters used;
   lo-- length at which first repeater is placed;
   dm-- material dispersion;
   bo-- band width for one Km. ;
   q-- a constant ;
   tr-- rise time;
   sm-- spectral width;
   lc-- connector loss;
   f-- data rate;
   s-- system margin;
   pr-- receiver sensitivity;
   ps-- source margin;
    ln-- length of the link;
*/
char sou[][20]={"LED","Laser diode","SM Laser diode"};
char det[][30]={"Silicon PIN","Germanium PIN","In Ga As PIN","Silicon APD","Ge
anium APD","In Ga As APD"};
char fib[][40]={"Multimode glass step index","Multimode glass graded index","S
gle mode glass","Plastic step index"};
clrscr();
printf("\n\n\tSELECTION OF FIBER\n");
gotoxy(9,4);
for(i=0; i<20; i++)
  printf("-");
printf("\n\t1.Multimode Glass\n");
printf("\n\t2.Single mode\n");
printf("\n\t3.Plastic\n");
printf("\nENTER THE FIBER : ");
scanf("%d",&ch);
switch(ch)
{
case 1:
printf("\n\t1.Step Index\n");
printf("\t2.Graded Index\n");
printf("\nENTER THE CHOICE : ");
scanf("%d",&ch1);
switch(ch1)
{
 case 1:
```

```
    /* Step index operation*/
    printf("\nSource is LIGHT EMITTING DIODE  ( LED )\n");
    wl=850;
    strcpy(fbr,fib[0]);
    l=5;fdl=33;strcpy(sc,sou[0]);
    break;
    case 2:
    /* Graded index operation*/
    printf("\n\tTwo types are there\n");
    printf("1.Wave length : 850\n");
    printf("2.Wave length : 1300\n");
    printf("ENTER THE SELECTION : ");
    scanf("%d",&ch2);
    strcpy(fbr,fib[1]);
     if(ch2==1)
     {
     wl=850;l=5;fdl=500;
     }
     if(ch2==2)
     {
     wl=1300;l=1;fdl=1000;
     }
   printf("\n\tTwo types of sources are possible\n");
   printf("1.Laser diode\n");
   printf("2.Light emitting diode\n");
   printf("ENTER THE SOURCE : ");
   scanf("%d",&ch3);
   if(ch3==1)
   strcpy(sc,sou[1]);
    if(ch2==2)
    strcpy(sc,sou[0]);
    break;
    }
   break;
   case 2:
   printf("\n\tThree wavelengths are available\n");
   printf("\t\t1.Wave length : 850\n");
   printf("\t\t2.Wave length : 1300\n");
   printf("\t\t3.Wave length : 1550\n");
   printf("\nENTER THE CHOICE : ");
   scanf("%d",&ch1);
   strcpy(fbr,fib[2]);
   printf("Source is SINGLE MODE LASER DIODE.\n");
   strcpy(sc,sou[2]);
   switch(ch1)
   {
    case 1:
    wl=850;l=4;fdl=1000;
    break;
    case 2:
    wl=1300;l=0.5;fdl=83000;
    break;
    case 3:
    wl=1550;l=0.2;fdl=83000;
    break;
    }
    break;
  case 3:
  printf("\n\tTwo wavelengths are available\n");
  printf("\t\t1.Wave length : 850\n");
```

```
printf("\t\t2.Wave length : 580\n");
printf("ENTER THE CHOICE : ");
scanf("%d",&ch1);
strcpy(fbr,fib[3]);
printf("Source is LIGHT EMITTING DIODE.\n");
strcpy(sc,sou[0]);
switch(ch1)
{
 case 1:
 wl=850;l=8;fdl=10;
 break;
 case 2:
 wl=850;l=200;fdl=10;
 break;
 }
 break;
}
 if((strcmp(sc,"LED"))==0)
 {
 sm=50;tt=100;
 }
 if((strcmp(sc,"Laser diode"))==0)
 {
 sm=2;tt=1;
 }
 if((strcmp(sc,"SM Laser diode"))==0)
 {
 sm=0.2;tt=0.01;
 }
 printf("\n\n\tSELECTION OF DETECTOR\n");
 switch(wl)
 {
  case 580:
  case 850:
   printf("\n\t1.Silicon PIN\n");
   printf("\t2.Germanium PIN\n");
   printf("\t3.Silicon APD\n");
   printf("\nENTER THE CHOICE : ");
   scanf("%d",&ch4);
   switch(ch4)
   {
    case 1:
     strcpy(dt,det[0]);
     tr=0.5;
     break;
    case 2:
     strcpy(dt,det[1]);
     tr=0.1;
     break;
    case 3:
     strcpy(dt,det[3]);
     tr=0.5;
     break;
   }
   break;
  case 1300:
  case 1550:
   printf("\n\t1.In Ga As PIN\n");
   printf("\t2.Germanium  PIN\n");
   printf("\t3.In Ga As APD\n");
```

```
    printf("\t4.Germanium APD\n");
    printf("\nENTER THE CHOICE : ");
    scanf("%d",&ch4);
    switch(ch4)
    {
     case 1:
      strcpy(dt,det[1]);
      tr=0.1;
      break;
     case 2:
      strcpy(dt,det[2]);
      tr=0.3;
      break;
     case 3:
      strcpy(dt,det[4]);
      tr=1.0;
      break;
     case 4:
      strcpy(dt,det[5]);
      tr=0.25;
      break;
      }
   break;
   }
   printf("\n\n STRIKE any key to continue\n");
   getch();
   clrscr();
   printf("\t INPUTS \n");
   printf("\t Length of the link(in KMs): ");
   scanf("%f",&ln);
   printf("\t Source coupling power(in dbm) : ");
   scanf("%f",&ps);
   printf("\t Reciever sensitivity(in db): ");
   scanf("%f",&pr);
   printf("\t System margin(in db): ");
   scanf("%f",&s);
   printf("\t Data rate(in Mb): ");
   scanf("%f",&f);
   printf("\t Connector loss(in db): ");
   scanf("%f",&lc);
   printf("\n Calculation starts now\n");
   delay(1000);
   lo=(ps-pr-2*lc-s)/l;
   n=ln/lo;
   c=(int)n;
   if(n>c)
   c=c+1;
   if(c < 0 )
     {
       printf("\n\n\t\t SOURCE COUPLING POWER IS LESS.");
       printf("\n\t\t   CHOOSE APPROPRIATE SOURCE.");
       printf("\n\n\t\t\t TRY AGAIN !!!!!\n\n");
       getch();
       exit(0);
     }
  if(wl==850)
  dm=0.07;
  else
  dm=0;
  bo=fdl/ln;
  q=0.7;
```

```
tsys=sqrt(pow(tt,2)+pow(dm,2)*pow(sm,2)*pow(ln,2)
        +pow((pow(ln,q)*440/bo),2)+pow(tr,2));
t=1/f;
t=70*t/100;
if (tsys>t)
{
printf("\n\n\n Transmission is possible in RZ format.\n");
}
else
{
printf("\n\nTransmision is possible in NRZ format.\n");
}
printf("\nRepeaters may be required.\n");
printf("\nNumber of repeaters required.-->%d\n",c);
printf("\nPRESS <ENTER> FOR SPECIFICATION\n\n");
while(getch()!=13);
if((strcmp(sc,"LED"))==0)
{
clrscr();
printf(" SPECIFICATIONS OF LIGHT EMITTING DIODE\n");
printf("\nSpectral width (in nm) :%f\n",sm);
printf("\nRise time(in ns):%f\n",tr);
printf("\nModulation bandwidth(in Mbits/Sec):300\n");
printf("\nCoupling efficiency:very low\n");
printf("\nFiber selected:%s\n",fbr);
printf("\nTemperature sensitivity:Low\n");
printf("\nCicuit compexity:Simple\n");
printf("\nLifetime(in hours):100000\n");
printf("\nCosts:Low\n");
printf("\n\nAPPLICATIONS : MODERATE PATHS,MODERATE DATA RATES");
}
    if((strcmp(sc,"Laser diode"))==0)
{
clrscr();
printf("\n SPECIFICATIONS OF LASER DIODE\n");
printf("\nSpectral width (in nm) :%f\n",sm);
printf("\nRise time(in ns):%f\n",tr);
printf("\nModulation bandwidth(in Mbits/Sec):2000\n");
printf("\nCoupling efficiency:moderate\n");
printf("\nFiber selected:%s\n",fbr);
printf("\nTemperature sensitivity:High\n");
printf("\nCicuit compexity:Complex\n");
printf("\nLifetime(in hours):100000\n");
printf("\nCosts:High\n");
printf("\n\nAPPLICATIONS : LONG PATHS,HIGH DATA RATES");
}
    if((strcmp(sc,"SM Laser diode"))==0)
{
clrscr();
printf(" SPECIFICATIONS OF SINGLE MODE LASER DIODE\n");
printf("\nSpectral width (in nm) :%f\n",sm);
printf("\nRise time(in ns):%f\n",tr);
printf("\nModulation bandwidth(in Mbits/Sec):6000\n");
printf("\nCoupling efficiency:high\n");
printf("\nFiber selected:%s\n",fbr);
printf("\nTemperature sensitivity:High\n");
printf("\nCicuit compexity:Complex\n");
printf("\nLifetime(in hours):100000\n");
printf("\nCosts:Very high\n");
printf("\n\nAPPLICATIONS : VERY LONG PATHS,VERY HIGH DATA RATES");
```

```
  }
getch();
clrscr();
gotoxy(25,12);
printf("END OF SOFTWARE\n");
getch();
}
```

```
        SELECTION OF FIBER
        ------------------

        1.Multimode Glass

        2.Single mode

        3.Plastic

ENTER THE FIBER : 2

        Three wavelengths are available
                1.Wave length : 850
                2.Wave length : 1300
                3.Wave length : 1550

ENTER THE CHOICE : 3


Source is SINGLE MODE LASER DIODE.


        SELECTION OF DETECTOR

        1.In Ga As PIN
        2.Germanium  PIN
        3.In Ga As APD
        4.Germanium APD

ENTER THE CHOICE : 4


 STRIKE any key to continue


         INPUTS
         Length of the link(in KMs): 1000
         Source coupling power(in dbm) : 30
         Reciever sensitivity(in db): 16
         System margin(in db): 6
         Data rate(in Mb): 4
         Connector loss(in db): 1

 Calculation starts now


 Transmission is possible in RZ format.

Repeaters may be required.

Number of repeaters required.-->34

PRESS <ENTER> FOR SPECIFICATION
```

SPECIFICATIONS OF SINGLE MODE LASER DIODE

Spectral width (in nm) :0.200000

Rise time(in ns):0.250000

Modulation bandwidth(in Mbits/Sec):6000

Coupling efficiency:high

Fiber selected:Single mode glass

Temperature sensitivity:High

Cicuit compexity:Complex

Lifetime(in hours):100000

Costs:Very high

APPLICATIONS : VERY LONG PATHS,VERY HIGH DATA RATES

END OF SOFTWARE

```
        SELECTION OF FIBER

        1.Multimode Glass

        2.Single mode

        3.Plastic

ENTER THE FIBER : 1

        1.Step Index
        2.Graded Index

ENTER THE CHOICE : 1



Source is LIGHT EMITTING DIODE  ( LED )

        SELECTION OF DETECTOR

        1.Silicon PIN
        2.Germanium PIN
        3.Silicon APD

ENTER THE CHOICE : 1

 STRIKE any key to continue


        INPUTS
        Length of the link(in KMs): 1560
        Source coupling power(in dbm) : 12
        Reciever sensitivity(in db): 14
        System margin(in db): 4
        Data rate(in Mb): 2
        Connector loss(in db): 1

Calculation starts now

              SOURCE COUPLING POWER IS LESS.
                CHOOSE APPROPRIATE SOURCE.

                    TRY AGAIN !!!!!
```

CHAPTER VII

ADVANTAGES OF FIBER OPTICS

CHAPTER 7

ADVANTAGES AND APPLICATIONS OF FIBER OPTICS

7.1 Advantages of optical fiber communication

Communication using an optical carrier wave guided along a glass fiber has a number of extremely attractive features. The advances in the technology to date have surpassed even the most optimistic predictions creating additional advantages. The main advantages of fiber optic communications is given below.

a) Enormous bandwidth

The optical carrier frequency in the range 10^{13} to 10^{16} Hz yields for a greater potential transmission bandwidth than metallic cable systems or even millimeter wave radio systems currently operating with modulation bandwidths of 700MHz. At present the bandwidth available to fiber systems is not fully utilized but modulation at several GHz over a few KMs and hundreds of MHz over tens of KMs without repeaters is possible. Therefore the information carrying capacity of optical fiber systems is already providing far superior to the best copper cable systems. By comparison the losses in wideband coaxial cable system restrict the transmission distance to only a few KMs at bandwidths over 100 MHz.

b) Small size and weight

Optical fibers have very small diameter which are often no greater than the diameter of a human hair.

Hence, even when such fibers are covered with protective coatings they are far smaller and much lighter than corresponding copper cables. This a tremendous boon towards the alleviation of congestion in cities, as well as allowing for an expansion of signal transmission within mobiles such as aircraft, satellites and even ships.

c) Electrical isolation

Optical fibers which are fabricated from glass or sometimes a plastic polymer are electrical insulators and therefore, unlike their metallic counter parts they do not exhabit earth loops and interface problems. Further more this property makes optical fiber tranamission ideally seated for communication in electrically hazardous environment as the fibers create no arcing or spark hazard at abrasions or short circuits.

d) Immunity to interfence and crosstalk

Optical fibers form a dielectric waveguide and are therefore free from electromagnetic interference,radio frequency interference or switching transients giving electromagnetic pulses. Hence the operation of an optical fiber common system is unaffected by transmission through an electrically noisy environment and thus fiber cable requires no shielding from electrically noisy environment. The fiber cable is also not susceptable to lightning strokes if used overhead rather than underground.Moreover it is fairly easy to

ensure that there is no optical interference between fibers and hence, unlike common using electrical conductors, crosstalks is negligible, even when many fibers are cabled together.

e) Signal security

The light from optical fibers does not radiate significantly and therefore they provide a high degree of signal security. Unlike the situation with copper cables, a transmitted optical signal cannot be obtained from a fiber in a noninvasive manner. This feature is obviously attractive for military, banking and general data transmission.

f) Low transmission loss

The development of optical fibers over the last 15 years has resulted in the production of optical fiber cables which exhibit very low attenuation or transmission loss in comparision with the best copper conductors.

It facilitates the implementation of communication links with extremely wide repeater spacing thus reducing cost and complexity.

7.2 APPLICATIONS AND FUTURE DEVELOPMENTS

7:2.1 INTRODUCTION

The Primary advantage obtained using Optical fibers for Line Transmission were discussed in the previous section. In this chapter we consider current and

potential applications of optical fibre communication systems together with some likely future devolopments in the general area of optical transmission and associated components. The discussion is primarly centered around application areas including the public network,military,civil and consumer,industrial and computer systems which are delt in coming sections.However,this discussion is extended with a brief review of integrated optical techniques and devices.

7:2.2 PUBLIC NETWORK APPLICATIONS

The public telecommunications network provides a variety of applications for optical fiber communication systems . The current plans of the major PTT administrations around the world feature the installation of increasing numbers of optical fiber links as an alternative to co axial and high frequency pair cable systems. According to the place where networks are used they are divided into

a. Trunk Network
b. Junction Network
c. Local and Rural Network
d. Submerged Systems

a. TRUNK NETWORK

The Trunk or Toll Network is used for carring telephone traffic between major conurbations. Hence there is generally a requrment for the use of

transmission systems which has a high capacity. The transmission distance for trunk system can vary enormously from under 20 km to over 300 km, and occasionally to as much as 1000 km. These systems operate in the 0.85 to 0.90 mm wave length region using injection laser sources via graded index fiber to silicon avalanche photo diode detectors with repeated spacings of between 8 and 10 km.

b.JUNCTION NETWORK

The junction or inter office network usually consists of routs within nature conurbations over distances of typically 5 to 20 km. The distribution of distances between swithing centers (telephone exchanges) or offices in the junction network of large urban areas varies considerably for various countries. A number of proprietary systems predominantly operating at 8 M bits/s using both injection laser and LED sources via multimode graded index fiber to Avalanche photo diode detectors are in operation in the UK with repeater spacing between 7.5 and 12 km.

c. LOCAL AND RURAL NETWORKS

The local and rural network or subscriber loop conects telephone subscribers to the local switching center or office . Possible network configurations are shown in **fig.7.1** and include a ring, tree and star topology from the local switching center. In a ring network any informations fed into the network by subscriber passes through all the network nodes and

hence a number of transmission channels must be provided between all nodes . The tree network, which consists of several branches , must also provide a number of transmission channels on its common links. In contrast the star network provides a seperate link for every subscriber to local switching center.

d. SUBMERGED SYSTEMS

Undersea cable systems are an integral part of the international telecommunications network.They find applications on shorter routes especially in Europe.On longer routes , such as across the Atlantic , they provide route diversity in conjunction with satellite links . It is predicted that single mode optical fiber systems operating at 1300 nm or 1550 nm will provide repeater spacing of 25 to 50 km and eventually even longer .

7:2.3 MILITARY APPLICATIONS

In these applications , although economics are important ,there are usually other , possibly overriding considerations such as size , weight ,deployability, surviavibility (in both conventional and nuclear attack) and security. The special attributes of optical fiber communication system therefore often lend themselves to the following uses.

a. MOBILES

One of the most promising areas of military applications for optical fiber communications is within

military mobiles such as Aircrafts , Ships and Tanks. The small size and weight of optical fibers provide an attractive solution to space problems in these mobiles. Further more , the immunity of optical transmission to electromagnetic interference, lightning and electromagnetic pulses (EMP) is a tremendous advantage. The electrical isolation and therefore safety , aspect of optical fiber communications also proves invaluable in these applications allowing routing through both fuel tanks and magazines.

b. COMMUNICATION LINKS

The other major area for the application of optical fiber communications in the military sphere includes both short and long distance communication links. Short distance optical fiber systems may be utilized to connect closely spaced items of electronic equipment in such areas as operation rooms and computer installations. There is also a requirment for long distance communication between military installations. Other long distance applications include Torpedo and Missile guidance , information links between military vessels and maritime , towed sensor arrays. Optical fiber cables has been installed and tested within the Ptarmigan tactical communication systems devoloped for British Army.

7.2.4 CIVIL AND CONSUMER APPLICATIONS

a) CIVIL

The introduction of optical fiber communication systems into the public network has stimulated investigation and application of these transmission techniques by public utility organizations. Optical fibers are eminently suitable for video transmission. Thus they can be used in commercial TV transmission. These applications include short distance link between studio and outside broadcast vans , links between studios and broadcast or receiving arials and closed circuit TV (CC TV) links for security and surveillance. In common with the military applications , other potential civil uses for optical fiber systems include short distance communications within buildings and within mobiles such as aircrafts and ships.

b) CONSUMER

A major consumer applications for optical fiber systems is within automotive electronics. Work is progressing within the automobile industry towards this end together with the use of microcomputers for engine and transmission control as well as control of convenience features such as power windows and controls. Other consumer applications are likely to include home applications where together with microprocessor technology, optical fibers may be able to make an impact.

7:2.5 INDUSTRIAL APPLICATIONS

Industrial uses for optical fiber communications cover a variety of generally on - premise applications within a single operational site.These systems ofter reliable telemetry and control communications for industrial environments where EMI and EMP cause problems for metallic cable links. Further more, optical fiber systems provide a far safer solution than conventional electrical monitoring in situations where explosive gases are abundant(e.g. chemical processing and petroleum refining plants)

SENSOR SYSTEMS

There is a requirement for the accurate measurement of parameters such as liquid levels,flow rate, position, temperature and pressure in these environments which may be facilitated by optical fiber systems. Electrooptical transducers together with optical fiber telemetry systems offer significant benefits over purely electrical systems in terms of immunity to EMI and EMP as well as intrinsic safety in the transmission to and from the transducer. Some of the optic transducers are shown in fig.7.2.

7:2.6 COMPUTER APPLICATIONS

Modern computer systems consist of a large number of interconnection. This ranges from lengths of a few micro meters to perhaps thousands of Km's for terrestrial links in computer networks. The transmission rates over these interconnections also cover a wide range from about 100 bits/sec for some tele type terminals to several hundred Mbits/sec for on-chip connections. Optical fibers are starting to find applications in this connection hierarchy where secure , interference free transmission is required.

LOCAL AREA NETWORKS

A LAN is generally defined as an interconnection topology entirely confined within a geographical area of a few square Km's. Such a network may support terminal connected to a host computer, or provide communication between multiple processors and terminals or work stations. In the latter application the LAN may also provide an interface to the local telecommunication network.

In common with local and rural networks LAN's may be designed in three major configurations : the star , the ring and the bus.

Although the LAN configuration and protocols are still largely under developement , optical fibers have been successfully utilised to provide such computer

interconnection.

Perhaps the largest scale applications at present for optical fibre systems within local area networks are with regard to single channel and multiplexed star networks. These network configurations tend to match to communication system design of large main frames and mini computers.

Recent installations of this type include airport data communication networks , traffic monitoring and control schemes and company on site or local intersite networks.

Further more , improvements in optical fiber connected technology and in the optical output power provided by light sources may lead to the extensive use of bus networks in the future.

7:2.7 INTEGRATED OPTICS

The multitude of potential application areas for optical fiber communications coupled with the tremendous advances in the field have over the last few years stimulated a resurgence of interest in the area of integrated optics. The concept of integrated optics involves the realisation of optical and electro-optical elements which may be integrated in large numbers on to a single substrate. Hence integrated optics seeks to provide an alternative to the conversion of an optical signal back into the electrical regime prior to signal processing by allowing such processing to be performed

on the optical signal. The thin transparent dielectric layers on planar substrates which act as possible wave guides are used in integrated optics to produce miniature optical components and circuits.

A major factor in the development of integrated optics is that it is essentially based on single mode optical wave guides and is therefore incompatible with multimode fiber systems. Hence integrated optics did not make a significant contribution to first and second generation optical fiber systems. The development , however of third generation or single mode fiber systems has been aided by integatred optical techniques.

7:2.8 INTEGRATED OPTICAL DEVICES

In this section some examples of various types of integrated optical devices together with their salient features are considered. Integrated optics provides optical methods for multipexing , modulation and routing. These various functions may be performed with a combination of optical beam splitters , switches, modulators , filters , sources and detectors.

Beam splitters and switches

Beam splitters are basic element of many optical fiber communication system often providing a Y-junction by which signals from seperate sources can be combined , or the received power divided between two or more channels.

The passive junction beam splitter find application where equal power division of the incident beam is required.

Modulators

To extend the band width capability of single mode fiber systems there is a requirement for high speed modulation which can be provided by integrated optical wave guide intensity modulators. Simple ON/OFF modulators may be based on the techniques utilized for the active beam splitters and switches. In addition a large vareity of predominantly electro-optic modulators exibit good chracteristics.

Periodic structure for filters and injection lasers

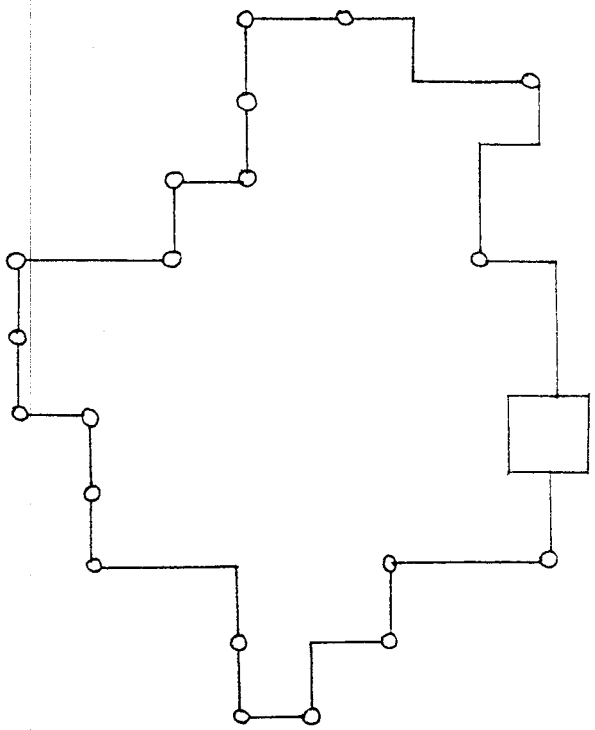
Periodic structures may be incorporated into planar wave guides to form integrated optical filters and resonators. Light is scattered in such a guide in a similar manner to light scattered by a diffraction grating. When light propagating in the guide impinges on the corrugation some of the energy will be diffracted out of the guide into either the core or the substrate. The device , however acts as a one-dimensional Bragg diffraction grating and light which satisfies the Bragg condition , is reflected back along the guide at 180 to the original direction of propogation.

Integrated optical tevhniques are used in the fabrication of sources for optical fiber communication. The source however which is directly compatible with the planar wave guide structure is single mode injection

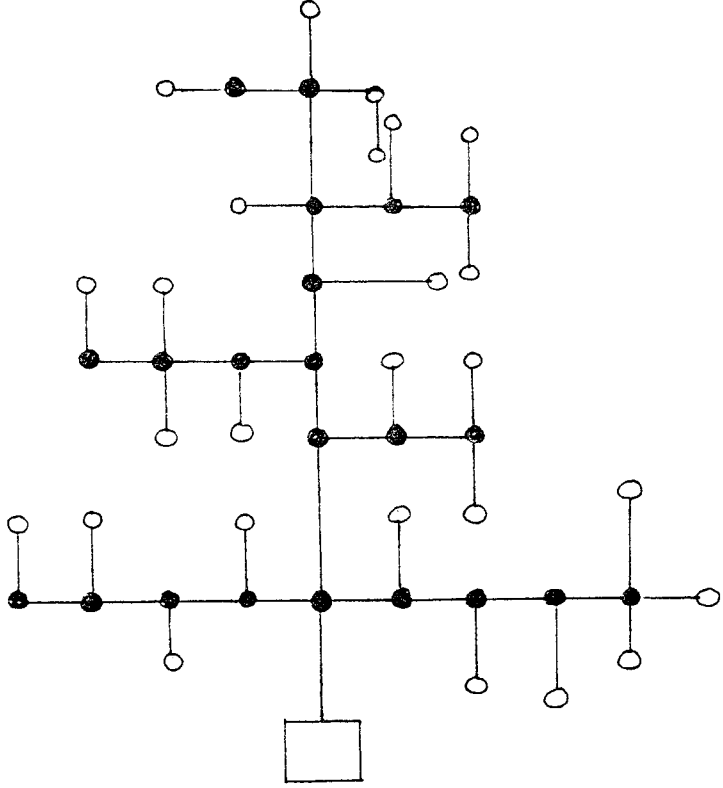
laser.

Bistable optical devices

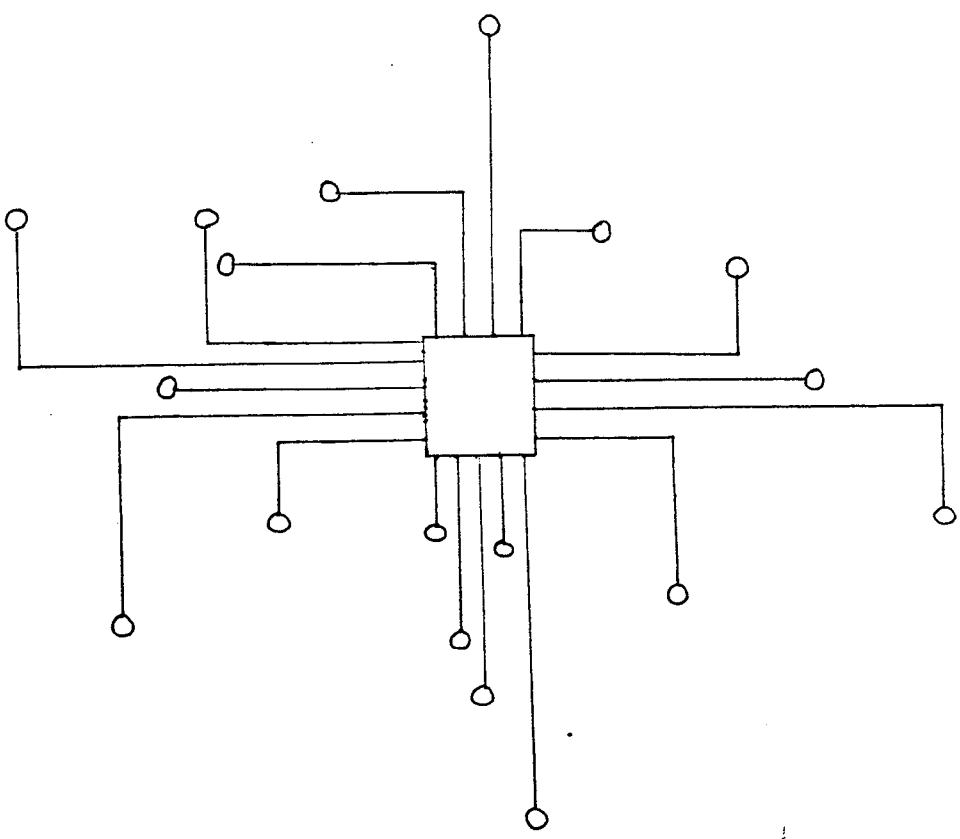
Bistable optical devices include optical logic and memory elements , power limiters and pulse shapers and A/D converters. An optical device may be made bistable when the optical transmission within it is nonlinear and there is feedback of the optical output to control this transmission.



RING NETWORK



TREE NETWORK



STAR NETWORK

Fig 7.1 : LOCAL AND RURAL NETWORK CONFIGURATIONS

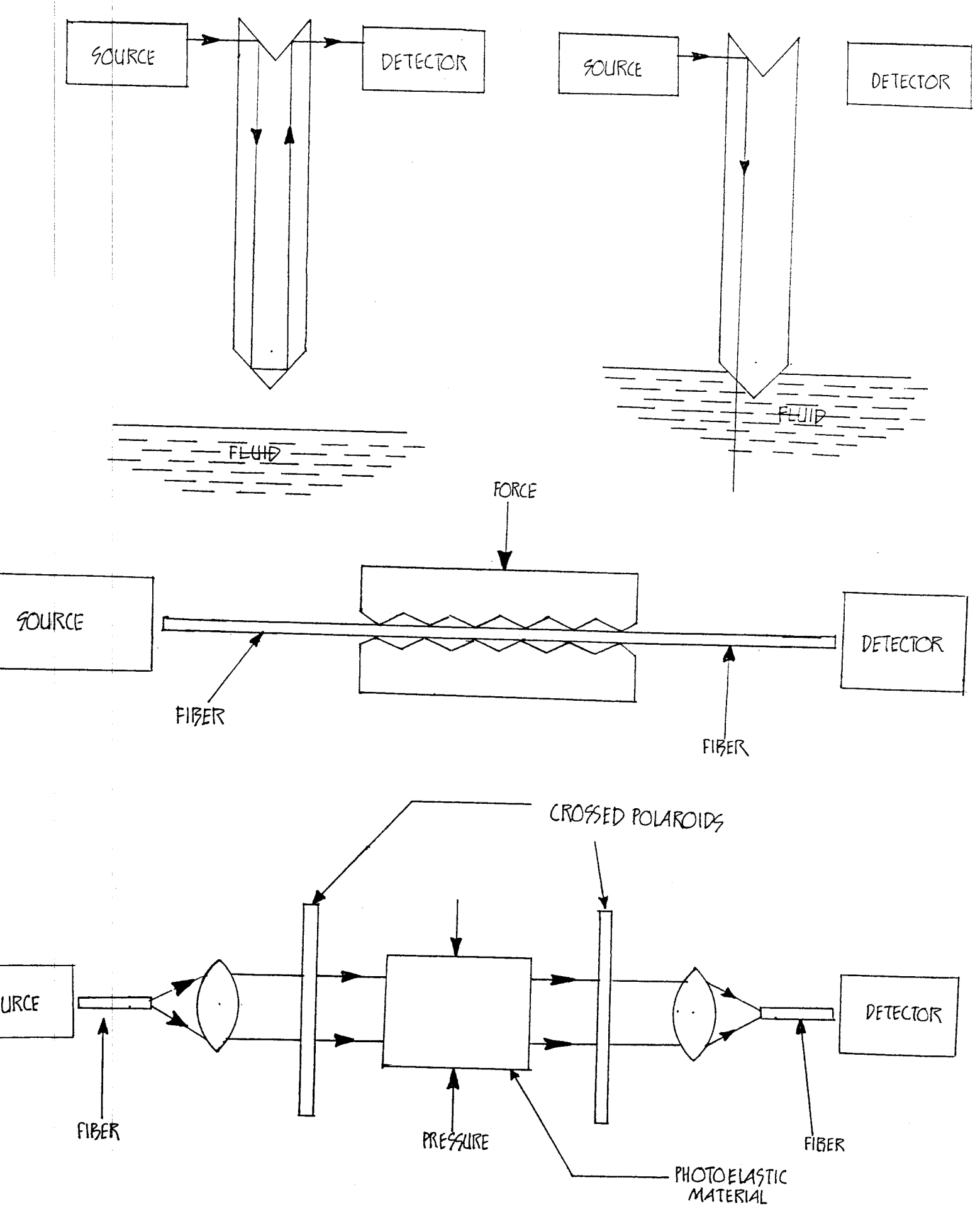


Fig 7.2 : FIBER OPTIC SENSORS

CHAPTER VIII

CONCLUSION AND FURTHER DEVELOPMENTS

CHAPTER 8

CONCLUSION AND FURTHER DEVELOPMENTS

An 8-channel digital audio link of 512Kbits/sec data rate and a software for fiber optic link simulation has been developed. A/D converter can work with a clock of 800KHz. The link works appreciably for a length of 30m, using drive currect of 25mA. A further increase in the trnsmission distance can be achieved by increasing the drive current to a maximum of 60mA which is the maximum current rating of the source used. Manchester coder and decoder are working properly. The sound reproduction at the receiver was very good. A back ground hum was heared if synchronization was not precise. As the bandwidth of the designed audio link is about 30Mbits/second, the system can be further developed to multiplex many more channels.

The software for link simulation can be modified incorporating colour commands to make the output attractive. The letter fonds can also be changed by modifying the programme. This software can be modified by including chractersitcs of fibers, sources & detectors of all manufacturers.

BIBLIOGRAPHY

BIBLIOGRAPHY

1. Robert J.Hoss, "FIBER OPTIC COMMUNICATIONS DESIGN HAND BOOK" - Prentice Hall International Editions; 1990.
2. Joseph C. Palais,"FIBER OPTIC COMMUNICATIONS" -Prentice Hall International Editions;1984.
3. Geird Keiser, "OPTICAL FIBER COMMUNICATIONS" -Mc Graw Hill Inc;1982.
4. Friedrick L. Allard, "FIBER OPTICS HAND BOOK" -Mc Graw Hill Inc;1990.
5. Harold B.Killen,"FIBER OPTIC COMMUNICATIONS" -Prentice Hall International Editions;1991.
6. CSELT,"OPTICAL FIBER COMMUNICATIONS" -Mc Graw Hill Company;1981.
7. B.S.Sonde ,"INTRODUCTION TO SYSTEM DESIGN USING INTEGRATED CIRCUITS"-Prentice Hall International Editions;1990.
8. John M.Senior, "OPTICAL FIBER COMMUNICATIONS-Principles and Practice" - Prentice Hall International Series;1985.
9. Jeff Hecht, "UNDERSTANDING FIBER OPTICS", -Howard W. Sams & Company;1987.
10. D.A.Hill,"FIBER OPTICS" -Business Books,1977.

APPENDIX

National Semiconductor

ADC0800 8-Bit A/D Converter

General Description

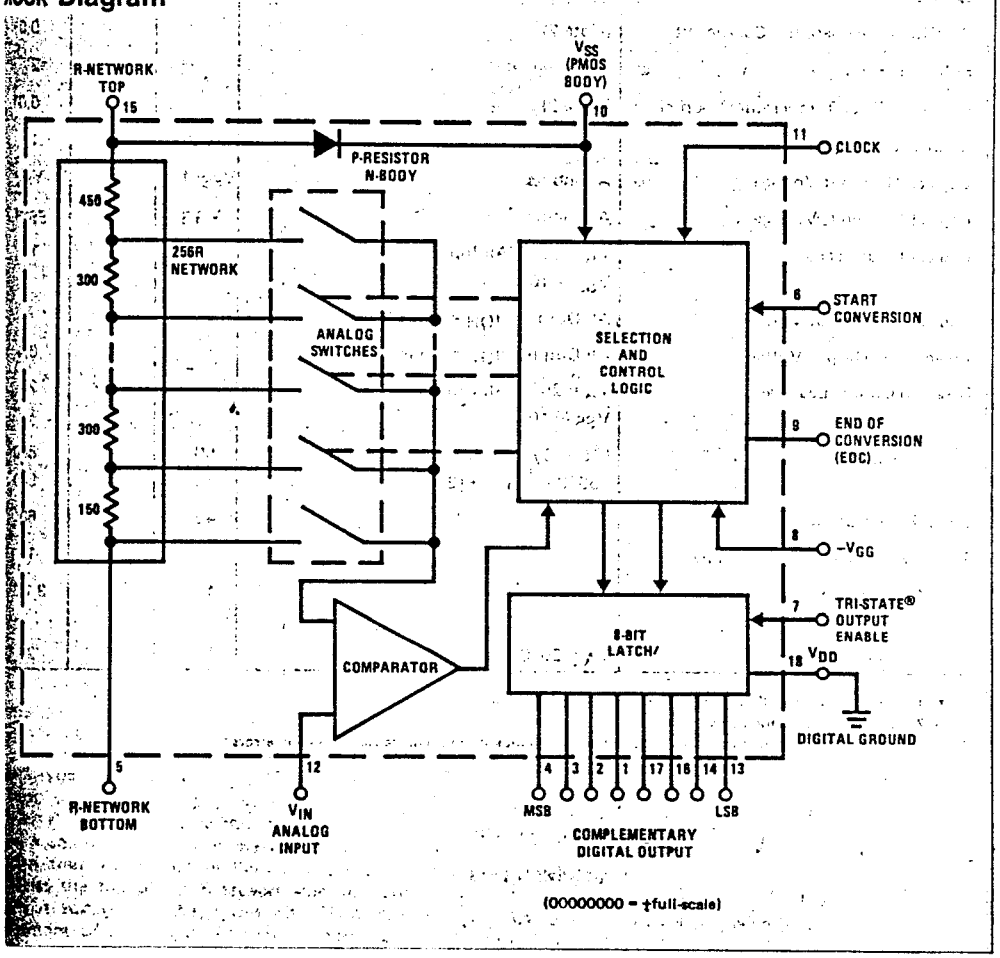
The ADC0800 is an 8-bit monolithic A/D converter using P-channel ion-implanted MOS technology. It contains a high input impedance comparator, 256 series resistors and analog switches, control logic and output latches. Conversion is performed using a successive approximation technique where the unknown analog voltage is compared to the resistor tie points using analog switches. When the appropriate tie point voltage matches the unknown voltage, conversion is complete and the digital outputs contain an 8-bit complementary binary word corresponding to the unknown. The binary output is TRI-STATE® to permit bussing on common data lines.

The ADC0800PD is specified over −55°C to +125°C and the ADC0800PCD is specified over 0°C to 70°C.

Features

- Low cost
- ±5V, 10V input ranges
- No missing codes
- Ratiometric conversion
- TRI-STATE outputs
- Fast — $T_C = 50\ \mu s$
- Contains output latches
- TTL compatible
- Supply voltages — 5 V_{DC} and −12 V_{DC}
- Resolution — 8 bits
- Linearity — ±1 LSB
- Conversion speed — 40 clock periods
- Clock range — 50 to 800 kHz

Block Diagram



Absolute Maximum Ratings

Supply Voltage (V_{DD})	V_{SS}–22V
Supply Voltage (V_{GG})	V_{SS}–22V
Voltage at Any Input	V_{SS} + 0.3V to V_{SS}–22V
Storage Temperature	150°C
Operating Temperature	
ADC0800PD	–55°C to +125°C
ADC0800PCD	0°C to +70°C
Lead Temperature (Soldering, 10 seconds)	300°C

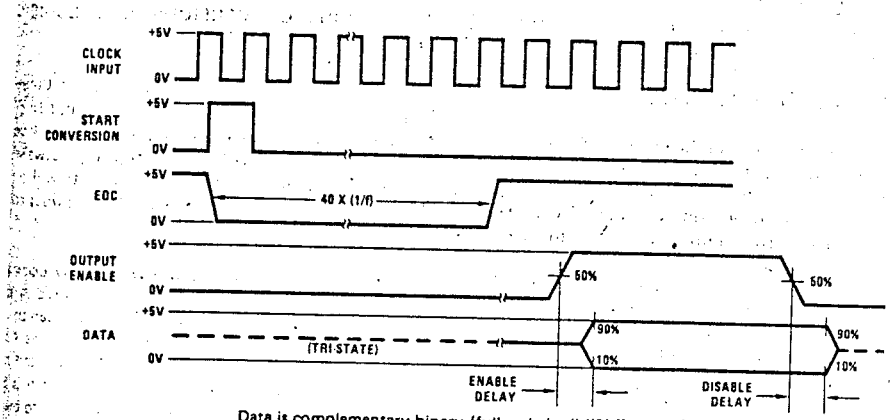
Electrical Characteristics

These specifications apply for V_{SS} = 5.0 V_{DC}, V_{GG} = –12.0 V_{DC}, V_{DD} = 0 V_{DC}, a reference voltage of 10.000 V the on-chip R-network ($V_{R\text{-}NETWORK\ TOP}$ = 5.000 V_{DC} and $V_{R\text{-}NETWORK\ BOTTOM}$ = –5.000 V_{DC}), and a quency of 800 kHz. For all tests, a 475Ω resistor is used from pin 5 to ground. Unless otherwise noted, these specifica over an ambient temperature range of –55°C to +125°C for the ADC0800PD and 0°C to +70°C for the ADC0800PC

PARAMETER	CONDITIONS	MIN	TYP	MAX
Non-Linearity	T_A = 25°C, (Note 1)			±1
	Over Temperature, (Note 1)			±2
Differential Non-Linearity				±1/2
Zero Error				±2
Zero Error Temperature Coefficient	(Note 2)			0.01
Full-Scale Error				±2
Full-Scale Error Temperature Coefficient	(Note 2)			0.01
Input Leakage				1
Logical "1" Input Voltage	All Inputs	V_{SS}–1.0		V_{SS}
Logical "0" Input Voltage	All Inputs	V_{GG}		V_{SS}–4.2
Logical Input Leakage	T_A = 25°C, All Inputs, V_{IL} = V_{SS} – 10V			1
Logical "1" Output Voltage	All Outputs, I_{OH} = 100 μA	2.4		
Logical "0" Output Voltage	All Outputs, I_{OL} = 1.6 mA			0.4
Disabled Output Leakage	T_A = 25°C, All Outputs, V_{OL} = V_{SS} @ 10V			2
Clock Frequency	0°C ≤ T_A ≤ +70°C	50		800
	–55°C ≤ T_A ≤ +125°C	100		500
Clock Pulse Duty Cycle		40		60
TRI-STATE Enable/Disable Time				1
Start Conversion Pulse	(Note 3)	1		3 1/2
Power Supply Current	T_A = 25°C			20

Note 1: Non-linearity specifications are based on best straight line.
Note 2: Guaranteed by design only.
Note 3: Start conversion pulse duration greater than 3 1/2 clock periods will cause conversion errors.

ning Diagram



Data is complementary binary (full scale is all "0's" output).

pplication Hints

ERATION

e ADC0800 contains a network with 256-300Ω istors in series. Analog switch taps are made at the ction of each resistor and at each end of the net-rk. In operation, a reference (10.00V) is applied ss this network of 256 resistors. An analog input gal is first compared to the center point of the ler via the appropriate switch. If V_{IN} is larger than $_{REF}/2$, the internal logic changes the switch points d now compares V_{IN} and 3/4 V_{REF}. This process, own as successive approximation, continues until the st match of V_{IN} and V_{REF}/N is made. N now defines pecific tap on the resistor network. When the conver-n is complete, the logic loads a binary word corres-nding to this tap into the output latch and an end of nversion (EOC) logic level appears. The output latches ld this data valid until a new conversion is completed d new data is loaded into the latches. The data transfer urs in about 200 ns so that valid data is present nually all the time. Conversion requires 40 clock riods. The device may be operated in the free run-g mode by connecting the Start Conversion line to g End of Conversion line. However, to ensure start-up der all possible conditions, an external Start Conver-n pulse is required during power up conditions.

EFERENCE

e reference applied across the 256 resistor network termines the analog input range. V_{REF} = 10.00V s the top of the R-network connected to 5V and the ttom connected to −5V gives a ±5V range. The erence can be level shifted between V_{SS} and V_{GG}. wever, the voltage, which is applied to the top of the twork (pin 15), must not exceed V_{SS} to prevent ward biasing the on-chip parasitic silicon diode ich exists between the P-diffused resistors (pin 15) d the N-type body (pin 10, V_{SS}). Use of a standard gle power supply for V_{SS} can cause problems, both e to initial voltage tolerance and changes over tem-rature. A solution is to power the V_{SS} line (15 mA k drain) from the output of the op amp which is o bias the top of the R-network (pin 15). The alog input voltage and the voltage which is applied the bottom of the R-network (pin 5) must be at least 7V above the $-V_{DD}$ supply voltage to insure adequate voltage drive to the analog switches.

Other reference voltages may be used (such as 10.24V). If a 5V reference is used, the analog range will be 5V and accuracy will be reduced by a factor of 2. Thus, for maximum accuracy, it is desirable to operate with at least a 10V reference. For TTL logic levels, this requires 5V and −5V for the R-network. CMOS can operate at the 10 V_{DC} V_{SS} level and a single 10 V_{DC} reference can be used. All digital voltage levels for both inputs and outputs will be from ground to V_{SS}.

ANALOG INPUT AND SOURCE RESISTANCE CONSIDERATIONS

The lead to the analog input (pin 12) should be kept as short as possible. Both noise and digital clock coupling to this input can cause conversion errors. To minimize any input errors, the following source resistance considerations should be noted:

For $R_s \leq 5k$	No analog input bypass capacitor required, although a 0.1 μF input bypass capacitor will prevent pick-up due to unavoidable series lead inductance.
For $5k < R_s \leq 20k$	A 0.1 μF capacitor from the input (pin 12) to ground should be used.
For $R_s > 20k$	Input buffering is necessary.

If the overall converter system requires lowpass filtering of the analog input signal, use a 20 kΩ or less series resistor for a passive RC section or add an op amp RC active lowpass filter (with its inherent low output resistance) to insure accurate conversions.

CLOCK COUPLING

The clock lead should be kept away from the analog input line to reduce coupling.

LOGIC INPUTS

The logical "1" input voltage swing for the Clock, Start Conversion and Output Enable should be (V_{SS} − 1.0V).

Application Hints (Continued)

CMOS will satisfy this requirement but a pull-up resistor should be used for TTL logic inputs.

RE-START AND DATA VALID AFTER EOC

The EOC line (pin 9) will be in the low state for a maximum of 40 clock periods to indicate "busy". A START pulse which occurs while the A/D is BUSY will reset the SAR and start a new conversion with the EOC signal remaining in the low state until the end of this new conversion. When the conversion is complete, the EOC line will go to the high voltage state. An additional 4 clock periods must be allowed to elapse after EOC goes high, before a new conversion cycle is requested. Start Conversion pulses which occur during this last 4 clock period interval may be ignored (see *Figures 1 and 2* for high speed operation). This is only a problem for high conversion rates and keeping the number of conversions per second less than $(1/44) \times f_{CLOCK}$ automatically guarantees proper operation. For example, for an 800 kHz clock, 18,000 conversions per second are allowed. The transfer of the new digital data to the output is initiated when EOC goes to the high voltage state.

POWER SUPPLIES

Standard supplies are V_{SS} = 5V, V_{GG} = −12V and V_{DD} = 0V. Device accuracy is dependent on stability of the reference voltage and has slight sensitivity to $V_{SS} - V_{GG}$. V_{DD} has no effect on accuracy. Noise spikes on the V_{SS} and V_{GG} supplies can cause improper conversion; therefore, filtering each supply with a 4.7 μF tantalum capacitor is recommended.

CONTINUOUS CONVERSIONS AND LOGIC CONTROL

Simply tying the EOC output to the Start Conversion input will allow continuous conversions, but an oscillation on this line will exist during the first 4 clock period after EOC goes high. Adding a D flip-flop between EOC (D input) to Start Conversion (Q output) will prevent the oscillation and will allow a stop/continuous control via the "clear" input.

To prevent missing a start pulse which may occur after EOC goes high and prior to the required 4 clock period time interval, the circuit of *Figure 1* can be used. The RS latch can be set at any time and the 4-bit shift register delays the application of the start pulse to the A/D by 4 clock periods. The RS latch is reset 1 clock period after the A/D EOC signal goes to the high voltage state. This circuit also provides a Start Conversion pulse to the A/D which is 1 clock period wide.

A second control logic application circuit is shown in *Figure 2*. This allows an asynchronous start pulse of arbitrary length less than T_C, continuously converting at a fixed high level and provides a single clock period start pulse to the A/D. The binary counter is loaded with a count of 11 when the start pulse to the A/D appears. Counting is inhibited until the EOC signal from the A/D goes high. A carry pulse is then generated 4 clock periods after EOC goes high and is used to reset the input RS latch. This carry pulse can be used to indicate that the conversion is complete, the data has transferred to the output buffers and the system is ready for the next conversion cycle.

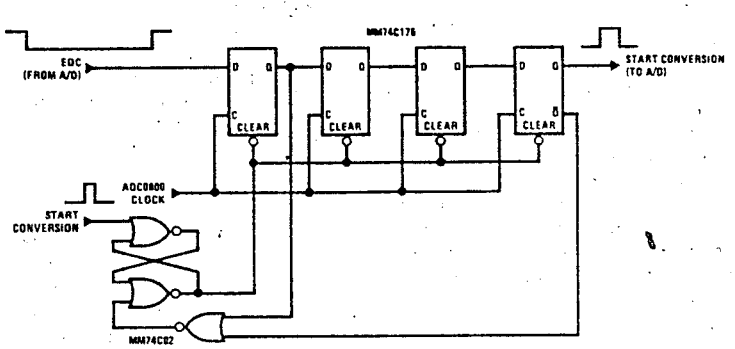


FIGURE 1. Delaying an Asynchronous Start Pulse

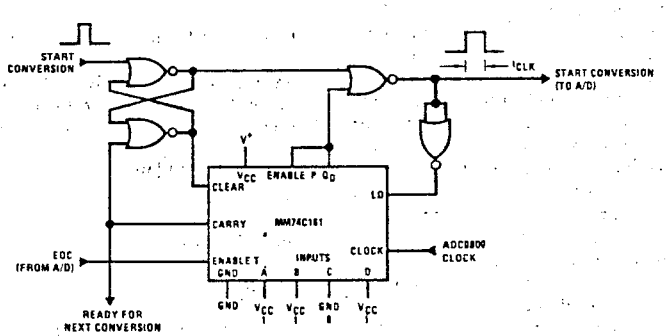


FIGURE 2. A/D Control Logic

lication Hints (Continued)

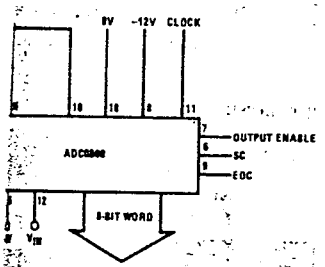
AND FULL-SCALE ADJUSTMENT

Adjustment: This is the offset voltage required at ottom of the R-network (pin 5) to make the 1111 to 11111110 transition when the input is 1/2 LSB (20 mV for a 10.24V scale). In most this can be accomplished by having a 1 kΩ pot on A resistor of 475Ω can be used as a non-adjustable pproximation from pin 5 to ground.

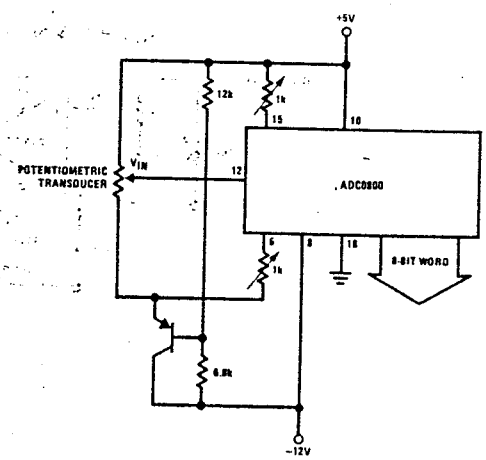
Full-Scale Adjustment: This is the offset voltage required at the top of the R-network (pin 15) to make the 00000001 to 00000000 transition when the input voltage is 1 1/2 LSB from full-scale (60 mV less than full-scale for a 10.24V scale). This voltage is guaranteed to be within 2 LSB for the ADC0800. In most cases, this can be accomplished by having a 1 kΩ pot on pin 15.

ical Applications

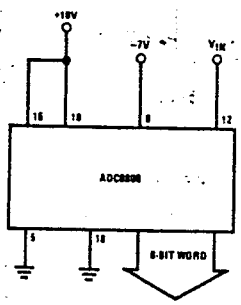
General Connection



Ratiometric Input Signal with Tracking Reference



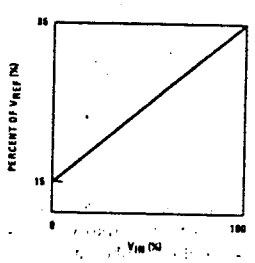
Hi-Voltage CMOS Output Levels

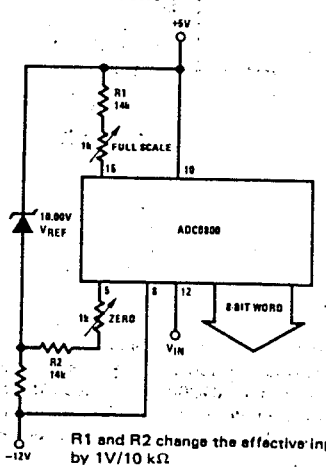


0V to 10V V_{IN} range
0V to 10V output levels

Level Shifted Zero and Full-Scale for Transducers

Level Shifted Input Signal Range

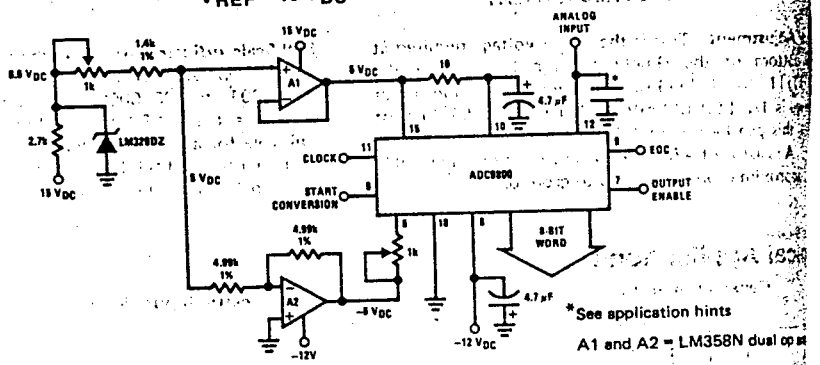




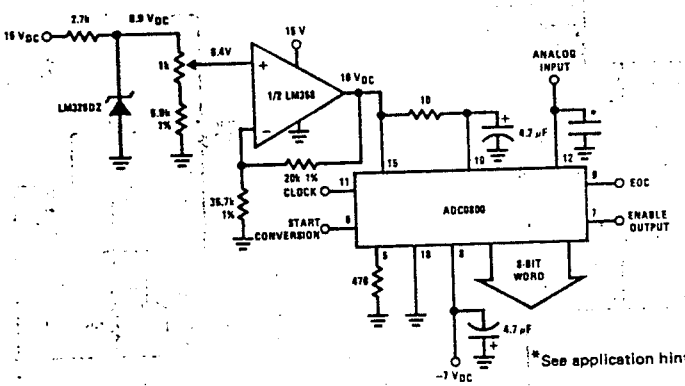
R1 and R2 change the effective input range by 1V/10 kΩ

Typical Applications (Continued)

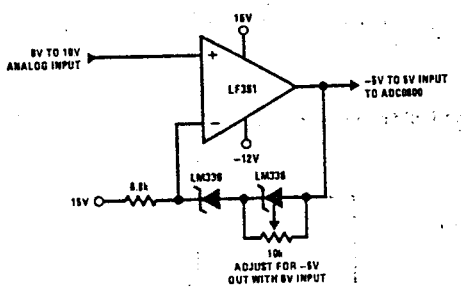
V_{REF} = 10 V_{DC} With TTL Logic Levels



V_{REF} = 10 V_{DC} With 10V CMOS Logic Levels



Input Level Shifting



- Permits TTL compatible outputs with 0V to 10V input range (0V to −10V input range achieved by reversing polarity of zener diodes and returning the 6.8k resistor to V^-).

MICROPROCESSOR INTERFACE

Figure 3 and the following sample program are included to illustrate both hardware and software requirements to allow output data from the ADC0800 to be loaded into the memory of a microprocessor system. For this example, National's INS8060, SC/MP II, microprocessor has been used.

The sample program, as shown, will start the conv load the converter's output data into the accumu keep track of the number of data bytes entered plement the data and store this data into suc memory locations. After 256 bytes have been st the control jumps to the user's program when

Typical Applications (Continued)

any of the data entered will be implemented. A more practical program whereby each data byte entered will be processed before another entry is made can easily be done by jumping back to the user's program at the end of the interrupt routine (where the data is loaded into the accumulator and stored in memory). The end of the user's program should provide a jump back to the INITIALIZE statement to start a new conversion and generate a new data entry.

The following arbitrarily chosen addresses and pointer assignments are used in this example:

Pointer 1 — WORD COUNT (ADDR:0100)
Also used to point to the A/D converter at address 0500 for this example when data is to be entered.

Pointer 2 — ENTERED DATA (ADDR's: 0200→02FF)
Data is stored in 2's complement binary form, i.e, 01111111 → +full-scale and 10000000 → – full-scale.

Pointer 3 — LOAD DATA SUBROUTINE (starts at ADDR:0300)
Executed when an EOC signal generates an interrupt request via sense A after an IEN (interrupt enable) instruction.

The address for the converter (0500) is unique for this particular sample program but may not be in a user's system so a different converter address must be used. Note that in *Figure-3* ADX and ADY for the address decode circuitry would be address bits ADB10 and ADB8 (pins 35 and 33 on the SC/MP II package) for converter address 0500.

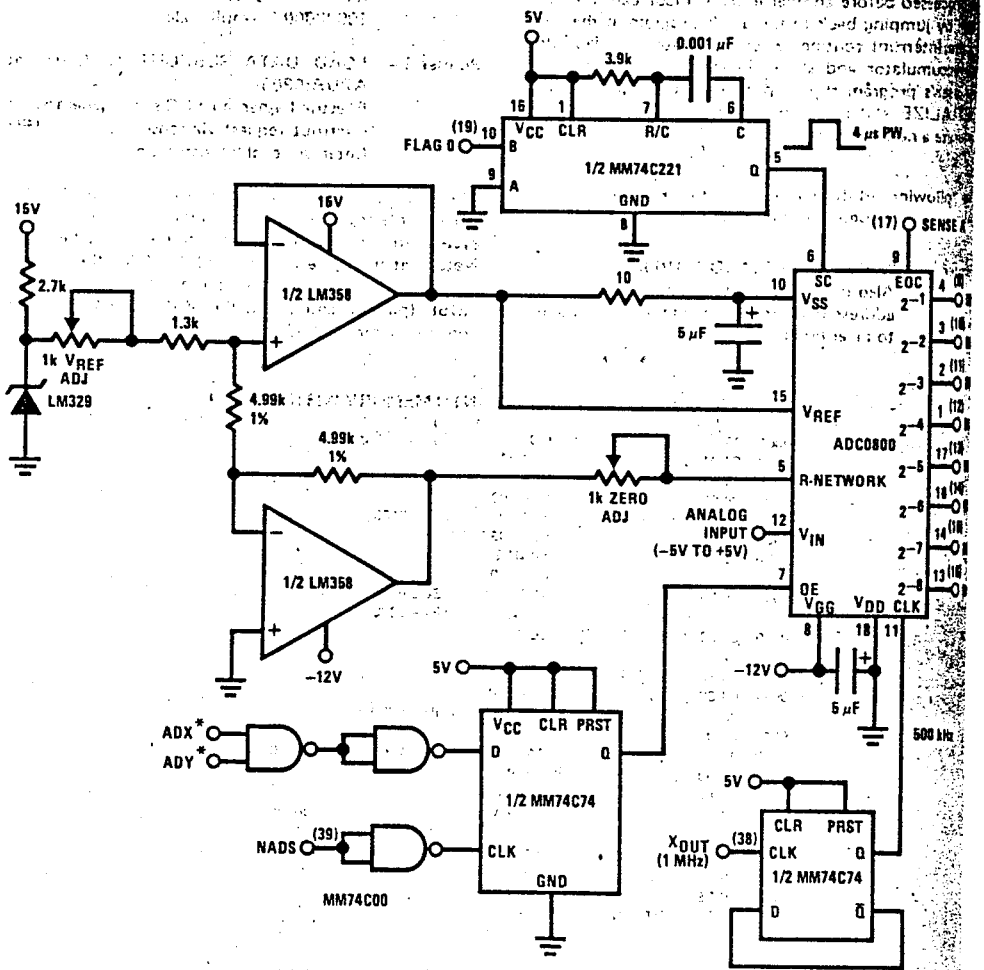
SAMPLE PROGRAM TO LOAD DATA INTO MEMORY WITH SC/MP II.

```
0001  08       START:    NOP
0002  C4 01               LDIX'01
0004  35                 XPAH 1
0005  C4 00               LDIX'00
0007  31                 XPAL 1      ;P1 = 0100
0008  C4 02               LDIX'02
000A  36                 XPAH 2
000B  C4 00               LDIX'00
000D  C9 00               ST(P1)      ;Zero word count (P1)
000F  32                 XPAL 2      ;P2 = 0200
0010  C4 03               LDIX'03
0012  37                 XPAH 3
0013  08       INITIALIZE: NOP
0014  C4 00               LDIX'00
0016  33                 XPAL 3      ;P3 = 0300
0017  C4 01               LDIX'01
0019  07                 CAS         ;Starts converter via flag 0
001A  C1 00               LD (P1)
001C  F4 FF               XRIX'FF'
001E  98 05               JZ DTA IN   ;Test to see if word count is FF,
                                       if so, jump to DTA IN
0020  05                 IEN         ;Enables INTERRUPT
0021  08       LOOP:     NOP
0022  90 FE               JMP LOOP    ;Loop until EOC
0024  08       DTA IN:   NOP

                                     ;User program to process data

                :DATA ENTRY SUBROUTINE
0300  08       DATA IN SR: NOP
0301  A9 00               ILD (P1)    ;Increment word count
0303  C4 05               LDIX'05
0305  36                 XPAH 1      ;P1 will point to converter
0306  C1 00               LD (P1)     ;Converter data loaded into
                                       accumulator
0308  F4 7F               XRIX'7F'    ;Put data in 2's complement form
030A  CE 01               ST @ 1(P2)  ;Store data
030C  C4 00               LDIX'00
030E  07                 CAS         ;Resets flag 0
030F  C4 01               LDIX'01
0311  35                 XPAH 1      ;Resets P1 to point at word count
0312  C4 13               LDIX'13
0314  33                 XPAL 3
0315  3F                 XPPC 3      ;Return to INITIALIZE to start a
                                       new conversion
```

Typical Applications (Continued)



- Setting flag 0 (FLG0 = 1) with software, starts conversion (FLG0 must be cleared before another conversion can be initiated)
- With interrupt enabled an EOC will force an interrupt. Interrupt subroutine should load converter data into the accumulator.
- Output data is in complementary offset binary form
- Numbers in parentheses denote pin numbers of SC/MP chip

*ADX and ADY can be any of the address lines but they must be high *only* at the time the converter output data is to be put on the data bus (i.e., the converter must have its own unique address)

FIGURE 3. Interfacing to the SC/MP II Microprocessor

ical Applications (Continued)

ING THE A/D CONVERTER

are many degrees of complexity associated with an A/D converter. One of the simplest tests is to a known analog input voltage to the converter LED's to display the resulting digital output shown in *Figure 4*. Note that the LED drivers the digital output of the A/D converter to provide ay display. A lab DVM can be used if a precision source is not available. After adjusting the zero ull-scale, any number of points can be checked, ired.

se of testing, a 10.24 V_{DC} reference is recom- ed for the A/D converter. This provides an LSB of V (10.240/256). To adjust the zero of the A/D, an input voltage of 1/2 LSB or 20 mV should be applied and the zero adjust potentiometer should be set to provide a flicker on the LSB LED readout with all the other display LEDs OFF.

To adjust the full-scale adjust potentiometer, an analog input which is 1 1/2 LSB less than the reference (10.240–0.060 or 10.180 V_{DC}) should be applied to the analog input and the full-scale adjusted for a flicker on the LSB LED, but this time with all the other LEDs ON.

A complete circuit for a simple A/D tester is shown in *Figure 5*. Note that the clock input voltage swing and the digital output voltage swings are from 0V to 10.24V. The MM74C901 provides a voltage translation to 5V operation and also the logic inversion so the readout LEDs are in binary.

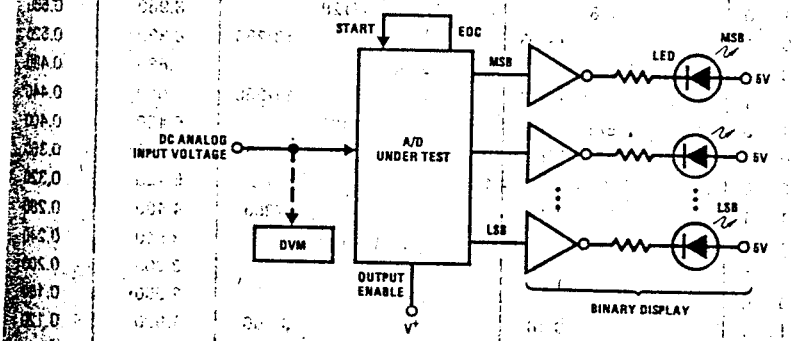


FIGURE 4. Basic A/D Tester

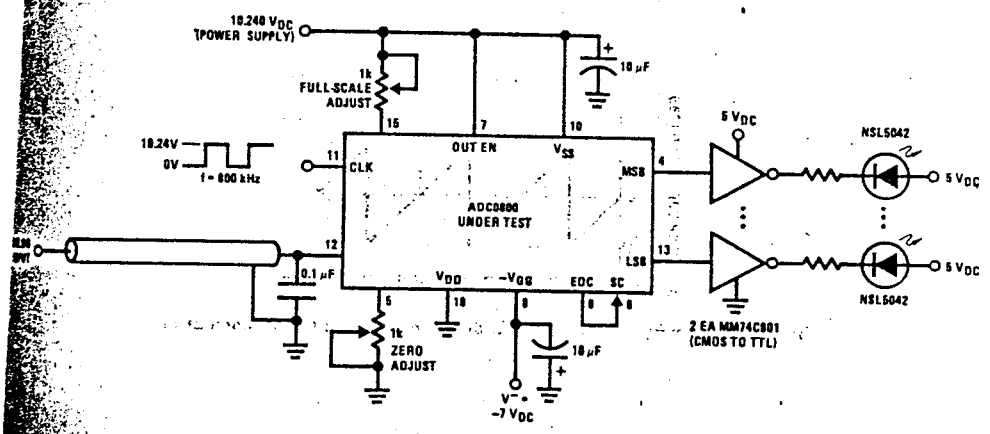


FIGURE 5. Complete Basic Tester Circuit

Typical Applications (Continued)

The digital output LED display can be decoded by dividing the 8 bits into the 4 most significant bits and 4 least significant bits. Table I shows the fractional binary equivalent of these two 8-bit groups. By adding the decoded voltages which are obtained from the column: "Input Voltage Value with a 10.240 V_{REF}" of both the MS and LS groups, the value of the digital display can be determined. For example, for an output LED display of "1011 0110" or "B6" (in hex) the voltage values from the table are 7.04 + 0.24 or 7.280 V_{DC}. These voltage values represent the values of a perfect A/D converter. The input voltage to change by ±1/2 LSB (±20 mV), the "quantization uncertainty" of an A/D, to obtain an output digital change. The effects of this quantization error have accounted for in the interpretation of the test A plot of this natural error source is shown in Fig where, for clarity, both the analog input voltage and error voltage are normalized to LSBs.

TABLE I. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY	FRACTIONAL BINARY VALUE FOR		INPUT VOLTAGE VALUE WITH 10.24 V_{REF}	
		MS GROUP	LS GROUP	MS GROUP	LS GROUP
F	1 1 1 1	15/16	15/256	9.600	0.600
E	1 1 1 0	7/8	7/128	8.960	0.560
D	1 1 0 1	13/16	13/256	8.320	0.520
C	1 1 0 0	3/4	3/64	7.680	0.480
B	1 0 1 1	11/16	11/256	7.040	0.440
A	1 0 1 0	5/8	5/128	6.400	0.400
9	1 0 0 1	9/16	9/256	5.760	0.360
8	1 0 0 0	1/2	1/32	5.120	0.320
7	0 1 1 1	7/16	7/256	4.480	0.280
6	0 1 1 0	3/8	3/128	3.840	0.240
5	0 1 0 1	5/16	5/256	3.200	0.200
4	0 1 0 0	1/4	1/64	2.560	0.160
3	0 0 1 1	3/16	3/256	1.920	0.120
2	0 0 1 0	1/8	1/128	1.280	0.080
1	0 0 0 1	1/16	1/256	0.640	0.040
0	0 0 0 0			0	0

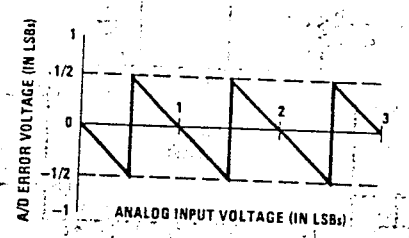


FIGURE 6. Error Plot of a Perfect A/D Showing Effects of Quantization Error

...ical Applications (Continued)

...low speed ramp generator can also be used to sweep ...analog input voltage and the LED outputs will ...ide a binary counting sequence from zero to full-...ale.

...e techniques described so far are suitable for an ...ineering evaluation or a quick check on performance. ...r a higher speed test system, or to obtain plotted ...a digital-to-analog converter is needed for the ...st set-up. An accurate 10-bit DAC can serve as the ...cision voltage source for the A/D. Errors of the A/D ...der test can be provided as either analog voltages or ...ferences in two digital words.

...basic A/D tester which uses a DAC and provides the ...or as an analog output voltage is shown in *Figure 7*. ...e 2 op amps can be eliminated if a lab DVM with a ...merical subtraction feature is available to directly ...adout the difference voltage, "A–C". The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis). The construction details of a tester of this type are provided in the NSC application note AN-179, "Analog-to-Digital Converter Testing".

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 8* where the output code transitions can be detected as the 10-bit DAC is incremented. This provides 1/4 LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

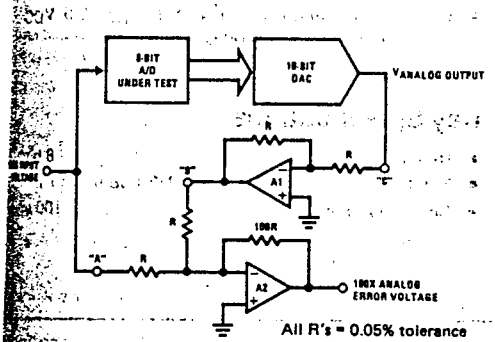


FIGURE 7. A/D Tester with Analog Error Output

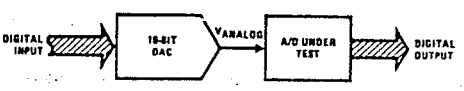
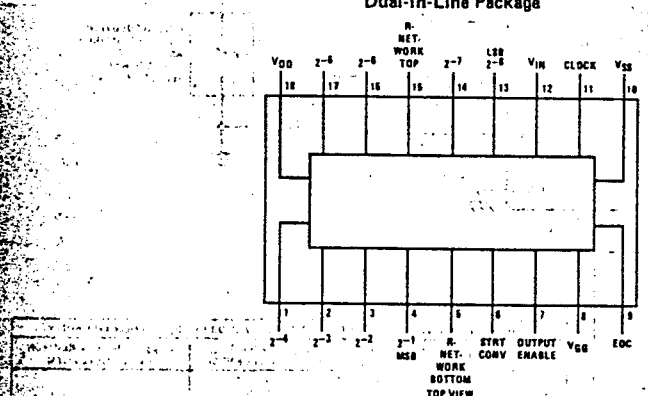


FIGURE 8. Basic "Digital" A/D Tester

Connection Diagram

Dual-In-Line Package



Order Number ADC0800PD (–55°C to +125°C)
or ADC0800PCD (0°C to +70°C)
See NS Package D18A

National Semiconductor

A to D, D to A

DAC0800, DAC0801, DAC0802 8-Bit Digital-to-Analog Converters

General Description

The DAC0800 series are monolithic 8-bit high-speed current-output digital-to-analog converters (DAC) featuring typical settling times of 100 ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC0800 series also features high compliance complementary current outputs to allow differential output voltages of 20 Vp-p with simple resistor loads as shown in *Figure 1*. The reference-to-full-scale current matching of better than ±1 LSB eliminates the need for full-scale trims in most applications while the nonlinearities of better than ±0.1% over temperature minimizes system error accumulations.

The noise immune inputs of the DAC0800 series will accept TTL levels with the logic threshold pin, V_{LC}, pin 1 grounded. Simple adjustments of the V_{LC} potential allow direct interface to all logic families. The performance and characteristics of the device are essentially unchanged over the full ± 4.5V to ±18V power supply range; power dissipation is only 33 mW with ±5V supplies and is independent of the logic input states.

The DAC0800, DAC0802, DAC0800C, DAC0801C and DAC0802C are a direct replacement for the DAC-08, DAC-08A, DAC-08C, DAC-08E and DAC-08H, respectively.

Features

- Fast settling output current — 100 ns
- Full scale error — ±1 LSB
- Nonlinearity over temperature — ±0.1%
- Full scale current drift — ±10 ppm/°C
- High output compliance — −10V to +18V
- Complementary current outputs
- Interface directly with TTL, CMOS, PMOS and others
- 2 quadrant wide range multiplying capability
- Wide power supply range — ±4.5V to ±18V
- Low power consumption — 33 mW at ±5V
- Low cost

Typical Applications

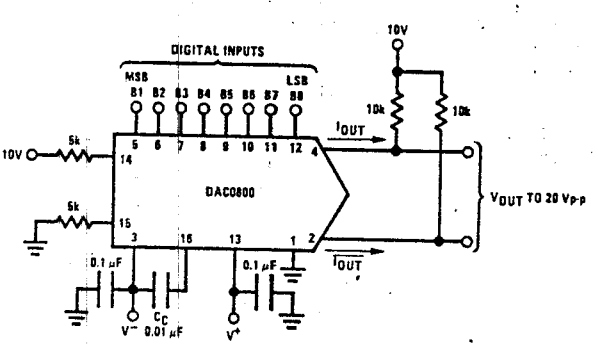
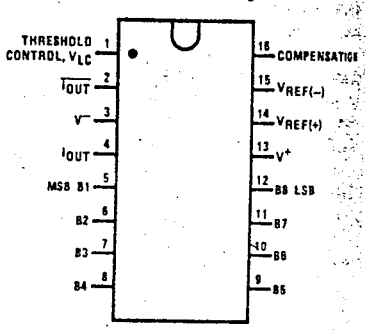


FIGURE 1. ±20 Vp-p Output Digital-to-Analog Converter

Connection Diagram

Dual-In-Line Package



TOP VIEW

Ordering Information

NON LINEARITY	TEMPERATURE RANGE	ORDER NUMBERS*					
		D PACKAGE (D16C)		J PACKAGE (J16A)		N PACKAGE (N16A)	
±0.1% FS	−55°C ≤ T_A ≤ +125°C	DAC0802LD	DAC-08AQ				
±0.1% FS	0°C ≤ T_A ≤ +70°C			DAC0802LCJ	DAC-08HQ	DAC0802LCN	DAC-08HP
±0.19% FS	−55°C ≤ T_A ≤ +125°C	DAC0800LD	DAC-08Q				
±0.19% FS	0°C ≤ T_A ≤ +70°C			DAC0800LCJ	DAC-08EQ	DAC0800LCN	DAC-08EP
±0.39% FS	0°C ≤ T_A ≤ +70°C			DAC0801LCJ	DAC-08CQ	DAC0801LCN	DAC-08CP

Note. Devices may be ordered by using either order number.

solute Maximum Ratings

...t Voltage	±18V or 36V
...e Dissipation (Note 1)	500 mW
...ence Input Differential Voltage (V14 to V15)	V^- to V^+
...ence Input Common-Mode Range (V14, V15)	V^- to V^+
...ence Input Current	5 mA
...g Inputs	V^- to V^- plus 36V
...g Current Outputs	*Figure 24*
...g Temperature	−65°C to +150°C
...Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Temperature (T_A)			
DAC0802L	−55	+125	°C
DAC0800L	−55	+125	°C
DAC0800LC	0	+70	°C
DAC0801LC	0	+70	°C
DAC0802LC	0	+70	°C

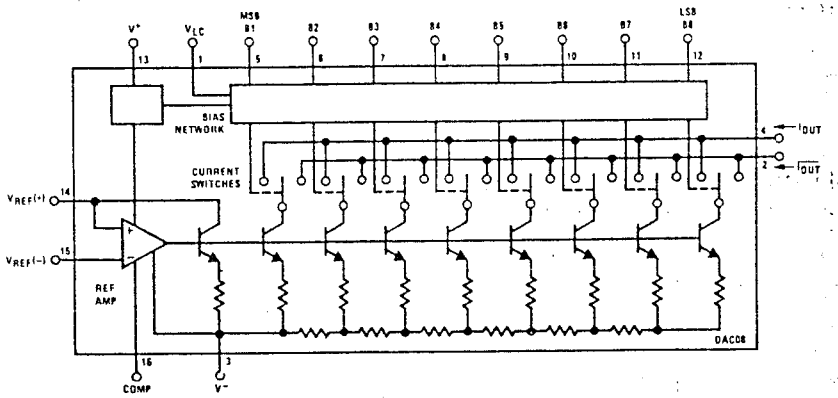
...trical Characteristics (V_S = ±15V, I_{REF} = 2 mA, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified.

...put characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.)

PARAMETER	CONDITIONS	DAC0802L/ DAC0802LC			DAC0800L/ DAC0800LC			DAC0801LC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Resolution		8	8	8	8	8	8	8	8	8	Bits
Monotonicity		8	8	8	8	8	8	8	8	8	Bits
Nonlinearity				±0.1			±0.19			±0.39	%FS
Settling Time	To ±1/2 LSB, All Bits Switched "ON" or "OFF", T_A = 25°C		100	135					100	150	ns
	DAC0800L					100	135				ns
	DAC0800LC					100	150				ns
t_{PHL} Propagation Delay	T_A = 25°C										
Each Bit			35	60		35	60		35	60	ns
All Bits Switched			35	60		35	60		35	60	ns
Full Scale Tempco			±10	±50		±10	±50		±10	±80	ppm/°C
Output Voltage Compliance	Full Scale Current Change < 1/2 LSB, R_{OUT} > 20 MΩ Typ	−10		18	−10		18	−10		18	V
Full Scale Current	V_{REF} = 10.000V, R14 = 5.000 kΩ R15 = 5.000 kΩ, T_A = 25°C	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Scale Symmetry	$I_{FS4} - I_{FS2}$		±0.5	±4.0		±1	±8.0		±2	±16	µA
Zero Scale Current			0.1	1.0		0.2	2.0		0.2	4.0	µA
Output Current Range	V^- = −5V	0	2.0	2.1	0	2.0	2.1	0	2.0	2.1	mA
	V^- = −8V to −18V	0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	mA
Logic Input Levels											
Logic "0"	V_{LC} = 0V			0.8			0.8			0.8	V
Logic "1"		2.0			2.0			2.0			V
Logic Input Current	V_{LC} = 0V										
Logic "0"	−10V ≤ V_{IN} ≤ +0.8V		−2.0	−10		−2.0	−10		−2.0	−10	µA
Logic "1"	2V ≤ V_{IN} ≤ +18V		0.002	10		0.002	10		0.002	10	µA
Logic Input Swing	V^- = −15V	−10		18	−10		18	−10		18	V
Logic Threshold Range	V_S = ±15V	−10		13.5	−10		13.5	−10		13.5	V
Reference Bias Current			−1.0	−3.0		−1.0	−3.0		−1.0	−3.0	µA
Reference Input Slew Rate	*(Figure 24)*	4.0	8.0		4.0	8.0		4.0	8.0		mA/µs
Power Supply Sensitivity	4.5V ≤ V^+ ≤ 18V		0.0001	0.01		0.0001	0.01		0.0001	0.01	%/%
	−4.5V ≤ V^- ≤ 18V I_{REF} = 1 mA		0.0001	0.01		0.0001	0.01		0.0001	0.01	%/%
Power Supply Current	V_S = ±5V, I_{REF} = 1 mA										
			2.3	3.8		2.3	3.8		2.3	3.8	mA
			−4.3	−5.8		−4.3	−5.8		−4.3	−5.8	mA
	V_S = 5V, −15V, I_{REF} = 2 mA										
			2.4	3.8		2.4	3.8		2.4	3.8	mA
			−6.4	−7.8		−6.4	−7.8		−6.4	−7.8	mA
	V_S = ±15V, I_{REF} = 2 mA										
			2.5	3.8		2.5	3.8		2.5	3.8	mA
			−6.5	−7.8		−6.5	−7.8		−6.5	−7.8	mA
Power Dissipation	±5V, I_{REF} = 1 mA		33	48		33	48		33	48	mW
	5V, −15V I_{REF} = 2 mA		108	136		108	136		108	136	mW
	±15V, I_{REF} = 2 mA		135	174		135	174		135	174	mW

...e 1: The maximum junction temperature of the DAC0800, DAC0801 and DAC0802 is 125°C. For operating at elevated temperatures, devices ...e dual-in-line J or D package must be derated based on a thermal resistance of 100°C/W, junction to ambient, 175°C/W for the molded dual-...e N package.

Block Diagram



Equivalent Circuit

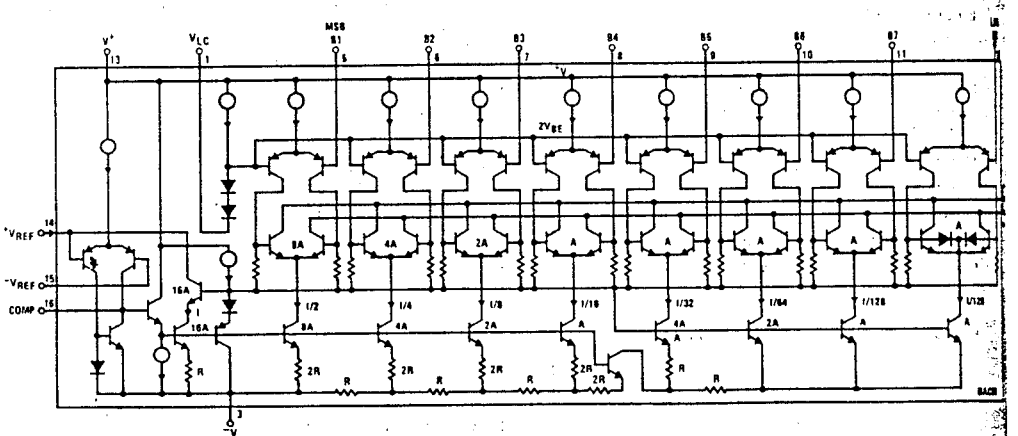


FIGURE 2

pical Performance Characteristics

Full Scale Current vs Reference Current

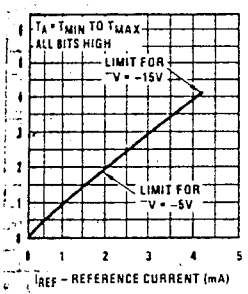


FIGURE 3

LSB Propagation Delay vs I_{FS}

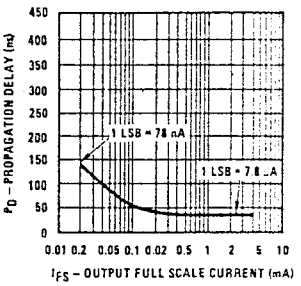
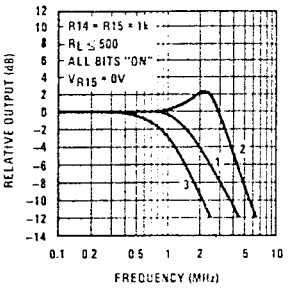


FIGURE 4

Reference Input Frequency Response



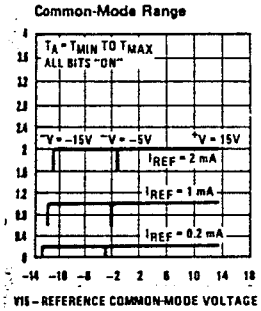
Curve 1: C_C = 15 pF, V_{IN} = 2 Vp-p centered at 1V.

Curve 2: C_C = 15 pF, V_{IN} = 50 mVp-p centered at 200 mV.

Curve 3: C_C = 0 pF, V_{IN} = 100 mVp-p at 0V and applied through 50 Ω connected to pin 14. 2V applied to R14.

FIGURE 5

Reference Amp Common-Mode Range



Note. Positive common-mode range is always (V+) – 1.5V.

FIGURE 6

Logic Input Current vs Input Voltage

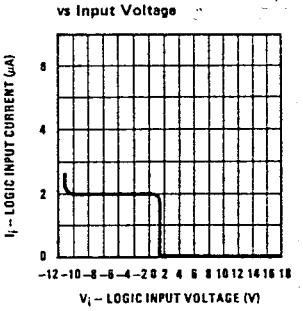


FIGURE 7

$V_{TH} - V_{LC}$ vs Temperature

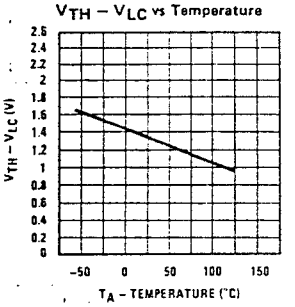


FIGURE 8

Output Current vs Output Voltage (Output Voltage Compliance)

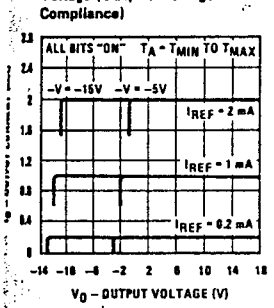


FIGURE 9

Output Voltage Compliance vs Temperature

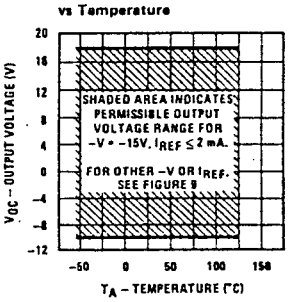
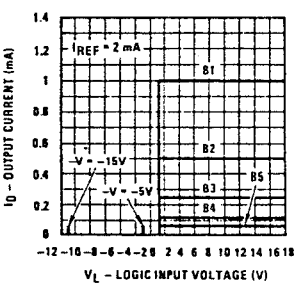


FIGURE 10

Bit Transfer Characteristics



Note. B1–B8 have identical transfer characteristics. Bits are fully switched with less than 1/2 LSB error, at less than ±100 mV from actual threshold. These switching points are guaranteed to lie between 0.8 and 2V over the operating temperature range (V_{LC} = 0V).

FIGURE 11

Typical Performance Characteristics (Continued)

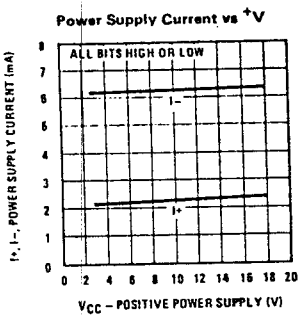


FIGURE 12

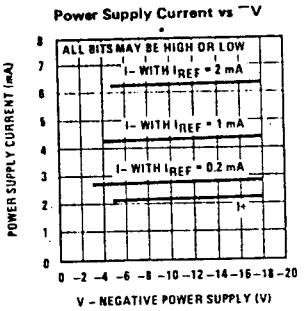


FIGURE 13

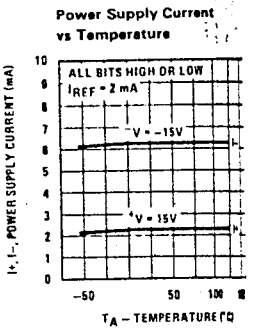
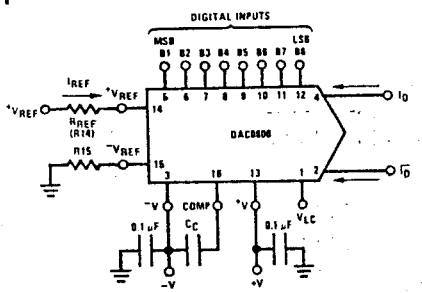


FIGURE 14

Typical Applications (Continued)



$$I_{FS} \approx \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$$

$I_O + \overline{I_O} = I_{FS}$ for all logic states

For fixed reference, TTL operation, typical values are:

$V_{REF} = 10.000V$
$R_{REF} = 5.000k$
$R15 \approx R_{REF}$
$C_C = 0.01\ \mu F$
$V_{LC} = 0V$ (Ground)

FIGURE 15. Basic Positive Reference Operation

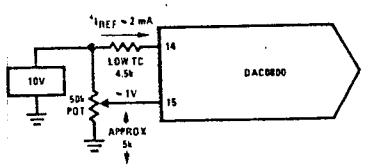
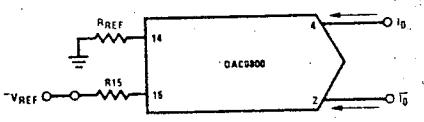


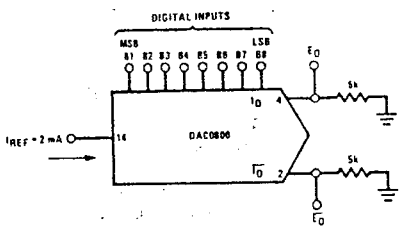
FIGURE 16. Recommended Full Scale Adjustment Circuit



$$I_{FS} \approx \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

Note. R_{REF} sets I_{FS}; R15 is for bias current cancellation

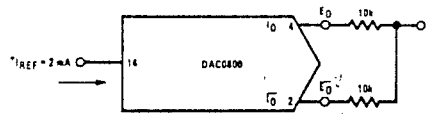
FIGURE 17. Basic Negative Reference Operation



	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$ mA	E_O	$\overline{E_O}$
Full Scale	1	1	1	1	1	1	1	1	1.992	0.000	−9.960	0.000
Full Scale−LSB	1	1	1	1	1	1	1	0	1.984	0.008	−9.920	−0.040
Half Scale+LSB	1	0	0	0	0	0	0	1	1.008	0.984	−5.040	−4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	0.992	−5.000	−4.960
Half Scale−LSB	0	1	1	1	1	1	1	1	0.992	1.000	−4.960	−5.000
Zero Scale+LSB	0	0	0	0	0	0	0	1	0.008	1.984	−0.040	−9.920
Zero Scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	−9.960

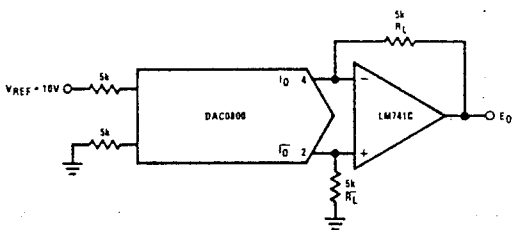
FIGURE 18. Basic Unipolar Negative Operation

...ical Applications (Continued)



	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
Pos. Full Scale	1	1	1	1	1	1	1	1	−9.920	+10.000
Pos. Full Scale−LSB	1	1	1	1	1	1	1	0	−9.840	+9.920
Zero Scale+LSB	1	0	0	0	0	0	0	1	−0.080	+0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero Scale−LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg. Full Scale+LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
Neg. Full Scale	0	0	0	0	0	0	0	0	+10.000	−9.920

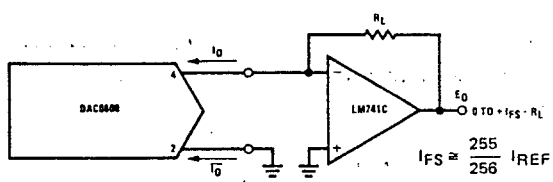
FIGURE 19. Basic Bipolar Output Operation



If $R_L = \overline{R_L}$ within ±0.05%, output is symmetrical about ground

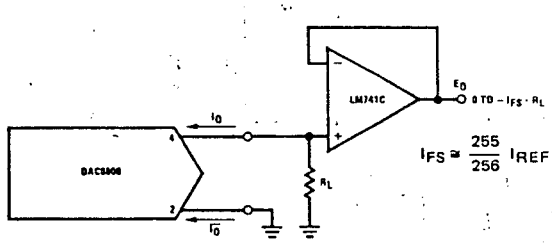
	B1	B2	B3	B4	B5	B6	B7	B8	E_O
Pos. Full Scale	1	1	1	1	1	1	1	1	+9.920
Pos. Full Scale−LSB	1	1	1	1	1	1	1	0	+9.840
(+) Zero Scale	1	0	0	0	0	0	0	0	+0.040
(−) Zero Scale	0	1	1	1	1	1	1	1	−0.040
Neg. Full Scale+LSB	0	0	0	0	0	0	0	1	−9.840
Neg. Full Scale	0	0	0	0	0	0	0	0	−9.920

FIGURE 20. Symmetrical Offset Binary Operation



For complementary output (operation as negative logic DAC), connect inverting input of op amp to $\overline{I_O}$ (pin 2), connect I_O (pin 4) to ground.

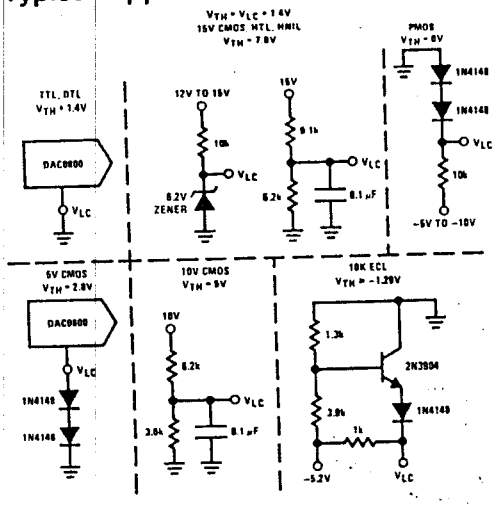
FIGURE 21. Positive Low Impedance Output Operation



For complementary output (operation as a negative logic DAC) connect non-inverting input of op amp to $\overline{I_O}$ (pin 2); connect I_O (pin 4) to ground.

FIGURE 22. Negative Low Impedance Output Operation

Typical Applications (Continued)



Note. Do not exceed negative logic input range of DAC.

FIGURE 23. Interfacing with Various Logic Families

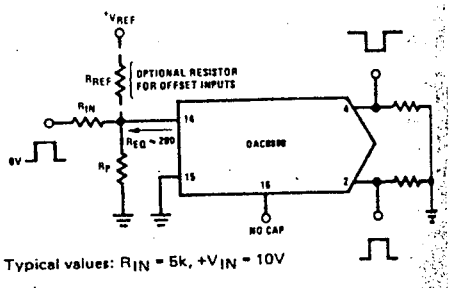
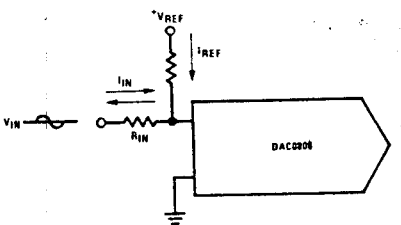
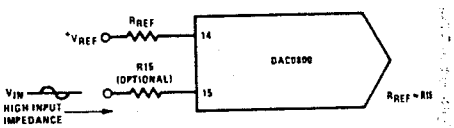


FIGURE 24. Pulsed Reference Operation



(a) $I_{REF} \geq$ peak negative swing of I_{IN}



(b) +V_{REF} must be above peak positive swing of V_{IN}

FIGURE 25. Accommodating Bipolar References

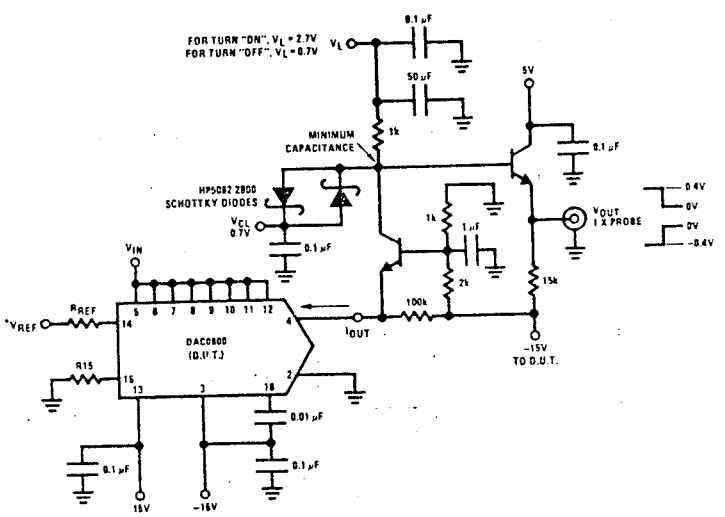
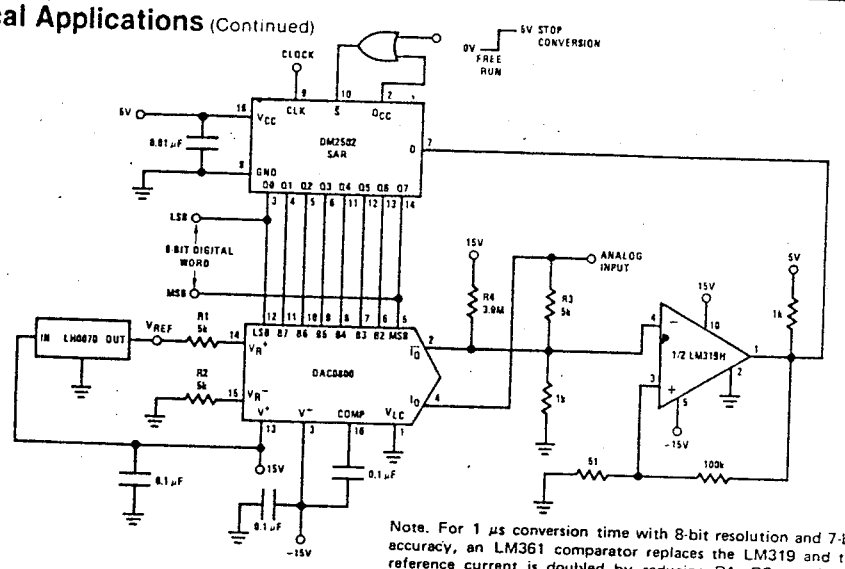


FIGURE 26. Settling Time Measurement

Typical Applications (Continued)



Note. For 1 μs conversion time with 8-bit resolution and 7-bit accuracy, an LM361 comparator replaces the LM319 and the reference current is doubled by reducing R1, R2 and R3 to 2.5 kΩ and R4 to 2 MΩ.

FIGURE 27. A Complete 2 μs Conversion Time, 8-Bit A/D Converter

8-CHANNEL ANALOGUE MULTIPLEXER/DEMULTIPLEXER

The HEF4051B is an 8-channel analogue multiplexer/demultiplexer with three address inputs (A_0 to A_2), an active LOW enable input ($\overline{E}$), eight independent inputs/outputs (Y_0 to Y_7) and a common input/output (Z).

The device contains eight bidirectional analogue switches, each with one side connected to an independent input/output (Y_0 to Y_7) and the other side connected to a common input/output (Z).

With $\overline{E}$ LOW, one of the eight switches is selected (low impedance ON-state) by A_0 to A_2. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of A_0 to A_2.

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (A_0 to A_2, and $\overline{E}$). The V_{DD} to V_{SS} range is 3 to 15 V. The analogue inputs/outputs (Y_0 to Y_7, and Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD}-V_{EE}$ may not exceed 15 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

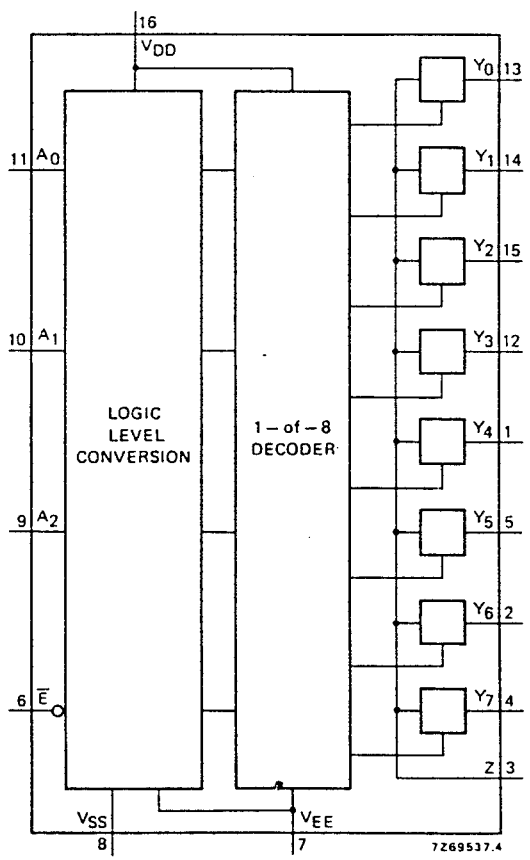


Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI

See Family Specifications

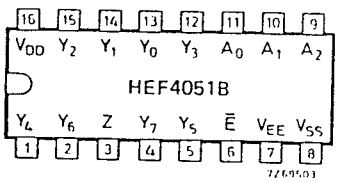


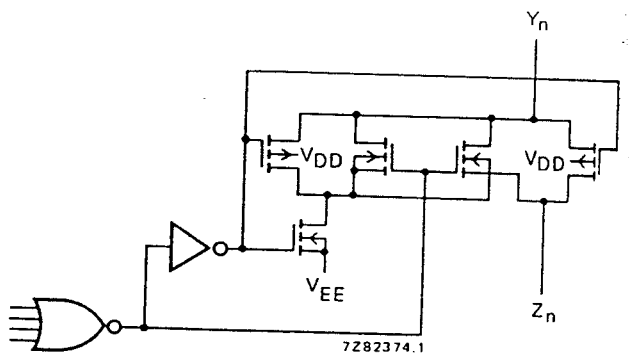
Fig. 2 Pinning diagram.

PINNING

Y_0 to Y_7	independent inputs/outputs
A_0 to A_2	address inputs
$\bar{E}$	enable input (active LOW)
Z	common input/output

HEF4051BP : 16-lead DIL; plastic (SOT-38Z).
HEF4051BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4051BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

Fig. 3 Schematic diagram (one switch).



FUNCTION TABLE

inputs				channel ON
$\bar{E}$	A_2	A_1	A_0	
L	L	L	L	Y_0–Z
L	L	L	H	Y_1–Z
L	L	H	L	Y_2–Z
L	L	H	H	Y_3–Z
L	H	L	L	Y_4–Z
L	H	L	H	Y_5–Z
L	H	H	L	Y_6–Z
L	H	H	H	Y_7–Z
H	X	X	X	none

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (with reference to V_{DD}) V_{EE} −18 to + 0,5 V

NOTE

To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{EE}.

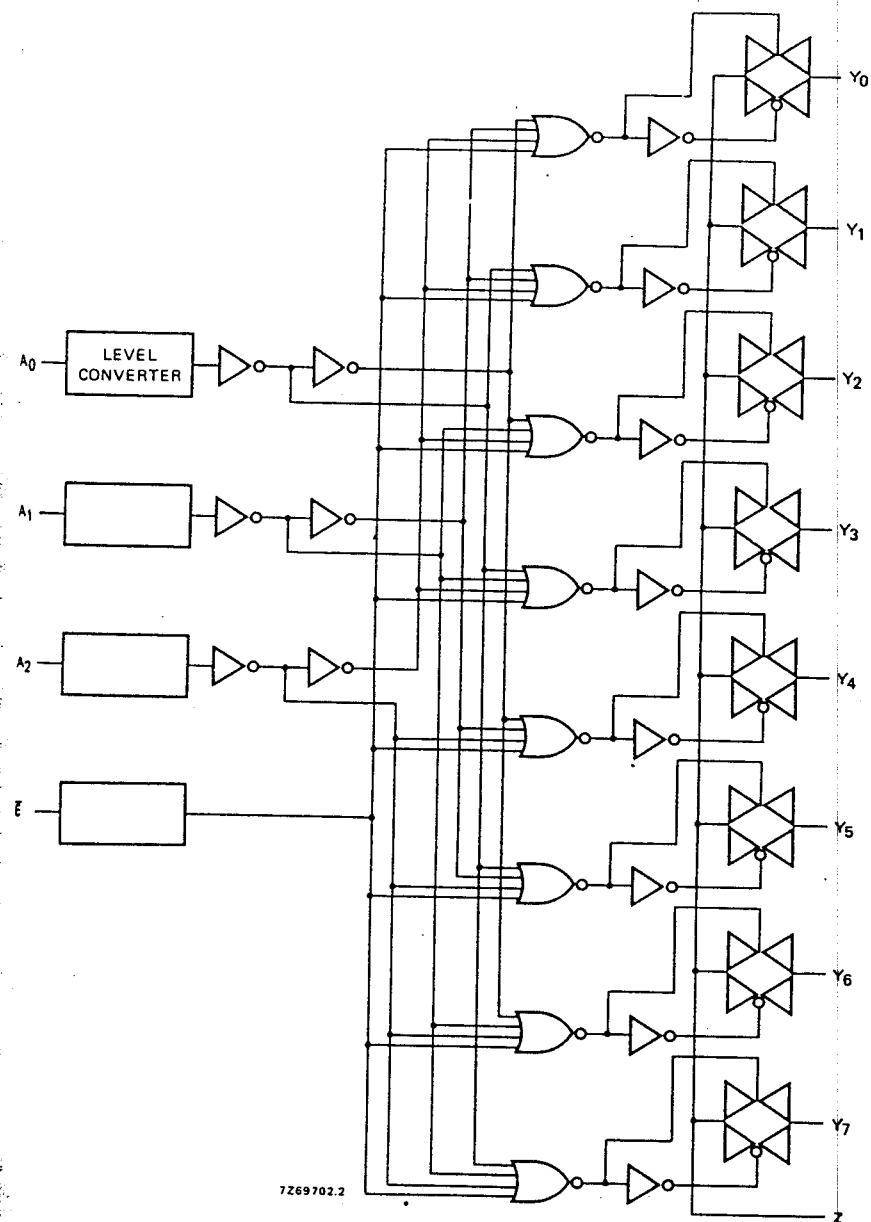


Fig. 4 Logic diagram.

D.C. CHARACTERISTICS

T_{amb} = 25 °C

	$V_{DD}-V_{EE}$ V	symbol	typ.	max.		conditions
ON resistance	5	R_{ON}	350	2500	Ω	V_{is} = 0 to $V_{DD}-V_{EE}$; see Fig. 6
	10		80	245	Ω	
	15		60	175	Ω	
ON resistance	5	R_{ON}	115	340	Ω	V_{is} = 0; see Fig. 6
	10		50	160	Ω	
	15		40	115	Ω	
ON resistance	5	R_{ON}	120	365	Ω	V_{is} = $V_{DD}-V_{EE}$; see Fig. 6
	10		65	200	Ω	
	15		50	155	Ω	
'Δ' ON resistance between any two channels	5	ΔR_{ON}	25	–	Ω	V_{is} = 0 to $V_{DD}-V_{EE}$; see Fig. 6
	10		10	–	Ω	
	15		5	–	Ω	
OFF-state leakage current, all channels OFF	5	I_{OZZ}	–	–	nA	$\overline{E}$ at V_{DD}; V_{SS} = V_{EE}
	10		–	–	nA	
	15		–	1000	nA	
OFF-state leakage current, any channel	5	I_{OZY}	–	–	nA	$\overline{E}$ at V_{SS}; V_{SS} = V_{EE}
	10		–	–	nA	
	15		–	200	nA	

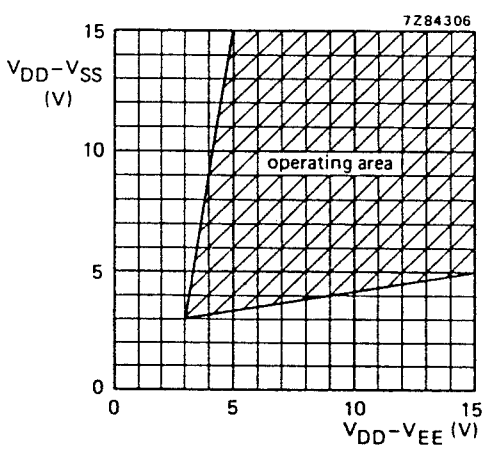


Fig. 5 Operating area as a function of the supply voltages.

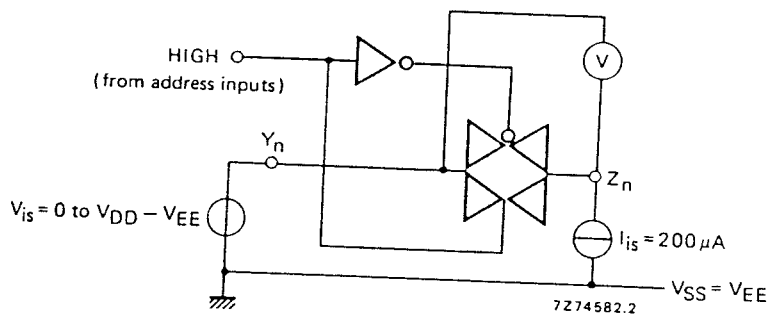


Fig. 6 Test set-up for measuring R_{ON}.

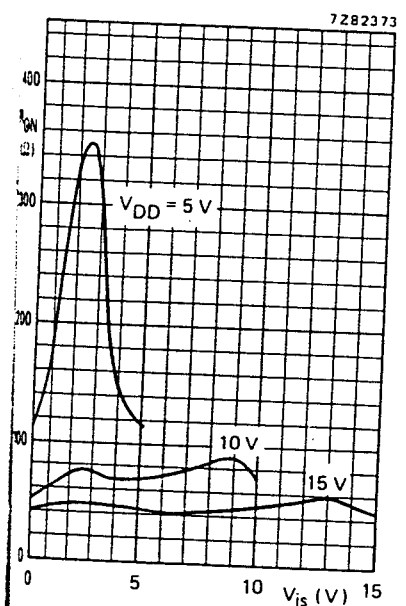


Fig. 7 Typical R_{ON} as a function of input voltage.

I_{is} = 200 μA
$V_{SS} = V_{EE}$ = 0 V

A.C. CHARACTERISTICS

$V_{EE} = V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5\,500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$15\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

$V_{EE} = V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		
Propagation delays						
$V_{is} \rightarrow V_{os}$						
HIGH to LOW	5	t_{PHL}	15	30	ns	note 1
	10		5	10	ns	
	15		5	10	ns	
LOW to HIGH	5	t_{PLH}	15	30	ns	note 1
	10		5	10	ns	
	15		5	10	ns	
$A_n \rightarrow V_{os}$						
HIGH to LOW	5	t_{PHL}	150	300	ns	note 2
	10		60	120	ns	
	15		45	90	ns	
LOW to HIGH	5	t_{PLH}	150	300	ns	note 2
	10		65	130	ns	
	15		45	90	ns	
Output disable times						
$\overline{E} \rightarrow V_{os}$						
HIGH	5	t_{PHZ}	120	240	ns	note 3
	10		90	180	ns	
	15		85	170	ns	
LOW	5	t_{PLZ}	145	290	ns	note 3
	10		120	240	ns	
	15		115	230	ns	
Output enable times						
$\overline{E} \rightarrow V_{os}$						
HIGH	5	t_{PZH}	140	280	ns	note 3
	10		55	110	ns	
	15		40	80	ns	
LOW	5	t_{PZL}	140	280	ns	note 3
	10		55	110	ns	
	15		40	80	ns	

A.C. CHARACTERISTICS

$V_{EE} = V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.	
Distortion, sine-wave response	5		0,25	%	note 4
	10		0,04	%	
	15		0,04	%	
Crosstalk between any two channels	5		–	MHz	note 5
	10		1	MHz	
	15		–	MHz	
Crosstalk; enable or address input to output	5		–	mV	note 6
	10		50	mV	
	15		–	mV	
OFF-state feed-through	5		–	MHz	note 7
	10		1	MHz	
	15		–	MHz	
ON-state frequency response	5		13	MHz	note 8
	10		40	MHz	
	15		70	MHz	

NOTES

V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.
V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.

1. $R_L = 10$ kΩ to V_{EE}; $C_L = 50$ pF to V_{EE}; $\overline{E} = V_{SS}$; $V_{is} = V_{DD}$ (square-wave); see Fig. 8.
2. $R_L = 10$ kΩ; $C_L = 50$ pF to V_{EE}; $\overline{E} = V_{SS}$; $A_n = V_{DD}$ (square-wave); $V_{is} = V_{DD}$ and R_L to V_{EE} for t_{PLH}; $V_{is} = V_{EE}$ and R_L to V_{DD} for t_{PHL}; see Fig. 8.
3. $R_L = 10$ kΩ; $C_L = 50$ pF to V_{EE}; $\overline{E} = V_{DD}$ (square-wave);
   $V_{is} = V_{DD}$ and R_L to V_{EE} for t_{PHZ} and t_{PZH};
   $V_{is} = V_{EE}$ and R_L to V_{DD} for t_{PLZ} and t_{PZL}; see Fig. 8.
4. $R_L = 10$ kΩ; $C_L = 15$ pF; channel ON; $V_{is} = ½ V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about $½ V_{DD}$); $f_{is} = 1$ kHz; see Fig. 9.
5. $R_L = 1$ kΩ; $V_{is} = ½ V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about $½ V_{DD}$); $20 \log \frac{V_{os}}{V_{is}} = -50$ dB; see Fig. 10.
6. $R_L = 10$ kΩ to V_{EE}; $C_L = 15$ pF to V_{EE}; $\overline{E}$ or $A_n = V_{DD}$ (square-wave); crosstalk is $|V_{os}|$ (peak value); see Fig. 8.
7. $R_L = 1$ kΩ; $C_L = 5$ pF; channel OFF; $V_{is} = ½ V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about $½ V_{DD}$); $20 \log \frac{V_{os}}{V_{is}} = -50$ dB; see Fig. 9.
8. $R_L = 1$ kΩ; $C_L = 5$ pF; channel ON; $V_{is} = ½ V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about $½ V_{DD}$); $20 \log \frac{V_{os}}{V_{is}} = -3$ dB; see Fig. 9.

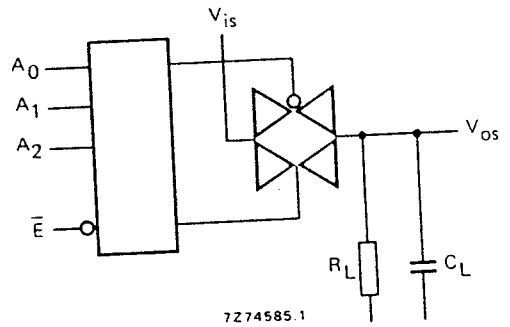


Fig. 8.

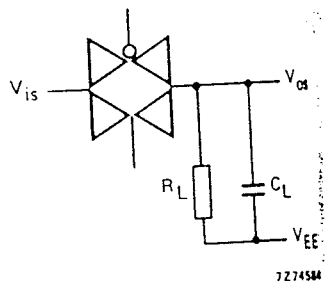


Fig. 9.

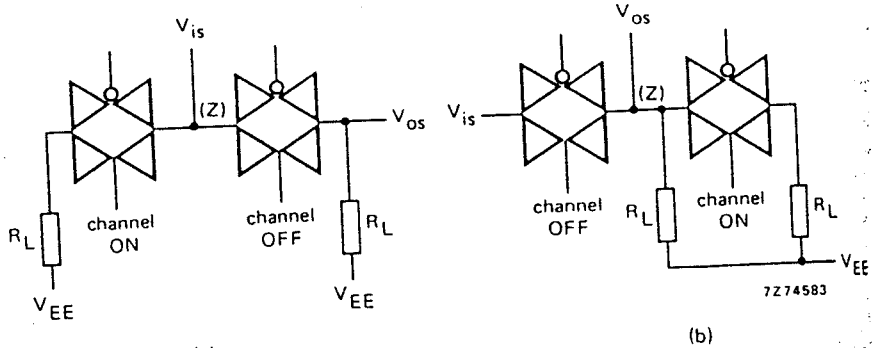


Fig. 10.

APPLICATION INFORMATION

Some examples of applications for the HEF4051B are:

- Analogue multiplexing and demultiplexing.
- Digital multiplexing and demultiplexing.
- Signal gating.

NOTE

If break before make is needed, then it is necessary to use the enable input.