Solid State Stabilizer

Project Report

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Submitted in Partial fulfilment of the Requirements for the award of Degree of Bachelor of Engineering in Electronics and Communication Engineering of Bharathiar University

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CERTIFICATE

This is to certify that the project report entitled

SOLID STATE STABILIZER

has been submitted by

Mr. S. ARUN, C. BALAJI, K. SATHISH KUMAR, B. V. SIVAKUMAR In partial fulfilment for the Award of Bachelor of Engineering in the Electronics and Communication Engineering Branch of the Bharathiar University, Coimbatore - 641 046.

During the Academic year 1993-'94

Guide

Head of Department

Certified that the candidate was examined by us in the project work viva-voce Examination held on ______________ and the University Register No. was ______________.

Internal Examiner

External Examiner

DEDICATED TO OUR BELOVED PARENTS

ACKNOWLEDGEMENT

ACKNOWLEDGEMENT

We express our thanks to our beloved principal **Dr.S.SUBRAMANIAN B.E., M.Sc (Engg)., P.hd., SMIEEE** for the facilities provided.

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We also express our sincere thanks to ECE staff members, lab assistants and friends for their invaluable help in completion of this project.

SYNOPSIS

SYNOPSIS

THE SOLID STATE STABILIZER is a novel and an advanced version of the servo stabilizer. The servo stabilizer uses a servo motor to select the required winding. But this new circuit incorporates only digital electronic components.

The electro mechanical moving parts are avoided in this circuit as they are the source of problems associated with any stabilizer.

This stabilizer involves only an ordinary transformer with several windings or taps. The triacs are used for switching appropriate taps and the number of triacs can be varied. The circuit acts very fast thus taking care of even sudden overshoots or undershoots of the main voltage.

The selection of taps is done using digital components which have high rise time and speed. The clock frequency being 50 HZ.

CONTENT

CONTENT

INTRODUCTION

CHAPTER 1

INTRODUCTION

The provisions of Indian Electricity Act require that power supply voltages should not drop or rise by more than four per cent, we find fluctuations taking the 230 V mains supply voltages to as low as 150 V or as high as 300 V occasionally.

With enormous increase in loads connected to distribution transformer, the electricity suppliers now find it exceedingly difficult to maintain the voltages within the stipulated values. This has necessitated the use of automatic voltage stabilizers for almost every instrument. Right from domestic appliances to complex electronic equipments, all need stabilizers before connecting power to them.

STABILIZERS-HEIRARCHY

CHAPTER 2

STABILIZERS - HEIRARCHY

In this chapter the different types of voltage stabilizers are described in detail.

Types of Voltage stabilizers

Ferro resonant stabilizer

In the early 70's the only commonly employed voltage stabilizer was the ferro resonant type. This used two transformers, one with a saturating core.

The principle of ferroresonance in a saturating core was used to keep the output voltage constant even though the input had variations over and below the rated nominal voltage.

Disadvantages

The disadvantage in such a stabilizer is distorted output similar to square wave due to saturation effects and some equipments face problems due to the distortion. But this stabilizer with all static parts is very reliable and has a long life.

Relay type automatic stabilizers

Relay type automatic stabilizer cater for small variations in input voltage. They employ one or two relays

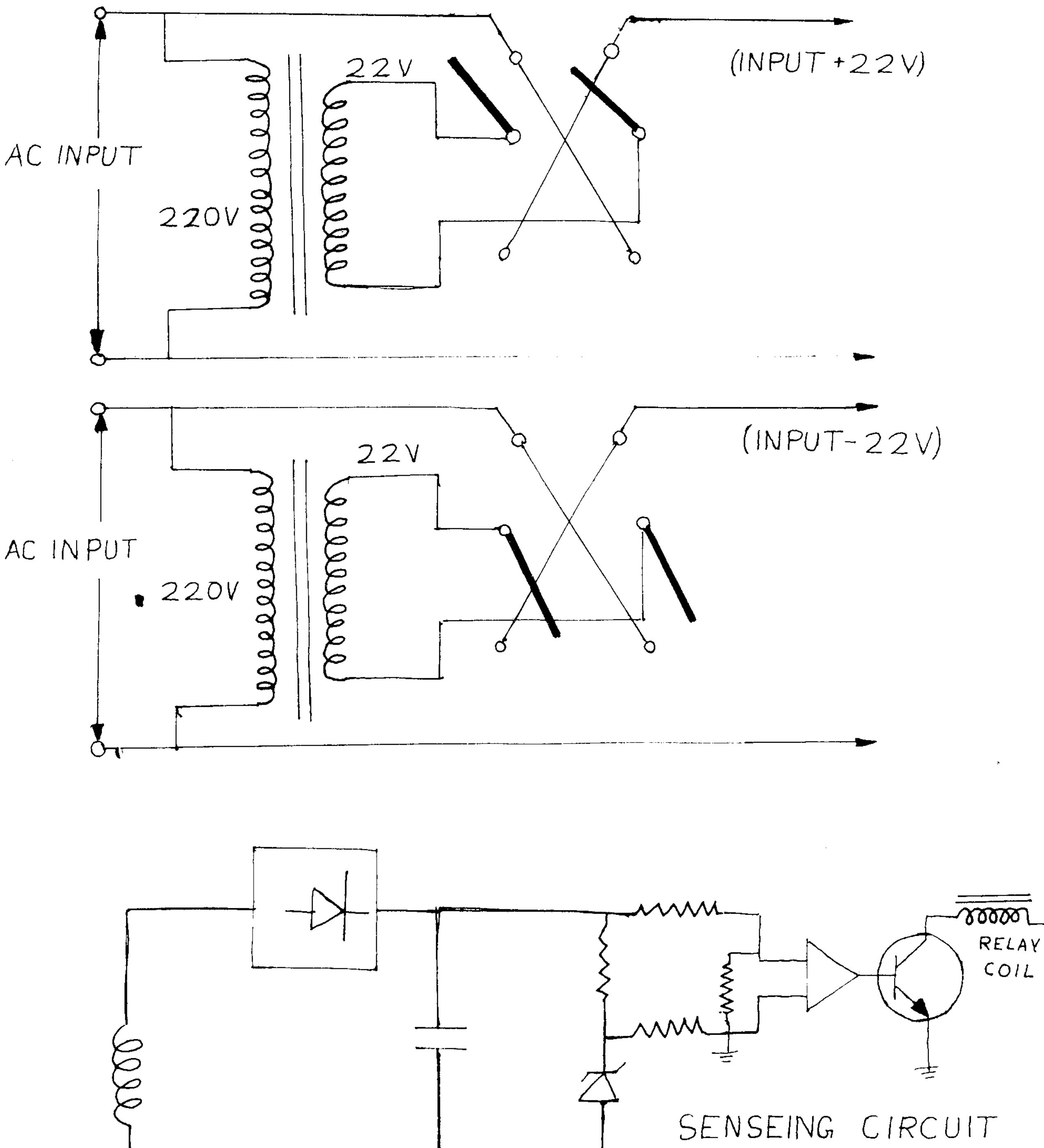

Figure-1 Principle of relay operated voltage stabilizer to switch voltage into the line so as to add to the input voltage when the input voltage falls below 220V. If the input rises above the nominal value it bucks or subtract this voltage. The winding of transformer is thus connected to either boost or buck the input voltage usually, if a 10 per cent variation is permitted below and above the nominal 220V a winding of the transformer with 22V (10 per cent) is connected either way to provide for inputs fluctuating from 200 to 240 V. The two position of the relays up and down in fig.1 are able to give a plus or minus 22V variation. But the input goes to 260 V, it will give 242 V and not 220 V output likewise if the input goes to 180 V it will give an output of 198 V only.

The relay contact changeover is done by a sensing circuit. This compares a fraction of the (rectified) input voltage with a fixed reference (Zener diode) voltage and depending on the value being above or below the reference it causes the relays to operate up or down positions as shown in fig 1. A number of variations are generally employed in practice.

Disadvantages of relay type voltage stabilizers

1. Power is off momentarily during relay change over affect sensitive equipement like computers, cannot afford this equipments with volatile memory will suffer a serious set back due to this problem.

2. The voltage range is very limited.

3. Limited accuracy of just 10 per cent.

4. Malfunctioning of electromagnetic relay contacts cause early worn out of the equipment.

Servo Stabilizers

These stabilizers employ a toroidal autotransformers and a servo motor driven by a circuit which sense the voltage. The toroidal auto tansformer has a toroidal core. It has a contact arm and houses a carbon brush which makes a sliding contact with the coil, wound over the toroid, just as in a potentiometer.

Enamelled copper wire, which is wound around the toroid uniformly is exposed (uncovered by enamel) at the top side where the contact is made by the carbon brush of the moving assembly. The output voltage is varied automatically on varying the position of this contact. For this purpose a servo motor fitted with gears is coupled to the contact arm.

The sensing circuit senses the voltage difference between the output and nominal voltage. It drives the servo motor, after suitable power amplification in clockwise or anticlockwise directions. As the motor moves the contact on the winding of the auto transformer, it reduces the voltage difference which becomes zero when output voltage reaches the nominal value. As there is no error signal now, servo

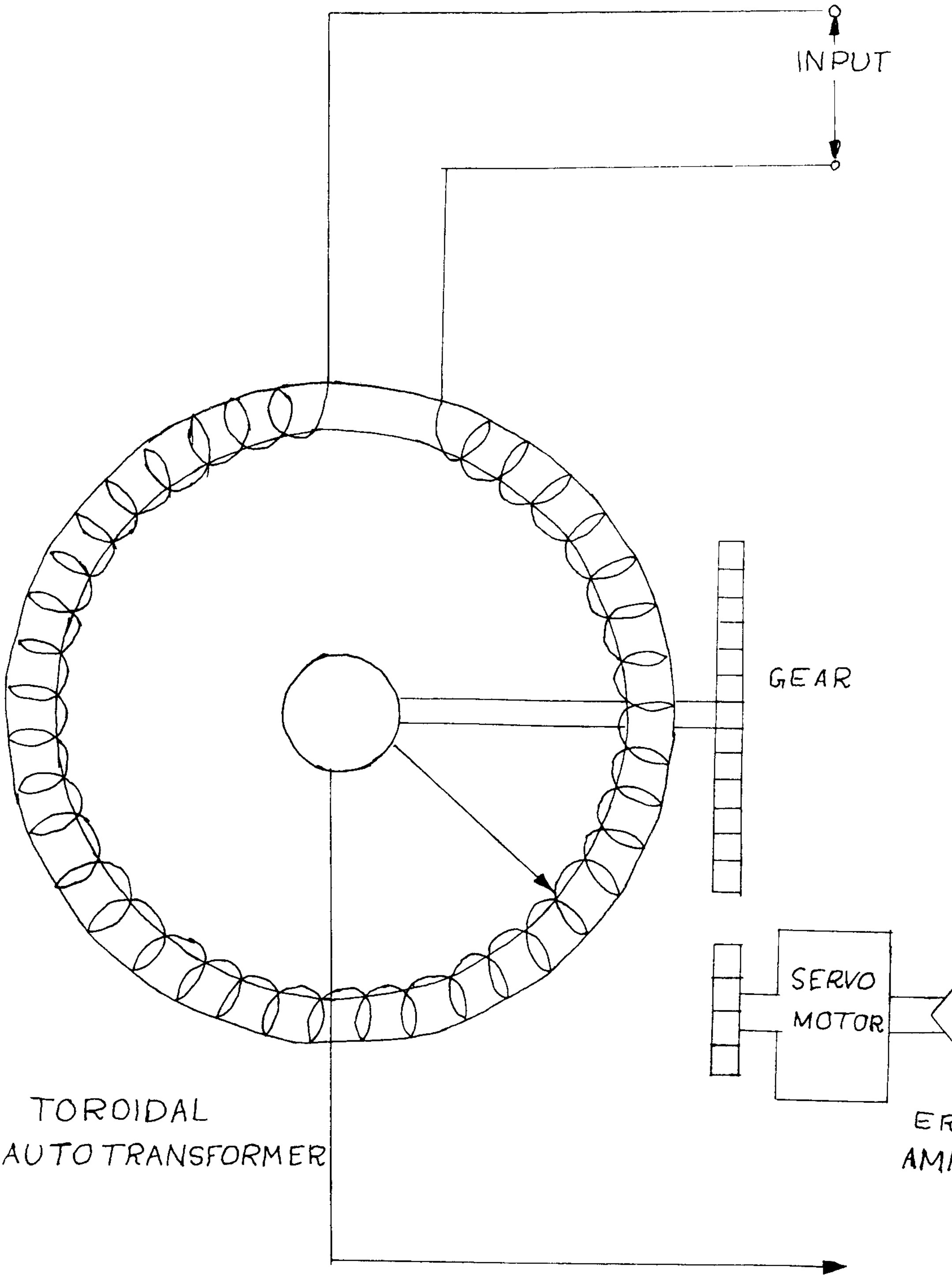

Figure-2 Servo type voltage stabilizer using servo motor and variable autotransformer motor stops. Further variations in mains causes the motor to move forward or backwards thus correcting the voltage.

The servo stabilizer it quite accurate as its resolution is the voltage across each turn of its toroidal winding. The resolution depends on core size of the toroid. If an autotransformer is wound for 280 V range it may have 1 V per turn and thus 280 turns wound over the toroid.

Disadvantages

A servo stabilizer has the tendency to 'hunt' if the input fluctuates too often. Also, it acts slowly and cannot adjust to sudden shoots or dips of main voltage. Actually, the servo motor takes atleast a second to make a movements for say a 20 V input change. But if the voltage fluctuates suddenly from say 180 to 260 V as is common when a heavy power load is switched off on the distribution line, it will take more than one second and during the time the requirement is subjected to this sudden over voltage of 260V.

SPECIFICATIONS

CHAPTER 3

SPECIFICATIONS

* INPUT	: 170 - 265 V
* OUTPUT	: 230 V
* POWER	: 0.5 KVA
* NUMBER OF STEPS	: 7
* INDICATION	: 3 1/2 DIGIT LED DISPLAY (DIGITAL)
* FEATURES	: 1. FREQUENCY 2. VOLTAGE OUPUT 3. VOL TAGE INPUT 4. POWER

* CURRENT LIMITING
* HIGH VOLTAGE CUT OFF
* LOW VOLTAGE CUT OFF
* START UP DELAY

PRINCIPLE

CHAPTER 4

PRINCIPLE

The solid state stabilizer consists of transformer, regulator, comparator, opto-coupler, triacs and digital logic gates.

Essentially, solid state stabilizer consists of an auto transformer with seven tappings. Each of the seven tapping is wound for 15 V. By connecting the phase of the mains supply at the centre of the tapping one can get upto 50 V above or below the input voltage by taking the output from one of the tap points.

Depending on the input voltage selection of the suitable winding is carried out. The selection is done by six triacs only one of which conducts at a time. Trigger pulses are applied at the gate of each triac to initiate its action.

The circuit consists of high and low voltage section. A pulse transformer was used in previous circuits to couple these two sections. But this circuits incorporates opto-couplers which are very efficient in coupling and thereby prevents any high current flowing into the low voltage section.

Trigger pulses which are needed to initiate triac action are got from opto-couplers. When the input voltage

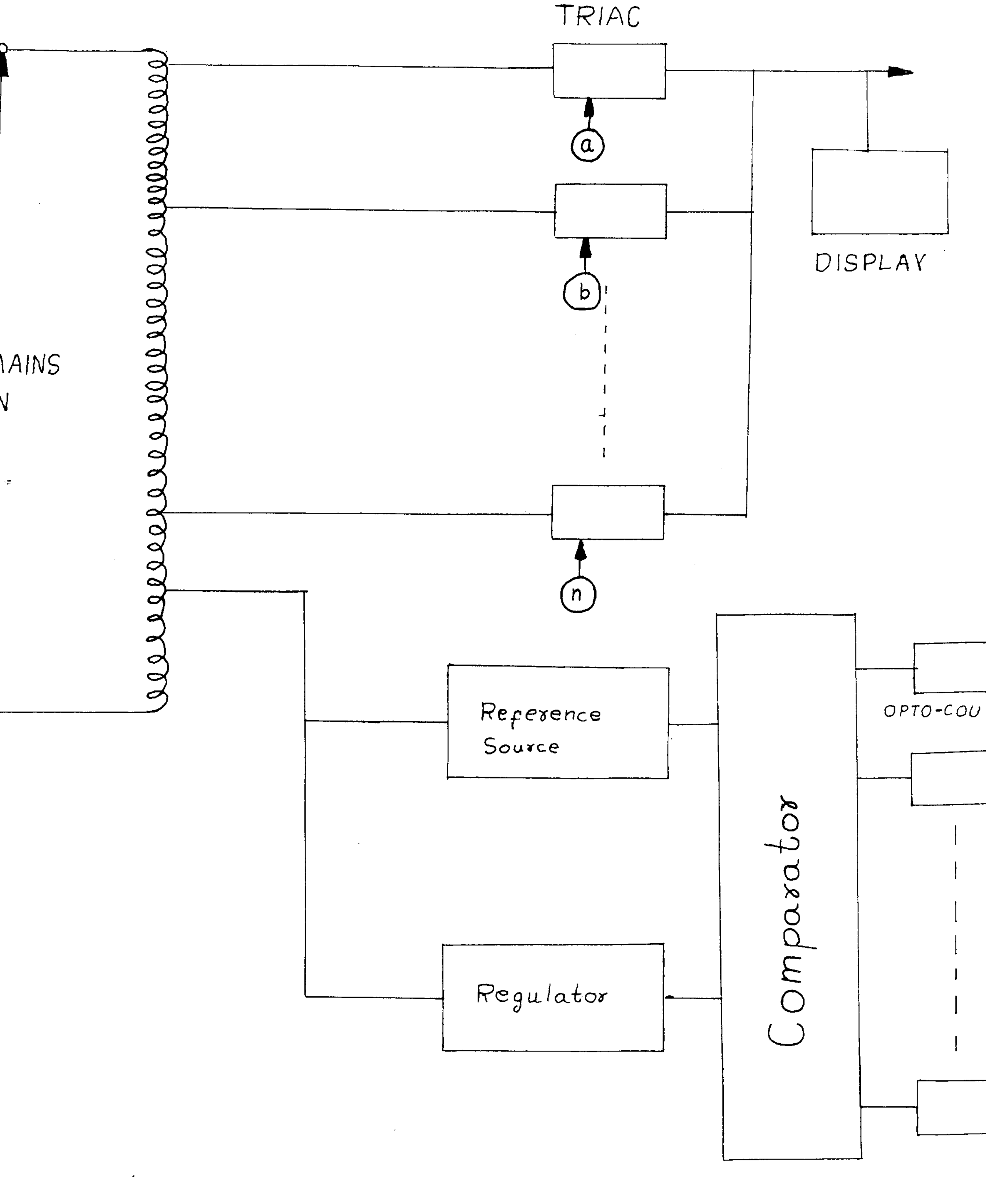

Figure 3 Block diagram representing the principle of operat

goes below the nominal voltage then the upper two triacs are triggered and when the input goes above the nominal voltages then lower four triacs are triggered. The outputs of all triacs are shorted.

A comparator integrated circuit used here provides seven outputs depending upon the input voltage. The comparator compare the input voltage with the regulated reference sources. Depending upon the magnitude of the error voltage a trigger pulse is applied to the corresponding triac.

The pulse circuit produce pulses coinciding with the zero crossing of AC sine wave. If pulse is not produced at zero crossing point, current flows in the circuit which leads to sparking. Thus the pulses cause the triac to start conduction from the zero of the alternating signal.

Thus output voltage is adjusted so as to buck or boost the input. The display section is used to display the input voltage, output voltage, frequency and power.

OPERATION

CHAPTER-5

OPERATION

The **SOLID STATE STABILIZER** circuit can be divided in to two sections.

1. Low voltage section
2. High voltage section

5.1. LOW VOLTAGE SECTION

The low voltage section mainly includes the switching circuits and display section.

5.1.1. SWITCHING CIRCUITS

The essential feature of this switching circuit is that it is completely digitised except for the comparators. The traditional systems required analog switching so as to provide a gradual change in the output winding positions. In our stabilizer the output is selected from the suitable tap. So digital switching is more efficient and reliable. Hence we have incorporated this in our project.

The voltage from the mains is reduced using a step-down transformer. This common voltage is fed to six potentiometers (50 kilo ohms) whose output vary in the increasing order. The output of the potentiometers is fed to a pair of quad comparators integerated circuits (LM 339). The reference voltage to these comparators is tied to a

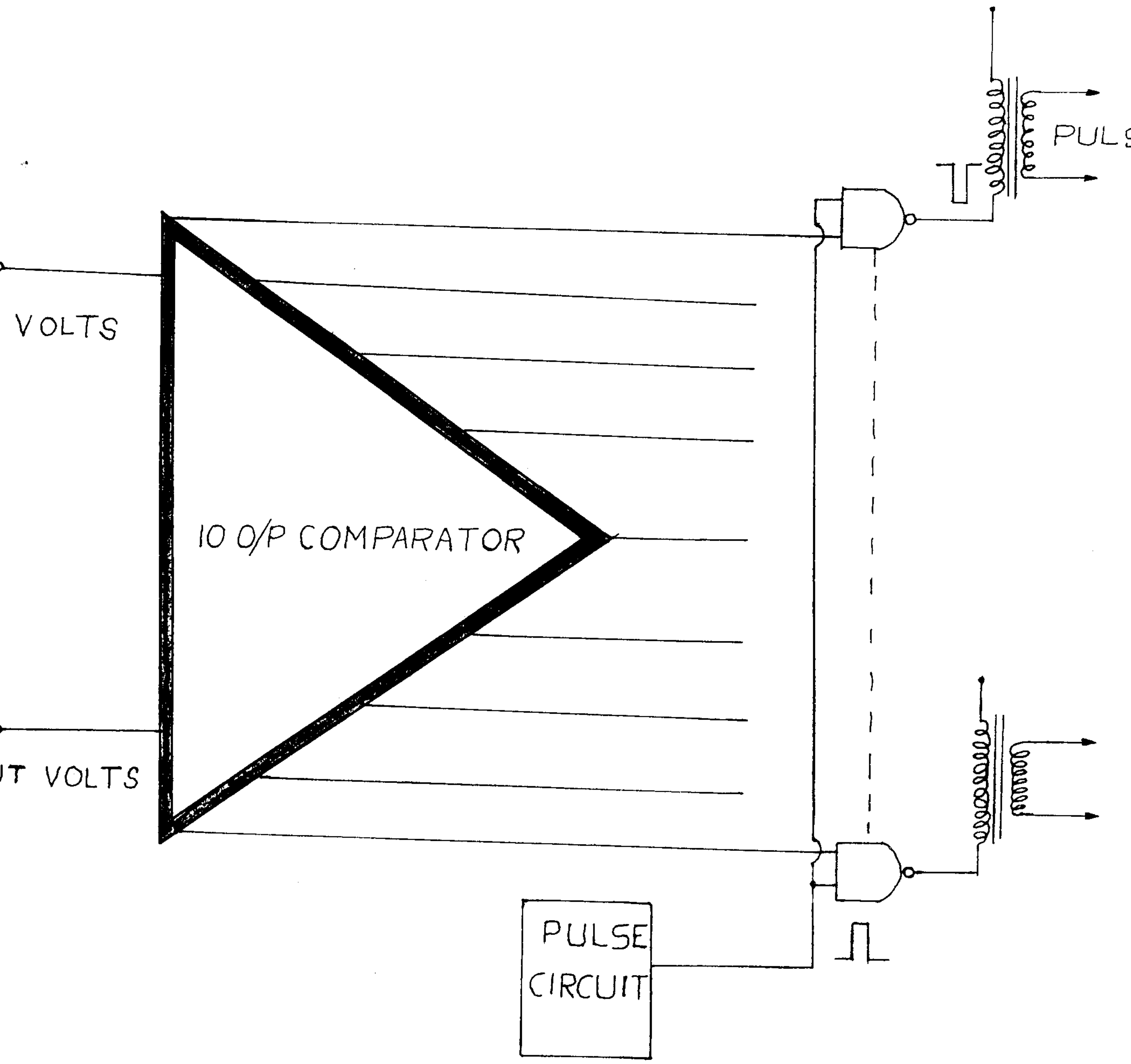

Figure -4 Block diagram of comparator circuit is 12 volts got directly from the mains. Each LM 339 chip has four comparators. The reference voltage is fed to the non-inverting terminals. The input from the potentiometers is fed to the inverting terminals of the comparators. If the inverting voltage is greater than the non-inverting voltage, then the output is tied to the inverting voltage or else the output is zero) The output of the comparators are fed to the BCD to decimal convertors (IC 74LS145).In order to maintain the necessary logic 1 threshold, an additional voltage is added to these voltages. The conversion principle is similar to peak detection method. The output amplitude is maximum of the input signal at a particular instant. Here the inputs are given to 4 terminals, A,B,C and D and the outputs are taken from pin numbers 2,4 & 9 which corresponds to decimal values 1,2 and 4.

Using two 74LS145 chips a total of six tappings can be selected which is used to control the voltages in the given range. The outputs from all the BCD to decimal convertors are inverted in IC 74LS04 and are stored in D flip flops.

The clock to the D FFs is maintained such that its contents are varied every 20 m seconds. The 20 m seconds clock is got from LM 311 which is used in zero crossing mode. The alternating 50 Hz signal is given to LM311. The output is a square wave which varies from +V to -V volts.

In order to give this signal as clock to the D FF it is passed through a zener diode which reduce the voltage to 0-5V range.

The special feature of this circuit is the delay on time. The main advantage of this delay on time to avoid sudden current spikes when switched ON. When the delayed swtich ON is used, the stabilizer waits for few seconds before giving out the output, when it is switched ON. During the wait period the output zero and after few seconds the suitable tapping is selected depending on the input voltage.

The DELAY ON time procedure is carried out by using IC74LS121 multivibrator. IC 74LS121 is used in monostable mode. The OFF time is determined based on RC values. Since this has to be given to the clear terminal of D flip flop it is inverted using IC 74LS00 NAND gate. The outputs from the D flip flop is maintained at 5 V using fixed bias transister amplifiers and fed to the opto-coupler.

Opto-coupler is similar to a transformer coupling but the coupling is optical in nature. Opto-coupler has a light emitting diode at the input side and photo detector at the output side. Depending upon the input, intensity of the light emitted from LED can be varied. This light is made to fall on the photo detector which converts light into electric signals. The important point to be remembered while using the opto-coupler is that the input and output should be electrically isolated.

Included are seven segement decoders, display drivers, a reference and a clock. The ICL7107 gives an unprecendented combination of high accuracy, verstaility and true economy. It features auto - zero to less than 10 micro volts, zero draft of less than 1 microvolt per centrigrade, bias current of 10 pA max and a roll - over error of less than one count.

The other important features of ICL 7107 are

- Direct display drive - No external components Required LED ICL 7107
- On chip clock and reference
- Low noise dissipation - Typically less than 10 MW

The output from ICL 7107 is given to 4 seven segment LED display chips (542). In order to indicate the parameter to be displayed, 3 LEDS are used.

To the right of the seven segment display 2 LEDS are used to indicate the units of the parameters. (Hz, VOLTS). The power supply for the display section is get from a seperate transformer |(10-0-10)V & 5V|.

Other than these displays, 5 LEDS are used to indicate the general ON/OFF condition of the stabilizer, time delay ON, time delay OFF, low voltage cut off, high voltage cut off conditions. Once the stabilizer is switched

ON, the general ON/OFF LED is finished ON and the time delay ON LED is also turned ON. After a suitable delay (approximately 5 sec) the time delay ON LED goes OFF and time delay OFF goes ON. The other 2 LED'S goes ON under suitable respective conditions. The other noteworthy feature in the display section is the use of 7 LEDS to indicate tap which is selected. This is very helpful in identification of trouble shooting points and thus easen the servicing of the stabilizer.

5.1.2 DISPLAY SECTION

The parameters that are displayed are input voltage, output voltage, frequency and power.

In order to display input and output voltages, the main voltage is dropped across a very small resistance such that the drop does not exceed 5 V. This drop is taken as input for the display section, where a four in single output switch is used. The other input to the switch is used to display the frequency of the mains.

In order to display the frequency, a frequency to voltage converter is used. Here the frequency to voltage converter is a RC network where the output is taken across the capcitor and is given to the switch.

The switch is a four in single out switch which provides a single output depending on the position of the switch. Thus the switch can be used to select any of the three parameters.

The output of this switch is given as input to ICL7107 3 1/2 digit LED display A/D converters containing all the necessary active devices on a single CMOS IC.

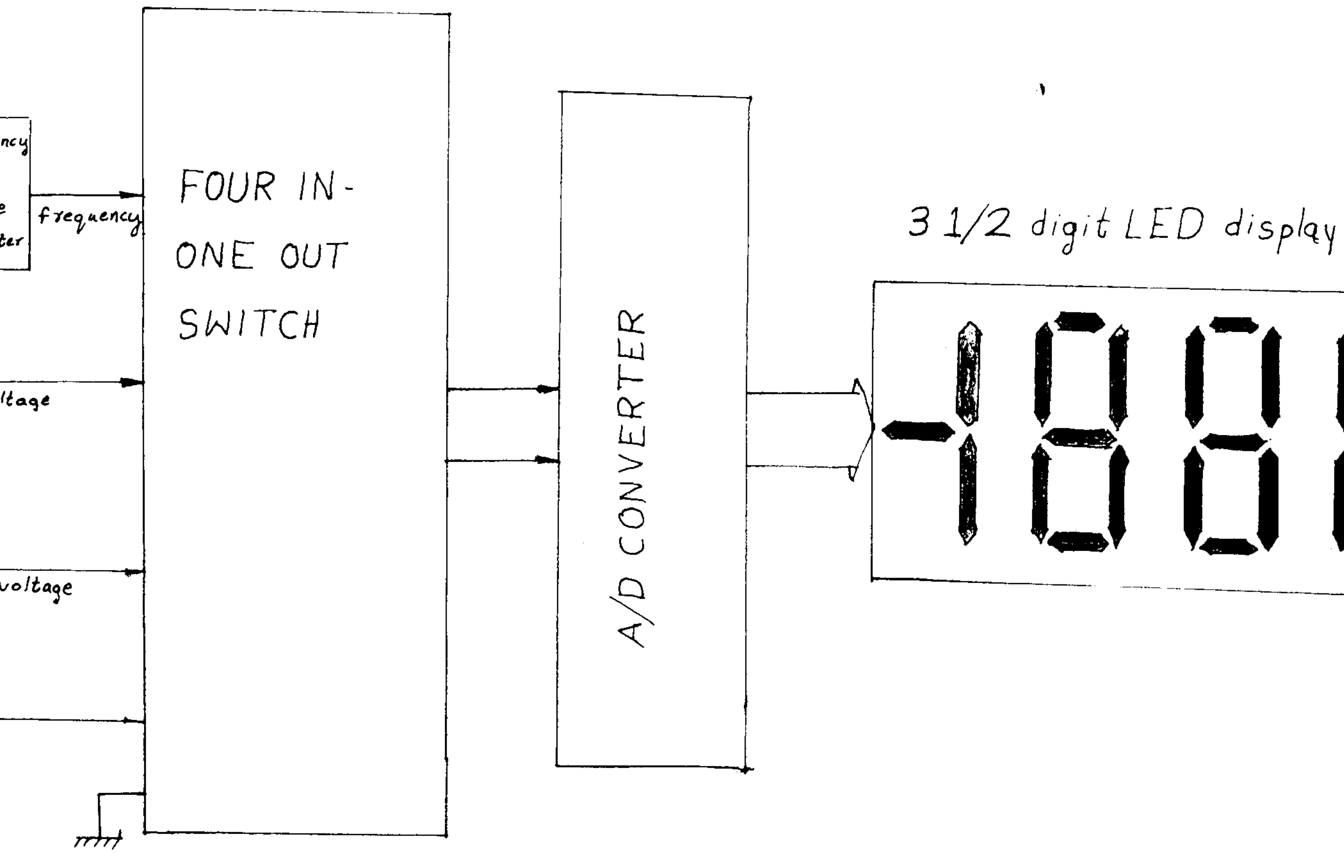

Figure-5 Block diagram of display section

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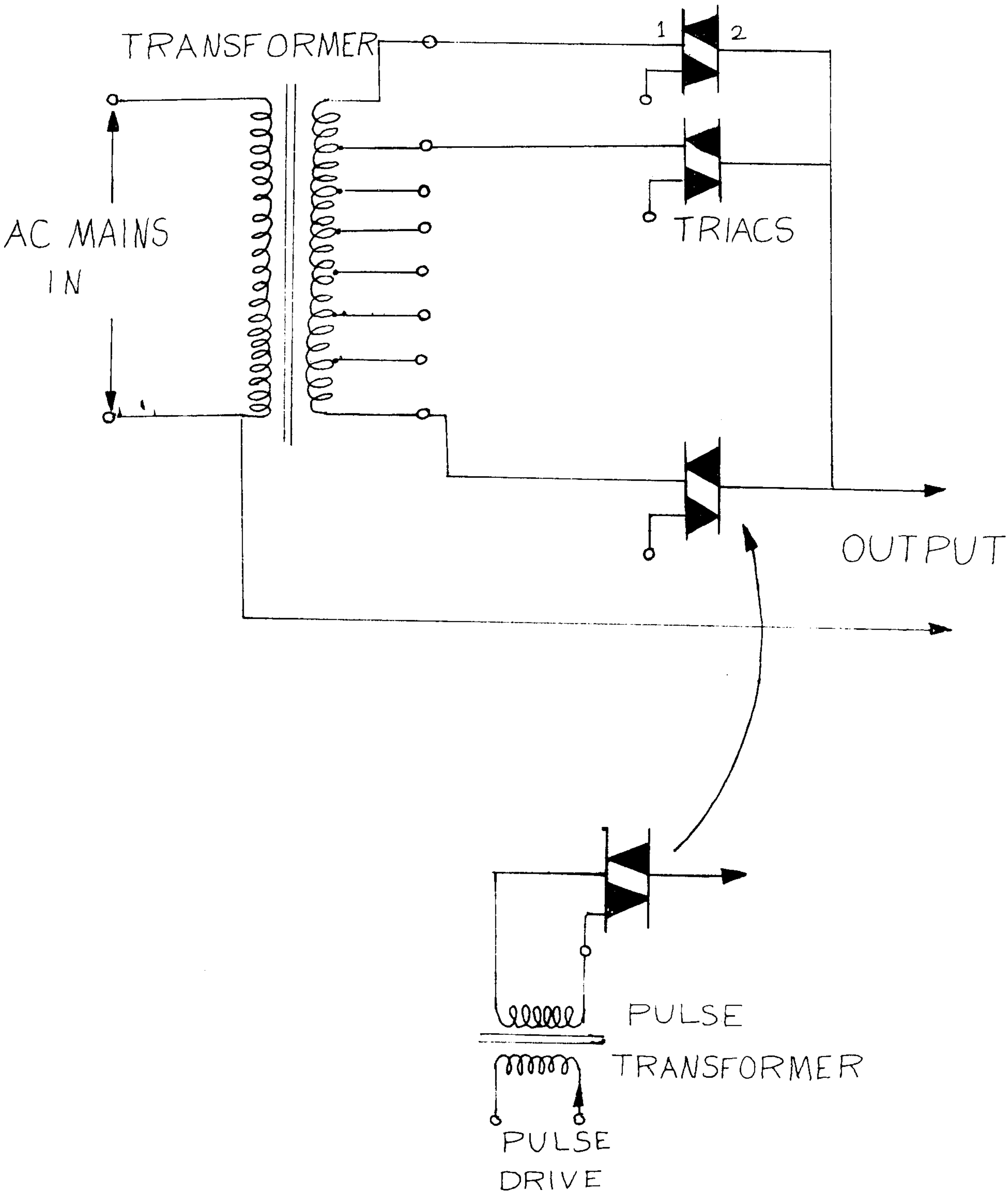
5.2 HIGH VOLTAGE SECTION

The voltage from the mains is given to an auto-transformer which is wound to the required current capacity. Output is taken from six tap points each wound for 15 V using which one can get upto 45 V above or below the input voltage.

The selection is done by seven triacs only one of which conducts at a time. Trigger pulses are used to start the triacs which are got from the opto coupler.

When the input goes below the nominal, the upper two triacs are triggered and when the input goes higher than the nominal, the lower four triacs are triggered. The output all the triacs are short circuited and hence output is taken from this point.



TRANSFORMER
1
2
AC MAINS
IN
TRIACS
OUTPUT
PULSE
TRANSFORMER
PULSE
DRIVE

5.2.1. THE TRIAC

Triac (triggers on ac) which can block voltages of either polarity but which starts the current flow in either direction by means of a pulse in or out of its single gate. The triac has four major layers NPNP, but several N regions are fitted into its lower P layer as shown in fig. 7.a one of these N region serves as terminal T1, and the other is the gate. Meanwhile, the upper P layer is made to protrude through part of the top N layer to form terminal T2.

Figure 7.b shows the triac symbol. The curves of anode current versus anode voltage is shown in fig 12.a Either T1 or T2 can be anode. When T2 is positive, the triac response is as shown in fig 8. a current pulse into the gate starts the main current flow from T2 to T1. When T2 is negative, very little anode current flows until there is a pulse of current out of the gate. With no gate current, the triac resists the applied voltage of either polarity . Only a few volts drop remains across the triac while it is conducting its rated 4 or 6 Amperes in either direction; the rest of the applied ac voltage appears across the load .

The top half of fig.8 demonstrates the possibility of negative or positive gate triggering. When T2 is positive with positive gate voltage, gate current flows from G to T, via the indicated forward biased pn junction.

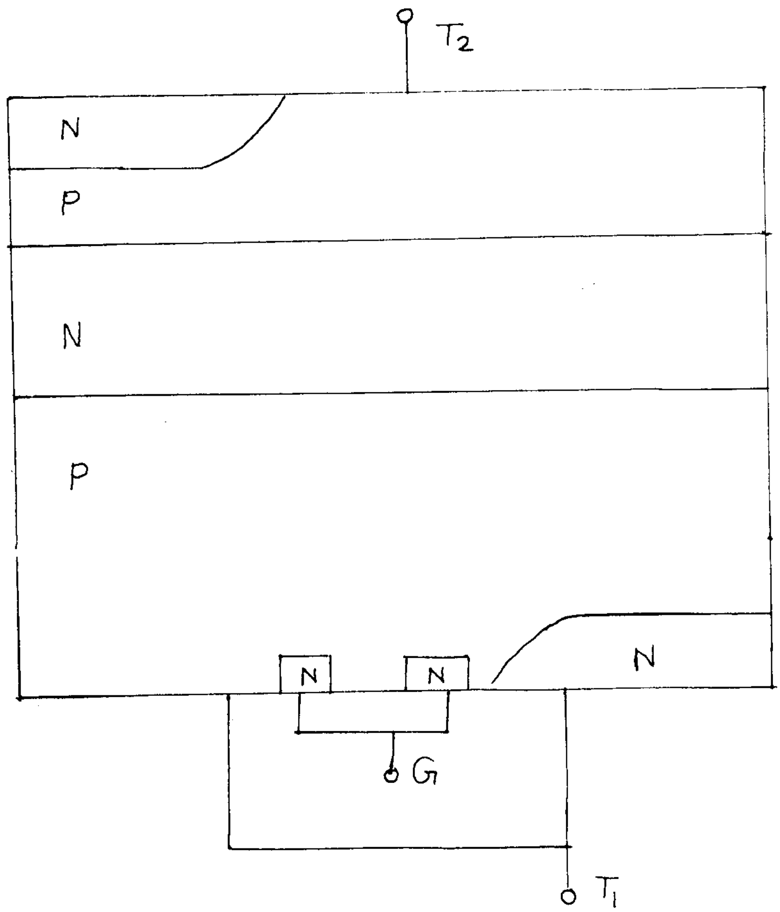


Figure 7a Triac structure

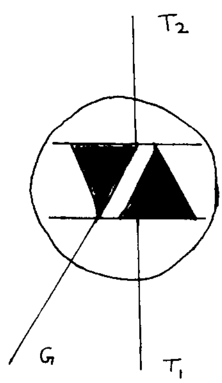
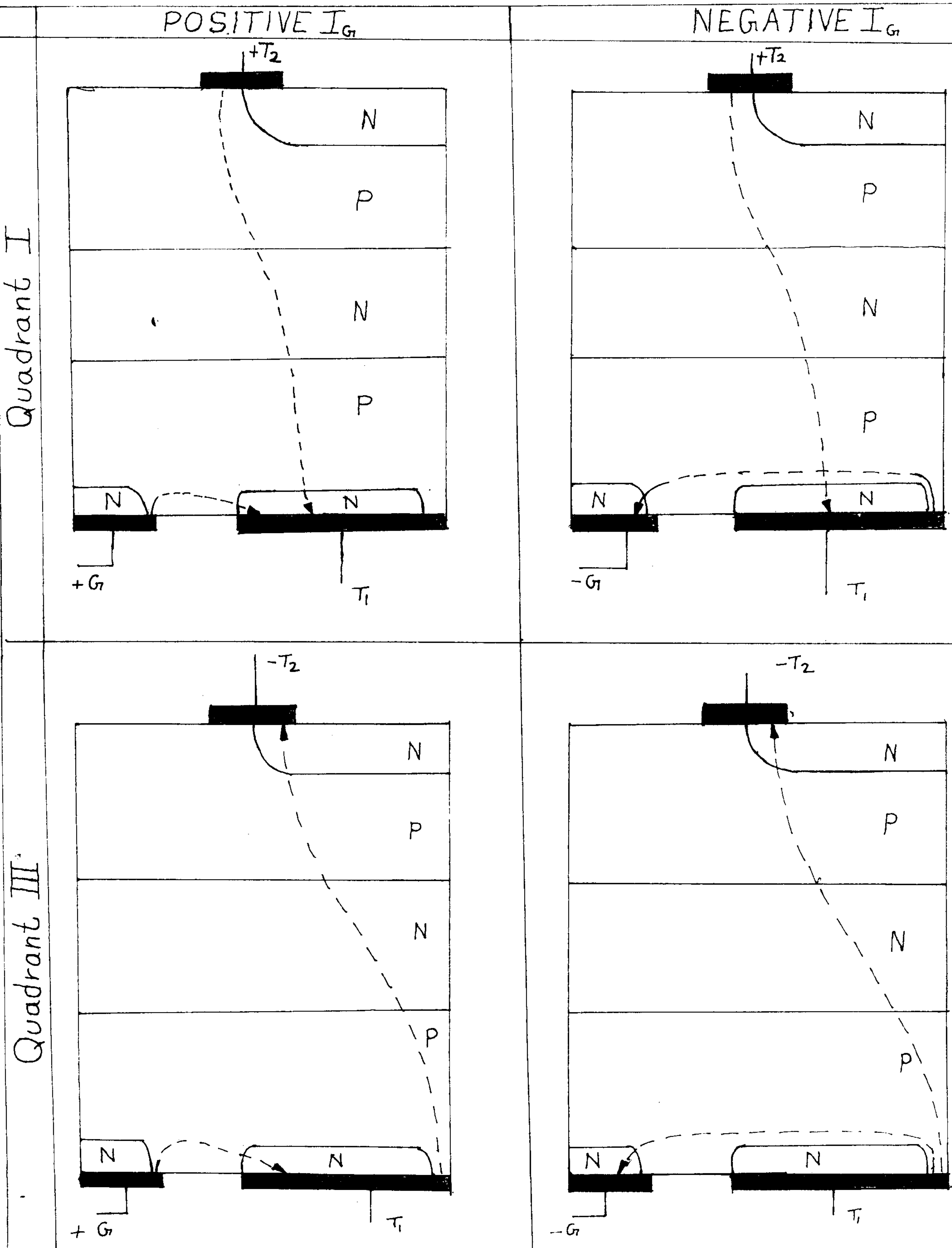


Figure 7b Triac symbol


POSITIVE I_G
NEGATIVE I_G
Quadrant I
Quadrant III
$+T_2$
N
P
N
P
N
N
$+G$
T_1
$+T_2$
N
P
N
P
N
N
$-G$
T_1
$-T_2$
N
P
N
P
N
N
$+G$
T_1
$-T_2$
N
P
N
P
N
N
$-G$
T_1

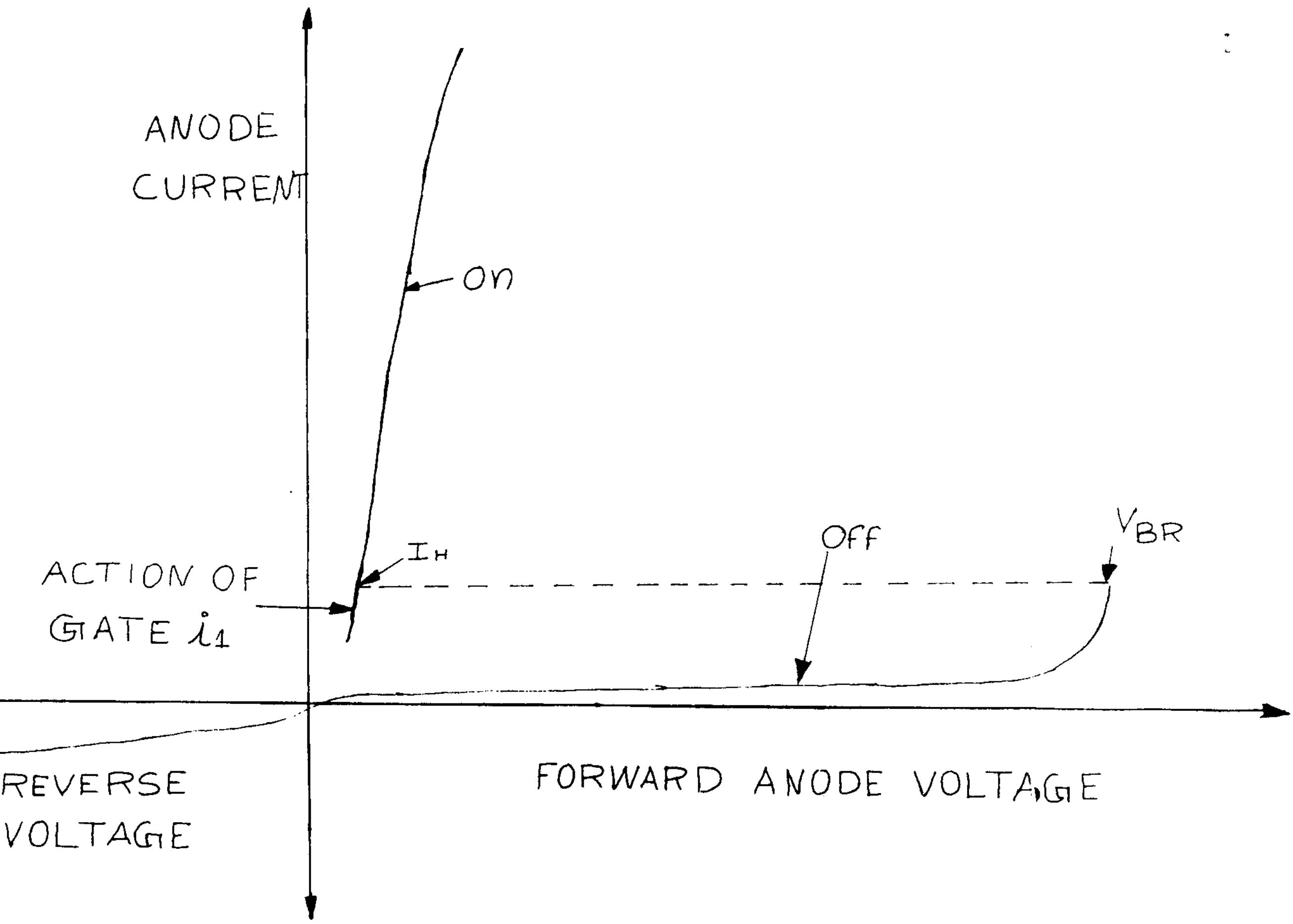


Figure-9 SCR anode current Versus anode Voltage

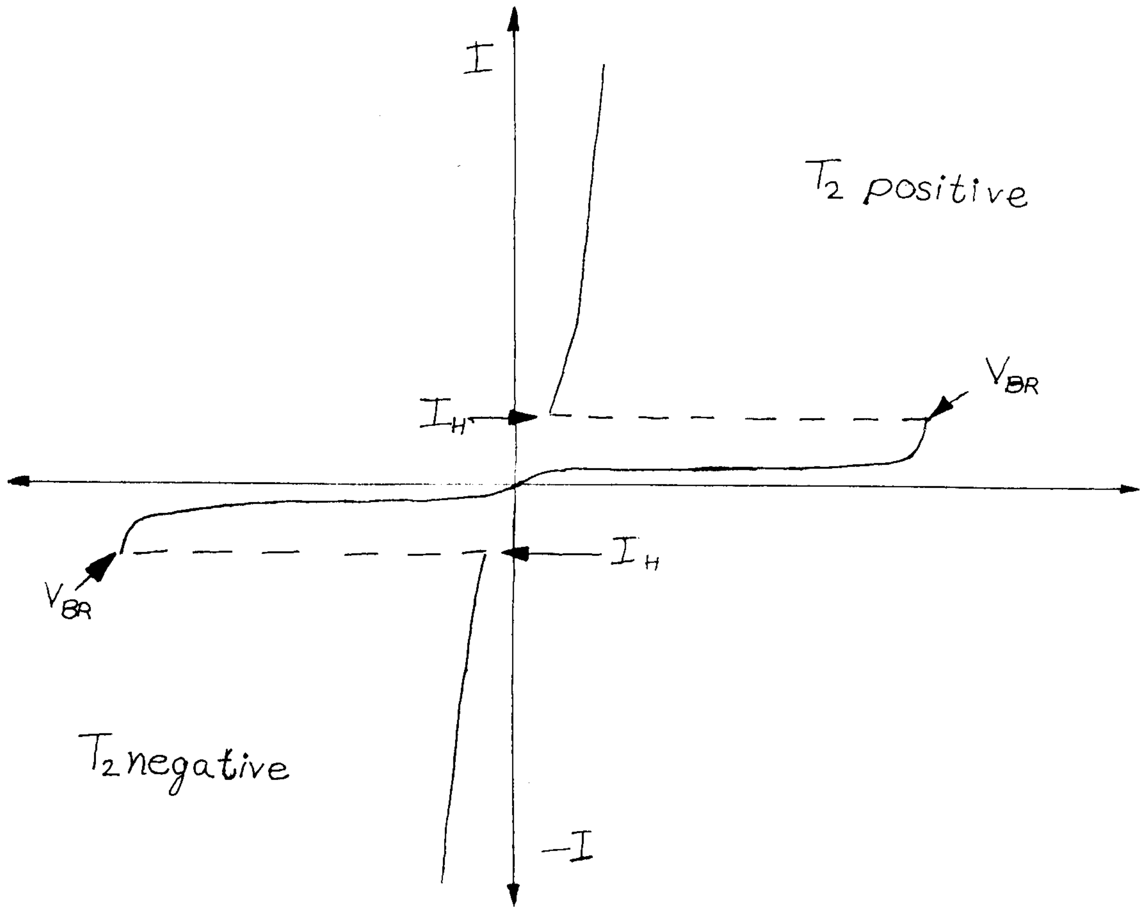


Figure.10a Triac current Verses voltage characteristic

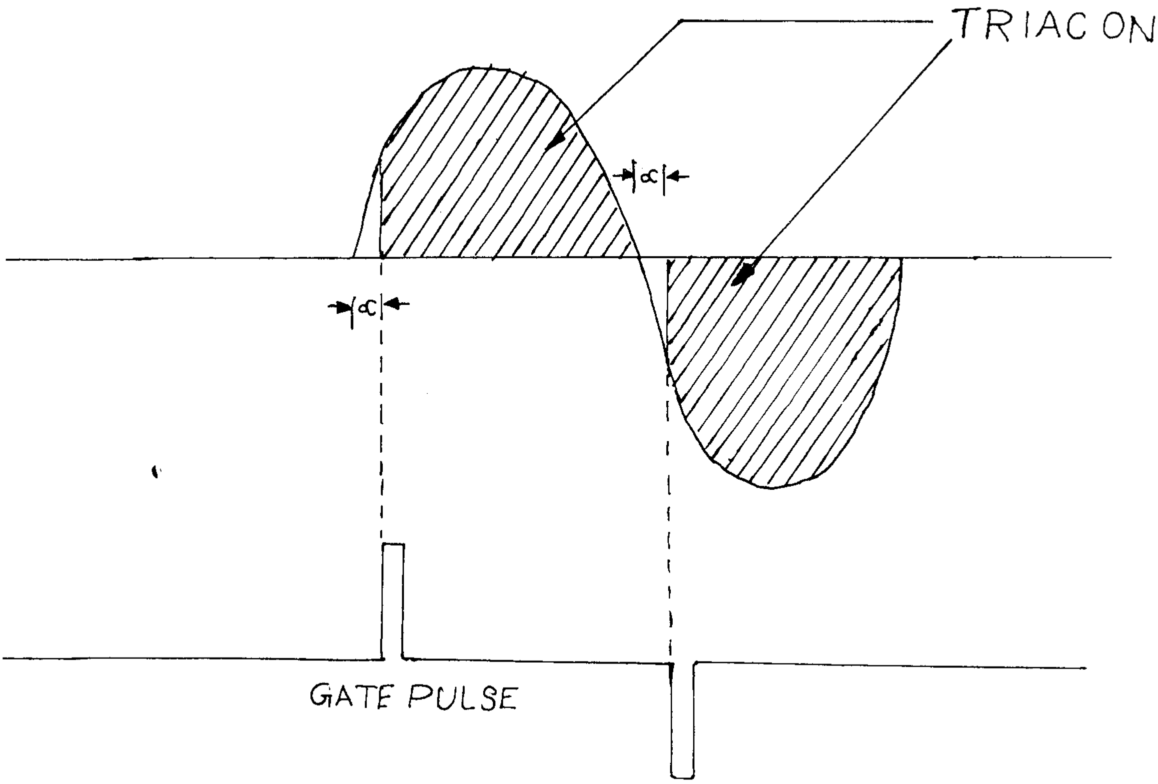


Figure.10b. Principle of Triac Conduction

Negative gate signals can also trigger the triac, the only difference being the path of gate-current flow and some differences in the required level of gate current due to non-symmetry and effects or principal current.

The device can reverse from non-conducting or OFF state to the conducting or ON state by exceeding the breakover voltage or by gate triggering. Once ON, the gate also loses control until the principal current is reduced below the holding-current level. The triac can be triggered ON by 1 or 2 volts at gate or a few tens of milliamperes.

5.2.2. AUTO TRANSFORMER

A transformer having a single continuous winding common to primary and secondary circuits is termed as autotransformer.

Figure 13 shows the schematic diagram of autotransformer, in which the winding AB forms the primary and the supply voltage is applied across it. The portion BC of the winding AB forms the secondary and as such the load is connected across BC. Hence the portion BC of the winding is common to both primary and secondary thus resulting in economy of material.

Autotransformers work on the same principle as an ordinary transformer. They are mainly used for connecting systems that operate at low voltages. They are also used as starters for starting 3 - phase squirrel cage induction motors. They are simple and relatively low cost compared to multi winding transformers.

Looking at the secondary side of the autotransformer, it can be considered equivalent to a potential divider.

The autotransformer voltage and turns ratio is

$$a^1 = \frac{E_{AC} + E_{CB}}{E_{CB}}$$

$$= \frac{N_{AC} + N_{CB}}{N_{CB}}$$

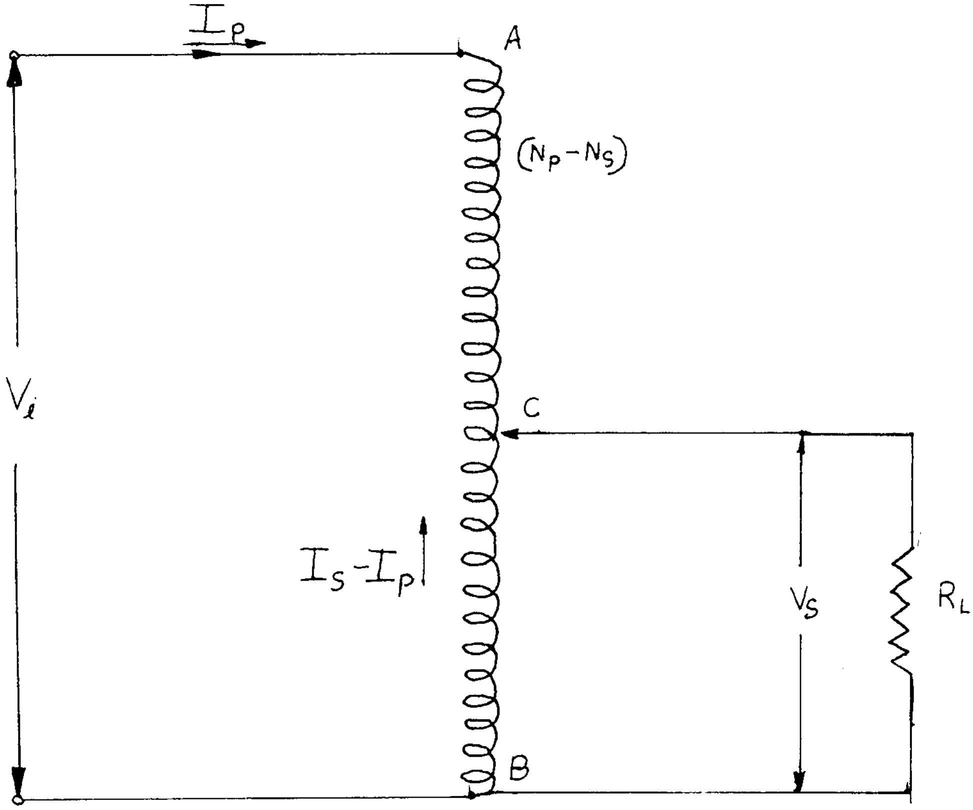


Figure-13 Autotransformer

$$a^1 = a + 1$$

Where 'a' is the voltage and turns ratio of the original two - winding transformer.

Besides furnishing a greater transforming action, a pair of windings connected as an autotransformer can also deliver more volt - amperes (apparent power) than when connected as a two - winding transformer. The reason is that the transformer of apparent power from primary to secondaryis not only by induction, as in a two - winding transformer, but by conduction as well.

SPECIAL FEATURES

CHAPTER 6

SPECIAL FEATURES

- No motors for servo.
- No bulky variable transformer.
- Simple novel circuit.
- Fast acting unlike motorised servo types.
- Same circuit for any capacity, only triacs to be altered.
- High efficiency.
- Highly economical.
- High and low voltage cut off LED indication.
- LED indication of parameters
  No meters required.
- No dynamic parts.
- Easy servicing and trouble - shooting indication.

CONCLUSION

CHAPTER 7

CONCLUSION

A year's diligence and intriguing work, has made project SOLID STATE STABILIZER successful. At this juncture we cannot but help cite Sir Issac Newton -

Knowledge is like a shell
I am just a child who picks
Up some of these colourful ones,
but when I look back there are
millions others still lying on the
shore of the "Ocean of knowledge"

The SOLID STATE STABILIZER has been tested and proved under actual working conditions. Our fledging efforts have proved successful yet a lot of developments are in the anvil, particularly in the controlling sections. Advanced FETS and power transistors replace triacs and thereby decreasing complexity and cost of the whole unit.

Though stabilizer have been existing for a long time, newer and advanced versions are always welcome to improve the efficiency and regulation. We have strived to achieve the above objectives in earnest.

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APPENDIX

½-Digit LCD/LED
gle-Chip A/D Converter

ERAL DESCRIPTION

Intersil ICL7106 and 7107 are high performance, low 3½-digit A/D converters containing all the necessary devices on a single CMOS I.C. Included are seven-ent decoders, display drivers, a reference, and a The 7106 is designed to interface with a liquid crystal y (LCD) and includes a backplane drive; the 7107 will y drive an instrument-size light emitting diode (LED) y.

7106 and 7107 bring together an unprecedented ination of high accuracy, versatility, and true economy. tures auto-zero to less than 10μV, zero drift of less 1μV/°C, input bias current of 10 pA max., and rollover of less than one count. True differential inputs and nce are useful in all systems, but give the designer an mmon advantage when measuring load cells, strain es and other bridge-type transducers. Finally, the true omy of single power supply operation (7106), enables n performance panel meter to be built with the addition ly 10 passive components and a display.

FEATURES

- Guaranteed Zero Reading for 0 Volts Input on All Scales
- True Polarity at Zero for Precise Null Detection
- 1pA Typical Input Current
- True Differential Input and Reference
- Direct Display Drive — No External Components Required — LCD ICL7106
  — LED ICL7107
- Low Noise - Less Than 15μV p-p
- On-Chip Clock and Reference
- Low Power Dissipation - Typically Less Than 10mW
- No Additional Active Circuits Required
- New Small Outline Surface Mount Package Available
- Evaluation Kit Available

2

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7106CPL	0°C to +70°C	40 pin plastic DIP
ICL7106CJL	0°C to +70°C	40 pin CERDIP
ICL7106CM44	0°C to +70°C	44 pin Surface Mount
ICL7107CJL	0°C to +70°C	40 pin CERDIP
ICL7107CPL	0°C to +70°C	40 pin plastic DIP
ICL7106EV/Kit ICL7107EV/Kit	Evaluation kits contain IC, display, circuit board, passive components and hardware.	

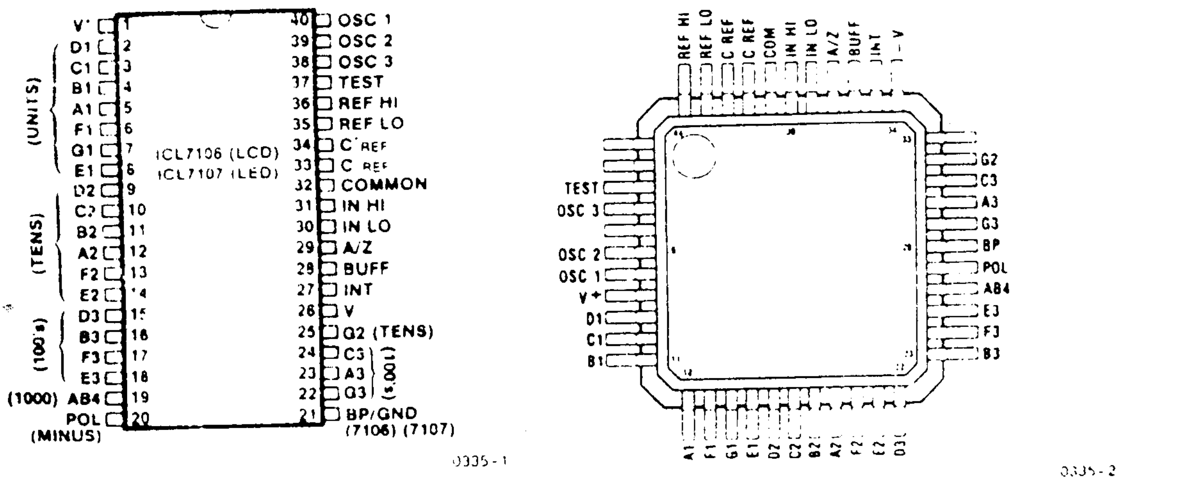


Figure 1: Pin Configurations

301650-003

ICL7106/ICL7107

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- ICL7106, V⁺ to V⁻ 15V
- ICL7107, V⁺ to GND ..... +6V
- ICL7107, V⁻ to GND ..... -9V

Analog Input Voltage (either input) (Note 1) ..... V⁺ to V⁻
Reference Input Voltage (either input) ..... V⁺ to V⁻
Clock Input
- ICL7106 ..... TEST to V⁺
- ICL7107 ..... GND to V⁺

Power Dissipation (Note 2)
- Ceramic Package 1000mW
- Plastic Package 800mW

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

ELECTRICAL CHARACTERISTICS (Note 3)

Characteristics	Test Conditions	Min	Typ	Max	Unit
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	V_{IN} = V_{REF} V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative inputs near Full Scale)	$-V_{IN}$ = $+V_{IN}$ ≈ 200.0mV	-1	±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200.0mV or full scale = 2.000V (Note 6)	-1	±.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		μV
Leakage Current Input	V_{IN} = 0 (Note 6)		1	10	pA
Zero Reading Drift	V_{IN} = 0 0° < T_A < 70°C (Note 6)		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° < T_A < 70°C (Ext. Ref. 0ppm/°C) (Note 6)		1	5	ppm/°C
V⁺ Supply Current (Does not include LED current for 7107)	V_{IN} = 0		0.8	1.8	mA
V⁻ Supply Current (7107 only)			0.6	1.8	mA
Analog Common Voltage (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply		80		ppm/°C

RICAL CHARACTERISTICS (Note 3) (Continued)

Characteristics	Test Conditions	Min	Typ	Max	Unit
ONLY Segment Drive Voltage Backplane Drive Voltage 5)	V+ to V− = 9V	4	5	6	V
ONLY ment Sinking Current ept Pin 19 & 20)	V+ = 5.0V Segment voltage = 3V	5	8.0		mA
9 only) 20 only)		10 4	16 7		mA

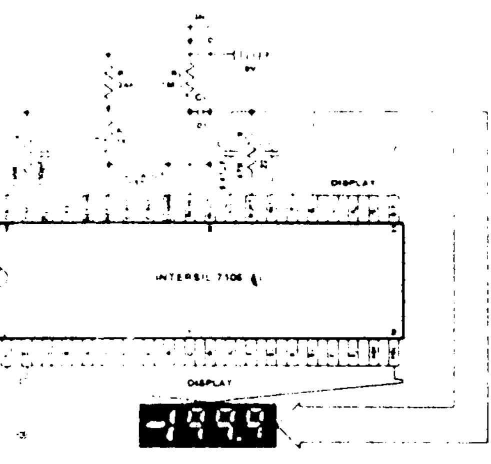
nless otherwise noted, specifications apply to both the 7106 and 7107 at $T_A = 25°C$, $f_{clock} = 48kHz$. 7106 is tested in the circuit of Figure 2. 7107 is sted in the circuit of Figure 3.

ote: Differential input discussion.

ack plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average C component is less than 50mV.

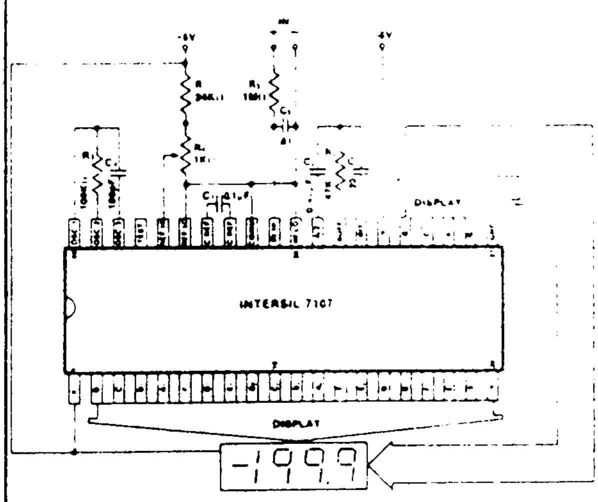
ot tested, guaranteed by design.

CIRCUITS



0335-3

ure 2: ICL7106 Test Circuit and Typical
pplication With Liquid Crystal Display



0335-4

Figure 3: ICL7107 Test Circuit and Typical Application With LED Display

e Gate Triacs

rectional Thyristors

ly for full-wave ac control applications, such as light dimmers, ting controls and power supplies; or wherever full-wave silicon d-state devices are needed. Triac type thyristors switch from a cting state for either polarity of applied anode voltage with gate triggering.

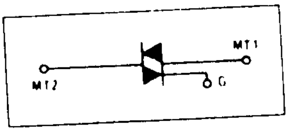
iggering (A and B versions) Uniquely Compatible for Direct L, HTL, CMOS and Operational Amplifier Integrated Circuit s

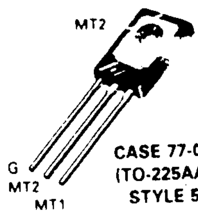
2 Mode — 2N6071, 2N6073, 2N6075
4 Mode — 2N6071,A,B, 2N6073,A,B, 2N6075,A,B
s to 600 Volts
Glass Passivated Junctions for Greater Parameter Uniformity

Thermopad Construction for Low Thermal Resistance, High Heat d Durability

2N6071,A,B
2N6073,A,B
2N6075,A,B

TRIACs
4 AMPERES RMS
200 thru 600 VOLTS





CASE 77-06
(TO-225AA)
STYLE 5

3

NGS

Rating	Symbol	Value	Unit
Off-State Voltage, Note 1 2N6071,A,B 2N6073,A,B 2N6075,A,B	V_{DRM}	 200 400 600	Volts
nt RMS (T_C = 85°C)	$I_{T(RMS)}$	4	Amps
rrent le, 60 Hz, T_J = −40 to +110°C)	I_{TSM}	30	Amps
Considerations	I^2t	3.7	A^2s
wer	P_{GM}	10	Watts
Power	$P_{G(AV)}$	0.5	Watt
ltage	V_{GM}	5	Volts

Registered Data.
ply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that e applied exceeds the rated blocking voltage.

MAXIMUM RATINGS

Rating	Symbol	Value
•Operating Junction Temperature Range	T_J	40 to +110
•Storage Temperature Range	T_{stg}	40 to +150
Mounting Torque (6-32 Screw) Note 1		8

•Indicates JEDEC Registered Data

Note 1. Torque rating applies with use of compression washer (B52200F006) Mounting torque in excess of 6 in. lb. does not appreciab to sink thermal resistance. Main terminal 2 and heatsink contact pad are common.

For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +200°C, for 1 Consult factory for lead bending options.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max
•Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.5
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75

•Indicates JEDEC Registered Data

ELECTRICAL CHARACTERISTICS (T_C 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	M
•Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_J 25°C	I_{DRM}, I_{RRM}	—	—	1
T_J 110°C		—	—	2
•On State Voltage (Either Direction) (I_{TM} 6 A Peak)	V_{TM}	—	—	2
•Peak Gate Trigger Voltage (Continuous dc) (Main Terminal Voltage 12 Vdc, R_L 100 Ohms, T_J 40°C)	V_{GT}			
MT2(+), G(+); MT2(−), G( ) All Types		—	1.4	2
MT2(+), G( ); MT2( ), G(+) 2N6071,A,B, 2N6073,A,B 2N6075,A,B		—	1.4	2
(Main Terminal Voltage Rated V_{DRM}, R_L 10 k ohms, T_J 110°C)				
MT2(+), G(+); MT2( ), G( ) All Types		0.2	—	—
MT2(+), G( ), MT2( ), G(+) 2N6071,A,B, 2N6073,A,B, 2N6075,A,B		0.2	—	—
•Holding Current (Either Direction) (Main Terminal Voltage 12 Vdc, Gate Open, T_J 40 C) (Initiating [illegible] 1 Adc) 2N6071, 2N6073, 2N6075	I_H	—	—	—
2N6071A,B, 2N6073,A,B, 2N6075,A,B		—	—	—
(T_J 25°C) 2N6071, 2N60[illegible] 2N6075		—	—	—
2N6071,A,B, 2N6073,A,B, 2N6075,A,B		—	—	—
Turn-On Time (Either Direction) (I_{TM} 14 Adc, I_{GT} = 100 mAdc)	t_{on}	—	1.5	
Blocking Voltage Application Rate at Con[illegible]tation [illegible] V_{DRM}, T_J = 85°C, Gate Open	dv/dt	—	5	

•Indicates JEDEC Registered Data

National Semiconductor

LM139/239/339, LM139A/239A/339A, LM2901, LM3302 Low Power Low Offset Voltage Quad Comparators

General Description

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

[illegible] comparators, simple [illegible] pulse, squarewave and [illegible] VCO; MOS clock [illegible] voltage digital logic [illegible] designed to directly [illegible] CMOS. When operated [illegible] power supplies, they [illegible] MOS logic— where the [illegible] LM339 is a distinct advantage over standard comparators.

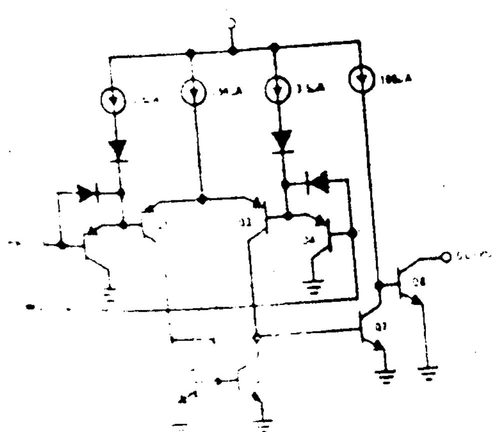
Advantages

- High [illegible] comparators
- Reduced [illegible] over temperature
- Eliminate need for dual supplies
- Allows sensing near gnd
- Compatible with all forms of logic
- Power drain suitable for battery operation

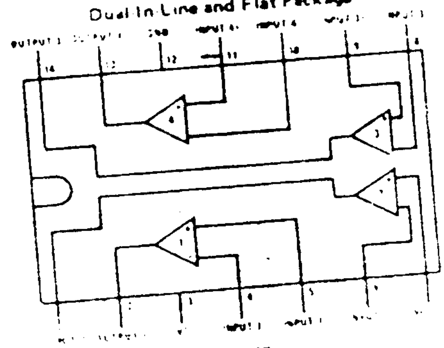
Features

- Wide single supply voltage range or dual supplies
  - LM139 series, 2 VDC to 36 VDC or ±1 VDC to ±18 VDC
  - LM139A series, LM2901
  - LM3302: 2 VDC to 28 VDC or ±1 VDC to ±14 VDC
- Very low supply current drain (0.8 mA) — independent of supply voltage (2 mW/comparator at +5 VDC)
- Low input biasing current: 25 nA
- Low input offset current: ±5 nA
- and offset voltage: ±3 mV
- Input common mode voltage range includes gnd
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage: 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Schematic and Connection Diagrams



Dual-In-Line and Flat Package

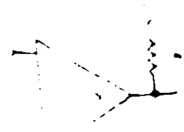


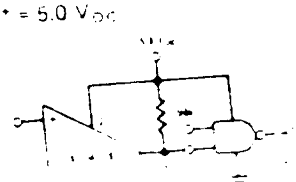
TOP VIEW

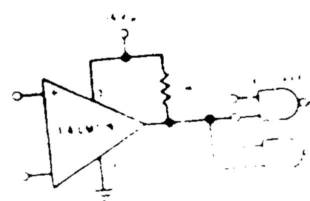
Order Number LM139J, LM139AJ, LM239J, LM239AJ, LM339J, LM339AJ, LM2901J or LM3302J
See NS Package J14A

Order Number LM339N, LM339AN, LM2901N or LM3302N
See NS Package N14A

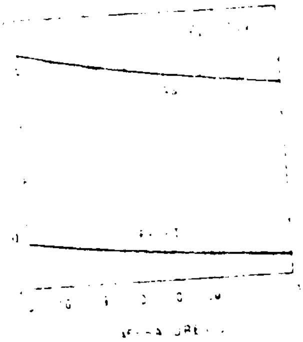
Typical Applications (V+ = 5.0 VDC)



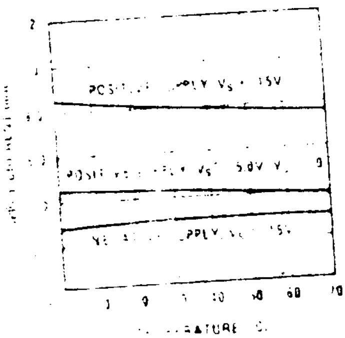




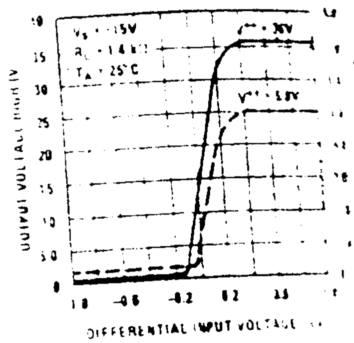
Typical Performance Characteristics LM319

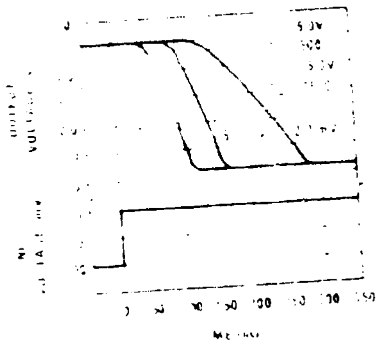


Supply Currents

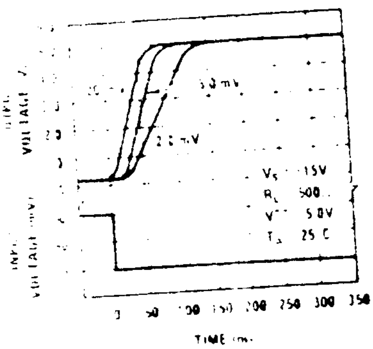


Transfer Function

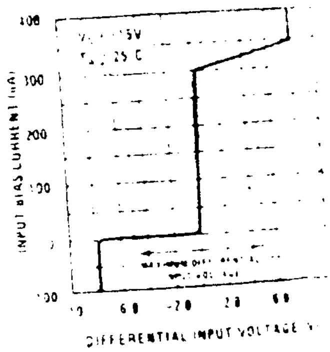




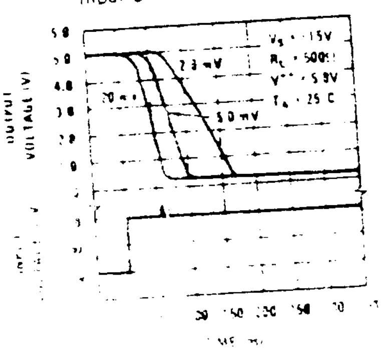
Response Time for Various Input Overdrives



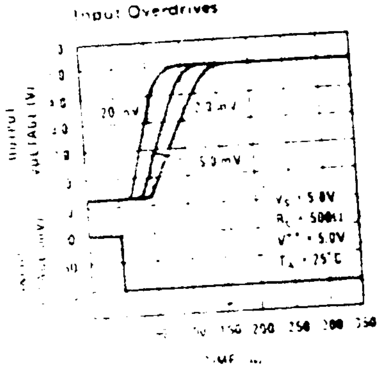
Input Characteristics



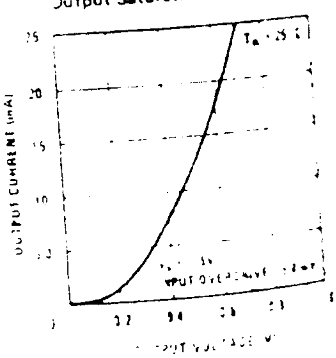
Response Time for Various Input Overdrives

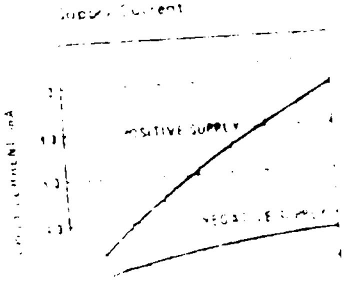


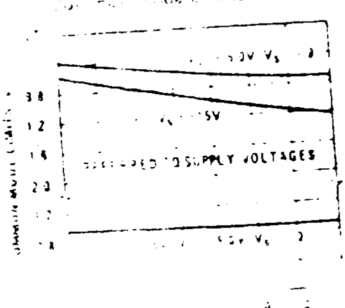
Response Time for Various Input Overdrives

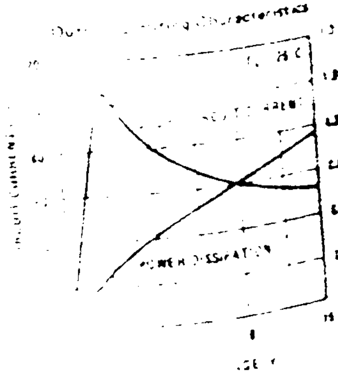


Output Saturation Voltage

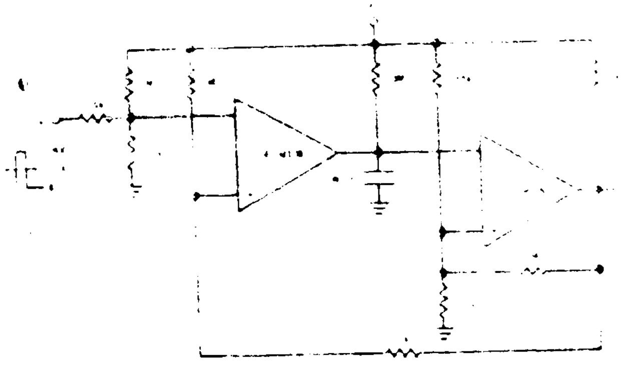




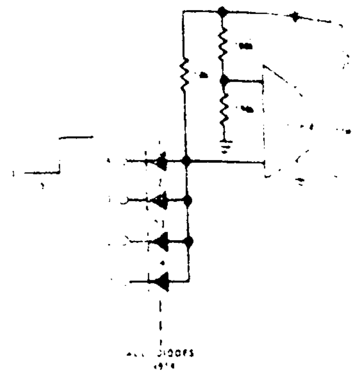




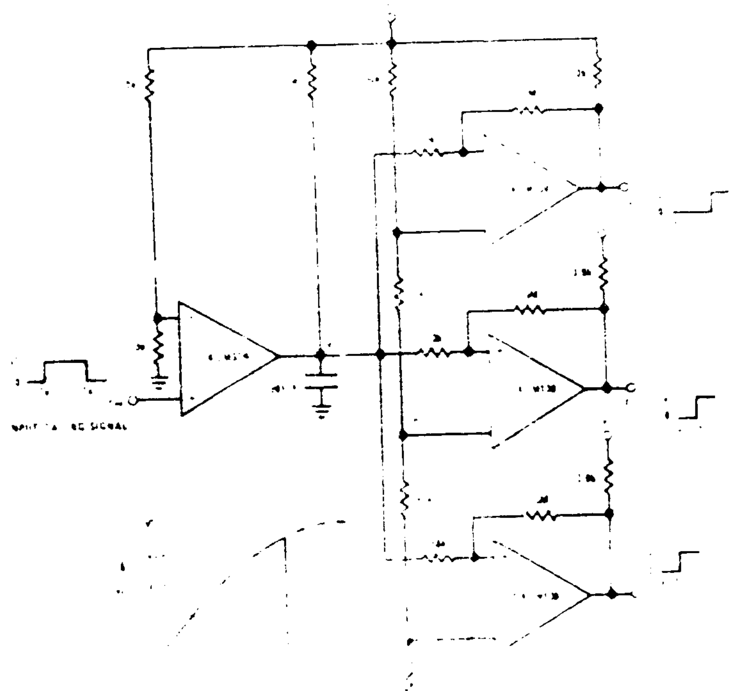
Typical Applications

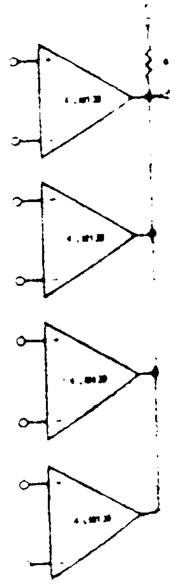


One-Shot Multivibrator with Input Lock Out



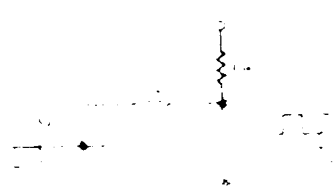
Large Fan-in AND Gate

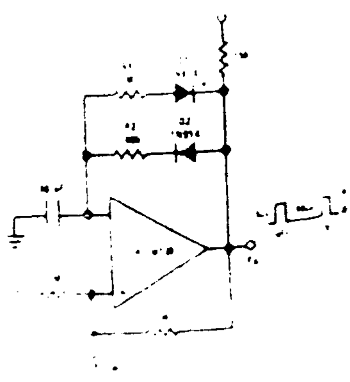




ORing the Outputs

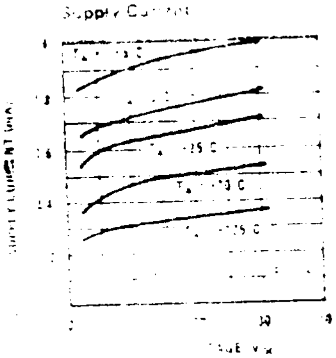
Time Delay Generator



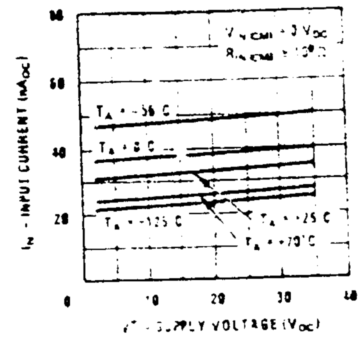


Typical Performance Characteristics LM139/LM239/LM339, LM139A/LM339A, LM3302

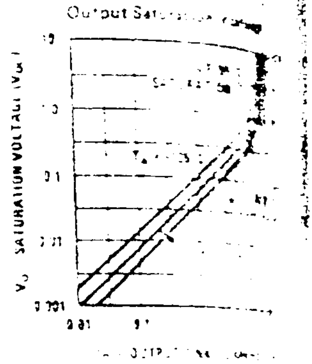
Supply Current



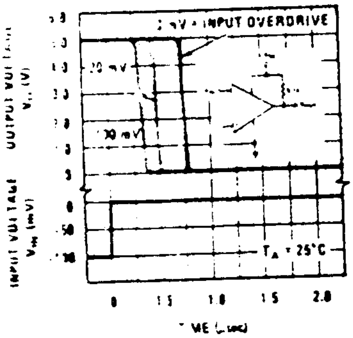
Input Current



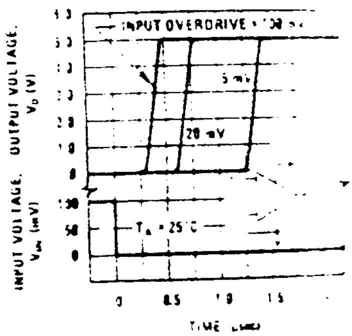
Output Saturation Voltage



Response Time for Various Input Overdrives — Negative Transition

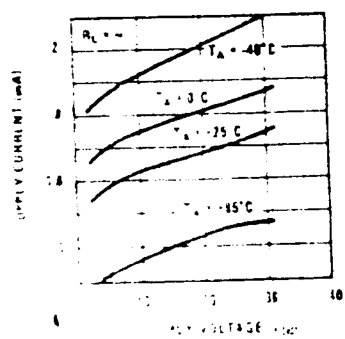


Response Time for Various Input Overdrives — Positive Transition

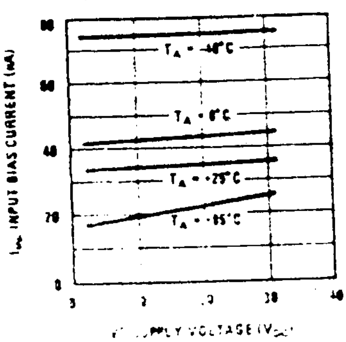


Typical Performance Characteristics LM2901

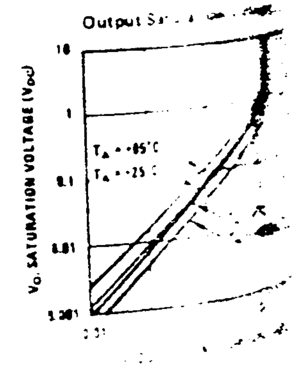
Supply Current



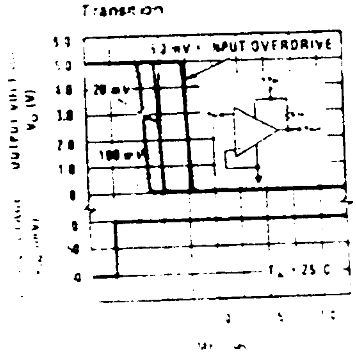
Input Current



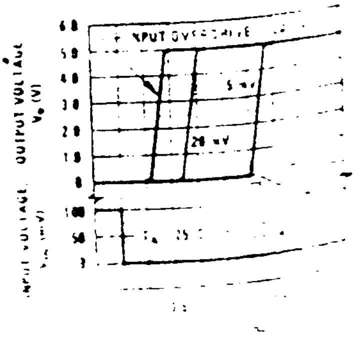
Output Saturation Voltage



Response Time for Various Input Overdrives—Negative Transition



Response Time for Various Input Overdrives—Positive Transition



...on Hints

...es are high gain, wide bandwidth ...ke most comparators, can easily ...tput lead is inadvertently allowed ...ple to the inputs via stray ...shows up only during the output ...tervals as the comparator chan... ...upply bypassing is not required ...blem. Standard PC board layout ...ces stray input-output coupling. ...ut resistors to < 10 kΩ reduces ...gnal levels and finally, adding even ...(1 to 10 mV) of positive feedback ...uses such a rapid transition that ...e to stray feedback are not possible. ...g the IC and attaching resistors to ...se input-output oscillations during ...ion intervals unless hysteresis is ...ut signal is a pulse waveform, with ...st ...e and fall times, hysteresis is not ...

... of any unused comparators should be ...

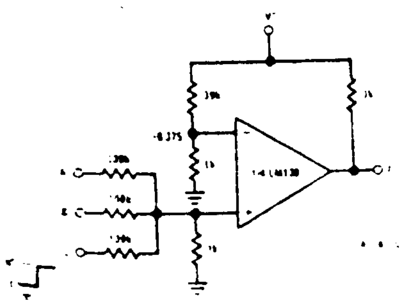
...etwork of the LM139 series establishes a ...which is independent of the magni... ...the power supply voltage over the range ...2 V_{DC} to 30 V_{DC}.

...unnecessary to use a bypass capacitor ...the power supply line.

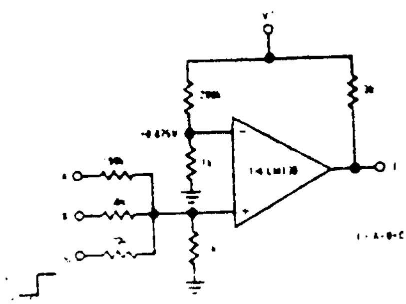
The differential input voltage may be larger than V$^+$ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than -0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in the applications section.

The output of the LM139 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V$^+$ terminal of the LM139A package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V$^+$) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω r_{sat} of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.

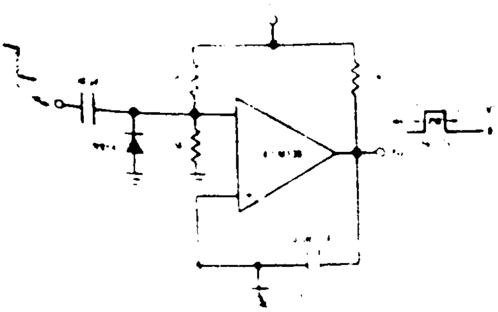
...ical Applications (V$^+$ = 15 V_{DC})

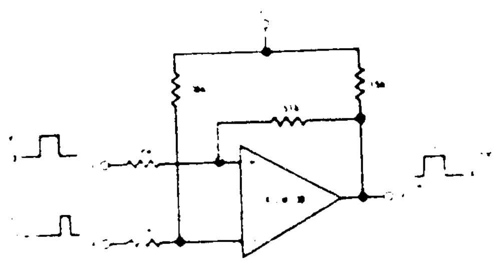


AND Gate



...R Gate





National Semiconductor

73MXX Series 3-Terminal Positive Regulators

eral Description

...es of three terminal regulators is ... fixed output ...ges, making them ... ge of applications ... these is ... eliminating ... distribution ... with single point regulation. The ... these regulators can be used in ... instrumentation, HiFi, and other solid ... equipment. Although designed primarily ... regulators, these devices can be used ... components to obtain ... voltages ...

...78MXX series is available in the plastic TO-202 ... This package allows these regulators to deliver ...5A if adequate heat sinking is provided. Current ... is included to limit the peak output current to ...value. Safe area protection for the output transis... provided to limit internal power dissipation. ...al power dissipation becomes too high for the ...king provided, the thermal shutdown circuit ...er preventing the IC from overheating.

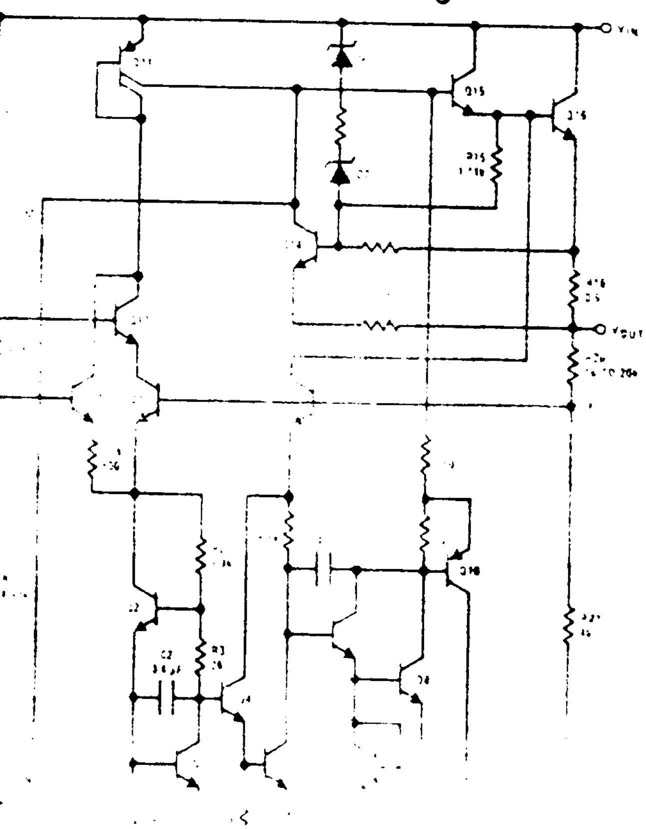
Considerable effort was expended to make the LM78MXX series of regulators ... the number of external components ... the output ... bypassing is needed ... far from the filter ...

For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

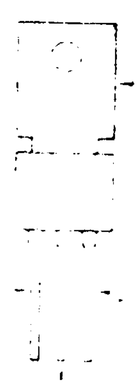
Features

- Output current in excess of 0.5A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in plastic TO-202 package
- Special circuitry allows start-up even if output is pulled to negative voltage (...es)

...matic and Connection Diagrams



Plastic Package



Order Numbers
LM78M05CP
LM78M12CP
LM78M15CP
See Package ...

ximum Ratings

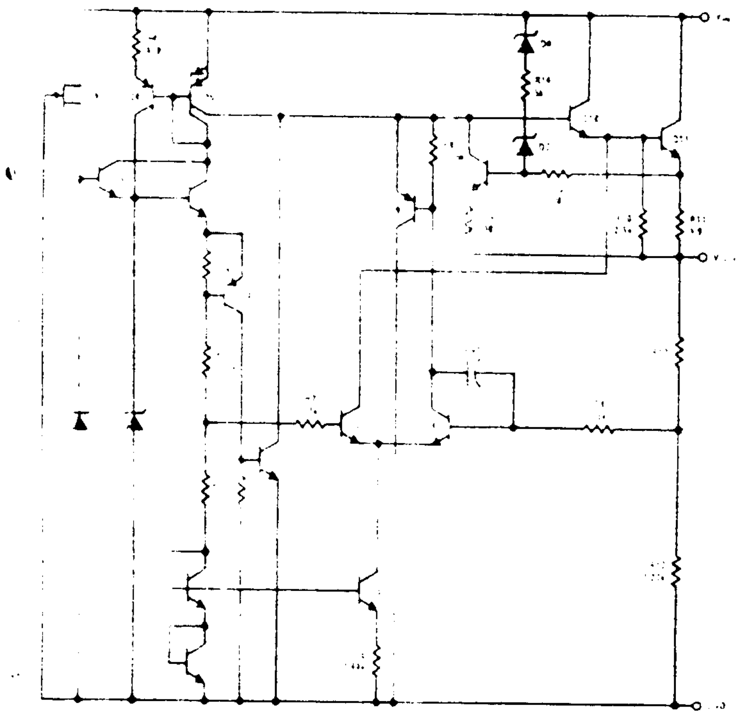
5V)	35V
pation (Note 1)	Internally Limited
ure Range	0°C to +70°C
Temperature	+125°C
e Range	−65°C to +150°C
Soldering, 10 seconds)	+230°C

haracteristics $T_A = 0°C$ to 70°C, I_O = 500 mA unless otherwise noted.

		5V			12V			15V			UNITS
ess otherwise noted)		10V			19V			23V			
	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
e	T_J = 25°C	[illegible]			[illegible]	[illegible]	12.5	14.4	15	15.6	
	$P_D \leq 7.5W$, 5 mA ≤ I_O ≤ 500 mA and $V_{MIN} \leq V_{IN} \leq V_{MAX}$	[illegible]			[illegible]		12.6	14.25		15.75	
		[illegible]			[illegible]		(V_{IN} ≤ 27)	(18 ≤ V_{IN} ≤ 30)			
on	T_J = 25°C, I_O = 100 mA						120			150	
	T_J = 25°C, I_O = 500 mA						240			300	
		[illegible]			[illegible]		[illegible]	(17.6 ≤ V_{IN} ≤ 30)			
on	T_J = 25°C, 5mA ≤ I_O ≤ 500 mA						240			300	
abi							48			60	[illegible]
rent	T_J = 25°C		4				10		4	10	
rent	T_J = 25°C, 5 mA ≤ I_O ≤ 500 mA						0.5			0.5	
	T_J = 25°C, $V_{MIN} \leq V_{IN} \leq V_{MAX}$	[illegible]			[illegible]		1 (V_{IN} ≤ 30)			1 (18 ≤ V_{IN} ≤ 30)	
Voltage	T_J = 25°C, f = 10 Hz–100 kHz		[illegible]			[illegible]			90		
on	f = 120 Hz		[illegible]			[illegible]			69		
Maintain on	T_J = 25°C, I_O = 500 mA	[illegible]			[illegible]			17.6			

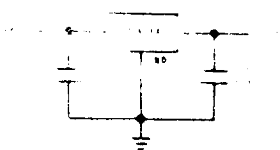
stance without a heat sink for [illegible] 2°C/W for the TO-202 package. Thermal resistance [illegible]
perature is 70°C/W for the TO [illegible]

Equivalent Circuit

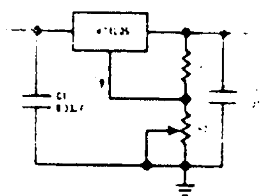


LM78LXX

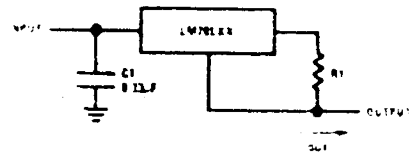
Typical Applications



Fixed Output Regulator



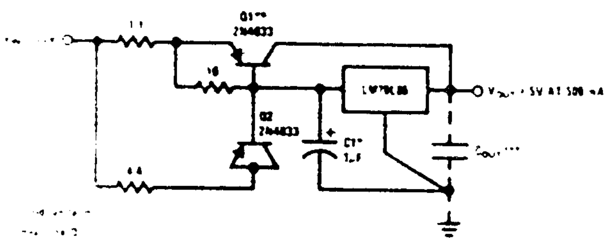
Adjustable Output Regulator



$I_{OUT} = (V_{23}/R1) + I_Q$

$\Delta I_Q = 1.5$ mA over line and load changes

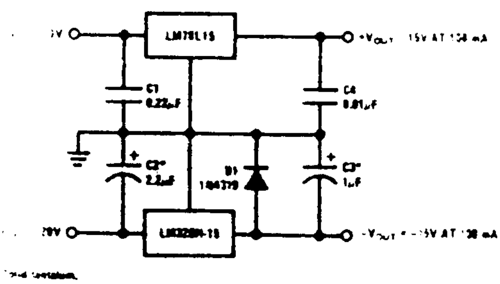
Current Regulator



... ripple rejection and transient response

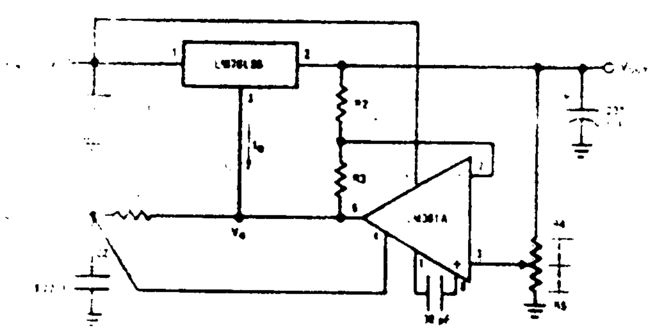
... 250 mA pulsed with t_{ON} = 50 ms

5V 500 mA Regulator with Short Circuit Protection



*Solid tantalum.

±15V, 100 mA Dual Power Supply



*Solid tantalum.

$V_{OUT} = V_Q + 5V$, R1 ...

V_{OUT} ... 5V ...

A 5.5V output ...

Variable Output ... 5V ...

National Semiconductor

LM311 Voltage Comparator

General Description

The LM311 is a voltage comparator that has input currents more than a hundred times lower than devices like the LM306 or LM710C. It is also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Its output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, it can drive lamps or relays, switching voltages up to 40V at currents as high as 50 mA.

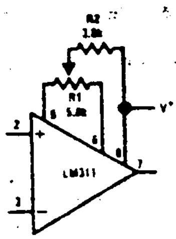
Features

- Operates from single 5V supply
- Maximum input current: 250 nA
- Maximum offset current: 50 nA
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

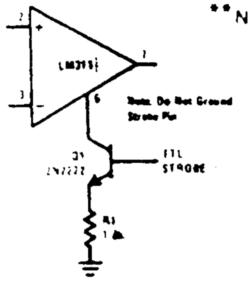
Both the input and the output of the LM311 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM306 and LM710C (200 ns response time vs 40 ns) the device is also much less prone to spurious oscillations. The LM311 has the same pin configuration as the LM306 and LM710C. See the "application hints" of the LM311 for application help.

Auxiliary Circuits**

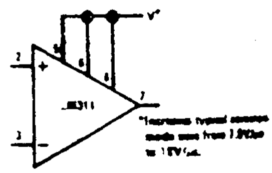
**Note: Pin connections shown on schematic diagram and typical applications are for TO-5 package.



Offset Balancing

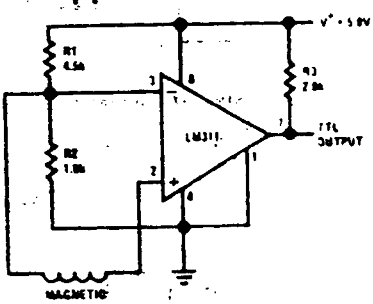


Strobing

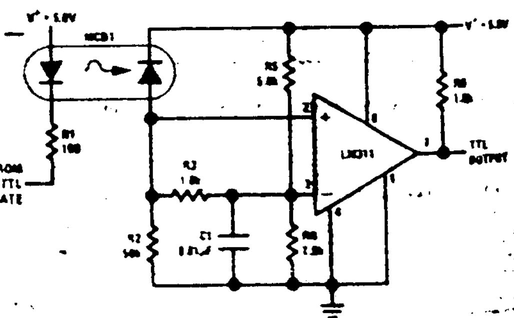


Increasing Input Stage Current*

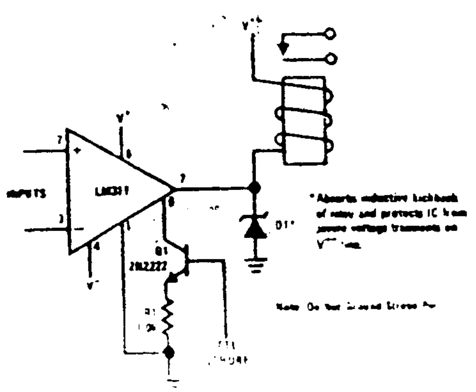
Typical Applications**



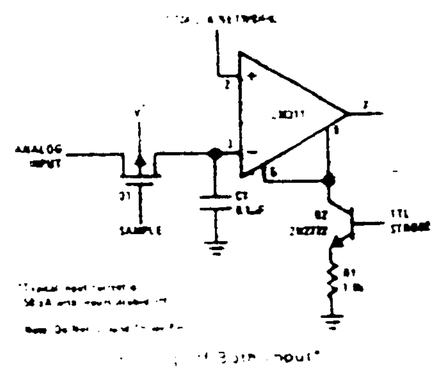
Detector for Magnetic Transducer



Digital Transmission Isolator



Driver with Strobe



Both Input* Stages

Absolute Maximum Ratings

Total Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage (V_{74})	40V
Ground to Negative Supply Voltage (V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (soldering, 10 sec)	300°C
Voltage at Strobe Pin	$V^+ - 5V$

Electrical Characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \le 50k$		2.0	7.5	mV
Input Offset Current (Note 4)	$T_A = 25°C$		6.0	50	nA
Input Bias Current	$T_A = 25°C$		100	250	nA
Voltage Gain	$T_A = 25°C$	40	200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \le -10$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$		0.75	1.5	V
Strobe ON Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \ge 10$ mV, $V_{OUT} = 35V$ $T_A = 25°C$, $I_{STROBE} = 3$ mA		0.2	50	nA
Input Offset Voltage (Note 4)	$R_S \le 50k$			10	mV
Input Offset Current (Note 4)				70	nA
Input Bias Current				300	nA
Input Voltage Range		−14.5	13.8,−14.7	13.0	V
Saturation Voltage	$V^+ \ge 4.5V$, $V^- = 0$ $V_{IN} \le -10$ mV, $I_{SINK} \le 8$ mA		0.23	0.4	V
Positive Supply Current	$T_A = 25°C$		5.1	7.5	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LM311 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and the Ground pin at ground, and $0°C < T_A < +70°C$, unless otherwise specified. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Note 6: Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

REVISED DECEMBER 1983

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

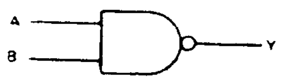
These devices contain four independent 2-input NAND gates.

The SN5400, SN54H00, SN54L00, and SN54LS00, and SN54S00 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7400, SN74H00, SN74LS00, and SN74S00 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

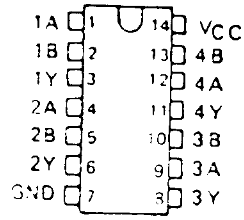
logic diagram (each gate)



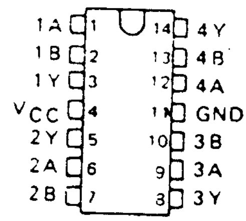
positive logic

$$Y = \overline{A \cdot B} \text{ or } Y = \overline{A} + \overline{B}$$

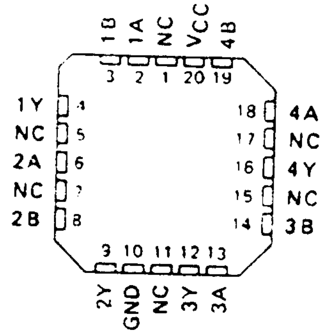
SN5400, SN54H00, SN54L00 . . . J PACKAGE
SN54LS00, SN54S00 . . . J OR W PACKAGE
SN7400, SN74H00 . . . J OR N PACKAGE
SN74LS00, SN74S00 . . . D, J OR N PACKAGE
(TOP VIEW)



SN5400, SN54H00 . . . W PACKAGE
(TOP VIEW)



SN54LS00, SN54S00 . . . FK PACKAGE
SN74LS00, SN74S00 . . . FN PACKAGE
(TOP VIEW)

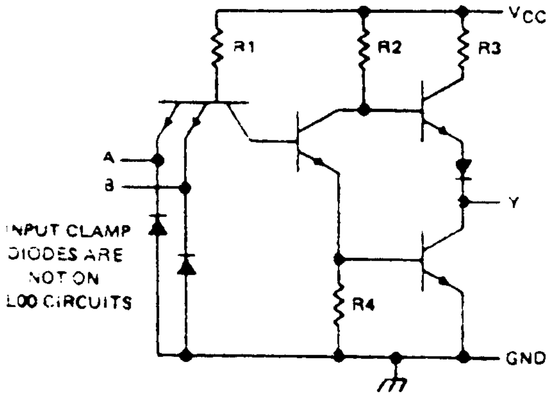


NC – No internal connection

TTL DEVICES 3

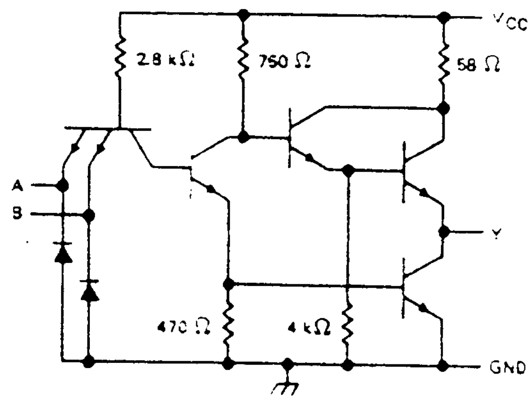
schematics (each gate)

'00, 'L00

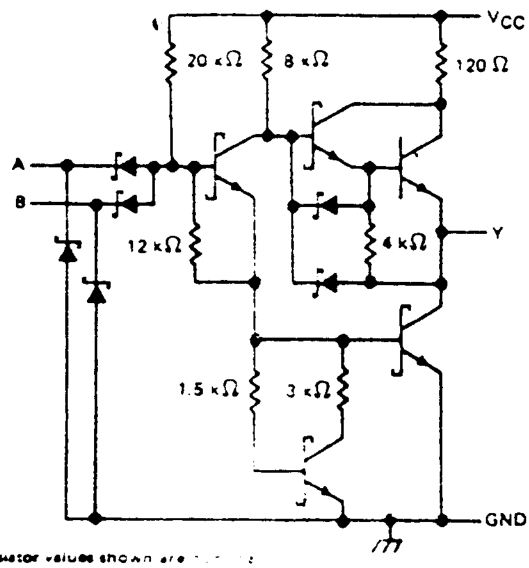


CIRCUIT	R1	R2	R3	R4
'00	4 kΩ	1.6 kΩ	130 Ω	1 kΩ
L00	40 kΩ	20 kΩ	500 Ω	12 kΩ

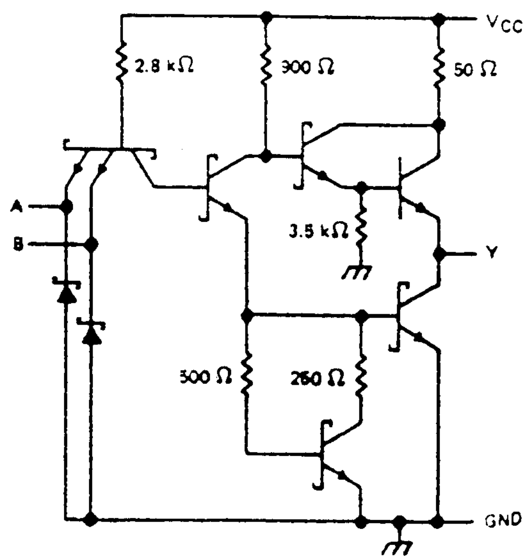
'H00



'LS00



'S00



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1) '00, 'H00, 'LS00, 'S00 7
'L00 . . . .
Input voltage: '00, 'H00, 'L00, 'S00 . . . . 5.5
'LS00 7
Operating free-air temperature range: SN54' . . . . – 55°C to 125
SN74' . . . . 0°C to 70
Storage temperature range . . . . – 65°C to 150

NOTE 1: Voltage values are with respect to network ground terminal.

3 TTL DEVICES

TYPES SN5404, SN54H04, SN54L04, SN54LS04, SN54S04, SN7404, SN74H04, SN74LS04, SN74S04 HEX INVERTERS

REVISED DECEMBER 1983

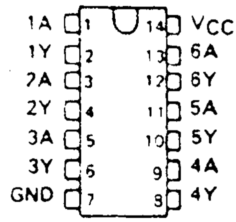
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

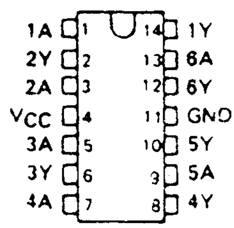
These devices contain six independent inverters.

The SN5404, SN54H04, SN54L04, SN54LS04 and SN54S04 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7404, SN74H04, SN74LS04 and SN74S04 are characterized for operation from 0°C to 70°C.

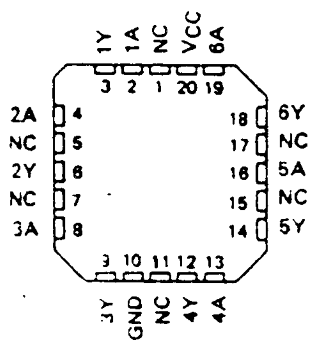
SN5404, SN54H04, SN54L04 . . . J PACKAGE
SN54LS04, SN54S04 . . . J OR W PACKAGE
SN7404, SN74H04 . . . J OR N PACKAGE
SN74LS04, SN74S04 . . . D, J OR N PACKAGE
(TOP VIEW)



SN5404, SN54H04 . . . W PACKAGE
(TOP VIEW)



SN54LS04, SN54S04 . . . FK PACKAGE
SN74LS04, SN74S04 . . . FN PACKAGE
(TOP VIEW)

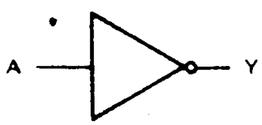


NC – No internal connection

FUNCTION TABLE (each inverter)

INPUTS A	OUTPUT Y
H	L
L	H

logic diagram (each inverter)



positive logic

$$Y = \overline{A}$$

recommended operating conditions

		SN54LS04			SN74LS04			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †			SN54LS04 MIN	TYP ‡	MAX	SN74LS04 MIN	TYP ‡	MAX	UNIT
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	V_{IL} = MAX,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4			0.4	V
	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 8 mA					0.25	0.5	
I_I	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				20			20	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
I_{OS} §	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			1.2	2.4		1.2	2.4	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			3.6	6.6		3.6	6.6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	R_L = 2 kΩ,	C_L = 15 pF		9	15	ns
t_{PHL}						10	15	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

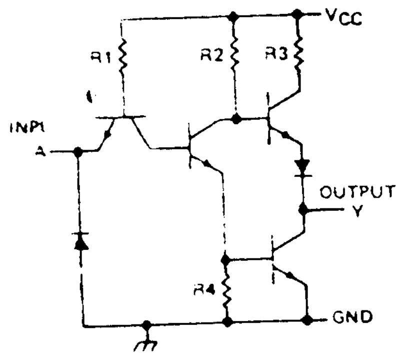
3

TEXAS INSTRUMENTS

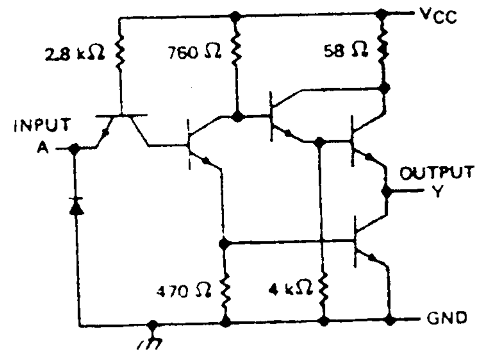
TYPES SN5404, SN54H04, SN54L04, SN54LS04, SN54S04, SN7404, SN74H04, SN74LS04, SN74S04 HEX INVERTERS

schematics (each gate)

'04, 'L04

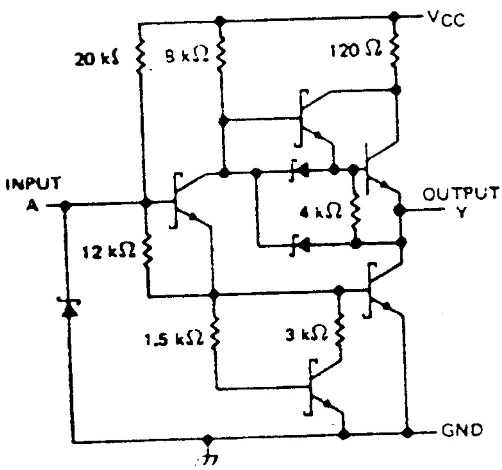


'H04

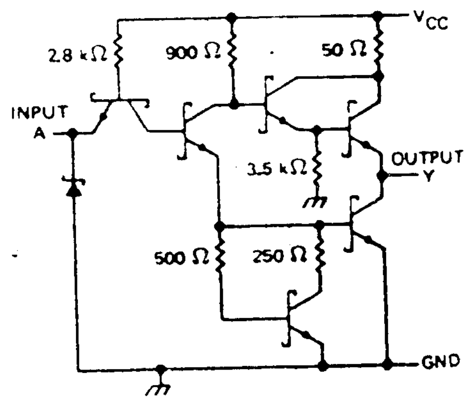


CIRCUIT	R1	R2	R3	R4
'04	4 kΩ	1.6 kΩ	130 Ω	1 kΩ
'L04	40 kΩ	20 kΩ	500 Ω	12 kΩ

'LS04



'S04



• Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC [illegible] '04, 'H04, 'LS04, 'S04 . . . . . .
'L04 . . . . . .

Input voltage: '04, 'H04, 'L04, 'S04 . . . . . .
'LS04 . . . . . .

Operating free-air temperature range: SN54' . . . . . . −55°C to
SN74' . . . . . . 0°C to

Storage temperature range . . . . . . −65°C to

NOTE 1: Voltage values are with respect to network ground terminal.

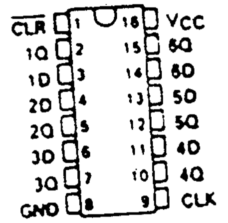
TTL DEVICES

DECEMBER 1972 – REVISED DECEMBER 1983

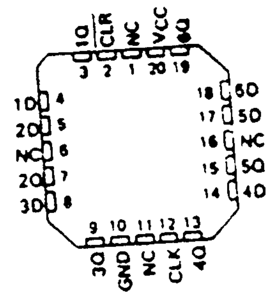
'174, 'LS174, 'S174 . . . HEX D-TYPE FLIP-FLOPS
'175, 'LS175, 'S175 . . . QUADRUPLE D-TYPE FLIP-FLOPS

- '174, 'LS174, 'S174 Contain Six Flip-Flops with Single-Rail Outputs
- 175, 'LS175, 'S175 Contain Four Flip-Flops with Double-Rail Outputs
- Three Performance Ranges Offered: See Table Lower Right
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications include:
  Buffer/Storage Registers
  Shift Registers
  Pattern Generators

SN54174, SN54LS174, SN54S174 . . . J OR W PACKAGE
SN74174 . . . J OR N PACKAGE
SN74LS174, SN74S174 . . . D, J OR N PACKAGE
(TOP VIEW)



SN54LS174, SN54S174 . . . FK PACKAGE
SN74LS174, SN74S174 . . . FN PACKAGE
(TOP VIEW)



description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the '175, 'LS175, and S175 feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These circuits are fully compatible for use with most TTL circuits.

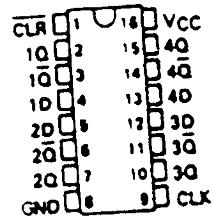
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

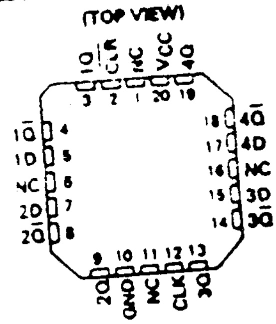
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady state input conditions were established.
† = '175, 'LS175, and 'S175 only.

TYPES	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'174, '175	35 MHz	38 mW
'LS174, 'LS175	40 MHz	14 mW
'S174, 'S175	110 MHz	75 mW

SN54175, SN54LS175, SN54S175 . . . J OR W PACKAGE
SN74175 . . . J OR N PACKAGE
SN74LS175, SN74S175 . . . D, J OR N PACKAGE
(TOP VIEW)



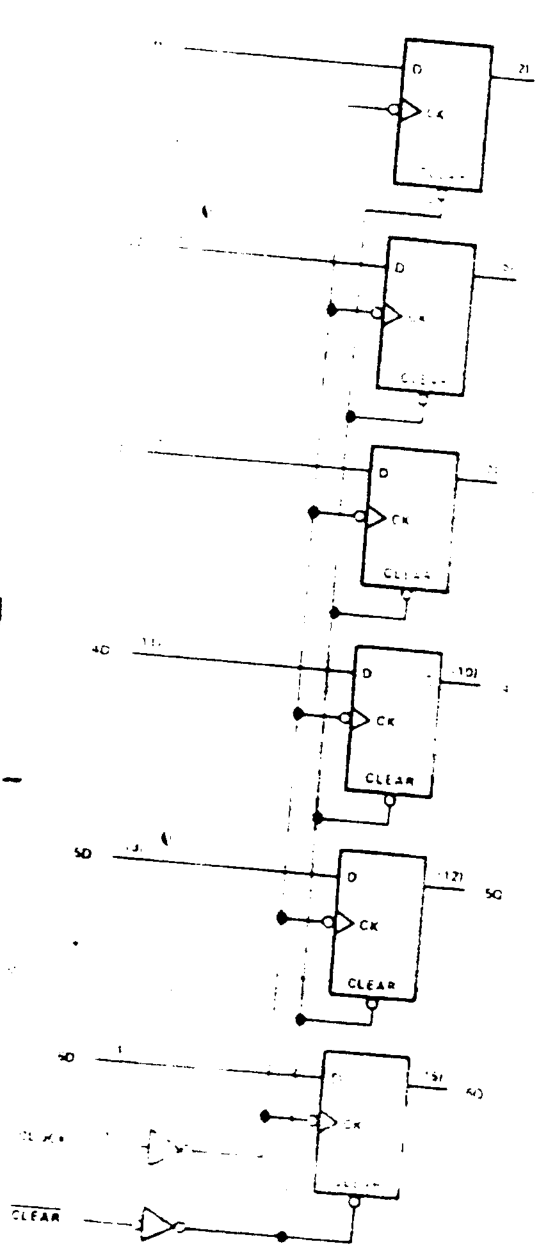
SN54LS175, SN54S175 . . . FK PACKAGE
SN74LS175, SN74S175 . . . FN PACKAGE
(TOP VIEW)



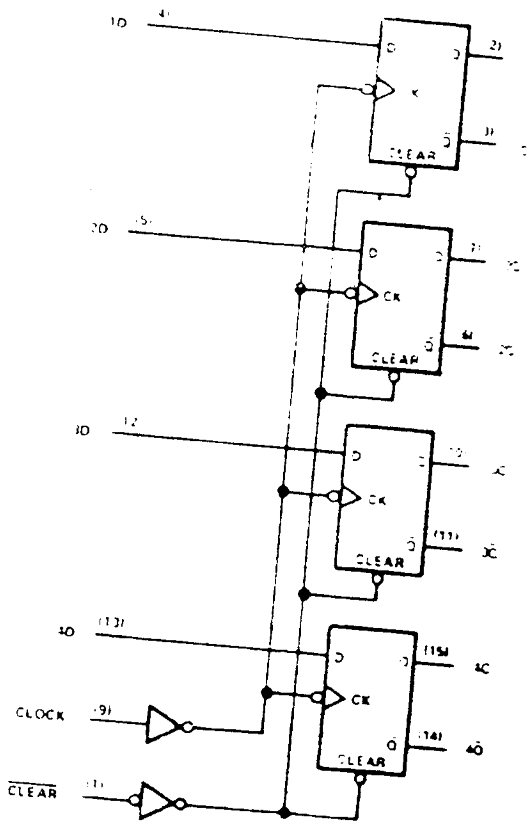
NC – No internal connection

logic diagrams

'174, 'LS174, 'S174



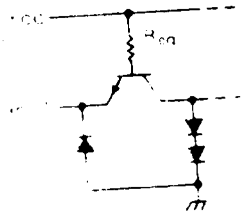
'175, 'LS175, 'S175



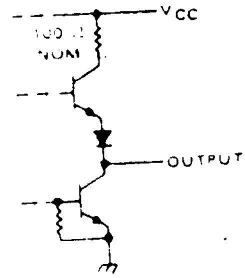
schematics of inputs and outputs

SN54174, SN54175, SN74174, SN74175

EQUIVALENT OF ALL INPUTS

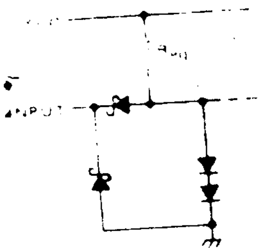


TYPICAL OF ALL OUTPUTS



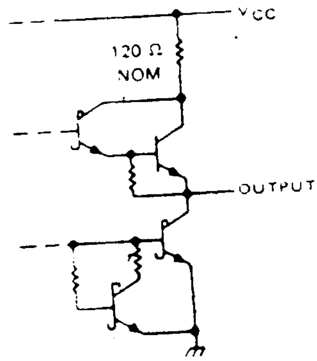
SN54LS174, SN54LS175, SN74LS174, SN74LS175

EQUIVALENT OF ALL INPUTS



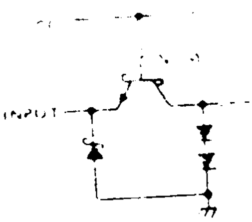
Clock R_{eq} = 17 kΩ NOM
Clear, D R_{eq} = 20 kΩ NOM

TYPICAL OF ALL OUTPUTS

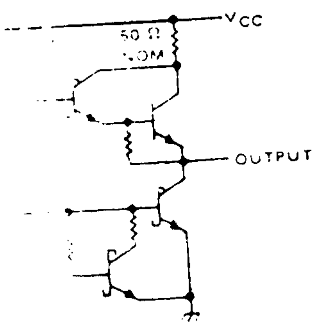


SN54S174, SN54S175, SN74S174, SN74S175

EQUIVALENT OF ALL INPUTS



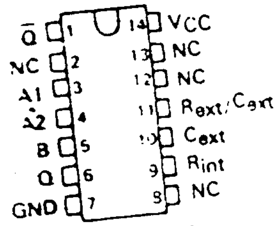
TYPICAL OF ALL OUTPUTS



- ...ble Output Pulse Width
  ... 35 ns Typ
  ... C_{ext} ... 40 ns to 28 Seconds
- ...ompensation for Virtual
  ...ure Independence
- ...e Operation up to 90%
  ...cle
- ...apability

SN54121 ... J OR W PACKAGE
SN54L121 ... J PACKAGE
SN74121 ... J OR N PACKAGE

(TOP VIEW)



NC - No internal connection

FUNCTION TABLE

INPUTS			OUTPUTS	
A1	A2	B	Q	Q̄
[illegible]	[illegible]	[illegible]	[illegible]	H
[illegible]	X	H	L†	H†
[illegible]	L	H	L†	H†
[illegible]	X	L	L†	H†
[illegible]	H	X	⎍	⎏
[illegible]	↓	H	⎍	⎏
[illegible]	H	H	⎍	⎏
[illegible]	↓	H	⎍	⎏
L	X	↑	⎍	⎏
X	L	↑	⎍	⎏

...lanation of function table symbols, see page ...
†These ...nes of the function table assume that the indicated steady state conditions at the A and B inputs have been setup long enough ...plete any pulse started before the setup.

...on

...e multivibrators feature dual negative-transition-triggered inputs and a single positive-transition-triggered input ...h can be used as an inhibit input. Complementary output pulses are provided.

...se triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. ...mitt-trigger input circuitry (TTL hysteresis) for the B input allows jitter-free triggering from inputs with transition ...es as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high ...munity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

...nce fired, the outputs are independent of further transitions of the inputs and are a function only of the timing ...mponents. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from ...0 nanoseconds to 28 seconds by choosing appropriate timing components. With no external timing components ...e, R_{int} connected to V_{CC}, C_{ext} and R_{ext}/C_{ext} open), an output pulse of typically 30 or 35 nanoseconds is achieved ...which may be used as a d-c triggered reset signal. Output rise and fall times are TTL compatible and independent of ...ulse length.

...ulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. ...most applications pulse stability will only be limited by the accuracy of external timing components.

...tter free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capac... ...ance (10 pF to 10 µF) and more than one decade of timing resistance (2 kΩ to 30 kΩ for the SN54121/SN54L121 ...d 2 kΩ to 40 kΩ for the SN74121). Throughout these ranges, pulse width is defined by the relationship $t_{w(out)} = C_{ext}R_T\ln 2 \approx 0.7\ C_{ext}R_T$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000 µF and timing ...esistance as low as 1.4 kΩ may be used. Also, the range of jitter-free output pulse widths is extended if V_{CC} is held to 5 volts and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_T. Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

TTL DEVICES 3

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

...ximum ratings over operating free-air temperature range (unless otherwise noted)

...oltage, V_{CC} (see Note 1) '121 .... 7 V
'L121 .... 8 V
...ltage .... 5.5 V
...ng free-air temperature range: SN54121, SN54L121 .... − 55°C to 125°C
SN74121 .... 0°C to 70°C
...temperature range .... − 65°C to 150°C

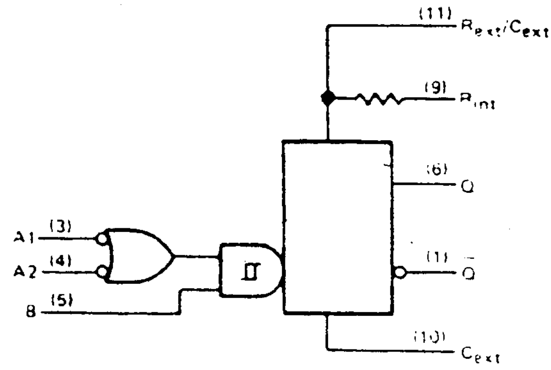
...oltage values are with respect to network ground terminal.

...led operating conditions

		SN54121 SN74121 MIN	SN54121 SN74121 NOM	SN54121 SN74121 MAX	SN54L121 MIN	SN54L121 NOM	SN54L121 MAX	UNIT
...tage	54 Family	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25				
...h-level output current				− 0.4			− 0.2	mA
...w-level output current				16			8	mA
...te of rise or fall of input pulse	Schmitt input B	1			1			V/s
	Logic inputs A1, A2	1			1			V/µs
...put pulse width		50			100			ns
...ternal timing capacitance	54 Family	1.4		30	1.4		30	kΩ
	74 Family	1.4		40				
...ternal timing capacitance		0		1000	0		1000	µF
...ty cycle	$R_T = 2\ k\Omega$			67			67	%
	$R_T = MAX\ R_T$			90			90	
...perating free-air temperature	54 Family	− 55		125	− 55		125	°C
	74 Family	0		70				

TTL DEVICES

logic diagram (positive logic)



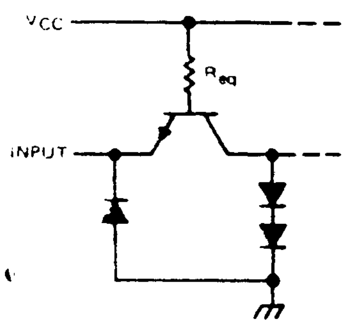
121 R_{int} = 2 kΩ NOM
'L121 R_{int} = 4 kΩ NOM

Pin numbers shown on logic notation are for J or N packages

NOTES 1. An external capacitor may be connected between C_{ext} (positive) and R_{ext}/C_{ext}.
2. To use the internal timing resistor, connect R_{int} to V_{CC}. For improved pulse width accuracy and repeatability, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open circuited.

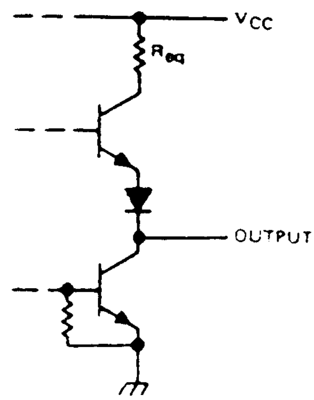
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



INPUT	R_{eq} NOM '121	R_{eq} NOM 'L121
[illegible]	[illegible]	[illegible] kΩ
A2	4 kΩ	8 kΩ
B	2 kΩ	4 kΩ

TYPICAL OF BOTH OUTPUTS



'121 R_{eq} = 1[illegible]0 Ω NOM
'L121 R_{eq} = 250 Ω NOM