MICRO COUNT

Micro Controller Based Production Data Counter

Submitted by

K. S. Ramesh

M. Robert Prakash Babu

R. Seshadri

N. Suresh Kumar

Under the Guidance of

Mr. N. Sanjeevi Ramanathan, M.E., MISTE.
Lecturer, Department of E.C.E.

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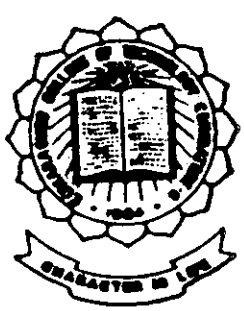

Department of Electronics and Communication Engineering

Kumaraguru College of Technology

Coimbatore-641 006

1994

Department of Electronics and Communication Engineering

Kumaraguru College of Technology

Coimbatore-641006

CERTIFICATE

This is to certify that the project report entitled

Microcount - Micro Controller Based Production Data Counter

has been Submitted by

K. S. RAMESH M. ROBERT PRAKASH BABU

Mr. R. SESHADRI N. SURESH KUMAR

In partial fulfilment for the award of

BACHELOR OF ENGINEERING

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N. Sanjeevi Ramanathan
Faculty Guide 28/3/94

H. O. D.

Certified that the Candidate was Examined by us in the project work Viva-Voce Examination held on ..... and the University Register No. was .....

Internal Examiner

External Examiner

Knowledge is like a shell,
I am just a child who picks
some of these colourful ones
but when I look back there are
millions others still lying on the
shore of the " OCEAN OF KNOWLEDGE "

Sir ISSAC NEWTON

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SYNOPSIS

Every step is to be meticulously measured in this world where survival exists only for the fittest. Anything that is created should be expressed in quantum. Even a small job like counting becomes cumbersome in an industrial setup where the quantity involved is large. Undoubtedly electronic devices cater to this dire demand.

MICROCOUNT - a microcontroller based production data counter is designed to suit different industrial output. This is a versatile counter that incorporates facilities other than conventional counting, such as total number of packages, machine run time, programming facility for parameter values, lock & key. The counting is done by the TIMER/COUNTER inside the microcontroller 8031 which is fed with pulses from the transducer which is a proximity switch.

The counter along with additional facilities, makes it a highly robust device suitable for automation. The device is equipped with facilities for further innovations in terms of software and hardware to make it compatible with the industrial requirements.

CONTENTS

INTRODUCTION

MICROCOUNT- Microcontroller based production data counter does the function of automatically counting any production output. The objects that are to be counted are sensed by the transducer which is a proximity switch. The proximity switch changes its output state when it encounters any object in its active region. The output pulses from the proximity switch which represent the number of objects that had been sensed by the transducer is fed to the inbuilt counter in the microcontroller 8031 through a buffer. The counter starts the counting process by incrementing its previous value each time when a change of state occurs at its input.

2.1 WHY A MICROPROCESSOR

A microprocessor inherently is known for its high degree of accuracy coupled with speed which are essential parameters of any efficient system. A simple dedicated chip for counting would only suffice the main operation of counting. Additional facilities such as displaying the process of counting, set target, total production of the day, machine run time & various other provisions could be met efficiently only by a microprocessor.

As microprocessor is a programmable device it offers high flexibility by means of updation and revision in the software. Maximum efficiency could be achieved by a better intellectual software. A microprocessor is highly compatible with computers which aids in the debugging of the software. Miniaturisation being the order of the day, the use of microprocessor considerably reduces the size of device without any negative influence on its efficency.

Hence the microprocessor in the design of real time industrial applications is highly indispensible.

2.2 THE LOGIC BEHIND SELECTING 8031

The standard eight bit processor 8085 is devoid of TIMER/COUNTER which is vital for our MICROCOUNT. In order to realise all the functions of MICROCOUNT using 8085 , external interfaces are essential. This increases the hardware and the cost.

The Intel's 8031 microcontroller belongs to MCS-51 family. It is a very popular microcontroller because of its unique architecture and powerful instruction set. As 8031 has built-in TIMER/COUNTER it finds wide application in the present day industrial field. It proves itself superior when compared to earlier processors in having the following features:

* 8 bit CPU optimized for control applications
* Extensive boolean processing capabilities
* 64 K program memory address space
* 64 K data memory address space
* 128 Bytes of on-chip data RAM
* 32 Bidirectionally and individually addressable I/O lines

* Two sixteen Bit TIMER/COUNTER
* Full duplex UART
* 6 source/ 5 vector interrupt structure with two priority levels

These features influence us to select the 8031 microcontroller.

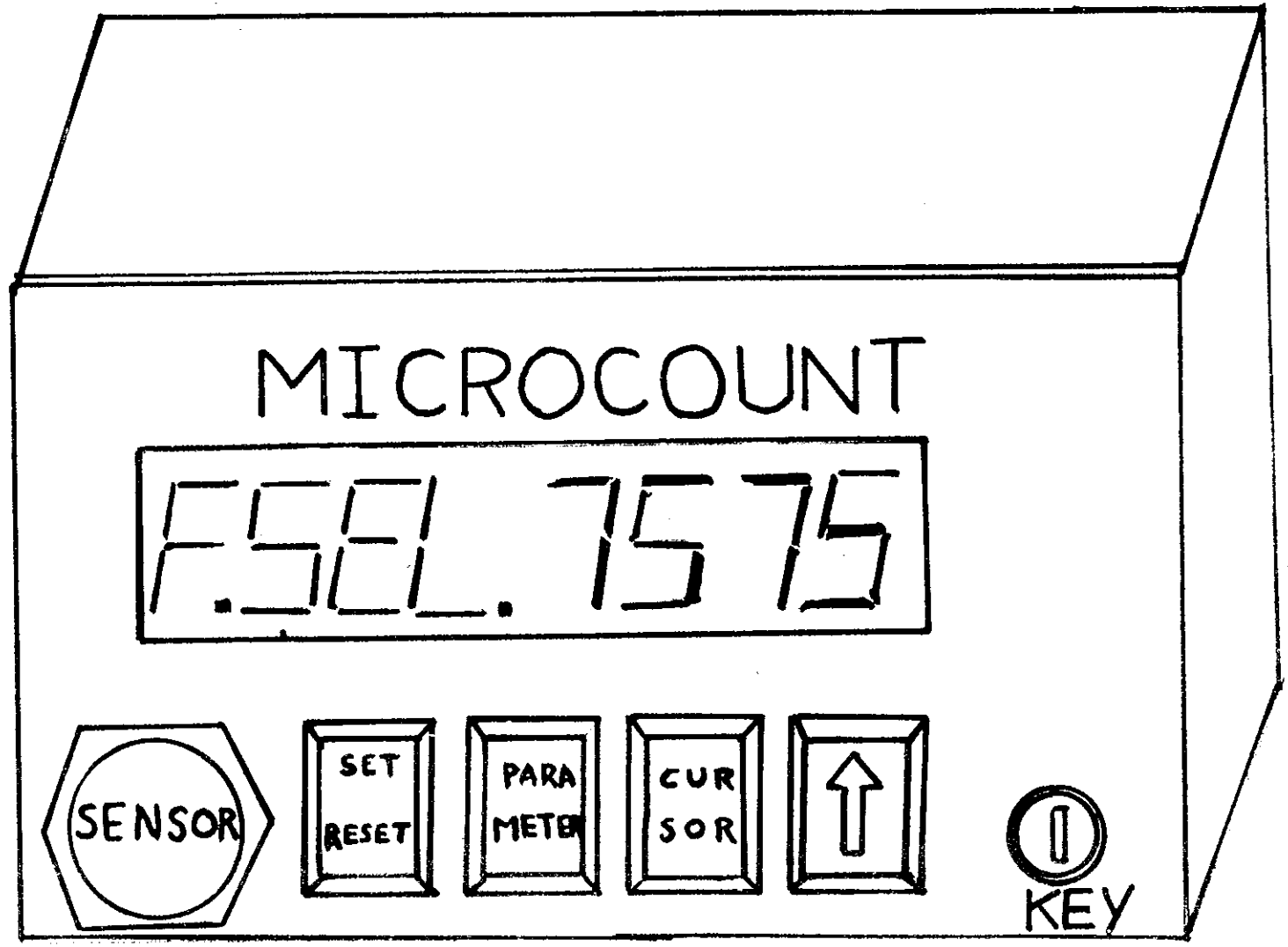


FIG:1. FRONT PANEL OF MICROCOUNT

2.3 ABOUT THE MICROCOUNT

Our MICROCOUNT is designed so as to count the number of any production output. The MICROCOUNT can be used to count items such as bottles, packets, length of paper and also the length of the yarn.

The front panel of the MICROCOUNT has totally eight 7-segment displays. The first four is used for numeric display and the last four for alphabet display. There are four push button switches which enables the counter to be programmed. A lock is provided so as to avoid tampering with the programmed details.

The transducer employed in our MICROCOUNT is a proximity switch, an inductive transducer. The proximity switch gives output pulses when it encounters any metal object within its active surface.

SENSOR

The sensor used in our MICROCOUNT is a proximity switch. A clue about the operation is evident from literal meaning of PROXIMITY - near by.

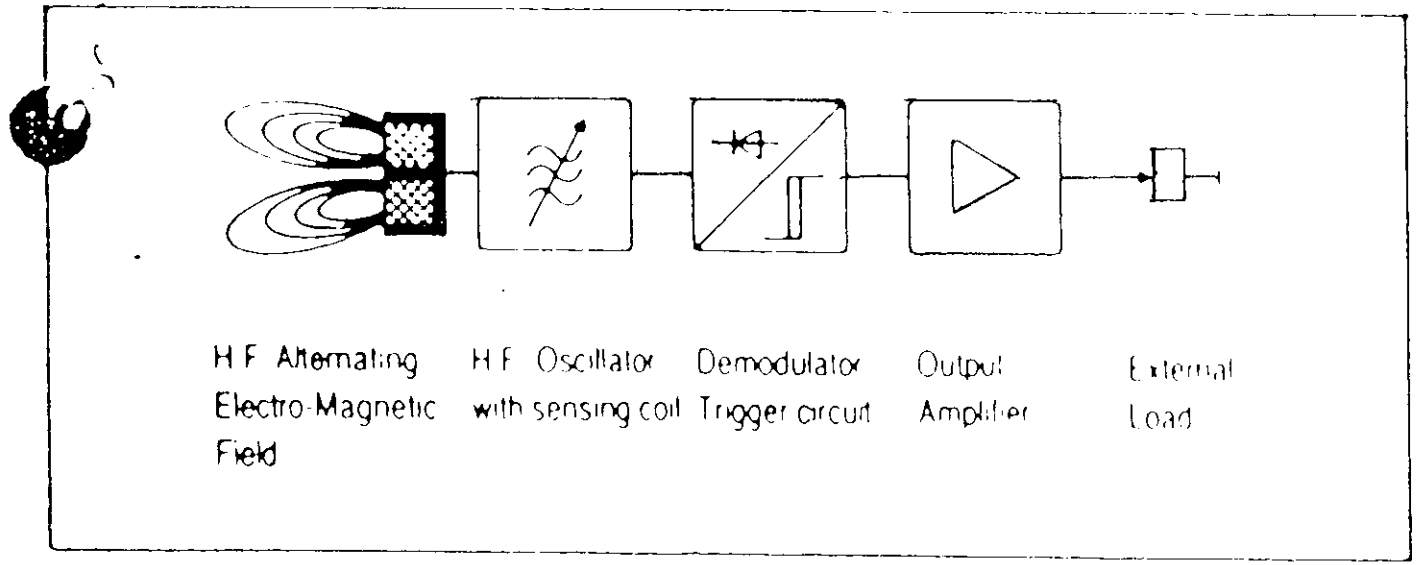


Fig.2 INTERNAL BLOCKS OF THE PROXIMITY SWITCH

Our sensor is basically an inductive transducer. A judicious selection has been done in the selection of inductive transducer from among the various transducers like photo sensor, capacitive transducer and the inductive transducer.

OPERATING PRINCIPLE

An high frequency oscillator generates an alternating electro-magnetic field which radiates through the active surface of the proximity switch. Active surface is the surface through which the high frequency electromagnetic field radiates. The element that activates the switch must come within the switching range of this surface. The oscillator output voltage is demodulated and fed via a trigger circuit to an amplified output stage.

Introduction of an electrically or magnetically conductive material in the region of the "active surface" will cause the oscillator to become "damped". As a result of this damping the oscillator output voltage reduces and at a certain level causes the trigger circuit and hence the output, to change state.

SWITCHING FUNCTION OF PROXIMITY SWITCH

NORMALLY OPEN (N.O.)

When the actuator element is with in the operating distance Sa (active surface damped) the output of the proximity switch is ON.

NORMALLY CLOSED (N.C.)

When the actuator element is within the operating distance Sa (active surface damped) the output of the proximity switch is OFF.

NPN output / negative switching

The load is connected between output and positive lines. It is energised when the output is switched to negative.

PNP output / positive switching

The load is connected between output and negative lines. It is energised when the output is switched to positive.

PROTECTIVE MEASURES

Switching inductive loads:

Our proximity switch contains an internal suppression circuit to limit the effects of switching

inductive loads. Additional suppression is not necessary.

Switch on pulse suppression

At the instant the supply voltage is applied to the proximity switch a special suppression circuit acts to prevent the output from producing unwanted pulses. This also means that the output is inactive for a momentary period at switch on.

Short circuit protection

This protection functions for the duration of the short circuit and prevents damage to the switch. Upon removal of the short circuit the proximity switch is automatically reset into normal operation. Switching of capacitive loads, filament lamps etc is possible without additional protective measures.

Reverse polarity protection

The proximity switch is protected against incorrect polarity connection as standard.

PROXIMITY SWITCH SPECIFICATIONS

Type : INDUCTIVE

MCX-A23-223L-P0

Voltage : 5-30 volts DC

Current : 200 mA

The lock in our MICROCOUNT has two modes namely the PROGRAM MODE and the RUN MODE. The program mode is enabled by opening the lock which enables the supervisor to set the target of production. The parameters to be SET in the program mode are the "FINAL SELECTION" which is the desired target of production and the "PRE-FINAL SELECTION" which is a value slightly less than the final selection value to alert the operator of the target being reached.

The four push-button switches used in our MICROCOUNT are:

1. PARAMETER switch
2. CURSOR switch
3. INCREMENTOR switch

& 4. SET/RESET switch

PARAMETER SWITCH

MICROCOUNT provides with four important parameters which are vital factors that incorporate facilites apart from counting.

The four parameters are

a) Final selection

b) Pre-Final selection

c) Machine run time

d) Total packages

FINAL SELECTION: The Final selection value is essentially the target production. When the MICROCOUNT is in the process of counting and on pressing the parameter button once the operator can see the target value. This value is displayed for six seconds and then it continues displaying the counting sequence.

PRE-FINAL SELECTION It is the value slightly less than the final selection value to alert the operator of the target being reached. While the MICROCOUNT is counting and when the parameter button is pressed twice the operator can see the PreFinal

selection value. This value is displayed for six seconds and then it continues displaying the counting sequence.

MACHINE RUN TIME This parameter keeps counting the time in hours for which the machine had been functioning. When the parameter button is pressed thrice the MICROCOUNT displays machine run time in hours. This display lasts for six seconds and then continues displaying the counting sequence. The machine run time is used for preventive maintainance.

TOTAL PACKAGES The MICROCOUNT keeps counting single pieces and when the set value or target is reached the total package parameter is incremented by one. In a similar way when a number of final targets are reached the total packages parameter has an account of them. The Parameter button when pressed four times will display the total packages that has been despatched, for six seconds after which it continues the counting sequence.

CURSOR & INCREMENTOR SWITCHES When the supervisor intends to set the production details of the day, he

enters the program mode by unlocking the lock. The previous day's target value may be different from present day's value. So in order to alter the values programmed already, he uses the two vital buttons viz cursor & incrementor. The cursor button shifts the control to the digits whose values are to be altered in the clockwise direction (i.e) from MSB to LSB. On pressing the cursor button once the control shifts one digit in the clockwise direction. When the cursor control is exercised on a particular digit, then that digit starts blinking informing the supervisor about the option of alteration of that digit. On pressing the incrementor button the blinking digit gets incremented by one for each time the button is pressed. Hence by the effective use of the cursor and incrementor buttons the desired Final selection & Pre-Final selection values can be apparently set.

SET / RESET BUTTON This button plays a dual role when the MICROCOUNT is in the program mode this acts as a SET, function and RESET function in the run mode.

SET FUNCTION Having apparently set the final and Pre-final selection values using the cursor and incrementer buttons, the values have to be stacked into the memory for program execution. This is enabled by pressing the set button in the program mode. Now the counter when turned to the run mode takes the Final and Pre-Final selection values that had been set.

RESET When the process of counting is in progress and if any detects in package (or) the item itself are noticed by the operator then the defective item is discarded and the MICROCOUNT is reset and the counting starts afresh.

LOCK & KEY

The principle behind this is just similar to an ordinary switch. When the supervisor sets the target values. The lock is opened i.e. in program mode and then it is locked when the production starts in the run mode. This eliminates unwanted tampering of the programmed values by the operator which renders the MICROCOUNT a fool proof one.

2.4 8031 - AN ARCHITECTURAL OVER VIEW

The 8031 is a 8 bit microcontroller. The device has 40 pins, requires a +5V single power supply and operates with a 12 MHz clock.

SPECIAL FUNCTION REGISTER (SFR)

Accumulator: ACC is the accumulator register

B register : This register is used during multiply and divide operation.

PSW : The Program status word register contains program status information.

Stack Pointer : The stack pointer register is 8 bit wide.

Data pointer : The Datapointer (DPTR) holds the 16 bit address.

Ports 0 to 3 : P0, P1, P2 & P3 are the SFR latches of the ports 0,1,2 & 3 respectively.

Serial Data buffer : This is actually 2 seperate register, a transmit buffer and a receive butter register.

Timer register : Register pairs (TH0 , TL0) and (TH1 , TL1) are the 16 bit counting registers

for TIMER / COUNTERS 0 & 1 respectively.

Control Registers : SFRS IP, IE, TMOD, TCON, T2CON, SCON and PCON are the control register.

Port structures : All 4 ports in 8031 are bidirectional. Each consists of a latch, an O/P driver and an input buffer.

All the port 3 pins are multifunctional

P 3.0 RXD (serial input port)

P 3.1 TXD (serial output port)

P 3.2 $\overline{\text{INT0}}$ (external interrupt)

P 3.3 $\overline{\text{INT1}}$ (external interrupt)

P 3.4 T0 (Timer / counter 0 external input)

P 3.5 T1 (Timer / counter 1 external input)

P 3.6 $\overline{\text{WR}}$ (external data memory write strobe)

P 3.7 $\overline{\text{RD}}$ (external data memory read strobe)

ACCESSING EXTERNAL MEMORY

There are 2 external memory the Program memory and Data memory.

$\overline{\text{PSEN}}$ (Program store enable) : Read strobe to access external program memory.

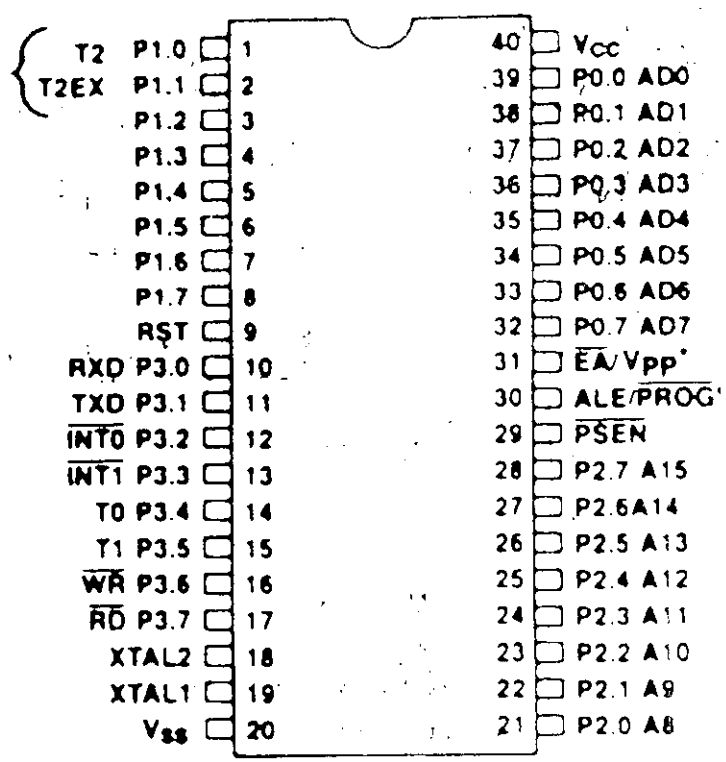
$\overline{\text{RD}}$ & $\overline{\text{WR}}$ strobe to access external Data memory.

Table:1. SPECIAL FUNCTION REGISTERS.

SPECIAL FUNCTION REGISTERS

Symbol	Name	Address
*ACC	Accumulator	0E0H
*B	B Register	0F0H
*PSW	Program Status Word	0D0H
SP	Stack Pointer	81H
DPTR	Data Pointer 2 Bytes	
DPL	Low Byte	82H
DPH	High Byte	83H
*P0	Port 0	80H
*P1	Port 1	90H
*P2	Port 2	0A0H
*P3	Port 3	0B0H
*IP	Interrupt Priority Control	0B8H
*IE	Interrupt Enable Control	0A8H
TMOD	Timer/Counter Mode Control	89H
*TCON	Timer/Counter Control	88H
*+T2CON	Timer/Counter 2 Control	0C8H
TH0	Timer/Counter 0 High Byte	8CH
TL0	Timer/Counter 0 Low Byte	8AH
TH1	Timer/Counter 1 High Byte	8DH
TL1	Timer/Counter 1 Low Byte	8BH
+TH2	Timer/Counter 2 High Byte	0CDH
+TL2	Timer/Counter 2 Low Byte	0CCH
+RCAP2H	T/C 2 Capture Reg. High Byte	0CBH
+RCAP2L	T/C 2 Capture Reg. Low Byte	0CAH
*SCON	Serial Control	98H
SBUF	Serial Data Buffer	99H
PCON	Power Control	87H

* = Bit addressable
+ = 8052 only



DIP

*EPROM only

**Do not connect reserved pins.

Fig:3. PIN CONFIGURATION OF 8031

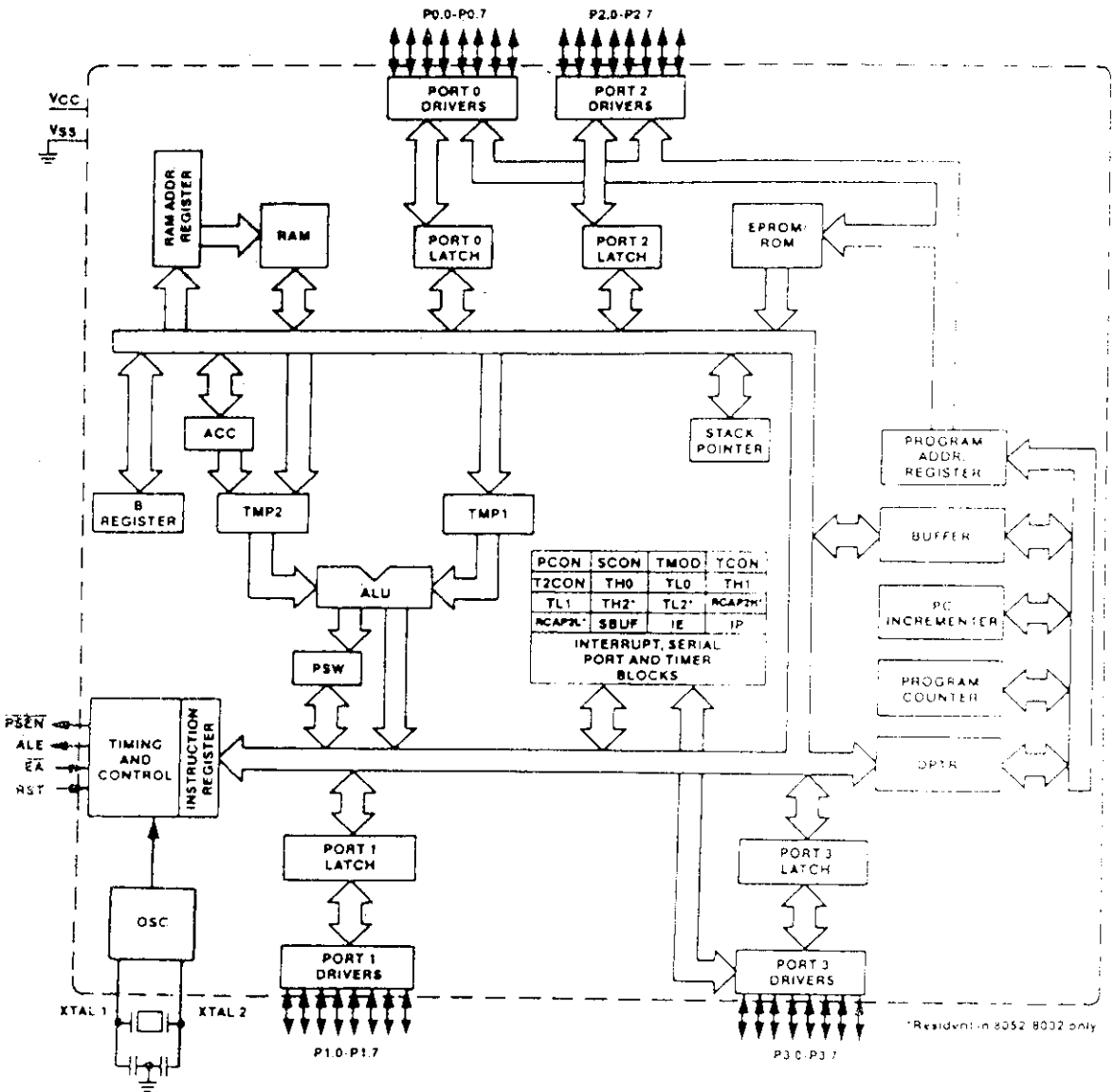


Fig:4. ARCHITECTURE OF 8031

2.5 PROCESS IN A NUTSHELL

The MICROCOUNT has five principal blocks. They are listed as follows

* SENSOR
* BUFFER
* MICROCONTROLLER 8031
* USER KEYBOARD
* DISPLAY

The sensor - a proximity switch that converts the trace of metallic objects within its active surface into electrical pulses. These pulses are given through a buffer to inbuilt counter of 8031 microcontroller. The buffer provides isolation between the transducer & the microcontroller and also avoids loading effects. For each input pulse to the microcontroller the counter increments its value by one. The counter has an account of the number of pulses emanating from the sensor. This in turn is the number of items to be counted.

The user keyboard comprising of four switches, are connected to the microcontroller.

These switches are efficiently utilised to program the microcontroller that renders us with a plethora of industrial facilities.

The output from the microcontroller is given to the display through the display interface. Thus the number of items traversed through the sensor is displayed.

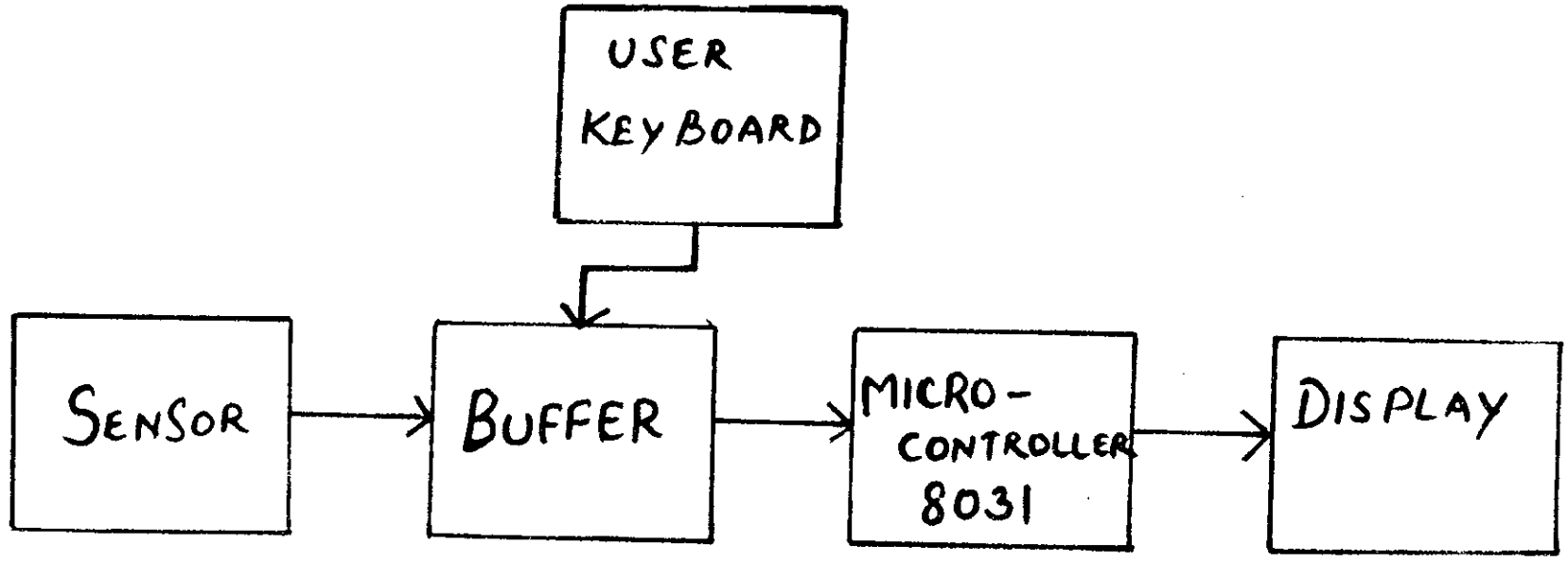
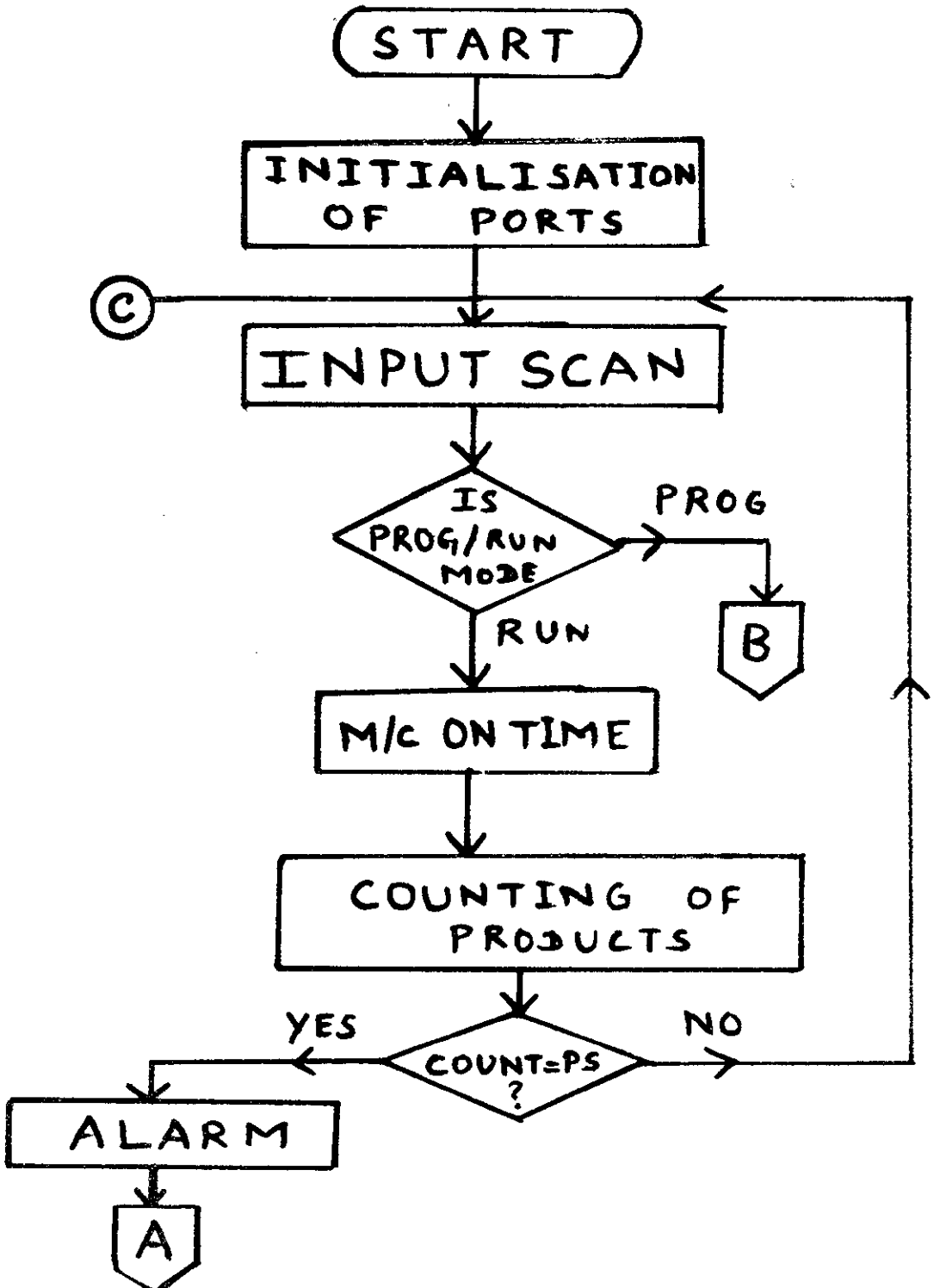
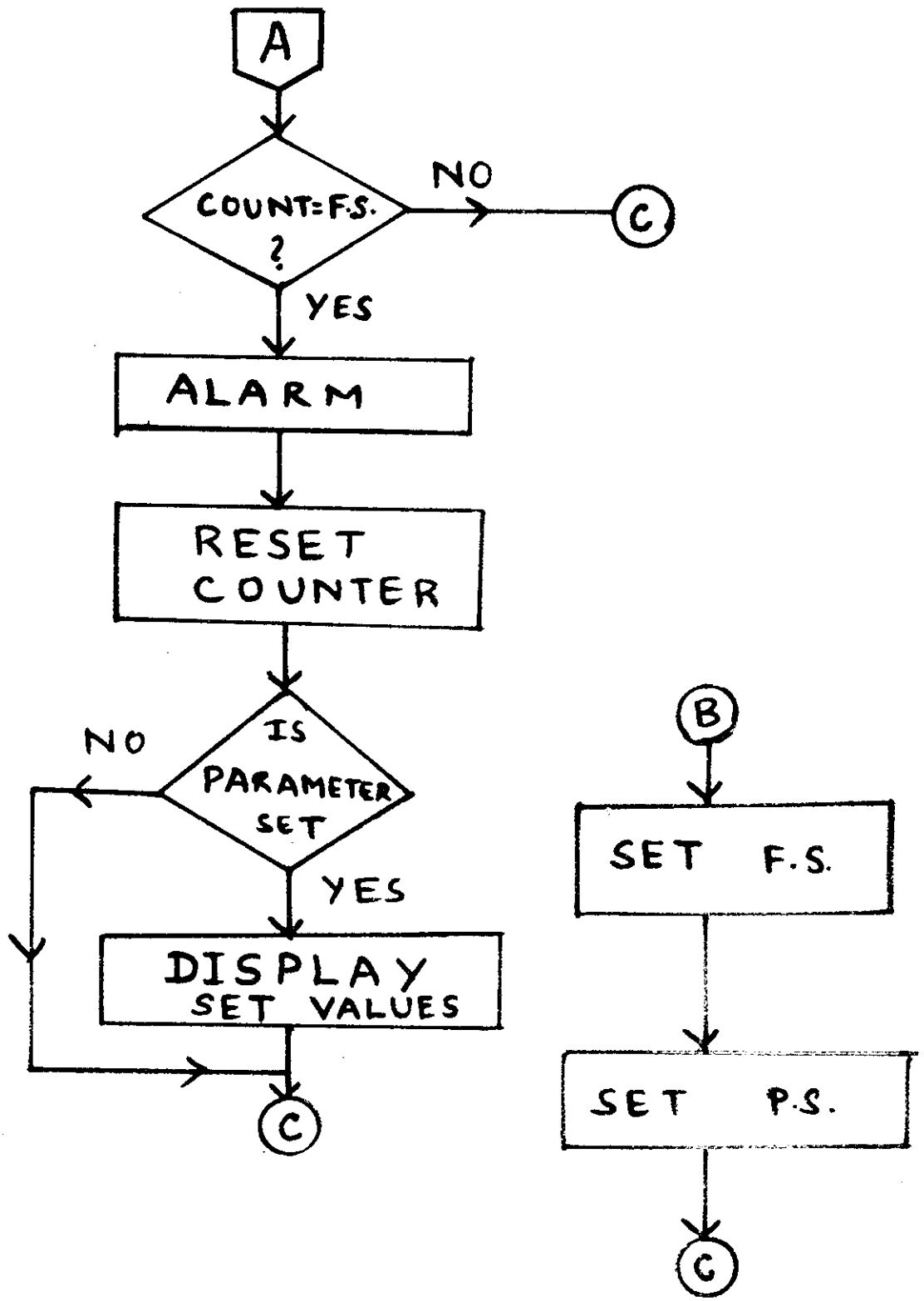


FIG:5 BLOCK DIAGRAM OF MICROCOUNT

F L O W C H A R T


START
INITIALISATION OF PORTS
C
INPUT SCAN
IS PROG/RUN MODE
PROG
B
RUN
M/c ON TIME
COUNTING OF PRODUCTS
YES
COUNT=PS ?
NO
ALARM
A


A
COUNT=F.S.
?
NO
C
YES
ALARM
RESET
COUNTER
IS
PARAMETER
SET
NO
YES
DISPLAY
SET VALUES
C
B
SET F.S.
SET P.S.
C

INITIALISATION OF PORT 1

ADDRESS	OPCODE	MNEMONIC
6000	7590FF	MOV 90,#FF
6003	121900	LCALL 1900
6006	7400	MOV A,#00
6008	904520	MOV DPTR,#4520
600B	F0	MOVX @DPTR,A
600C	904510	MOV DPTR,#4510
600F	F0	MOVX @DPTR,A
6010	904511	MOV DPTR,#4511
6013	F0	MOVX @DPTR,A
6014	904514	MOV DPTR,#4514
6017	F0	MOVX @DPTR,A
6018	7401	MOV A,#01
601A	904512	MOV DPTR,#4512
601D	F0	MOVX @DPTR,A
601E	904522	MOV DPTR,#4522
6021	F0	MOVX @DPTR,A
6022	904523	MOV DPTR,#4523
6025	F0	MOVX @DPTR,A
6026	758C00	MOV 8C,#00
6029	758A00	MOV 8A,#00
602C	758905	MOV 89,#05
602F	D28C	SETB 8C

INITIALISE & INITIATE THE COUNTER

ADDRESS	OPCODE	MNEMONIC
6031	75D000	MOV D0,#00
6034	7800	MOV R0,#00
6036	7901	MOV R1,#01
6038	901000	MOV DPTR,#1000
603B	309005	JNB 90,6043
603E	E9	MOV A,R1
603F	F0	MOVX @DPTR,A
6040	026045	LJMP 6045
6043	E8	MOV A,R0
6044	F0	MOVX @DPTR,A
6045	A3	INC DPTR
6046	309105	JNB 91,604E
6049	E9	MOV A,R1
604A	F0	MOVX @DPTR,A
604B	026050	LJMP 6050
604E	E8	MOV A,R0
604F	F0	MOVX @DPTR,A
6050	A3	INC DPTR
6051	309205	JNB 92,6059
6054	E9	MOV A,R1
6055	F0	MOVX @DPTR,A
6056	02605B	LJMP 605B

INPUT SCAN

```
ADDRESS   OPCODE     MNEMONIC              INPUT  SCAN
  6059    E8         MOV  A,R0
  605A    F0         MOVX @DPTR,A
  605B    A3         INC DPTR
  605C    309305     JNB 93,6064
  605F    E9         MOV  A,R1
  6060    F0         MOVX @DPTR,A
  6061    026066     LJMP 6066
  6064    E8         MOV  A,R0
  6065    F0         MOVX @DPTR,A
  6066    A3         INC DPTR
  6067    309405     JNB 94,606F
  606A    E9         MOV  A,R1
  606B    F0         MOVX @DPTR,A
  606C    026071     LJMP 6071
  606F    E8         MOV  A,R0
  6070    F0         MOVX @DPTR,A
  6071    A3         INC DPTR
  6072    309505     JNB 95,607A
  6075    E9         MOV  A,R1
  6076    F0         MOVX @DPTR,A
  6077    02607C     LJMP 607C


  607A    E8         MOV  A,R0          CHECK FOR PROGRAM
  607B    F0         MOVX @DPTR,A       &  RUN  MODE
  607C    901000     MOV DPTR,#1000
  607F    E0         MOVX A,@DPTR
  6080    B40103     CJNE A,#01,6086
  6083    026093     LJMP 6093
  6086    901005     MOV DPTR,#1005
  6089    E0         MOVX A,@DPTR
  608A    B40003     CJNE A,#00,6090
  608D    026093     LJMP 6093
  6090    0262CC     LJMP 62CC          PROGRAM  MODE
  6093    901001     MOV DPTR,#1001
  6096    E0         MOVX A,@DPTR
  6097    B40103     CJNE A,#01,609D
  609A    026281     LJMP 6281          RUN  MODE
  609D    901004     MOV DPTR,#1004
  60A0    E0         MOVX A,@DPTR
  60A1    B40103     CJNE A,#01,60A7
  60A4    0261F1     LJMP 61F1
  60A7    901000     MOV DPTR,#1000
  60AA    E0         MOVX A,@DPTR
  60AB    B40103     CJNE A,#01,60B1
  60AE    0260B6     LJMP 60B6
```

```
ADDRESS   OPCODE     MNEMONIC
  60B0    B6C28C     CJNE @R0,#C2,60BF
  60B3    026031     LJMP 6031
  60B6    75D000     MOV D0,#00
  60B9    904503     MOV DPTR,#4503
  60BC    E0         MOVX A,@DPTR
  60BD    FC         MOV R4,A
  60BE    0C         INC R4
  60BF    EC         MOV  A,R4
  60C0    903201     MOV DPTR,#3201
  60C3    F0         MOVX @DPTR,A
  60C4    903200     MOV DPTR,#3200
  60C7    7400       MOV  A,#00
  60C9    F0         MOVX @DPTR,A
  60CA    1225FD     LCALL 25FD
  60CD    903501     MOV DPTR,#3501
  60D0    E0         MOVX A,@DPTR
  60D1    9045F0     MOV DPTR,#45F0
  60D4    904503     MOV DPTR,#4503
  60D7    EC         MOV  A,R4
  60D8    F0         MOVX @DPTR,A
  60D9    BCB803     CJNE R4,#B8,60DF
  60DC    0260E2     LJMP 60E2


  60DF    0261F1     LJMP 61F1
  60E2    904500     MOV DPTR,#4500
  60E5    7400       MOV  A,#00
  60E7    F0         MOVX @DPTR,A
  60E8    904503     MOV DPTR,#4503
  60EB    F0         MOVX @DPTR,A
  60EC    904504     MOV DPTR,#4504
  60EF    E0         MOVX A,@DPTR
  60F0    FD         MOV R5,A
  60F1    0D         INC R5
  60F2    ED         MOV  A,R5
  60F3    903201     MOV DPTR,#3201
  60F6    F0         MOVX @DPTR,A
  60F7    903200     MOV DPTR,#3200
  60FA    7400       MOV  A,#00
  60FC    F0         MOVX @DPTR,A
  60FD    1225FD     LCALL 25FD
  6100    903501     MOV DPTR,#3501
  6103    E0         MOVX A,@DPTR
  6104    904501     MOV DPTR,#4501
  6107    F0         MOVX @DPTR,A
  6108    904504     MOV DPTR,#4504
  610B    ED         MOV  A,R5
```

RUN TIME CLOCK

ADDRESS	OPCODE	MNEMONIC
610C	F0	MOVX @DPTR,A
610D	BD0903	CJNE R5,#09,6113
6110	026116	LJMP 6116
6113	0261F1	LJMP 61F1
6116	904501	MOV DPTR,#4501
6119	7400	MOV A,#00
611B	F0	MOVX @DPTR,A
611C	904504	MOV DPTR,#4504
611F	F0	MOVX @DPTR,A
6120	904504	MOV DPTR,#4504
6123	E0	MOVX A,@DPTR
6124	FE	MOV R6,A
6125	0E	INC R6
6126	EE	MOV A,R6
6127	903201	MOV DPTR,#3201
612A	F0	MOVX @DPTR,A
612B	903200	MOV DPTR,#3200
612E	7400	MOV A,#00
6130	F0	MOVX @DPTR,A
6131	1225FD	LCALL 25FD
6134	903501	MOV DPTR,#3501
6137	E0	MOVX A,@DPTR
6138	904502	MOV DPTR,#4502
613B	F0	MOVX @DPTR,A
613C	904505	MOV DPTR,#4505
613F	EE	MOV A,R6
6140	F0	MOVX @DPTR,A
6141	00	NOP
6142	BE3C03	CJNE R6,#3C,6148
6145	02614B	LJMP 614B
6148	0261F1	LJMP 61F1
614B	904502	MOV DPTR,#4502
614E	7400	MOV A,#00
6150	F0	MOVX @DPTR,A
6151	904505	MOV DPTR,#4505
6154	F0	MOVX @DPTR,A
6155	904506	MOV DPTR,#4506
6158	E0	MOVX A,@DPTR
6159	FF	MOV R7,A
615A	0F	INC R7
615B	EF	MOV A,R7
615C	903201	MOV DPTR,#3201
615F	F0	MOVX @DPTR,A
6160	903200	MOV DPTR,#3200

RUN TIME CLOCK

```
ADDRESS   OPCODE      MNEMONIC
  6163    7400        MOV  A,#00
  6165    F0          MOVX @DPTR,A
  6166    1225FD      LCALL 25FD
  6169    903501      MOV DPTR,#3501
  616C    E0          MOVX A,@DPTR
  616D    904507      MOV DPTR,#4507
  6170    F0          MOVX @DPTR,A
  6171    904506      MOV DPTR,#4506
  6174    EF          MOV  A,R7
  6175    F0          MOVX @DPTR,A
  6176    BF3C03      CJNE R7,#3C,617C
  6179    02617F      LJMP 617F
  617C    0261F1      LJMP 61F1
  617F    904507      MOV DPTR,#4507
  6182    7400        MOV  A,#00
  6184    F0          MOVX @DPTR,A
  6185    904506      MOV DPTR,#4506
  6188    F0          MOVX @DPTR,A
  6189    904508      MOV DPTR,#4508
  618C    E0          MOVX A,@DPTR
  618D    FC          MOV R4,A
  618E    0C          INC R4


  618F    EC          MOV  A,R4
  6190    903201      MOV DPTR,#3201
  6193    F0          MOVX @DPTR,A
  6194    903200      MOV DPTR,#3200
  6197    7400        MOV  A,#00
  6199    F0          MOVX @DPTR,A
  619A    1225FD      LCALL 25FD
  619D    903501      MOV DPTR,#3501
  61A0    E0          MOVX A,@DPTR
  61A1    904509      MOV DPTR,#4509
  61A4    F0          MOVX @DPTR,A
  61A5    904508      MOV DPTR,#4508
  61A8    EC          MOV  A,R4
  61A9    F0          MOVX @DPTR,A
  61AA    BC6403      CJNE R4,#64,61B0
  61AD    0261B3      LJMP 61B3
  61B0    0261F1      LJMP 61F1
  61B3    904508      MOV DPTR,#4508
  61B6    7400        MOV  A,#00
  61B8    F0          MOVX @DPTR,A
  61B9    904509      MOV DPTR,#4509
  61BC    F0          MOVX @DPTR,A
  61BD    90450A      MOV DPTR,#450A
```

RUN TIME CLOCK

```
ADDRESS   OPCODE      MNEMONIC
  61C0    E0          MOVX A,@DPTR
  61C1    FD          MOV R5,A
  61C2    0D          INC R5
  61C3    ED          MOV  A,R5
  61C4    903201      MOV DPTR,#3201        RUN  TIME  CLOCK
  61C7    F0          MOVX @DPTR,A
  61C8    903200      MOV DPTR,#3200
  61CB    7400        MOV  A,#00
  61CD    F0          MOVX @DPTR,A
  61CE    1225FD      LCALL 25FD
  61D1    903501      MOV DPTR,#3501
  61D4    E0          MOVX A,@DPTR
  61D5    90450B      MOV DPTR,#450B
  61D8    F0          MOVX @DPTR,A
  61D9    90450A      MOV DPTR,#450A
  61DC    ED          MOV  A,R5
  61DD    F0          MOVX @DPTR,A
  61DE    BD6403      CJNE R5,#64,61E4
  61E1    0261E7      LJMP 61E7
  61E4    0261F1      LJMP 61F1
  61E7    90450A      MOV DPTR,#450A
  61EA    7400        MOV  A,#00


  61EC    F0          MOVX @DPTR,A
  61ED    90450B      MOV DPTR,#450B
  61F0    F0          MOVX @DPTR,A
  61F1    858A10      MOV 10,8A             COUNTING  STARTS
  61F4    E510        MOV  A,10
  61F6    903201      MOV DPTR,#3201
  61F9    F0          MOVX @DPTR,A
  61FA    858C11      MOV 11,8C
  61FD    E511        MOV  A,11
  61FF    903200      MOV DPTR,#3200
  6202    F0          MOVX @DPTR,A
  6203    1225FD      LCALL 25FD
  6206    903500      MOV DPTR,#3500
  6209    E0          MOVX A,@DPTR
  620A    F511        MOV 11,A
  620C    903501      MOV DPTR,#3501
  620F    E0          MOVX A,@DPTR
  6210    F510        MOV 10,A
  6212    902001      MOV DPTR,#2001
  6215    E0          MOVX A,@DPTR
  6216    B51009      CJNE A,10,6222
  6219    902000      MOV DPTR,#2000
  621C    E0          MOVX A,@DPTR
```

ADDRESS	OPCODE	MNEMONIC	
621D	B51102	CJNE A,11,6222	
6220	C296	CLR 96	
6222	902004	MOV DPTR,#2004	
6225	E0	MOVX A,@DPTR	COUNTING IN PROGRESS
6226	B5100C	CJNE A,10,6235	
6229	902003	MOV DPTR,#2003	
622C	E0	MOVX A,@DPTR	
622D	B51105	CJNE A,11,6235	
6230	C297	CLR 97	
6232	026245	LJMP 6245	
6235	121800	LCALL 1800	
6238	901004	MOV DPTR,#1004	
623B	E0	MOVX A,@DPTR	
623C	B40103	CJNE A,#01,6242	
623F	026026	LJMP 6026	
6242	02602F	LJMP 602F	
6245	7905	MOV R1,#05	
6247	7AFF	MOV R2,#FF	
6249	7BFF	MOV R3,#FF	
624B	DBFE	DJNZ R3,624C	
624D	DAFA	DJNZ R2,6249	
624F	D9F6	DJNZ R1,6247	
6251	D296	SETB 96	
6253	D2D7	SETB D7	
6255	904510	MOV DPTR,#4510	
6258	E0	MOVX A,@DPTR	
6259	04	INC A	
625A	F0	MOVX @DPTR,A	
625B	903201	MOV DPTR,#3201	
625E	F0	MOVX @DPTR,A	
625F	903200	MOV DPTR,#3200	
6262	7400	MOV A,#00	
6264	F0	MOVX @DPTR,A	
6265	1225FD	LCALL 25FD	
6268	903501	MOV DPTR,#3501	
626B	E0	MOVX A,@DPTR	
626C	904511	MOV DPTR,#4511	
626F	F0	MOVX @DPTR,A	
6270	904510	MOV DPTR,#4510	
6273	E0	MOVX A,@DPTR	
6274	FC	MOV R4,A	
6275	BC6406	CJNE R4,#64,627E	
6278	7400	MOV A,#00	
627A	904510	MOV DPTR,#4510	
627D	F0	MOVX @DPTR,A	

ADDRESS	OPCODE	MNEMONIC	
627E	026026	LJMP 6026	
6281	901001	MOV DPTR,#1001	
6284	E0	MOVX A,@DPTR	
6285	B40106	CJNE A,#01,628E	
6288	904512	MOV DPTR,#4512	
628B	E0	MOVX A,@DPTR	
628C	04	INC A	
628D	F0	MOVX @DPTR,A	FINAL SELECTION
628E	904512	MOV DPTR,#4512	DISPLAY
6291	E0	MOVX A,@DPTR	
6292	B4010A	CJNE A,#01,629F	
6295	F0	MOVX @DPTR,A	
6296	121400	LCALL 1400	
6299	121500	LCALL 1500	PRE-FINAL SELECTION
629C	0262C9	LJMP 62C9	DISPLAY
629F	B4020A	CJNE A,#02,62AC	
62A2	F0	MOVX @DPTR,A	
62A3	121200	LCALL 1200	
62A6	121500	LCALL 1500	
62A9	0262C9	LJMP 62C9	
62AC	B4030A	CJNE A,#03,62B9	
62AF	F0	MOVX @DPTR,A	RUN TIME DISPLAY
62B0	121600	LCALL 1600	
62B3	121500	LCALL 1500	TOTAL PACKAGES
62B6	0262C9	LJMP 62C9	DISPLAY
62B9	B40407	CJNE A,#04,62C3	
62BC	F0	MOVX @DPTR,A	
62BD	121700	LCALL 1700	
62C0	121500	LCALL 1500	
62C3	B40503	CJNE A,#05,62C9	
62C6	7400	MOV A,#00	
62C8	F0	MOVX @DPTR,A	
62C9	026031	LJMP 6031	
62CC	901001	MOV DPTR,#1001	
62CF	E0	MOVX A,@DPTR	
62D0	B4010C	CJNE A,#01,62DF	
62D3	904520	MOV DPTR,#4520	
62D6	E0	MOVX A,@DPTR	
62D7	04	INC A	
62D8	F0	MOVX @DPTR,A	
62D9	904521	MOV DPTR,#4521	
62DC	7401	MOV A,#01	
62DE	F0	MOVX @DPTR,A	
62DF	904521	MOV DPTR,#4521	
62E2	E0	MOVX A,@DPTR	

ADDRESS	OPCODE	MNEMONIC	
62E3	B40103	CJNE A,#01,62E9	
62E6	0262EC	LJMP 62EC	
62E9	026031	LJMP 6031	
62EC	904520	MOV DPTR,#4520	
62EF	E0	MOVX A,@DPTR	
62F0	B40103	CJNE A,#01,62F6	
62F3	026436	LJMP 6436	SELECTION OF
62F6	B40203	CJNE A,#02,62FC	PARAMETER
62F9	026308	LJMP 6308	SETTING
62FC	B40306	CJNE A,#03,6305	
62FF	7401	MOV A,#01	
6301	904520	MOV DPTR,#4520	
6304	F0	MOVX @DPTR,A	
6305	0262DF	LJMP 62DF	
6308	901002	MOV DPTR,#1002	
630B	E0	MOVX A,@DPTR	
630C	B40106	CJNE A,#01,6315	
630F	904522	MOV DPTR,#4522	
6312	E0	MOVX A,@DPTR	
6313	04	INC A	
6314	F0	MOVX @DPTR,A	
6315	904522	MOV DPTR,#4522	
6318	E0	MOVX A,@DPTR	
6319	B40103	CJNE A,#01,631F	
631C	02633D	LJMP 633D	
631F	B40203	CJNE A,#02,6325	SETTING OF
6322	02637A	LJMP 637A	PRE-FINAL
6325	B40303	CJNE A,#03,632B	VALUE
6328	0263B0	LJMP 63B0	
632B	B40403	CJNE A,#04,6331	
632E	0263ED	LJMP 63ED	
6331	B40506	CJNE A,#05,633A	
6334	7400	MOV A,#00	
6336	904522	MOV DPTR,#4522	
6339	F0	MOVX @DPTR,A	
633A	026308	LJMP 6308	
633D	902000	MOV DPTR,#2000	
6340	E0	MOVX A,@DPTR	
6341	FA	MOV R2,A	
6342	C4	SWAP A	
6343	540F	ANL A,#0F	
6345	FB	MOV R3,A	
6346	901003	MOV DPTR,#1003	
6349	E0	MOVX A,@DPTR	
634A	B40101	CJNE A,#01,634E	

```
ADDRESS   OPCODE     MNEMONIC
  634D    0B         INC R3
  634E    902000     MOV DPTR,#2000
  6351    BB0A02     CJNE R3,#0A,6356
  6354    7B00       MOV  R3,#00
  6356    7CA0       MOV  R4,#A0
  6358    EA         MOV  A,R2
  6359    540F       ANL A,#0F
  635B    4C         ORL A,R4
  635C    F0         MOVX @DPTR,A
  635D    121200     LCALL 1200
  6360    121500     LCALL 1500
  6363    EB         MOV  A,R3
  6364    C4         SWAP A
  6365    FB         MOV R3,A
  6366    EA         MOV  A,R2
  6367    540F       ANL A,#0F
  6369    4B         ORL A,R3
  636A    902000     MOV DPTR,#2000
  636D    F0         MOVX @DPTR,A
  636E    121200     LCALL 1200
  6371    121500     LCALL 1500


  6374    EB         MOV  A,R3
  6375    C4         SWAP A
  6376    FB         MOV R3,A
  6377    026420     LJMP 6420
  637A    902000     MOV DPTR,#2000
  637D    E0         MOVX A,@DPTR
  637E    FA         MOV R2,A
  637F    540F       ANL A,#0F
  6381    FB         MOV R3,A
  6382    901003     MOV DPTR,#1003
  6385    E0         MOVX A,@DPTR
  6386    B40101     CJNE A,#01,638A
  6389    0B         INC R3
  638A    902000     MOV DPTR,#2000
  638D    BB0A02     CJNE R3,#0A,6392
  6390    7B00       MOV  R3,#00
  6392    7C0A       MOV  R4,#0A
  6394    EA         MOV  A,R2
  6395    54F0       ANL A,#F0
  6397    4C         ORL A,R4
  6398    F0         MOVX @DPTR,A
  6399    121200     LCALL 1200
  639C    121500     LCALL 1500
```

```
ADDRESS   OPCODE      MNEMONIC
  639F    EA          MOV  A,R2
  63A0    54F0        ANL A,#F0
  63A2    4B          ORL A,R3
  63A3    902000      MOV DPTR,#2000
  63A6    F0          MOVX @DPTR,A
  63A7    121200      LCALL 1200
  63AA    121500      LCALL 1500
  63AD    026420      LJMP 6420
  63B0    902001      MOV DPTR,#2001
  63B3    E0          MOVX A,@DPTR
  63B4    FA          MOV R2,A
  63B5    C4          SWAP A
  63B6    540F        ANL A,#0F
  63B8    FB          MOV R3,A
  63B9    901003      MOV DPTR,#1003
  63BC    E0          MOVX A,@DPTR
  63BD    B40101      CJNE A,#01,63C1
  63C0    0B          INC R3
  63C1    902001      MOV DPTR,#2001
  63C4    BB0A02      CJNE R3,#0A,63C9
  63C7    7B00        MOV  R3,#00


  63C9    7CA0        MOV  R4,#A0
  63CB    EA          MOV  A,R2
  63CC    540F        ANL A,#0F
  63CE    4C          ORL A,R4
  63CF    F0          MOVX @DPTR,A
  63D0    121200      LCALL 1200
  63D3    121500      LCALL 1500
  63D6    EB          MOV  A,R3
  63D7    C4          SWAP A
  63D8    FB          MOV R3,A
  63D9    EA          MOV  A,R2
  63DA    540F        ANL A,#0F
  63DC    4B          ORL A,R3
  63DD    902001      MOV DPTR,#2001
  63E0    F0          MOVX @DPTR,A
  63E1    121200      LCALL 1200
  63E4    121500      LCALL 1500
  63E7    EB          MOV  A,R3
  63E8    C4          SWAP A
  63E9    FB          MOV R3,A
  63EA    026420      LJMP 6420
  63ED    902001      MOV DPTR,#2001
  63F0    E0          MOVX A,@DPTR
```

```
ADDRESS   OPCODE     MNEMONIC
  63F1    FA         MOV R2,A
  63F2    540F       ANL A,#0F
  63F4    FB         MOV R3,A
  63F5    901003     MOV DPTR,#1003
  63F8    E0         MOVX A,@DPTR
  63F9    B40101     CJNE A,#01,63FD
  63FC    0B         INC R3
  63FD    902001     MOV DPTR,#2001
  6400    BB0A02     CJNE R3,#0A,6405
  6403    7B00       MOV  R3,#00
  6405    7C0A       MOV  R4,#0A
  6407    EA         MOV  A,R2
  6408    54F0       ANL A,#F0
  640A    4C         ORL A,R4
  640B    F0         MOVX @DPTR,A
  640C    121200     LCALL 1200
  640F    121500     LCALL 1500
  6412    EA         MOV  A,R2
  6413    54F0       ANL A,#F0
  6415    4B         ORL A,R3
  6416    902001     MOV DPTR,#2001
  6419    F0         MOVX @DPTR,A


  6420    901004     MOV DPTR,#1004
  6423    E0         MOVX A,@DPTR
  6424    B4010C     CJNE A,#01,6433
  6427    904521     MOV DPTR,#4521
  642A    7400       MOV  A,#00
  642C    F0         MOVX @DPTR,A
  642D    904522     MOV DPTR,#4522
  6430    7401       MOV  A,#01
  6432    F0         MOVX @DPTR,A
  6433    026561     LJMP 6561
  6436    901002     MOV DPTR,#1002
  6439    E0         MOVX A,@DPTR
  643A    B40106     CJNE A,#01,6443
  643D    904523     MOV DPTR,#4523
  6440    E0         MOVX A,@DPTR
  6441    04         INC A
  6442    F0         MOVX @DPTR,A
  6443    904523     MOV DPTR,#4523
  6446    E0         MOVX A,@DPTR
  6447    B40103     CJNE A,#01,644D
  644A    02646B     LJMP 646B
  644D    B40203     CJNE A,#02,6453
  6450    0264A8     LJMP 64A8
```

ADDRESS	OPCODE	MNEMONIC
6453	B40303	CJNE A,#03,6459
6456	0264DE	LJMP 64DE
6459	B40403	CJNE A,#04,645F
645C	02651B	LJMP 651B
645F	B40506	CJNE A,#05,6468
6462	7400	MOV A,#00
6464	904523	MOV DPTR,#4523
6467	F0	MOVX @DPTR,A
6468	026436	LJMP 6436
646B	902003	MOV DPTR,#2003
646E	E0	MOVX A,@DPTR
646F	FA	MOV R2,A
6470	C4	SWAP A
6471	540F	ANL A,#0F
6473	FB	MOV R3,A
6474	901003	MOV DPTR,#1003
6477	E0	MOVX A,@DPTR
6478	B40101	CJNE A,#01,647C
647B	0B	INC R3
647C	902003	MOV DPTR,#2003
647F	BB0A02	CJNE R3,#0A,6484

SETTING OF
FINAL VALUE

6482	7B00	MOV R3,#00
6484	7CA0	MOV R4,#A0
6486	EA	MOV A,R2
6487	540F	ANL A,#0F
6489	4C	ORL A,R4
648A	F0	MOVX @DPTR,A
648B	121200	LCALL 1200
648E	121500	LCALL 1500
6491	EB	MOV A,R3
6492	C4	SWAP A
6493	FB	MOV R3,A
6494	EA	MOV A,R2
6495	540F	ANL A,#0F
6497	4B	ORL A,R3
6498	902003	MOV DPTR,#2003
649B	F0	MOVX @DPTR,A
649C	121200	LCALL 1200
649F	121500	LCALL 1500
64A2	EB	MOV A,R3
64A3	C4	SWAP A
64A4	FB	MOV R3,A
64A5	02654E	LJMP 654E
64A8	902003	MOV DPTR,#2003

```
ADDRESS    OPCODE      MNEMONIC
  64AB     E0          MOVX A,@DPTR
  64AC     FA          MOV R2,A
  64AD     540F        ANL A,#0F
  64AF     FB          MOV R3,A
  64B0     901003      MOV DPTR,#1003
  64B3     E0          MOVX A,@DPTR
  64B4     B40101      CJNE A,#01,64B8
  64B7     0B          INC R3
  64B8     902003      MOV DPTR,#2003
  64BB     BB0A02      CJNE R3,#0A,64C0
  64BE     7B00        MOV  R3,#00
  64C0     7C0A        MOV  R4,#0A
  64C2     EA          MOV  A,R2
  64C3     54F0        ANL A,#F0
  64C5     4C          ORL A,R4
  64C6     F0          MOVX @DPTR,A
  64C7     121200      LCALL 1200
  64CA     121500      LCALL 1500
  64CD     EA          MOV  A,R2
  64CE     54F0        ANL A,#F0
  64D0     4B          ORL A,R3
  64D1     902003      MOV DPTR,#2003
```

```
ADDRESS    OPCODE      MNEMONIC
  64D4     F0          MOVX @DPTR,A
  64D5     121200      LCALL 1200
  64D8     121500      LCALL 1500
  64DB     02654E      LJMP 654E
  64DE     902004      MOV DPTR,#2004
  64E1     E0          MOVX A,@DPTR
  64E2     FA          MOV R2,A
  64E3     C4          SWAP A
  64E4     540F        ANL A,#0F
  64E6     FB          MOV R3,A
  64E7     901003      MOV DPTR,#1003
  64EA     E0          MOVX A,@DPTR
  64EB     B40101      CJNE A,#01,64EF
  64EE     0B          INC R3
  64EF     902004      MOV DPTR,#2004
  64F2     BB0A02      CJNE R3,#0A,64F7
  64F5     7B00        MOV  R3,#00
  64F7     7CA0        MOV  R4,#A0
  64F9     EA          MOV  A,R2
  64FA     540F        ANL A,#0F
  64FC     4C          ORL A,R4
  64FD     F0          MOVX @DPTR,A
```

```
ADDRESS   OPCODE     MNEMONIC
  64FE    121200     LCALL 1200
  6501    121500     LCALL 1500
  6504    EB         MOV  A,R3
  6505    C4         SWAP A
  6506    FB         MOV R3,A
  6507    EA         MOV  A,R2
  6508    540F       ANL A,#0F
  650A    4B         ORL A,R3
  650B    902004     MOV DPTR,#2004
  650E    F0         MOVX @DPTR,A
  650F    121200     LCALL 1200
  6512    121500     LCALL 1500
  6515    EB         MOV  A,R3
  6516    C4         SWAP A
  6517    FB         MOV R3,A
  6518    02654E     LJMP 654E
  651B    902004     MOV DPTR,#2003
  651E    E0         MOVX A,@DPTR
  651F    FA         MOV R2,A
  6520    540F       ANL A,#0F
  6522    FB         MOV R3,A
  6523    901003     MOV DPTR,#1003


  6526    E0         MOVX A,@DPTR
  6527    B40101     CJNE A,#01,652B
  652A    0B         INC R3
  652B    902004     MOV DPTR,#2004
  652E    BB0A02     CJNE R3,#0A,6533
  6531    7B00       MOV  R3,#00
  6533    7C0A       MOV  R4,#0A
  6535    EA         MOV  A,R2
  6536    54F0       ANL A,#F0
  6538    4C         ORL A,R4
  6539    F0         MOVX @DPTR,A
  653A    121200     LCALL 1200
  653D    121500     LCALL 1500
  6540    EA         MOV  A,R2
  6541    54F0       ANL A,#F0
  6543    4B         ORL A,R3
  6544    902004     MOV DPTR,#2004
  6547    F0         MOVX @DPTR,A
  6548    121200     LCALL 1200
  654B    121500     LCALL 1500
  654E    901004     MOV DPTR,#1004
  6551    E0         MOVX A,@DPTR
  6552    B4010C     CJNE A,#01,6561
```

ADDRESS	OPCODE	MNEMONIC
6555	904521	MOV DPTR,#4521
6558	7400	MOV A,#00
655A	F0	MOVX @DPTR,A
655B	904523	MOV DPTR,#4523
655E	7401	MOV A,#01
6560	F0	MOVX @DPTR,A
6561	901005	MOV DPTR,#1005
6564	E0	MOVX A,@DPTR
6565	B40103	CJNE A,#01,656B
6568	026031	LJMP 6031
656B	026026	LJMP 6026

ADDRESS	OPCODE	MNEMONIC	
1500	75D010	MOV D0,#10	DELAY ROUTINE
1503	7902	MOV R1,#02	
1505	7AFF	MOV R2,#FF	
1507	7BFF	MOV R3,#FF	
1509	DBFE	DJNZ R3,1509	
150B	DAFA	DJNZ R2,1507	
150D	D9F6	DJNZ R1,1505	

ADDRESS	OPCODE	MNEMONIC
150F	75D000	MOV D0,#00
1512	22	RET

ADDRESS	OPCODE	MNEMONIC	
1900	75D010	MOV D0,#10	DELAY ROUTINE
1903	7905	MOV R1,#05	
1905	7AFF	MOV R2,#FF	
1907	7BFF	MOV R3,#FF	
1909	DBFE	DJNZ R3,1909	
190B	DAFA	DJNZ R2,1907	
190D	D9F6	DJNZ R1,1905	
190F	75D000	MOV D0,#00	
1912	22	RET	

ADDRESS	OPCODE	MNEMONIC
1200	75D010	MOV D0,#10
1203	7490	MOV A,#90
1205	90B821	MOV DPTR,#B821

ADDRESS	OPCODE	MNEMONIC
1208	F0	MOVX @DPTR,A
1209	902000	MOV DPTR,#2000
120C	7F02	MOV R7,#02
120E	E0	MOVX A,@DPTR
120F	FE	MOV R6,A
1210	C4	SWAP A
1211	540F	ANL A,#0F
1213	900200	MOV DPTR,#0200
1216	93	MOVC A,@A+DPTR
1217	90B820	MOV DPTR,#B820
121A	F0	MOVX @DPTR,A
121B	EE	MOV A,R6
121C	540F	ANL A,#0F
121E	900200	MOV DPTR,#0200
1221	93	MOVC A,@A+DPTR
1222	90B820	MOV DPTR,#B820
1225	F0	MOVX @DPTR,A
1226	902001	MOV DPTR,#2001
1229	DFE3	DJNZ R7,120E
122B	902003	MOV DPTR,#2003
122E	7F01	MOV R7,#01

DISPLAY ROUTINE FOR PRE-FINAL VALUE

ADDRESS	OPCODE	MNEMONIC
1230	E0	MOVX A,@DPTR
1231	FE	MOV R6,A
1232	C4	SWAP A
1233	540F	ANL A,#0F
1235	900200	MOV DPTR,#0200
1238	93	MOVC A,@A+DPTR
1239	90B820	MOV DPTR,#B820
123C	F0	MOVX @DPTR,A
123D	EE	MOV A,R6
123E	540F	ANL A,#0F
1240	900200	MOV DPTR,#0200
1243	93	MOVC A,@A+DPTR
1244	90B820	MOV DPTR,#B820
1247	F0	MOVX @DPTR,A
1248	00	NOP
1249	00	NOP
124A	00	NOP
124B	DFE3	DJNZ R7,1230
124D	75D000	MOV D0,#00
1250	22	RET

ADDRESS	OPCODE	MNEMONIC
1400	75D010	MOV D0,#10
1403	7490	MOV A,#90
1405	90B821	MOV DPTR,#B821
1408	F0	MOVX @DPTR,A
1409	902003	MOV DPTR,#2003
140C	7F02	MOV R7,#02
140E	E0	MOVX A,@DPTR
140F	FE	MOV R6,A
1410	C4	SWAP A
1411	540F	ANL A,#0F
1413	900200	MOV DPTR,#0200
1416	93	MOVC A,@A+DPTR
1417	90B820	MOV DPTR,#B820
141A	F0	MOVX @DPTR,A
141B	EE	MOV A,R6
141C	540F	ANL A,#0F
141E	900200	MOV DPTR,#0200
1421	93	MOVC A,@A+DPTR
1422	90B820	MOV DPTR,#B820
1425	F0	MOVX @DPTR,A
1426	902004	MOV DPTR,#2004
1429	DFE3	DJNZ R7,140E

DISPLAY ROUTINE FOR FINAL VALUE

ADDRESS	OPCODE	MNEMONIC
142B	902005	MOV DPTR,#2005
142E	7F01	MOV R7,#01
1430	E0	MOVX A,@DPTR
1431	FE	MOV R6,A
1432	C4	SWAP A
1433	540F	ANL A,#0F
1435	900200	MOV DPTR,#0200
1438	93	MOVC A,@A+DPTR
1439	90B820	MOV DPTR,#B820
143C	F0	MOVX @DPTR,A
143D	EE	MOV A,R6
143E	540F	ANL A,#0F
1440	900200	MOV DPTR,#0200
1443	93	MOVC A,@A+DPTR
1444	90B820	MOV DPTR,#B820
1447	F0	MOVX @DPTR,A
1448	00	NOP
1449	00	NOP
144A	00	NOP
144B	DFE3	DJNZ R7,1430
144D	75D000	MOV D0,#00
1450	22	RET

ADDRESS	OPCODE	MNEMONIC
1600	75D010	MOV D0,#10
1603	7490	MOV A,#90
1605	90B821	MOV DPTR,#B821
1608	F0	MOVX @DPTR,A
1609	90450B	MOV DPTR,#450B
160C	7F02	MOV R7,#02
160E	E0	MOVX A,@DPTR
160F	FE	MOV R6,A
1610	C4	SWAP A
1611	540F	ANL A,#0F
1613	900200	MOV DPTR,#0200
1616	93	MOVC A,@A+DPTR
1617	90B820	MOV DPTR,#B820
161A	F0	MOVX @DPTR,A
161B	EE	MOV A,R6
161C	540F	ANL A,#0F
161E	900200	MOV DPTR,#0200
1621	93	MOVC A,@A+DPTR
1622	90B820	MOV DPTR,#B820
1625	F0	MOVX @DPTR,A
1626	904509	MOV DPTR,#4509
1629	DFE3	DJNZ R7,160E

DISPLAY ROUTINE
FOR RUN
TIME

ADDRESS	OPCODE	MNEMONIC
162B	902007	MOV DPTR,#2007
162E	7F01	MOV R7,#01
1630	E0	MOVX A,@DPTR
1631	FE	MOV R6,A
1632	C4	SWAP A
1633	540F	ANL A,#0F
1635	900200	MOV DPTR,#0200
1638	93	MOVC A,@A+DPTR
1639	90B820	MOV DPTR,#B820
163C	F0	MOVX @DPTR,A
163D	EE	MOV A,R6
163E	540F	ANL A,#0F
1640	900200	MOV DPTR,#0200
1643	93	MOVC A,@A+DPTR
1644	90B820	MOV DPTR,#B820
1647	F0	MOVX @DPTR,A
1648	00	NOP
1649	00	NOP
164A	00	NOP
164B	DFE3	DJNZ R7,1630
164D	75D000	MOV D0,#00
1650	22	RET

ADDRESS	OPCODE	MNEMONIC
1700	75D010	MOV D0,#10
1703	7490	MOV A,#90
1705	90B821	MOV DPTR,#B821
1708	F0	MOVX @DPTR,A
1709	904514	MOV DPTR,#4514
170C	7F02	MOV R7,#02
170E	E0	MOVX A,@DPTR
170F	FE	MOV R6,A
1710	C4	SWAP A
1711	540F	ANL A,#0F
1713	900200	MOV DPTR,#0200
1716	93	MOVC A,@A+DPTR
1717	90B820	MOV DPTR,#B820
171A	F0	MOVX @DPTR,A
171B	EE	MOV A,R6
171C	540F	ANL A,#0F
171E	900200	MOV DPTR,#0200
1721	93	MOVC A,@A+DPTR
1722	90B820	MOV DPTR,#B820
1725	F0	MOVX @DPTR,A
1726	904511	MOV DPTR,#4511
1729	DFE3	DJNZ R7,170E

DISPLAY ROUTINE
FOR TOTAL
PACKAGES

ADDRESS	OPCODE	MNEMONIC
172B	902009	MOV DPTR,#2009
172E	7F01	MOV R7,#01
1730	E0	MOVX A,@DPTR
1731	FE	MOV R6,A
1732	C4	SWAP A
1733	540F	ANL A,#0F
1735	900300	MOV DPTR,#0300
1738	93	MOVC A,@A+DPTR
1739	90B820	MOV DPTR,#B820
173C	F0	MOVX @DPTR,A
173D	EE	MOV A,R6
173E	540F	ANL A,#0F
1740	900300	MOV DPTR,#0300
1743	93	MOVC A,@A+DPTR
1744	90B820	MOV DPTR,#B820
1747	F0	MOVX @DPTR,A
1748	00	NOP
1749	00	NOP
174A	00	NOP
174B	DFE3	DJNZ R7,1730
174D	75D000	MOV D0,#00
1750	22	RET

ADDRESS	OPCODE	MNEMONIC
1800	75D010	MOV D0,#10
1803	7490	MOV A,#90
1805	90B821	MOV DPTR,#B821
1808	F0	MOVX @DPTR,A
1809	903500	MOV DPTR,#3500
180C	7F02	MOV R7,#02
180E	E0	MOVX A,@DPTR
180F	FE	MOV R6,A
1810	C4	SWAP A
1811	540F	ANL A,#0F
1813	900200	MOV DPTR,#0200
1816	93	MOVC A,@A+DPTR
1817	90B820	MOV DPTR,#B820
181A	F0	MOVX @DPTR,A
181B	EE	MOV A,R6
181C	540F	ANL A,#0F
181E	900200	MOV DPTR,#0200
1821	93	MOVC A,@A+DPTR
1822	90B820	MOV DPTR,#B820
1825	F0	MOVX @DPTR,A
1826	903501	MOV DPTR,#3501
1829	DFE3	DJNZ R7,180E

DISPLAY ROUTINE
FOR CURRENT
QUANTITY

ADDRESS	OPCODE	MNEMONIC
182B	903502	MOV DPTR,#3502
182E	7F01	MOV R7,#01
1830	E0	MOVX A,@DPTR
1831	FE	MOV R6,A
1832	C4	SWAP A
1833	540F	ANL A,#0F
1835	900300	MOV DPTR,#0300
1838	93	MOVC A,@A+DPTR
1839	90B820	MOV DPTR,#B820
183C	F0	MOVX @DPTR,A
183D	EE	MOV A,R6
183E	540F	ANL A,#0F
1840	900300	MOV DPTR,#0300
1843	93	MOVC A,@A+DPTR
1844	90B820	MOV DPTR,#B820
1847	F0	MOVX @DPTR,A
1848	00	NOP
1849	00	NOP
184A	00	NOP
184B	DFE3	DJNZ R7,1830
184D	75D000	MOV D0,#00
1850	22	RET

ADDRESS	OPCODE	MNEMONIC	
25FD	75D018	MOV D0,#18	
2600	903200	MOV DPTR,#3200	
2603	E0	MOVX A,@DPTR	Comments
2604	F9	MOV R1,A	
2605	A3	INC DPTR	
2606	E0	MOVX A,@DPTR	Conversion
2607	FA	MOV R2,A	of
2608	7D00	MOV R5,#00	hexadecimal
260A	7B03	MOV R3,#03	to
260C	7CE8	MOV R4,#E8	decimal
260E	8A20	MOV 20,R2	value
2610	8921	MOV 21,R1	
2612	B90303	CJNE R1,#03,2618	
2615	022621	LJMP 2621	
2618	20D703	JB D7,261E	
261B	02262D	LJMP 262D	
261E	02264E	LJMP 264E	
2621	BAE803	CJNE R2,#E8,2627	
2624	02262D	LJMP 262D	
2627	20D7F4	JB D7,261E	
262A	02262D	LJMP 262D	
262D	BAE800	CJNE R2,#E8,2630	
2630	30D70C	JNB D7,263F	
2633	C2D7	CLR D7	
2635	74FF	MOV A,#FF	
2637	9C	SUBB A,R4	
2638	2A	ADD A,R2	
2639	04	INC A	
263A	FA	MOV R2,A	
263B	19	DEC R1	
263C	022642	LJMP 2642	
263F	EA	MOV A,R2	
2640	9C	SUBB A,R4	
2641	FA	MOV R2,A	
2642	C2D7	CLR D7	
2644	E9	MOV A,R1	
2645	9B	SUBB A,R3	
2646	F9	MOV R1,A	
2647	20D704	JB D7,264E	
264A	0D	INC R5	
264B	02260E	LJMP 260E	
264E	AA20	MOV R2,20	
2650	A921	MOV R1,21	
2652	7E64	MOV R6,#64	
2654	7F00	MOV R7,#00	

```
ADDRESS   OPCODE     MNEMONIC
  2656    8A20       MOV 20,R2
  2658    BA6400     CJNE R2,#64,265B
  265B    30D711     JNB D7,266F
  265E    C2D7       CLR D7
  2660    74FF       MOV  A,#FF
  2662    9E         SUBB A,R6
  2663    2A         ADD A,R2
  2664    04         INC A
  2665    FA         MOV R2,A
  2666    C2D7       CLR D7
  2668    E9         MOV  A,R1
  2669    9401       SUBB A,#01
  266B    F9         MOV R1,A
  266C    022672     LJMP 2672
  266F    EA         MOV  A,R2
  2670    9E         SUBB A,R6
  2671    FA         MOV R2,A
  2672    20D704     JB D7,2679
  2675    0F         INC R7
  2676    022656     LJMP 2656
  2679    AA20       MOV R2,20
  267B    7800       MOV  R0,#00


  267D    8A20       MOV 20,R2
  267F    C2D7       CLR D7
  2681    EA         MOV  A,R2
  2682    940A       SUBB A,#0A
  2684    FA         MOV R2,A
  2685    20D704     JB D7,268C
  2688    08         INC R0
  2689    02267D     LJMP 267D
  268C    AA20       MOV R2,20
  268E    EA         MOV  A,R2
  268F    E8         MOV  A,R0
  2690    C4         SWAP A
  2691    54F0       ANL A,#F0
  2693    4A         ORL A,R2
  2694    903501     MOV DPTR,#3501
  2697    F0         MOVX @DPTR,A
  2698    ED         MOV  A,R5
  2699    C4         SWAP A
  269A    54F0       ANL A,#F0
  269C    4F         ORL A,R7
  269D    903500     MOV DPTR,#3500
  26A0    F0         MOVX @DPTR,A
  26A1    75D000     MOV D0,#00


  26A4    22         RET
```

ADDRESS	OPCODE	CODE FOR
0200	F3	0
0201	60	1
0202	B5	2
0203	F4	3
0204	66	4
0205	D6	5
0206	D7	6
0207	70	7
0208	F7	8
0209	76	9
020A	00	BLANKING THE DISPLAY
020B	37	P
020C	D6	S
020D	17	F
020E	67	H
020F	05	r
0300	93	C
0301	87	t
0302	37	P
2002	BC	TO DISPLAY PS
2005	DC	TO DISPLAY FS
2007	EF	TO DISPLAY Hr
2009	12	TO DISPLAY tP
3502	01	TO DISPLAY Ct

CONCLUSION

MICROCOUNT apart from the basic operation of counting has provision for

* A fool proof arrangement, i.e. a lock to avoid tampering of the counter by the operator.
* Setting of desired parameter values (Production target level)
* Alarm signal informing the completion of counting to the operator
* Counting the total number of packages
* Indicating machine run time.

The MICROCOUNT is very flexible so that it can be employed to count variety of production output only with a change in the type of sensor.

The MICROCOUNT may be transformed more efficient as suggested below :

* A Centralised, CPU monitoring system for all the counters employed in a factory may be established to furnish the details regarding the shift, employee code number, production in a particular shift, monthly production and the employee's salary.

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2. National semiconductor - LS/S/TTL Logic data book.

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4. RAMESH.S.GAONKAR - "Microprocessor architecture, programming & applications" - Wiley Eastern Limited.1986

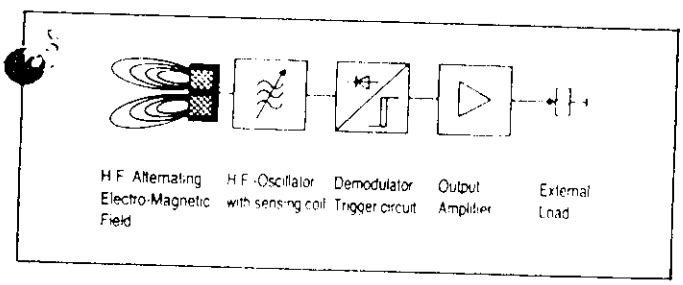
5. CONTROL SYSTEMS Transducer Catalogue.

6. Towers International Transistor Selection.

Technical Principles

Operating Principle

An H.F.-Oscillator generates an alternating electro-magnetic field which radiates through the "active surface" of the proximity switch. The oscillator output voltage is demodulated and fed via a trigger circuit to an amplified output stage. Introduction of an electrically or magnetically conductive material in the region of the "active surface" will caused the oscillator to become "damped". As a result of this damping the oscillator output voltage reduces and at a certain level causes the trigger circuit, and hence the output, to change state.



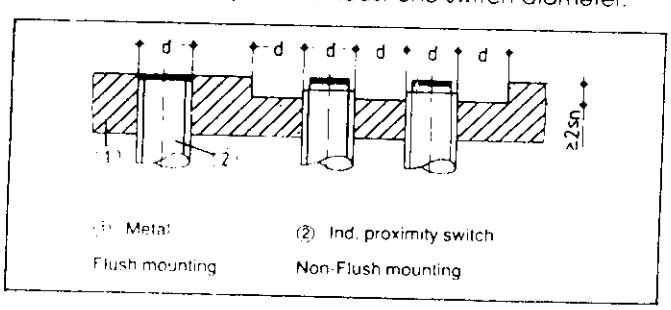
Mounting

Flush Mounting

The "active surface" may be flush with the metal in which the switch in mounted. Proximity switches of this type can be mounted next to one another without spacing.

Non-Flush Mounting

The "active surface" must have a free zone in which no metal is present. The distance between two adjacent proximity switches must be equal to at least one switch diameter.



Active Surface

Is the surface through which the high frequency electro-magnetic field radiates. The element that actuates the switch must come within the switching range of this surface.

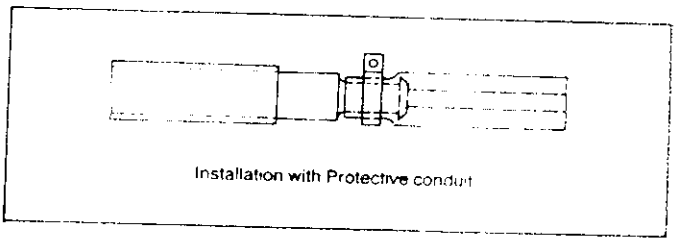
Torque Ratings

For proximity switches in threaded cylindrical housings it is recommended that the torque settings shown are not exceeded when tightening the fixing nuts. This ensures that no mechanical or electrical damage occurs.

Thread	Max. Torque
M 8 × 1	4 Nm
M 12 × 1	10 Nm
M 18 × 1	25 Nm
M 18 × 1	40 Nm

Installations with Protective Conduit

For use in demanding conditions such as Machine Shops etc., it is advisable to install proximity switches with protective conduit over the connection cables. The cable exit sleeves on Visolux proximity switches are designed to allow fixing of protective conduity by clamping in the middle for the sleeve.



Actuation

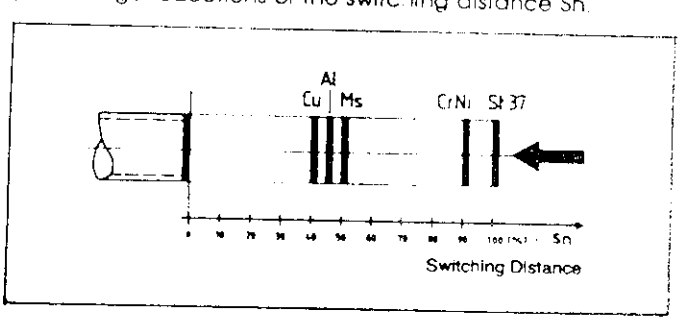
Actuating Elements

Inductive Proximity switches can be actuated by almost any component made of metal.

In the Product Specifications the Normal Switching Distance Sn is shown for operation with a square actuating element manufactured in 1 mm thick ST 37 steel. The sides of this actuator are equal in length to the diameter of the switch in question. Smaller sizes of actuator or use o other metals will cause a reduction in switching distance. Use of thin foils can however increase the switching distance.

Reduction Factors

Deviations from ST 37 as the actuator material ar shown below percentage reductions of the switching distance Sn.



Nominal Switching Distance Sn

is the stated value for a proximity switch operating under tightly controlled conditions. Deviations caused by fluctuations in temperature or supply voltage are not considered.

Real Switching Distance Sr

is the stated value for an individual proximity switch operating at 20°C with nominal supply voltage. This value must be within the range of 90% to 110% of Sn.

Useable Switching Distance Su

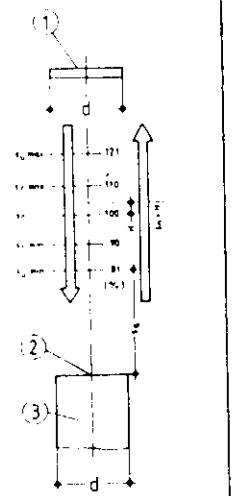
is the stated value for a proximity switch operating within the temp range — 25°C to + 70°C and also with 80% to 115% of supply voltage. This value must be within the range of 81% to 121% of Sn.

Operating Distance Sa

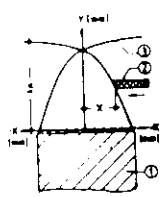
is the stated value for a proximity switch operating anywhere within its specified voltage and temperature limits and at which value functioning of the switch is guaranteed. This value will be within the range 0% to 81% of Sn.

Actuator Approach

Inductie proximity switches exhibit a variation in switching characteristic according to whether the actuator element approaches the active surface ina perpendicular or horizontal direction. A smaller switching distance is necessary for switches operated by actuators with horizontal approach paths.



① Actuator Element
② Active Surface
③ Proximity Switch



① Inductive Proximity Switch
② Actuator Element
③ Switching Curve

Hysteresis

The threshold levels of the trigger circuit in the proximity switch provide a difference between switch on point and switch off point. This difference is known as Hysteresis S and helps provide a definite switching action without hunting.

Electrical Values

Supply Voltage

The supply voltages stated for CONTROL SYSTEMS proximity switches are selected to match the needs of todays market. The values given in the Product Specifications are the limits which will ensure reliable operation at all times A.C. Ripple above and below these values is permitted with the stated limits.

Ripple

The supply voltage may have a superimposed peak to peak ripple voltage on it. The value is given as a percentage of supply voltage.

No load current

is the current of the proximity switch without an external load connected.

Maximum Output current

is the maximum permissible load current through the output of the proximity switch. This value is valid for the complete range of supply voltage.

Voltage Drop

is the maximum voltage drop with maximum current flowing through the output.

Leakage current

is the residual current that flows through the load with the output switched off.

Switching frequency

is the maximum number of successive switching operation caused by a cyclical charge between damped and undamped states. This value defines the maximum rat between successive actuation signals.

Temperature Drift

is the maximum deviation from the Real Switching Distance within the permissible temperature range -25°C to +4 70°C This value will not exceed ± 10% of Sr.

Switching functions

Normally open (N.O.)

When the actuator element is within the Operating Distanc Sa. (active surface damped) the output of the proxim switch is on.

Normally closed (N.C.)

When the actuator element is within the Operating Distan Sa (active surface damped) the output of the proxim switch is off.

FOR DC OPERATION

Complementary Function (Antivalent)

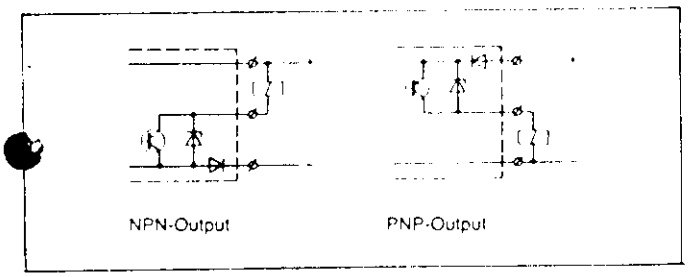
The proximity switch has two outputs, one with normally open function and the other with normally closed function.

NPN Output/Negative Switching

The load is connected between output and positive lines. It is energised when the output is switched to negative.

PNP Output/Positive Switching

The load is connected between output and negative lines. It is energised when the output is switched to positive.



Connection Identification to Cenelec Standard EN 50044

Indian Standard

3 wire Proximity Switches

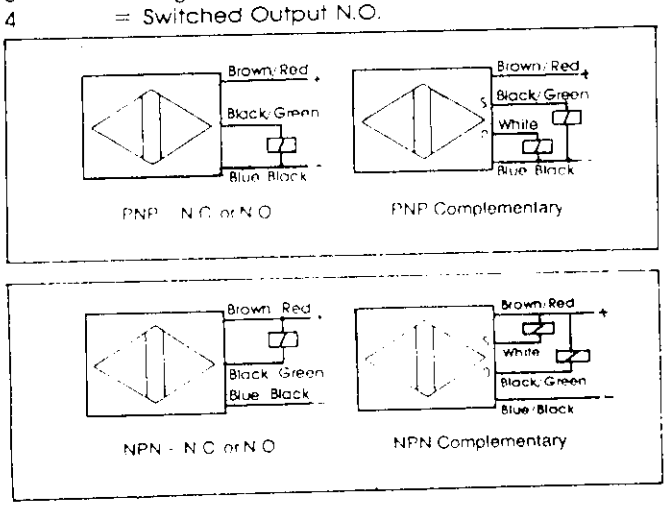
Brown	Positive Line	Red
Blue	Negative Line	Black
Black	Switched Output	Green

4 wire Proximity Switches

Brown	Positive Line	Red
Blue	Negative Line	Black
Black	= Switched Output N.O.	Green
Black	= Switched Output N.C.	Yellow

Proximity Switches with Terminals

1 = Positive Line
2 = Switched Output N.C.
3 = Negative Line
4 = Switched Output N.O.



Switching Combinations

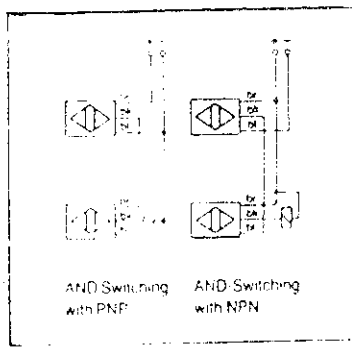
By connecting proximity switches as shown in the connection diagrams below it is possible to select a variety of switching posibilities without the need for additional contactors or relays.

AND Connection

Please note:

Each proximity switch has a maximum voltage drop of 2.5 V and therefore the switching voltage requirement of the load (Relay, Contactor etc.) must be borne in mind.

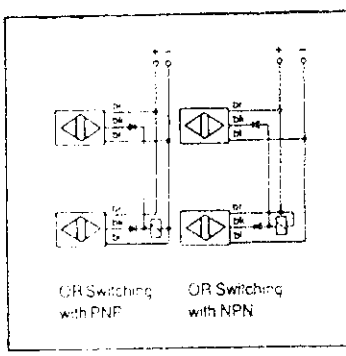
For each proximity switch connected the maximum output current available to drive the load must be reduced by 20 mA.



OR Connection

Please note:

Use of blocking diodes to isolate outputs means that when wiring proximity switches with integral indicator LED's not all LED's will illuminate when one switch is switched on.



Protective Measures

Switching Inductive Loads

CONTROL SYSTEMS proximity switches contain an interna suppression circuit to limit the effects of switching inductiv loads. Additional suppression is not necessary.

Switch On Pulse Suppression

At the instant the supply voltage is applied to CONTRO SYSTEMS proximity switch a special suppression circuit acts t prevent the output from producing unwanted pulses. This als means that the output is inactive for a momentary period a switch on.

Short Circuit Protection

All CONTROL SYSTEMS proximity switches with the letter K o the end of the order number have internal short circu protection. This protection functions for the duration of th short circuit and prevents damage to the switch. Upo removal of the short circuit the CONTROL SYSTEMS proximi switch is automatically reset into normal operation.

Switching of capacitive loads, filament lamps etc is possib without additional protective measures.

Reverse Polarity Protection

CONTROL SYSTEMS proximity switches are protected agair incorrect polarity connection as standard.

National Semiconductor

54LS09/DM54LS09/DM74LS09
Quad 2-Input AND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic AND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Features

- Alternate Military/Aerospace device (54LS09) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

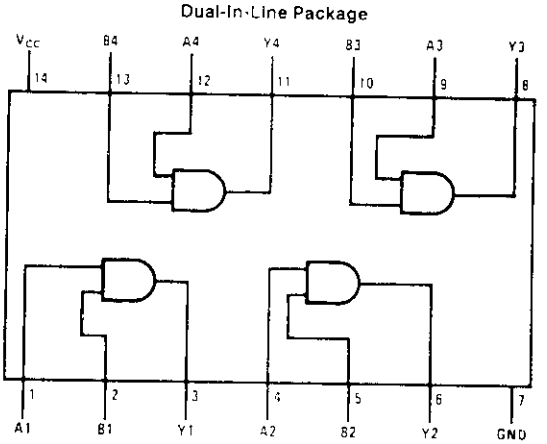
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/5348–1

Order Number 54LS09DMQB, 54LS09FMQB, DM54LS09J, DM54LS09W, DM74LS09M or DM74LS09N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = AB$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS09			DM74LS09			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V, V_{IH} = Min				100	µA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			2.4	4.8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			4.4	8.8	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	5	20	8	45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	4	15	6	27	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

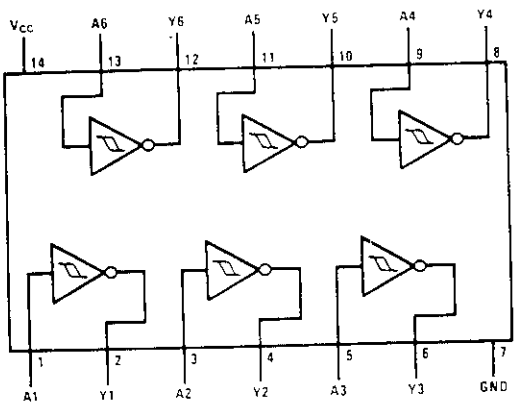
54LS14/DM74LS14 Hex Inverters with Schmitt Trigger Inputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

Connection Diagram

Dual-In-Line Package



TL/F/6353-1

Order Number 54LS14DMQB, 54LS14FMQB, 54LS14LMQB, DM74LS14M or DM74LS14N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS14			DM74LS14			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 1)	1.5	1.6	2.0	1.4	1.6	1.9	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 1)	0.6	0.8	1.1	0.5	0.8	1	V
V_{HYS}	Input Hysteresis (Note 1)	0.4	0.8		0.4	0.8		V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS		0.25	0.4	V
			DM74		0.35	0.5	
		V_{CC} = Min, I_{OL} = 4 mA	DM74		0.25	0.4	
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, V_I = V_T	DM74		−0.14		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, V_I = V_T	DM74		−0.18		mA
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	DM74			0.1	mA
		V_{CC} = Max, V_I = 10.0V	54LS				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			8.6	16	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			12	21	mA

Note 1: V_{CC} = 5V.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

54LS138/DM54LS138/DM74LS138, 54LS139/DM54LS139/DM74LS139 Decoders/Demultiplexers

General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The LS138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The LS139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

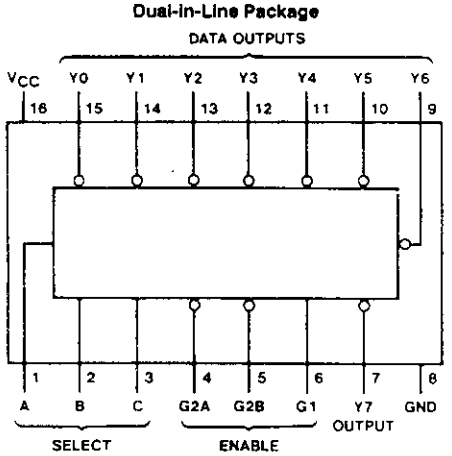
All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

Features

- Designed specifically for high speed:
  - Memory decoders
  - Data transmission systems
- LS138 3-to-8-line decoders incorporates 3 enable inputs to simplify cascading and/or data reception
- LS139 contains two fully independent 2-to-4-line decoders/demultiplexers
- Schottky clamped for high performance
- Typical propagation delay (3 levels of logic)
  - LS138 21 ns
  - LS139 21 ns
- Typical power dissipation
  - LS138 32 mW
  - LS139 34 mW
- Alternate Military/Aerospace devices (54LS138, 54LS139) are available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagrams

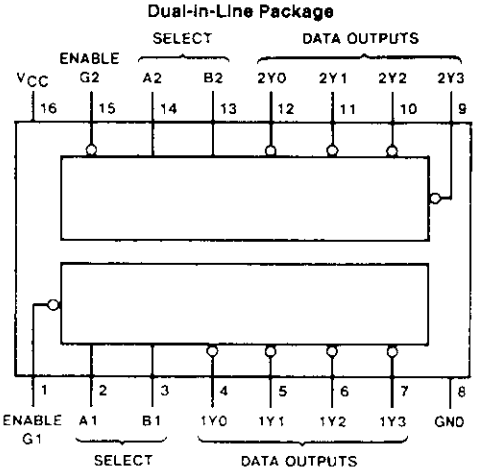
Dual-In-Line Package



TL/F/6391–1

Order Number 54LS138DMQB, 54LS138FMQB, 54LS138LMQB, DM54LS138J, DM54LS138W, DM74LS138M or DM74LS138N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Dual-In-Line Package



TL/F/6391–2

Order Number 54LS139DMQB, 54LS139FMQB, 54LS139LMQB, DM54LS139J, DM54LS139W, DM74LS139M or DM74LS139N
See NS Package Number E20A, J16A, M16A, N16E or W16A

te Maximum Ratings (Note)

Aerospace specified devices are required, ntact the National Semiconductor Sales tributors for availability and specifications.

age	7V
je	7V
ree Air Temperature Range	
and 54LS	−55°C to + 125°C
	0°C to + 70°C
mperature Range	−65°C to + 150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

mended Operating Conditions

Parameter	DM54LS138			DM74LS138			Units
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
High Level Input Voltage	2			2			V
Low Level Input Voltage			0.7			0.8	V
High Level Output Current			−0.4			−0.4	mA
Low Level Output Current			4			8	mA
Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

mended operating free air temperature range (unless otherwise noted)

Parameter	Conditions		Min	Typ (Note 1)	Max	Units
Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
		DM74	2.7	3.4		
Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
		DM74		0.35	0.5	
	I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
		DM74	−20		−100	
Supply Current	V_{CC} = Max (Note 3)			6.3	10	mA

ypicals are at V_{CC} = 5V, T_A = 25°C

more than one output should be shorted at a time, and the duration should not exceed one second.

s measured with all outputs enabled and open

National Semiconductor

54LS155/DM54LS155/DM74LS155, 54LS156/DM54LS156/DM74LS156 Dual 2-Line to 4-Line Decoders/Demultiplexers

General Description

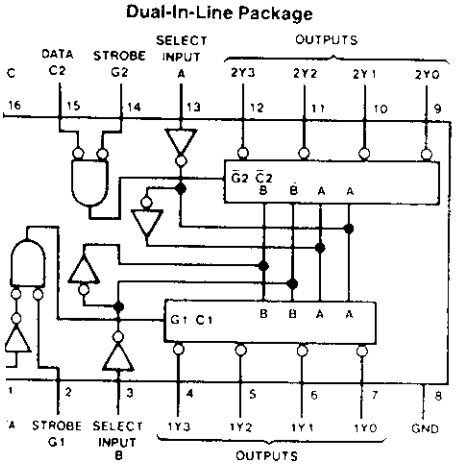
These TTL circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied at C2 is true through its outputs. The inverter following the C1 data input permits use as a 3-to-8-line decoder, or 1-to-8-line demultiplexer, without external gating. Input clamping diodes are provided on these circuits to minimize transmission-line effects and simplify system design.

Features

- Applications:
  Dual 2-to-4-line decoder
  Dual 1-to-4-line demultiplexer
  3-to-8-line decoder
  1-to-8-line demultiplexer
- Individual strobes simplify cascading for decoding or demultiplexing larger words
- Input clamping diodes simplify system design
- Choice of outputs:
  Totem-pole (LS155)
  Open-collector (LS156)
- Alternate Military/Aerospace device (54LS155/156) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram and Function Tables

Dual-In-Line Package



TL/F/6395–1

Order Number 54LS155DMQB, 54LS155FMQB, 54LS155LMQB, DM54LS155J, DM54LS155W, DM74LS155M, DM74LS155N, 54LS156DMQB, 54LS156FMQB, DM54LS156J, DM54LS156W, DM74LS156M or DM74LS156N
See NS Package Number E20A, J16A, M16A, N16E or W16A

2-Line-to-4-Line Decoder or 1-Line-to-4-Line Demultiplexer

Inputs				Outputs			
Select		Strobe	Data				
B	A	G1	C1	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Inputs				Outputs			
Select		Strobe	Data				
B	A	G2	C2	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-Line-to-8-Line Decoder or 1-Line-to-8-Line Demultiplexer

Inputs			Outputs							
		Strobe Or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
	X	H	H	H	H	H	H	H	H	H
	L	L	L	H	H	H	H	H	H	H
	H	L	H	L	H	H	H	H	H	H
	L	L	H	H	L	H	H	H	H	H
	L	L	H	H	H	L	H	H	H	H
	H	L	H	H	H	H	L	H	H	H
	L	L	H	H	H	H	H	L	H	H
	H	L	H	H	H	H	H	H	L	H

*C = Inputs C1 and C2 connected together
‡G = Inputs G1 and G2 connected together
H = High level, L = Low level, X = Don't care

S155 Switching Characteristics

V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

mbol	Parameter	From (input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
H	Propagation Delay Time Low to High Level Output	A, B, C2, G1 or G2 to Y		16		22	ns
L	Propagation Delay Time High to Low Level Output	A, B, C2, G1 or G2 to Y		27		35	ns
H	Propagation Delay Time Low to High Level Output	A or B to Y		18		24	ns
L	Propagation Delay Time High to Low Level Output	A or B to Y		27		35	ns
H	Propagation Delay Time Low to High Level Output	C1 to Y		20		24	ns
L	Propagation Delay Time High to Low Level Output	C1 to Y		27		35	ns

ommended Operating Conditions

ol	Parameter	DM54LS156			DM74LS156			Units
		Min	Nom	Max	Min	Nom	Max	
	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
	High Level Input Voltage	2			2			V
	Low Level Input Voltage			0.7			0.8	V
	High Level Output Voltage			5.5			5.5	V
	Low Level Output Current			4			8	mA
	Free Air Operating Temperature	−55		125	0		70	°C

156 Electrical Characteristics

ecommended operating free air temperature range (unless otherwise noted)

ol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
	High Level Output Current	V_{CC} = Min, V_O = 5.5V; V_{IL} = Max, V_{IH} = Min				100	µA
	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max; V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
	Input Current at Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
	Supply Current	V_{CC} = Max (Note 2)			6.1	10	mA

All typicals are at V_{CC} = 5V, T_A = 25°C

I_{CC} is measured with all outputs open, A, B, and C1 inputs at 4.5V, and C2, G1, and G2 grounded.

National Semiconductor

54LS161A/DM54LS161A/DM74LS161A, 54LS163A/DM54LS163A/DM74LS163A Synchronous 4-Bit Binary Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The LS16*A and LS163A are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable input. Low-to-high transitions at the load input are perfectly acceptable, regardless of the logic levels on the clock or enable inputs. The clear function for the LS161A is asynchronous; and a low level at the clear input sets all four of the flip-flop outputs low, regardless of the levels of clock, load, or enable inputs. The clear function for the LS163A is synchronous; and a low level at the clear inputs sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output.

Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low level transitions at the enable P or T inputs may occur, regardless of the logic level of the clock.

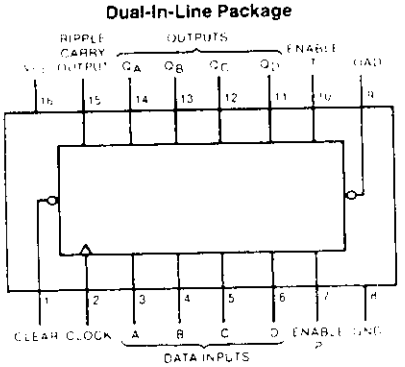
These counters feature a fully independent clock circuit. Changes made to control inputs (enable P or T or load) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable set-up and hold times.

Features

- Synchronously programmable
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs
- Typical propagation time, clock to Q output 14 ns
- Typical clock frequency 32 MHz
- Typical power dissipation 93 mW
- Alternate Military/Aerospace device (54LS16* 54LS163) is available. Contact a National Semiconductor Sales Office/Distributor for specificaitons.

Connection Diagram

Dual-In-Line Package



TL/F/6397–1

Order Numbers 54LS161ADMQB, 54LS161AFMQB, 54LS161ALMQB, 54LS163ADMQB, 54LS163AFMQB, 54LS163ALMQB, DM54LS161AJ, DM54LS161AW, DM54LS163AJ, DM54LS163AW, DM74LS161AM, DM74LS161AN, DM74LS163AM or DM74LS163AN
See NS Package Number E20A, J16A, M16A, N16E or W16A

ɔlute Maximum Ratings (Note)

'ıary/Aerospace specified devices are required, ı contact the National Semiconductor Sales ıDistributors for availability and specifications.

:oltage	7V
ɔtage	7V
'g Free Air Temperature Range	
-LS and 54LS	−55°C to +125°C
:LS	0°C to +70°C
ıTemperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

ɔmmended Operating Conditions

Parameter		DM54LS161A			DM74LS161A			Units
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
High Level Input Voltage		2			2			V
Low Level Input Voltage				0.7			0.8	V
High Level Output Current				0.4			0.4	mA
Low Level Output Current				4			8	mA
Clock Frequency (Note 1)		0		25	0		25	MHz
Clock Frequency (Note 2)		0		20	0		20	MHz
Pulse Width (Note 1)	Clock	20	6		20	6		ns
	Clear	20	9		20	9		
Pulse Width (Note 2)	Clock	25			25			ns
	Clear	25			25			
Setup Time (Note 1)	Data	20	8		20	8		ns
	Enable P	25	17		25	17		
	Load	25	15		25	15		
Setup Time (Note 2)	Data	20			20			ns
	Enable P	30			30			
	Load	30			30			
Hold Time (Note 1)	Data	0	−3		0	−3		ns
	Others	0	−3		0	−3		
Hold Time (Note 2)	Data	5			5			ns
	Others	5			5			
Clear Release Time (Note 1)		20			20			ns
Clear Release Time (Note 2)		25			25			ns
Free Air Operating Temperature		55		125	0		70	°C

15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5.5V

50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5.5V

National Semiconductor

54LS244/DM74LS244 Octal TRI-STATE® Buffers/Line Drivers/Line Receivers

General Description

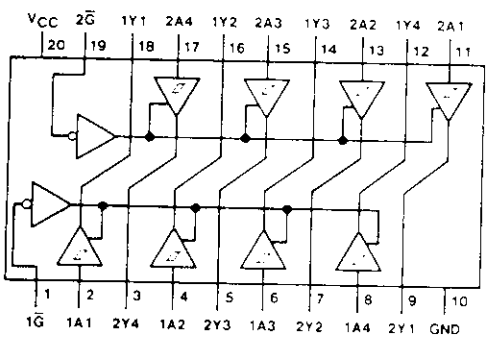
These buffers/line drivers are designed to improve both the performance and PC board density of TRI-STATE buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs and can be used to drive terminated lines down to 133Ω.

Features

- TRI-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at data inputs improves noise margins
- Typical I_{OL} (sink current)
  - 54LS 12 mA
  - 74LS 24 mA
- Typical I_{OH} (source current)
  - 54LS 12 mA
  - 74LS 15 mA
- Typical propagation delay times
  - Inverting 10.5 ns
  - Noninverting 12 ns
- Typical enable/disable time 18 ns
- Typical power dissipation (enabled)
  - Inverting 130 mW
  - Noninverting 135 mW

Connection Diagram

Dual-In-Line Package



TL/F/8442–1

Order Number 54LS244DMQB, 54LS244FMQB, 54LS244LMQB, DM74LS244WM or DM74LS244N
See NS Package Number E20A, J20A, M20B, N20A or W20A

Function Table

Inputs		Output
G	A	Y
L	L	L
L	H	H
H	X	Z

L Low Logic Level
H High Logic Level
X Either Low or High Logic Level
Z High Impedance

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	54LS244			DM74LS244			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions			Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$) Data Inputs Only	V_{CC} = Min			0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = −1 mA		DM74	2.7			V
		V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = −3 mA		54LS/DM74	2.4	3.4		V
		V_{CC} = Min, V_{IH} = Min, V_{IL} = 0.5V, I_{OH} = Max		54LS/DM74	2			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OL} = 12 mA	54LS/DM74			0.4	V
			I_{OL} = Max	DM74			0.5	V
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max, V_{IL} = Max, V_{IH} = Min	V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied		V_O = 0.4V				−20	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 7V (DM74) V_I = 10V (54LS)				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.4V		−0.5		−200	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		54LS	−50		−225	mA
				DM74	−40			
I_{CC}	Supply Current	V_{CC} = Max, Outputs Open	Outputs High			13	23	mA
			Outputs Low			27	46	
			Outputs Disabled			32	54	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

LS245/DM54LS245/DM74LS245
RI-STATE® Octal Bus Transceiver

neral Description

e octal bus transceivers are designed for asynchro- two-way communication between data buses. The ol function implementation minimizes external timing rements.

Device allows data transmission from the A bus to the B r from the B bus to the A bus depending upon the logic at the direction control (DIR) input. The enable input an be used to disable the device so that the buses are ively isolated.

tures

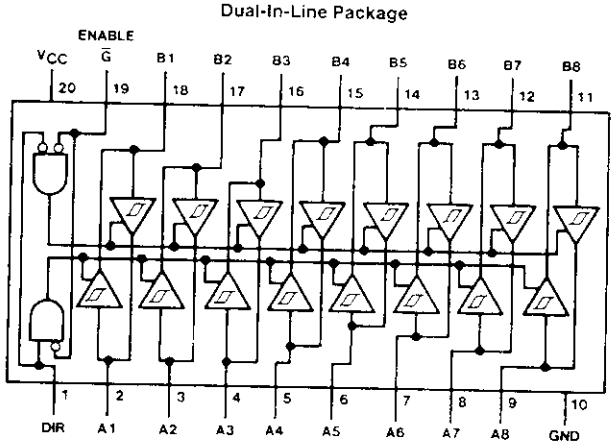
Directional bus transceiver in a high-density 20-pin kage

-STATE outputs drive bus lines directly

- PNP inputs reduce DC loading on bus lines
- Hysteresis at bus inputs improve noise margins
- Typical propagation delay times, port-to-port 8 ns
- Typical enable/disable times 17 ns
- I_{OL} (sink current)
  - 54LS 12 mA
  - 74LS 24 mA
- I_{OH} (source current)
  - 54LS 12 mA
  - 74LS 15 mA
- Alternate Military/Aerospace device (54LS245) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

nnection Diagram

Dual-In-Line Package



TL/F/6418-1

Order Number 54LS245DMQB, 54LS245FMQB, 54LS245LMQB, DM54LS245J, DM54LS245W, DM74LS245WM or DM74LS245N
See NS Package Number E20A, J20A, M20B, N20A or W20A

unction Table

Enable $\overline{G}$	Direction Control DIR	Operation
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = High Level, L = Low Level, X = Immaterial

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	
DIR or $\overline{G}$	7V
A or B	5.5V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS245			DM74LS245			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions			Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
HYS	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = Min			0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = −1 mA		DM74	2.7			V
		V_{CC} = Min, V_{IL} = Min, V_{IL} = Max, I_{OH} = −3 mA		DM54/DM74	2.4	3.4		V
		V_{CC} = Min, V_{IH} = Min, V_{IL} = 0.5V, I_{OH} = Max		DM54/DM74	2			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OL} = 12 mA	DM74			0.4	V
			I_{OL} = Max	DM54			0.4	V
				DM74			0.5	V
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max, V_{IL} = Max, V_{IH} = Min	V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied		V_O = 0.4V				−200	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	A or B	V_I = 5.5V			0.1	mA
			DIR or $\overline{G}$	V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V					20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V					−0.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)			−40		−225	mA
I_{CC}	Supply Current	Outputs High		V_{CC} = Max		48	70	mA
		Outputs Low				62	90	mA
		Outputs at Hi-Z				64	95	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, not to exceed one second duration.

National Semiconductor

DM54LS373/DM74LS373, 54LS374/DM54LS374/DM74LS374 TRI-STATE® Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. (Continued)

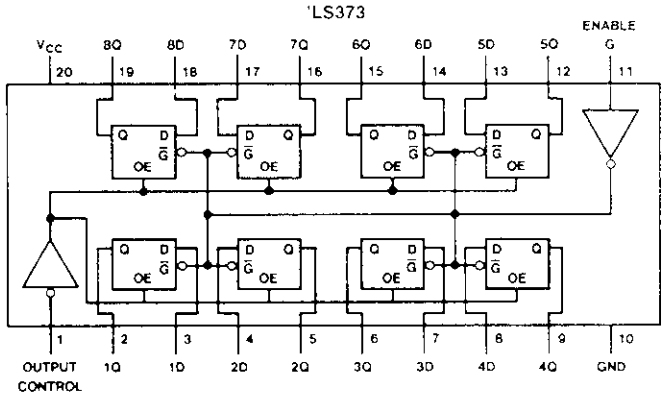
Features

- Choice of 8 latches or 8 D-type flip-flops in a single package
- TRI-STATE bus-driving outputs
- Full parallel-access for loading
- Buffered control inputs
- P-N-P inputs reduce D-C loading on data lines
- Alternate military/aerospace device (54LS374) is available. Contact a National Semiconductor sales office/distributor for specifications.

Connection Diagrams

Dual-In-Line Packages

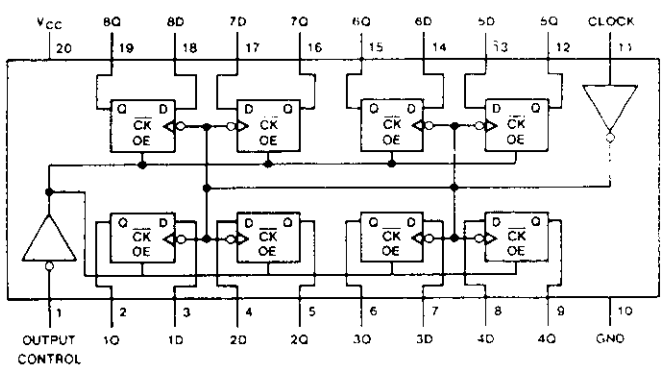
'LS373



TL/F/6431–1

Order Number DM54LS373J, DM54LS373W, DM74LS373N or DM74LS373WM
See NS Package Number J20A, M20B, N20A or W20A

'LS374



TL/F/6431–2

Order Number 54LS374DMQB, 54LS374FMQB, 54LS374LMQB, DM54LS374J, DM54LS374W, DM74LS374WM or DM74LS374N
See NS Package Number E20A, J20A, M20B, N20A or W20A

General Description (Continued)

The eight latches of the DM54/74LS373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

The eight flip-flops of the DM54/74LS374 are edge-triggered D-type flip flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Function Tables

DM54/74LS373

Output Control	Enable G	D	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

DM54/74LS374

Output Control	Clock	D	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = High Level (Steady State), L = Low Level (Steady State), X = Don't Care

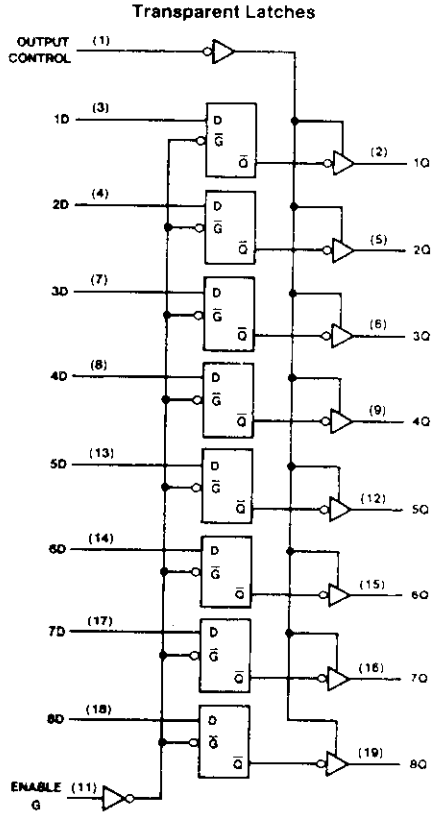
↑ = Transition from low-to-high level, Z = High Impedance State

Q_0 = The level of the output before steady-state input conditions were established

Logic Diagrams

DM54/74LS373

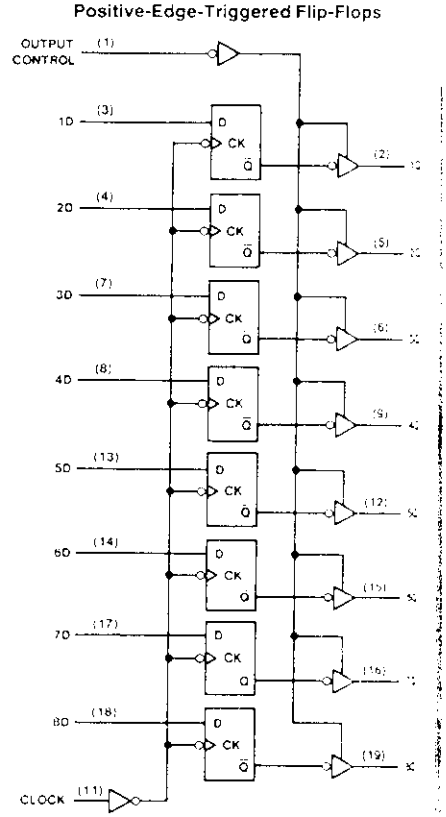
Transparent Latches



TL/F/6431-3

DM54/74LS374

Positive-Edge-Triggered Flip-Flops



Absolute Maximum Ratings (See Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS373			DM74LS373			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Votage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
t_w	Pulse Width (Note 2)	Enable High	15			15			ns
		Enable Low	15			15			
t_{su}	Data Setup Time (Notes 1 & 2)		5 ↓			5 ↓			ns
t_h	Data Hold Time (Notes 1 & 2)		20 ↓			20 ↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.

Note 2: T_A = 25°C and V_{CC} = 5V

'LS373 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V, V_{IH} = Min, V_{IL} = Max				20	µA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V, V_{IH} = Min, V_{IL} = Max				−20	µA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−50		−225	mA
			DM74	−50		−225	
I_{CC}	Supply Current	V_{CC} = Max			24	40	mA

MOTOROLA

MC14001UB
Quad 2-Input NOR Gate

MC14002UB
Dual 4-Input NOR Gate

MC14011UB
Quad 2-Input NAND Gate

MC14012UB
Dual 4-Input NAND Gate

MC14023UB
Triple 3-Input NAND Gate

MC14025UB
Triple 3-Input NOR Gate

CMOS SSI
(LOW-POWER COMPLEMENTARY MOS)

UB-SERIES GATES

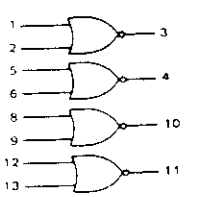
UB-SUFFIX SERIES CMOS GATES

The UB Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired. The UB set of CMOS gates are inverting non-buffered functions.

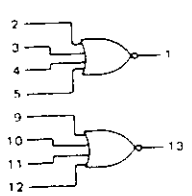
- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linear and Oscillator Applications
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two RTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for Corresponding CD4000 Series UB Suffix Devices
- Formerly Listed without UB Suffix

LOGIC DIAGRAMS

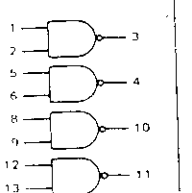
MC14001UB
Quad 2-Input NOR Gate



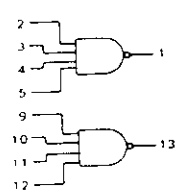
MC14002UB
Dual 4-Input NOR Gate



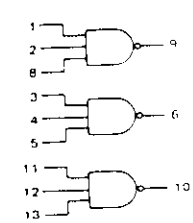
MC14011UB
Quad 2-Input NAND Gate



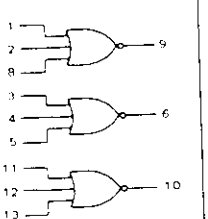
MC14012UB
Dual 4-Input NAND Gate



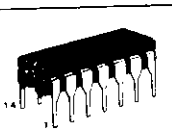
MC14023UB
Triple 3-Input NAND Gate



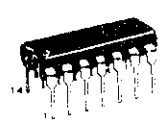
MC14025UB
Triple 3-Input NOR Gate



V_{DD} = Pin 14
V_{SS} = Pin 7
for All Devices



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXUB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125, -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0		0.05		0	0.05		0.05	Vdc
		10		0.05		0	0.05		0.05	
		15		0.05		0	0.05		0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95		4.95	5.0		4.95		Vdc
		10	9.95		9.95	10		9.95		
		15	14.95		14.95	15		14.95		
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 Vdc)		5.0		1.0		2.25	1.0		1.0	
(V_O = 9.0 Vdc)		10		2.0		4.50	2.0		2.0	
(V_O = 13.5 Vdc)		15		2.5		6.75	2.5		2.5	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 Vdc)		5.0	4.0		4.0	2.75		4.0		
(V_O = 1.0 Vdc)		10	8.0		8.0	5.50		8.0		
(V_O = 1.5 Vdc)		15	12.5		12.5	8.25		12.5		
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2		-1.0	-1.7		-0.7		
(V_{OH} = 4.6 Vdc)		5.0	-0.25		-0.2	-0.36		-0.14		
(V_{OH} = 9.5 Vdc)		10	-0.62		-0.5	-0.9		-0.35		
(V_{OH} = 13.5 Vdc)		15	-1.8		-1.5	-3.5		-1.1		
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64		0.51	0.88		0.36		mAdc
(V_{OL} = 0.5 Vdc)		10	1.6		1.3	2.25		0.9		
(V_{OL} = 1.5 Vdc)		15	4.2		3.4	8.8		2.4		
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0		-0.8	-1.7		-0.6		
(V_{OH} = 4.6 Vdc)		5.0	-0.2		-0.16	-0.36		-0.12		
(V_{OH} = 9.5 Vdc)		10	-0.5		-0.4	-0.9		-0.3		
(V_{OH} = 13.5 Vdc)		15	-1.4		-1.2	-3.5		-1.0		
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52		0.44	0.88		0.36		mAdc
(V_{OL} = 0.5 Vdc)		10	1.3		1.1	2.25		0.9		
(V_{OL} = 1.5 Vdc)		15	3.6		3.0	8.8		2.4		
Input Current (AL Device)	I_{in}	15		±0.1		±0.00001	±0.1		±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15		±0.3		±0.00001	±0.3		±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}					5.0	7.5			pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0		0.25		0.0005	0.25		7.5	μAdc
		10		0.50		0.0010	0.50		15.0	
		15		1.00		0.0015	1.00		30.0	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0		1.0		0.0005	1.0		7.5	μAdc
		10		2.0		0.0010	2.0		15.0	
		15		4.0		0.0015	4.0		30.0	
Total Supply Current**† (Dynamic plus Quiescent, Per Gate, C_L = 50 pF)	I_T	5.0	I_T = (0.3 μA/kHz) f + I_{DD}/N							μAdc
		10	I_T = (0.6 μA/kHz) f + I_{DD}/N							
		15	I_T = (0.8 μA/kHz) f + I_{DD}/N							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise Immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
0.6 Vdc min @ V_{DD} = 5.0 Vdc
1.0 Vdc min @ V_{DD} = 10 Vdc
1.0 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF

$$I_T(C_L) = I_T(50\ pF) + N \times 10^{-3}(C_L - 50)V_{DD}f$$

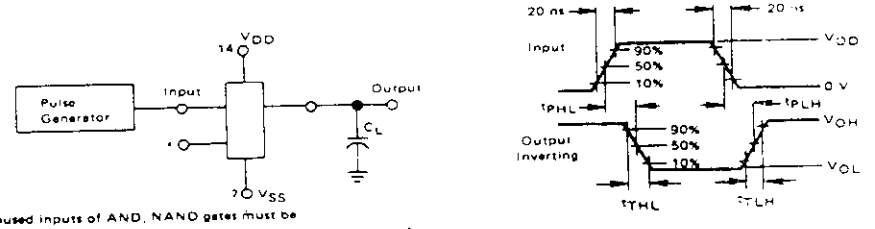
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, f in kHz is input frequency and N is number of gates per package.

**The formulas given are for the typical characteristics only at 25°C

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

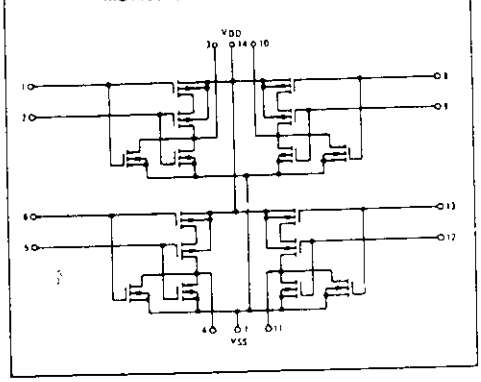
Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time t_{TLH} = (3.0 ns/pF) C_L + 30 ns t_{TLH} = (1.5 ns/pF) C_L + 15 ns t_{TLH} = (1.1 ns/pF) C_L + 10 ns	t_{TLH}	5.0 10 15	– – –	180 90 65	360 180 130	ns
Output Fall Time t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 30 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 22 ns t_{PLH}, t_{PHL} = (0.50 ns/pF) C_L + 15 ns	t_{PLH}, t_{PHL}	5.0 10 15	– – –	90 50 40	180 100 80	ns

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

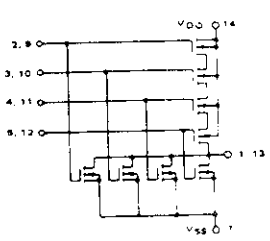


*All unused inputs of AND, NAND gates must be connected to V_{DD}.
All unused inputs of OR, NOR gates must be connected to V_{SS}.

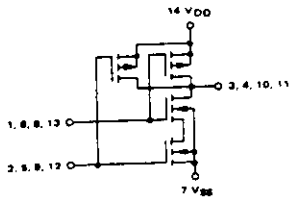
MC14001UB CIRCUIT SCHEMATIC



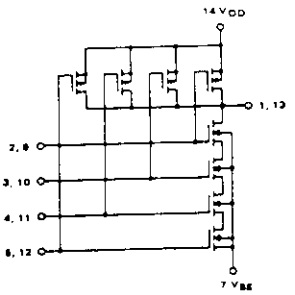
MC14002UB CIRCUIT SCHEMATIC
(1/2 of Device Shown)



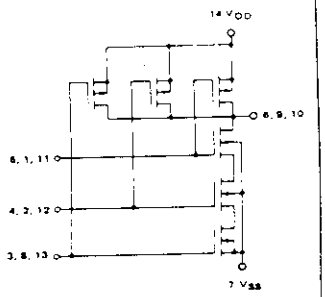
MC14011UB CIRCUIT SCHEMATIC
(1/4 of Device Shown)



MC14012UB CIRCUIT SCHEMATIC
(1/2 of Device Shown)



MC14023UB CIRCUIT SCHEMATIC
(1/3 of Device Shown)



MC14025UB CIRCUIT SCHEMATIC
(1/3 of Device Shown)

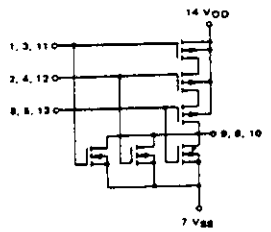


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

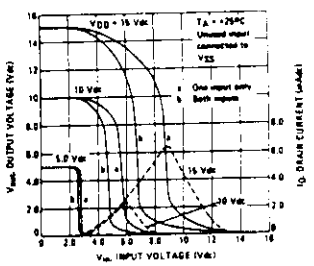


FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

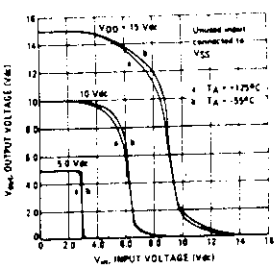


FIGURE 4 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

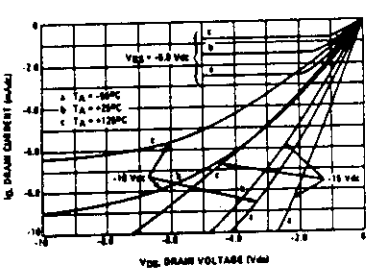


FIGURE 5 – TYPICAL OUTPUT SINK CHARACTERISTICS