# Microcontroller Based VF2 Cluster Test Jig

## Project Report



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IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE AWARD OF THE DEGREE OF

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

**KUMARAGURU COLLEGE OF TECHNOLOGY**

**COIMBATORE-641 006.**

APRIL 1994

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

# Kumaraguru College of Technology

COIMBATORE - 641 006

## CERTIFICATE

*This is to certify that the report entitled*

**MICROCONTROLLER BASED YE2 CLUSTER TEST JIG**

*has been submitted by*

*Mr.* _____

*In Partial fulfilment for the award of*

*Bachelor of Engineering in Electronics and Communication*

*Engineering Branch of Bharathiar University,*

*Coimbatore - 641 046.*

*during the academic year 1993-94*

_____ _____

*Guide* 28 3 94 *Head of Department*

*Certified that the candidate was examined by us in the Project work*

*Viva-Voce Examination held on* _____ *and the University*

*Register Number was* _____

_____ _____

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March 23,1994

## CERTIFICATE

This is to certify that **Mr R Jayapal** student of Kumaraguru College of Technology, Coimbatore has successfully completed the project work on MICROCONTROLLER BASED YE2 CLUSTER TEST JIG in our organisation from 21.08.93 to 23.03.94.

During this period, he was attached to our **PRODUCTION ENGINEERING DEPARTMENT.** His conduct and attendance were good.

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We express our gratitude from the bottom of our heart to **Mr. K. RAMPRAKASH**, M.E., MISTE, Senior Lecturer, Department of Electronics and Communication Engineering for his inspiring guidance, constructive support and timely advice.

**We are greatly indebted to M/s. PRICOL** for having consented to provide us the facilities required to carry out this project.

We are also grateful to **Mr. VIJAYMOHAN (Managing Director, PRICOL), Mr. R. KRISHNAMURTHY (Deputy General Manager, R & D ELECTRONICS** and Mr. N. RAMESH (Deputy Manager, PED), PRICOL for encouraging us to take up this project.

# SYNOPSIS

The Project "MICROCONTROLLER BASED YE2 CLUSTER TEST JIG" is based on the 8748 Microcontroller. This project is to check the performance of the cluster for its operation of the Lamps, Temperature Guages,Fuel Guages, Speedometer etc.

The project involves the switching of lamps in a programmed sequence to check the intensity of lamps, allowing different currents through the coils of the Temperature and the Fuel Guages to check their performance. In addition to the above, this test Jig also tests the Speedometer performance.

The project is a low cost version and is provided with necessary provisions for interface improvements for future calibration and testing of the clusters.

CONTENTS

# INTRODUCTION

Present day automobiles extensively employ electronic indicating devices. Not only fuel level, oil level etc. are indicated but various other sophisticated parameters are also displayed with the help of an integrated panel meter. There was a long felt need of the automobile industry to have a sophisticated automatic testing equipment for such panel meters.

Our project is a pioneering attempt in satisfying their need. The ever increasing desire of the customer to have a high quality product and the pressure of the industry to produce such products in large quantities in quick time has necessiated an accurate and fast test equipments. Our test JIG has successfully met these challenges by providing as quick and accurate means to test lamps in the cluster, fuel level indication, oil temperature indication etc.

It is a pride that this test JIG is being used by a leading automobile cluster manufacturer M/s. PRICOL for testing the clusters which are exported to Japan.

# TEST JIG HARDWARE

## 2.1. INTRODUCTION

The hardware is based on a Microcontroller. Intel's single component 8-bit microcontroller 8748, equipped with powerful instruction set and other versatile functions is used. This will serve as a controlling element to all the other chips provided in the unit. It mainly controls the sequence of timing and sends various data through the buses and ports depending on the sequence timing. These datas signify the necessary outputs.

The other units of the system like decoders, and the DAC efficiently utilise and modify the outputs according to the requirement.

## 2.2. DESCRIPTION OF TEST JIG:

The hardware is based on microcontroller based I/O interface. The microcontroller used is the 8748 Version of the MCS 8048 System. ie. EPROM Version of 8048. The system block diagram is shown in Fig. 1.

The hardware study can be divided into the following categories.

1. Micro Controller
2. Decoders
3. Output Section
4. Digital to Analog Converter
5. Isolation Circuit for the Dac
6. Drive Section

### 2.2.1. MICROCONTROLLER

The heart of the test jig is the Microcontroller and the operation of it is fully controlled by the software.

The Ports of the controller are all programmed as the outputs and these outputs will control the operation of the relays and function of the Guages. The ports of the controller are connected to the I/O through buffers.

The bidirectional bus i.e DB0 to DB7 of the controller is used to drive the Relays which are in turn connected to the lamps. The driving circuit consists of the

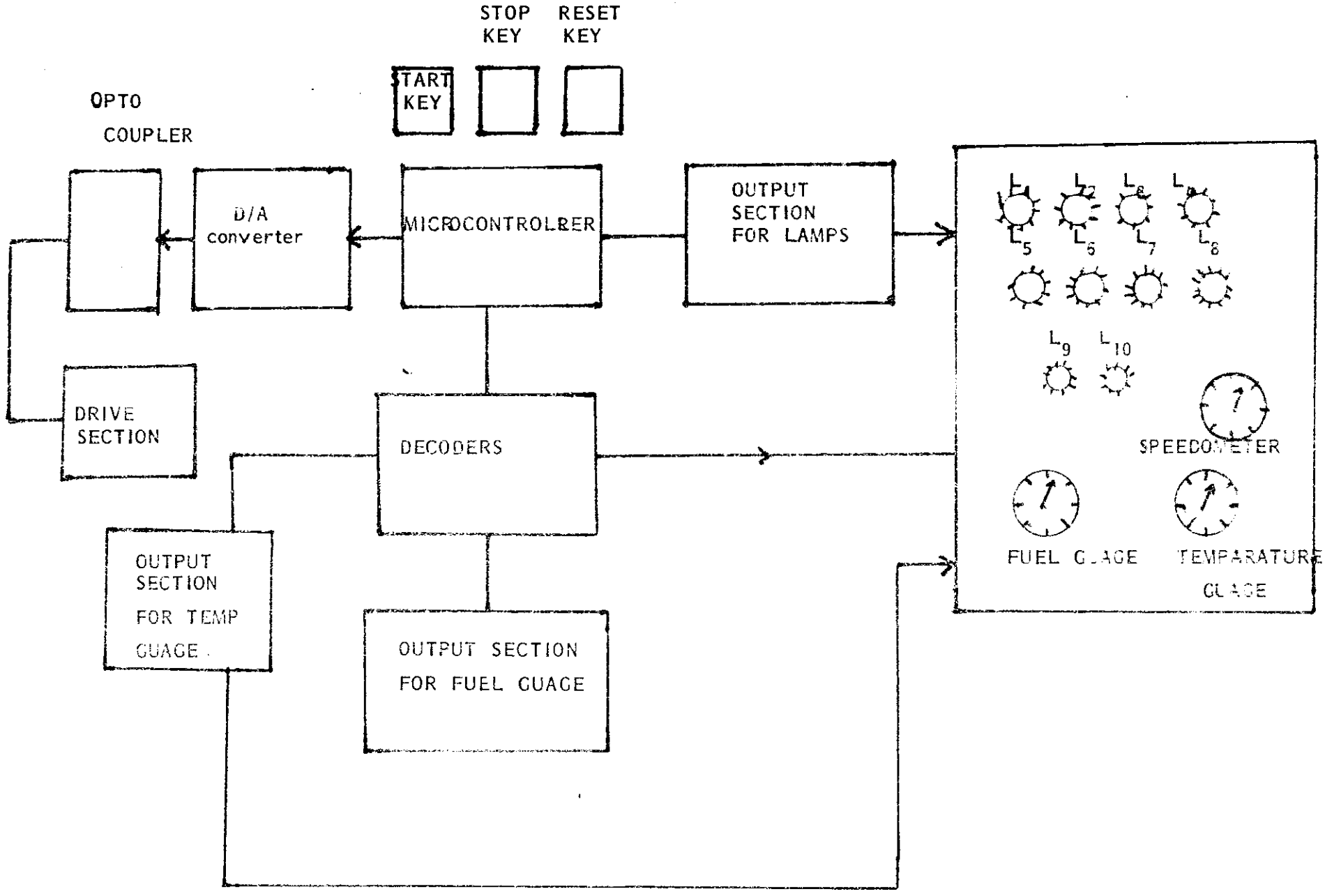


FIG:1 JIG BLOCK DIAGRAM

NPN transistors for switching. The data on the bus will switch ON/OFF the transistors and hence the relay outputs are also changed. The software loaded inside the chip will control the action of the output ie. the way of switching ON/OFF the lamps in cluster.

The Port 1 of the controller is connected to the decoder and the outputs of the latter is used for driving the relays for the Guages.

The Port 2 is fully used for the checking of the REEDSWITCH of the SPEEDOMETER of the cluster. The pins P2.0 to P2.7 of Port 2 is used as the digital input for the DAC. The outputs of Port 2 are connected to an isolator circuit before given to the DAC, to avoid noise problem.

A crystal of 6.00 MHz is used to derive the clock of the processor. Noise filtering circuits are provided at each of the input signals. The built in timer is used for the time delay.

The Rest pin of the processor is connected through a micro switch, which when pressed, resets the complete system and the jig starts functioning from the beginning.

The interrupt pin of Microcontroller is connected to another microswitch, which when pressed, stops the operation of the processor and the stop function is accomplished and the processor waits for the start key to be

pressed. Skip function is also sensed by the start key.

### 2.2.2. DECODERS:

The main criteria for adding the decoder logic is that the number of port pins, can be saved for future expansion.

There are two decoders used in this circuit. They are

a) 2-4 line decoder

b) 3-8 line decoder

### 2.2.2(a) FUNCTIONS OF THE 2-4 LINE DECODER:

The main function of the 2-4 line decoder is indicating the status of operation of the jig. The indication is through the LED's. The various status of operation that LED's indicate are

a) Lamp check

b) Fuel Gauge check

c) Temperature Gauge check

d) Spark check

The input to this decoder is from Port 1 of the controller. The output of the decoder are connected to the indication LED's. The 2-4 line decoder type 74LS139 is used. 74LS139 decoder is an active high decoder in which the outputs are wired to the indication LED's, for status indication. The first LED indicaters Lamp check operation,

Second LED indicates Temp check operation, Third LED indicates Fuel check operation, Fourth LED indicates Reed Switch Check operation.

2.2.2(b) **FUNCTIONS OF THE 3-8 LINE DECODER:**

The function of this decoder is in the checking of the Fuel and temperature Guages. The inputs are derived from the Port 1 of the controller. The first five outputs ie. Yo to Y4 are connected to the temperature guage stages and the next three ie. $Y_5$ to $Y_7$ are wired for checking the fuel guage.

The outputs of the decoder are connected to relays and each relay's NO (Normally open contact) is connected to different values of resistances, which control the current through the coil of the guages. The Port 2 drives a buffer which acts as a protective device.

The 3-8 line decoder type used is 74LS138. The 74LS138 is a active low 3-8 line decoder. The outpus are divided into two parts.

a) **Fuel check outputs**

b) **Temperature check outputs**

In fuel check outputs, the delay between the switching over of outputs are very high (8 minutes) because of the high damping values of the fuel gauges.

The fuel check has got three stages namely empty

Half and Full. For the temperature check the delay is low (15 seconds) because of low damping value of the temperature guages. The temperature check has five stages and each stage switches on a particular relay and the relay, in turn connects itself to a particular resistance which changes the current through the coil of the gauge accordingly. The various values of currents and resistances are given in the specification lists.

2.2.3. OUTPUT SECTION:

The output section mainly consists of the Relays and the protection circuit for the Relays. The relays cannot be driven directly from the port pins,as the current is insufficient from the port pins. Hence transistors are used for driving the relays. When a trigger is given to the transistor, the relay gets energised. The diodes are used across the relays for avoiding the chattering of the relay. The base of the transistor is provided with a resistance to avoid over base current. The minimum current required to energize a relay is around 80 mA. One end of the relay coil is provided with 12 V DC and the other end is connected to the collector of the driver transistor.

The relay used here is 12V DC/75/1/C/O. The NO (Normally Open) contacts are used as the outputs. The outputs are given to the cluster to glow the lamps. and activate the guages. The pole of the relay is given the

ground potential. The hysterisis from these relays are Neglected as it is of less importance to our project.

### 2.2.4. ISOLATION CIRCUIT:

The complete digital ground and circuit are isolated by using an opto-isolator. An opto-isolator is used to avoid line noise and acts as a protective device, in saving the controller (or) the low Voltage Port. The opto isolators used here are MCT 2E (data sheets are provided in appendix). The output of the isolator circuit is from the buffer 74LS244. The output of the isolator, act as the input to the Digital to analog converter. Thus the analog and digital ground are clearly isolated.

The output of the isolaters are pulled high ie. at '0' analog input the DAC outputs are high.

The opto isolator circuit consists of the photo diode and a transistor. Whenever a pulse is given to the diode, the diode conducts and the transistor due to photo effect gets ON and the collector output is at logic '0'.



When the input to diode is '0' the transistor is OFF and hence the output is at logic 1. This acts as an inverted isolator. An opto-isolator is shown in figure 2.

### 2.2.5. DIGITAL TO ANALOG CONVERTER

The digital to analog convertor is used to generate a ramp voltage for the DC drive. The output of the

DAC is varied from 0V to 12V depending on the data outputs of Port 2 of the Microcontroller. This output of the DAC causes the speed of DC shunt motor to vary. The reference to the DAC is derived from the potential divider cut. The 8 bit DAC 0800 is used(Data Sheets in Appendix). The DAC 0800 series are monolithic 8-bit high speed current output digital to analog converters, featuring typical settling time of 100nS. When used as a Multiplying DAC, monotyonic performance over a Multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC 0800 series also features high compliance complimentary current outputs to allow differential output voltages of 20V P.P with simple resistor loads. The reference to full-scale current matching of better than ± LSB eliminates the need for full-scale trims in most applications while the non-linearities of better than ± 0.1% over temperature minimizes system error accumulation.

The performance and characteristics of the device are essentially unchanged over the full ± 4.5 V to ± 18 V power supply range; power dissipation is only 33 mw with ± 5V supplies and is independent of the logic input states. The DAC 0800 is an R-22 ladder digital to analog converter.

## 2.2.6. DRIVE SECTION

The output of the DAC is used to drive the motor. The motor used is a DC shunt motor. The motor can be armature controlled (or) field controlled. In armature controlled tupe tyhe armature flux is varied and field flux is kept constant. In the case of field control it is vice-versa.

A ramp voltage is used for speed control of motor. This ramp voltage is generated using comparator as shown inm the schematic diagram. The speed control of a motor via thyristor bridge is achieved from a techogenerator (alternately isolated armature voltage) with a DC reference voltage.

In this application, the field flux of the dc motor is kept constant and the armature voltage is controlled by single phase fully controlled thyristor bridge, A 240 V, 50 Hz main supply iss rectified by a bridge rectifier made up of diodes to obtain a constant field voltage. A speed sensor is attached to the shaft of the motor. According to the speed of the motor and with respect to reference ramp, an error voltage is produced. The ramp voltage is used for synchronization and is compared with a differential voltage to produce pulse width modulation. The pulse width modulated signal is applied to the emitter of UJT which inturn is

applied to a pulse transformer. The output of the transformer is used to trigger an SCR bridge which in turn controls the armature voltage accordingly and hence the speed of the motor varies. Thus the speedometer of the cluster can be checked for various readings (KMPH) by changing the RPM of type motor accordingly.

## 2.3. WORKING AND DESIGN

The working of hardware can be studied under the following categories.

1. Testing of Lamps
2. Testing of Fuel Guage
3. Testing of Temperature Guage
4. Testing of Reed Switch(Spark check)

### 2.3.1. LAMP CHECK:

This mainly checks all the lamps in the cluster. The main point considered is the checking of the intensity of lamps,of various parameters.

The lamps are connected in the cluster in such a way that there is a common terminal from all the lamps. This common terminal is given to +12V supply. The sequence of the lamps are known and programmed in the chip. Whenever the datas from microcontroller are put through the bus the corresponding transistor gets ON and their respective relays get energized. Hence the ground path is obtained and the lamp glows, and intensity is checked. The lamp check is initiated by the start button and the lamp check LED glows indicating the lamp check. The sequence of lamp check is programmed earlier. The delay between the lamp outputs are also programmable through software. At present the sequence of lamp check is as follows.

i) **Parking lamp**

ii) **Check engine**

iii) **Oil check**

iv) **Battery**

v) **Brake**

vi) **Left turn**

vii) **Right turn and**

viii) **Radium glow**

ix) **High beam**

The delay now provided in the software is about '2' seconds. Suppose if the lamp check for an individual output is desired for a long time, HOLD facility is provided (ref. Art 2.36). If lamp check is to be by passed the function can be skipped (ref. Art 2.35).

2.3.2. **FUEL GUAGE CHECK:**

This checks the power stability and accuracy of the fuel Gauge. The fuel guage deflection is proportional to the current flowing through the coil of the guage. The current through the coil is controlled by the resistance value. At different stages different resistance are selected and hence we get the different deflections.

For the first stage(Empty to Full)a resistance value of 6 ohms is selected and the deflection will be maximum. The second stage (Full to Half) has a resistance of

32.5 ohms and the deflection of the coil reaches half. In the third stage (Half to Empty) the deflection reaches zero point and its resistance 97 ohms.

A delay of 8 minutes is provided between each stage.

The various stages, the resistances, deflections and typical gradations are shown below:

| GRADATION | RESISTANCE | ANGLE WITH TOLERANCE | TIMINGS |
|---|---|---|---|
| FULL | 6 Ohms | 80 ± 2.5° | 8 MINUTES |
| HALF | 32.5 Ohms | 40 ± 5° | 8 MINUTES |
| EMPTY | 97 Ohms | 0 ± 2.5° | 8 MINUTES |

### 2.3.3. TEMPERATURE GUAGE CHECK

This checks the deflection of the temperature guage. This is done in five stages. The principle of working is same as the fuel guage. Here the notable change is that there should be no deflection between the second and third stage.

Damping provided for this guage is low compared to that hof fuel guage. Hence the delay between the stages is programmed for 15 seconds.

The various stages, the resistances, deflections and gradations are shown below.

Speed, RPM and tolerance levels are shown below:

CALIBRATION OF SPEEDOMETER

| STANDARD SPEED IN KMPH | RPM | TOLERANCE LEVELS (KMPH) | |
|---|---|---|---|
| | | MINIMUM | MAXIMUM |
| 20 | 212 | 18.5 | 22.4 |
| 40 | 425 | 38.2 | 43.7 |
| 60 | 637 | 58.2 | 64.1 |
| 80 | 850 | 79.4 | 84.3 |
| 100 | 1062 | 99.5 | 104.7 |
| 120 | 1274 | 119.8 | 125.1 |
| 140 | 1486 | 139.7 | 145.4 |

2.3.5. **SKIP FUNCTION:**

Suppose a function is not needed for operation, a facility is provided in the software to skip the complete function. When the start button is pressed once, the function in operation is skipped and the next function is resumed. During temperature check pressing the reset will skip the temperature check.

2.3.6. **HOLD FUNCTION:**

Pressing the start key and not releasing it will effect the hold facility. The hold facility is released only after the release of the Hold Key.

## 2.4. CLUSTER SPECIFICATION

**COMBIMETER ILLUMINATION**

| INDICATION LAMPS | VOLTAGE | WATTAGE |
|---|---|---|
| PARKING | 12 V | 1.4 W |
| CHECK ENGINE | 12 V | 1.4 W |
| BATTERY | 12 V | 1.4 W |
| OIL CHECK | 12 V | 1.4 W |
| BRAKE | 12 V | 1.4 W |
| LEFT TURN | 12 V | 1.4 W |
| RIGHT TURN | 12 V | 1.4 W |
| RADIUM GLOW | 12 V | 3.4 W |
| HIGH BEAM | 12 V | 1.4 W |

**CALIBRATION OF SPEEDO SYSTEMS:**

| STANDARD SPEED IN KMPH | RPM | TOLERANCE LIMIT(KMPH) | |
|---|---|---|---|
| | | MINIMUM | MAXIUM |
| 20 | 212 | 18.5 | 23.4 |
| 40 | 425 | 38.2 | 43.7 |
| 60 | 637 | 58.2 | 64.1 |
| 80 | 850 | 79.4 | 84.3 |
| 100 | 1062 | 99.5 | 104.7 |
| 120 | 1274 | 119.8 | 125.1 |
| 140 | 1486 | 139.7 | 145.4 |

**TEMPERATURE GUAGE;**

| GRADATION | RESISTANCE | ANGLE WITH TOLERANCE | DELAY TIME |
|---|---|---|---|
| 50°C | 181.4 ohms | 0 ± 8.5° | 15 Secs |
| 83°C | 48.8 ohms | 32° ± 5° | 15 secs |
| 105°C | 26.7 ohms | 32° ± 5° | 15 secs |
| 120°C | 17.9 ohms | 64° ± 2.5° | 15 secs |
| 130°C | 14.2 ohms | FOR REFERENCE | 15 secs |

**FUEL GUAGE:**

| GRADATION | RESISTANCE | ALONG WITH TOLERANCE | DELAY TIME |
|---|---|---|---|
| FULL | 6 ohms | 80° ± 2.5° | 8 MINUTES |
| HALF | 32.5 ohms | 40° ± 5° | 8 MINUTES |
| EMPTY | 97 ohms | 0 ± 2.5° | 8 MINUTES |

# DESIGN OF HARDWARE

**Selection of Transistors($T_1$ - $T_8$):**

The selection of transistors is based on the amount of current that can be allowed to flow through the collector. The collector current should be able to drive the relay. The relay rating is as follows:

12V DC, 75 Ohms, 1 C/O

A minimum of 80 mA current is required for driving a relay. BC 547 type is best suited for our purpose, since it can sink a maximum collector current of 400 mA.

**Selection of Base Resistance:**

We know that

$$R_B \simeq (V_{cc}/I_c) - V_{CE}(Sat)$$

Since $V_{CE\ (Sat)}$ = 0.2 V when transistor is ON it can be neglected.

Therefore,

$$R_B = V_{cc} / I_c$$

Let $I_c$ = 20 mA (minimum)

$$R_B = 12 / 20 \text{ mA} = 0.6K$$

(or) $R_B \simeq$ 1 K

**Criteria for Selecting Inverting Buffer:**

$U_2$ in the Schematic is used as an inverting buffer to drive the transistor. It also acts as a protecting device when there is high Sinking of Current.

**Criteria for Selection of Diodes ($D_1$ - $D_8$)**

Diodes ($D_1$ - $D_8$) across the relay coils $C_1$ to $C_8$ are used to avoid chattering of ther relays during switch over from one stage to other. It also bypasses negative spikes, if any during the operation of the relays. Diode type 1N407 is used(Data sheets in Appendix). The DAC 0800 series are monolithic 8-bit high speed currents output digital to analog converters, featuring typical settling time of 100 nS. When used as a Multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC 0800 series also features high compliance complimentary current outputs to allow differential output voltages of 20V P-P with simple resistor loads. The reference to full-scale current matching of better than ± LSB eliminates the need for full-scale trims in most applications while the non-linearities of better than ± 0.1% over temperature minimizes system error accumulation.

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# MICROCONTROLLER 8748

## 3.1 INTRODUCTION

The heart of the test jig is the system controller. In order to provide room for flexibility and versatility, the use of such a system controller becomes essential. Instead of opting for a microprocessor which requires the use of additional peripheral devices like program memory, data memory, 8255 PPI etc, choice of a microcontroller is more suitable.

Microcontrollers are microcomputers used for dedicated applications incorporating clock, CPU, RAM ROM, I/O ports and interrupt capability all within a single chip. Hence, the use of microcontrollers increases the efficiency, reduces overall cost, occupies less space and is more advantageous. Some of the benefits which arise from having a one-chip micromputer are:

1. Small size and power for the controller portion of an instrument.
2. The opportunity to identify one chip as a "Kernel" for the digital portion of an instrument for self-test purposes.

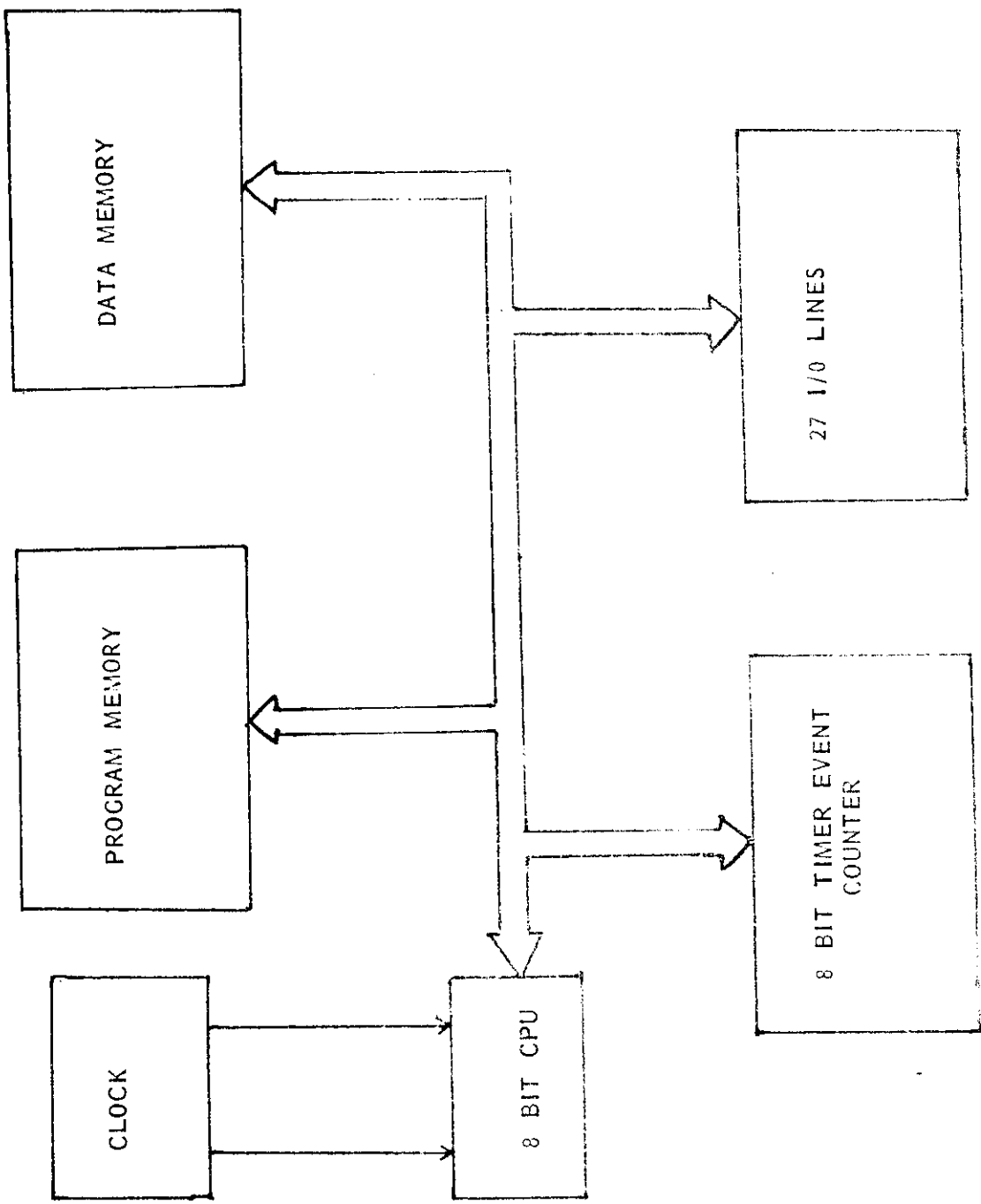



FIG: BLOCK DIAGRAM OF 8748 MICROCONTROLLER

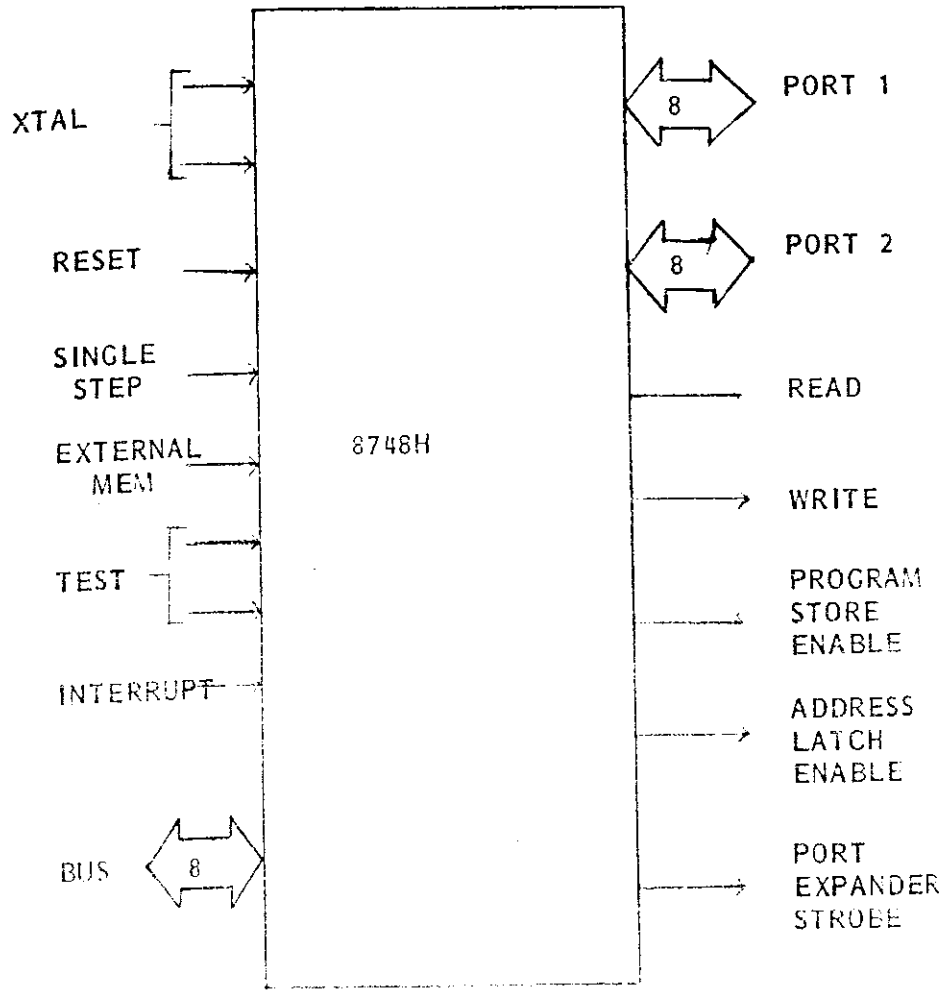



FIG:

LOGIC SYMBOL

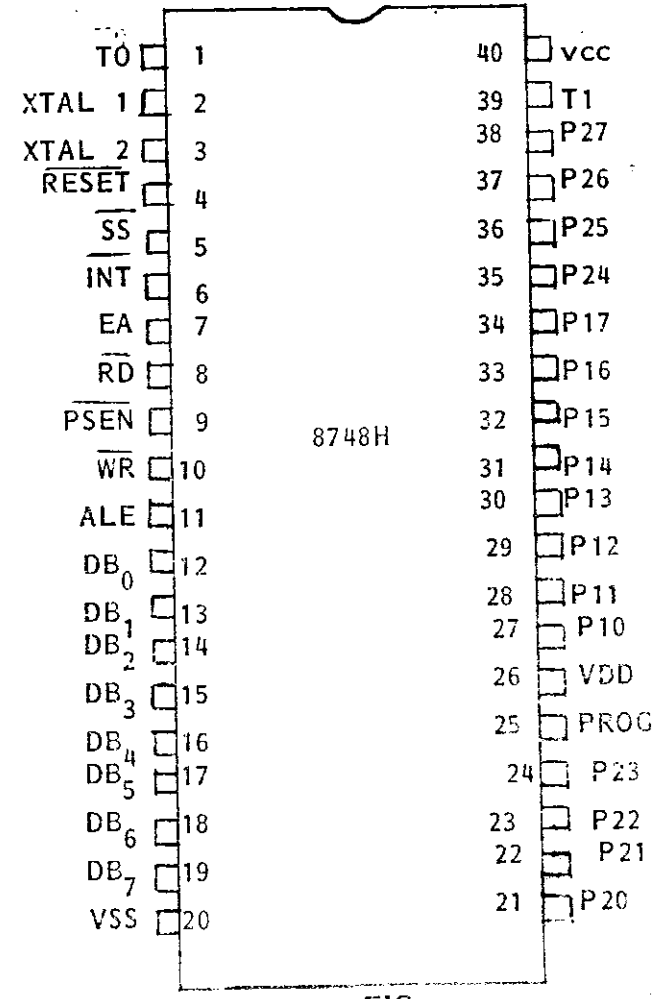



FIG:

PIN CONFIGURATION

3. The definition of an especially effificient instruction set, with mostly one byte instructions.

## 3.2. SELECTION OF PROCESSOR

Selection of a microcontroller well suited to our application requires a wide range of analysis of the existing microcontrollers. Intel 8048 and 8051 series, Motorolas M6801 series, the MOS Technology 370, Texas Instruments TMS 1000 Zilog's Z8 and Toshiba's OKI series are some of the microcontrollers available.

Most of these microcomputers are 8-bit micromputers except TMS 1000 which has a word length of 4 bits. The Intel 8748, which is also very popular is a member of Intel 8048 series. The Intel 8051 is the latest single chip 8-bit micro- computers which has a very powerful instruction set and operates with 12 MHz clock. Intel 8096 series of microcomputer are 16-bit single chip microcomputers. Of these microcontrollers available, the final bid was made on 8748. This microncontroller has a program memory of 1K bytes and a data memory of 64 bytes. It has 2 ports of 8 pins each and a bidirectional databus (8 pins). It has an inbuilt timer/ counter also. All these options suit our requirements very well. In terms of cost also 8748 is the most economical processor of all other controllers and hence chosen.

## 3.3. ARCHITECTURE OF 8748

Intel's single chip microcontroller 8748 is pin compatible with 8048 which is considered to be the head of intel's-MCS-48 family of microcontrollers. The instruction set for both of them are same.

Microcontroller 8748 is provided with a 8-bit CPU, 1 K x 8 ROM programe memory, 64 x 8 RAM data memory, 27 I/O lines and an 8-bit timer / event counter. The main advantage is that either the capacity of program memory or data memory or even both can be expanded by connecting memory chips externally.

**ARCHITECTURE:**

**ARITHMETIC SECTION:**

The arithmetic section of the processor contains the basic data manipulation function of the 8748 and can be divided into the following blocks:

1. Arithmetic Logic unit
2. Accumulator
3. Carry flag
4. Instruction decoder

**Instruction Decoder:**

The operation code portion of each program instruction is stored in the instruction decoder and converted to outputs which control the function of each of the blocks of the Arithmetic section. There lines control

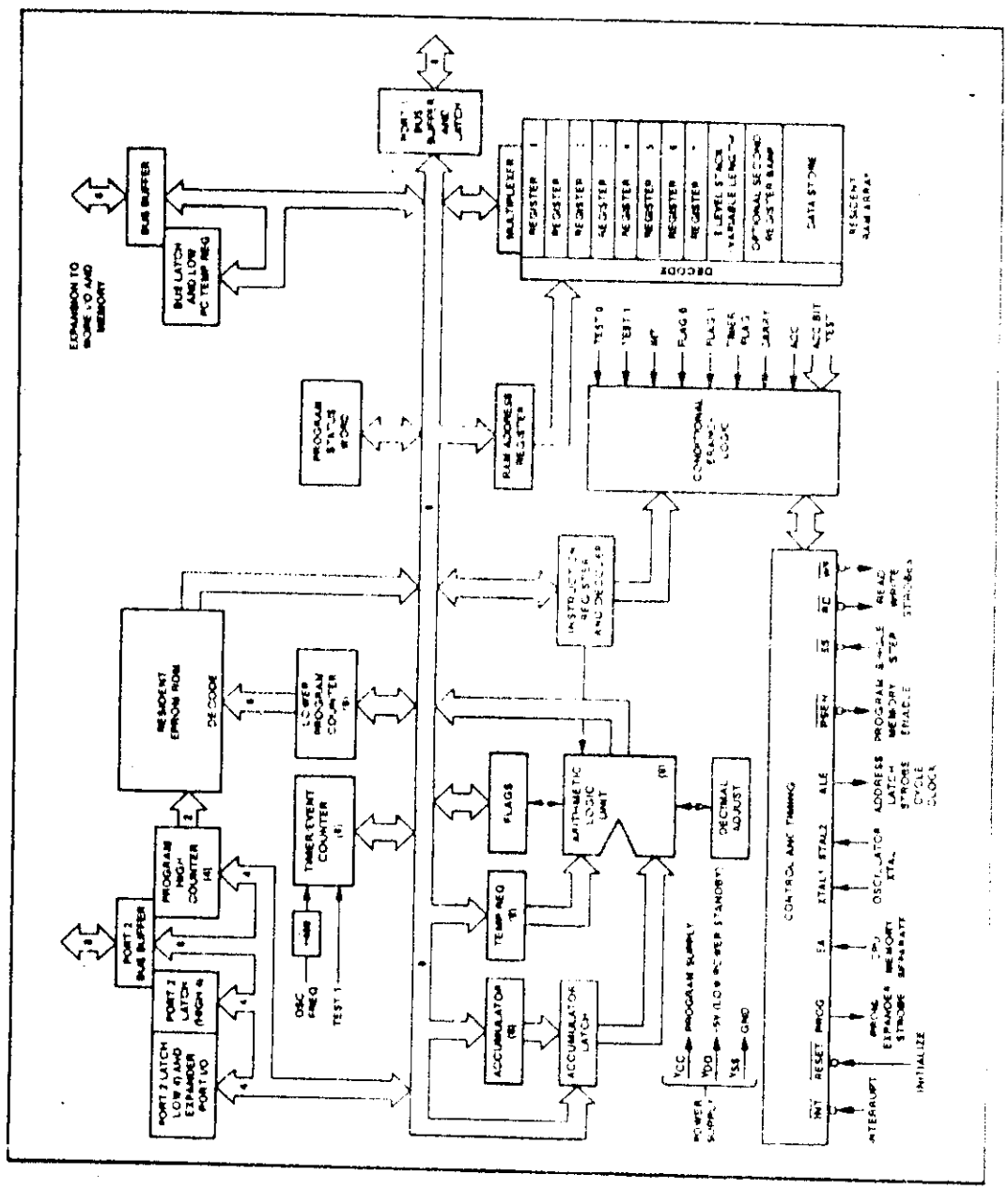



FIG: ARCHITECTURE OF 8748

the source of data and the destination register as well as the function performed in the ALU.

**ALU:**

The ALU accepts 8-bit data words from one or two sources and generally an 8-bit result under control of the instruction decoder. The ALU can perform functions like Add with or without carry, AND, OR, EX-OR, Increment / Decrement, Bit complement, Rotate left, right, swap nibbles BCD decimal adjust etc. If the operation performed by the ALU results is a value represented by more than 8-bits, a carry flag is set in the program status word.

**ACCUMULATOR:**

Accumulator is the single most important data register in the processor, being one of the sources of input to the ALU and often the destination of the result of operations performed in the ALU. Data to and from I/O ports and memory also normally passes through the accumulator.

**PROGRAM MEMORY**

Resident program memory consists of 1024, 2048 and 4096 words eight bits wide which are addressed by the program counter. In the 8748 this memory is user programmable and erasable EPROM. There are three locations in program memory of special importance. They are :

1. **Location 0** : Activating the rest line of the processor causes the first instruction to be fetched from location 0.
2. **Location 3** : Activating the interruprt input line of the processor causes a jump to subroutine at lcoation 3.
3. **Location 7:** A timer /counter interrupt resulting from timer / counter overflow causes a jump to subroutine at location 7.

Therefore the first instruction to be executed after initialization is stored is location 0, the first word of the interrupt service subroutine is stored in location 3 and the first word of a timer / counter service routine is stored in location 7.

Program memory can also be used to store constants as well as program instructions. The program memory map has been shown in Appendix B.

**Data Memory:**

Resident data memory is organised as 64 words 8-bit wide. All locations are indirectly addressable through

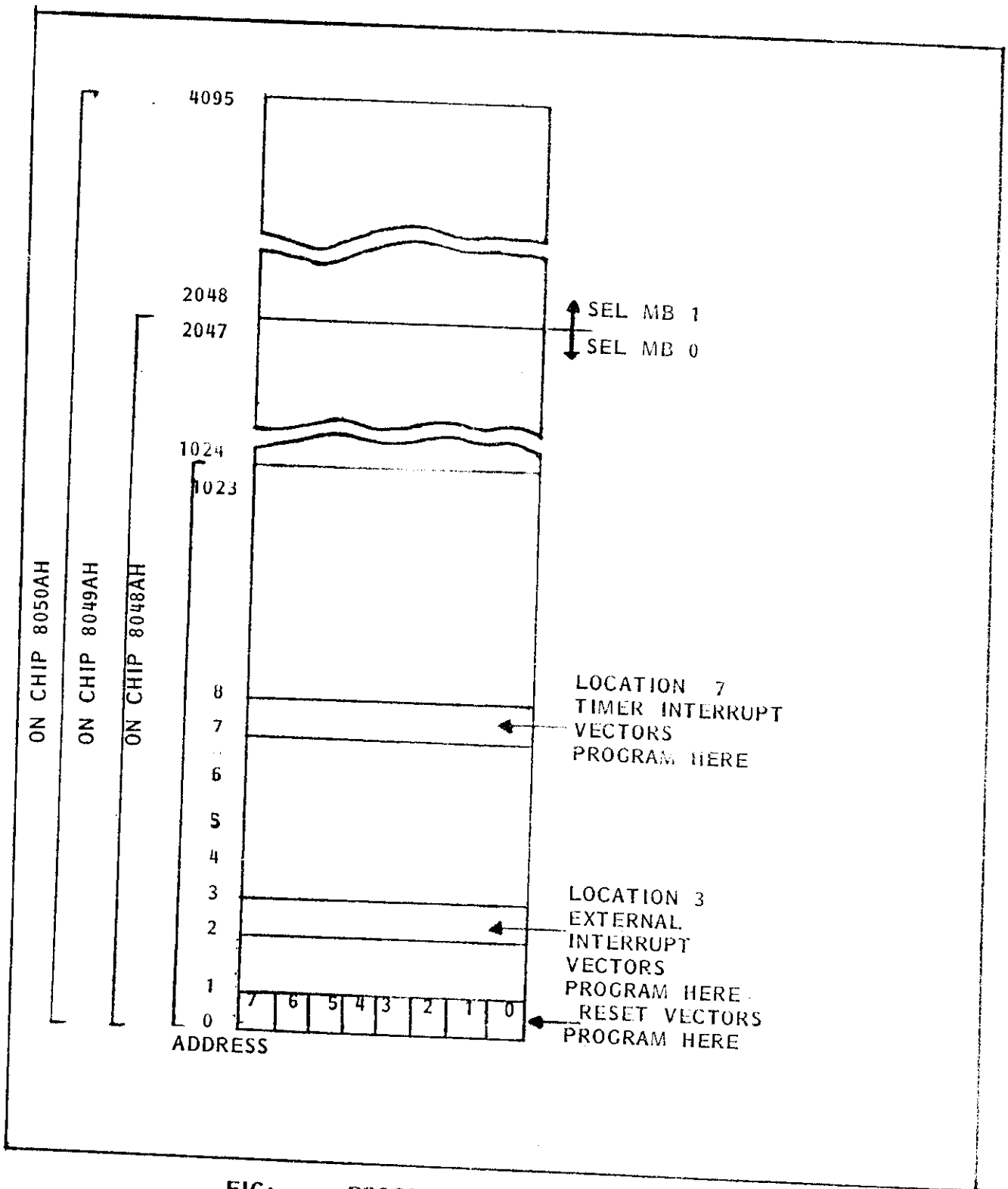



**FIG: PROGRAM MEMORY MAP**

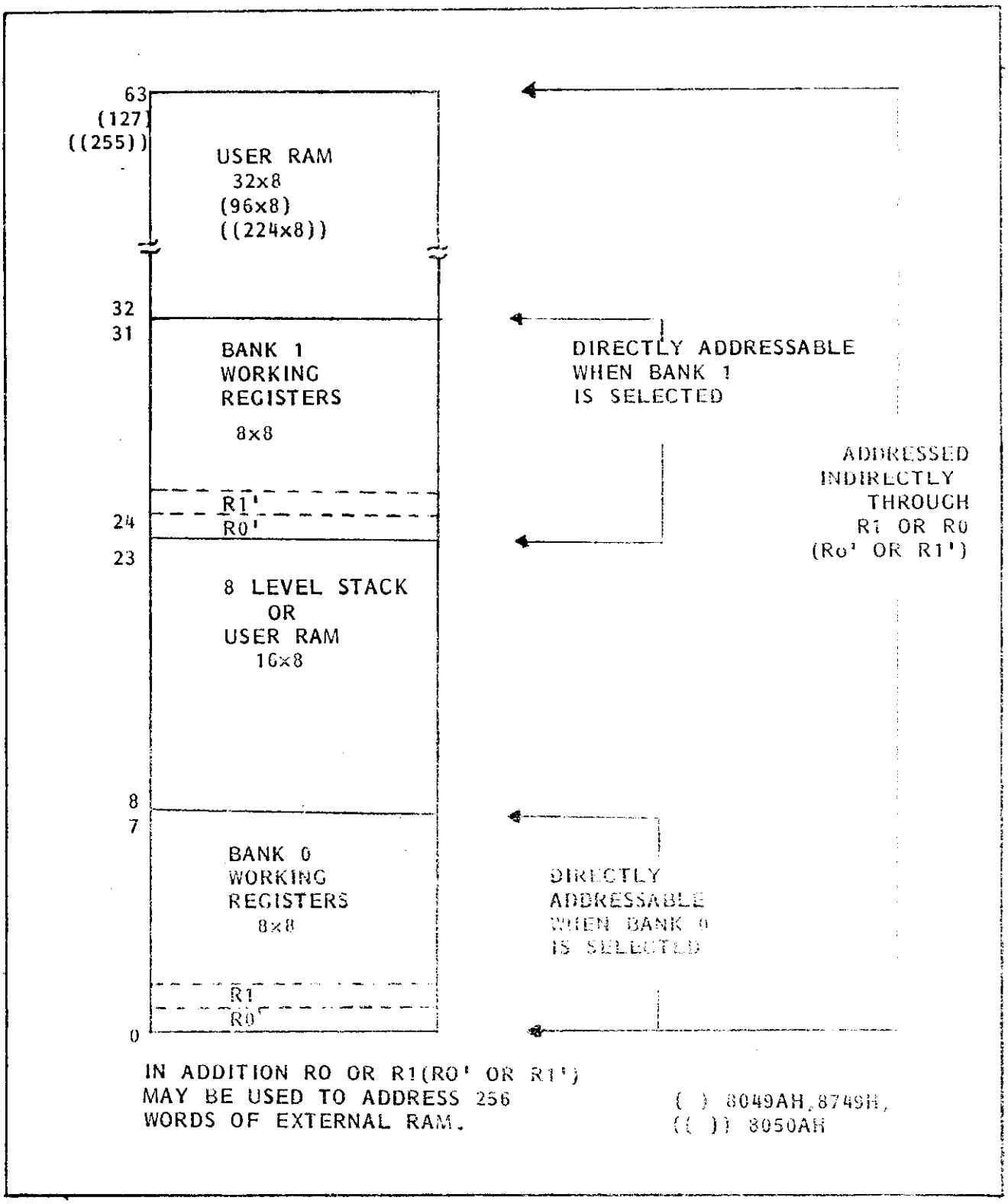



**FIG: DATA MEMORY MAP**

either of RAM the pointer registers which reside at address 0 and 1 of the register array. In addition as shown in the diagram the first eight locations of the register array are designated as the working register and are directly addressable by several instructions. Since these registers are easily addressed they are used mostly to store more frequently accessed intermediate results.

By executing a register bank switch instruction (SEL RB) loc 24- 31 over designated as working registers in place of loc 0-7 and are then directly addressable. This second bank of registers may be used as an extension of the first bank or unserved for use during interrupt service subroutines allowing the registers of bank 0 used in the main program to be instantly 'saved' by a bank switch. Registers R0 and R1 are a part of the working register array, bank switching effectively used to access upto four separate working areas in RAM at a time.

RAM locations (8-23) also serve a dual role in that they contain the program counter stack. These locations are addressed by the stack pointer as well as by the pointers R0 and R1. The data memory map has been shown in Appendix B.

**Input / Output :**

It has got 27 lines which can be used for input or output functions. These lines are grouped as 3 ports of 8 lines. These serve as either I/P, O/P or bidirectional ports

and 3 test I/Ps which can alter the program sequences which listed by conditional jump instruction.

Ports 1 and 2 are each 8- bit wide and have identical characteristics. As input ports these are non-latching ie., inputs must be present until read by an input instruction. The lines of port 1 and 2 are called quasi-directional because of a special output circuit structures which allows each lines to serve as an I/P, O/P or both, even though O/Ps are statically latched. Each lines is continuously pulled up to Vcc through a resistive device of relatively high impedance.

It is important to note that the ORL and ANL are read/write operations. When executed, the Controller "reads" the port, modifies the data according to the instructions, then "writes" the data back into the port. The "writing" enables the low impedance pull-up momentarily again even if the data was unchanged from a "1". This specifically applies to configuration that have inputs and 1 outputs mixed together on the same port.

**BUS:**

Bus is also an 8-bit port which is a true bidirectional port with associated input and output strobes. If the bidirectional feature is not needed, bus can serve as either a statically latched output port or non-latching input

port. I/P and O/P lines on this port cannot be mixed however.

As static port, data is written and latched using the OUTL instruction and inputted using the INS inst. The INS and OUTL unit generate pulses on the corresponding $\overline{RD}$ and $\overline{WR}$ output strobe lines, however, in the static port mode they are generally not used. As a bidirectional port the MOVX instructions are used to read and write port. A write to the port generates a pulse on the $\overline{WR}$ output line and output data generates a pulse on the $\overline{RD}$ output line and input data must be valid at the trailing edge of $\overline{RD}$. When not being written or read, the BUS lines are in a high impedance state.

**Test and Int. Inputs:**

Three pins serve as inputs and are testable with the conditional jump inst. These are T0, T1 and $\overline{INT}$. These pins allow inputs to cause program branches without the necessity to load an input port into the accumulator. The T0, T1 and $\overline{INT}$ pins have other possible functions as well.

**Program Counter and Stack**

The program counter is an independent counter and the program counter stack is implemented using pairs of registers in the data memory array. The program counter is initialized to zero by activating the $\overline{RESET}$ line.

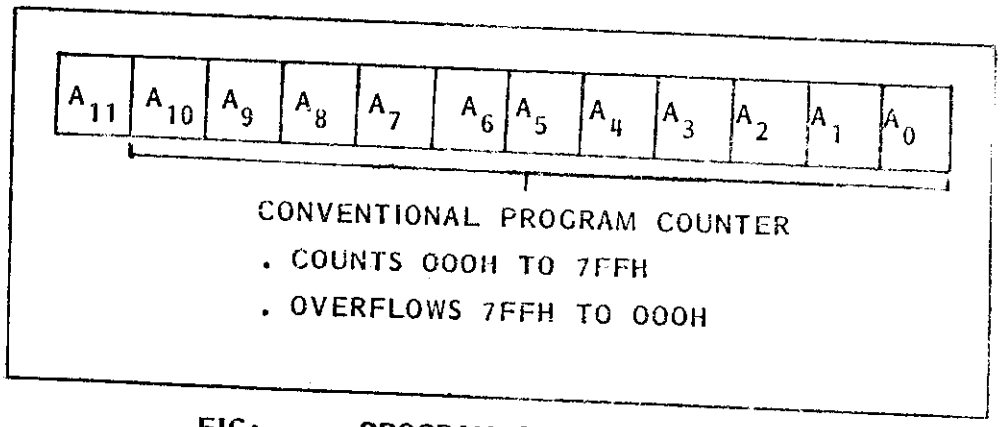



FIG: PROGRAM COUNTER

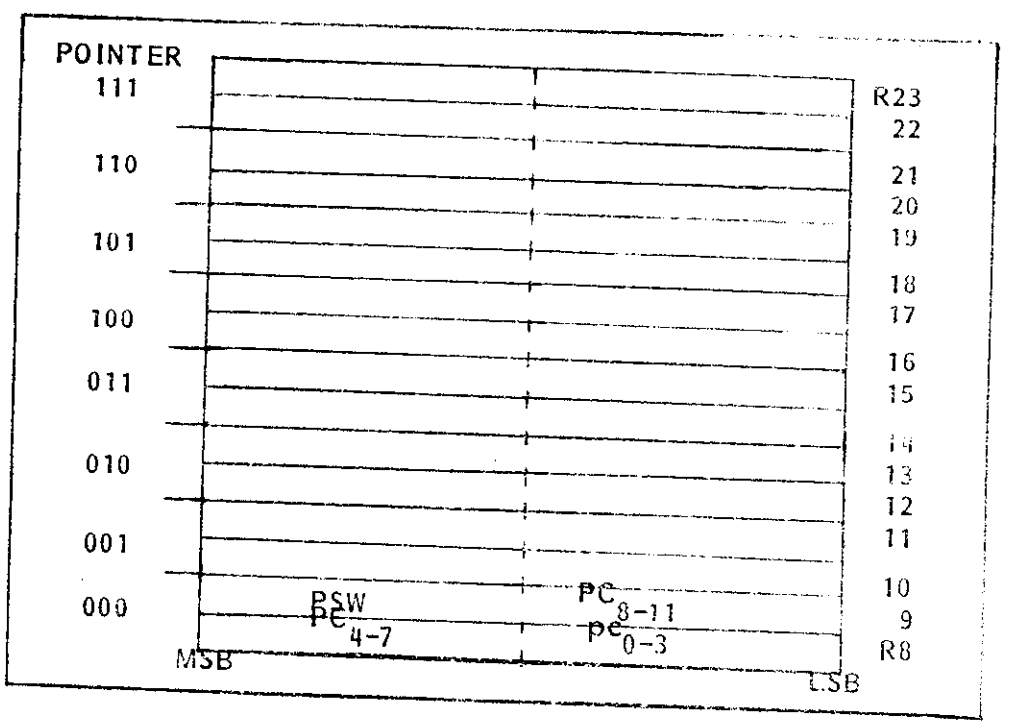



FIG: PROGRAM COUNTER STACK

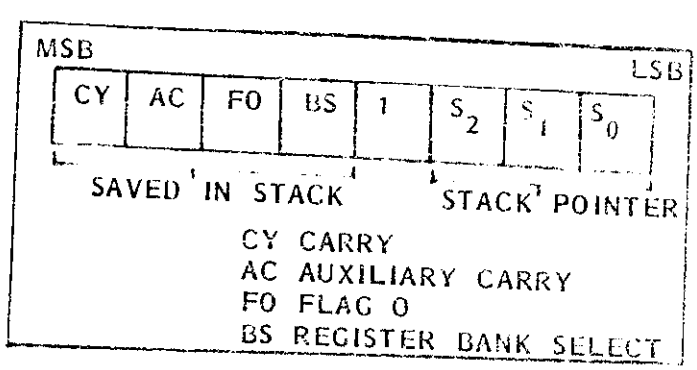



FIG: PROGRAM STATUS WORD(PSW)

An interrupt or CALL to a subroutine causes the contents of the Program Counter to be stored in one of the 8-register pairs of the Program Counter stack as shown.

The pair to be used is determined by a 3 bit stack pointer which is part of the program status word (PSW) data RAM locations 0-29 are available as stack registers and are used to store the current Program Counter value and 4 bits of PSW as shown.

Nesting of subroutines within subroutines can continue up to eight times without over flowing the stack. The end of a subroutine, which is signalled by a return instruction causes the stack pointer to be decremented and the contents of the resulting register pair to be transferred to the program counter.

**Program status word**

An 8-bit status word which can be loaded to and from the accumulator exists called the Program Status Word. The PSW is a collection of flip-flop which can be read or written as a whole. The ability to write to PSW allows for easy restoration of machine status after a power down sequence.

The upper four bits of PSW are stored in the Program Counter stack with every call to subroutine or interrupt vector and are optionally restored upon returns with the RETR instruction. The RET instruction does not update PSW.

**PSW:**

| | | |
|---|---|---|
| Bits 0 - 2 | - | Stack pointer bits (SD0, S1, S2) |
| Bit 3 | - | Not used ('1' level when read 1) |
| Bit 4 | - | Working register back switch bit(BS)<br>0 = Bank 0<br>1 = Bank 1 |
| Bit 5 | - | Flag0 bit (F0) user controlled flag which can be complemented or cleared and tested with the conditional jump instruction JF0. |
| Bit 6 | - | Auxillary carry (AC) bit generated by an ADD instruction and used by the decimal adjust instruction DAA. |
| Bit 7 | - | Carry (CY) carry flag which indicates that the previous operation has resulted in overflow of the accumulator. |

**Conditional branch logic:**

The conditional branch logic within the processor enables several conditional branches internal and external to the processor to be tested by the user's program.

**Interrupt:**

An interrupt sequence is initiated by applying a low '0' level input to the INT pin. The interrupt line is sampled every instruction the interrupt line is sampled in the 2nd cycle only. The $\overline{INT}$ must be held low for atleast 3 machine cycles to ensure proper interrupt operations. As in any CALL to subroutines, the program counter and program status word are saved in the stack. The interrupt system is single level in that once an interrupt is detected all

further interrupt requests are ignored until execution of an RETR enables the interrupt input logic. This occurs at the beginning of the second cycle of the RETR instruction. This sequence holds true also for an internal interrupt generated by timer, overflow. If an internal timer/counter generated interrupt and an internal interrupt are detected at the same time, the external source will be recognized.

**Timer / Counter:**

The 8748 contains a counter to aid the user in counting external events and generating accurate time delays without placing a burden on the processor for these functions.

**Counter:**

The 8-bit binary counter is presettable and readable with two MOV instructions which transfer the contents of the accumulator to the counter and vice versa. The counter content may be affected by $\overline{\text{RESET}}$ and should be initialized by software. The counter is stopped by a $\overline{\text{RESET}}$ or STOP TCNT instruction and is started by a START T instruction or as an event counter by START CNT instruction. Once started the counter will increment to this maximum count (FF) and overflow to zero continueing its count until stoped by a STOP TCNT instruction. The increment from maximum count to zero results in the setting of an overflow flag flip-flop and in the generation of an interrupt request. The state of the overflow flag is testable with the conditions jump

instruction JTF. The flag is reset by executing a JTF or by $\overline{\text{RESET}}$. The timer interrupt may be enabled or disabled independently of external interrupt by the ENT CNTI and DIS CNTI instruction. If enabled, the counter overflow will cause a subroutine call to location 7 where the timer or counter service routine may be stored. If the timer and external interupt occur simultaneously, the external source will be recognized and the call will be to location 3. Since the timer interrupt is latched it will remain pending until the external device is serviced and immediately be recognized upon return from the services routine. The pending timer interrupt is reset by the call to location 7 or may be removed by executing a DISCNTI instruction.

**Event Counter:**

The counter input is connected with the T1 I/P pin as START CNT instruction is executed and the counter iks enabled. The T1 input is sampled at the beginning of state 3. Subsequent high to low transition on T1 will cause the counter to increment T1 must be held for atleast one T cycle to ensure that it won't be missed. The maximum rate at which the counter may be incremented is once per three instruction cycles. There is no minimum frequency T1 input must remain high atleast 1/5 of a T cycle after transition.

Timer:

Execution of a START instruction connects an internal clock to the counter input and enables the counter. The internal clock is derived by passing the basic machine cycle clock through a 32 prescaler. The prescalar is reset during START instruction. The resulting clock increments the counter every 32 machine cycle. Various delay from 1 to 256 counter can be obtained by presetting the counter and detecting overflow. ALE divided by 3 or more can serve as an external clock. Very small detage of 'fine timing' of larger delays can be easily accomplished by software delay loops.

## 3.4. Programming the 8748

The following chapter gives a brief overview of the system controller (8748) architecture and its design aspects.

The MCS-48 instruction set is extensive for machine of its size and has been tailored to be straight forward and very efficient in its use of program memory. All instructions are either one of two bytes in length and over 80% are only one byte long. Also, call instructions execute in either one or two cycles and over 50% of all instructions execute in a single cycle. Double cycle instructions include all immediate instructions, and all two byte instructions.

The MCS - 48 microcomputers have been designed to handle arithmetic operations efficiently in both binary and

BCD as well as handle the single-bit operations required in control applications. Special instructions have also been included to simplify loop counters, table took-up routines, and N-way branch routines.

**Data transfers:**

The 8-bit accumulator is the central point for all data transfers within the 8048. Data can be transferred between the 8 registers of each working register bank and the accumulator directly, i.e., the source or destination register is specified by the instruction. The remaining locations of the internal RAM array are referred to as Data Memory and are addressed indirectly via an address stored in either R0 and R1 are also used to indirectly address external data memory when it is present. Transfers to and from internal RAM require on cycle, while transfers to external RAM requiure two. Constants stored in Program Memory can be loaded directly to the accumulator and to the 8 working registers. Data can also be transferred directly between the accumulator and the on-board timer counter or the accumulator and the Program Status word (PSW). Writing to the PSW alters machine status after an 8 bit word is written to the stack pointer if necessary.

**Accumulator Operations:**

Immediate data, data memory, or the working

registers can be added with or without carry to the accumulator. These sources can also be ANDed, ORed, or Exclusive ORed to the accumulator. Data may be moved to or from the accumulator and working registers or data memory. The two values can also be exchanged in a single operation.

In addition, the lower 4 bits of the accumulator can be exchanged with the lower 4-bits of any of the internal RAM locations. This instruction, along with an instruction which swaps the upper and lower 4-bit halves of the accumulator, provides for easy handling of 4-bit quantities, including BCD numbers. To facilitate BCD arithmetic, a Decimal Adjust instruction is included. This instruction is used to correct the result of the binary addition of two 2-digit BCD numbers. Performing a decimal adjust on the result in the accumulator produces the required BCD result.

Finally, the accumulator can be incremented, decremented, cleared, or complemented and can be rotated left or right I bit at a time with or without carry.

Although there is no subtract instruction in the 8048AH, this operation can be easily implemented with three single byte single-cycle instruction.

A value may be subtracted from the accumulator with the result in the accumulator by:

Complementing the accumulator

Adding the value to the accumulator

Complementing the accumulator

**Register operations:**

The working registers can be accessed via the accumulator as explained above, or can be loaded immediate with constants from program memory. In addition, they can be incremented or decremented or used as loop counters using the decrement and jump, if not zero instruction, as explained under branch instructions.

All Data Memory including working registers can be accessed with indirect instructions via R0 and R1 and can be incremented.

**Flags:**

There are four user-accessible flags in the 8048AH; Carry, Auxiliary Carry, F0, and F1.Carry indicates overflow of the accumulator, and Auxiliary Carry is used to indicate overflow between BCD digits and is used during decimal-adjust operation. Both Carry and Auxiliary Carry are accessible as part of the program status word and are stored on the stack during subroutines. F0 and F1 are undedicated general-purpose flags to be used as the programmer desires. Both flags can be cleared or complemented and tested by conditional jump instructions. F0 is also accessible via the Program Status word and is stored on the stack with the carry flags.

**Branch Instructions:**

The unconditional jump instruction is two bytes and allows jumps anywhere in the first 2K words of program memory. Jumps to the second 2K of memory (4K words are directly addressable) are made first by executing a select memory bank instruction, then executing the jump instruction. The 2K boundary can only be crossed via a jump or subroutine call instruction, i.e., the bank switch does not occur until a jump is executed. Once a memory bank has been selected all subsequent jumps will be to the selected bank until another select memory instruction is executed. A subroutine in the opposite bank can be accessed by a select memory bank instruction followed by a call instruction. Upon completion of the subroutine, execution will automatically return to the original bank; however, unless the original bank is reselected, the next jump instruction encountered will again transfer execution to the opposite bank.

Conditional jumps can test the following inputs and machine status.

To Input pin
T1 Input pin
INI Inpuut Pin
Accumulator Zero
Any bit of Accumulator
Carry Flag
F0 Flag
F1 Flag

Conditional jumps allow a branch to any address within the current page (256 words) of execution. The conditions tested are the instantaneous values at the time the conditional jump is executed. For instance, the jump on accumulator zero instruction tests the accumulator itself not an intermediate zero flag.

The decrement register and jump if not zero instruction combines a decrement and a branch instructions to create an instruction very useful implementing a loop counter. This instruction can design any one of the working registers as a counter and can elect a branch to any address within the current page of execution.

A single-byte indirect jump instruction allows the program to be vectored to any one of several different locations based on the contents of the accumulator. The contents of the accumulate points to a location to program memory which contains the jump address. The 8-bit jump address refers to the current page of execution. This instruction could be used. For instance, to vector to any one of several routines based on an ASC II character which has been loaded in the accumulator to this way ASCII key key inputs can be used to initiate various routine.

**Subroutines:**

Subroutines are entered by executing a call instruction. Calls can be made like unconditional jumps to

any address in a 2K word bank, and jumps across the 2K boundary are executed in the same manner. Two separate return instruction determine whether nor not status (Upper 4-bits of PSW) is restored upon return from the subroutine.

The return and restore status instruction also signals the end of an interrupt service routine if one has been in progress.

**Timer Instructions:**

The 8-bit on board timer counter can be loaded or read via the accumulator while the counter is stopped or while counting. The counter can be started as a timer with an external clock applied to the TI input pin. The instruction executed determines which clock source is used. A single instruction stops the counter whether it is operating with an internal or an external clock source. In addition, two instructions allow the timer interrupt to be enabled or disabled.

**Control Instructions:**

Two instructions allow the external interrupt source to be enabled or disabled. Interrupts are initially disabled and are automatically disabled while an interrupt service routine is in progress and re-enabled afterward.

There are four memory bank select instructions, two to designate the active working register bank and two to

control designate the active working register bank and two to control program memory banks. The working register bank switch instructions allow the programmer to immediately substitute second 8 - register working register bank for the one is use. This effectively provides 16 working registers or it can be used as a means of quickly saving the contents of the registers in response to an interrupt. The user has the option to switch or not to switch banks on interrupt. However, if the banks are switched, the original bank will be automatically resotred upon execution of a return and restore status instruction at the end of the interrupt service routine.

A special instruction enables an internal clock, which is the XTAL frequency divided by three to be output on pin T0. This clock can be used as a general purpose clock in the user's system. The instruction should be used only to initialize the system since the clock output can be disabled only by application of system reset.

**Input/Output Instructions:**

Ports 1 and 2 are 8-bit static I/O ports which can be loaded to and from the accumulator. Outputs are statically latched but inputs are not latched and must be read while inputs are present. In addition, immediate data from program memory can be ANDed or ORed directly to Port 1 and Port 2 with the result remaining on the port. This

allows "masks" stored in program memory to selectively set or reset individual bits lof the I/O ports. Ports 1 and 2 configured to allows input on a given pin by first writing a "I" out to the pin.

An 8-bit port called BUS can also be accessed via the accumultor and can have statically latched outputs as well. It too can have immediate data AND ed ORed directly to its outputs, however, unlike ports 1 and 2, all eight lines of BUS must be treated as either input or output at any one time. In additions to being a static port, BUS can be used as a true syncrhonous bi-directional port using the Move External instructions used to access external data memory. When these instructions are executed, a corresponding READ or WRITE pulse is generated and data is valid only at that time. When data is not being transferred, BUS is in a high impedance state. Note that the OUTL, ANL, and the BRL instructions for the BUS are for use with internal memory only.

The basic three on-board I/O ports can be expaned via a 4-bit expander bus using half of port 2.I/O expander devices on this bus consist of four 4-bit ports which are addressed as ports 4 through 7. These ports have their own AND and OR instructions like the on-board ports as well as move instructions to transfer datas in or out. The expander

AND and OR instructions, however, combine the contents of accumulator with the selected port rather than immediate data as is done with the on-board ports. I/O devices can also be added externally using the BUS port as the expansion bus. In this case the I/O port become "memory mapped", i.e., they are addressed in the same way as external data memory and exist in the external data memory address space addressed by pointer register Ro or R1.

The instruction set has been given in the Appendix (d).

# SYSTEM SOFTWARE

## 4.1. INTRODUCTION

The sequence and the timing for the testing of the Jig is mainly accomplished by the software loaded into the EPROM of the chip. The software is based on Assembly language of Intel's 8748 chip. The cross assembler used here is X8748. The linker used is link 48. The cross-assembler will convert the assembly language to object file. The linker will convert the object code to Hex Code. The complete program is first tested on an emulator. Once the program is working, it is down loaded into microcontroller EPROM through an EPROM programmer. The procedure of EPROM programming is explained in the next section.

## 4.2. EPROM PROGRAMMING:

The procedure for EPROM programming is given below :

1. Erase EPROM (8748) in UV ERASER for 10 minutes
2. Switch on PC
3. Wait for PROMPT C:\> TEXCOM
4. TYPE XTIPP
5. Switch on programmer
6. Press space bar twice

7. TYPE M4
8. Insert Blank EPROM FROM ERASER INTO Programmer observing correct polarity
9. TUYPE vb
10. If non-blank is displayed Goto 1 and 8 ELSE PROCEED
11. Wait for Prompt >
12. Press 'Ctrl' 'D', Then Answer menu
13. Wait for LED IN programmer to blink and and stop
14. Take out EPROM for use.

## 4.3. SOFTWARE OVERVIEW:

### 8748 SOFTWARE CHARACTERISTICS:

1. DATA MANIPULATION INSTRUCTIONS:

   a) Arithmatic and logic data manipulation instructions.

   b) Bit set and reset data manipulation instructions.

2. DATA MOVEMENT INSTRUCTIONS:

Both internal and external RAM are fully accessible by instruction set. Indirect and direct data fetches are also possible.

3. PROGRAM-MANIPULATION INSTRUCTIONS:

Decrement and skip if zero, over twenty conditional branches, 8-level stack with expansion capability, 2-Vector interupts, 2-programmable flag bit under software control.

4. PROGRAM-STATUS MANIPULATION INSTRUCTIONS:

Status word is fully accessible and is stored in the stack.

### SPECIFICATION SUMMARY:

8048 systems have split memory architecture with 1K to 4K bytes of program ROM (or) EPROM on chip and 64 to 256 bytes in seperate space, also on chip. I/O has its own

space and instructions to operate directly on I/O ports. All spaces are expandable, program memory to 4K bytes, data memory to 256 bytes, I/O to unlimited amounts. I/O can use 8085/85 peripherals. Devices have 8-level stack for subroutine testing and interrupt response. Dual banks of working registers, aloow rapid content switching. 8048 family members execute their 1 and 2 cycle instructions at 1-cycle times raning from 1.36 to 15 usec. It is NMOS 5 V technology in 40 DIP and 44-Pad chip carriers.

UV-erasable ROMS (EPROMS) and windowless PROM parts are available. CMOS Version available with idle and power down feature and optional flatpack packages.

The operation of the Jig is controlled by the software loaded into the EPROM of the controller. To make thing as easy, the software needed is broken into many separate routines. These are:

i) Lamp Scan Routine

ii) Fuel Scan Routine

iii) Temperature Scan Routine

iv) DAC Routine

v) Spark Test Routine

vi) Counter/Timer Interrupt Routine and

vii) Delay Routines

viii) Skip and Hold Routines

The lamp scan routine starts first, according to the programmed sequence. First the break and oil indication lamps are switched ON, then the other lamps are switched sequentially. The sequence is programmed as needed by the manufacturer. The corresponding data of a sequence are outputted on the Ports/Bus. The stop routine is the interrupt routine. Whenever the interrupt occurs the processor vectorises and jumps to a particular location say 03H for INT. In the interrupt subroutine the processor does not do any work and it waits for the start key to be pressed.

The skip routine just jumps to the next function to be performed. This is sensed by the start key.

During the temperature and the fuel check the datas are outputted on the port 1 of the controller and then, the output of the decoders will activate the proper relay. The proper datas are taken from the look-up table which will be programmed earlier in the chip. These data activate the proper relay contacts. Here the look up table is stored in the third page of the controller i.e. from 300H to 3FFH.

Reed Switch or Spark test checking or speedometer checking is done by outputting digital data for an equivalent RPM through Port 2. Then the digital data is converted into Analog O/P. This will run the motor at a particular speed according to the data input. Since the speedometer cable is coupled to the motar it rotates. The reed switch also rotates and produces pulses. The pulse output of the reed switch is connected to $T_1$ input of the controller. The counter starts counting the pulses. The spark LED is made to blink while spark test is done.

**CALCULATION OF DELAY TIME:**

The number of machine cycles for a particular instruction is fixed. So a combination of many instructions will provide a particular delay. This is the principle used in the calculation of delay time for various operations. Now

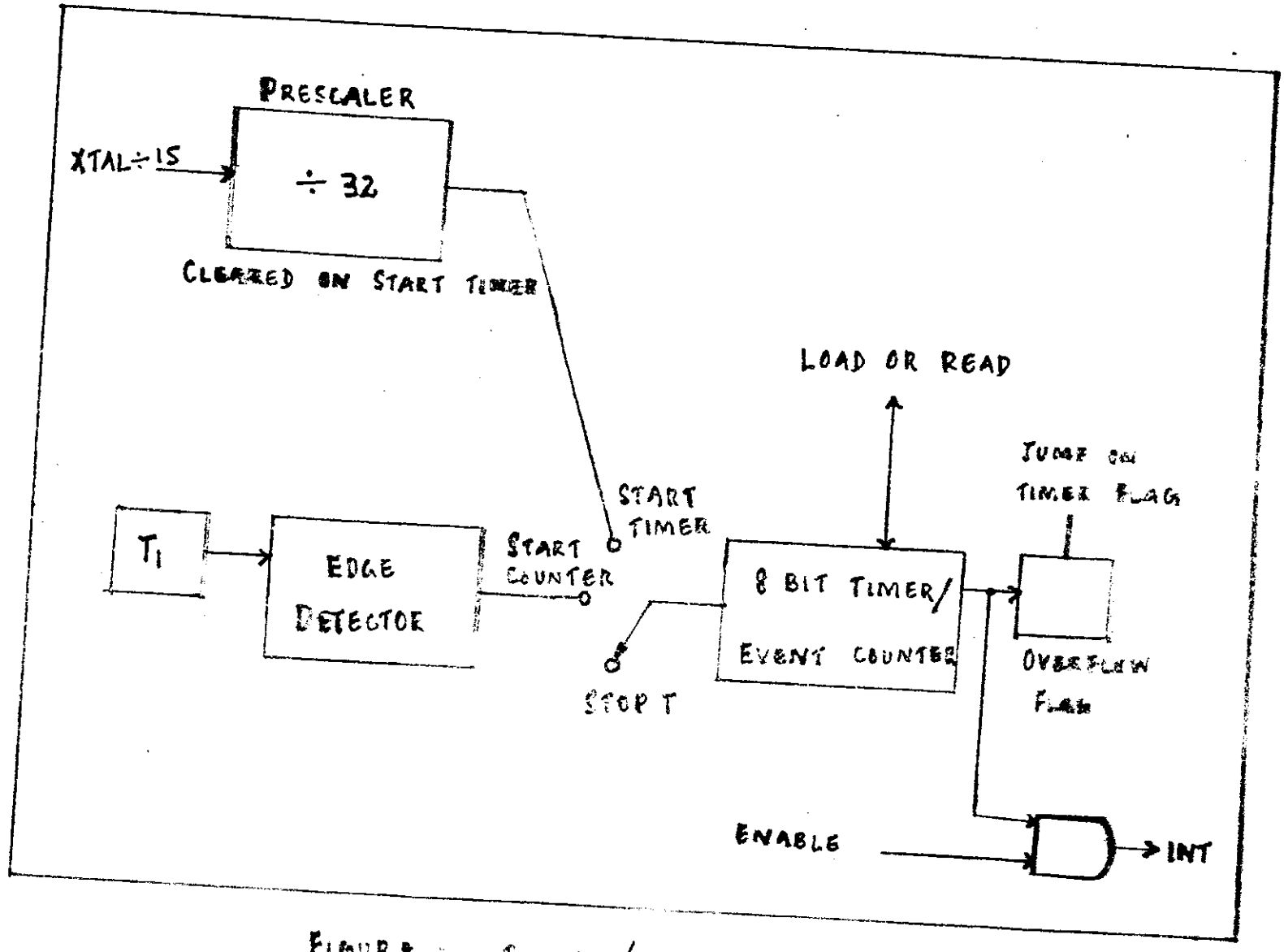
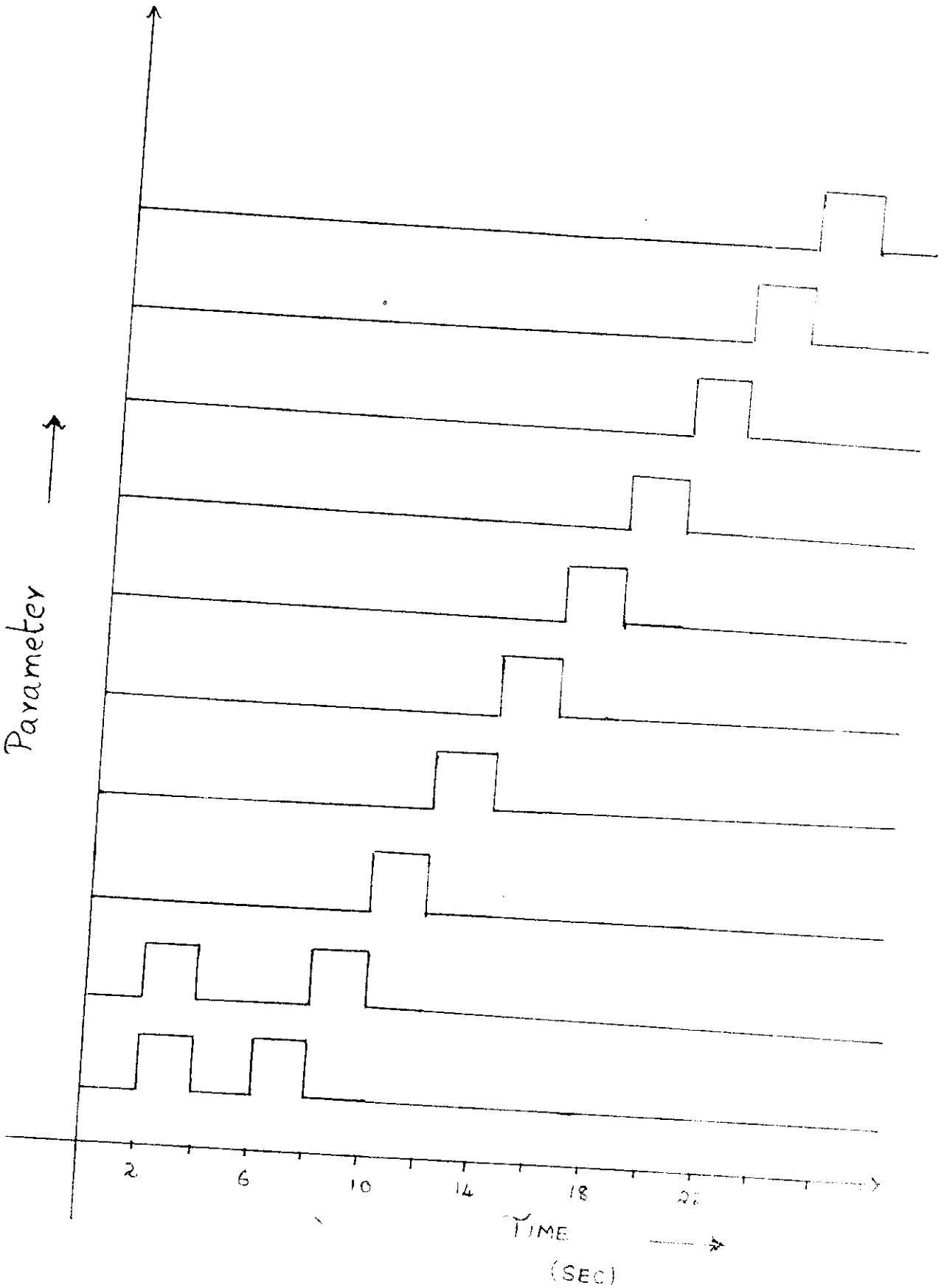
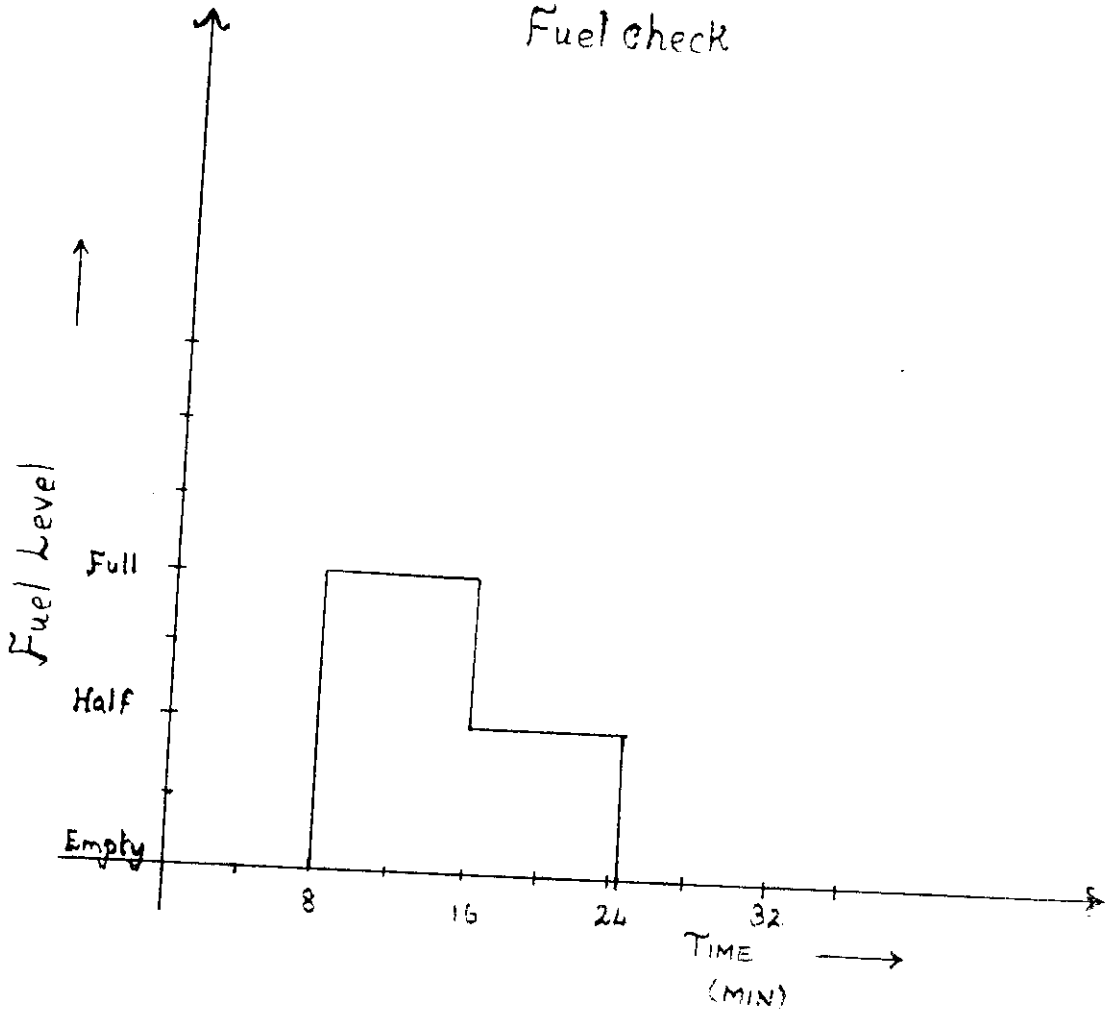



FIGURE : TIMER / EVENT COUNTER

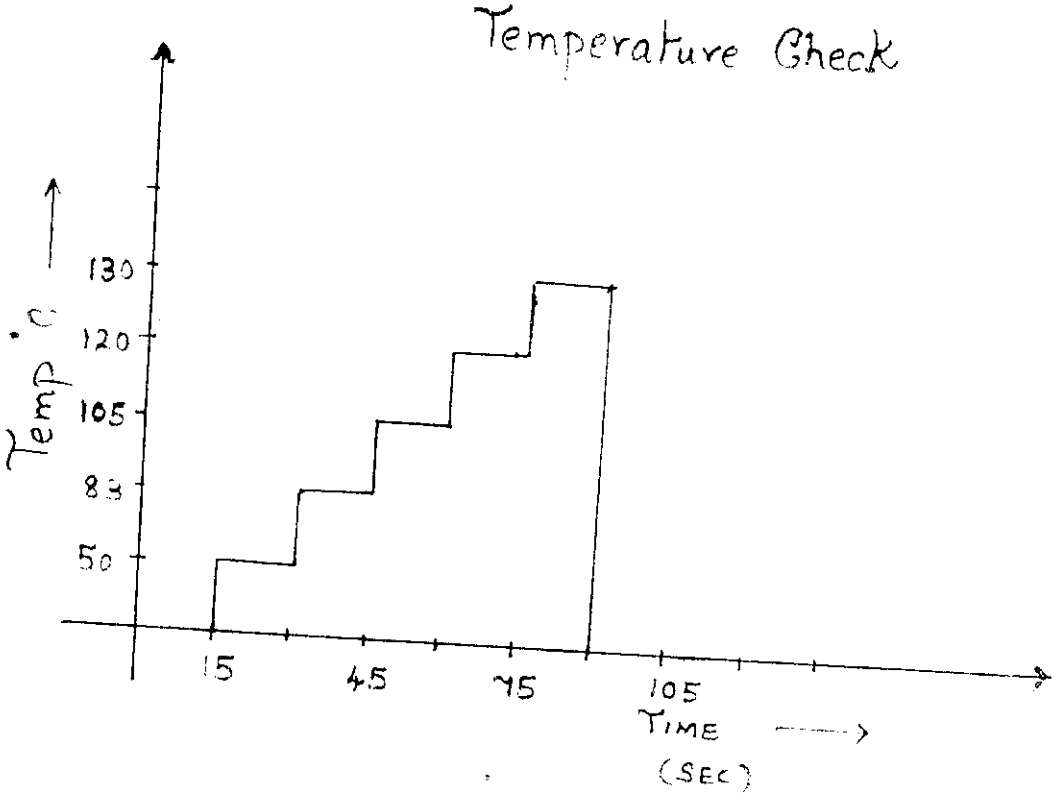
# Lamp Check



## Fuel check




## Temperature Check



if a loaded counter is decremented itself to zero it takes a particular time. Thus by adjusting the value of the Delay counter, it will be possible to get different delays. The timing diagrams for various scans is shown in figures 8 and 9.

Let a 10 MHz crystal be provided for the controller. Then the ALE frequency is given by 10 MHz + 15 (as shown in figure 7). For the timer to increment by one, it takes frequency divided by a prescaler value of 32. Thus for one increment of timer of a 10 MHz crystal it takes,

1/Time = Frequency /(15 x 32)

= 10 MHz /(15 x 32)

= 20833.33

Therefore the time required for increment of timer of a 10 MHz crystal is 48 microseconds

For a timer counter with value FF it takes -

48 x 255 = 12 milli-seconds.

for the timer counter to overflow.

Thus by counting the number of overflows and comparing it with the setvalue of time we can have different delay timings.

EXAMPLE: A practical example for having approximately 1 second delay is shown below.

Let Crystal selected = 10 MHz

1 timer count = 48 microseconds

For 0 to 255 counts of timer or for 1 overflow we have,

= 48x255microseconds

Therefore for 1 second we have = $1.224 \times 10^{-2}$ seconds

$1/(1.224 \times 10^{-2})$ = 81.69 Counts

or

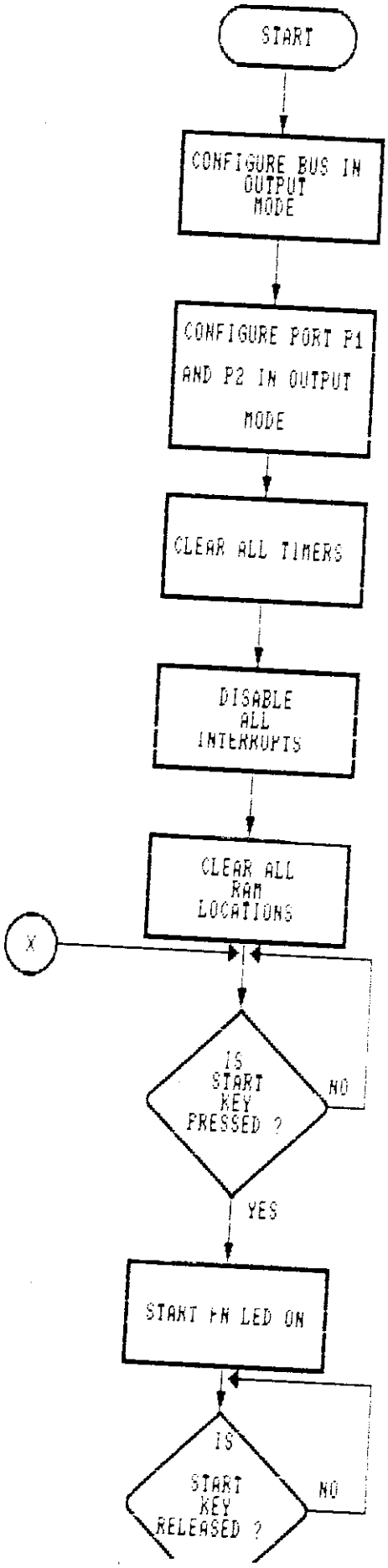
= $52_H$ Counts.

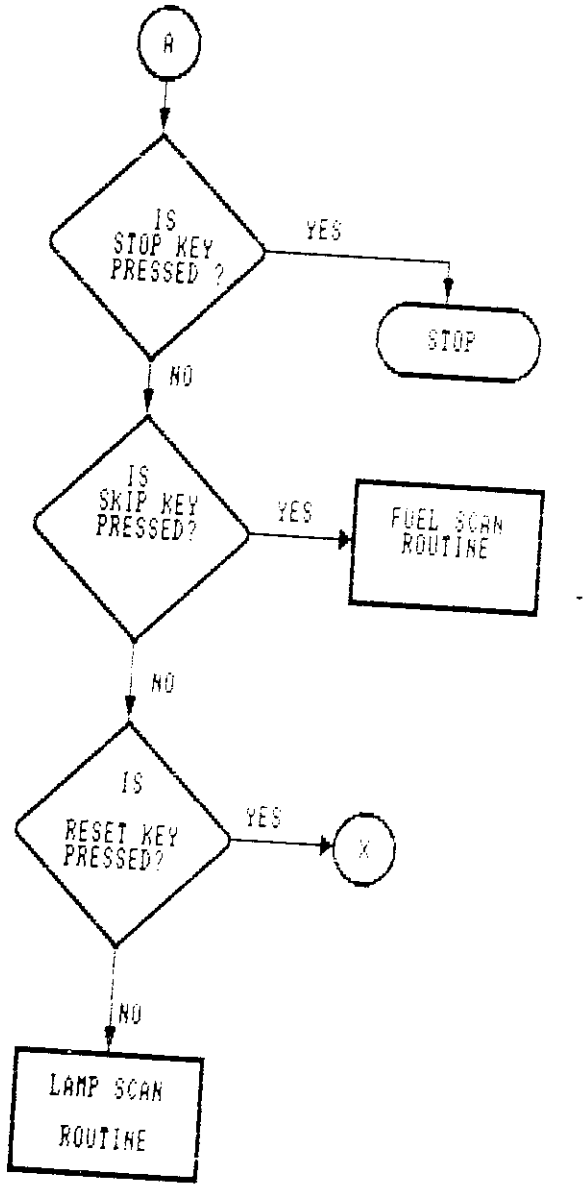
Therefore, the value of $52_H$ has to be put as a software external prescalar in the memory location.

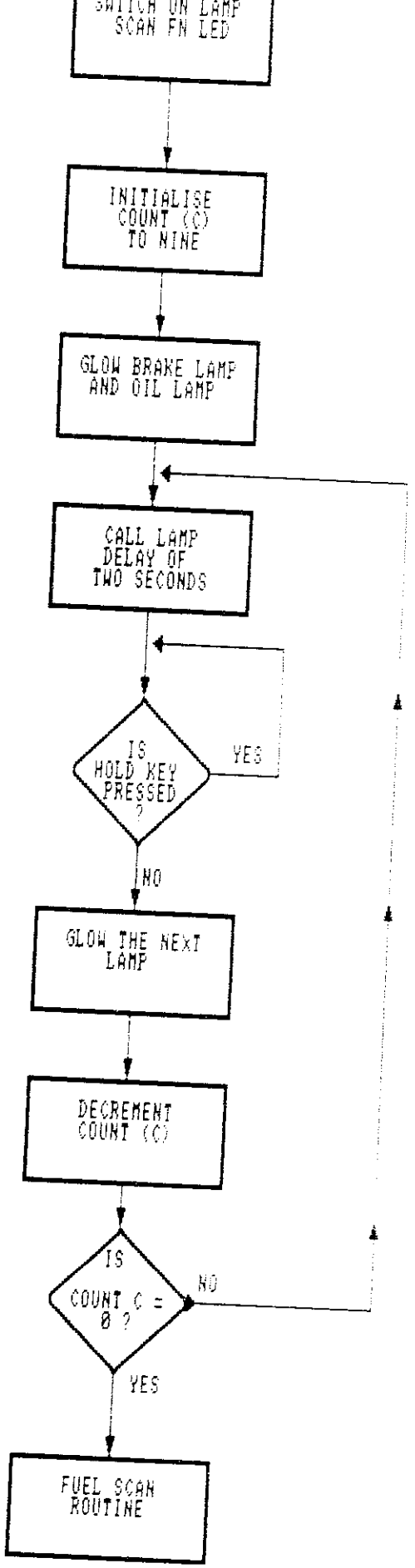
The timing changes for different crystal frequencies.

The above method is most widely used in software programs. This is called as Real time delay or Real time timer interrupt.

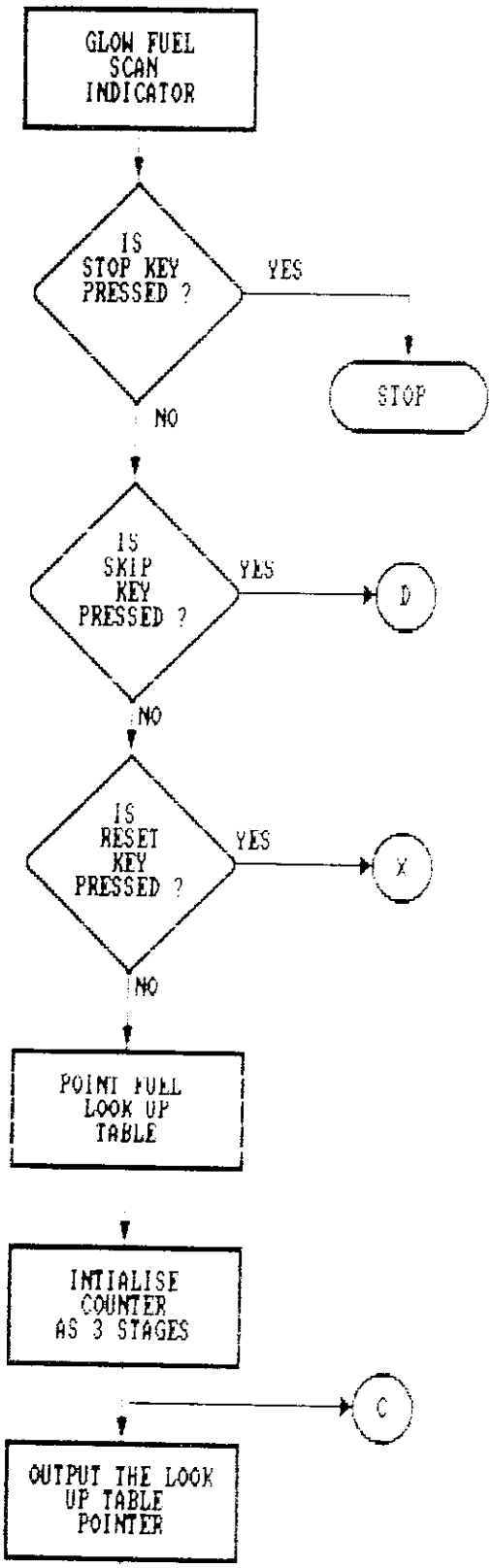
MAIN FLOW

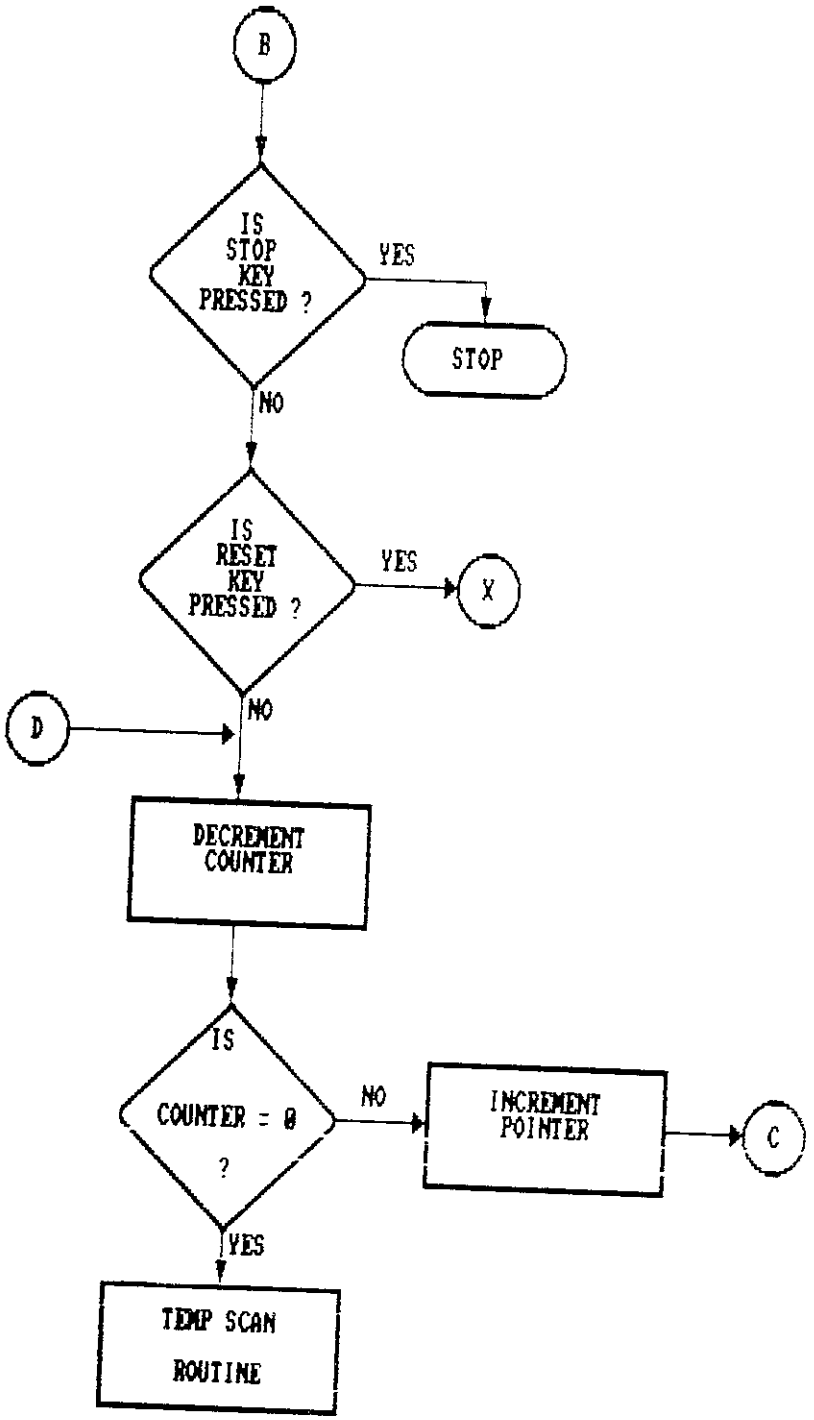

START
CONFIGURE BUS IN OUTPUT MODE
CONFIGURE PORT P1 AND P2 IN OUTPUT MODE
CLEAR ALL TIMERS
DISABLE ALL INTERRUPTS
CLEAR ALL RAM LOCATIONS
X
IS START KEY PRESSED ?
NO
YES
START FM LED ON
IS START KEY RELEASED ?
NO

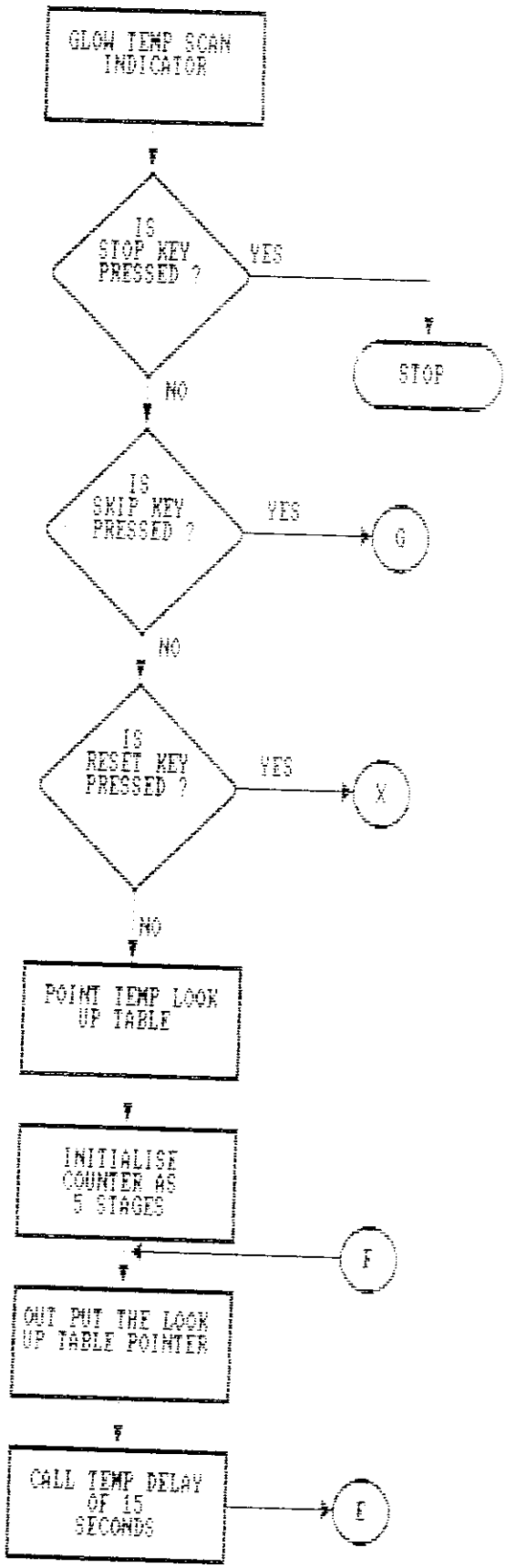

A
IS STOP KEY PRESSED ?
YES
STOP
NO
IS SKIP KEY PRESSED?
YES
FUEL SCAN ROUTINE
NO
IS RESET KEY PRESSED?
YES
X
NO
LAMP SCAN ROUTINE


SWITCH ON LAMP SCAN FN LED
INITIALISE COUNT (C) TO NINE
GLOW BRAKE LAMP AND OIL LAMP
CALL LAMP DELAY OF TWO SECONDS
IS HOLD KEY PRESSED ?
YES
NO
GLOW THE NEXT LAMP
DECREMENT COUNT (C)
IS COUNT C = 0 ?
NO
YES
FUEL SCAN ROUTINE

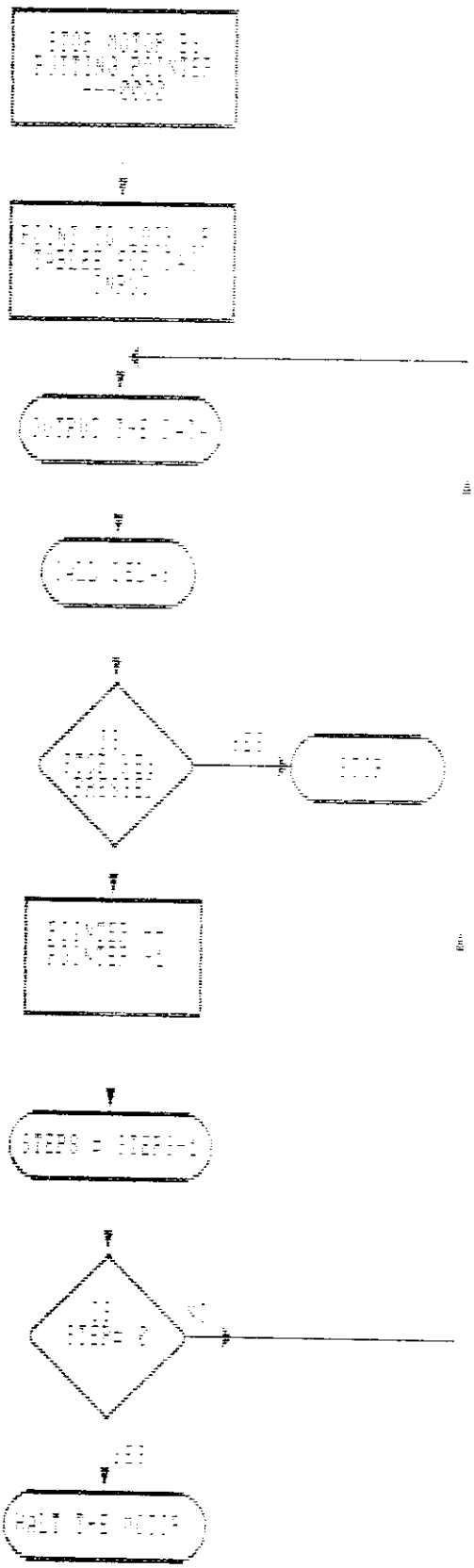
FUEL SCAN ROUTINE



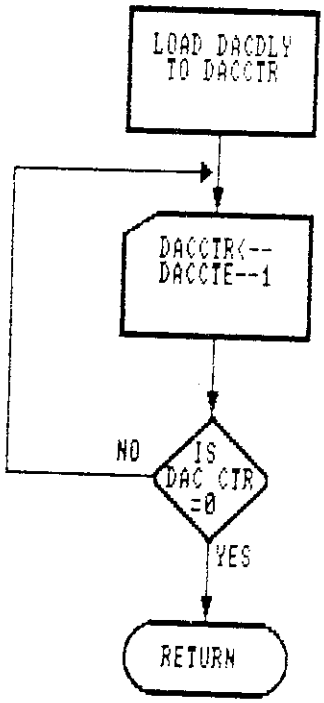

B
IS STOP KEY PRESSED ?
YES
STOP
NO
IS RESET KEY PRESSED ?
YES
X
D
NO
DECREMENT COUNTER
IS COUNTER = 0 ?
NO
INCREMENT POINTER
C
YES
TEMP SCAN ROUTINE


GLOW TEMP SCAN INDICATOR
IS STOP KEY PRESSED ?
YES
STOP
NO
IS SKIP KEY PRESSED ?
YES
G
NO
IS RESET KEY PRESSED ?
YES
X
NO
POINT TEMP LOOK UP TABLE
INITIALISE COUNTER AS 5 STAGES
F
OUT PUT THE LOOK UP TABLE POINTER
CALL TEMP DELAY OF 15 SECONDS
E

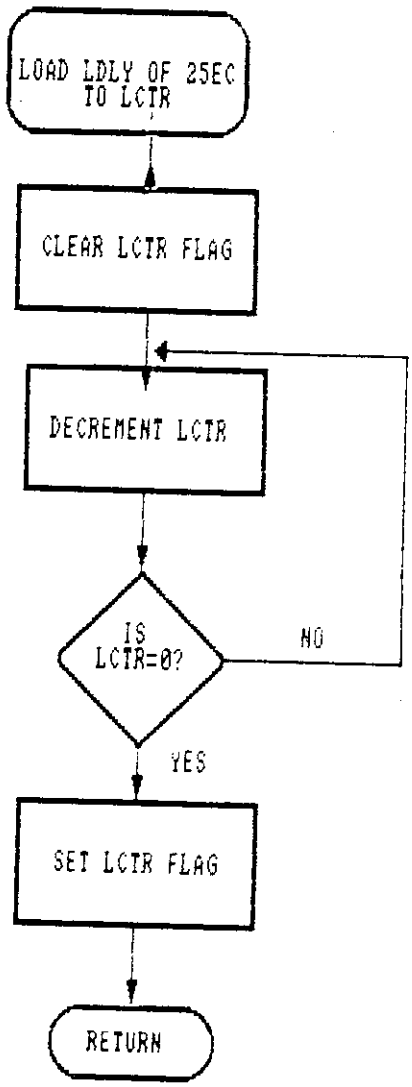
DAC ROUTINE



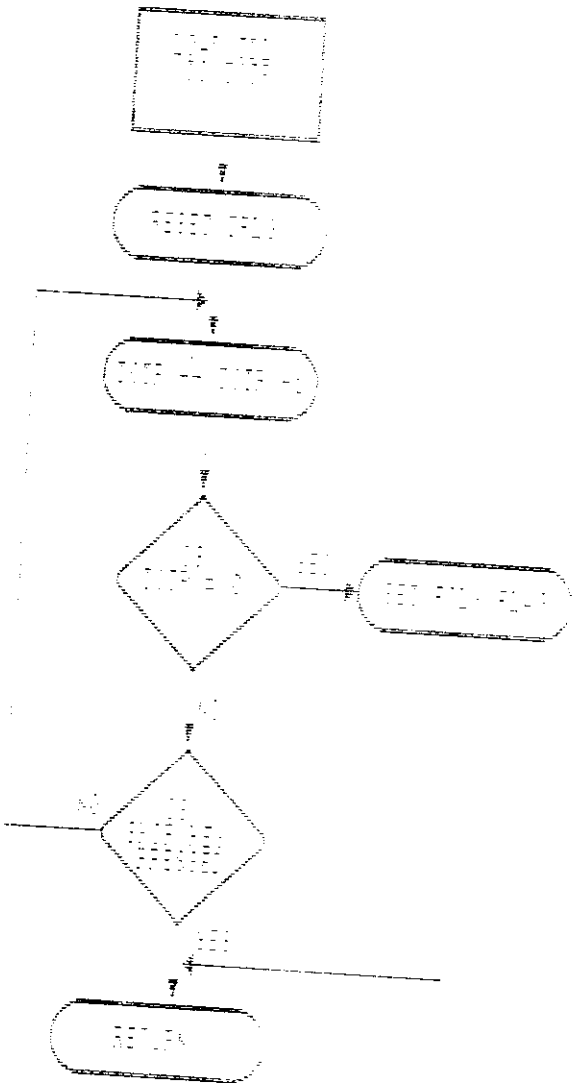
## DAC DELAY ROUTING



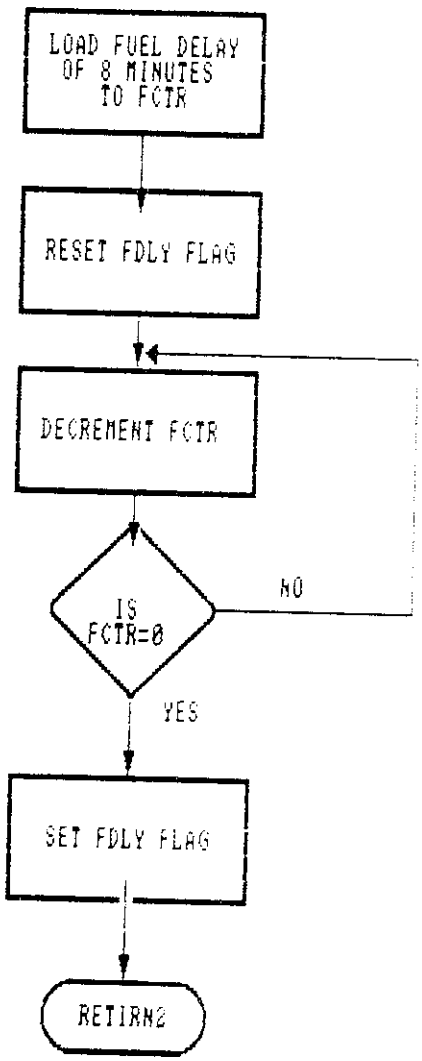
LAMP SCAN DELAY ROUTING



TEMERATURE DELAY ROUTINE



FUEL SCAN DELAY ROUTINE



```
            ;Software for test jig of YE2  combimeter
            ;FOR NIPPENDENSO  JAPAN.
            ;developed by THE STUDENTS OF KCT.
            ;started on 21 dec 93 14.00 hrs
            ;file =jig.asm
            ; !!This is for new fuel\temp data \8 min dly!!!!!!!!!!
            ;Thi is again Modified for the indication of the 8min dly
            ;This is done on the requestion of Mr RAMESH,DY MANAGER PED
;   SYSYEM EQUATES:
            ;look up table equates
            FULKTBL:  EQU 10H      ;look up table starts from here for fuel(310
            TMLKTBL:  EQU 14H      ;look up table starts from here for Temp(314

            ;counter equates
            LAMPSTG:  EQU 08H      ;Eight lamps to be scanned first and one next
            FUELSTG:  EQU 03H      ;THREE  relays of fuel scan
            TEMPSTG:  EQU 05H      ;FIVE relays of the temp scan
            DEBNCTR:  EQU 93H      ;DEBOUNCE COUNTER
;misc equates

            BLINKON:  EQU 00110000B    ;BLink the spark led
            BLINKOF:  EQU 11001111B
            DIODECK:  EQU 11101110B
            FLAG:     EQU  25H



            ;NOW THE PROGRAM BEGINS !!!!!!!!

            ORG 00h
                                  ;RESET LOC OF THE PROCESSOR
            JMP INIT

            ORG 03H

            JMP INITR

INIT:       DIS I
            DIS TCNTI
            ORL BUS,#11111111B
            ANL P1,#11110001B           ;Denergise all lamp relays
            ORL  P2,#11111111B          ;switch OFF all indicators and ON spa
            ANL  P2,#11111101B    ;de energise all temp and fuel relays
```

```
          JNT0 BEGIN1
          JMP START                ;IS STARTKEY PRESSED?
                                   ;!! no Wait there !!!!!

BEGIN1:   ANL  P2,#11111110B
          MOV  R6,#DEBNCTR
                                   ;DEBounce for some time ~~10msec~~

BEGIN2:   DJNZ R6,BEGIN2
          JT0  BEGIN
          JMP BEGIN1


BEGIN:    EN I
          ANL P1,#01001111B        ;light on the START led
          CALL LAMPSCN
          ORL  P2,#00000010B
ENTFUEL:  CALL FUEL
ENTTEMP:  CALL TEMP
          JMP  START

     ;this routine will scan 9 lamps
     ;the intesity is tested by the user manually,ie visually
     ;R6 will have the data to be put on the lamps

LAMPSCN:  MOV A,#EEH
          OUTL BUS,A               ;break.oil indication on
          CALL DLY
          MOV  R6,#11111110B       ;check for the diode of parking
          MOV R7,#LAMPSTG          ;first output of the lamp
LMLOOP1:  MOV A,R6
          OUTL BUS,A
          RL   A
          MOV R6,A
          CALL DLY
          DJNZ  R7,LMLOOP1         ;delay of appox 2 seconds
          ORL BUS,#FFH
          ANL P1,#11111110B        ;switch ON lamp 9!!!!!
          CALL DLY
          RET

          ;temp scans will be for the 5 stages
          ;datas are taken from the lookup tble
          ;the lookup table is from the third page of the memory

TEMP:     MOV R7,#05H              ;no of stages are five
          MOV R1,#TMLKTBL          ;point to the lookup tabler
LOOP4:    MOV A,R1
          MOVP3 A,@A               ;third page entry
          OUTL P1,A
```

```
                ;CHECK THE CONTENTS OF INT BFR


DLYTEMP:        SEL RB1
                MOV R7,#18H
BACK3T:         MOV R6,#FFH
BACK2T:         MOV R5,#FFH
BACK1T:         NOP
                DJNZ R5,BACK1T
                DJNZ R6,BACK2T
                DJNZ R7,BACK3T
                SEL RB0
                RET


                ORG  200H


DLYFUEL:        SEL RB1
                MOV R4,#03H
BACK4F:         MOV R7,#FFH
BACK3F:         MOV R6,#FFH
BACK2F:         MOV R5,#FFH
BACK1F:         JNT0  FUELSKP
                DJNZ R5,BACK1F
                DJNZ R6,BACK2F
                DJNZ R7,BACK3F
                DJNZ R4,BACK4F

WARNHIM:        ANL  P2,#11111110B
                ORL P1,#BLINKON
                CALL BLNKDLY
                ORL  P2,#00000001B
                CALL BLNKDLY
                MOV  R0,#FLAG
                MOV  A,@R0
                JB0  BITSET
                JMP  WARNHIM


BITSET:         MOV  R0,#FLAG
                MOV @R0,#00H
                ANL  P2,#11111110B
                JMP COMOUT


FUELSKP:        MOV  R6,#DEBNCTR
WAIT2:          DJNZ R6,WAIT2                   ;DEBounce for some time ~~10msec~~
```

```
WAIT3:    JT0   COMOUT                ;SEnse THE FALLing edge
          JMP WAIT3
COMOUT:   SEL RB0
          RET


BLNKDLY:  MOV R5,#99H
BLKLOOP2: MOV R6,#FFH
BLKLOOP1: JNT0    STGSKIP
          DJNZ    R6,BLKLOOP1
          DJNZ    R5,BLKLOOP2
          RET


STGSKIP:  MOV   R6,#DEBNCTR           ;DEBounce for some time ~~10msec~~
WAIT4:    DJNZ R6,WAIT4
WAIT5:    JT0   SKIPOUT               ;SEnse THE FALLing edge
          JMP WAIT5

SKIPOUT:  MOV R0,#FLAG
          MOV   @R0,#01H
          RET


          ORG   310H
          DB   6FH,6DH,6BH,
          ORG   314H
          DB    51H,53H,55H,57H,59H,

WAITDLY:      SEL     RB1
              MOV     R4,#01H
WAIT4:        MOV     R7,#FFH
WAIT3:        MOV     R6,#FFH
WAIT2:        MOV     R5,#FFH
WAIT1:        JT0     SKIP_WT
              DJNZ    R5,WAIT1
              DJNZ    R6,WAIT2
              DJNZ    R7,WAIT3
              DJNZ    R4,WAIT4
              SEL     RB0
              MOV     R0,#CURRAM
              CALL    ADD_03
              MOV     R0,#TEARAM
```

```
                CALL    ADD_03
SKIP_WT:        SEL     RB0                                              81
                RET
REPWR:          JTO     BEGINPD
                ANL     P2 ,#11111000B
                ORL     P2 ,#00000001B          ;CLK,CS,DI low
                ORL     P2 ,#00000010B          ;CS high
                ANL     P2 ,#11111011B          ;Clk L->H, to issue the
                                                ;dummy clk after chip select

                MOV     R3 ,#10000000B          ;Program ENable (PEN) opcode
                MOV     R2 ,#03                 ;write only 5bits, from DB7
                CALL    WRITE
                MOV     R3 ,#11000000B                  ;PEA - 2nd byte wr;
                MOV     R2 ,#06
                CALL    WRITE

                ANL     P2,#11110110B
                ORL     P2,#01

                MOV     R3 ,#10100000B
                MOV     R2 ,#03                         ;NV RAM's op code to
                CALL    WRITE                   ;write -
                MOV     A  ,R5
                MOV     R3 ,A
                MOV     R2 ,#6                  ;start storing from 1st loc
                CALL    WRITE                   ;6 bit address
                MOV     A  ,@R1
                MOV     R3 ,A                   ;get data to be stored
                MOV     R2 ,#8
                CALL    WRITE
                INC     R1                      ;storing 1st byte
                MOV     A  ,@R1
                MOV     R3 ,A
                MOV     R2 ,#8                  ;storing 2nd byte
                CALL    WRITE
                ANL     P2,#11110110B   ;**************

                CALL    DY10MS
                INC     R1                      ;wait for 10mS/check BUSY pi
                MOV     A  ,R5                  ;increment RAM pointer
                ADD     A,  #4
                MOV     R5 ,A                   ;increment the MSBits of NV
                DJNZ    R4 ,REPWR1              ;address
                RET                             ;write all bytes
REPWR1:         JMP REPWR

;[[[[ if required for calibration only !!!!!!!!!

;Delay for 10 m sec,
```

```
          CALL DLYTEMP                ;dly for the 15 seconds
          INC R1
          DJNZ R7,LOOP4               ;count =count-1
          MOV A,#C1H
          OUTL P1,A
          RET

          ;FUEL SCAN FOR 3 RELAYS
          ;this cheks the stages for the fuel guages

FUEL:     MOV A,#FFH
          OUTL BUS,A
          MOV R7,#03H
          MOV R1,#FULKTBL
LOOP5:    MOV A,R1
          MOVP3 A,@A
          OUTL P1,A
          CALL DLYFUEL
          INC  R1
          DJNZ R7,LOOP5
          RET

          ;IF INT HAS OCCURED RESET ,STOP & WAIT

INITR:    ANL P1,#10111111B
          JNT0  BEGIN1
          JMP INITR
          ;DELAY FOR SCAN

DLY:      SEL RB1
          MOV R7,#03H
BACK3:    MOV R6,#FFH
BACK2:    MOV R5,#FFH
BACK1:    JNT0  INDEFWT
          DJNZ R5,BACK1
          DJNZ R6,BACK2
          DJNZ R7,BACK3
          SEL RB0
          RET


INDEFWT:  MOV  R6,#FFH
BEGIN20:  DJNZ R6,BEGIN20
          JNT0   INDEFWT
          SEL    RB0
          RET
```

```
DYTOMBTBBL:
        MOV     R4,#TB.
D100:   MOV     R0,#OFFH
D101:   DJNZ    R0,D101
        DJNZ    R4,D100
        SEL     RB0
```

The utility value of the Jig is enhanced to a great extent if it could be operated by an ordinary worker.

One of the things which puzzles and confuses many people when they first come across automatic testing system is the operating procedure for such systems. This section will be very helpful to overcome this handicap.

## 5.1. PROCEDURE FOR OPERATING THE JIG

1. **Getting Started:**

Before switching ON the power supply, insert the connector of the Jig into the socket found in the back of the cluster. Ensure that they fit in properly.

2. Switch on the power supply. Now the Power ON LED will start glowing.

3. When you want to start the checking of the cluster, press the Start switch.

NOTE: Your start switch is also the sensing element for SKIP FUNCTION, which provides facilities like skipping of any stage of the check or the stage itself, so, ensure that the start key is pressed only once. Pressing of the start key twice or more may lead to skipping of lamp and fuel check stages. This may not be the intention of the user.

the position of the needle at various time intervals. The pressing of start key thrice will skip the fuel check and, temperature check is started. If any fault is observed stop the check and switch OFF power supply, before removing the cluster.

6. **Temperature Check:**

The temperature check is the last check and the observer should monitor carefully the needle position at the given time intervals. The time interval is very short and hence it calls for greater care during monitoring of temperature check. During temperature check the reset key acts as a sensing element for the stop funciton (i.e.) the system is brought to initial conditions when reset key is pressed and it is ready for checking of lamps again.

7. Spark test, if necessary is done after the temperature check. The spark LED glows when the working condition of the reed switch is satisfactory.

## 5.2. KEYS AND THEIR FUNCTIONS:

| KEYS | WHEN PRESSED | FUNCTION |
|---|---|---|
| START KEY | ONCE | STARTS THE OPERATION OF THE SYSTEM |
| START KEY | TWICE | SKIPS LAMP CHECK |
| START KEY | FIVE TIMES | SKIPS LAMP AND TEMPERATURE |
| STOP KEY | ONCE | WILL STOP THE OPERATION OF THE SYSTEM |
| STOP KEY | PRESSING ONCE AND i) NOT RELEASING ii) WHEN RELEASED | WILL SERVE HOLD FUNCTION<br>HOLD IS DISCONTINUED AND NORMAL SEQUENCE OF OPERATION IS CONTINUED |
| RESET KEY | ONCE DURING ANY CHECK | WILL RESET THE SYSTEM |
| | ONCE DURING TEMPERATURE CHECK | WILL SKIP TEMPERATURE CHECK |

**Recommendations:**

i) While monitoring the lamp check switch OFF the lights in the room and make the room

dark, so that intensity of lamps can be properly seen.

ii) During temperature and fuel check, switch ON the lights and ventilate the room, so that the user can comfortably observe the needle deflections.

iii) Use high quality and precision function stop clocks to observe timing intervals.

## 5. CONCLUSION:

The project was carried out at Pricol, Coimbatore succeessfully. All necessary specifications for checking of the cluster, as provided by the manufacturer were successfully met.

There were some minor problems, during the checking of lamps. We found that the relays used to switch ON and OFF itself intermediately. When analysed we found that the relay was chattering. By connecting a diode across the relay coil, we overcame this problem.

Stray lead capacitance effects caused changes in crystal frequency and the processor was made to hang. To overcome this, we added a very low capacitance of 20 pico-farads between ground and crystal points.

This project was very much helpful in automatic checking of the clusters at a faster rate. It employs a wide range of user friendly operation procedures like skipping facilities of any stage of the check or the stage itself. It also provides a hold function, with the help of which the operator may monitor a specific operation to his fullest satisfaction and may again continue with the normal sequence of checking.

The project has wide application not only in checking of clusters, but can also be used as timers.

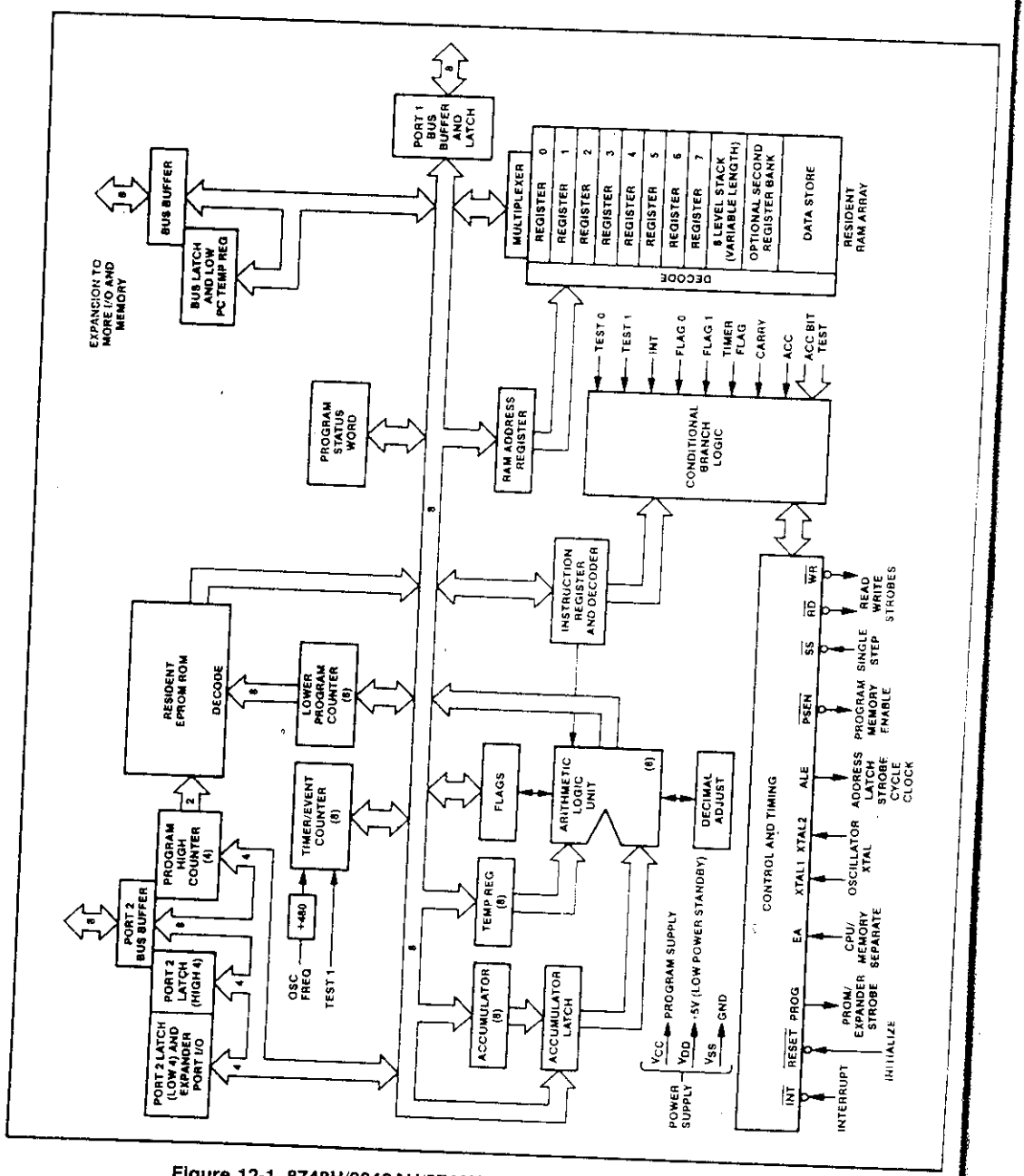



**Figure 12-1. 8748H/8048AH/8749H/8049AH/8050AH Block Diagram**

## Table 2. Instruction Set

**Accumulator**

| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| ADD A, R | Add register to A | 1 | 1 |
| ADD A, @R | Add data memory to A | 1 | 1 |
| ADD A, # data | Add immediate to A | 2 | 2 |
| ADDC A, R | Add register with carry | 1 | 1 |
| ADDC A, @R | Add data memory with carry | 1 | 1 |
| ADDC A, # data | Add immediate with carry | 2 | 2 |
| ANL A, R | And register to A | 1 | 1 |
| ANL A, @R | And data memory to A | 1 | 1 |
| ANL A, # data | And immediate to A | 2 | 2 |
| ORL A, R | Or register to A | 1 | 1 |
| ORL A @R | Or data memory to A | 1 | 1 |
| ORL A, # data | Or immediate to A | 2 | 2 |
| XRL A, R | Exclusive or register to A | 1 | 1 |
| XRL A, @R | Exclusive or data memory to A | 1 | 1 |
| XRL, A, # data | Exclusive or immediate to A | 2 | 2 |
| INC A | Increment A | 1 | 1 |
| DEC A | Decrement A | 1 | 1 |
| CLR A | Clear A | 1 | 1 |
| CPL A | Complement A | 1 | 1 |
| DA A | Decimal adjust A | 1 | 1 |
| SWAP A | Swap nibbles of A | 1 | 1 |
| RL A | Rotate A left | 1 | 1 |
| RLC A | Rotate A left through carry | 1 | 1 |
| RR A | Rotate A right | 1 | 1 |
| RRC A | Rotate A right through carry | 1 | 1 |

**Input/Output**

| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| IN A, P | Input port to A | 1 | 2 |
| OUTL P, A | Output A to port | 1 | 2 |
| ANL P, # data | And immediate to port | 2 | 2 |
| ORL P, # data | Or immediate to port | 2 | 2 |
| INS A, BUS | Input BUS to A | 1 | 2 |
| OUTL BUS, A | Output A to BUS | 1 | 2 |
| ANL BUS, # data | And immediate to BUS | 2 | 2 |
| ORL BUS, # data | Or immediate to BUS | 2 | 2 |
| MOVD A, P | Input expander port to A | 1 | 2 |
| MOVD P, A | Output A to expander port | 1 | 2 |
| ANLD P, A | And A to expander port | 1 | 2 |
| ORLD P, A | Or A to expander port | 1 | 2 |

**Registers**

| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| INC R | Increment register | 1 | 1 |
| INC @R | Increment data memory | 1 | 1 |
| DEC R | Decrement register | 1 | 1 |

**Branch**

| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| JMP addr | Jump unconditional | 2 | 2 |
| JMPP @A | Jump indirect | 1 | 2 |
| DJNZ R, addr | Decrement register and skip | 2 | 2 |
| JC addr | Jump on carry = 1 | 2 | 2 |
| JNC addr | Jump on carry = 0 | 2 | 2 |
| JZ addr | Jump on A zero | 2 | 2 |
| JNZ addr | Jump on A not zero | 2 | 2 |
| JT0 addr | Jump on T0 = 1 | 2 | 2 |
| JNT0 addr | Jump on T0 = 0 | 2 | 2 |
| JT1 addr | Jump on T1 = 1 | 2 | 2 |
| JNT1 addr | Jump on T1 = 0 | 2 | 2 |
| JF0 addr | Jump on F0 = 1 | 2 | 2 |
| JF1 addr | Jump on F1 = 1 | 2 | 2 |
| JTF addr | Jump on timer flag | 2 | 2 |
| JNI addr | Jump on INT = 0 | 2 | 2 |
| JBb addr | Jump on accumulator bit | 2 | 2 |

**Subroutine**

| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| CALL addr | Jump to subroutine | 2 | 2 |
| RET | Return | 1 | 2 |
| RETR | Return and restore status | 1 | 2 |

**Flags**

| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| CLR C | Clear carry | 1 | 1 |
| CPL C | Complement carry | 1 | 1 |
| CLR F0 | Clear flag 0 | 1 | 1 |
| CPL F0 | Complement flag 0 | 1 | 1 |
| CLR F1 | Clear flag 1 | 1 | 1 |
| CPL F1 | Complement flag 1 | 1 | 1 |

Table 2. Instruction Set (Continued)

**Data Moves**

| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| MOV A, R | Move register to A | 1 | 1 |
| MOV A, @R | Move data memory to A | 1 | 1 |
| MOV A, # data | Move immediate to A | 2 | 2 |
| MOV R, A | Move A to register | 1 | 1 |
| MOV @R, A | Move A to data memory | 1 | 1 |
| MOV R, # data | Move immediate to register | 2 | 2 |
| MOV @R, # data | Move immediate to data memory | 2 | 2 |
| MOV A, PSW | Move PSW to A | 1 | 1 |
| MOV PSW, A | Move A to PSW | 1 | 1 |
| XCH A, R | Exchange A and register | 1 | 1 |
| XCH A, @R | Exchange A and data memory | 1 | 1 |
| XCHD A, @R | Exchange nibble of A and register | 1 | 1 |
| MOVX A, @R | Move external data memory to A | 1 | 2 |
| MOVX @R, A | Move A to external data memory | 1 | 2 |
| MOVP A, @A | Move to A from current page | 1 | 2 |
| MOVP3 A, @A | Move to A from page 3 | 1 | 2 |

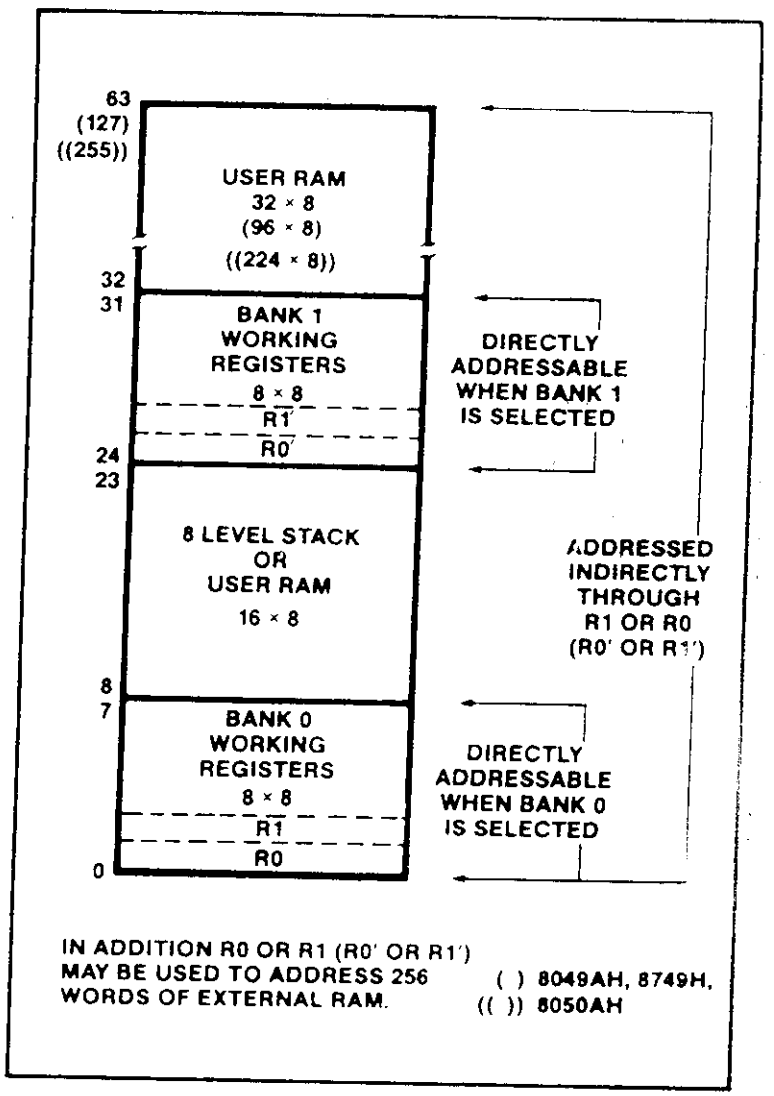
**Timer/Counter**

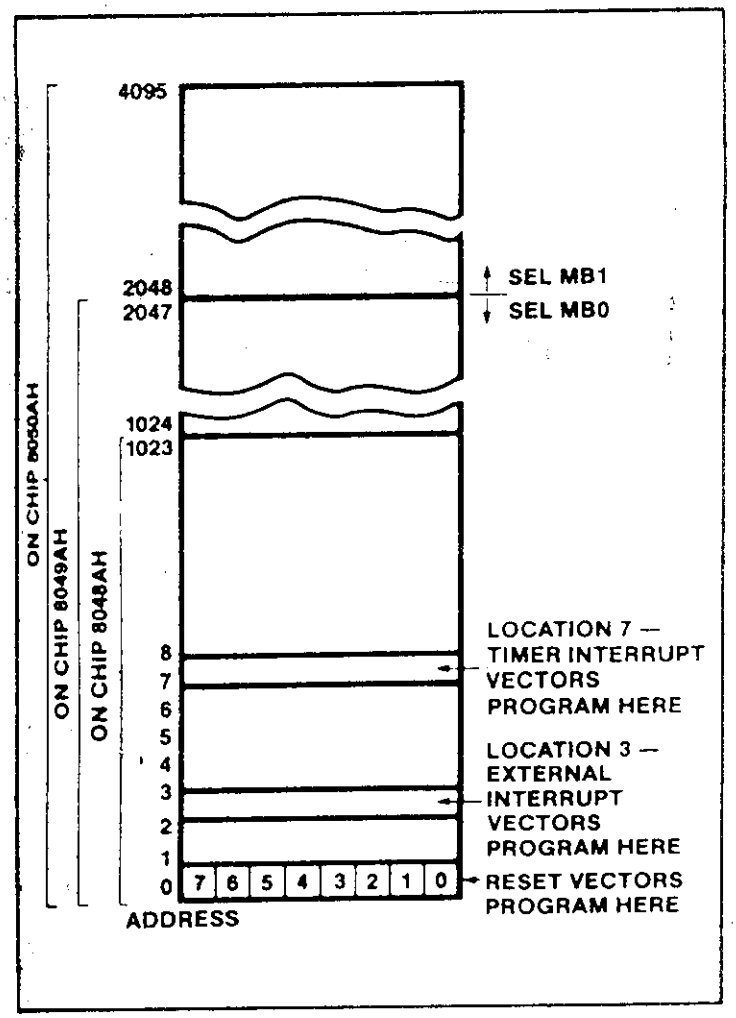
| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| MOV A, T | Read timer/counter | 1 | 1 |
| MOV T, A | Load timer/counter | 1 | 1 |
| STRT T | Start timer | 1 | 1 |
| STRT CNT | Start counter | 1 | 1 |
| STOP TCNT | Stop timer/counter | 1 | 1 |
| EN TCNTI | Enable timer/counter interrupt | 1 | 1 |
| DIS TCNTI | Disable timer/counter interrupt | 1 | 1 |

**Control**

| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| EN I | Enable external interrupt | 1 | 1 |
| DIS I | Disable external interrupt | 1 | 1 |
| SEL RB0 | Select register bank 0 | 1 | 1 |
| SEL RB1 | Select register bank 1 | 1 | 1 |
| SEL MB0 | Select memory bank 0 | 1 | 1 |
| SEL MB1 | Select memory bank 1 | 1 | 1 |
| ENT0 CLK | Enable clock output on T0 | 1 | 1 |

| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| NOP | No operation | 1 | 1 |


63
(127)
((255))
USER RAM
32 × 8
(96 × 8)
((224 × 8))
32
31
BANK 1
WORKING
REGISTERS
8 × 8
R1'
R0'
24
23
8 LEVEL STACK
OR
USER RAM
16 × 8
8
7
BANK 0
WORKING
REGISTERS
8 × 8
R1
R0
0
DIRECTLY
ADDRESSABLE
WHEN BANK 1
IS SELECTED
ADDRESSED
INDIRECTLY
THROUGH
R1 OR R0
(R0' OR R1')
DIRECTLY
ADDRESSABLE
WHEN BANK 0
IS SELECTED
IN ADDITION R0 OR R1 (R0' OR R1')
MAY BE USED TO ADDRESS 256
WORDS OF EXTERNAL RAM.
( ) 8049AH, 8749H,
(( )) 8050AH


ON CHIP 8050AH
ON CHIP 8049AH
ON CHIP 8048AH
4095
2048
2047
1024
1023
8
7
6
5
4
3
2
1
0
7 6 5 4 3 2 1 0
ADDRESS
SEL MB1
SEL MB0
LOCATION 7 — TIMER INTERRUPT VECTORS PROGRAM HERE
LOCATION 3 — EXTERNAL INTERRUPT VECTORS PROGRAM HERE
RESET VECTORS PROGRAM HERE

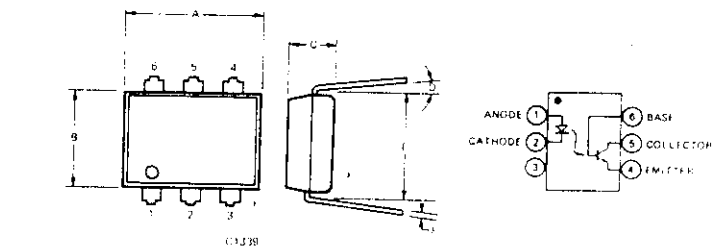
**GENERAL INSTRUMENT**
**Optoelectronics**

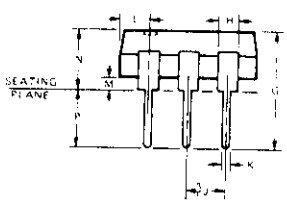
# MCT2E
## PHOTOTRANSISTOR OPTOISOLATOR

### PRODUCT DESCRIPTION

The MCT2E is a NPN silicon planar phototransistor optically coupled to a gallium arsenide diode. It is mounted in a six-lead plastic DIP package.

### PACKAGE DIMENSIONS




| SYMBOL | INCH MAX. | MM MAX. | NOTES |
|---|---|---|---|
| A | .365 | 9.27 | |
| B | .270 | 6.73 | |
| C | .120 | 3.18 | |
| D | .15 | 1.5 | |
| E | 300 Ref. | 7.62 Ref. | |
| F | .014 | 0.36 | |
| G | .325 | 8.26 | |
| H | .070 | 1.78 | |
| J | .110 | 2.79 | |
| K | .022 | 0.56 | |
| L | .085 | 2.16 | 2 |
| M | | | 3 |
| N | .175 | 4.45 | 4 |
| P | | | 3 |

PACKAGE MATERIALS
Leads Tinned with 60-40 tin-lead
Body Silicone plastic

NOTES
1. Installed position of lead centers.
2. Four places.
3. Overall installed position.
4. These measurements are made from the seating plane.

### APPLICATIONS

- Utility/economy isolator
- AC line/digital logic isolator
- Digital logic/digital logic isolator
- Telephone/telegraph line receiver
- Twisted pair line receiver
- High frequency power supply feedback control
- Relay contact monitor
- Power supply monitor
- UL Approved Product File E50151

### ABSOLUTE MAXIMUM RATINGS

Storage temperature −55°C to 150°C
Operating temperature −55°C to 100°C
Lead temperature (Soldering, 10 sec) 260°C

Input Diode
- Forward current . . . . . 60 mA
- Reverse voltage . . . . . 3.0 V
- Peak forward current (1 μs pulse, 300 pps) . . . . . 3.0 A
- Power dissipation at 25°C ambient . . . . 200 mW
- Derate linearly from 25°C . . . . . .2.6 mW/°C

Output Transistor
- Power dissipation at 25°C ambient . . . . .200 mW
- Derate linearly from 25°C . . . . . .2.6 mW/°C
- Isolation rating . . . . . 3550 VDC

Total package power dissipation at 25°C ambient (LED plus detector) .250 mW
Derate linearly from 25°C . . . . .3.3 mW/°C
Collector-Emitter Current ($I_{CE}$) . . . . . 50 mA

### ELECTRO-OPTICAL CHARACTERISTICS (25°C Free Air Temperature Unless Otherwise Specified)

| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Input Diode | | | | | | |
| Forward Voltage | $V_F$ | | 1.25 | 1.50 | V | $I_F$ = 20 mA |
| Reverse Breakdown Voltage | $BV_R$ | 3.0 | 25 | | V | $I_R$ = 10 μA |
| Junction Capacitance | $C_J$ | | 50 | | pF | $V_F$ = 0 V |
| Reverse Leakage Current | $I_R$ | | 0.1 | 10 | μA | $V_R$ = 3.0 V |
| Output Transistor | | | | | | |
| DC Forward Current Gain | $h_{FE}$ | 100 | 250 | | | $V_{CE}$ = 5 V, $I_F$ = 500 μA |
| Collector To Emitter Breakdown Volt. | $BV_{CEO}$ | 30 | 80 | | V | $I_C$ = 1.0 mA, $I_F$ = 0 |
| Collector To Base Breakdown Voltage | $BV_{CBO}$ | 70 | 165 | | V | $I_C$ = 10 μA |
| Emitter to Collector Breakdown Voltage | $BV_{ECO}$ | 7 | 14 | | V | $I_E$ = 100 μA, $I_F$ = 0 |
| Collector To Emitter, Leakage Current | $I_{CEO}$ | | 5 | 50 | nA | $V_{CE}$ = 10 V, $I_F$ = 0 |
| Collector To Base Leakage Current | $I_{CBO}$ | | 0.1 | 20 | nA | $V_{CB}$ = 10 V, $I_E$ = 0 |

## TYPICAL ELECTRO-OPTICAL CHARACTERISTIC CURVES

(25°C Free Air Temperature Unless Otherwise Specified)

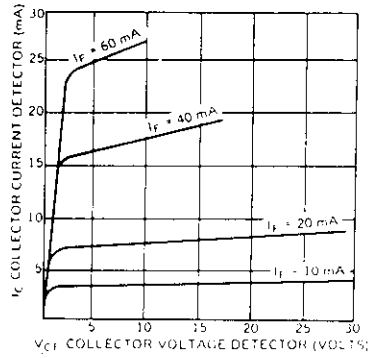



*Fig. 1 Collector Current vs. Collector Voltage (for Typical CTR 30%)*

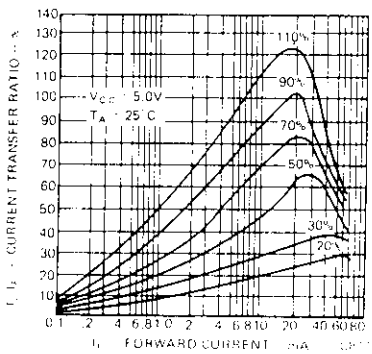



*Fig. 2 Current Transfer Ratio vs. Forward Current*

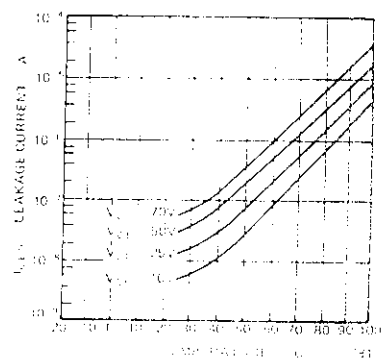



*Fig. 3 Dark Current vs. Temperature*

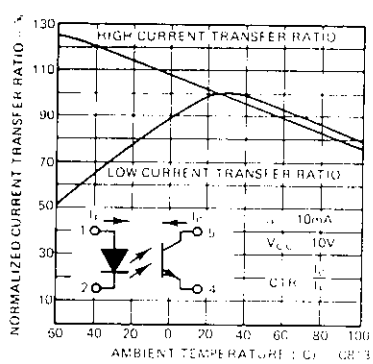



*Fig. 4 Current Transfer Ratio vs. Temperature*

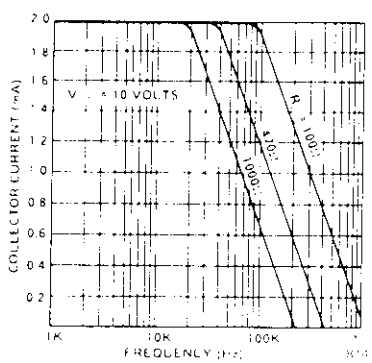



*Fig. 5 Collector Current vs. Frequency*

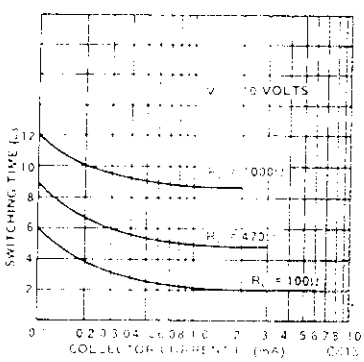



*Fig. 6 Switching Time vs. Collector Current*

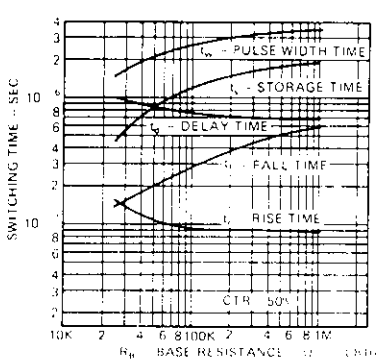



*Fig. 7 Switching Time vs. Base Resistance*

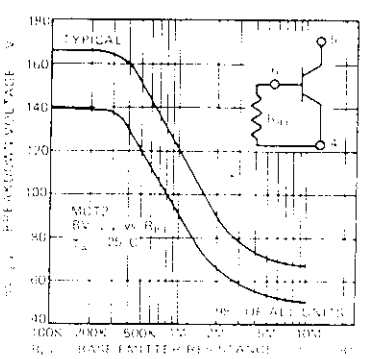



*Fig. 8 Collector – Emitter Breakdown Voltage vs. Base Resistance*

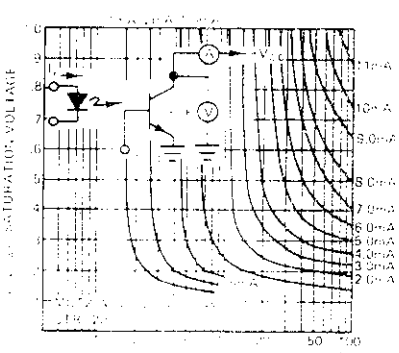



*Fig. 9 Saturation Voltage vs. Forward Current*

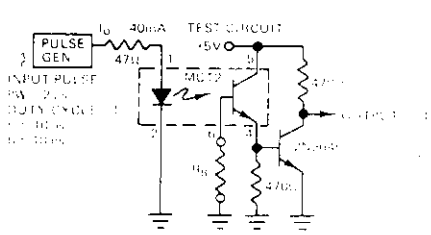



*Fig. 10 Circuit for Figure 7*

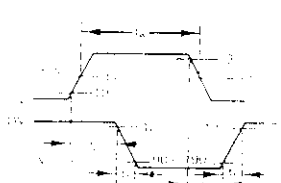
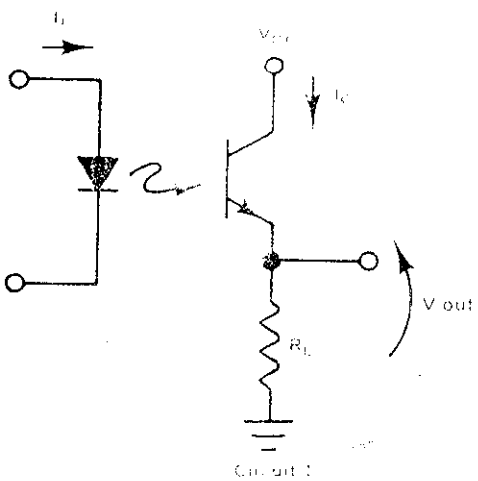


*Fig. 11 Waveforms for Figure 7*

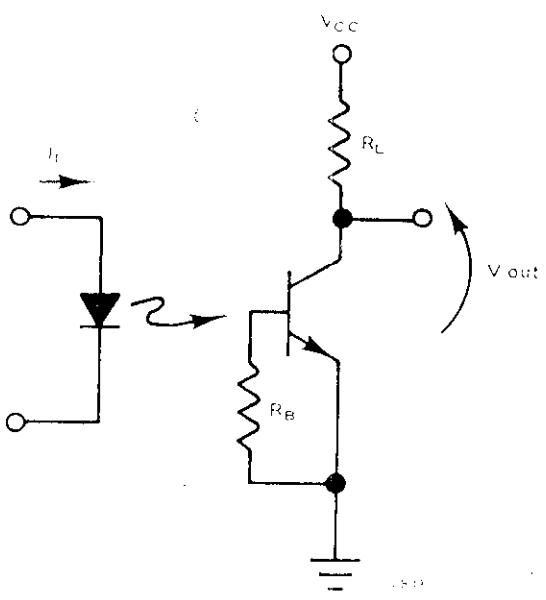
## ELECTRO-OPTICAL CHARACTERISTICS (25°C Free Air Temperature Unless Otherwise Specified)

| CHARACTERISTIC | SYMBOL | GUAR MIN. | TYP. | GUAR MAX. | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Capacitance Collector to Emitter | $C_{CE}$ | | 8 | | pf | $V_{CE}$ = 0 |
| Capacitance Collector to Base | $C_{CB}$ | | 20 | | pf | $V_{CB}$ = 10 V |
| Capacitance Emitter to Base | $C_{EB}$ | | 30 | | pf | $V_{BE}$ = 0 |
| **Coupled** | | | | | | |
| DC Collector Current Transfer Ratio | $I_C/I_F$ | 20 | 60 | | % | $V_{CE}$ = 10 V, $I_F$ = 10 mA, Note 1 |
| DC Base Current Transfer Ratio | $I_B/I_F$ | | .35 | | % | $V_{CB}$ = 10 V, $I_F$ = 10 mA |
| Surge Isolation | $V_{ISO}$ | 3550 | | | VDC | Relative humidity ≤ 50%<br>$T_A$ = +25°C, $I_{I-O}$ ≤ 10 μA |
| | | 2500 | | | VAC-rms | 1 second |
| Steady state Isolation | $V_{ISO}$ | 3150 | | | VDC | Relative humidity ≤ 50%,<br>$T_A$ = +25°C, $I_{I-O}$ ≤ 10 μA |
| | | 2250 | | | VAC-rms | 1 minute |
| Isolation Voltage | | 2500 | | | $V_{RMS}$ | f = 60 Hz |
| | $B_V$(I-O) | 3500 | | | VDC | |
| Isolation Resistance | | $10^{11}$ | $10^{12}$ | | Ω | $V_{I-O}$=500 V |
| Isolation Capacitance | | | .5 | | pF | f=1MHz |
| Collector-Emitter, Saturation Voltage | $V_{CE}$ (sat) | | 0.24 | 0.4 | V | $I_C$ = 2.0 mA, $I_F$ = 16 mA |
| Bandwidth (see note 1) | $B_W$ | | 150 | | KHz | $I_C$ = 2 mA, $V_{CE}$ = 10 V, $R_L$ = 100 Ω (Circuit No. 1) |

| SWITCHING TIMES | | | TYP | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|
| Non-Saturated | | | | | |
| Collector | Delay Time | $t_d$ | 0.5 | μs | $R_L$ = 100 Ω, $I_C$ = 2 mA, $V_{CC}$ = 10 V (Circuit No. 1) |
| | Rise Time | $t_r$ | 2.5 | | |
| | Storage Time | $t_s$ | 0.1 | | |
| | Fall Time | $t_f$ | 2.6 | | |
| Non-Saturated | | | | | |
| Collector | Delay Time | $t_d$ | 2.0 | μs | $R_L$ = 1 KΩ, $I_C$ = 2 mA, $V_{CC}$ = 10V (Circuit No. 1) |
| | Rise Time | $t_r$ | 15 | | |
| | Storage Time | $t_s$ | 0.1 | | |
| | Fall Time | $t_f$ | 15 | | |
| Saturated | | | | | |
| t on (from 5 V to 0.4 V) | | $t_{on}$ (SAT) | 5 | μs | $R_L$ = 2 KΩ, $I_F$ = 15 mA, $V_{CC}$ = 5 V $R_B$ = open (Circuit No. 2) |
| t off (from SAT to 4 V) | | $t_{off}$ (SAT) | 25 | | |
| Saturated | | | | | |
| t on (from 5 V to 0.4 V) | | $t_{on}$ (SAT) | 5 | μs | $R_L$ = 2 KΩ, $I_F$ = 20 mA, $V_{CC}$ = 5 V $R_B$ = 100 KΩ (Circuit No. 2) |
| t off (from SAT to 4 V) | | $t_{off}$ (SAT) | 18 | | |
| Non-Saturated | | | | | |
| Base | Rise Time | $t_r$ | 175 | ns | $R_L$ = 1 KΩ, $V_{CB}$ = 10 V |
| | Fall Time | $t_f$ | 175 | ns | |




Circuit 1




Circuit 2

## TYPICAL ELECTRO-OPTICAL CHARACTERISTIC CURVES

(25° C Free Air Temperature Unless Otherwise Specified)

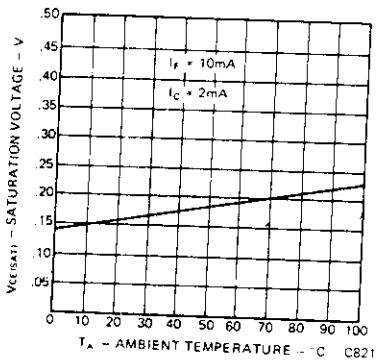



*Fig. 12. Saturation Voltage vs. Temperature*

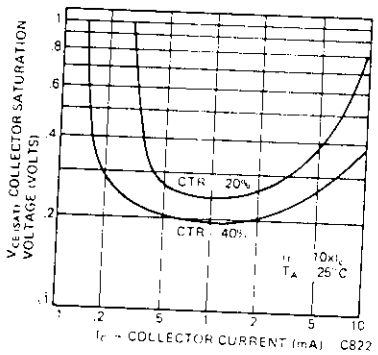



*Fig. 13. Saturation Voltage vs. Collector Current*

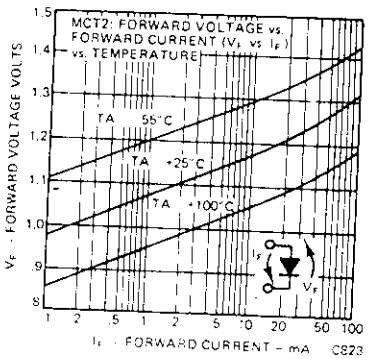



*Fig. 14. Forward Voltage vs. Forward Current*

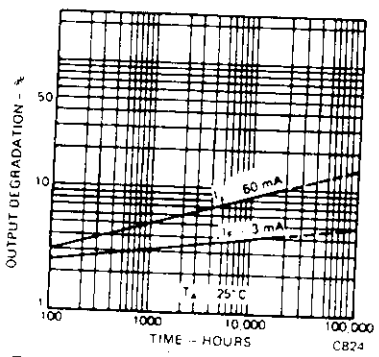



*Fig. 15. Lifetime vs. Forward Current (Note 4)*

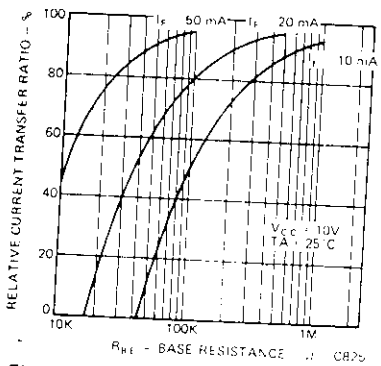



*Fig. 16. Sensitivity vs. Base Resistance*

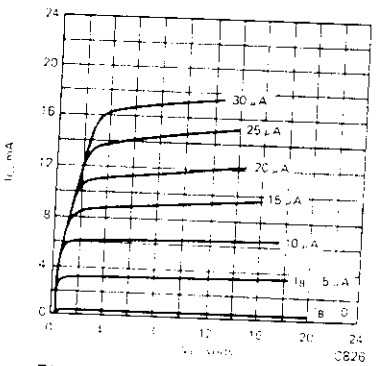
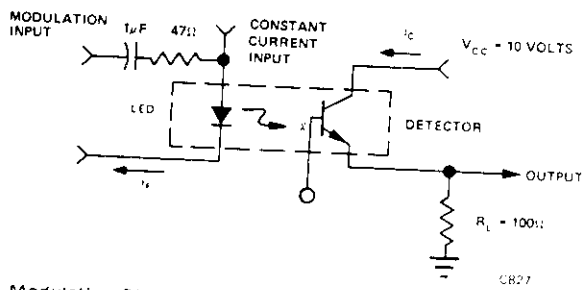
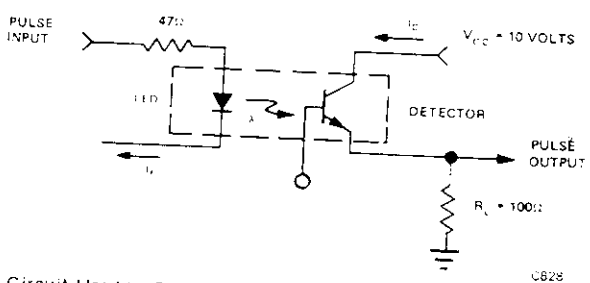



*Fig. 17. Detector Typical $h_{fe}$ Curves*

## OPERATING SCHEMATICS




Modulation Circuit Used to Obtain Output vs Frequency Plot




Circuit Used to Obtain Switching Time vs Collector Current Plot

## NOTES

1. *The current transfer ratio ($I_C/I_F$) is the ratio of the detector collector current to the LED input current with $V_{CE}$ at 10 volts.*
2. *The frequency at which $i_c$ is 3 dB down from the 1 kHz value.*
3. *Rise time ($t_r$) is the time required for the collector current to increase from 10% of its final value, to 90%.*
   *Fall time ($t_f$) is the time required for the collector current to decrease from 90% of its initial value, to 10%.*
4. *Normalized CTR degradation* $= \dfrac{CTR_o - CTR}{CTR_o}$

# Octal TRI-STATE® Buffers/Line Drivers/Line Receivers

## General Description

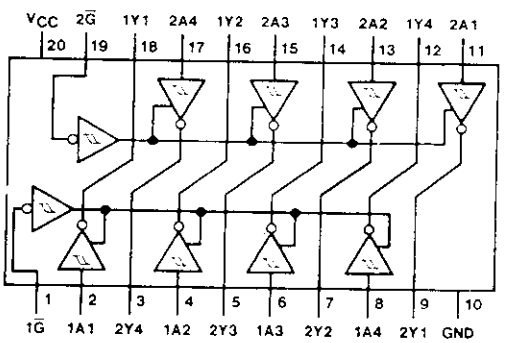
These buffers/line drivers are designed to improve both the performance and PC board density of TRI-STATE® buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs, and can be used to drive terminated lines down to 133 Ω.

## Features

- TRI-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at inputs improves noise margins

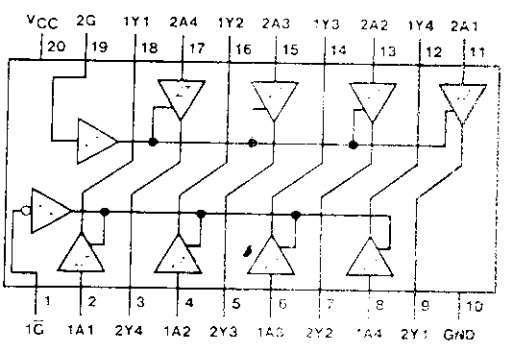
| | Typical $I_{OL}$ (Sink Current) | Typical $I_{OH}$ (Source Current) | Typical Propagation Delay Times Inverting | Noninverting | Typical Enable Disable Times | Typical Power Dissipation (Enabled) Inverting | Noninverting |
|---|---|---|---|---|---|---|---|
| 54LS | 12 mA | −12 mA | 10.5 ns | 12 ns | 15 ns | 130 mW | 135 mW |
| 74LS | 24 mA | −15 mA | 10.5 ns | 12 ns | 15 ns | 130 mW | 135 mW |
| 54S | 48 mA | −12 mA | 4.5 ns | 5 ns | 7 ns | 450 mW | 538 mW |
| 74S | 64 mA | −15 mA | 4.5 ns | 5 ns | 7 ns | 450 mW | 538 mW |

## Connection Diagrams



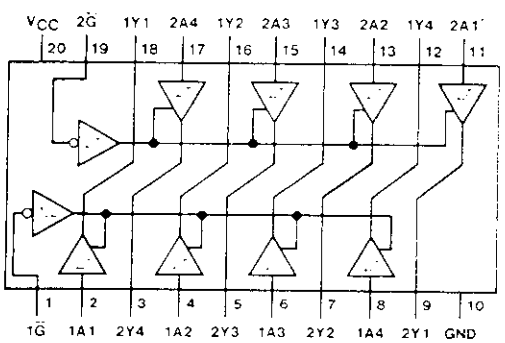

**54LS240 (J)**
**54S240 (J)**

**74LS240 (N)**
**74S240 (N)**




**54LS241 (J)**
**54S241 (J)**

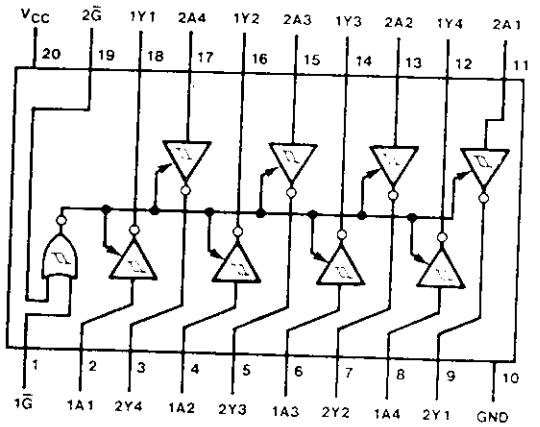
**74LS241 (N)**
**74S241 (N)**



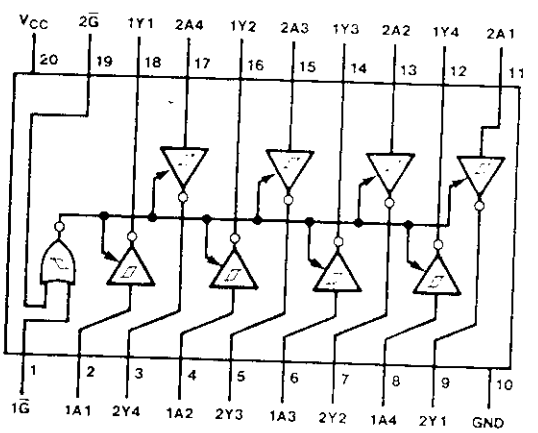

**54LS244 (J)**
**54S244 (J)**

**74LS244 (N)**
**74S244 (N)**

## Connection Diagrams (Continued)




**54S940 (J); 74S940 (N)**




**54S941 (J); 74S941 (N)**

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 LS240, LS241 LS244 | | | DM54/74 S240, S241, S244 S940, S941 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | | −1.5 | | | −1.2 | V |
| | Hysteresis ($V_{T+} - V_{T-}$) | $V_{CC}$ = Min | | | 0.2 | 0.4 | | 0.2 | 0.4 | | V |
| $I_{OH}$ | High Level Output Current | | | DM54 | | | −12 | | | −12 | mA |
| | | | | DM74 | | | −15 | | | −15 | |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −1 mA | | | 2.7 | | | 2.7 | | | |
| | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −3 mA | | | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.5 V, $I_{OH}$ = Max | | | 2 | | | 2 | | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 12 | | | 48 | mA |
| | | | | DM74 | | | 24 | | | 64 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IL}$ = 0.8 V, $V_{IH}$ = 2 V | $I_{OL}$ = 12 mA | | | | 0.4 | | | | V |
| | | | $I_{OL}$ = Max | DM54 | | | 0.4 | | | | |
| | | | | DM74 | | | 0.5 | | | 0.55 | |
| $I_{OZH}$ | Off-State Output Current High Level Voltage Applied | $V_{CC}$ = Max, $V_{IL}$ = 0.8 V, $V_{IH}$ = 2 V | $V_O$ = 2.7 V | | | | 20 | | | | µA |
| | | | $V_O$ = 2.4 V | | | | | | | 50 | |
| $I_{OZL}$ | Off-State Output Current, Low Level Voltage Applied | | $V_O$ = 0.4 V | | | | −20 | | | | |
| | | | $V_O$ = 0.5 V | | | | | | | −50 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 7 V | | | | 0.1 | | | | mA |
| | | | $V_I$ = 5.5 V | | | | | | | 1 | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.7 V | | | | | 20 | | | 50 | µA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.4 V | | | | −0.2 | | | | mA |
| | | | $V_I$ = 0.5 V | Any A | | | | | | −400 | µA |
| | | | | Any G | | | | | | −2 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | | −40 | | −225 | −50 | | −225 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max, Outputs Open | Outputs High | LS240, 241, 244 | | 13 | 23 | | | | |
| | | | | S240, S940 | DM54 | | | | 80 | 123 | mA |
| | | | | | DM74 | | | | 80 | 135 | |
| | | | | S241, 244, S941 | DM54 | | | | 95 | 147 | |
| | | | | | DM74 | | | | 95 | 160 | |
| | | | Outputs Low | LS240 | | 26 | 44 | | | | |
| | | | | LS241, 244 | | 27 | 46 | | | | |
| | | | | S240, S940 | DM54 | | | | 100 | 145 | |
| | | | | | DM74 | | | | 100 | 150 | |
| | | | | S241, 244, S941 | DM54 | | | | 120 | 170 | |
| | | | | | DM74 | | | | 120 | 180 | |
| | | | Outputs Disabled | LS240 | | 29 | 50 | | | | |
| | | | | LS241, 244 | | 32 | 54 | | | | |
| | | | | S240, S940 | DM54 | | | | 100 | 145 | |
| | | | | | DM74 | | | | 100 | 150 | |
| | | | | S241, 244, S941 | DM54 | | | | 120 | 170 | |
| | | | | | DM74 | | | | 120 | 180 | |

Note 1: All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

Note 2: Not more than one output should be shorted at a time and duration should not exceed one second.

5

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | Conditions | | | DM54/74 LS240, LS241 LS244 | | | DM54/74 S240, S241, S244 S940, S941 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $t_{PLH}$ | Propagation Delay Time Low to High Level Output | $C_L$ = 45 pF | $R_L$ = 667 Ω | LS240 | 3 | 9 | 14 | | | | ns |
| | | | | LS241, 244 | 5 | 12 | 18 | | | | |
| | | | $R_L$ = 90 Ω | S240, 940 | | | | 2 | 4.5 | 7 | |
| | | | | S241, 244, 941 | | | | 2 | 6 | 9 | |
| $t_{PHL}$ | Propagation Delay Time High to Low Level Output | $C_L$ = 45 pF | $R_L$ = 667 Ω | LS240 | 5 | 12 | 18 | | | | ns |
| | | | | LS241, 244 | 7 | 12 | 18 | | | | |
| | | | $R_L$ = 90 Ω | S240, 940 | | | | 2 | 4.5 | 7 | |
| | | | | S241, 244, 941 | | | | 2 | 6 | 9 | |
| $t_{PZL}$ | Output Enable Time to Low Level | $C_L$ = 45 pF | $R_L$ = 667 Ω | LS240 | 10 | 20 | 30 | | | | ns |
| | | | | LS241, 244 | 10 | 20 | 30 | | | | |
| | | | $R_L$ = 90 Ω | S240, 940 | | | | 3 | 10 | 15 | |
| | | | | S241, 244, 941 | | | | 3 | 10 | 15 | |
| $t_{PZH}$ | Output Enable Time to High Level | $C_L$ = 45 pF | $R_L$ = 667 Ω | LS240 | 5 | 15 | 23 | | | | ns |
| | | | | LS241, 244 | 10 | 15 | 23 | | | | |
| | | | $R_L$ = 90 Ω | S240, 940 | | | | 2 | 6.5 | 10 | |
| | | | | S241, 244, 941 | | | | 3 | 8 | 12 | |
| $t_{PLZ}$ | Output Disable Time from Low Level | $C_L$ = 5 pF | $R_L$ = 667 Ω | LS240 | 7 | 15 | 25 | | | | ns |
| | | | | LS241, 244 | 8 | 15 | 25 | | | | |
| | | | $R_L$ = 90 Ω | S240, 940 | | | | 4 | 10 | 15 | |
| | | | | S241, 244 941 | | | | 2 | 10 | 15 | |
| $t_{PHZ}$ | Output Disable Time from High Level | $C_L$ = 5 pF | $R_L$ = 667 Ω | LS240 | 5 | 10 | 18 | | | | ns |
| | | | | LS241, 244 | 5 | 10 | 18 | | | | |
| | | | $R_L$ = 90 Ω | S240, 940 | | | | 2 | 6 | 9 | |
| | | | | S241, 244, 941 | | | | 2 | 6 | 9 | |
| $t_{PLH}$ | Propagation Delay Time Low to High Level Output | $C_L$ = 150 pF | $R_L$ = 667 Ω | LS240 | 5 | 11 | 18 | | | | ns |
| | | | | LS241, 244 | 6 | 14 | 21 | | | | |
| | | | $R_L$ = 90 Ω | S240, 940 | | | | 3 | 7 | 10 | |
| | | | | S241, 244, 941 | | | | 4 | 9 | 12 | |
| $t_{PHL}$ | Progapation Delay Time High to Low Level Output | $C_L$ = 150 pF | $R_L$ = 667 Ω | LS240 | 6 | 15 | 22 | | | | ns |
| | | | | LS241, 244 | 6 | 15 | 22 | | | | |
| | | | $R_L$ = 90 Ω | S240, 940 | | | | 3 | 7 | 10 | |
| | | | | S241, 244, 941 | | | | 4 | 9 | 12 | |
| $t_{PZL}$ | Output Enable Time to Low Level | $C_L$ = 150 pF | $R_L$ = 667 Ω | LS240 | 12 | 22 | 33 | | | | ns |
| | | | | LS241, 244 | 12 | 22 | 33 | | | | |
| | | | $R_L$ = 90 Ω | S240, 940 | | | | 6 | 14 | 21 | |
| | | | | S241, 244, 941 | | | | 6 | 14 | 21 | |
| $t_{PZH}$ | Output Enable Time to High Level | $C_L$ = 150 pF | $R_L$ = 667 Ω | LS240 | 6 | 18 | 26 | | | | ns |
| | | | | LS241, 244 | 11 | 18 | 26 | | | | |
| | | | $R_L$ = 90 Ω | S240, 940 | | | | 4 | 9 | 12 | |
| | | | | S241, 244, 941 | | | | 4 | 10 | 15 | |

National Semiconductor



# LM741/LM741A/LM741C/LM741E Operational Amplifier

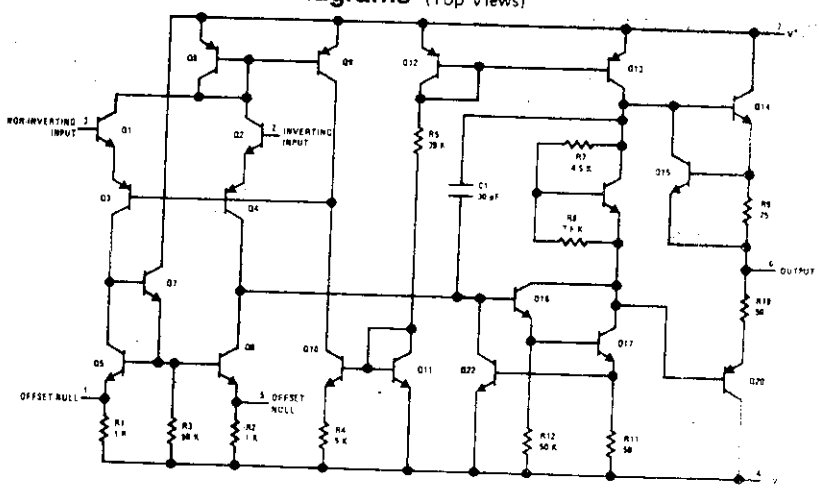
## General Description

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

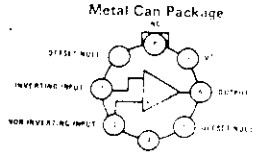
The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

The LM741C/LM741E are identical to the LM741/LM741A except that the LM741C/LM741E have their performance guaranteed over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

## Schematic and Connection Diagrams (Top Views)

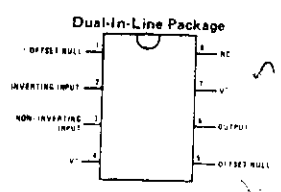



Metal Can Package



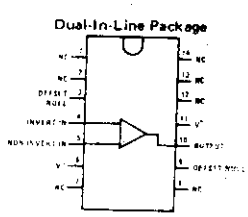
Order Number LM741H, LM741AH, LM741CH or LM741EH
See NS Package H08C

Dual-In-Line Package



Order Number LM741CN or LM741EN
See NS Package N08B
Order Number LM741CJ
See NS Package J08A

Dual-In-Line Package



Order Number LM741CN-14
See NS Package N14A
Order Number LM741J-14, LM741AJ-14 or LM741CJ-14
See NS Package J14A

National Semiconductor

A to D, D to

# DAC0800, DAC0801, DAC0802 8-Bit Digital-to-Analog Converters

## General Description

The DAC0800 series are monolithic 8-bit high-speed current-output digital-to-analog converters (DAC) featuring typical settling times of 100 ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC0800 series also features high compliance complementary current outputs to allow differential output voltages of 20 Vp-p with simple resistor loads as shown in *Figure 1*. The reference-to-full-scale current matching of better than ±1 LSB eliminates the need for full-scale trims in most applications while the nonlinearities of better than ±0.1% over temperature minimizes system error accumulations.

The noise immune inputs of the DAC0800 series will accept TTL levels with the logic threshold pin, $V_{LC}$ pin 1 grounded. Simple adjustments of the $V_{LC}$ potential allow direct interface to all logic families. The performance and characteristics of the device are essentially unchanged over the full ± 4.5V to ±18V power supply range; power dissipation is only 33 mW with ± 5V supplies and is independent of the logic input states.

The DAC0800, DAC0802, DAC0800C, DAC0801C a DAC0802C are a direct replacement for the DAC-0 DAC-08A, DAC-08C, DAC-08E and DAC-08 respectively.

## Features

- Fast settling output current — 100
- Full scale error — ±1 LS
- Nonlinearity over temperature — ±0.1
- Full scale current drift — ±10 ppm/
- High output compliance — −10V to +18
- Complementary current outputs
- Interface directly with TTL, CMOS, PMOS an others
- 2 quadrant wide range multiplying capability
- Wide power supply range — ±4.5V to ±18V
- Low power consumption — 33 mW at ±5V
- Low cost

## Typical Applications

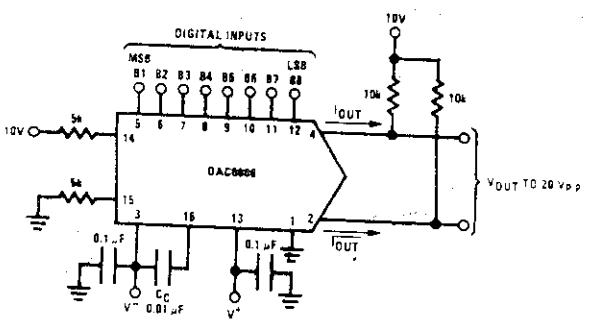
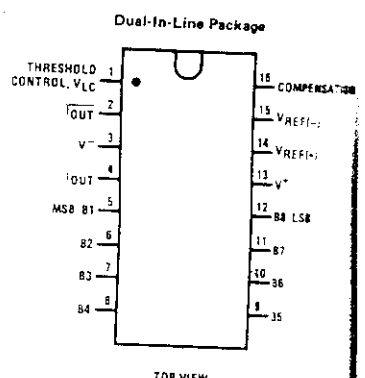



FIGURE 1. ±20 Vp-p Output Digital-to-Analog Converter

## Connection Diagram

Dual-In-Line Package



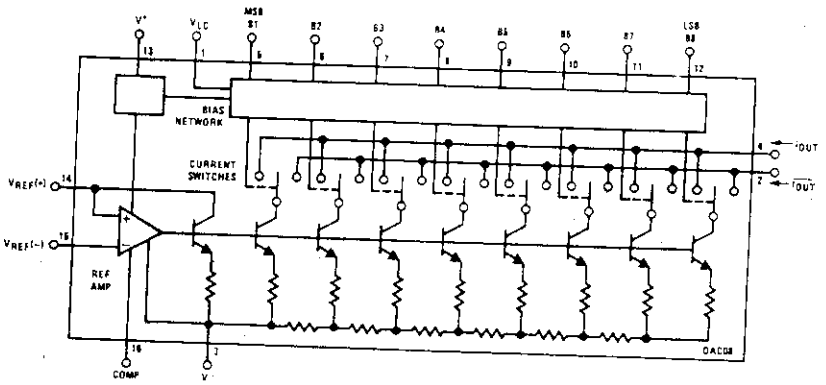

TOP VIEW

## Ordering Information

| NON LINEARITY | TEMPERATURE RANGE | ORDER NUMBERS* | | | | | |
|---|---|---|---|---|---|---|---|
| | | D PACKAGE (D16C) | | J PACKAGE (J16A) | | N PACKAGE (N16A) | |
| ±0.1% FS | −55°C ≤ $T_A$ ≤ +125°C | DAC0802LD | DAC-08AQ | DAC0802LCJ | DAC-08HQ | DAC0802LCN | DAC-08H |
| ±0.1% FS | 0°C ≤ $T_A$ ≤ +70°C | | | | | | |
| ±0.19% FS | −55°C ≤ $T_A$ ≤ +125°C | DAC0800LD | DAC-08Q | | | | |
| ±0.19% FS | 0°C ≤ $T_A$ ≤ +70°C | | | | | | |
| ±0.39% FS | 0°C ≤ $T_A$ ≤ +70°C | | | DAC0800LCJ | DAC-08EQ | DAC0800LCN | DAC-08E |
| | | | | DAC0801LCJ | DAC-08CQ | DAC0801LCN | DAC-08C |

*Note. Devices may be ordered by using either order number.

## Block Diagram




## Equivalent Circuit

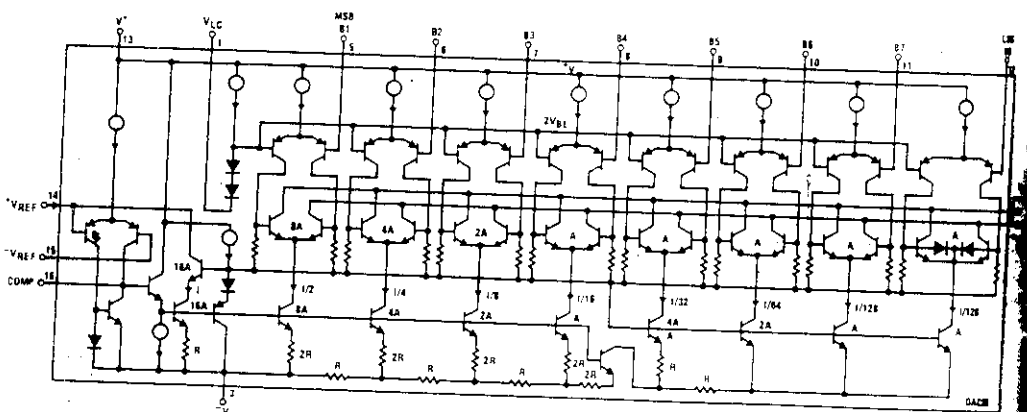



FIGURE 2

## ...olute Maximum Ratings

| | |
|---|---|
| ...y Voltage | ±18V or 36V |
| ... Dissipation (Note 1) | 500 mW |
| ...ence Input Differential Voltage (V14 to V15) | $V^-$ to $V^+$ |
| ...ence Input Common-Mode Range (V14, V15) | $V^-$ to $V^+$ |
| ...ence Input Current | 5 mA |
| ...Inputs | $V^-$ to $V^-$ plus 36V |
| ...g Current Outputs | *Figure 24* |
| ... Temperature | −65°C to +150°C |
| ...Temperature (Soldering, 10 seconds) | 300°C |

## Operating Conditions

| | MIN | MAX | UNITS |
|---|---|---|---|
| Temperature ($T_A$) | | | |
| DAC0802L | −55 | +125 | °C |
| DAC0800L | −55 | +125 | °C |
| DAC0800LC | 0 | +70 | °C |
| DAC0801LC | 0 | +70 | °C |
| DAC0802LC | 0 | +70 | °C |

## ...trical Characteristics ($V_S$ = ±15V, $I_{REF}$ = 2 mA, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified.

... characteristics refer to both $I_{OUT}$ and $\overline{I_{OUT}}$.)

| PARAMETER | CONDITIONS | DAC0802L/ DAC0802LC | | | DAC0800L/ DAC0800LC | | | DAC0801LC | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| Resolution | | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | Bits |
| Monotonicity | | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | Bits |
| Nonlinearity | | | | ±0.1 | | | ±0.19 | | | ±0.39 | %FS |
| Settling Time | To ±1/2 LSB, All Bits Switched "ON" or "OFF", $T_A$ = 25°C | | 100 | 135 | | | | | 100 | 150 | ns |
| | DAC0800L | | | | | 100 | 135 | | | | ns |
| | DAC0800LC | | | | | 100 | 150 | | | | ns |
| ... Propagation Delay | $T_A$ = 25°C | | | | | | | | | | |
| Each Bit | | | 35 | 60 | | 35 | 60 | | 35 | 60 | ns |
| All Bits Switched | | | 35 | 60 | | 35 | 60 | | 35 | 60 | ns |
| Full Scale Tempco | | | ±10 | ±50 | | ±10 | ±50 | | ±10 | ±80 | ppm/°C |
| Output Voltage Compliance | Full Scale Current Change < 1/2 LSB, $R_{OUT}$ > 20 MΩ Typ | −10 | | 18 | −10 | | 18 | −10 | | 18 | V |
| Full Scale Current | $V_{REF}$ = 10.000V, R14 = 5.000 kΩ R15 = 5.000 kΩ, $T_A$ = 25°C | 1.984 | 1.992 | 2.000 | 1.94 | 1.99 | 2.04 | 1.94 | 1.99 | 2.04 | mA |
| Full Scale Symmetry | $I_{FS4} - I_{FS2}$ | | ±0.5 | ±4.0 | | ±1 | ±8.0 | | ±2 | ±16 | µA |
| Zero Scale Current | | | 0.1 | 1.0 | | 0.2 | 2.0 | | 0.2 | 4.0 | µA |
| Output Current Range | $V^-$ = −5V | 0 | 2.0 | 2.1 | 0 | 2.0 | 2.1 | 0 | 2.0 | 2.1 | mA |
| | $V^-$ = −8V to −18V | 0 | 2.0 | 4.2 | 0 | 2.0 | 4.2 | 0 | 2.0 | 4.2 | mA |
| Logic Input Levels | | | | | | | | | | | |
| Logic "0" | $V_{LC}$ = 0V | | | 0.8 | | | 0.8 | | | 0.8 | V |
| Logic "1" | | 2.0 | | | 2.0 | | | 2.0 | | | V |
| Logic Input Current | $V_{LC}$ = 0V | | | | | | | | | | |
| Logic "0" | −10V ≤ $V_{IN}$ ≤ +0.8V | | −2.0 | −10 | | −2.0 | −10 | | −2.0 | −10 | µA |
| Logic "1" | 2V ≤ $V_{IN}$ ≤ +18V | | 0.002 | 10 | | 0.002 | 10 | | 0.002 | 10 | µA |
| ... Logic Input Swing | $V^-$ = −15V | −10 | | 18 | −10 | | 18 | −10 | | 18 | V |
| ... Logic Threshold Range | $V_S$ = ±15V | −10 | | 13.5 | −10 | | 13.5 | −10 | | 13.5 | V |
| ... Reference Bias Current | | | −1.0 | −3.0 | | −1.0 | −3.0 | | −1.0 | −3.0 | µA |
| Reference Input Slew Rate | *(Figure 24)* | 4.0 | 8.0 | | 4.0 | 8.0 | | 4.0 | 8.0 | | mA/µs |
| Power Supply Sensitivity | 4.5V ≤ $V^+$ ≤ 18V | | 0.0001 | 0.01 | | 0.0001 | 0.01 | | 0.0001 | 0.01 | %/% |
| | −4.5V ≤ $V^-$ < 18V | | 0.0001 | 0.01 | | 0.0001 | 0.01 | | 0.0001 | 0.01 | %/% |
| | $I_{REF}$ = 1 mA | | | | | | | | | | |
| Power Supply Current | $V_S$ = ±5V, $I_{REF}$ = 1 mA | | | | | | | | | | |
| | | | 2.3 | 3.8 | | 2.3 | 3.8 | | 2.3 | 3.8 | mA |
| | | | −4.3 | −5.8 | | −4.3 | −5.8 | | −4.3 | −5.8 | mA |
| | $V_S$ = 5V, −15V, $I_{REF}$ = 2 mA | | | | | | | | | | |
| | | | 2.4 | 3.8 | | 2.4 | 3.8 | | 2.4 | 3.8 | mA |
| | | | 6.4 | 7.8 | | 6.4 | 7.8 | | 6.4 | 7.8 | mA |
| | $V_S$ = ±15V, $I_{REF}$ = 2 mA | | | | | | | | | | |
| | | | 2.5 | 3.8 | | 2.5 | 3.8 | | 2.5 | 3.8 | mA |
| | | | 6.5 | 7.8 | | 6.5 | 7.8 | | 6.5 | 7.8 | mA |
| Power Dissipation | ±5V, $I_{REF}$ = 1 mA | | 33 | 48 | | 33 | 48 | | 33 | 48 | mW |
| | 5V, −15V, $I_{REF}$ = 2 mA | | 108 | 136 | | 108 | 136 | | 108 | 136 | mW |
| | ±15V, $I_{REF}$ = 2 mA | | 135 | 174 | | 135 | 174 | | 135 | 174 | mW |

... The maximum junction temperature of the DAC0800, DAC0801 and DAC0802 is 125°C. For operating at elevated temperatures, devices ...-in-line J or D package must be derated based on a thermal resistance of 100° C/W, junction to ambient, 175°C/W for the molded dual-... package.

## Performance Characteristics

Full Scale Current vs Reference Current

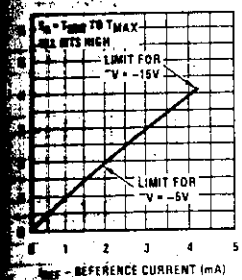



FIGURE 3

LSB Propagation Delay vs $I_{FS}$

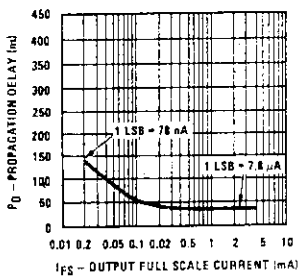
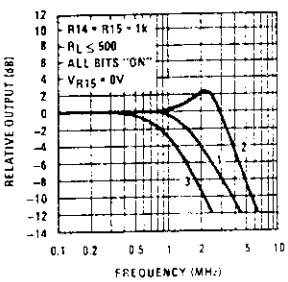



FIGURE 4

Reference Input Frequency Response



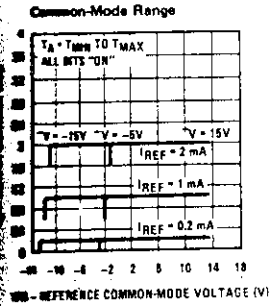

**Curve 1:** $C_C$ = 15 pF, $V_{IN}$ = 2 Vp-p centered at 1V.

**Curve 2:** $C_C$ = 15 pF, $V_{IN}$ = 50 mVp-p centered at 200 mV.

**Curve 3:** $C_C$ = 0 pF, $V_{IN}$ = 100 mVp-p at 0V and applied through 50 Ω connected to pin 14. 2V applied to R14.

FIGURE 5

Reference Amp Common-Mode Range




Note: Positive common-mode range is always (V+) − 1.5V.

FIGURE 6

Logic Input Current vs Input Voltage

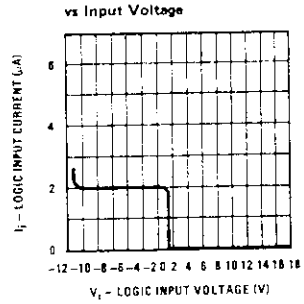



FIGURE 7

$V_{TH} - V_{LC}$ vs Temperature

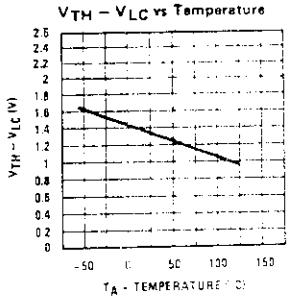



FIGURE 8

Output Current vs Output Voltage (Output Voltage Compliance)

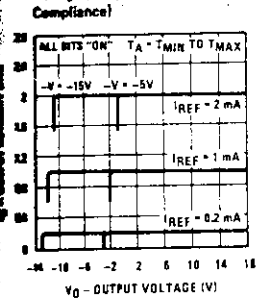



FIGURE 9

Output Voltage Compliance vs Temperature

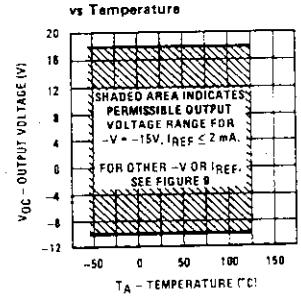
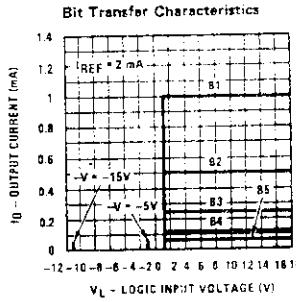



FIGURE 10

Bit Transfer Characteristics




Note: B1–B8 have identical transfer characteristics. Bits are fully switched with less than 1/2 LSB error, at less than ±100 mV from actual threshold. These switching points are guaranteed to lie between 0.8 and 2V over the operating temperature range ($V_{LC}$ = 0V).

FIGURE 11

## General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The LS138 and S138 decode one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The LS139 and S139 comprise two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

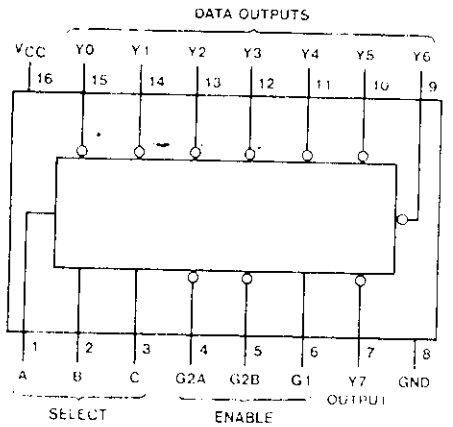
All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

## Features

- Designed specifically for high-speed
  - Memory decoders
  - Data transmission systems
- S138 and LS138 3-to-8-line decoders incorporate 3 enable inputs to simplify cascading and/or data reception
- S139 and LS139 contain two fully independent 2-to-4-line decoders/demultiplexers
- Schottky clamped for high performance

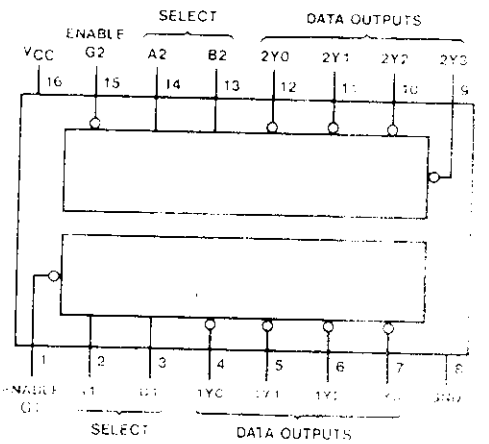
| Type | Typical Propagation Delay (3 Levels of Logic) | Typical Power Dissipation |
|---|---|---|
| LS138 | 21 ns | 32 mW |
| S138 | 8 ns | 245 mW |
| LS139 | 21 ns | 34 mW |
| S139 | 7.5 ns | 185 mW |

## Connection Diagrams




54LS138 (J,W)
54S138 (J,W)

74LS138 (N)
74S138 (N)

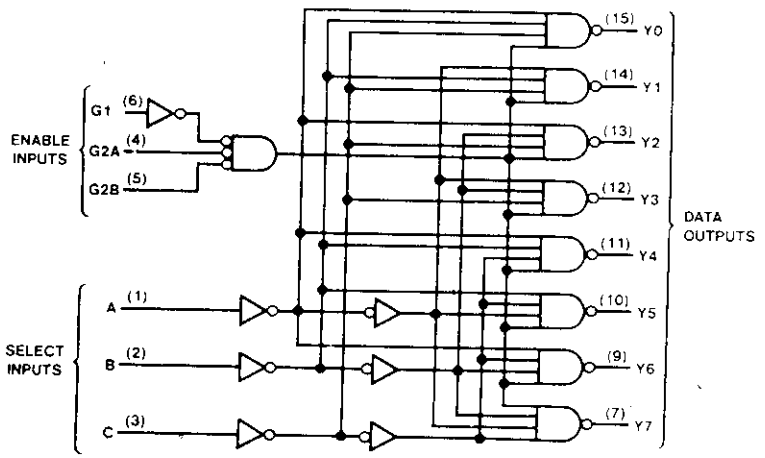



54LS139 (J,W)
54S139 (J,W)

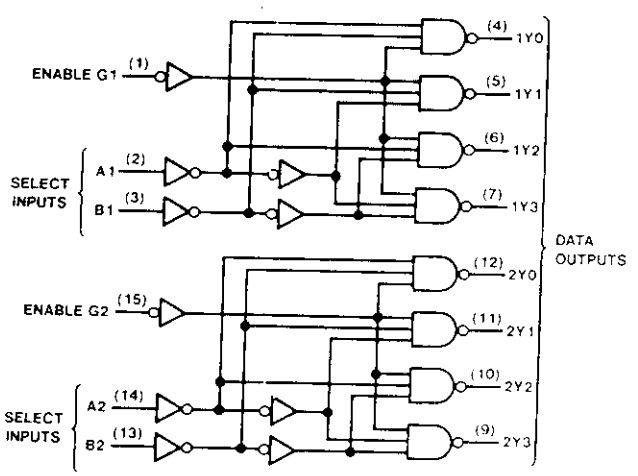
74LS139 (N)
74S139 (N)

## Logic Diagrams

138, S138, LS138




139, S139, LS139



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 LS138, LS139 Min | Typ (1) | Max | DM54/74 S138, S139 Min | Typ (1) | Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | | −1.5 | | | −1.2 | V |
| $I_{OH}$ | High Level Output Current | | | | | | −400 | | | −1000 | µA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OH}$ = Max | | DM54 | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | | | DM74 | 2.7 | 3.4 | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 4 | | | 20 | mA |
| | | | | DM74 | | | 8 | | | 20 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $I_{OL}$ = Max | DM54 | | 0.25 | 0.4 | | | 0.5 | V |
| | | | | DM74 | | 0.35 | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 4 mA | DM74 | | 0.25 | 0.4 | | | | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | | | | 1 | mA |
| | | | $V_I$ = 7 V | | | | 0.1 | | | | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max | $V_I$ = 2.7 V | | | | 20 | | | 50 | µA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.4 V | | | | −0.36 | | | | mA |
| | | | $V_I$ = 0.5 V | | | | | | | −2 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | DM54 | −20 | | −100 | −40 | | −100 | mA |
| | | | | DM74 | −20 | | −100 | −40 | | −100 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max, Outputs Enabled and Open | | LS138, S138 | | 6.3 | 10 | | 49 | 74 | mA |
| | | | | LS139, S139 | | 6.8 | 11 | | 60 | 90 | |

Note 1. All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25 °C.

Note 2. Not more than one output should be shorted at a time, and duration of short-circuit should not exceed one second.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | Levels of Delay | Conditions | DM54/74 LS138 Min | DM54/74 LS138 Typ | DM54/74 LS138 Max | DM54/74 LS139 Min | DM54/74 LS139 Typ | DM54/74 LS139 Max | Conditions | DM54/74 S138 Min | DM54/74 S138 Typ | DM54/74 S138 Max | DM54/74 S139 Min | DM54/74 S139 Typ | DM54/74 S139 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low to High Level Output | Binary Select | Any | 2 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 18 | 27 | | 18 | 27 | $C_L$ = 15 pF, $R_L$ = 280 kΩ | | 4.5 | 7 | | 5 | 7.5 | ns |
| | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 16 | 27 | | 16 | 27 | $C_L$ = 50 pF, $R_L$ = 280 kΩ | | 6 | 9 | | 6.5 | 10 | |
| $t_{PHL}$ | Propagation Delay Time, High to Low Level Output | | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 17 | 27 | | 17 | 27 | $C_L$ = 15 pF, $R_L$ = 280 kΩ | | 7 | 10.5 | | 6.5 | 10 | |
| | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 23 | 40 | | 23 | 40 | $C_L$ = 50 pF, $R_L$ = 280 kΩ | | 9 | 14 | | 8.5 | 13 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low to High Level Output | | | 3 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 13 | 18 | | 13 | 18 | $C_L$ = 15 pF, $R_L$ = 280 kΩ | | 7.5 | 12 | | 7 | 12 | |
| | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 16 | 27 | | 16 | 27 | $C_L$ = 50 pF, $R_L$ = 280 kΩ | | 9 | 14 | | 8.5 | 15 | |
| $t_{PHL}$ | Propagation Delay Time, High to Low Level Output | | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 17 | 27 | | 17 | 27 | $C_L$ = 15 pF, $R_L$ = 280 kΩ | | 8 | 13 | | 8 | 13 | |
| | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 23 | 40 | | 23 | 40 | $C_L$ = 50 pF, $R_L$ = 280 kΩ | | 10 | 15 | | 10 | 15 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low to High Level Output | | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 13 | 18 | | 13 | 18 | $C_L$ = 15 pF, $R_L$ = 280 kΩ | | 5 | 8 | | 6 | 8 | |
| | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 18 | 27 | | 18 | 27 | $C_L$ = 50 pF, $R_L$ = 280 kΩ | | 8 | 12 | | 6.5 | 9 | |
| $t_{PHL}$ | Propagation Delay Time, High to Low Level Output | | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 18 | 27 | | 18 | 27 | $C_L$ = 15 pF, $R_L$ = 280 kΩ | | 8 | 12 | | 8.5 | 13 | |
| | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 22 | 40 | | 22 | 40 | $C_L$ = 50 pF, $R_L$ = 280 kΩ | | 10 | 15 | | 10 | 15 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low to High Level Output | Enable | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 18 | 27 | | N.A. | | $C_L$ = 15 pF, $R_L$ = 280 kΩ | | 5 | 8 | | N.A. | | |
| | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 18 | 27 | | N.A. | | $C_L$ = 50 pF, $R_L$ = 280 kΩ | | 8.5 | 13 | | N.A. | | ns |
| $t_{PHL}$ | Propagation Delay Time, High to Low Level Output | | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 19 | 29 | | N.A. | | $C_L$ = 15 pF, $R_L$ = 280 kΩ | | 7 | 11 | | N.A. | | |
| | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 25 | 40 | | N.A. | | $C_L$ = 50 pF, $R_L$ = 280 kΩ | | 9 | 14 | | N.A. | | ns |

## Truth Tables

LS138, S138

| Inputs | | | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Enable | | Select | | | | | | | | | | |
| G1 | G2* | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | H | H | H | H | H | H | H | H | H | H | L |

*G2 = G2A + G2B

H = High level, L = low level, X = don't care

LS139, S139

| Inputs | | | Outputs | | | |
|---|---|---|---|---|---|---|
| Enable | Select | | | | | |
| G | B | A | Y0 | Y1 | Y2 | Y3 |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
| L | H | L | H | H | L | H |
| L | H | H | H | H | H | L |

H = High level, L = low level, X = don't care

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