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Automobile Antitheft Alarm

Project Work 1994-95

Submitted by

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Certificate

This is to Certify that the report entitled

"AUTOMOBILE ANTITHEFT ALARM"

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Head of the Department

Certified that the candidate was examined by us in the project work Viva–Voce Examination held on 6-04-95 *and the University Register number was* _____

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External Examiner

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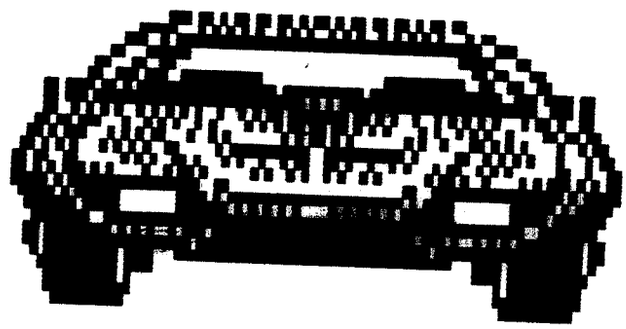
AUTOMOBILE ANTITHEFT ALARM



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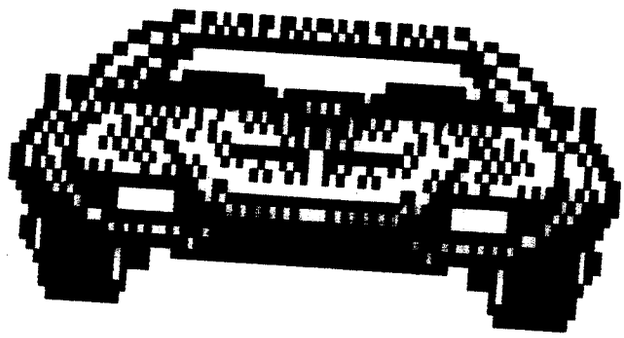

ACKNOWLEDGEMENT

ACKNOWLEDGEMENTS

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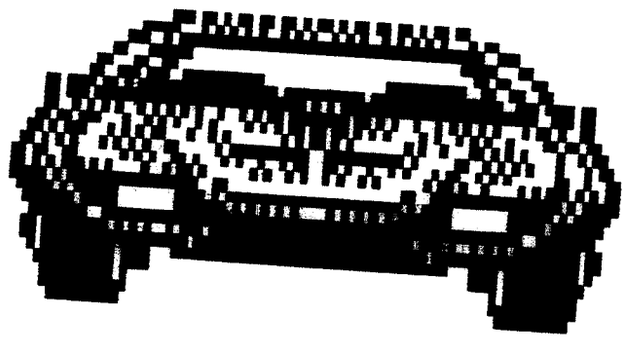


SYNOPSIS

SYNOPSIS

Car theft has increased throughout the country. There are experts who can steal cars within minutes. It is common knowledge that the car accessories cost more than 50% of the total cost of the car. So care should be taken to protect these accessories also from being stolen. The purpose of this system Automobile Antitheft Alarm is to prevent the car as well as the car accessories from being stolen The system is so designed that it takes care of all the possibilities of a thief entering a car.

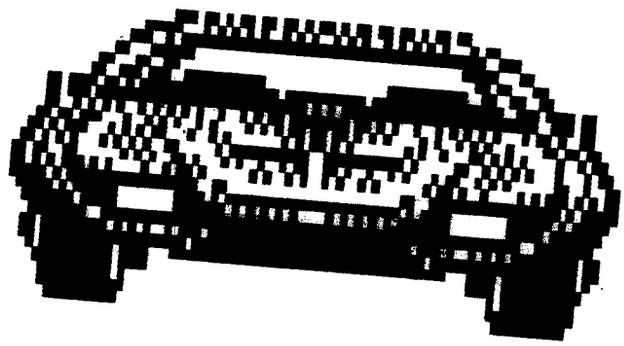
The alarm system used should be in such a way that it attracts the people in and around the place. At the same time, the alarm should not be of nuisance value to the owner. If so, the system can readily be made to give false alarms, so that the theives can easily persuade the owners to disconnect the system by repeatedly false triggering the alarms. This can be avoided by adjusting the sensitivity of the system.

The microcontroller we make use of for this system is Zilog Z86E04. The use of this microcontroller reduces the size as well as the cost of the whole system. The reliability also increases to a greater extent as the life

of the controller is the main fact to be considered whereas if a controller is not used, the life of each block has to be considered separately. So the Failure Mode Effect Analysis [F M E A] becomes complicated.

This system enables the owner to be free without the tension of his car being stolen. The system is so designed that the owner need not take any pains to check if the system is "ON" before he gets out of the car. The system is switched on by itself when the owner locks the car door.

This system has been tested and found to be working to the customer's satisfaction. Some real time pilot units of this system have been released by "PRICOL" to survey the response of this unit in the market.



INTRODUCTION

I. INTRODUCTION

The automobile antitheft alarm has been designed mainly to provide a fool proof method to protect the automobile from theft.

Vehicle antitheft devices come in two basic types. The first of these is the immobiliser which is intended simply to reduce a theif's chances of starting or driving away the target vehicle.

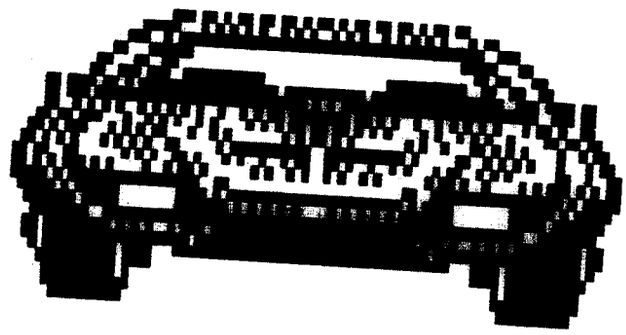
The second type gives protection against the car burglar who merely wishes to steal objects that are left inside the vehicle and other car accessories.

The Automobile Antitheft Alarm is a combination of both these types and in other words is the true burglar alarm.

The urge for designing such a system is due to the increased rate of theft of cars and car accessories. One more reason which added fuel to fire to design such a system is that there is no Indian company that actually manufactures a car theft alarm. Generally it is imported and then sold in India.

The systems so far available in the market have no protection against tow-away thieves. This Automobile Antitheft Alarm provides protection against tow-away thieves also.

Moreover, this system is reliable and inexpensive.



MODES OF BURGLARY

II. MODES OF BURGLARY:

To either get on access to the car or to drive away the car a burglar may handle many techniques which would be seen very commonly in day to day life. The following are the popular modes of burglary found often.

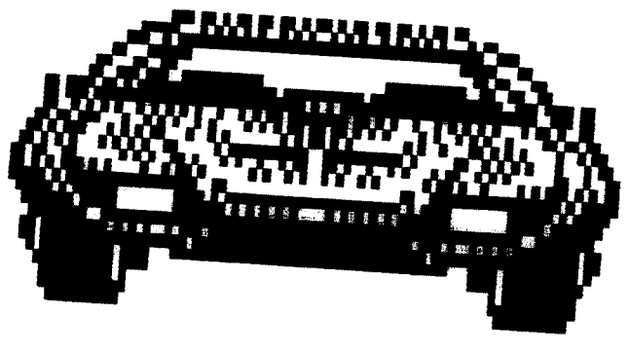
* The prime mode of a burglar to access a car is to use a duplicate key. This is the simplest technique by which he can enter the car by opening the lock, even in a densely packed area. But there may be a chance of the owner using different key for ignition. In that case, the burglar may even try another duplicate to drive away the car or he may run away with the things left in the car and most commonly tape recorders are stolen away.

* The next mode of a thief is to cut the beading of the window and remove the glass with ease either by pushing it down or using a glass cutter to cut the glass and open the door lock thereby entering the car.

* There are even certain cases where when the beading is cut the whole glass would come off easily enabling the burglar to directly enter the car and steal things or

even run away with the car. The thief can use duplicate ingnition key or by shorting the wire of the ignition from the cut-out board. This is called hot wiring.

* Another common mode used is the stealing of the engine, horn, battery, pumps, carburetters etc. This usually cannot be prevented unless the owner makes a point to park it in safe areas.



SYSTEM OVERVIEW

III. SYSTEM OVERVIEW :

Let us first have a precise and clear cut idea of the whole system. The power supply to the overall system comes from the car battery. It is given through a regulator (7805) for conversion from 12 V to 5 V.

The input signals to the microcontroller come from

i) The transducer

ii) The password control (DIP switch) and the output signals go to the

i) DAC ladder network

ii) Alarm and

iii) Immobilizer unit.

A 4 MHz external clock is generated by a crystal with a RC network. The output of DAC is connected to P33 which is used as a reference.

The owner loads a password from the socket in to a buffer initially and when the driver sidedoor is locked, the password is transferred to the controller. By giving

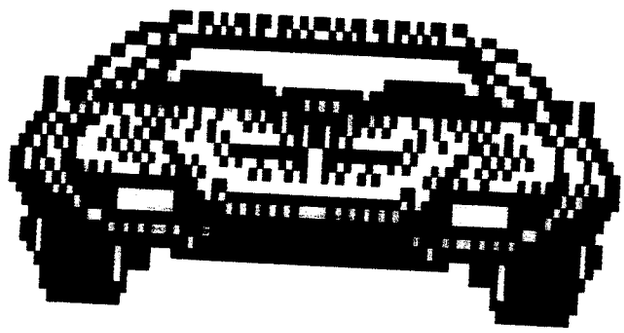
several inputs to the DAC and comparing it with the transducer output a digital reference is generated.

The output of the transducer is sampled regularly and when any variation is sensed it immediately triggers a timer routine. Within 10 seconds, the system expects a password. which if not given precisely triggers the alarm and the immobilizer, thus performing two functions simultaneously ie.,

i) informing the public

ii) preventing the vehicle from getting started by means of hot-wiring

In case of a failure of the alarm, as an alternative, the car horn can be made to sound.



SALIENT PARTS OF A CAR USED IN THIS SYSTEM

IV. SALIENT PARTS OF A CAR USED IN THIS SYSTEM

4.1 SHOCK ABSORBERS

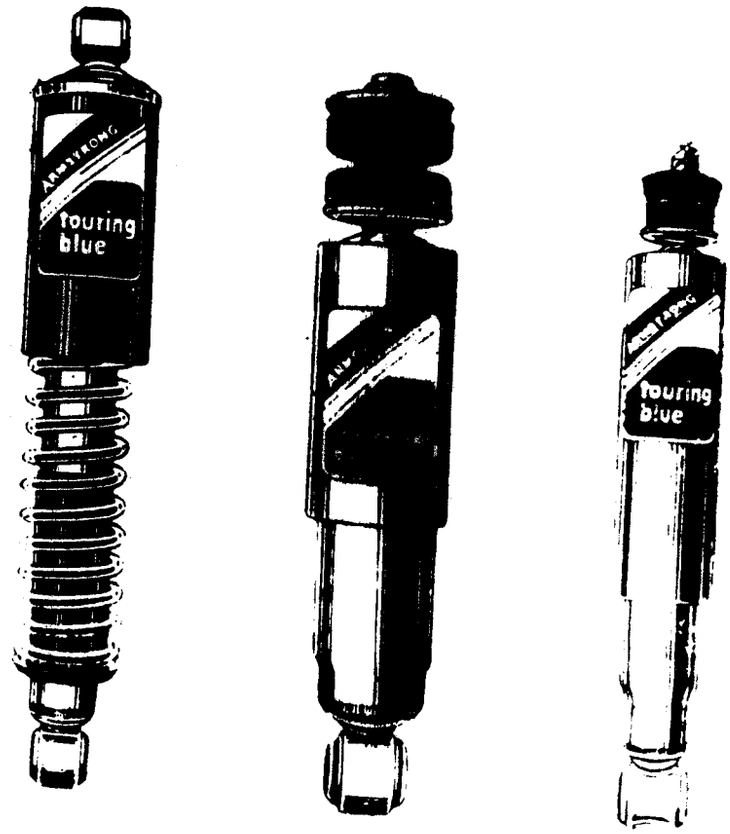
A wide variety of shock absorbing devices have been used to control spring action. Today, however, direct double acting, "telescoping" hydraulic shock absorbers have almost universal application.

At the front, each shock absorber often extends through the coil spring from the lower control arm to a bracket attached to the frame. On Chrylser cars with torsion bar suspension, the front shock absorbers attach to the lower control arm and mount to a bracket on the frame.

In the case of high-mounted coil spings, each front shock absorber extends from the upper control arm to a platform mounted in the spring tower or to a bracket on the wheel housing in the engine compartment.

At the rear, the lower end of the shock absorber usually is attached to a bracket welded to the axle housing. The upper end is fastened to the frame or to the coil spring upper seat, which is integral with the frame or body On cars with rear left springs, the rear shock absorbers

SHOCK ABSORBERS



generally extend from a stud attached to the spring U-bolt mounting bracket to the frame cross member. Quite often the rear shock absorbers are mounted at an angle to assist in restricting lateral movement as well as vertical movement.

Some Oldsmobile Toronado and Cadillac Eldorado cars use four rear shock absorbers to give better ride control. And, for this same reason, some Chevrolet cars have "biar-mounted" rear shock absorbers. The curb-side unit is mounted in front of the axle housing; the steet-side unit is mounted in back of the housing. Some Ford cars feature this arrangement, too.

The operating principle of direct-acting hydraulic shock absorbers consists of forcing fluid through restricting orifices in the valves. The restricted flow serves to slow down and control the rapid movement of the car springs as they react to road irregularities. Generally, fluid flow through the piston is controlled by spring-loaded valves.

The hydraluic shock absorber automatically adapts itself to the severity of the shock. If the axle moves slowly, resistance to the flow of fluid will be light. If axle movement is rapid or forceful, the resistance is much

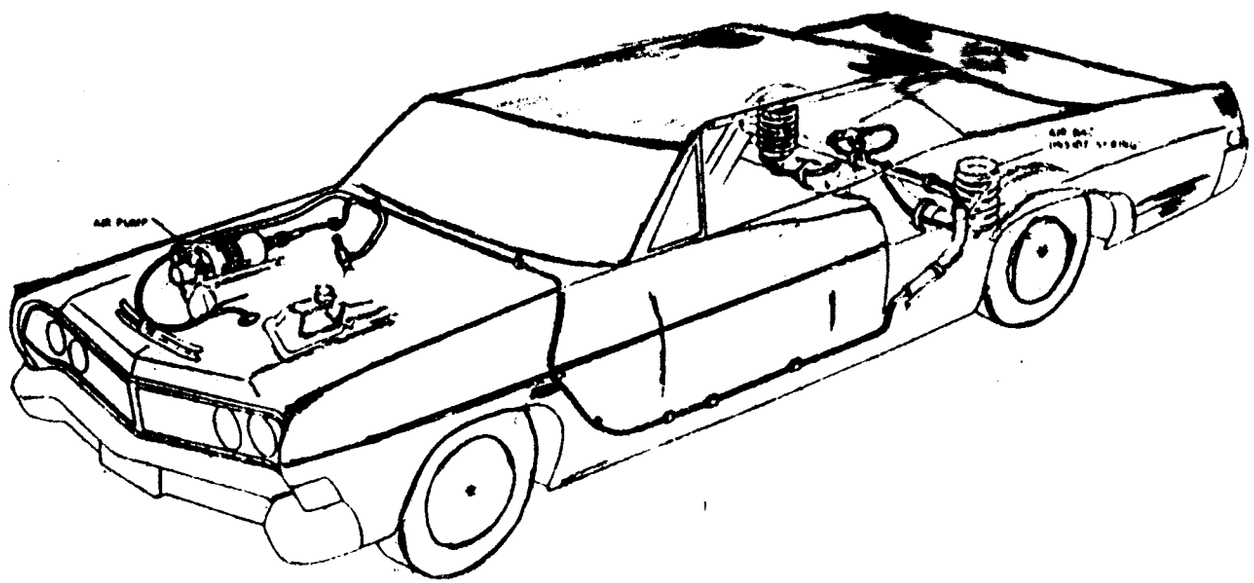


Fig. 38-17. Older Fords had an optional air spring stabilizing system in which minimum clearance is maintained between body frame and rear axle under loaded conditions.

stronger since more time is required to force fluid through the orifices.

By these hydraulic actions and reaction, the shock absorbers permit a soft ride over small bumps and provide firm control over spring action for cushioning large bumps. The double-acting units operate efficiently in both directions. Spring rebound can be almost as violent as the original action that compressed the shock absorber.

4.2 BATTERY IGNITION

4.2.1. IGNITION IN THE SPARK IGNITION ENGINE :

The design of the ignition system in the spark-ingnition engine depends upon how ignition is triggered, ignition timing adgustment and how the high tension is distributed and conveyed. Table 1 shows a classification of various ignition systems.

4.2.2 IGNITION POINT :

The ignition point is essentially dependent on the variables "engine speed" and "load". It is dependent upon the engine speed since the time taken for complete combustion of the mixture at constant charge and with a

Table 1.

Definition of the ignition system.

An ignition system must perform atleast the following functions

Function	Ignition system			
	CI	TI	SI	BSI
	Coil ignition	Transistorized ignition	Semiconductor ignition	Distributor-less semiconduct ignition
Ignition triggering (pulse generator)	Mechanical	Electronic	Electronic	Electronic
Determining the ignition angle of the basis of the speed and load condition of the engine	Mechanical	Mechanical	Electronic	Electronic
High-tension generation	Inductive	Inductive	Inductive	Inductive
Distribution and assignment of the ignition spark to the correct cylinder	Mechanical	Mechanical	Mechanical	Electrnic
Power section	Mechanical	Electronic	Electronic	Electronic

constant air-fuel ratio is constant and, thus, ignition must occur earlier with increasing engine speed. The dependence upon the load is influenced by the leaner mixture in the case of low loads, the residual gas content and the lower charge of the cylinder. This influence causes a longer ignition delay and lower combustion rates in the mixture so that the ignition angle needs to be advanced.

4.2.3 SPARK ADVANCE :

The behaviour of the ignition system as a function of the engine speed and load is incorporated in the ignition-timing function. In the simplest case, the ignition-timing function comprises a centrifugal advance mechanism and a vaccum control unit. The vaccum is largely a measure of the engine load.

Semiconductor ignition systems also allow for other influences of the engine, e.g., temperature or changes in the mixture composition. The values of all ignition timing functions are linked either mechanically or electronically in order to determine the ignition point. The energy storage device must be charged in good time before the actual ignition point. This requires the formation of a dwell period or dwell angle in the ignition system. The

energy is generally stored in an inductive storage device, and, in rare cases, in a capacitive storage device. The high tension results from disconnecting the primary inductor from the power supply followed by transformation. The high tension is applied to the cylinder currently performing the working stroke. The position information of the crankshaft required for this is provided by an appropriate mechanism via the ignition distributor drive if using an ignition distributor.

In the case of stationary high-tension distribution an electrical signal from the crankshaft or the camshaft is required for this purpose. The connecting elements (plugs and hightension cable) convey the high tension to the spark plug. The spark plug must function reliably in all operating ranges of the engine in order to always ensure ignition of the mixture.

4.2.4 FIRING VOLTAGE :

The excess air factor and the cylinder pressure which is determined by charge and compressor have, together with the electrode gap of the spark plug, a crucial influence upon the required voltage and, thus, upon the required secondary available voltage of the ignition system

4.2.5 IGNITION OF THE MIXTURE - IGNITION ENERGY :

Approximately 0.2 mJ of energy is required per individual ignition for igniting an air-fuel mixture by electric sparks, providing the mixture (static, homogeneous) has a stoichiometric composition. Rich and lean mixtures (turbulent) require over 3 mJ. This amount of energy is but a fraction of the total energy contained in the ignition spark, the ignition energy.

If insufficient ignition energy is available, ignition does not occur; the mixture cannot ignite and there are combustion misses. This is why adequate ignition energy must be provided to ensure that, even under worst-case external conditions, the air-fuel mixture always ingnites It may suffice for a small cloud of explosive mixture to move past the spark. The cloud of mixture ignites and, in turn, ignites the rest of the mixture in the cylinder, thus initiating fuel combusion.

4.2.6 INFLUENCES ON IGNITION CHARACTERISTICS:

Good induction and easy access of the mixture to the ignition spark improve the ignition characteristics as do long spark duration and great spark length or large

electrode gap. Intense turbulence of the mixture also has a similarly favourable effect providing that adequate energy is available. The spark position and spark length are determined by the dimensions of the spark plug. The spark duration is determined by the type and design of ignition system and the instantaneous ignition conditions. The spark position and accessibility of the mixture to the spark plug influence the exhaust gas, particularly in the idle range.

Particularly high ignition energy and a long spark duration are favourable in the case of lean mixtures. This can be demonstrated by way of example on an engine at idele. During idele, the mixture may be very inhomogeneous. Valve overlap results in a high residual gas component.

If we compare a normal breaker-triggered coil ignition system and a high energy transistorized ignition system, we can see that the spark of the transistorized ignitoin system clearly reduces and stabilizes HC emission. Smooth running of he engine is also stabilized at the same time.

Fouling of the spark plug is also an important factor. It spark plugs are heavily fouled, energy is discharged from the ignition coil via the spark-plug shunt path during the period in which the high tension is being built up. This

shortens the spark duration, thus affecting the exhaust gas and, in critical cases (if the spark plugs are badly fouled or wet) may result in complete misfiring. A certain amount of misfiring is normally not noticed by the driver but does result in higher fuel consumption and may damage the catalytic converter.

4.2.7 POLLUTANT EMISSION :

The ignition angle $_z$ or the ignition point has an important influence on the exhaust gas values, the torque, the fuel consumption and the driveability of the spark ignition engine. The most important pollutants in the exhaust gas are the unbuned hydrocarbons (HC), oxides of nitrogen (NO_x) and carbon monoxide (CO).

The emission of unburned hydrocarbons increases with more advanced ignition. NO_x emission increases with more advanced ignition in the entire air-fuel ratio range. The reason for this is the rise in combustion chamber temperature together with increasing ignition advance.

CO emission is practically independent of the ignition point and is virtually exclusively a function of the air fuel ratio.

4.2.8 FUEL CONSUMPTION :

The influence of the ignition point on fuel consumption conflicts with the influence on pollutant emission. With increasing excess-air factor , ignition must occur earlier in order to compensate for the lower combustion rate and thus maintain an optimum combustion process. Thus, an advanced ignition point means lower fuel consumption and high torque but only if the mixture is controlled accordingly.

4.2.9 KNOCKING TENDENCY :

One further important interrelationship is that between ignition point and the tendency of the engine to knock This is demostrated by way of the effect of a too early or too late ignition point (by comparison with the correct ignition point) on the pressure in the combustion chamber If the ignition point is too early, mixture at various points in the combustion chamber also ignites owing to the ignition pressure wave. This means that the mixture burns irregularly and intense pressure fluctuations occur with high . combustion pressure peaks. This effect, called knocking, can be heard clearly at low engine speeds. At high engine speeds, the noise is smothered by the engine

noise. But it is precisely in this range that knocking may lead to engine damage and it must thus be avoided by finding an optimum combination of suitable fuel and ignition point.

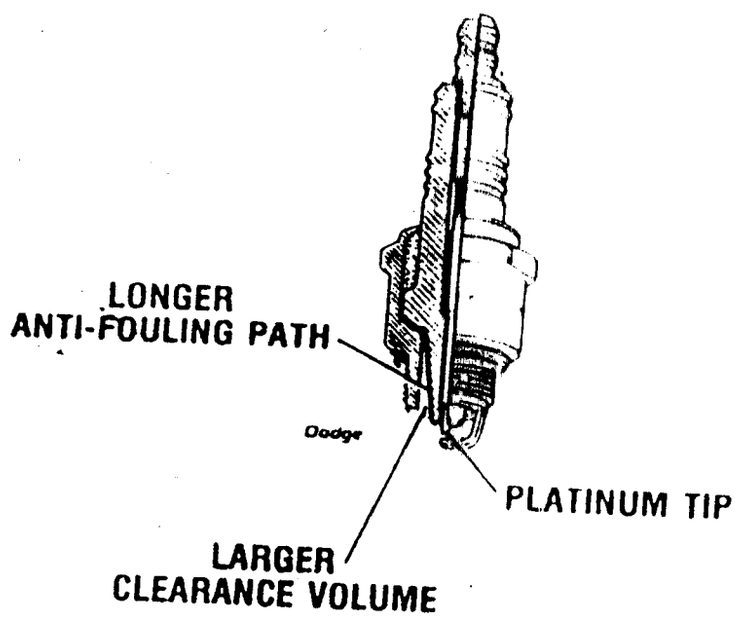
4.3 SPARK PLUGS :

The spark plug in a spark ignition engine provides the gap across which the high tension voltage jumps, to create the spark that ignites the compressed air-fuel mixture.

The spark plug consists of a centre electrode, which is connected to the ignition coil secondary through the distributor. The center electrode is insulated from the spark plug shell by means of a moulded insulator resembling porcelain. The side electrode protrudes from the bottom edge of the spark plug shell. It is positioned so that there is a gap between it and the center electrode.

The spark plug gap is adjusted by bending the side electrode.

Spark plug gaps (U.S. engines) range from approximately 0.020 to 0.080 in (0.501 to 2.032 mm). The gap must be carefully set in accordance with the manufacturer's specification. The size of the gap is dependent on the compression ratio of the engine, and on characteristics of


LONGER
ANTI-FOULING PATH
Dodge
PLATINUM TIP
LARGER
CLEARANCE VOLUME

the combustion chambers and ignition system. The trend toward wider spark plug gaps was made possible by improved ignition systems.

Once, a 0.25 in (0.635 mm) gap was virtually standard on all engines. Today, however, manufacturers specify gaps of 0.030, 0.035, 0.060 and 0.080 in (o.762, 0.890, 1.52 and 2.03 mm) A wider gap includes more air fuel mixture than an narrow gap, so there is more opportunity to ignite it.

The shell of the spark plug is threaded, so it can be removed and reinstalled with ease. All but tapered seat plugs require a gasket. The following thread sizes are used : 10 mm, 14 mm, and 18 mm.

In addition to having the correct size thread, the spark plug must extend into the combustion chamber the correct amount (reach). The correct point for the spark plug electrodes in the combustion chamber is determined by the engine engineer.

Installing plugs with a longer reach than specified may result in the valves or piston striking the spark plug. If a plug with a short reach is installed, the electrodes become partly sheltered by the spark plug hole in he

cylinder head. In this case, engine roughness and missing probably will result.

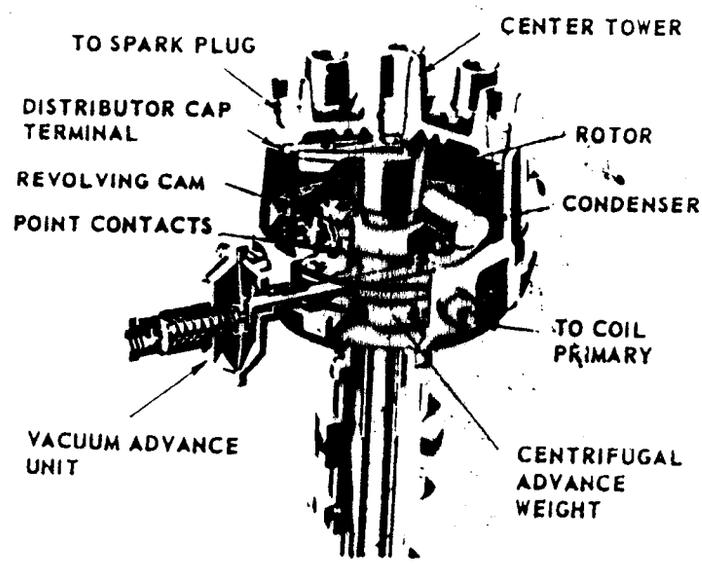
4.4. IGNITION COIL

4.4.1.CONSTRUCTION :

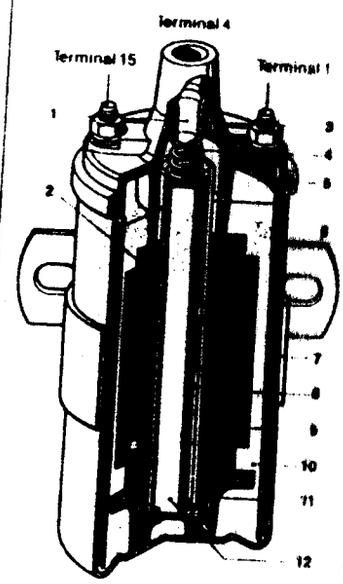
The ignition coil consists of a metal housing which accommodates metal plate jackets for reducing stray magnetic fields. The secondary winding is wound directly onto the laminated iron core and connected electrically to the center tower in the cap of the ignition coil via the core. Since the high tension is applied to the iron core, the core must be insulated by the cap and an additional insulator inserted in the base. The primary winding is located near to the outside around the secondary winding.

The insulated ignition coil cap contains the terminals 15 and 1 for the battery voltage and the connection to the contact breaker, symmetrically with the high-tension tower, terminal 4. The windings are insulated and mechanically locked in position by potting with asphalt. Oil-filled ignition coils are also available.

Fig. 35-3. Sectional view of an ignition distributor for a V-8 engine.



4) Section through an ignition coil.
1 High tension connection on the outside
2 Winding layers with insulating paper,
3 Insulating cap, 4 High tension connection on the inside via spring contact, 5 Case, 6 Mounting bracket, 7 Metal plate jacketing (magnetic)
8 Primary winding, 9 Secondary winding
10 Sealing compound, 11 Insulator, 12 Iron core



The power loss occurs chiefly in the primary winding The heat is dissipated through the metal plate jackets to the can. This is why the ignition coil is secured to the bodywork with such a wide clamp so that as much heat as possible is dissipated via this metal band.

4.4.2 FUNCTION :

The primary current which is switched on and off by the ignition distributor flows through the primary widing of the ignition coil. The magnitude of the current is determined by the battery voltage at terminal 15 and the ohmic resistance of the primary winding. The primary resistance may lie between 0.2 and 3 ohms, dependent upon use of the ignition coil. The primary inductance L_1 is a few mH. The following formula applies to the energy stored in the magnetic field of the ignitin coil

$$W_{sp} = 1/2\ L_1 \cdot i^2_1$$

W_{sp} stored energy, L_1 inductance of the primary winding, i_1 current wihch flows in the ignition distributor at the moment at which the contact breaker opens.

At the ignition point, the voltage at terminal 4 (high-tension tower of the ignition coil) rises approximately sinusoidally. the rate of rise is determined by the capacitive load at terminal 4. When the breakdown voltage at the spark plug is reached, the voltage drops to the spark voltage of the spark plug and the energy stored in the ignition coil flows to the ignition spark. As soon as the energy no longer suffices to maintain the glow discharge, the spark breaks down and the remaining energy decays in the secondary circuit of the ignition coil.

The high tension is polarized such that the center electrode of the spark plug is negative with respect to the vehicle chassis or ground. If the polarity were the reverse, this would mean a slightly higher required voltage. The ignition coil is desigined as an auto-transformer such that the secondary side is connected to terminal 1 to 15.

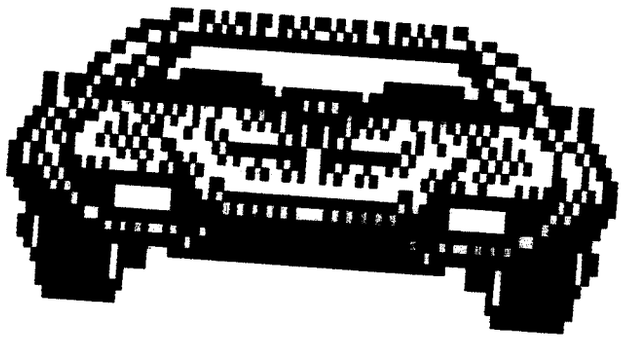
In the same way as the primary inductance and the primary resistance determine the stored energy, the secondary inductance determines the high tension and spark characteristic. A typical turns-ratio of primary to secondary windings is 1 : 100. The induced voltage, the spark current and the spark duration are dependent upon both the stored energy and the secondary inductance.

4.4.3 CONTACT BREAKER :

The contact breaker is controlled via the breaker cam which has as many lobes as the number of cylinders in the engine. The breaker cam can be turned on the ignition distributor shaft; it is adjusted dependent upon the engine speed. dependent ignition timing adjustment input from the centrifugal advance mechanism. The cam is configured such that there results a dwell angle corresponding to the ignition coil and the sparking rate.

Thus, the dwell angle is permanently preset for a breaker tirggered ignition system and is invariable throughout the entire engine speed range. However the dwell angle does change throughout the service life of the engine owing to wear of the cam follower on the breaker lever. The abrasion which is thus produced means that the contact breaker opens at a later point. The resultant ignition retard generally results in higher fuel consumption. This is one of the reasons why the contact breaker needs to be renewed regularly and the dwell angle checked. Another reason why maintenance is required is contact erosion (pitting). The contact must switch currents of up to 5 A and break voltages of up to 500 V. On a 4-cylinder engine with an engine speed of 6000 min^{-1} the contact switches 12.

000 times per minute, this corresponding to a frequency of 200 Hz. Defective contacts mean inadequate charging of the ignition coil. Undefined ignition points and, thus, higher fuel consumption and poorer exhaust-gas values.



FUNCTIONAL DESCRIPTION OF THE PROJECT BLOCK DIAGRAM

V. FUNCTIONAL DESCRIPTION OF THE PROJECT BLOCK DIAGRAM

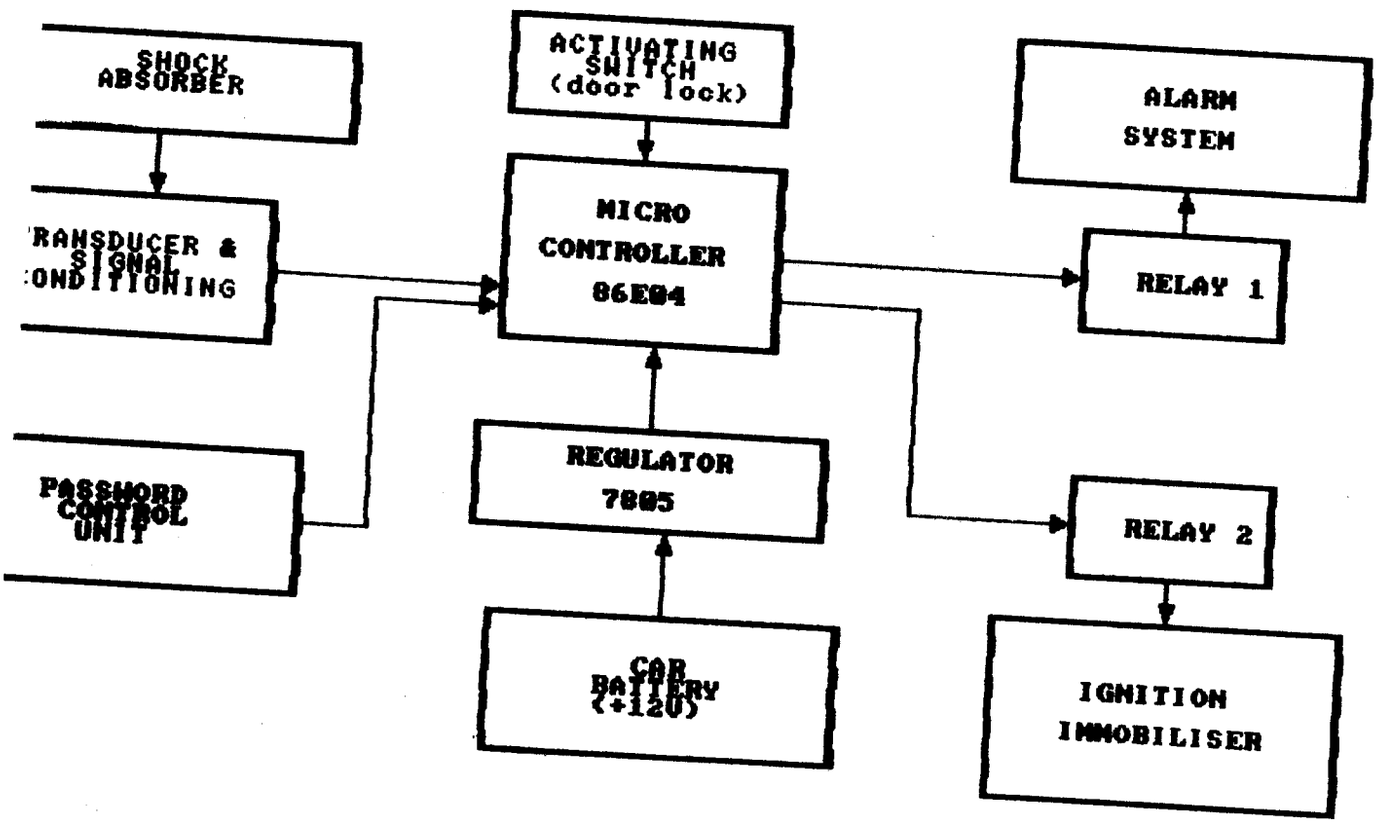
5.1. DESCRIPTION OF INDIVIDUAL BLOCKS

The system operation is described as various blocks.

5.1.1 SHOCK ABSORBER:

The various types of shock absorbers have already been dealt with in the previous chapter. Due to the high sensitivity of the shock absorber, the transducer is placed in the shock absorber. Though there are four shock absorbers above all the 4 wheels, the transudcer is placed in the shock absorber which is below the driver's seat. The reason for this is that it is this shock absorber which will come into play for maximum theft conditions. It is to be noted that even if there is a pressure given at the back of the car, the driver seat shock absorber will be affected. The reason for choosing shock absorber for our system is due to its versatality in sensing any minute movement in any part of the car, especially while towing.

HARDWARE BLOCK DIAGRAM



5.1.2 TRANSDUCER :

The pressure transducer used here is a gauge or differential package transducer. It is based around a power active element piezo resistive bridge construction which has been laser trimmed to enhance device performance. The gauge sensors use atmospheric pressure as a reference whereas the differential sensors will accept two independent pressure sources simultaneously.

Gauge style - In this mode, pressure is applied to port P2 and port P1 vents to ambient pressure. Pin1 is notched and is shown at the right of the package. Pin2 is next to pin1

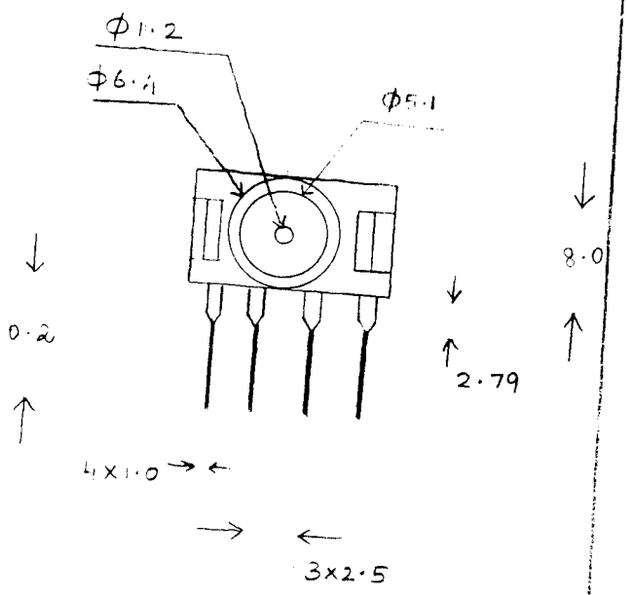
Differential Style - Port1 is near terminals.

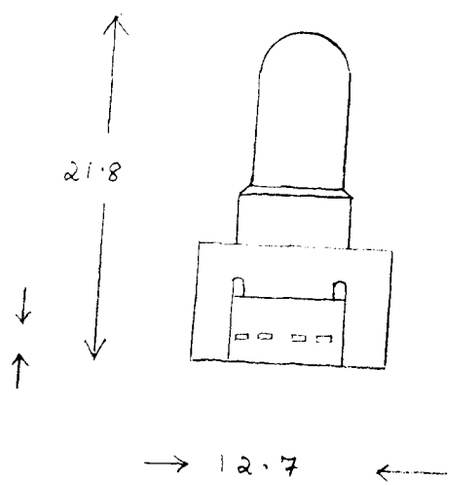
Electrical connections for the two modes is shown in the figure

Note :

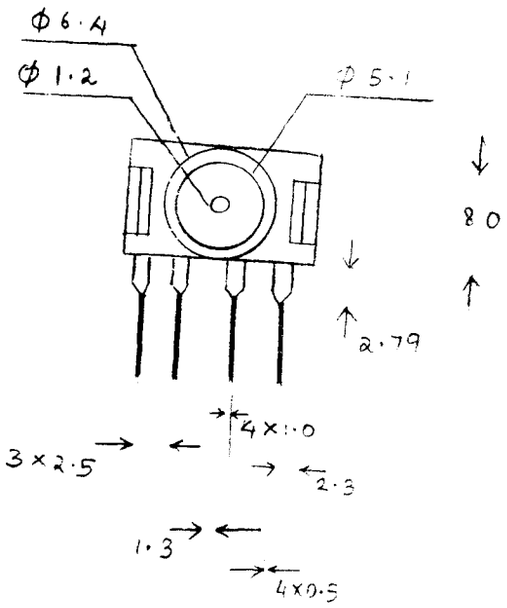
1. Circled numbers refer to sensor terminals
2. Vo changes with pressure change Terminals

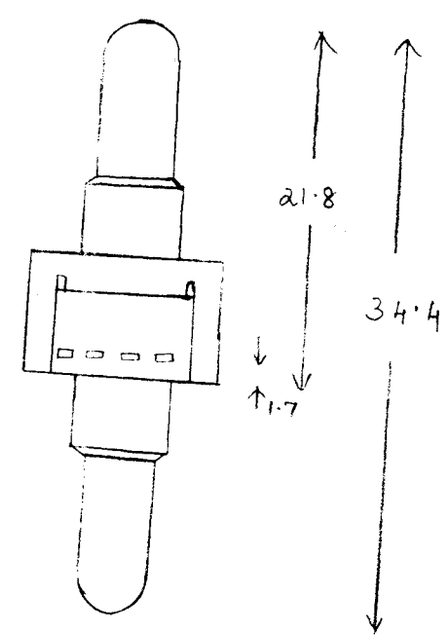
GAUGE STYLE

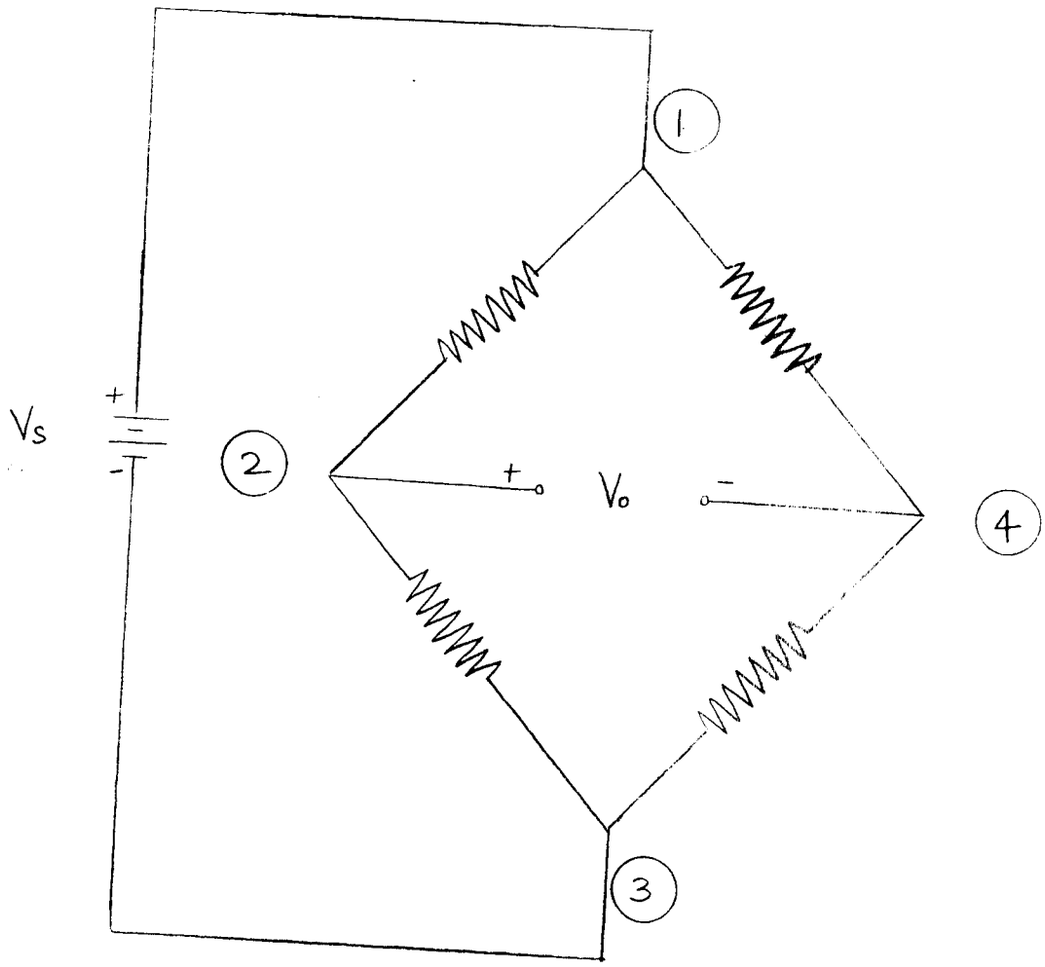




DIFFERENTIAL STYLE







ELECTRICAL CONNECTIONS

Gauge Style

Differential Style

Technical specification

	RS stock no. 286-658			RS stock no. 286-664			RS stock no. 286-670			RS stock no. 286-686			RS stock no. 286-692			RS stock no. 286-709			
Parameter	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Units**
Pressure range		0-5			0-15			0-30			0-5			0-15			0-30		psi
FSO (Full scale output) P2>P1	47	50	53	97	100	103	97	100	103	47	50	53	97	100	103	97	100	103	mV
Null offset	-1.5	0	+1.5	+1.5	0	+1.5	-1.5	0	+1.5	-1.5	0	+1.5	-1.5	0	+1.5	-1.5	0	+1.5	mV
Sensitivity		10			6.67			3.33			10			6.67			3.33		mV/psi
overpressure			20			45			60			20			45			60	psi
Response time			1.0			1.0			1.0			1.0			1.0			1.0	ms
Recommended excitation voltage		10	16		10	16		10	16		10	16		10	16		10	16	=
Linearity (best fit straight line) P2>P1			±1			±1			±1			+1			±1			±1	%FSO
Temperature error 0°C +50°C																			
Sensitivity shift			±1			±1			±1			±1			±1			±1	%FSO
Null shift			±1			±1			±1			±1			±1			±1	mV
Repeatability and hysteresis		±0.2			±0.2			±0.2			±0.2			±0.2			±0.2		%FSO
Stability over 1 year		±0.5			±0.5			±0.5			±0.5			±0.5			±0.5		%FSO
Input resistance		7.5k			7.5k			7.5k			7.5k			7.5k			7.5k		Ω

1. Pin 1 = V_S (+)
2. Pin 2 = Output (+)
3. Pin 3 = Ground (-)
4. Pin 4 = Output (-)

Pin 1 is notched, cabeled on plastic Pin 2 is next to pin 1

5.1.3 MICROCONTROLLER :

The microcontroller is the heart of the system. The input to the microcontroller is the output of the transducer and the password.

The system gets activated when the car door is locked. The output of the transducer at that instant is converted to digital value and then stored at a particular register. The tolerance value which is got after practical consideratins is added to the value in this register. This becomes the reference value.

Similarly the password is sent through 8 lines. This is multiplexed for the sake of convenience. This password is stored in two registers ie., the lower half in one register and the upper half in another. These two are "or"ed and stored in another register.

When a thief tries to break into the car, there will be some movement in the shock absorber and subsequently the output of the pressure transducer will change. Once the change in transducer output is detected, a timer waits for 10 sec for the correct password to be keyed in. After this delay, if the password is not entered, then the alarm begins to sound and the ignition is immobilised.

If the correct password is given within the delay time, he system accepts it and the car resumes ot its normal state.

NOTE:

The system gets activated when the door is locked and it gets deactivated only when the correct password is given.

5.1.4. PASSWORD CONTROL :

The password control board, which can be a keypad is held as a separate unit. The password can be entered by plugging this unit into the socket provided in the dashboard. The password entered before the system gets "ON" is held in a buffer. When the door is locked, the system gets "ON" and the password in the buffer is moved into a register.

Again after sometime when the owner returns to the car, he opens the door. At this moment a delay of 10 sec starts. Now the owner has to get into the car, plug in the unit and then enter the passwword within the delay time. Now if this password matches the one that is already stored inthe register, the system gets deactivated. Or else the alarm sounds.

The aim of having this as a separate unit is so that the thief doesn't have an input unit to key in the password or to even have a try. This is optional. If the owner finds this arrangement to be of nuisance value, he can leave this unit permanently connected to the socket inside the car.

5.1.5. **BATTERY** :

Basically the car battery is designed for a 12 V supply. As most of the digital IC's used work only with 5 V supply we go in for a regulator. For this particular system no special battery system is needed apart from the regular battery. Supply can be drawn directly from the distributor. But proper care should be taken to note that the batteries are charged fully since in case of failure of the battery system the entire alarm system will be disabled. Hence some servicing techniques and charging procedures should be

software is to be effective in execution and concise in size. It can be seen that this software has achieved both these objectives.

The software has been written considering all possible loop holes which a burglar might think, so that any possibility of arriving at the correct password by mere guess work is totally avoided. Thus we can see that the system is quite fool proof.

The possibility of losing data in RAM due to any powersurges may cause the password to vanish. In such emergencies a default routine takes control of the system. Techniques like vector manipulations, masking of interrupt registers etc have been employed, thus increasing the efficiency of the program.

7.4. EMULATOR CONCEPTS

7.4.1. INTRODUCTION :

The Z86E04 and Z86C19 are low cost powerful microcontrollers that embody the full core of the consumer controller processor (CCP) in a small 18-pin package. In addition to its small size, dual analog comparators, and low power. modes of operation, the watchdog timers make these products useful in many applications.

An emulator is an excellent development tool for economical code development, for reducing the expense of using one time programmable (OTP) parts during early development, and primarily for reducing risk before going to a maskable ROM part. Commercial emulators have their applications but in many instances are not required. One case where the investment in a commercial emulator is unwanted is during part evaluation and parameter testing before initial application development actually begins. The simple emulator outlined in this application note is also a sufficient development tool for applications requiring only small amounts of code.

7.4.2 CCP EMULATOR DETAILED DESCRIPTION :

The basic 18-pin CCP emulator is very simple to build and use. Its major parts are the Z86C90 ROM less CCP microprocontroller, an EEPROM, and some addess/Data demultiplexing logic. An EEPROM serves as an excellent development device with the ROM less CCP microcontroller as it allows endless versions of code checking and modification with little effort.

The complete schematic for the basic low cost Z8 MCU emulator is show in the figure. The pin outs of the

components shown are for Dual in LIne package (DIP) parts. This circuit configuration provides the user with the most basic real time hardware emulation capability. To maximize the ease of use, a Zero insertion force (ZIF) socket should be used for the EEPROM. The core building block can be enhanced in a number of different ways to provide the user with an emulator that can be tailored to the specific needs of the user.

7.4.3. OSCILLATOR AND POWER CONSIDERATIONS :

The schematic diagram shown in figure assumes that a ceramic resonator or crystal is being used as a clocking source for the microcontroller. Note, the source should be directly applied to the Z86C90. This provides a more accurate representation of the oscillator performance than the allternative method of pumping the clocking signals through a cable, via the socketing connector, to the Z86C90. There are two significant reasons for this. First, the cable adds a significant capacitive load to these signals. Secondly because the clock is the highest frequency signal, it is more susceptible to distortion and noise.

The emulator consumes more power than the target microcontroller. As a result, basic power distribution and filtering rules apply to the emulator power source. It is recommended that the same power source use the targeted microcontroller and the emulator rather than using a separate isolated supply. The schematic accounts for 0.1 Uf capacitors placed near the VCC pins of each of the active devices. A 10Uf capacitor is placed near the emulator input power source.

7.4.5. MULTIPLEXED ADDRESS/DATA LOGIC :

For this emulator application, Port 1 of the Z86C90 is configured as a multiplexed address/data bus, and port 0 is configured as the upper portion of the address bus. This gives the emulator the capability of addressing more than the 4 k of ROM memory limit imposed by the Z86C19. The EEPROM (Xicor X2864B-18) is an 8 K x 8 device that allows twice the program storage memory of the Z86C19 and four times the storage of the Z86C09. This extra memory is useful for patching the code under development. Extra memory allows the programmer to concentrate on code development as a primary concern, and then code optimization and "squeezing" can be a secondary concern.

Because the address and data buses of the Z86C90 are multiplexed, they are separated for accessing program memory. The Z86C90 makes this task easy by supplying the /AS (Address strobe - active low) and the /DS (Data Strobe - active low) signals. An inverted / AS signal is used by the transparent latches to hold the address / data for the EEPROM. The / DS signal is used as on output enable (/OE - active low) for the EEPROM to place the program data on the multiplexed addressdata bus. A timing diagram of the program memory access is shown in figure. Note that the usage of program memory is always a read operation by the Z86C90 when emulating the Z86E04/19.

7.4.6 SPECIAL PROGRAMMING

There are a few programming considerations when using the Z86C90 to emulate the X86E04/19. First the Z86C90 has 236 General purpose registers (R4-R239) while the Z86E04/19 is limited to 124 General purpose register (R4-R127).

In addition to the number of general purpose registers available to the user, there are also some differences in the control and status registers (R240-R255) between the devices. The first of these differences occurs in the Watchdog Timer Mode Register [WTMR - extended register % (F)

OF]. The differences occur if you program bit D4 of this register to select the XTAL option as the watchdog timer driving source (D4-1). By using the on chip RC circuit (the default condition) there are no differences in the watchdog timer activation periods. The differences in the watchdog timer activation period between the devices when the crystal option is selected is outlined in Table 2.

Take care when programming from the port 3 mode register (R2247 p3m) to properly emulate the Z86E04/19 bits D7:D2 must be programmed as all zeros. This sets P31, P32 and P33 as inputs ; P34, P35 and P36 as outputs. Bits D7:D2 are reserved in the Z86E04/19, so setting these bits to) will have no effect.

The port 0 and Port 1 mode register (R248 P01M) is one register that must be programmed differently between the devices. To properly emulate the Z86E04/19, the POIM register of the Z86E90 is set to 96 H. However bit D4 of Z86E04/19 must be set to zero. The remaining bits of the POIM register in the Z86E04/19 are reserved and should be programmed as all zeros. It is important that these differences are remembered when converting the code from one processor to the other.

The RAM protect option of the Z86C90 (R251 - 1MR bit D6) should be enabled. This bit should be programmed as a 0 for both types of devices.

7.4.7 ADDITIONAL ENHANCEMENTS

Additonal EEPROM (or other) memory is supported by using the unused latched address lines, a 3 : 8 demultiplexer, and the /CE inputs of the EEPROMS. A full 64 K of memory is accessed using the schematic. Because addtional circuitry is being added there is an additional time delay in data availability. The maximum specified value, from/DS going active to data required by the Z86C9012, is 130 ns. A faster EEPROM (Xicor X2864B-12) may be required. This depends on the clock speeds being used in the application.

By adding some RAM and setting bit D2 of register 248 to a one, an external stack can be added. This is useful for debugging applications that are interrupt intensive Register 254 and 255 are programmed to map into the appropriate RAM space.

Additional memory is not the only useful enhancement. Other useful features include single stepping, break points,

real time traces, and adding a direct computer link. Unfortunately the Z86C90 is not the perfect in Circuit Emulator (ICE) chip, and adding single stepping and break points is not done easily. This is where the commercial emulators come in. However, adding real time trace capability and an external computer link are possible.

A real time trace is achieved by storing the latched addess information and EEPROM data. These values are stored at the rising edges of /AS and /DS. The user then designs circuitry control of the trace (turn on, turn off, stop when full, overwrite, etc.)

Adding a computer link is probably the most challenging task, and for those who do not like removing the EEPROM and placing it in a programmer device it is a useful enchancment. Also it controls other enchancements like the trace function and can report the contents of an external stack. A logical candidate for this application is the Z86C91. The UART on this microcontroller can be used to execute an RS-232 interface. The design rules for the Z86C91 are the same as those outlined for the Z86C90, so half of the design is already complete.

Table 1.

Emulator EEPROM Timing Parameters

No.	Parameter	Min	Max
1	Address valid to /AS high delay	35	
2	Address float to /DS active delay	0	
3	/AS inactive to /DS active	65	
4	/DS active to EEPROM data valid delay		100
5	MCU address valid to EEPROM address valid		44
6	EEPROM address valid to EEPROM valid data		180
7	/AS inactive to DAta input required		250
8	/DS active to data input required		130
9	Data input setup time to /DS inactive	75	
10	Data input hold time to /DS inactive	0	
11	/DS inactive to EEPROM data float	0	50
12	/DS inactive to MCU address valid	65	

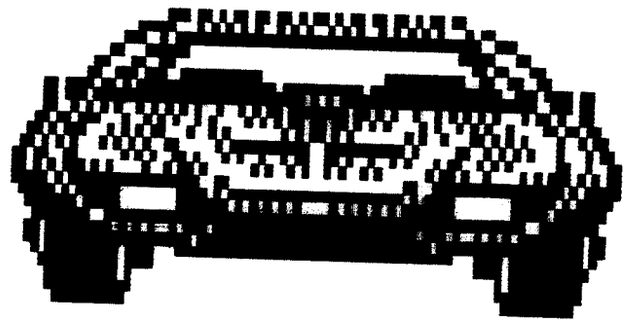
Table 2.

WDTMR XTAL Differences

D1	D0	XTAL 1 Timeout	
		Z86E04/19	Z86C90
0	0	XTAL 1/512	XTAL 1/256
0	1	XTAL 1/1024	XTAL 1/512
1	0	XTAL 1/2048	XTAL 1/1024
1	1	XTAL 1/8192	XTAL 1/4096

7.4.8 CONCLUSION

The Z8 microcontroller family is very powerful. The CCP series offers very cost effective solutions for consumer and automotive applications. Emulating these devices is simple and cost effective plus it provides keen insight into their specific uses.



SYSTEM RELIABILITY

VIII. SYSTEM RELIABILITY

The system which has been designed now has the following advantages:

* Cost effectiveness
* High efficiency of operation
* Maximum reliability
* Easy user access

Of the above advantages, system reliability is the important criteria as far as this particular product is concerned. Hence let us look in to the important aspects as for as reliability is conerned.

Speaking about the reliability of the system, the system is definitely reliable especially in comparison with the very many other anti-theft products existing in the market. The reason is due to its versatility. The system is reliable against the following cases;

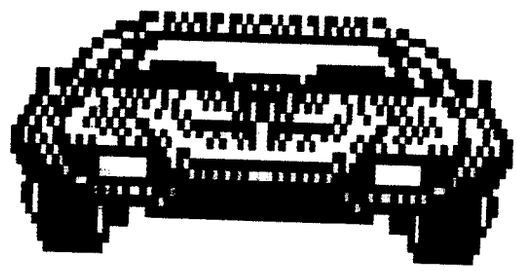
* No one can easily enter the car and even in case of entry, he will be scared by the alarm system after a delay of 10 secs.

* Also the password control would be in a handy package which only the owner can use for that particular unit in use ,as we have locks and keys with specific numbers.

* Even in case if the thief manages to get a duplicate hand set, the probability of him to get the right password is very less , since we may adopt a keypad which has nearly infinite number of combinations.

* In case of flats type of residence only very limited number of tenants would have an opportunity to park their vehicles within their compound. Others usually park it outside, which makes the burglar easy to tow it away using a mini- crane system. This particular system is very reliable against theft by towing, because the transducer used is sensitive towards bi-directional motion.

As a jist it can be said that, the entire system is cent percent reliable and can be used with ease and comfort.



USER'S MANUAL

IX. USER'S MANUAL

To enable the owner to have an easy access to this system a simple procedure would be of great help.

The DO's and DONT's of the system are depicted below:

DO's :

* Just before leaving the car, make it a point to give the latest password you wish and get out of the vehicle.
* Ensure that the wiring system from the doorlock is always proper and is not open.
* Check the shock absorbers now and then and see that you replace them when they become very weak.
* Ensure that you make no mistake in entering the password within 10 secs at any cause.
* Check the battery systems now and then to avoid passive system response.
* Have auxillary charge devices for emergency needs.

* Design a parallel alarm system, say the horn itself in case of the system alarm failure, using your local electrician.

* Check the package of the unit if it were sealed.

DONT's :

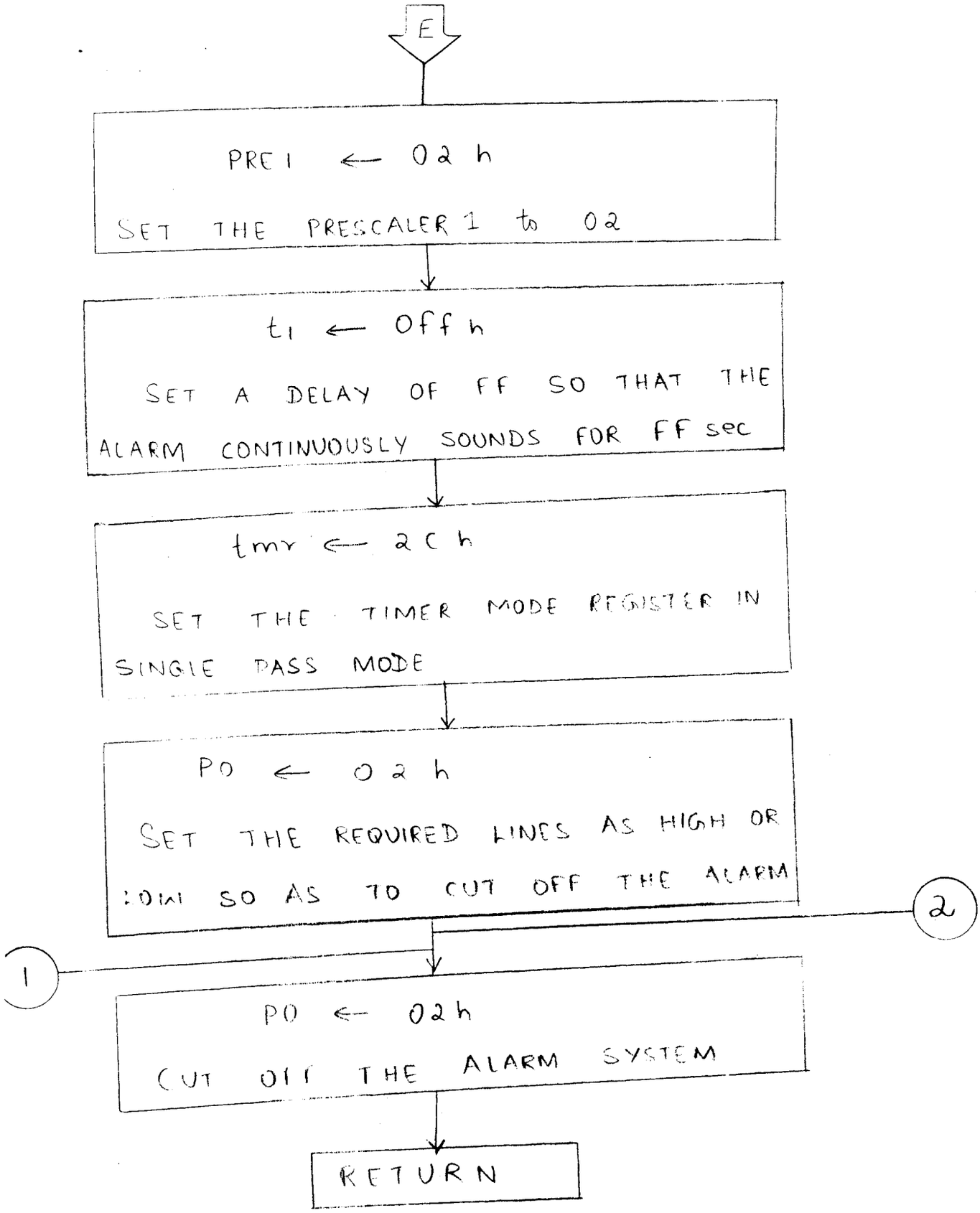
* Do not pick up a conversation with any one outside the car during the 10 sec delay time and end up in a embarassing situation with the alarm yelling in your own presence.

* Do not forget to give a new password before you leave the car to avoid confusion.

* Do not forget your password otherwise you might end up in trouble.

* Do not enter the password in the presence of strangers.

* Do not forget to cut-off the alarm by giving the password again after 5 minutes from the sounding of the alarm.


E
PRE 1 ← 02 h
SET THE PRESCALER 1 to 02
t1 ← Off h
SET A DELAY OF FF SO THAT THE ALARM CONTINUOUSLY SOUNDS FOR FF sec
tmr ← 2C h
SET THE TIMER MODE REGISTER IN SINGLE PASS MODE
P0 ← 02 h
SET THE REQUIRED LINES AS HIGH OR LOW SO AS TO CUT OFF THE ALARM
2
1
P0 ← 02h
CUT OFF THE ALARM SYSTEM
RETURN

VI. DESIGN OF SYSTEM HARDWARE

6.1. HARDWARE CIRCUIT DESCRIPTION

The hardware circuit diagram shown clearly depicts the entire system in a jist. Let us precisely explain the important features of the hardware in use.

6.1.1 FEATURES OF Z8-8604 :

The salient features of the microcontroller 8604 (Zilog) has been clearly described in the appendix.

The chip has 3 ports in it. Port 0 is an output port. Port .2 is an I/O port & port 3 is an input port and is strictly an analog input port. The reason for going into zilog family is that they are generally very much cost effective and highly reliable. Along with that they are loaded with highly efficient instruction set. This particular chip has been specially designed for a new level of sophistication to single chip architecture. The chip falls into Z8 single chip microcontroller family with 1 KB of 1-time PROM and falls under CMOS technology. These devices allow easy software development and debug, prototyping and small production runs not uneconomically desirable with a masked ROM version.

They have a flexible I/O scheme, an efficient register and address structure. Usually the lines in this chip are grouped in to three ports and are configurable under software control to provide I/O timing and status signals. There are two basic address spaces available and 124 bytes of general purpose registers. They offer progammable EPROM protect and programmable lownoise.

6.1.2 ACTIVATING SWITCH :

An activating switch for tamper proof operation is kept at the door lock. The output of the switch is connected to Port 0 of the microcontroller. The switch is strictly a one way switch, once triggered would make the system completely "ON" and the system can be switched "OFF" only if the right password is entered. Opening of the lock would not disable the system .

6.1.3 DIP SWITCH :

Password control is done with the help of software manipulations and DIP switch. Initialy first four bits are considered and later the next four bits on the input side. This is done by making use of two control signals. According to the combination ofthe DIP switch the multiplexed data is stored in two registers.

Later when the owner enters the car after opening the door , he should give the password within the allowed delay of 10 seconds.In case of a true password the relays would be cut-off and hence the alarm would not sound and the immmobiliser would not work.

In case of a false password the system would give a huge alarm, capturing the attention of the public and the immobiliser circuit would be in action disenabling the thief to move the vehicle. This is the salient feature of this system design.

6.1.4 R-2R LADDER NETWORK :

This is basically a resistor circuit connected in a ladder form performing digital to analog conversion. The input to the lader network is from port 2 of the microcontroller. The output of the network would be an analog signal. It will be compared with the transducer output which is also an analog signal. The inputs to ladder network is incremented and the above operation is repeated until the output of the comparator is zero. The current digital input to the ladder network is stroed in a register which becomes the reference value.

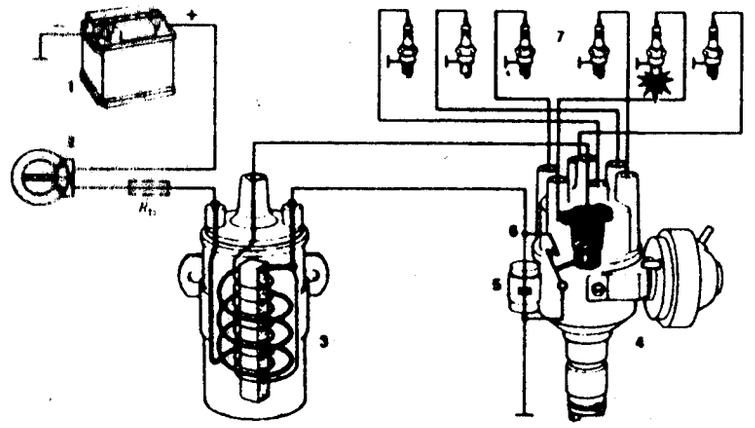
6.1.5 REGULATOR :

A commonly used 7805 regulator as explained before is used which has an output of 5 V and used to energise the microcontroller as well as to give the DIP switch a proper combination to form a password.

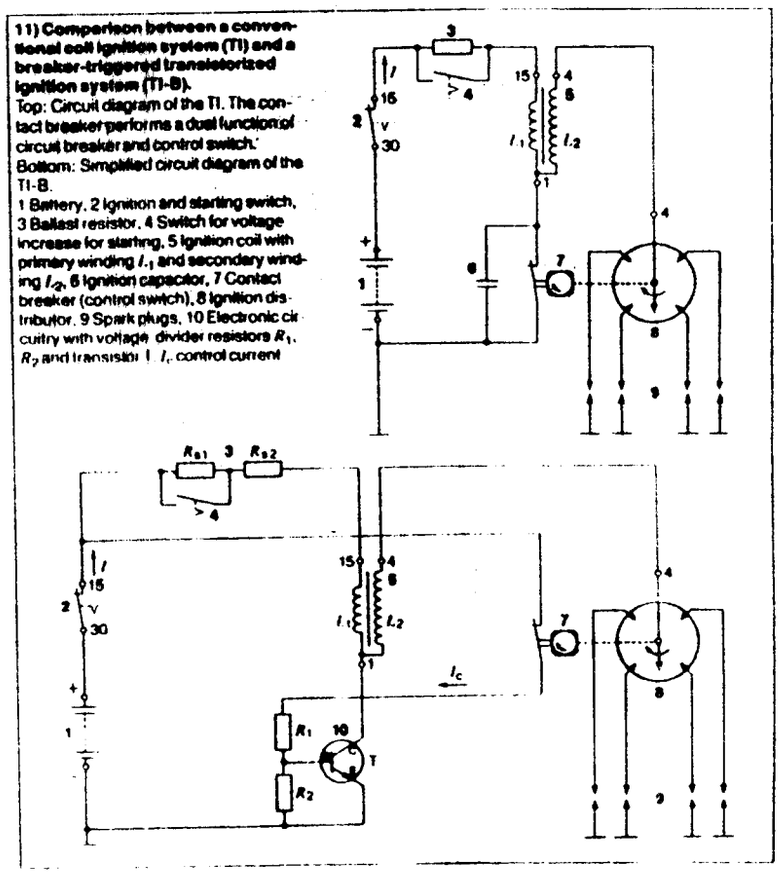
6.2 IGNITION IMMOBILISATION SYSTEM:

The ignition distributor of the breaker-triggered transistorized ignition system (TI-B) is identical to the ignition distrbutor of the breaker - triggered coil ignition system (SI). However since the contact operates in conjucntion with a transistorized ignition system, the contact breaker no longer needs to switch the primary current for the transistorized ignition system. The transistorized ignitions system itself playsthe role of current amplifier and switches the primary current via an ignition transistor (generally a Darliginton transistor). In order to facilitate understaindg, the wiring of the contanct and the function of simple TI-B are compared below to a breaker-triggered coil ignition system.

2) Ignition system with conventional coil ignition.
1 Battery, 2 Ignition and starting switch, 3 Ignition coil, 4 Ignition distributor, 5 Ignition capacitor, 6 Contact breaker, 7 Spark plugs, R_v ballast resistor for boosting the starting voltage (not always fitted)



11) Comparison between a conventional coil ignition system (TI) and a breaker-triggered transistorized ignition system (TI-B).
Top: Circuit diagram of the TI. The contact breaker performs a dual function of circuit breaker and control switch.
Bottom: Simplified circuit diagram of the TI-B.
1 Battery, 2 Ignition and starting switch, 3 Ballast resistor, 4 Switch for voltage increase for starting, 5 Ignition coil with primary winding I_1 and secondary winding I_2, 6 Ignition capacitor, 7 Contact breaker (control switch), 8 Ignition distributor, 9 Spark plugs, 10 Electronic circuitry with voltage divider resistors R_1, R_2 and transistor T, I_c control current



6.2.1 OPERATING PRINCIPLE :

Figure clearly shows that the breaker triggered transistorized ignition system is a further development of the conventional, non-electornic coil ignition system. The transistor T is used as the circuit breaker in place of the contact breaker and assumes its switching function in the primary circuit of the ignition system. However, since the transistor has a relay characteristic, it must be caused to switch in the same way as the relay. This can be done, for instance, as shown in Figure aa, with a control switch. Such transistorized ignition systems are thus termed breaker triggered. In Bosch transistorized ignition systems, the cam operated breaker performs the function of this control switch. When the contact is closed, a control current I_s flows to the base B and the transistor is electrically conductive between the emitter E and the collector C. In this condition, it corresponds to a switch in the "ON" position and current can flow through the primary winding I_1 of the ignition coil. However if the contact of the breaker is open no control current flows through to the base and the transistor is electrically non conductive. It thus blocks the primary current and, in this condition, corresponds to a switch in the "OFF" position.

6.2.2. ADVANTAGES :

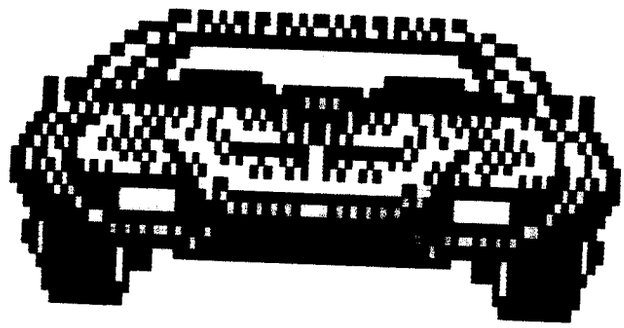
The breaker triggered transistorized ignition system has two essential advantages over the breaker triggered coil ignition system:

- An increase in the primary current and
- considerably longer service life of the contact.

The primary current can be increased if using a switching transistor since a mechanical contanct can switch currents of only up to 5 A for long periods and with the required frequency. Since the stored energy is proportional to the square of the primary current, the power of the ignition coil increases and thus also all high tension data such as secondary available voltage, spark duration and spark current. Thus a breaker triggered transistorized ignition system also requires a special ignition coil in addition to the ignition trigger box.

A far longer service life of the TI-B results from the fact that the contact breaker is not required to switch high currents. In addition, the TI-B is also not subject to two other phenomena which indefinably reduce the secondary available voltage of contact triggered coil ignition systems: contact chatter and the contact breaking spark

which results from the inductance of the ignition coil. The contact breaking spark causes the available energy to be reduced and the high-tension voltage rise to be delayed particularly at low engine speed and when starting. Conversely, contact chatter occurs at high engine speeds owing to the high switching frequency of the contact and is a disturbing influence. The contact bounces when closing and thus charges the ignition coil less intensely precisely at a point in time at which the dwell period is reduced anyway. The first negative characteristic of the contact breaker is not applicable to the breaker triggered transistorized ignition system the second is.



DESIGN OF SYSTEM SOFTWARE

VII. DESIGN OF SYSTEM SOFTWARE

7.1 SOFTWARE OVERVIEW:

The software has been written using the Assembly Language Instruction set exclusively available for Z86E04. The software plays a very major role in normal functioning of this system. Since the micro controller has only a one time programable ROM, the software was tested using an emulator. The prominant function performed by the software are;

i) Accepting the input from the transducer and comparing it with the output of DAC to generate a digital reference.

ii) To keep constant vigil over the environment and to respond to any changes effectively.

iii) To take care of all password manipulations.

iv) Appropriate triggering of alarm and immobilizer units.

The availability of flexible I/O ports and a very powerful instruction set of the microcontroller has made this system very efficient. The primary objectives of any

7.2. ALGORITHM

1. Start the program.

2. Call the subroutine "capt - passwd". The job of this routine is to multiplex port 2 and collect the pass word.

3. Call the subroutine "adc". The job of this routine is to get the digital equivalent of the analog output of the transducer.

4. Move the digital value which is in a general purpose register (GPR) compare - ram to another GPR ref.

5. Add the tolerance value to this register. This resultant value which is in GPR ref now acts as the reference value.

6. Call the subroutine "shock".

The job of this routine is to check if there is any movement in the shock. If so, the o/p of the pressure transducer will change. If there is a change, this routine will then check for the correct password and connect or disconnect the alarm accordingly.

Subroutine adc

1. Clear the General Purpose Registers over - flag and compare - ram. Over-flag register is used as a flag register to get an interrupt and thereby stop the counting sequence. Compare - ram register is used as a counter.

2. Increment the counter register.

3. Move the counter register's value to the port 2 lines.

4. Give a delay time for the transducer o/p to settle down.

5. Load the over - flag register with FFh so that when there is a change, it can be noted.

6. If the over - flag has not been set, go to step 2.

7. Or else return to the main program.

Subroutine capt - password

1. Set the port 2 mode register to 0Fh thereby making the port 2 as an input port.

2. Set the control line P24 high to get the four Most Significant Bits of the password.

3. Store the four Most Significant Bits in a register pwd high1.

4. Set the control line P25 high to get the four Least Significant Bits of the password.

5. Store the four Least Significant Bits in a register pwd low1.

6. "Or" the value in the two registers and store the "or" ed value in the pwdhigh1.

7. Set the port 2 mode register to 00h thereby making the port 2 as an output port.

8. Return to the main program.

Subroùtine shock

1. Call the subroutine "adc".

2. Move the present transducer output which is in the GPR compare - ram to another GPR current - shock.

3. Subtract the already stored reference value in register ref from this present value current shock.

4. If the resultant value is zero, go to step 1 and go through this loop again and again till there is some variation in the transducer output.

5. Set the prescaler0 to 00h and give the required delay of 10 seconds in the timer register "to".

6. Set the timer mode register to 23h thus making it to be in the single pass mode ie, it will count the required delay and then change to zero.

7. Move the already stored content of the original password which is in GPR pwdhigh1 to another GPR pwdhigh.

8. Call the subroutine "capt - password" to get the current password.

9. Move the current password to another GPR current - pw.

10. Subtract the original password from the current password.

11. If it is zero go to step 18.

12. Make the port 0 mode register as an output port.

13. Make the port 0 line going to alarm high and the ignition immobiliser low by setting the value of P0 register 01h.

14. Set the prescaler1 to 02h and give a delay of ffh in the timer register "t1".

15. Set the timer mode register in single pass mode by setting a value of 2Ch in tmr.

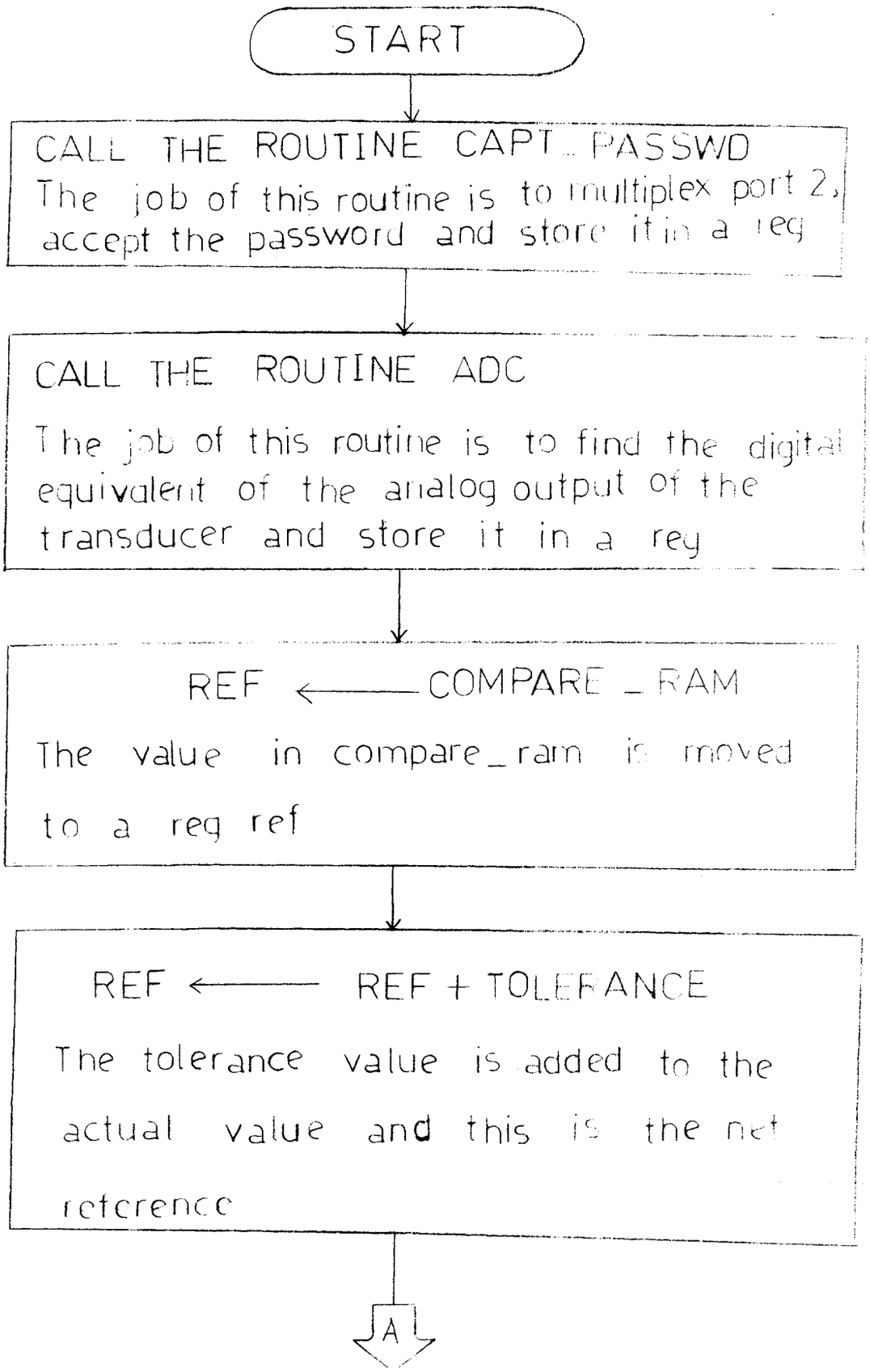
16. Make the port 0 line going to the alarm low and the immobiliser high by setting 02h to P0.

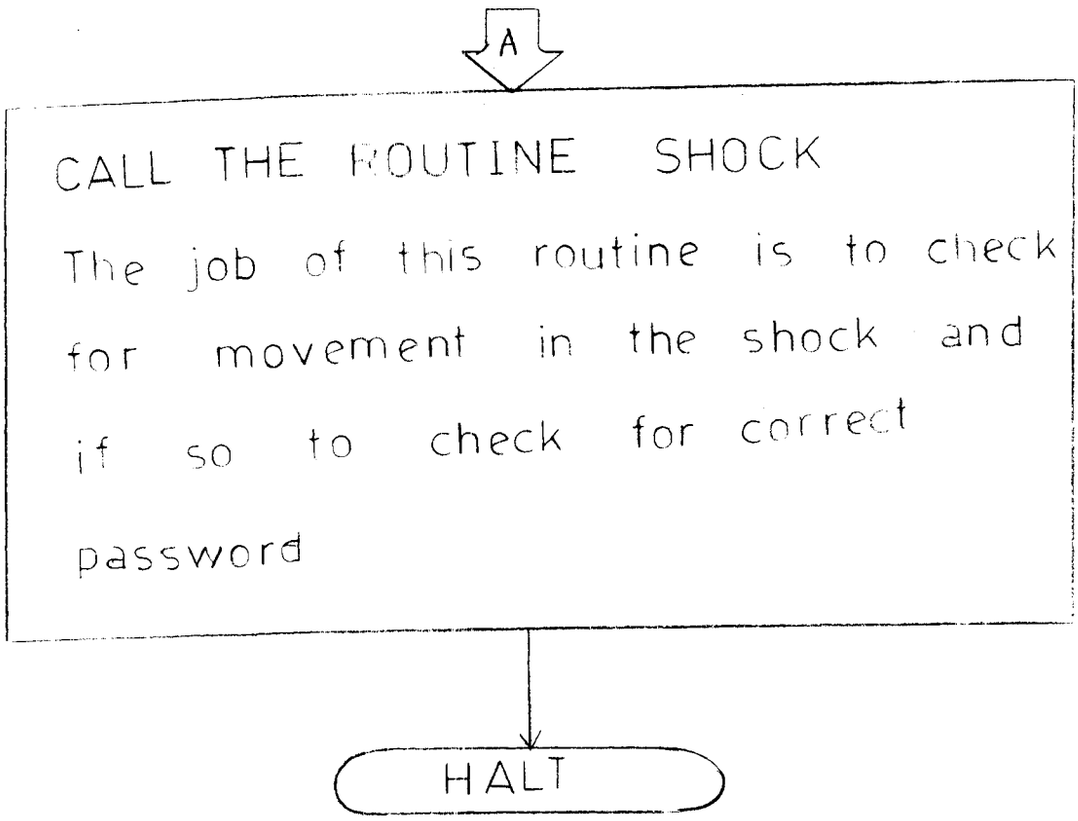
17. Jump to step 5.

18. Make the port 0 line going to the alarm low and the immobiliser high by setting 02h to P0.

19. Return to the main program.

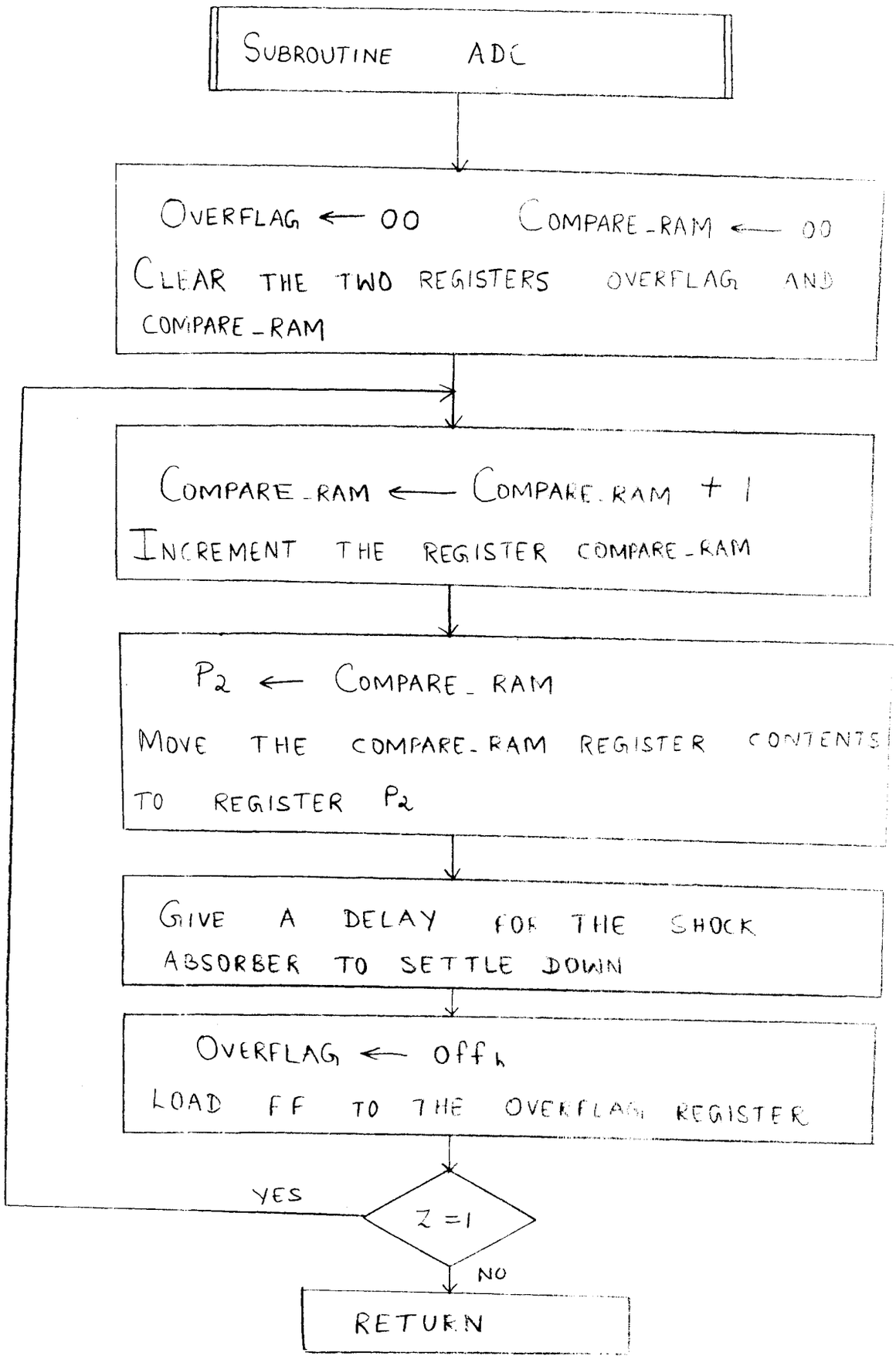
FLOWCHART


START
CALL THE ROUTINE CAPT_PASSWD
The job of this routine is to multiplex port 2, accept the password and store it in a reg
CALL THE ROUTINE ADC
The job of this routine is to find the digital equivalent of the analog output of the transducer and store it in a reg
REF ← COMPARE_RAM
The value in compare_ram is moved to a reg ref
REF ← REF + TOLERANCE
The tolerance value is added to the actual value and this is the net refcrence
A

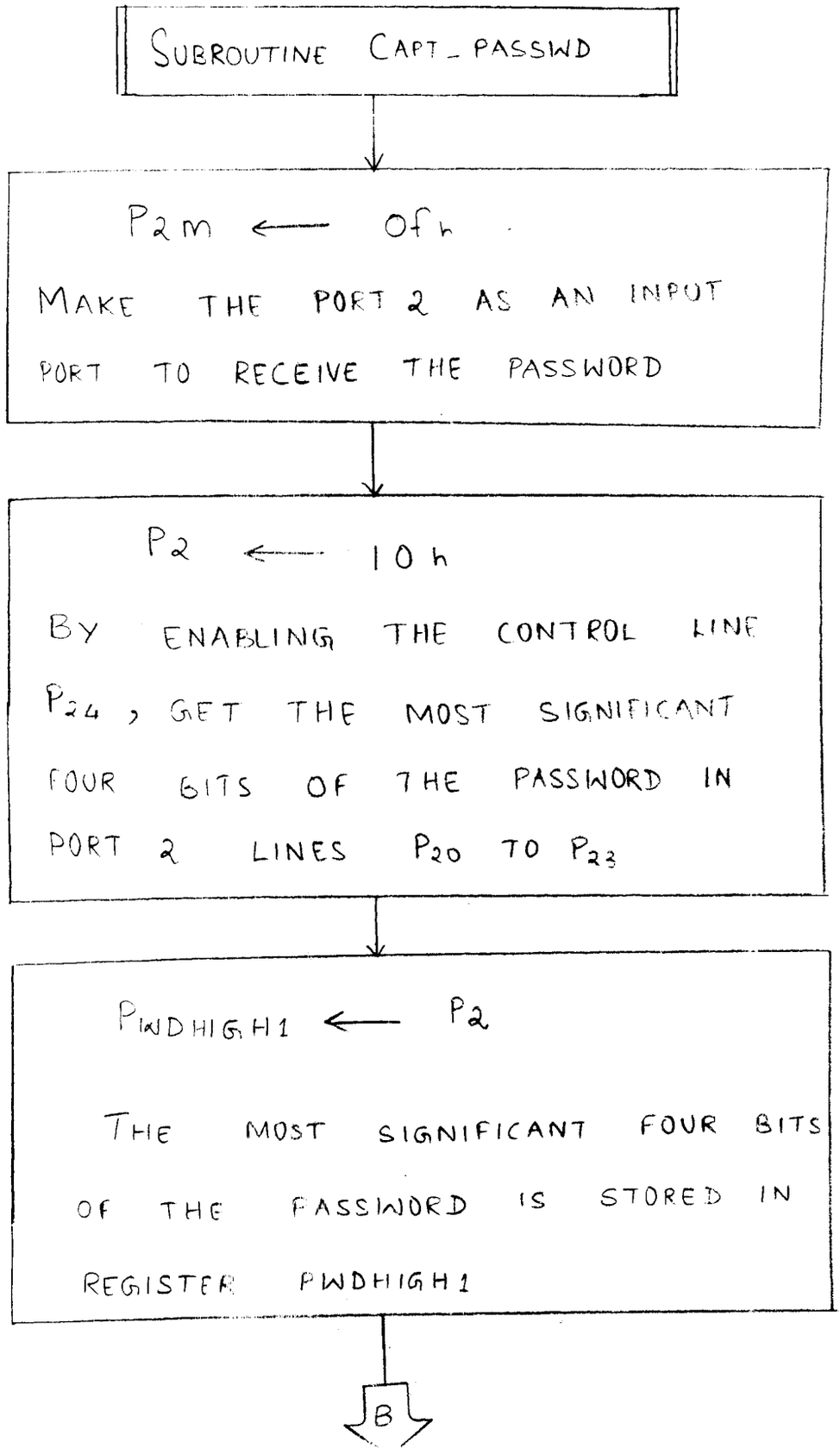


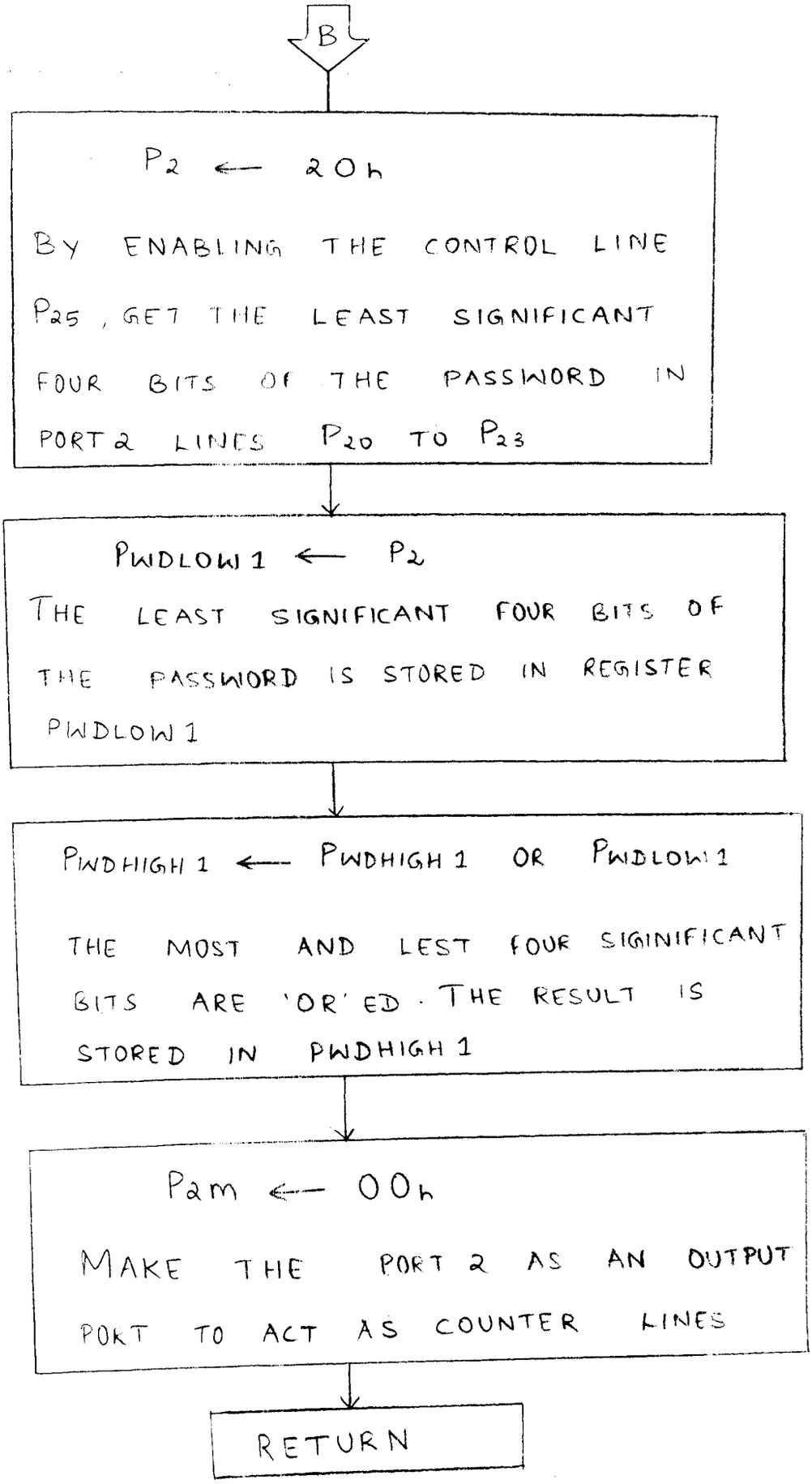
MAIN PROGRAM

SUBROUTINE ADC

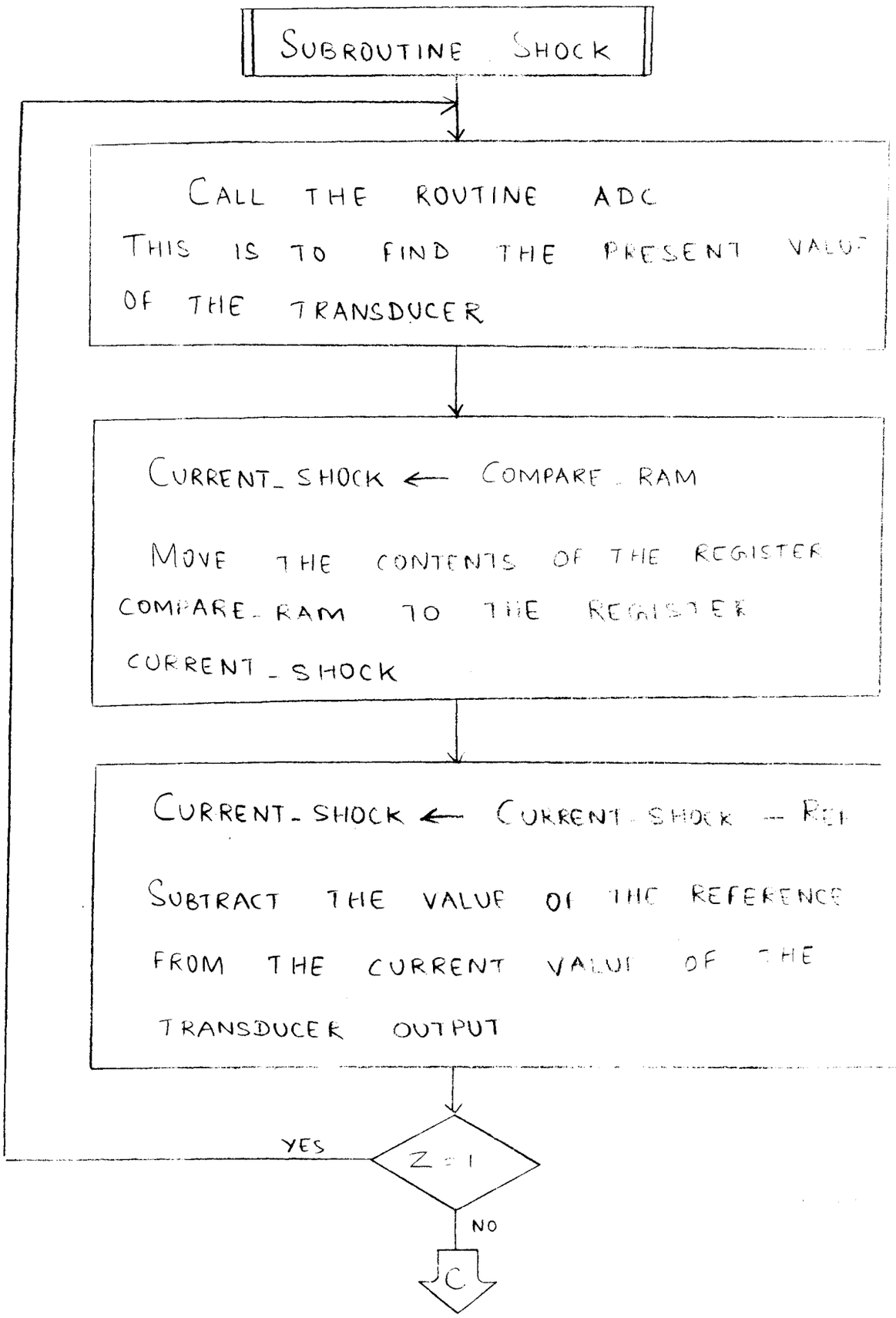


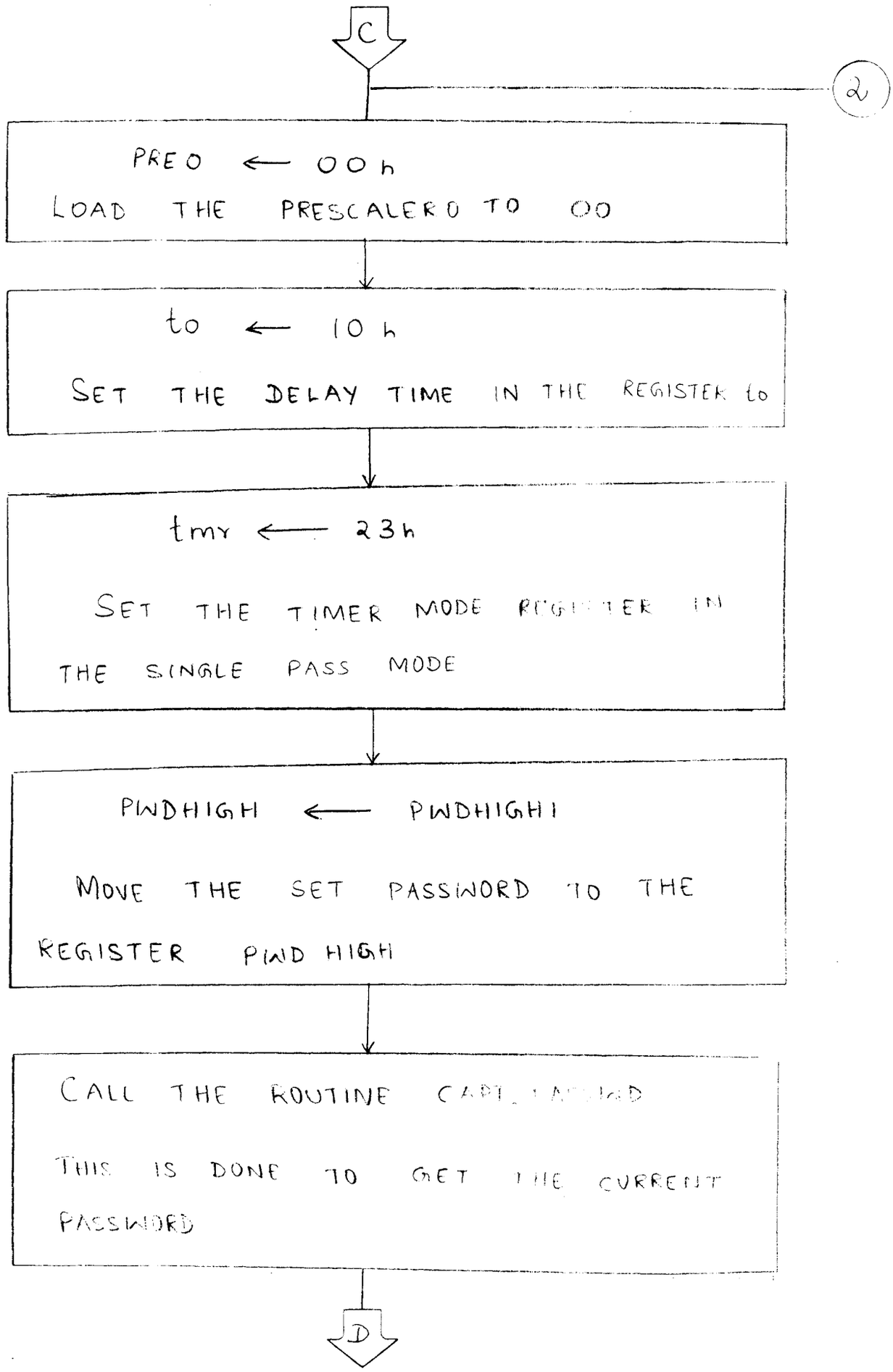
SUBROUTINE CAPT_PASSWD

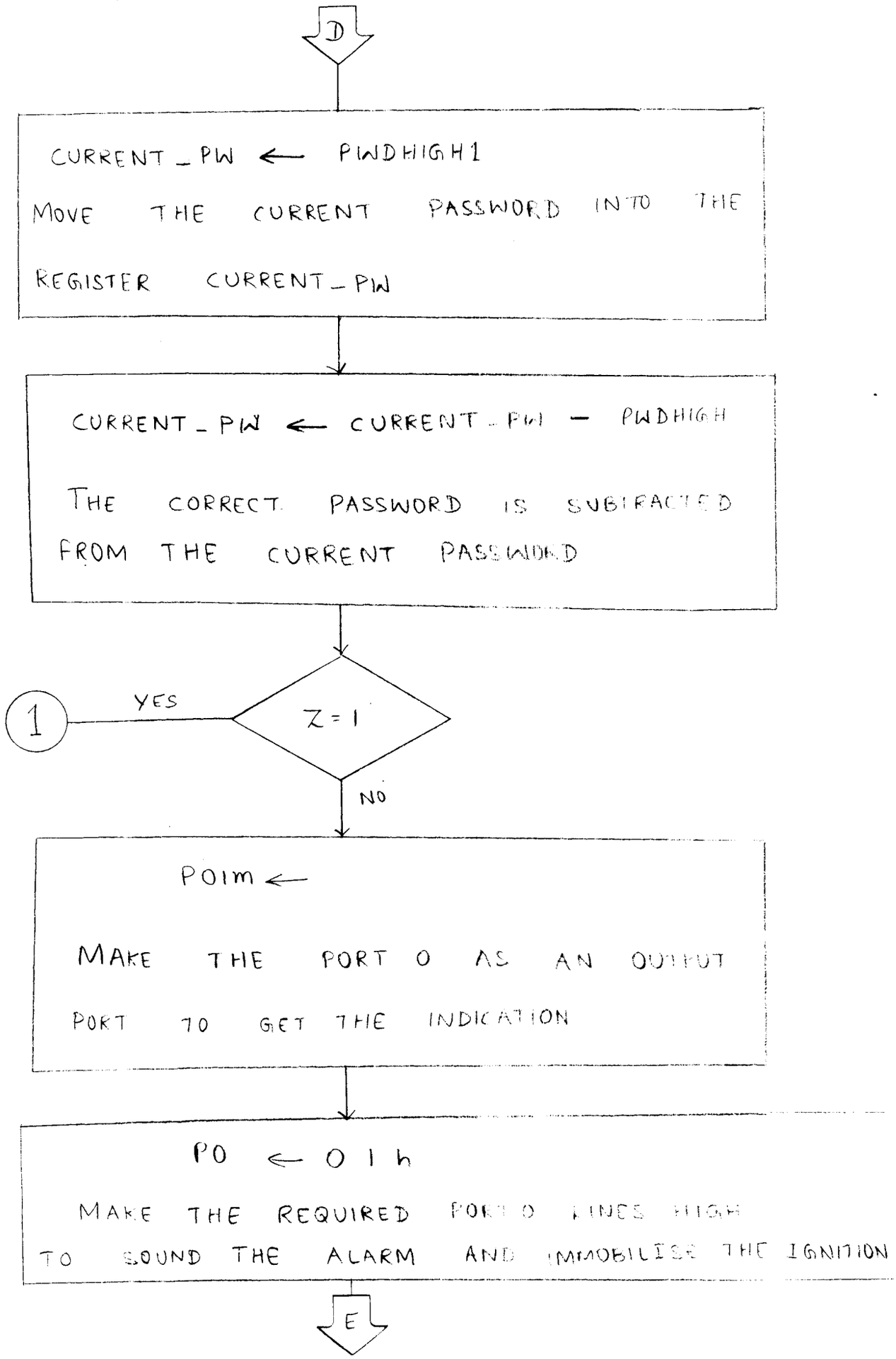


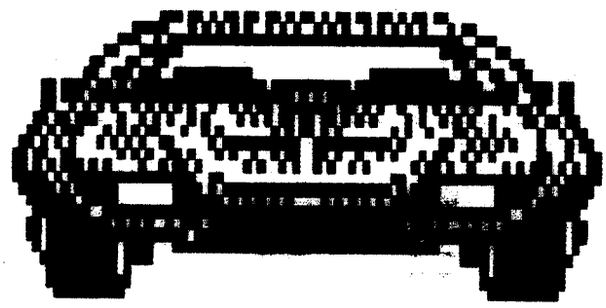

B
P2 ← 20h
BY ENABLING THE CONTROL LINE P25, GET THE LEAST SIGNIFICANT FOUR BITS OF THE PASSWORD IN PORT 2 LINES P20 TO P23
PWDLOW1 ← P2
THE LEAST SIGNIFICANT FOUR BITS OF THE PASSWORD IS STORED IN REGISTER PWDLOW1
PWDHIGH1 ← PWDHIGH1 OR PWDLOW1
THE MOST AND LEST FOUR SIGINIFICANT BITS ARE 'OR' ED. THE RESULT IS STORED IN PWDHIGH1
P2m ← 00h
MAKE THE PORT 2 AS AN OUTPUT PORT TO ACT AS COUNTER LINES
RETURN

SUBROUTINE SHOCK

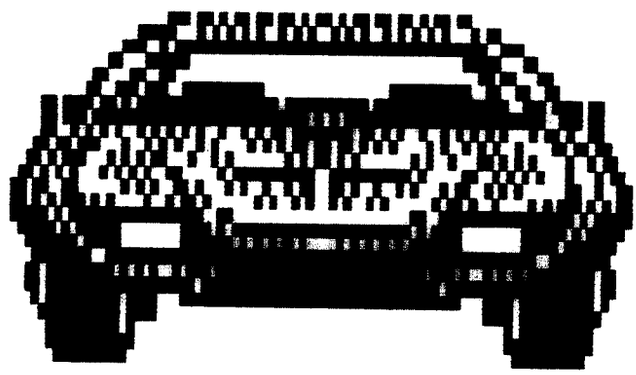



C
2
PRE 0 ← 00 h
LOAD THE PRESCALER 0 TO 00
to ← 10 h
SET THE DELAY TIME IN THE REGISTER to
tmr ← 23h
SET THE TIMER MODE REGISTER IN
THE SINGLE PASS MODE
PWDHIGH ← PWDHIGH1
MOVE THE SET PASSWORD TO THE
REGISTER PWD HIGH
CALL THE ROUTINE
THIS IS DONE TO GET THE CURRENT
PASSWORD
D


D
CURRENT_PW ← PWDHIGH1
MOVE THE CURRENT PASSWORD INTO THE REGISTER CURRENT_PW
CURRENT_PW ← CURRENT_PW − PWDHIGH
THE CORRECT PASSWORD IS SUBTRACTED FROM THE CURRENT PASSWORD
1
YES
Z = 1
NO
P0IM ←
MAKE THE PORT 0 AS AN OUTPUT PORT TO GET THE INDICATION
P0 ← 01h
MAKE THE REQUIRED PORT 0 LINES HIGH TO SOUND THE ALARM AND IMMOBILISE THE IGNITION
E



DESIGN OF SYSTEM HARDWARE



APPENDIX

Z86E04/08 OTP

CMOS Z8® 8-BIT MICROCONTROLLER

FEATURES

- 8-Bit CMOS Microcontroller
- 18-Pin DIP Package
- Low Cost
- Low Noise Programmable
- ROM Protect Programmable
- 4.0V to 5.5V Operating Range
- Low Power Consumption - 50 mW (Typical)
- Fast Instruction Pointer - 1 µs @ 12 MHz (E08), 1.25 µs @ 8 MHz (E04)
- Two Standby Modes - STOP and HALT
- 14 Input/Output Lines
- All Digital Inputs, CMOS Levels, Schmitt-Triggered
- 2 Kbytes of One-Time PROM (E08); 1 Kbytes of One-Time PROM (E04)
- 124 Bytes of General-Purpose RAM
- Two Programmable 8-Bit Counter/Timers Each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Clock Speeds up to 12 MHz (E08), 8 MHz (E04)
- Watch-Dog Timer
- Power-On Reset
- Two On-Board Comparators
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive
- Programmable Interrupt Polarity

4

GENERAL DESCRIPTION

The Z86E04/08 Microcontrollers (MCUs) introduce a new level of sophistication to single-chip architecture. The Z86E04/08 are members of the Z8 single-chip microcontroller family with 1K/2K bytes of one-time PROM for the Z86E04 and Z86E08, respectively. The devices are housed in an 18-pin DIP or SOIC, and are manufactured in CMOS technology. The devices allow easy software development and debug, prototyping, and small production runs not economically desirable with a masked ROM version.

The Z86E04/08 have a flexible I/O scheme, an efficient register, and address space structure. Also, they have a number of ancillary features that are useful in many consumer, industrial, and commercial applications.

For applications which demand powerful I/O capabilities, the Z86E04/08 provide 14 pins dedicated to input and output. These lines are grouped into three ports, and are configurable under software control to provide I/O, timing, and status signals.

There are two basic address spaces available to support this wide range of configurations: program memory and 124 bytes of general-purpose registers.

The Z86E04/08 each offer programmable EPROM Protect and programmable Low Noise. When the part is programmed for EPROM Protect, the Low Noise feature will automatically be enabled. When programmed for Low Noise, the EPROM Protect feature is optional.

GENERAL DESCRIPTION (Continued)

To unburden the program from coping with real-time tasks such as counting/timing and I/O data communications, the Z86E04/08 offers two on-chip counter/timers with a large number of user selectable modes. Included, are two on-board comparators that process analog signals with a minimum external voltage (Figures 1 and 2).

Notes:
A, S signals with a preceding front slash "/" are active Low.
B. W/(WORD) is active Low. /(DW/(BYTE) is active Low.

Power connections follow conventional descriptions.

Connection	Circuit	Device
Power	V_{CC}	
Ground	GND	

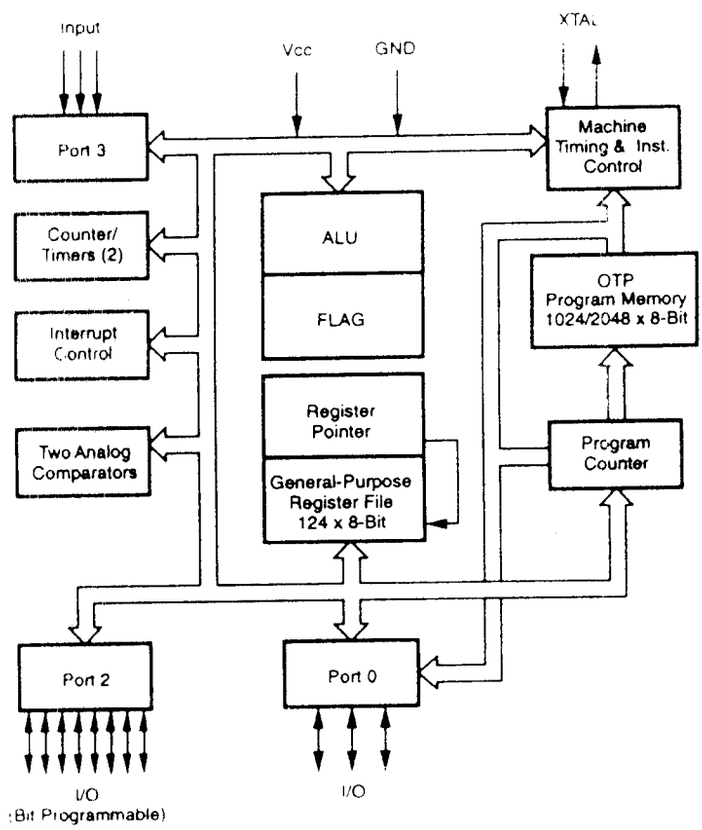


Figure 1. Functional Block Diagram

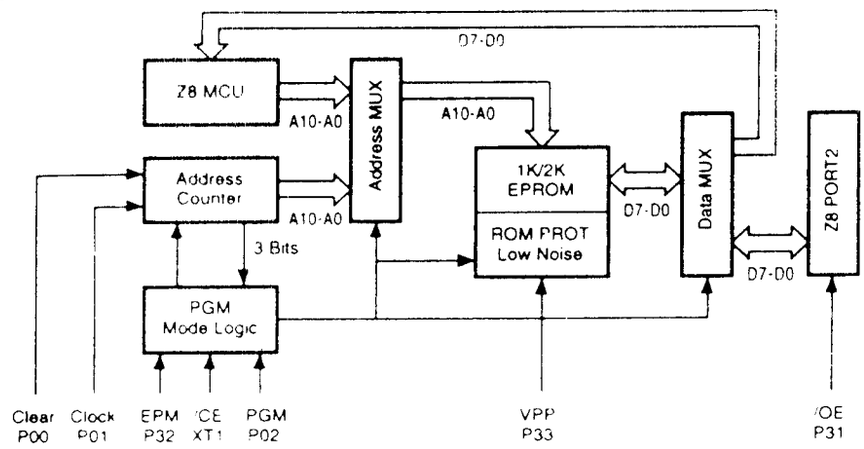


Figure 2. EPROM Mode Block Diagram

PIN DESCRIPTION

Table 1. EPROM Mode Pin Identification

Z86E04/08 Pin #	EPROM Mode Symbol	Function	Direction
1-4	D7-D4	Data 4, 5, 6, 7	In/Output
5	V_{CC}	Power Supply	
6	N/C	No Connection	
7	/CE	Chip Enable	Input
8	/OE	Output Enable	Input
9	EPM	EPROM Prog Mode	Input
10	V_{PP}	Prog Voltage	Input
11	Clear	Clear Clock	Input
12	Clock	Address	Input
13	/PGM	Prog Mode	Input
14	GND	Ground	
15-18	D3-D0	Data 0, 1, 2, 3	In/Output

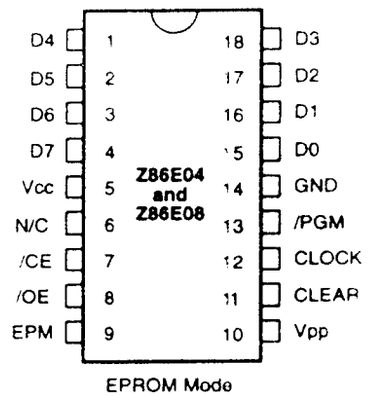
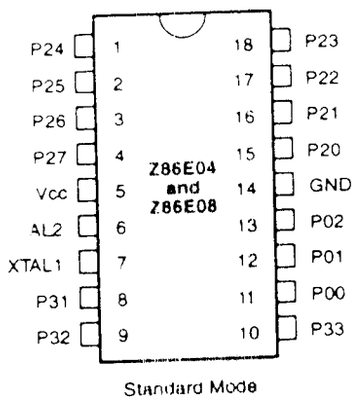


Figure 3. EPROM Mode Pin Configuration

4

PIN DESCRIPTION



Standard Mode

Figure 4. Standard Mode Pin Configuration

Table 2. Standard Mode Pin Identification

Z86E04/08 Pin #	Standard Mode Symbol	Function	Direction
1-4	P27-P24	Port 2, Pins 4, 5, 6, 7	In/Output
5	V_{cc}	Power Supply	
6	XTAL2	Crystal Osc. Clock	Output
7	XTAL1	Crystal Osc. Clock	Input
8	P31	Port 3, Pin 1	Input
9	P32	Port 3, Pin 2	Input
10	P33	Port 3, Pin 3	Input
11-13	P02-P00	Port 0, Pins 0, 1, 2	Input/Output
14	GND	Ground	
15-18	P23-P20	Port 2, Pins 0, 1, 2, 3	In/Output

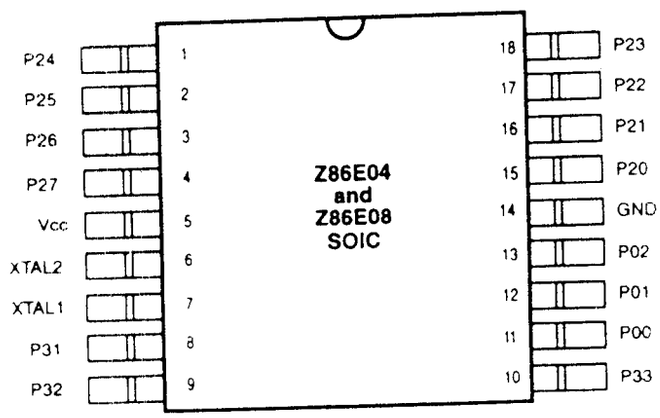


Figure 5. 18-Pin SOIC Pin Configuration

Table 3. 18-Pin SOIC Pin Identification

Pin #	Symbol	Function	Direction
1-4	P24-P27	Port 2, Pins 4,5,6,7	In/Output
5	V_{cc}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8	P31	Port 3, Pin 1, AN1	Input
9	P32	Port 3, Pin 2, AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11-13	P00-P02	Port 0, Pins 0,1,2	In/Output
14	GND	Ground	
15-18	P20-P23	Port 2, Pins 0,1,2,3	In/Output

PIN FUNCTIONS

OTP Programming Mode

D7-D0 *Data Bus*. The data can be read from or written to the EPROM through this data bus.

V_{CC} *Power Supply*. It is 5V during the EPROM Read mode and 6V during the other mode.

/CE *Chip Enable* (active Low). This pin is active during EPROM Read Mode, Program Mode and Program Verify Mode.

/OE *Output Enable* (active Low). This pin drives the Data Bus direction. When this pin is Low, the Data Bus is output. When High, the Data Bus is input.

EPM *EPROM Program Mode*. This pin controls the different EPROM Program Modes by applying different voltages.

V_{PP} *Program Voltage*. This pin supplies the program voltage.

Clear *Clear* (active High). This pin resets the internal address counter at the High Level.

Clock *Address Clock*. This pin is a clock input. The internal address counter increases by one with one clock signal.

/PGM *Program Mode* (active Low). Low Level at this pin programs the data to the EPROM through the Data Bus.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if **excessive noise** surges above V_{CC} occur on the following specific pins:

- XTAL1 pin
- /RESET pin

In addition, processor operation of Z8 One-Time Programmable devices may be affected by excessive noise surges on the V_{PP} pin while the microcontroller is in standard mode.

Recommendations for dampening voltage surges in both test and OTP mode include the following:

- Using a clamping diode to Vcc
- Adding a capacitor to the affected pin

Z86E04/08 STANDARD MODE

XTAL1, XTAL2 *Crystal In, Crystal Out* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, LC, or an external single-phase clock (8 MHz or 12 MHz max) to the on-chip clock oscillator and buffer.

Port 0, P02-P00. Port 0 is a 3-bit bi-directional Schmitt-triggered CMOS compatible I/O port. These three I/O lines can be globally configured under software control to be an input or output (Figure 6).

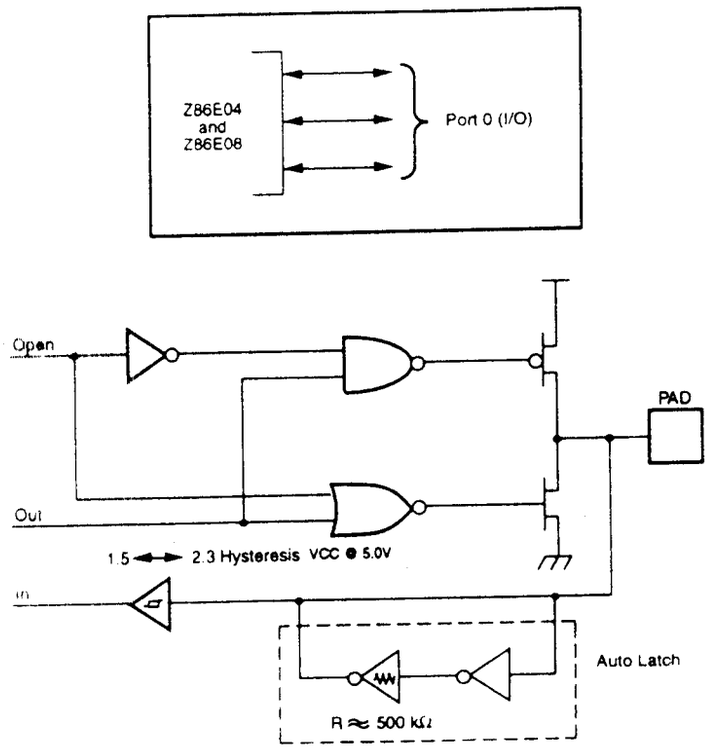


Figure 6. Port 0 Configuration

Port 2, P27-P20. Port 2 is an 8-bit, bit programmable, bidirectional Schmitt-triggered CMOS compatible I/O port. These eight I/O lines can be configured under software control to be an input or output, independently. Bits programmed as outputs can be globally programmed as either push-pull or open-drain (Figure 7).

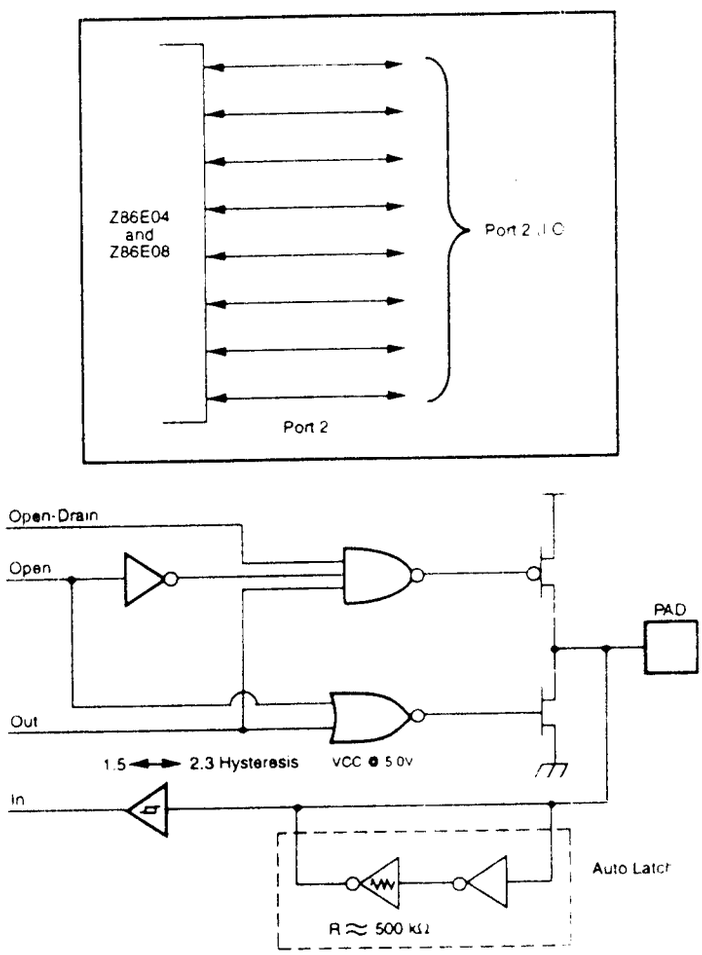


Figure 7. Port 2 Configuration

Z86E04/08 Standard Mode (Continued)

Port 3, P33-P31. Port 3 is a 3-bit, CMOS compatible port with three fixed input (P32-P30) lines. These three input lines can be configured under software control as digital inputs or analog inputs. These three input lines are also used as the interrupt sources IRQ0-IRQ3 and as the timer input signal (T_{IN} - Figure 8).

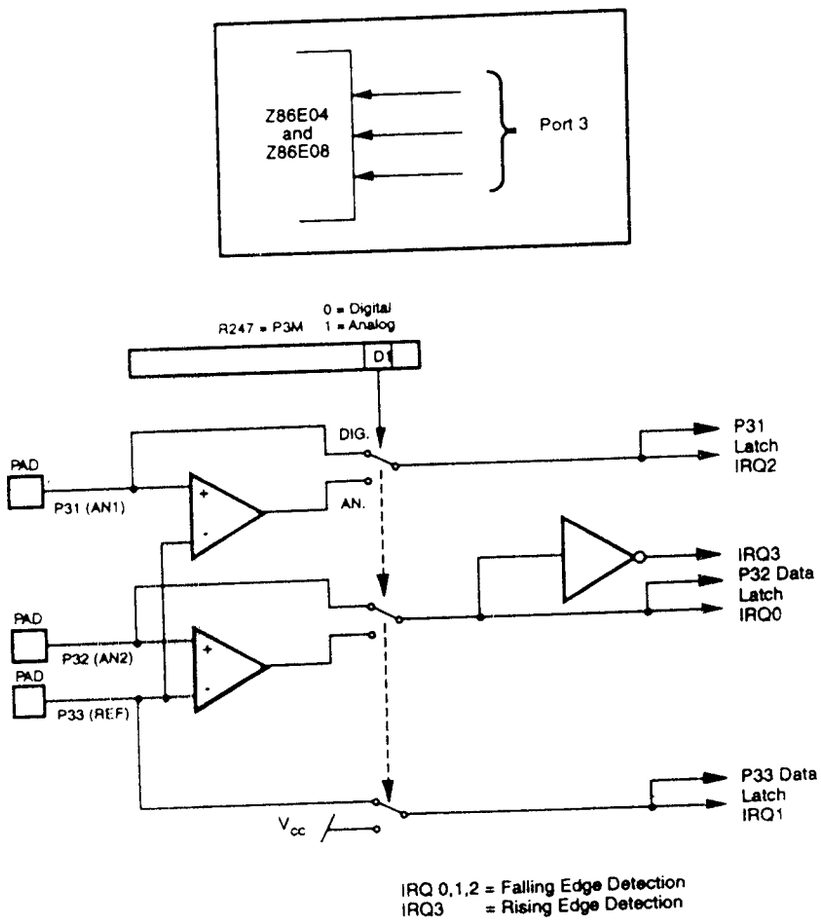


Figure 8. Port 3 Configuration

ZILOG

Comparator Inputs. Two analog comparators are added to input of Port 3, P31 and P32, for interface flexibility. The comparators reference voltage P3 (REF) is common to both comparators.

Typical applications for the on-board comparators: Zero crossing detection, A/D conversion, voltage scaling, and threshold detection. In analog mode, P33 input functions serve as a reference voltage to the comparators.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP mode. The common voltage range is 0-4 V when the V_{CC} is 5.0 V, the power supply and common mode rejection ratios are 90dB and 60dB, respectively.

Interrupts are generated on either edge of comparator 2's output, or on the falling edge of comparator 1's output. The comparator output is used for interrupt generation, Port 3 data inputs, or T_{IN} through P31. Alternatively, the comparators can be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

SPECIAL FUNCTIONS

The Z8 MCU incorporates special functions to enhance the Z8's application in industrial, scientific and advanced technologies applications.

RESET is accomplished through Power-On or a Watch Dog Timer Reset. Upon power-up, the power-on reset circuit waits for T_{POR} msec plus 18 crystal clocks and then starts program execution at address 000C (Hex). Reference Table 4 for the Z86E04/08 control registers reset values (Figure 9).

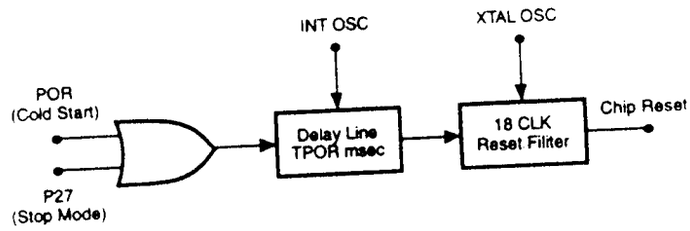


Figure 9. Internal Reset Configuration

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for a POR timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the four following conditions:

- Power bad to power good status
- Stop-Mode Recovery
- WDT time-out
- WDH time-out

Watch-Dog Timer Reset. The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and is retriggered on subsequent execution of the WDT instruction. The timer circuit is driven by an on-board RC oscillator.

SPECIAL FUNCTIONS (Continued)

Table 4. Z86E04/08 Control Registers

Addr.	Reg.	Reset Condition D7	D6	D5	D4	D3	D2	D1	D0	Comments
F1	TMR	0	0	0	0	0	0	0	0	
F2	T1	U	U	U	U	U	U	U	U	
F3	PRE1	U	U	U	U	U	U	0	0	
F4	T0	U	U	U	U	U	U	U	U	
F5	PRE0	U	U	U	U	U	U	U	0	
F6*	P2M	1	1	1	1	1	1	1	1	Inputs after reset.
F7*	P3M	U	U	U	U	U	U	0	0	
F8*	P01M	U	U	U	0	U	U	0	1	
F9	IPR	U	U	U	U	U	U	U	U	
FA	IRQ	U	0	0	0	0	0	0		IRQ3 is used for positive edge detection.
PB	IMR	0	U	U	U	U	U	U	U	
PC	FLAGS	U	U	U	U	U	U	U	U	U
FD	RP	0	0	0	0	0	0	0	0	
FF	SPL	U	U	U	U	U	U	U	U	

Note:
* Registers are not reset after a Stop-Mode Recovery using P27 pin. A subsequent reset will cause these control registers to be reconfigured as shown in Table 4 and the user must avoid bus contention on the port pins or it may affect device reliability

Program Memory. The Z86E04/08 addresses up to 1K/2K bytes of internal program memory (Figure 10). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0-1024/2048 are on-chip one-time programmable ROM

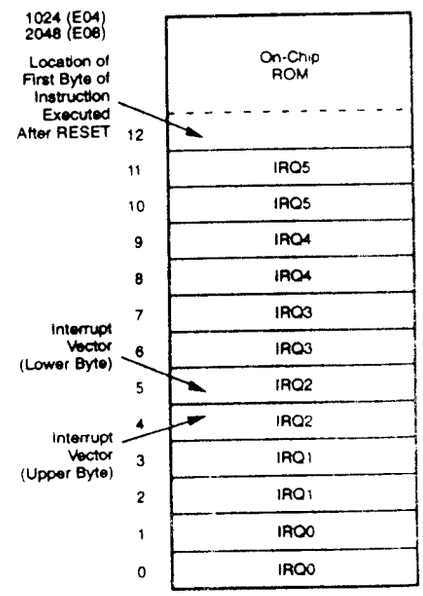


Figure 10. Program Memory Map

Register File. The Register File consists of three I/O port registers, 124 general-purpose registers, and 14 control and status registers (R0-R3, R4-R127 and R241-R255, respectively (Figure 11). General-purpose registers occupy the 04H to 7FH address space. I/O ports are mapped as per the existing CMOS Z8. The Z86E04/08 instructions can access registers directly or indirectly through an 8-bit address field. This allows short 4-bit register addressing using the Register Pointer. In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 contiguous locations. The Register Pointer (Figure 12) addresses the starting location of the active working-register group.

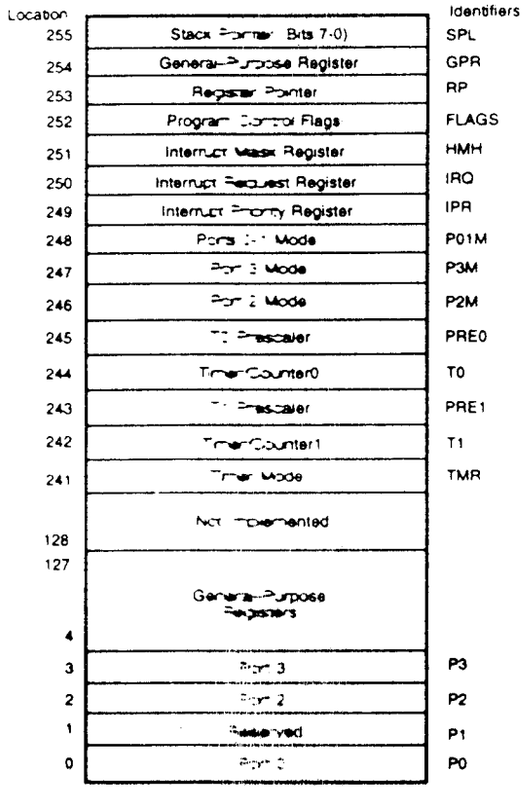


Figure 11. Register File

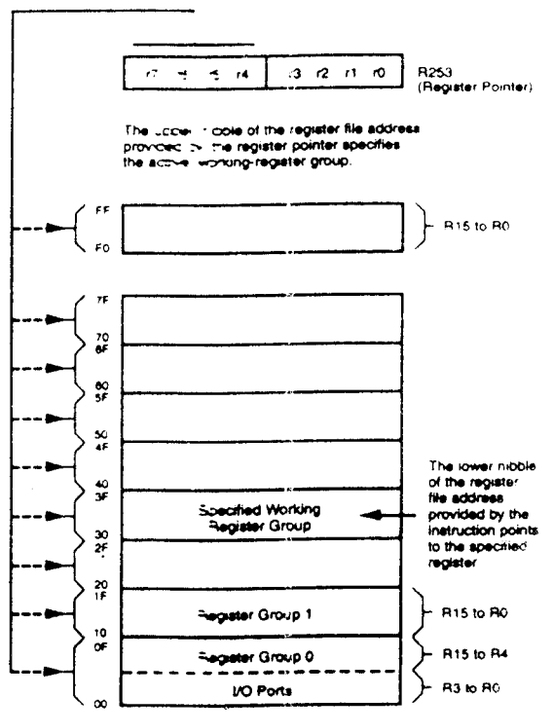


Figure 12. Register Pointer

SPECIAL FUNCTIONS (Continued)

Stack Pointer. The Z86E04/08 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general-purpose registers.

GPR *(R254)*. This register is a general-purpose register.

Counter/Timer. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources, however, the T0 can be driven by the internal clock source only (Figure 13).

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters are also programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P30) as an external clock, a trigger input that is retriggerable or not retriggerable, or used as a gate input for the internal clock.

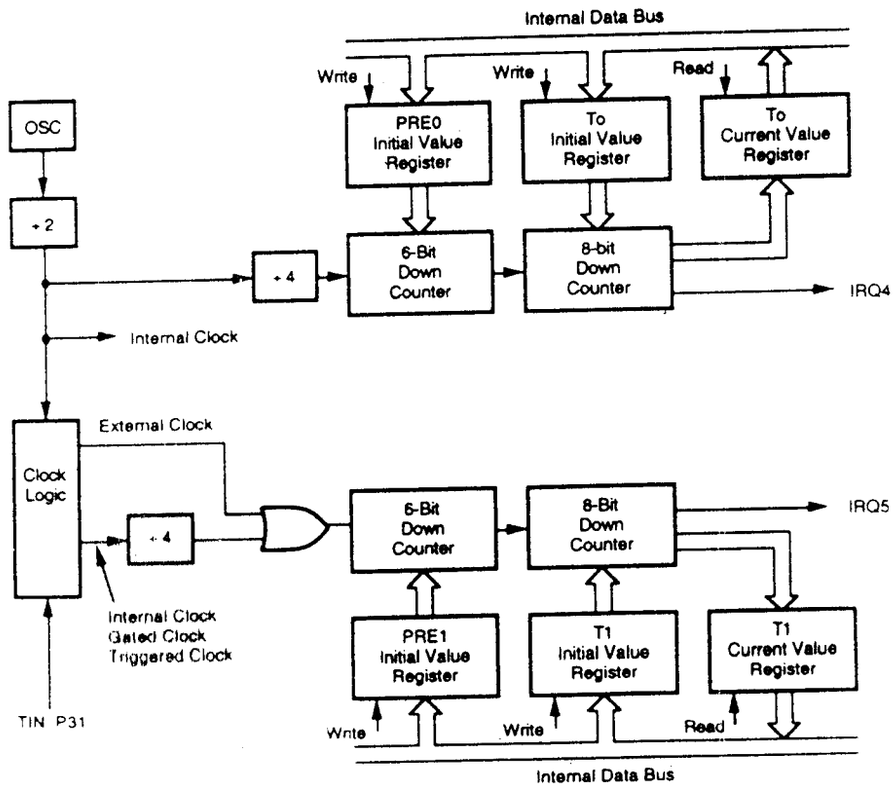


Figure 13. Counter/Timers Block Diagram

SPECIAL FUNCTIONS (Continued)

Interrupts. The Z86E04/08 has six interrupts from five different sources. These interrupts are maskable and prioritized (Figure 14). The sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and two counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 5).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86E04/08 interrupts are vectored through locations in program memory. When an Interrupt machine cycle is activated, an Interrupt Request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

Table 5. Interrupt Types, Sources, and Vectors

Source	Name	Vector Location	Comments
AN2(P32)	IRQ0	0,1	External (F)Edge
REF(P33)	IRQ1	2,3	External (F)Edge
AN1(P31)	IRQ2	4,5	External (F)Edge
AN2(P32)	IRQ3	6,7	External (R)Edge
T0	IRQ4	8,9	Internal
T1	IRQ5	10,11	Internal

Notes:
F = Falling edge triggered
R = Rising edge triggered

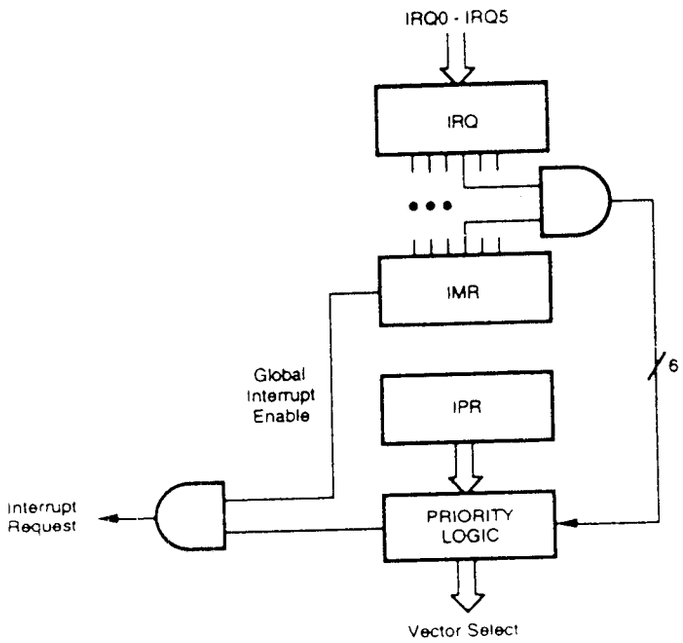
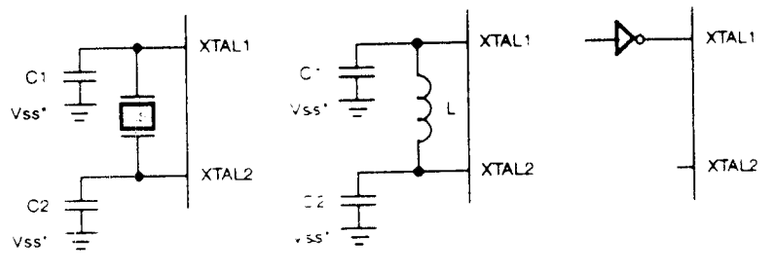


Figure 14. Interrupt Block Diagram

Clock. The Z86E04/08 on-chip oscillator has a high-gain parallel-resonant amplifier for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = INPUT, XTAL2 = OUTPUT). The crystal should be AT cut, 8 MHz or 12 MHz max, with a series resistance (RS) of less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendors crystal recommended capacitors from each pin directly to device ground pin 14 (Figure 15). Note that the crystal capacitor loads should be connected to V_{SS}, Pin 14 to reduce Ground noise injection.



Ceramic Resonator or Crystal

LC Clock

External Clock

* Device Ground Pin

Figure 15. Oscillator Configuration

HALT Mode. Turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP Mode. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA. The STOP mode is released by a RESET through a Stop-Mode Recovery (pin P27). A Low input condition on P27 releases the STOP mode. Program execution begins at location 000C(Hex). However, when P27 is used to release the STOP mode, the I/O port mode registers are not reconfigured to their default power-on conditions. This prevents any I/O, configured as output when the STOP instruction was executed, from glitching to an unknown state. To use the P27 release approach with STOP mode, use the following instruction:

```
LD      P2M, #1XXX XXXXB
NOP
STOP
```

* = Depending on user application

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode = FFH) immediately before the appropriate sleep instruction, i.e.:

```
FF    NOP;    clear the pipeline
6F    STOP;   enter STOP mode
              or
FF    NOP;    clear the pipeline
7F    HALT;   enter HALT mode
```

Watch-Dog Timer (WDT). The Watch-Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT is refreshed when it is enabled with every 1Twdt period; otherwise, the Z86E04 resets itself. The WDT instruction affects the flags accordingly: Z=1, S=0, V=0.

WDT = 5F (Hex)

Opcode WDT (5FH). The first time opcode 5FH is executed, the WDT is enabled and subsequent execution clears the WDT counter. This has to be done at least every 15 µsec. Otherwise, the WDT times out and generates a reset. The generated reset is the same as a power-on reset of 50 µsec +18 XTAL clock cycles.

SPECIAL FUNCTIONS (Continued)

Opcode WDH (4FH). When this instruction is executed it enables the WDT during HALT. If not, the WDT stops when entering HALT. This instruction does not clear the counters; it just makes it possible to have the WDT running during HALT mode. A WDH instruction executed without executing WDT (5FH) has no effect.

Auto Reset Voltage (V_{RST}). The Z86E04/08 has an auto-reset built-in. The auto-reset circuit resets the Z86E04/08 when it detects the V_{CC} below V_{RST}. Figure 16 shows the Auto Reset Voltage vs temperature. The Z86E04/08 does not function from VRST to below 4.5V. Upon power-up of the device, the V_{CC} rise time must reach 4.5V. Upon power-up of the device, the V_{CC} rise time must reach 4.5V before the T_{POR} expires so that program execution begins with the V_{CC} in the range 4.5V to 5.5V.

If the V_{CC} drops below 4.5V while the device is in operation, the device must be powered down and then re-powered up again.

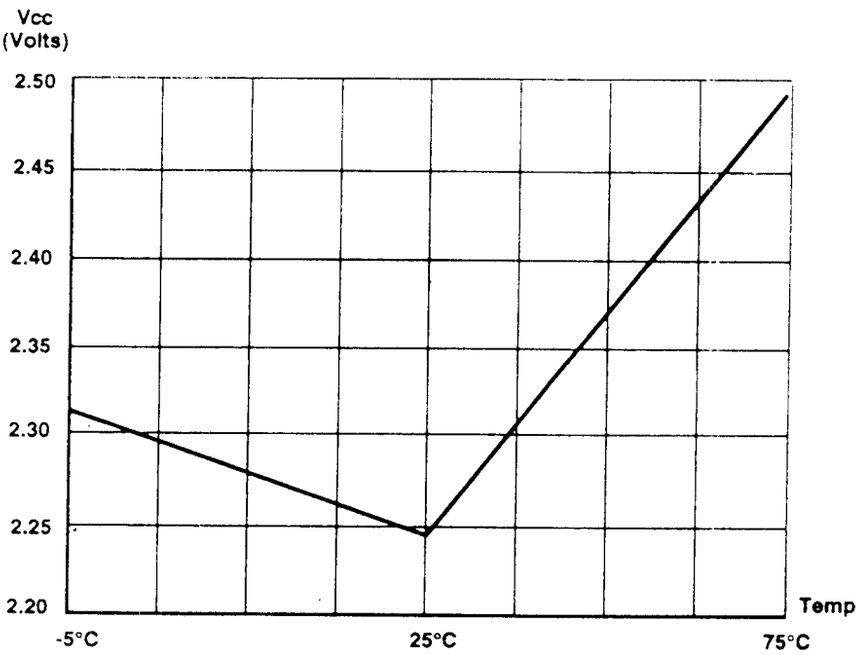


Figure 16. Typical Auto Reset Voltage (V_{RST}) vs Temperature

4

SPECIAL FUNCTIONS (Continued)

Low EMI Emission

The Z86E04/08 can be programmed to operate in a low EMI emission mode by means of an EPROM programmable bit option. Use of this feature results in:

- Less than 1 mA consumed during HALT mode.
- All drivers slew rates reduced to 10 ns (typical).
- Internal SCLK/TCLK = XTAL operation limited to a maximum of 4 MHz - 250 ns cycle time
- Output drivers have resistances of 200 ohms (typical).
- Oscillator divide-by-two circuitry eliminated

The Z86E04/08 offers programmable ROM Protect and programmable Low Noise features. When programmed for Low Noise, the ROM Protect feature is optional.

Besides V_{DD} and GND (V_{SS}), the Z86E04/08 changes all its pin functions in the EPROM mode. XTAL2 has no function, XTAL1 functions as /CE, P31 functions as /OE, P32 functions as EPM, P33 functions as V_{PP}, and P02 functions as /PGM.

ROM Protect. ROM Protect fully protects the Z86E04/08 ROM code from being read externally. When ROM Protect is selected, the Z86E04/08 will disable the instructions LDC and LDCI (Z86E04/08 and Z86C04/08 do not support the instructions of LDE and LDEI). When the device is programmed for ROM Protect, the Low Noise feature will automatically be enabled.

Please note that when using the device in a noisy environment, it is suggested that the voltages on the EPM and CE pins be clamped to V_{CC} through a diode to V_{CC} to prevent accidentally entering the OTP mode. The V_{PP} requires both a diode and a 100 pF capacitor.

User Modes. Table 6 shows the programming voltage of each mode of Z86E04/08.

Table 6. OTP Programming Table

Programming Modes	Device	V_{PP}	EPM	/CE	/OE	/PGM	ADDR	DATA	V_{CC}*
EPROM READ1	All	X	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	4.5V
EPROM READ2	All	X	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	5.5V
PROGRAM	All	V_H	X	V_{IL}	V_{IH}	V_{IL}	ADDR	In	6.0V
PROGRAM VERIFY	All	V_H	X	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	6.0V
EPROM PROTECT	All	V_H	V_H	V_H	V_{IH}	V_{IL}	NU	NU	6.0V
LOW NOISE SELECT	E04/08	V_H	V_{IH}	V_H	V_{IH}	V_{IL}	NU	NU	6.0V

Notes:
V_H = 12.5V ±0.5V
V_{IH} = As per specific Z8 DC specification.
V_{IL} = As per specific Z8 DC specification.
X = Not used, but must be set to V_{IH}, V_{IH}, or V_{IL} level
NU = Not used, but must be set to either V_{IH} or V_{IL} level
I_{PP} during programming = 40 mA maximum.
I_{CC} during programming, verify, or read = 40 mA maximum
* V_{CC} has a tolerance of ±0.25V

Internal Address Counter. The address of Z86E04/08 is generated internally with a counter clocked through pin P01 (Clock). Each clock signal increases the address by one and the "high" level of pin P00 (Clear) will reset the address to zero. Figure 17 shows the set-up time of the serial address input.

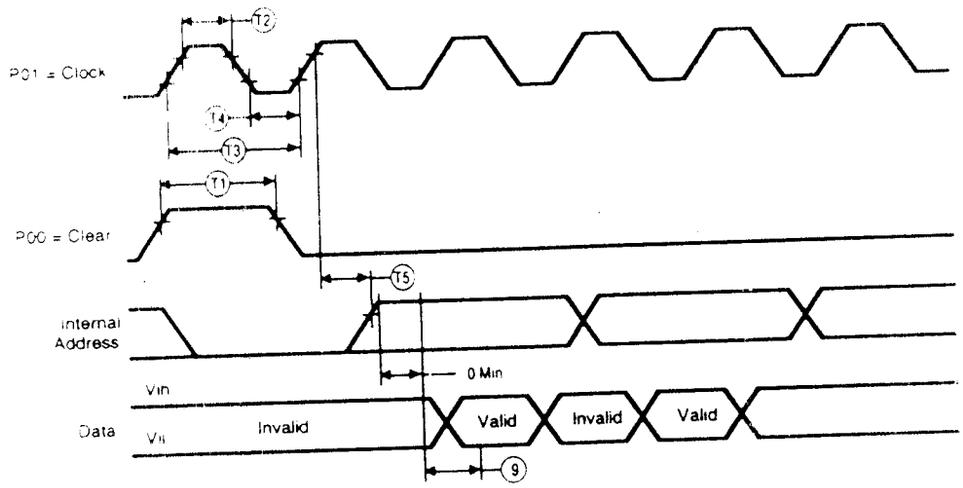
Programming Waveform. Figures 18, 19 and 20 show the programming waveforms of each mode. Table 7 shows the timing of programming waveforms.

Programming Algorithm. Figure 21 shows [illegible] of the Z86E04/08 programming algorithm.

Table 7. Timing of Programming Waveforms

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		[illegible]
2	Data Setup Time	2		[illegible]
3	V_{pp} Setup	2		[illegible]
4	V_{cc} Setup Time	2		[illegible]
5	Chip Enable Setup Time	2		[illegible]
6	Program Pulse Width	0.95		[illegible]
7	Data Hold Time	2		[illegible]
8	/OE Setup Time	2		[illegible]
9	Data Access Time		200	[illegible]
10	Data Output Float Time		100	[illegible]
11	Overprogram Pulse Width	2.85		[illegible]
12	EPM Setup Time	2		[illegible]
13	/PGM Setup Time	2		[illegible]
14	Address to /OE Setup Time	2		[illegible]
15	Option Program Pulse Width	78		[illegible]

Low EMI Emission (Continued)



Legend:	
T1 Reset Clock Width	30 ns Min
T2 Input Clock High	30 ns Min
T3 Input Clock Period	70 ns Min
T4 Input Clock Low	30 ns Min
T5 Clock to Address Counter Out Delay	15 ns Max

Figure 17. Z86E04/08 Address Counter Waveform

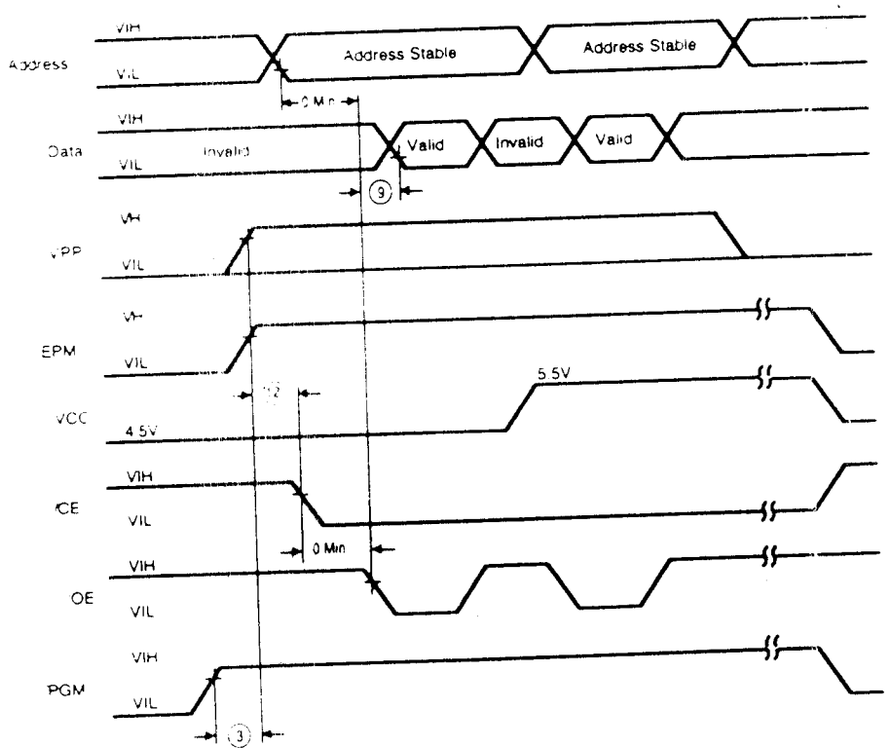


Figure 18. Z86E04/08 Programming Waveform (EPROM Read)

Low EMI Emission (Continued)

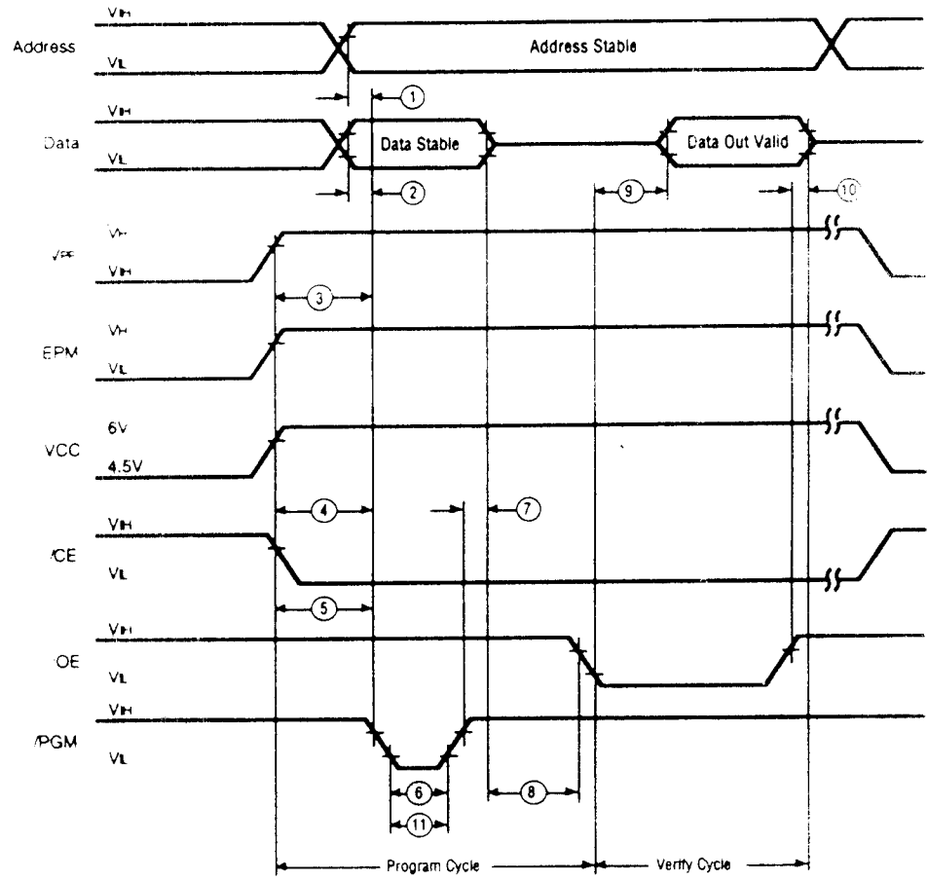


Figure 19. Z86E04/08 Programming Waveform (Program and Verify)

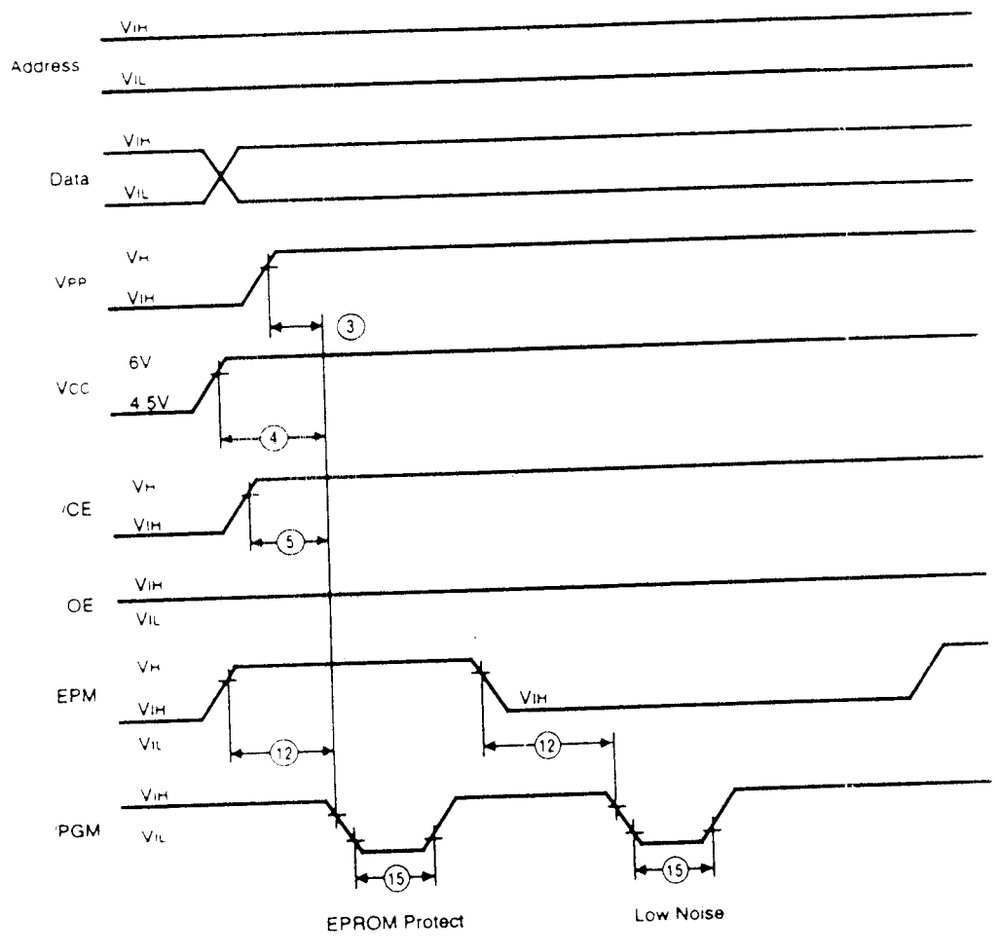


Figure 20. Z86E04/08 Programming Waveform (EPROM Protect and Low EMI Program)

Low EMI Emission (Continued)

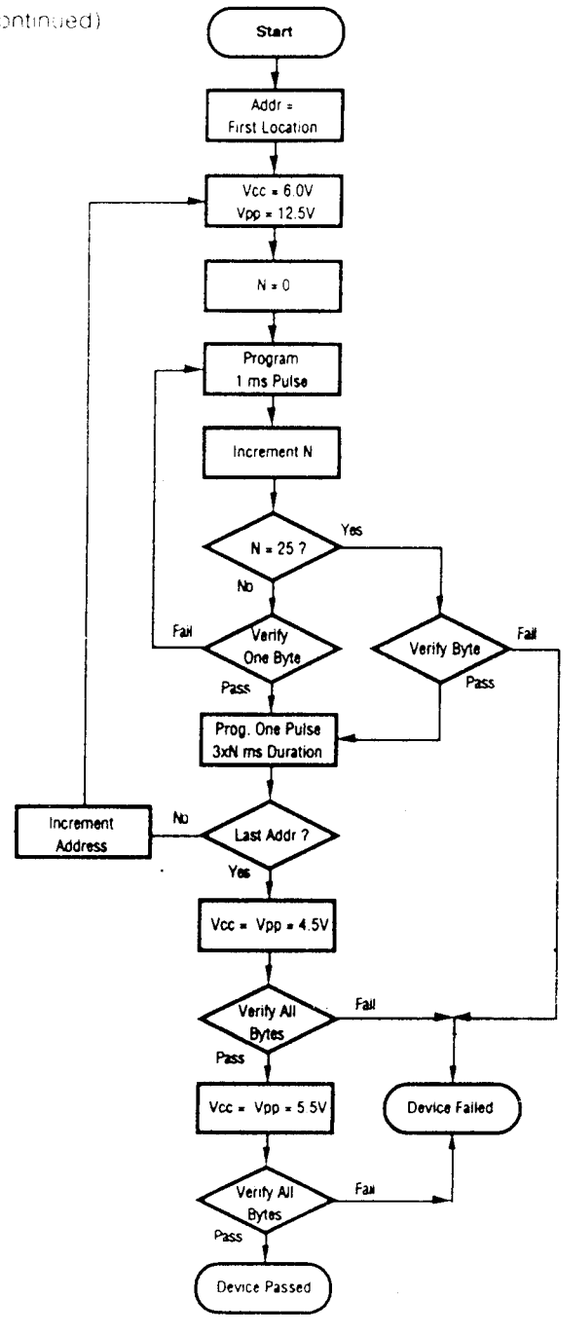


Figure 21. Z86E04/08 Programming Algorithm

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Ambient Temperature under Bias	-40	+105	C
Storage Temperature	-65	+150	C
Voltage on any Pin with Respect to V_{SS} [Note 1]	-0.6	+7.0	V
Voltage on V_{DD} Pin with Respect to V_{SS}	-0.3	+7.0	V
Voltage on Pin 6 with Respect to V_{SS} [Note 2]	-0.6	V_{DD} +1.0	V
Total Power Dissipation		462	mW
Maximum Current out of V_{SS}		84	mA
Maximum Current into V_{DD}		84	mA
Maximum Current into an Input Pin [Note 3]	-600	+600	µA
Maximum Current into an Open-Drain Pin [Note 4]	-600	+600	µA
Maximum Output Current Sinked by Any I/O Pin		12	mA
Maximum Output Current Sourced by Any I/O Pin		12	mA
Total Maximum Output Current Sinked by Port 2		70	mA
Total Maximum Output Current Sourced by Port 2		70	mA

Notice:
Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 462 mW for the package. Power dissipation is calculated as follows:

Notes:
[1] This applies to all pins except where otherwise noted. Maximum current into pin must be ±600µA.
[2] There is no input protection diode from pin to V_{DD}.
[3] This excludes Pin 6 and Pin 7.
[4] Device pin is not at an output Low state.

Total Power dissipation = V_{DD} x [I_{DD} - (sum of I_{OH})] + sum of [(V_{DD} - V_{OH}) x I_{OH}] + sum of (V_{OL} x I_{OL})

4

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 22).

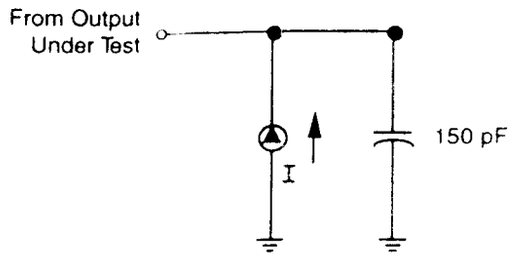


Figure 22. Test Load Diagram

CAPACITANCE

T_A = GND = 0V, f = 1.0 MHz, unmeasured pins to GND.

Parameter	Max
Input capacitance	10 pF
Output capacitance	20 pF
I/O capacitance	25 pF

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
	Max Input Voltage	4.5V		12		V	I_{IN} < 250 µA	
		5.5V		12		V	I_{IN} < 250 µA	
	Clock Input High Voltage	4.5V	0.8 V_{CC}	V_{CC}+0.3	2.4	V	Driven by External Clock Generator	
		5.5V	0.8 V_{CC}	V_{CC}+0.3	2.6	V	Driven by External Clock Generator	
	Clock Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.6		Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	0.2 V_{CC}	2.3	V	Driven by External Clock Generator	
	Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	2.1	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.7	V		
	Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.2	V		
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.7	V		
V_{OH}	Output High Voltage	4.5V	V_{CC}–0.4		3.9	V	I_{OH} = –2.0 mA	[3]
		5.5V	V_{CC}–0.4		5.4	V	I_{OH} = –2.0 mA	[3]
V_{OH}	Output Low Voltage	4.5V	V_{CC}–0.4			V	Low Noise ⓞ I_{OH} = –0.5 mA	
		5.5V	V_{CC}–0.4			V	Low Noise ⓞ I_{OH} = –0.5 mA	
V_{OL}	Output Low Voltage	4.5V		0.4		V	Low Noise ⓞ I_{OL} = +1 mA	
		5.5V		0.4		V	Low Noise ⓞ I_{OL} = +1 mA	
V_{OL}	Output Low Voltage	4.5V		0.8	0.2	V	I_{OL} = +4.0 mA	[3]
		5.5V		0.4	0.2	V	I_{OL} = +4.0 mA	[3]
V_{OL}	Output Low Voltage	4.5V		TBD	0.7	V	I_{OL} = +12 mA 3 Pin Max	[3]
		5.5V		0.8	0.5	V	I_{OL} = +12 mA 3 Pin Max	[3]
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		10	6	mV		
		5.5V		25	7	mV		
V_{RST}	Auto Reset Voltage		1.55	2.7	2.4	V		
	Input Leakage	4.5V	–1.0	1.0	1.0	µA	V_{IN} = 0V, V_{CC}	
	Input Bias Current of Comparators	5.5V	1.0	1.0	1.0	µA	V_{IN} = 0V, V_{CC}	
	Output Leakage	4.5V	1.0	1.0	1.0	µA	V_{IN} = 0V, V_{CC}	
		5.5V	1.0	1.0	1.0	µA	V_{IN} = 0V, V_{CC}	
V_{ICR}	Input Common Mode Voltage Range		0	V_{CC}–1.0		V		

Symbol	Parameter	V_{cc}	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions
	Supply Current (Standard Mode	4.5V		4.0	2.2	mA	All Output and I/O Pins Floating @ 2 MHz
		5.5V		7.0	5.0	mA	All Output and I/O Pins Floating @ 2 MHz
		4.5V		9.0	4.5	mA	All Output and I/O Pins Floating @ 8 MHz
		5.5V		11.0	8.3	mA	All Output and I/O Pins Floating @ 8 MHz
		4.5V		13	6.1	mA	All Output and I/O Pins Floating @ 12 MHz (E08)
		5.5V		15	10.5	mA	All Output and I/O Pins Floating @ 12 MHz (E08)
	Standby Current (Standard Mode)	4.5V		2.5	0.5	mA	HALT mode V_{IN} = 0V, V_{cc} @ 2 MHz
		5.5V		4.0	1.1	mA	HALT mode V_{IN} = 0V, V_{cc} @ 2 MHz
		4.5V		4.0	1.0	mA	HALT mode V_{IN} = 0V, V_{cc} @ 8 MHz
		5.5V		5.0	2.0	mA	HALT mode V_{IN} = 0V, V_{cc} @ 8 MHz
		4.5V		5.0	1.3	mA	HALT mode V_{IN} = 0V, V_{cc} @ 12 MHz (E08)
		5.5V		7.0	2.3	mA	HALT mode V_{IN} = 0V, V_{cc} @ 12 MHz (E08)
I_{cc}	Supply Current (Low Noise Mode)	4.5V		4.0	2.2	mA	All Output and I/O Pins Floating @ 1 MHz
		5.5V		7.0	4.2	mA	All Output and I/O Pins Floating @ 1 MHz
		4.5V		5.0	2.9	mA	All Output and I/O Pins Floating @ 2 MHz
		5.5V		9.0	5.5	mA	All Output and I/O Pins Floating @ 2 MHz
		4.5V		8.0	4.4	mA	All Output and I/O Pins Floating @ 4 MHz
		5.5V		11.0	7.9	mA	All Output and I/O Pins Floating @ 4 MHz

DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions
	Standby Current (Low Noise Mode	4.5V		1.2	0.4	mA	HALT mode V_{IN} = 0V V_{CC} @ 1 MHz
		5.5V		1.6	0.9	mA	HALT mode V_{IN} = 0V V_{CC} @ 1 MHz
		4.5V		1.5	0.5	mA	HALT mode V_{IN} = 0V V_{CC} @ 2 MHz
		5.5V		1.9	1	mA	HALT mode V_{IN} = 0V V_{CC} @ 2 MHz
		4.5V		2.0	0.8	mA	HALT mode V_{IN} = 0V V_{CC} @ 4 MHz
		5.5V		2.4	1.3	mA	HALT mode V_{IN} = 0V, V_{CC} @ 4 MHz
	Standby Current	4.5V		10	1.0	µA	STOP mode V_{IN} = 0V, V_{CC} WDT is not Running
		5.5V		10	1.0	µA	STOP mode V_{IN} = 0V, V_{CC} WDT is not Running
I_{ALL}	Auto Latch Low Current	4.5V		10	6.0	µA	$0V < V_{IN} < V_{CC}$
		5.5V		15	11.5	µA	$0V < V_{IN} < V_{CC}$
I_{ALH}	Auto Latch High Current	4.5V		-7.0	-3.3	µA	$0V < V_{IN} < V_{CC}$
		5.5V		-7.0	-6.5	µA	$0V < V_{IN} < V_{CC}$

Notes:

(1) I_{CC1}

	Typ	Max	Unit	Freq
Clock Driven	0.3	5.0	mA	8 MHz
Crystal or Resonator	3.5	5.0	mA	8 MHz

(2) V_{SS} = 0V = GND

AC ELECTRICAL CHARACTERISTICS

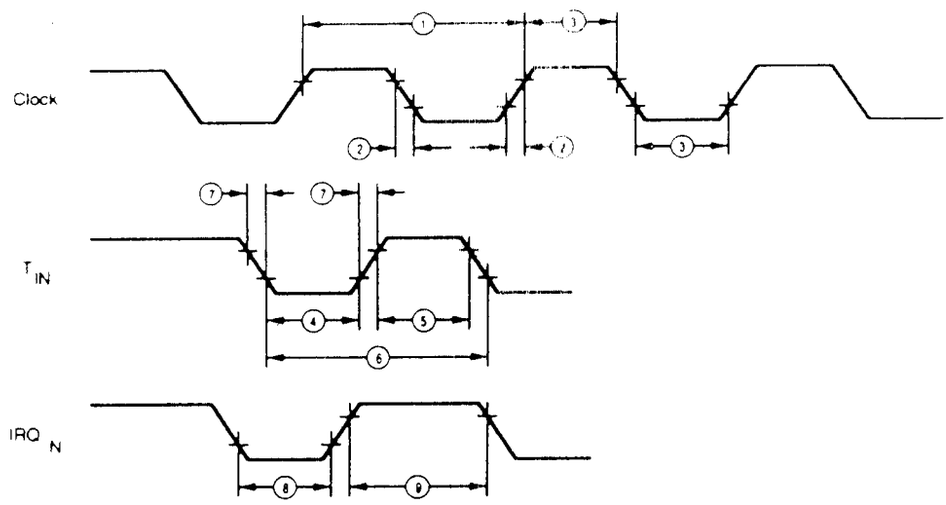


Figure 23. Electrical Timing Diagram

AC ELECTRICAL CHARACTERISTICS

EMA Noise Mode

				T_A = 0°C to +70°C					
				1 MHz		4 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	4.5V	1000	DC	250	DC	ns	[1]
			5.5V	1000	DC	250	DC	ns	[1]
2	TrC,TfC	Clock Input Rise and Fall Times	4.5V		25		25	ns	[1]
			5.5V		25		25	ns	
3	TwC	Input Clock Width	4.5V	500		125		ns	[1]
			5.5V	500		125		ns	[1]
4	TwTinL	Timer Input Low Width	4.5V	100		100		ns	[1]
			5.5V	70		70		ns	[1]
5	TwTinH	Timer Input High Width	4.5V	2.5TpC		2.5TpC			[1]
			5.5V	2.5TpC		2.5TpC			[1]
6	TpTin	Timer Input Period	4.5V	4TpC		4TpC			[1]
			5.5V	4TpC		4TpC			[1]
7	TrTin, TfTin	Timer Input Rise and Fall Timer	4.5V		100		100	ns	[1]
			5.5V		100		100	ns	[1]
8	TwIL	Int. Request Input Low Time	4.5V	100		100		ns	[1,2]
			5.5V	70		70		ns	[1,2]
9	TwIH	Int. Request Input High Time	4.5V	2.5TpC		2.5TpC			[1]
			5.5V	2.5TpC		2.5TpC			[1,2]
10	Twdt	Watch-Dog Timer Delay Time	4.5V		15		15	ms	[1]
			5.5V		10		10	ms	[1]
11	POR	Power-On Reset Time	4.5V	15		10		ms	[1]
			5.5V	15		10		ms	[1]

Notes:
[1] Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
[2] Interrupt request through Port 3 (P33-P31)

AC ELECTRICAL CHARACTERISTICS
Standard Mode, Standard Temperature

				T_A = 0°C to +70°C					
				8 MHz (E04)		12 MHz (E08)			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	4.5V	125	DC	83	DC	ns	[1]
			5.5V	125	DC	83	DC	ns	[1]
2	TrC,TfC	Clock Input Rise and Fall Times	4.5V		25		15	ns	[1]
			5.5V		25		15	ns	
3	TwC	Input Clock Width	4.5V	62		41		ns	[1]
			5.5V	62		41		ns	[1]
4	TwTinL	Timer Input Low Width	4.5V	100		100		ns	[1]
			5.5V	70		70		ns	[1]
5	TwTinH	Timer Input High Width	4.5V	5TpC		5TpC			[1]
			5.5V	5TpC		5TpC			[1]
6	TpTin	Timer Input Period	4.5V	8TpC		8TpC			[1]
			5.5V	8TpC		8TpC			[1]
7	TrTin TfTin	Timer Input Rise and Fall Timer	4.5V		100		100	ns	[1]
			5.5V		100		100	ns	[1]
8	TwIL	Int. Request Input Low Time	4.5V	100		100		ns	[1,2]
			5.5V	70		70		ns	[1,2]
9	TwIH	Int. Request Input High Time	4.5V	5TpC		5TpC			[1]
			5.5V	5TpC		5TpC			[1,2]
10	Twdt	Watch-Dog Timer Delay Time	4.5V		15		15	ms	[1]
			5.5V		10		10	ms	[1]
11	TPOR	Power-On Reset Timer	4.5V		60		60	ms	[1]
			5.5V		45		45	ms	[1]

Notes:
[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request through Port 3 (P33-P31)

Z8 CONTROL REGISTERS

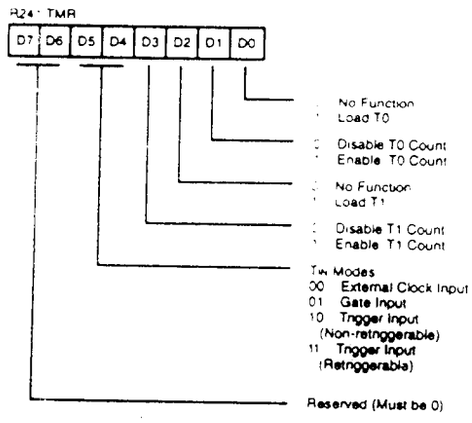


Figure 24. Timer Mode Register
(F1H: Read/Write)

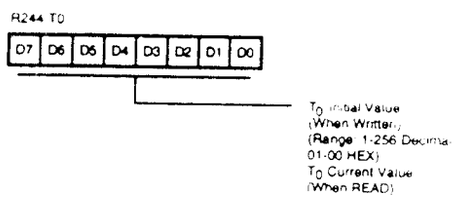


Figure 27. Counter/Timer 0 Register
(F4H: Read/Write)

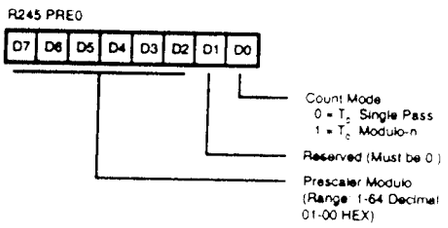


Figure 28. Prescaler 0 Register
(F5H: Write Only)

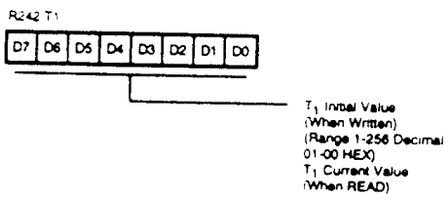


Figure 25. Counter Timer 1 Register
(F2H: Read/Write)

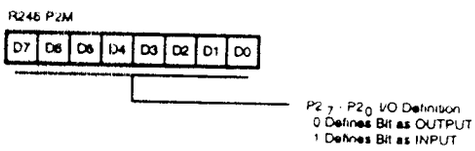


Figure 29. Port 2 Mode Register
(F6H: Write Only)

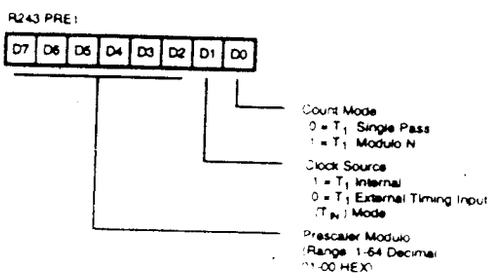


Figure 26. Prescaler 1 Register
(F3H: Write Only)

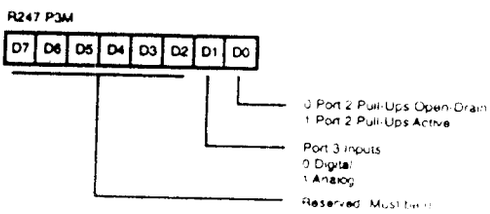


Figure 30. Port 3 Mode Register
(F7H: Write Only)

Z8 CONTROL REGISTERS (Continued)

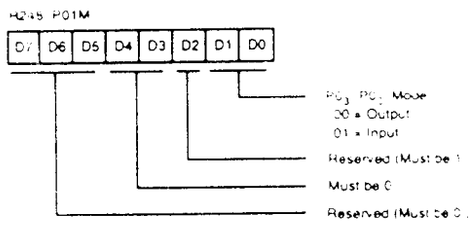


Figure 31. Port 0 and 1 Mode Register
(F8H: Write Only)

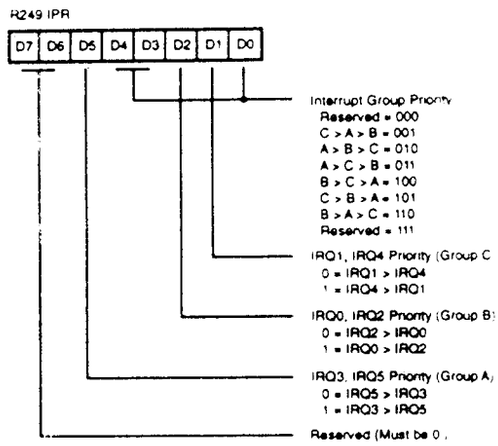


Figure 32. Interrupt Priority Register
(F9H: Write Only)

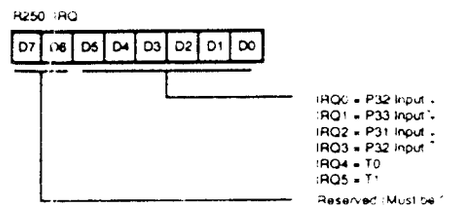


Figure 33. Interrupt Request Register
(FAH: Read/Write)

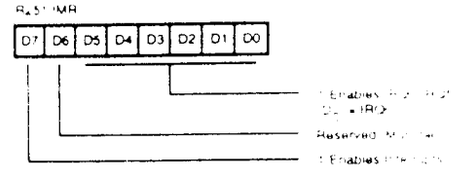


Figure 34. Interrupt Mask Register
(FBH: Read/Write)

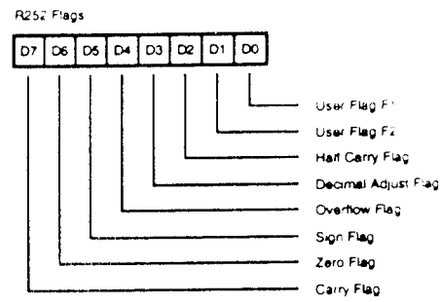


Figure 35. Flag Register
(FCH: Read/Write)

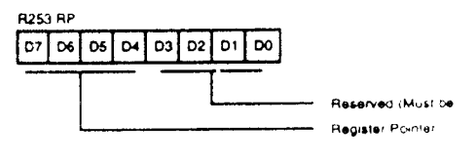


Figure 36. Register Pointer
(FDH: Read/Write)

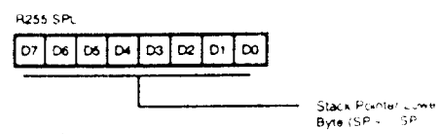


Figure 37. Stack Pointer
(FFH: Read/Write)

OPERATING MODES

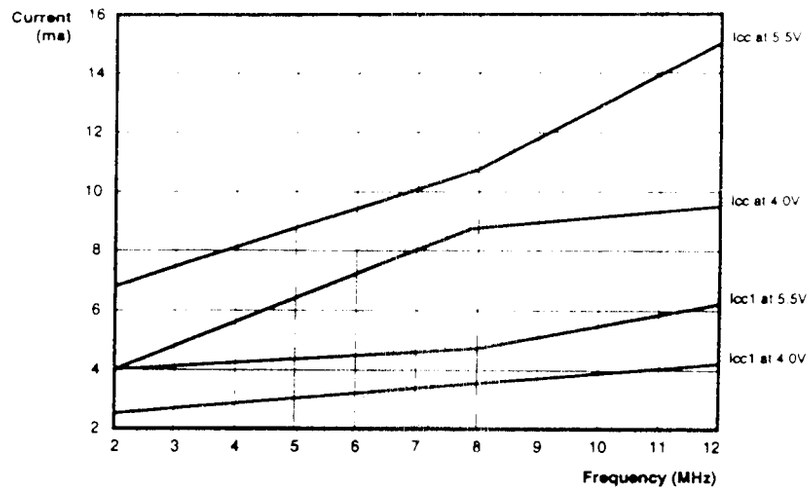


Figure 38. Maximum I_{CC} and I_{CC1} vs Frequency in Standard Mode

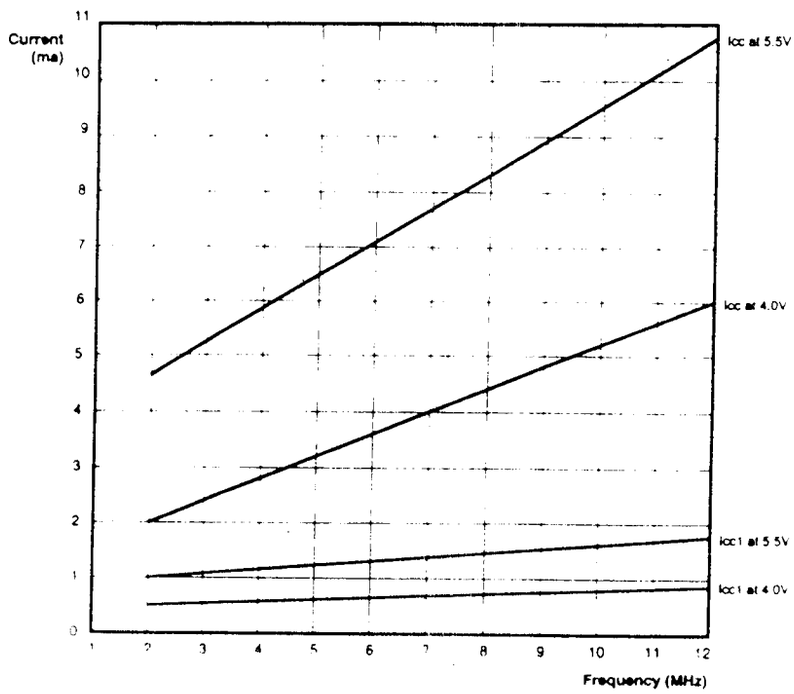


Figure 39. Typical I_{CC} and I_{CC1} vs Frequency in Standard Mode

OPERATING MODES (Continued)

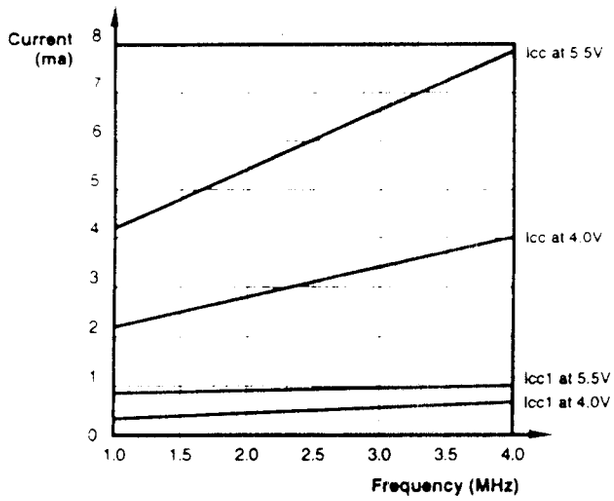


Figure 40. Typical I_{CC} and I_{CC1} vs Frequency in Low EMI Mode

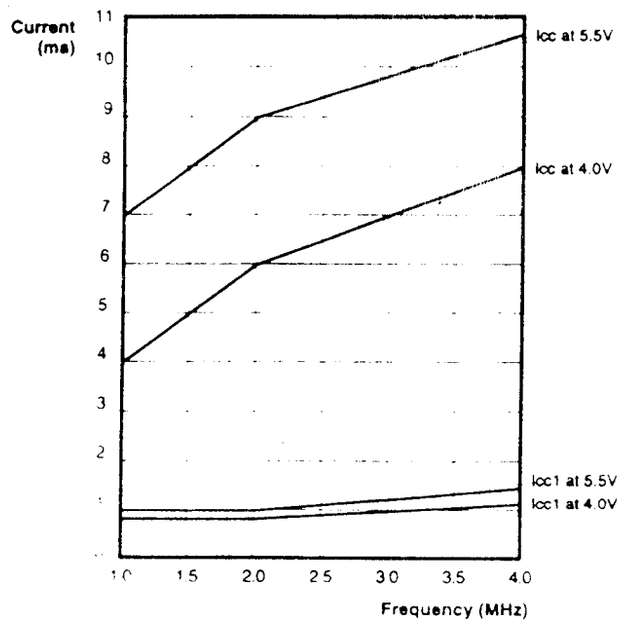


Figure 41 Maximum I_{CC} and I_{CC1} vs Frequency in Low EMI Mode

4

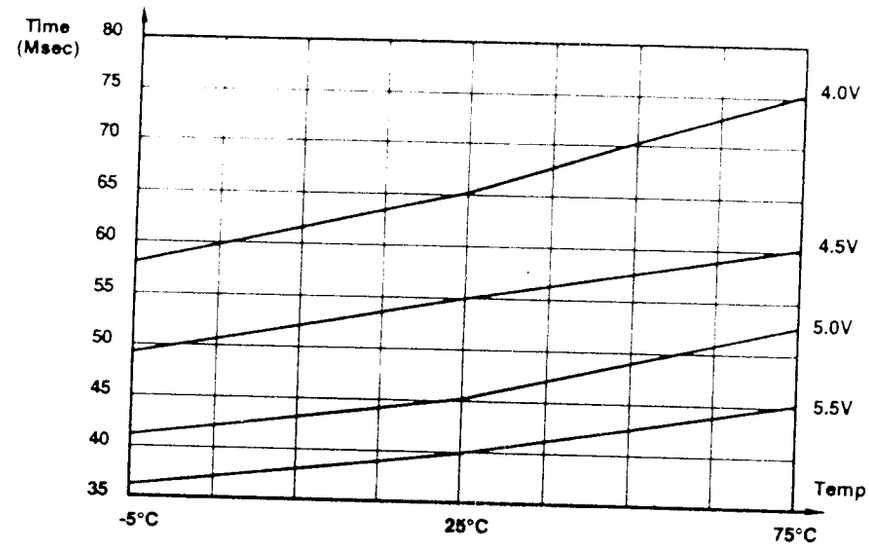


Figure 42. Typical POR Time Out Period vs Temperature

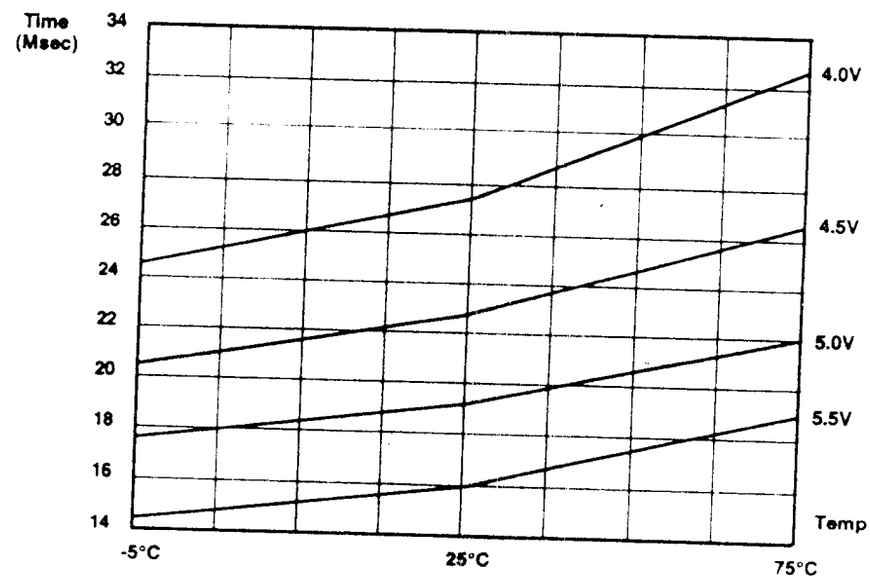


Figure 43. Typical WDT Time Out Period vs Temperature

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary

Symbol	Meaning
RR	Indirect register pair or indirect working-register pair address Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack pointer
PC	Program counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by

0	Clear to zero
1	Set to one
*	Set to clear according to operation
	Unaffected
X	Undefined

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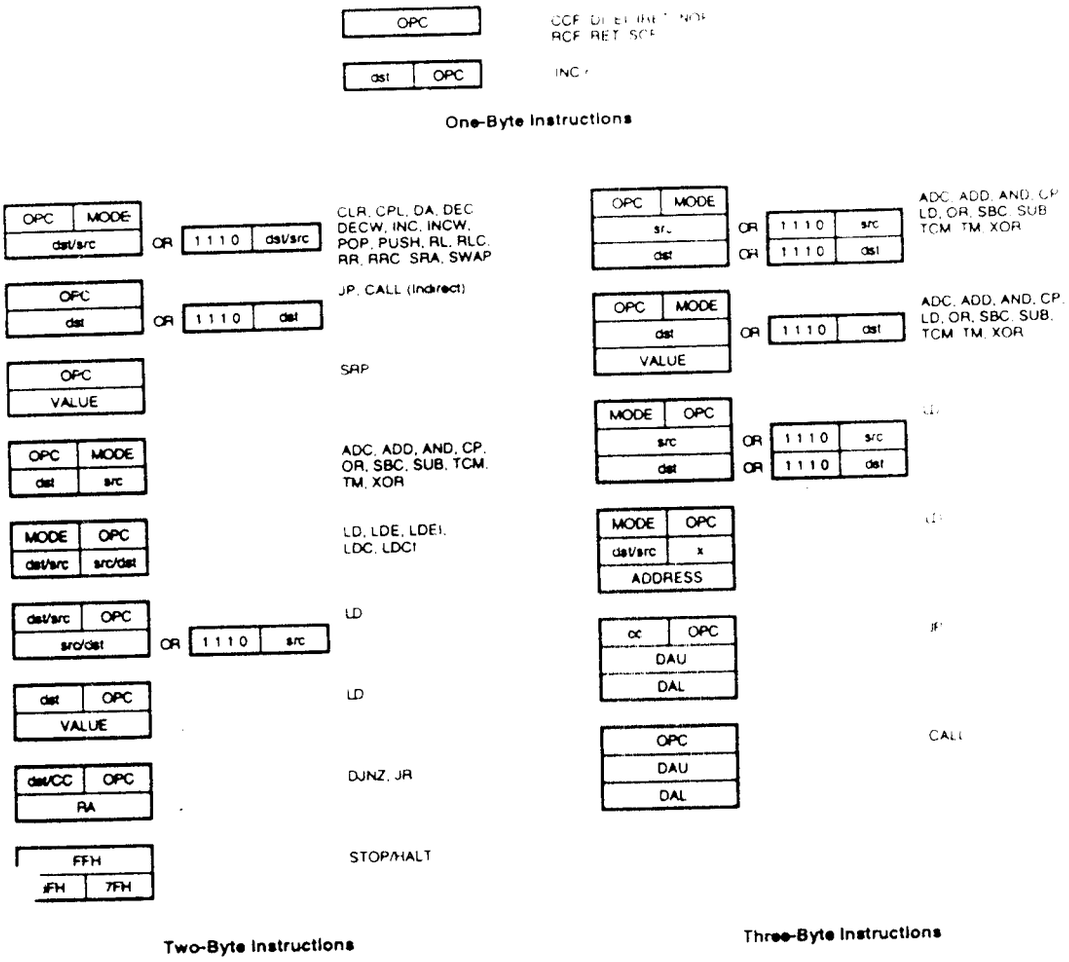
CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000	--	Always true	---
0111	C	Carry	C=1
1111	NC	No Carry	C=0
0110	Z	Zero	Z=1
1110	NZ	Not zero	Z=0
1101	PL	Plus	S=0
0101	MI	Minus	S=1
0100	OV	Overflow	V=1
1100	NOV	No overflow	V=0
0110	EQ	Equal	Z=1
)	NE	Not equal	Z=0
1001	GE	Greater than or equal	(S XOR V)=0
0001	LT	Less than	(S XOR V)=1
1010	GT	Greater than	[Z OR (S XOR V)]=0
0010	LE	Less than or equal	[Z OR (S XOR V)]=1
1111	UGE	Unsigned greater than or equal	C=0
0111	ULT	Unsigned less than	C=1
1011	UGT	Unsigned greater than	(C = 0 AND Z=0)=1
0011	ULE	Unsigned less than or equal	(C OR Z)=1
0000	F	Never true (Always False)	---

INSTRUCTION FORMATS



INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol "←". For example

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example

dst(7)

refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	C	Z	S	V	D	H
ADC dst, src dst←dst + src +C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP – 2 @SP←PC PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst – src	†		A[ ]	*	*	*	*		-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst – 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst – 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZ r, dst r←r – 1 if r ≠ 0 PC←PC + dst Range: +127, –128	RA		rA r = 0 - F	-		-	-	-	-
EI IMR(7)←1			9F						
HALT			7F						

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	C	Z	S	V	D	H
INC dst dst←dst + 1	r		E r = 0 - F		*	*	*		
	R		20						
	IR		21						
INCW dst dst←dst + 1	RR		A0		*	*	*		
	IR		A1						
IRET FLAGS←@SP SP←SP + 1 PC←@SP SP←SP + 2 IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true PC←dst	DA		cD c = 0 – F						
	IRR		30						
JR cc, dst if cc is true, PC←PC + dst Range: +127, –128	RA		cB c = 0 – F						
LD dst, src dst←src	r	Im	rC						
	r	R	r8						
	R	r	r9						
			r = 0 – F						
	r	X	C7						
	X	r	D7						
	r	Ir	E3						
	Ir	r	F3						
	R	R	E4						
	R	IR	E5						
	R	IM	E6						
	IR	IM	E7						
	IR	R	F5						
LDC dst, src dst←src	r	Irr	C2						
LDCI dst, src dst←src r←r + 1 rr←rr + 1	Ir	Irr	C3						

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
NOP		FF	
OR dst, src dst←dst OR src	†	4[ ]	* * 0 -
POP dst @SP SP←SP + 1	R IR	50 51	
PUSH src SP←SP − 1 @SP←src	R IR	70 71	
RCF C←0		CF	0 - - -
RET PC←@SP SP←SP + 2		AF	
RL dst	R IR	90 91	* * * * - -
RLC dst	R IR	10 11	* * * * - -
RR dst	R IR	E0 E1	* * * * - -
dst	R IR	C0 C1	* * * * - -
SBC dst, src dst←dst − src − C	†	3[ ]	* * * * 1 *
SCF C←1		DF	1 - - - - -
SRA dst	R IR	D0 D1	* * * 0 -
SRP dst RP←src	Im	31	

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
STOP		6F	
SUB dst, src dst←dst − src	†	2[ ]	* * * * 1 *
SWAP dst	R IR	F0 F1	X * * X - -
TCM dst, src (NOT dst) AND src	†	6[ ]	* * 0 -
TM dst, src dst AND src	†	7[ ]	* * 0 -
WDH		4F	- - -
WDT		5F	X X X
XOR dst, src dst←dst XOR src	†	B[ ]	* * 0 -

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	Address Mode src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

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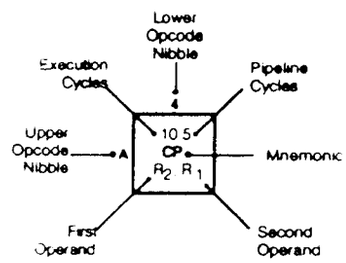
OPCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								4.0 **WDH**
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								5.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1														8.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1														9.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1.x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1			20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2.x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1										6.0 **NOP**
Bytes per Instruction	2			3					2				3		1	



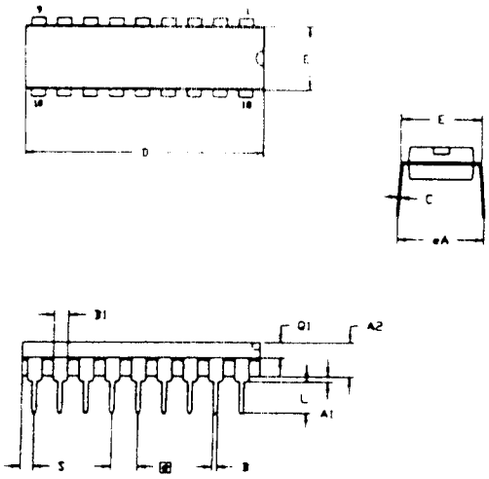
Legend:
R = 8-bit address
r = 4-bit address
R_1 or r_1 = Dst address
R_2 or r_2 = Src address

Sequence:
Opcode, First Operand
Second Operand

Note: Blank areas not defined

* 2-byte instruction appears as a 3-byte instruction

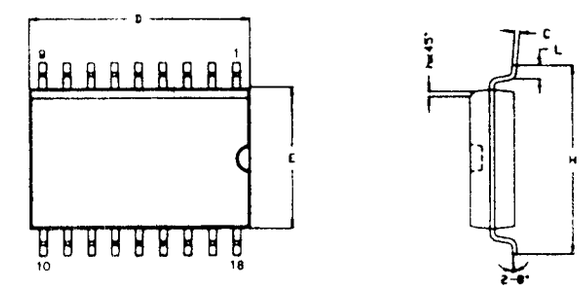
PACKAGE INFORMATION

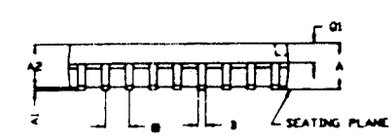


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	020	032
A2	3.25	3.43	128	135
B	0.38	0.53	.015	021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	920
E	7.62	8.13	.300	320
E1	6.22	6.48	245	255
eB	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	350
L	3.18	3.81	125	150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS - INCH

18-Pin DIP Package Diagram





SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	11.40	11.75	.449	.463
E	7.40	7.60	.291	.299
e	1.27 TYP		.050 TYP	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

CONTROLLING DIMENSIONS - MM
LEADS ARE COPLANAR WITHIN .004 INCH

18-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86E08	Z86E04
12 MHz	**8 MHz**
Z86E0812PSC	Z86E0408PSC
Z86E0812SSC	Z86E0808SSC

For fast results, contact your local Zilog sales office or technical center for assistance in ordering the part desired

Package
P = Plastic DIP
S = SOIC

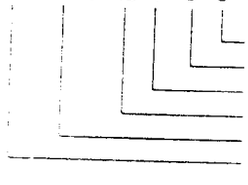
Temperature
S = 0°C to +70°C

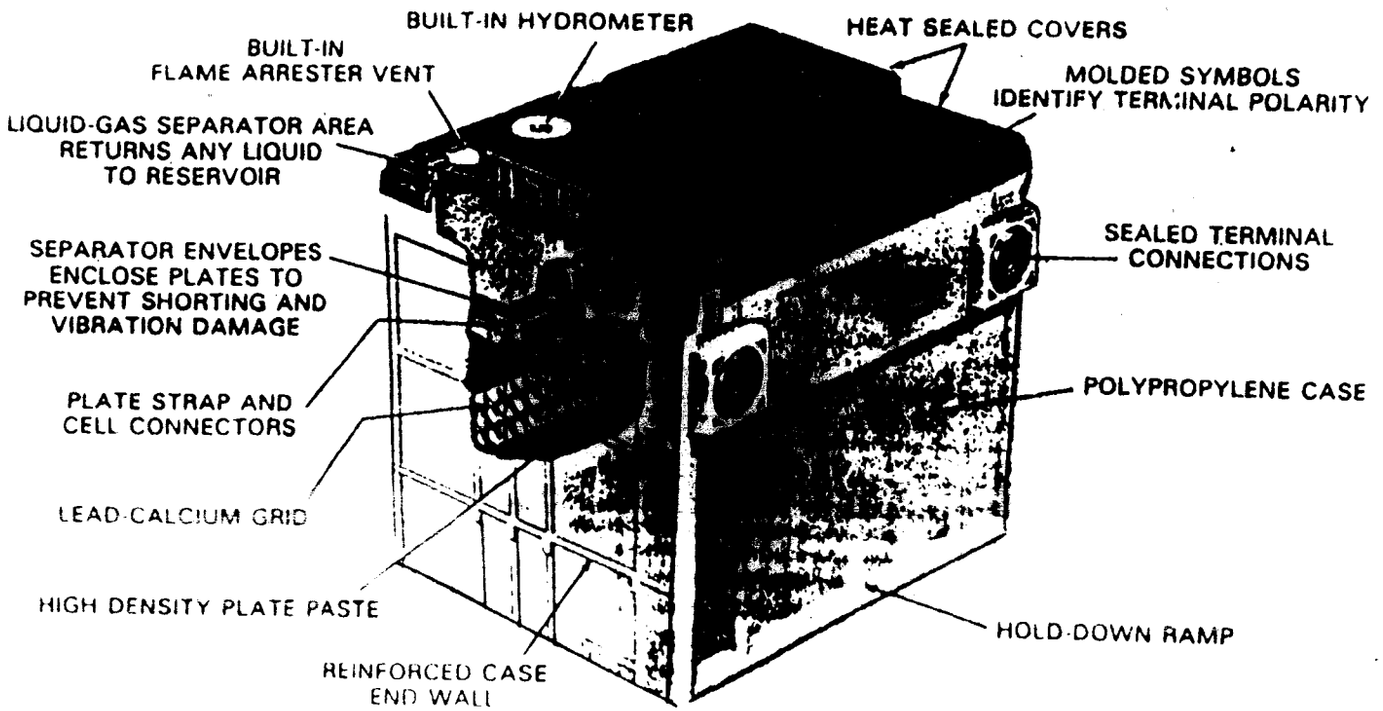
Speeds:
12 = 12 MHz
8 = 8 MHz

Environmental
C= Plastic Standard

Example:

Z 86E08 12 P S C is an Z86E08, 12 MHz, DIP, 0°C to +70°C, Plastic Standard Flow





A typical 12 volt side terminal battery. Note sealed construction and use of built in hydrometer. (General Motors)

regularly undertaken. The general diagram of a 12 V battery is enclosed page over.

5.1.6. BATTERY SERVICE

The battery plays a key role in the overall functioning of the electrical system. To insure reliability and to extend useful service life, the battery should receive periodic inspection and maintenance.

A visual inspection will help to determine which maintenance services are needed. Typical needs could include; cleaning of cable terminals, battery posts, and battery top; adding distilled water to cells (not needed with maintenance - free battery); tightening battery hold down; battery charging, or replacement.

BATTERIES CAN BE DANGEROUS

Battery electrolyte contains about 38 per cent sulphuric acid and can cause serious skin and eye burns. If the electrolyte comes in contact with the skin, flush the area with large quantities of cold water. If in the eyes, flush with cold water and then consult a physician. Battery acid on the car or on clothing should be flushed with cold water. Follow with a mixture of baking soda and water to neutralize the acid.

The following safety rules should be observed at all times:

1. When handling battery electrolyte, wear goggles and rubber gloves. 2. If mixing sulphuric acid and water to make an electrolyte mixture POUR ACID INTO WATER, DO NOT POUR WATER INTO ACID. Add acid slowly and stir constantly with a clean stick.

3. Never strike a spark, light a match, or bring other open flames near a battery. The charging process creates a mixture of hydrogen and oxygen gases which can ignite and burn with EXPLOSIVE FORCE. This could rupture the battery case and throw acid over a wide area.

4. Use a properly fitted lift strap to move batteries.

5. When a battery is removed from the car, place where it will not be knocked over, dropped, or exposed to sparks or flame.

6. Store battery acid or dry-charge battery electrolyte where the containers will be safe from breakage.

BATTERY VISUAL CHECK

Examine the battery for signs of corrosion, cracking, and leakage. Inspect hold-down terminals, cables, and electrolyte level.

IMPORTANT NOTE : When testing either DC generator or alternator systems, instructions provided by the manufacturer of the test equipment should be carefully followed. Be sure to use specifications, voltage drop, current output, and voltage output speficied for the exact make and model being tested.

5.1.7. REGULATOR:

The regulator we make use of in our system is the 7805 regulator. The function of this regulator is to step down the 12 V supply given by the car battery to 5 V for digital applications.

This series of fixed-voltage monolithic integrated circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these

uA7805C and uA7805Q electrical characteristics at specified virtual junction temperature, V_I = 10 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	MIN	TYP	MAX	UNIT
Output voltage‡		25°C	4.8	5	5.2	V
	I_O = 5 mA to 1 A, V_I = 7 V to 20 V, $P \leq 15$ W	Full range§	4.75		5.25	
Input regulation	V_I = 7 V to 25 V	25°C		3	100	mV
	V_I = 8 V to 12 V				50	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz	Full range§	62	78		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		15	100	mV
	I_O = 250 mA to 750 mA			5	50	
Output resistance	f = 1 kHz	Full range§		0.01		Ω
Temperature coefficient of output voltage	I_O = 5 mA	Full range§		-1.1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		40		μV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		4.2	8	mA
Bias current change	V_I = 7 V to 25 V	Full range§			1.3	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		750		mA
Peak output current		25°C		2.2		A

uA7806C electrical characteristics at specified virtual junction temperature, V_I = 11 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	MIN	TYP	MAX	UNIT
Output voltage‡		25°C	5.75	6	6.25	V
	I_O = 5 mA to 1 A, V_I = 8 V to 21 V, $P \leq 15$ W	0°C to 125°C	5.7		6.3	
Input regulation	V_I = 8 V to 25 V	25°C		5	120	mV
	V_I = 9 V to 13 V			1.5	60	
Ripple rejection	V_I = 9 V to 19 V, f = 120 Hz	0°C to 125°C	59	75		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		14	120	mV
	I_O = 250 mA to 750 mA			4	60	
Output resistance	f = 1 kHz	0°C to 125°C		0.019		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		-0.8		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		45		μV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		4.3	8	mA
Bias current change	V_I = 8 V to 25 V	0°C to 125°C			3	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		550		mA
Peak output current		25°C		2.2		A

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a [illegible] μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

§ Full range virtual junction temperature is 0°C to 125°C for the uA7805C and -40°C to 125°C for the uA7805Q.

FREE-AIR TEMPERATURE
DISSIPATATION DERATING CURVE

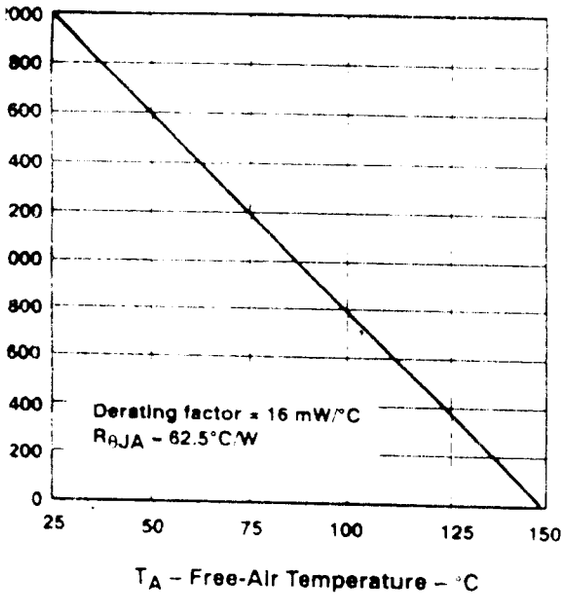


Figure 1

CASE TEMPERATURE
DISSIPATION DERATING CURVE

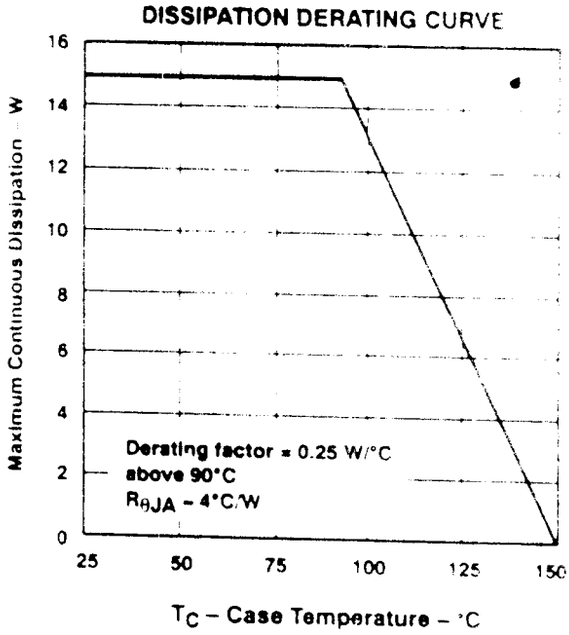
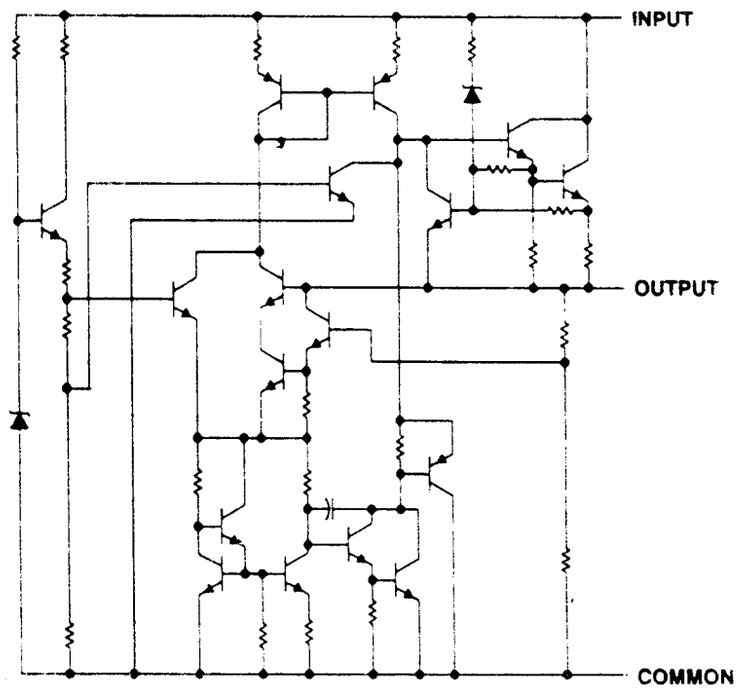


Figure 2

ommended operating conditions

		MIN	MAX	UNIT
t voltage V_I	uA7805C	7	25	
	uA7806C	8	25	
	uA7808C	10.5	25	
	uA7885C	10.5	25	
	uA7810C	12.5	28	
	uA7812C	14.5	30	
	uA7815C	17.5	30	
	uA7818C	21	33	
	uA7824C	27	38	
put current, I_O			1.5	A
erating virtual junction temperature, T_J	uA7800C Series	0	125	°C
	uA7805Q, uA7812Q	−40	125	

schematic



absolute maximum ratings over operating temperature ranges (unless otherwise noted)

Input voltage:	uA7824C	40 V
	All others	35 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 1)		2 W
Continuous total dissipation at (or below) 90°C case temperature (see Note 1)		15 W
Operating free-air, case, or virtual junction temperature range		−40 to 150°C
Storage temperature range		−65 to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

NOTE 1: For operation above 25°C free-air or 90°C case temperature, refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

regulators can deliver up to 1.5 A of output current. The internal current limiting and thermal shutdown features of these regulators make them essentially immune to overload. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power pass element in precision regulators. The uA7800C series is characterizes for operation over the virtual junction temperature range of $0^{o}C$ to $125^{o}C$. The uA7805Q and uA7812Q are characterized for operation over the virtual junction temperature range of $-40^{o}C$ to $125^{o}C$.

5.1.7 BUZZER:

When the password given is wrong, then the relay closes and the buzzer sounds. This is used as an indication to the owner to know that his car is being tempered with. The buzzer used can operate over a voltage range of 1.5 to 27V DC.

5.1.8. IGNITION IMMOBILISER :

This is used to prevent the thief from driving away with the car inspite of the alarm. When the password given is wrong, then the relay opens and the ignition is cut off.

The details of this ignition system can be found in the forthcoming chapter.

5.1.9. LIMIT SWITCHES :

Highly reliable limit switches are placed in the bonnet so as to ensure any burglar from stealing away the engine, Horn, Carburetter and pumps etc.

X. CONCLUSION

The system designed by us was after looking into all the constraints posed.To put in a different angle, the system was designed after putting us into the role of a burglar who struggles to outwit the system rightly.

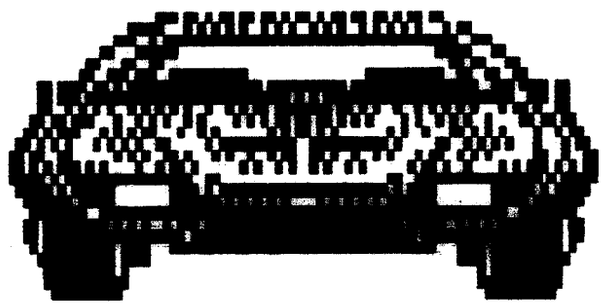
There was a series of data collection, survey and a thorough analysis of what and how the public had suffered and the entire project was worked upon only after recieving proper suggestions given by the victims of car burglary and also some renowned industrialists.

With the stride and advancement in the field of Electronics and IC technology, we public should look in for an entire foolproof system in order to avoid losses.

The scope for an innovative anti-theft system has been hidden for the past decade and the evolution of such a system would be a wonderful output for our fellow people. Also, there is very less task to do for the owner in operating the system.

The discrete model of this system was also tested in the Laboratory environment and their characteristics were studied. The components in that model included DAC, Counters, Displays etc. Based on this prototype model, an advanced design using a " LVDT" transducer was tested successfully.

But, to reduce the cost and size of the system and to increase the reliability, the discrete model has been modified using micro controller. Now "PRICOL" is assisting us to technically promote the system and to further increase its sophistication.



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XI. BIBLIOGRAPHY

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