P-1309

Micro Computer - 80186 Based ECG Monitor - Optional Portable LCD Model

PROJECT REPORT

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In partial fulfilment of the requirements for the award of the Degree of

BACHELOR OF ENGINEERING IN ELECTRONICS AND COMMUNICATION ENGINEERING

of the Bharathiar University, Coimbatore.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Kumaraguru College of Technology

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APRIL 1995

DEPARTMENT OF
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KUMARAGURU COLLEGE OF TECHNOLOGY

COIMBATORE - 641 006

CERTIFICATE

This is to Certify that the Report Entitled

MICROCOMPUTER - 80186 BASED ECG MONITOR

- OPTIONAL PORTABLE LCD MODEL

HAS BEEN SUBMITTED BY

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in partial fulfilment for the award of the Degree of Bachelor of Engineering in Electronics and Communication Engineering Branch of the Bharathiar University, Coimbatore - 641 046 during the academic year 1994 - 95

GUIDE

HEAD OF THE DEPT

Certified that the candidate was examined by us in the Project work Viva-Voce examination held on 6-4-95

and the University Register Number was _____

INTERNAL EXAMINER

EXTERNAL EXAMINER

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CERTIFICATE

This is to certify that the following students of Final year, Electronics and Communication Engineering branch of Kumaraguru College of Technology, have been associated with our R & D (Electronics) Department, concerning a Product Development, throughout their Final year. The product, **Portable ECG Analyser** with LCD display, is proceeding as per schedule and is expected to be completed by June, 1995.

The conduct and interest shown by the students is good.

The students are:

R.Sakthidharan
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Dedicated to our
beloved parents,
teachers & friends

Acknowledgement

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Synopsis

SYNOPSIS

The best known application of Computers in Medical diagnosis, is their use in analysing and evaluating Electrocardiograms.

In this project, we have built an ECG analyser with an interface to Micro Computer. In this system, the ECG signal, which is picked by the electrode placed on various parts of human body is amplified, processed and the ECG waveform is made available at the CRT monitor of Microcomputer. For implementing this system a powerful 80186 processor is used. It's speed flexibility and its memory accessing capability being advantageous.

A generalised processor board is implemented with facilities in excess of the requirements of a data acquistion system to make on-board emulation possible. The software is also made intelligent enough for limited analysis.

Further, we wish to make this system, a portable module, with a graphic LCD display, under the auspicies of our backers, M/s. PRICOL Industries, Coimbatore.

Introduction

INTRODUCTION

The ability of Electronic Computers to store very large quantities of data and to have it readily available for further processing makes them extremely useful in a Hospital setup. In Clinical application, the object of the use of the computer is to make a contribution to better and quicker diagnosis, and treatment free from subjective errors. The computer does in no way relieve the physician of the task of making a decision but at the same time it provides him information on the clinical examinations in a clearer form and saves him from drudgery of doing repetitive and routine calulations. An additional advantage is that of storage of clinical patient data for future study and analysis.

The ECG is got from human body as a differential summation of potential at two points. This is taken to the computer by suitable means, where processing includes digital filtering, removal of artefact, averaging of complexes and fully automated measurement of the P,QRS,T wave amplitudes and duration.

Chapter I tries to explain the basics of Electrocardigraphy and describes the normal Electrogram complex. It also contains notes on various lead positions and bio potential sensors.

Chapter II gives an indepth coverage of the normal ECG amplifier and the characteristic features of INA102 Instrumentation amplifier used in this development.

Chapter III provides an overall view of the Designed system, explaining the functions and advantages of the various ICs used in the realisation of the Dataprocessing system.

Chapter IV gives the part played by the Intel 80186 processor used in our project, and explains salient features.

Chapter V gives the functions of the various on-board Peripherals used in the system and their related devices.

Chapter VI incorporates the realisation of the various designs, which indicate the practical effort put-in.

Chapters VII & VIII include the software required for the functioning of both the Dataprocessing and Display sytems.

The Electrocardiogram

THE ELECTROCARDIOGRAM

The Electrocardiogram is a reflection of the electrical activity of the heart. The ECG is a quasi-periodical, rhythmically repeating signal synchronised by the function of the heart, which acts as a generator of bio-electric events. The potentials originating in the individual fibres of the heart muscles are added to produce the ECG waveform. This generated signal can be described by means of a simple electric dipole, consisting of a pair of a positive and a negative charge. The dipole generates a field vector, changing nearly periodically in time and space and its effects are measured on the surface. Thus an ECG reflects the rhythmic electrical depolarisation and repolarisation of the myocardium (heart muscle) associated with the contraction of the atria and the ventricles. The shape, time interval and amplitude of the ECG give the details of state of the heart. Any form of Arrhythmia (disturbances in the heart rhythm) can be easily diagonised using the electrocardiogram.The heart is unique among the muscles of the body in that it posseses the property of automatic rhythemic contraction. The impulses necessary to maintain the pulsations, arise from a specialised location interior to the heart. The heartbeat is a spontaneous, periodic, electrical potential, originating in a small area of the heart muscle tissue, the Sinoatrial node. The fundamental beat generated in the S.A. node, first travels through the heart muscle to the atria, causing them to simultaneously contract. The electric wave then travels to the Atrioventricular node,

which permits transmission of the contractions, causing potentials to the venticles. These are conducted throughout the heart by dedicated fibres which result in the exitation of muscle fibres throughout the myocardium. The impulse formation and conduction also produces weak electric currents conducted to the body surface, from where these can be measured by connecting electrodes because they travel through the body which is an infinite homogenous conductor. The ECG is recorded as a the differential sum of the outputs of the various electrodes placed at different locations in the body.

ECG LEAD CONFIGURATIONS

To record an electrcardiogram, a number of elecrtrodes,usually twelve are affixed to the body of the patient. These leads are placed in three standardised electrode positions:

(1) Bipolar limb leads or Standard leads.

(2)Augmented unipolar limb leads.

(3) Chest leads or Precordial leads.

Bipolar limb leads :

These consist of the standard leads I, II and III. The three bipolar limb leads were first introduced by Einthoven. In these, the potentials are tapped from four locations of the body - (i) Right arm (RA), (ii) Left arm (LA), (iii)Right leg (RL), and (iv) Left leg (LL).

Usually the right leg electrode acts as the ground reference electrode. The lead positions (shown in fig.1.) are as follows:

Lead I : Left arm and Right arm.

Lead II : Left leg and Right arm.

Lead III : Left leg and Left arm.

The closed path RA to LA to LL and back to RA is called the EINTHOVEN TRIANGLE. According to Einthoven, in the Frontal plane of the body, the cardiac electric field vector is a two dimensional one. The ECG, measured from any one of the three limb leads, is a time varient, single dimensional component of that vector. Along the sides of this triangle, the three projections of the ECG vector are measured, as shown in fig.4. Further the vector sum of the projections on all the three sides is equal to zero. The relation between the three leads is expressed algebrically by Einthoven's equation:

Lead II = Lead I + Lead III.

This is based on Kirchoff's law, which states that the algebric sum of all the potential differences in a closed circuit is zero. If Einthoven had reversed the polarity of LeadII the three bipolar lead axes would result in a closed circuit and Leads I + II + III would equal zero. However, since Einthoven did make this alteration, in the polarity of the Lead II axis, the equation becomes: I - II + III = 0.

Hence, II = I + III.

The electrical potential as recorded from any one extremity will be the same no matter where the electrode is placed on the extremity. The electrodes are usually applied just above the wrists and ankles.

Augmented Unipolar limb leads:

In this system, introduced by Wilson, the ECG is recorded between a single exploratory electrode, and the central terminal, which has a potential corresponding to the centre of the body. This central terminal is obtained by connecting the three active limb electrodes together through resistors of same size. In Unipolar limb leads, one of the limb electrodes is used as an exploratory electrode as well as contributing to the central terminal. This double use results in an ECG signal, that has a very small amplitude. By means of Augmented ECG

lead connections, a small increase in the ECG voltage can be realised. The Augmented lead connections (shown in fig.2.) are:

(1) aVR - Augmented voltage Right arm.

(2) aVL - Augmented voltage Left arm.

(3) aVF - Augmented voltage foot.

Unipolar Chest leads :

In the case of Unipolar chest leads, the exploratory electrode is obtained from one of the chest electrodes. The chest electrodes are placed, on six different points of the chest, close to the heart, as shown in fig.3. These chest positions are called the PRECORDIAL UNIPOLAR LEADS, and are designated, V1 to V6. All the three active limb electrodes are used to obtain the central terminal, while a seperate chest electrode is used as an exploratory electrode. The common precordial electrode positions used are:

V1 : Fourth Intercostal space at right Sternal margin.

V2 : Fourth Intercostal space at left Sternal margin.

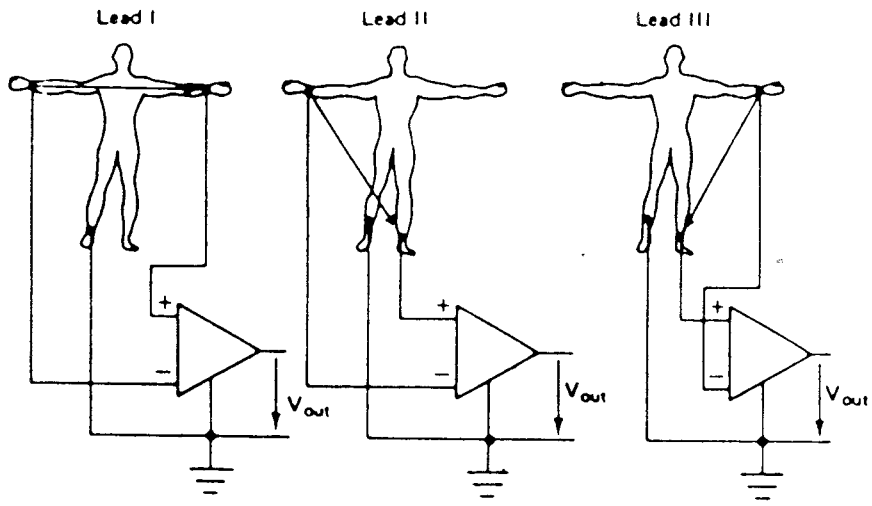
V3 : Midway betweeen V2 and V4.

V4 : Fifth Intercostal space in the Mid-clavicular line

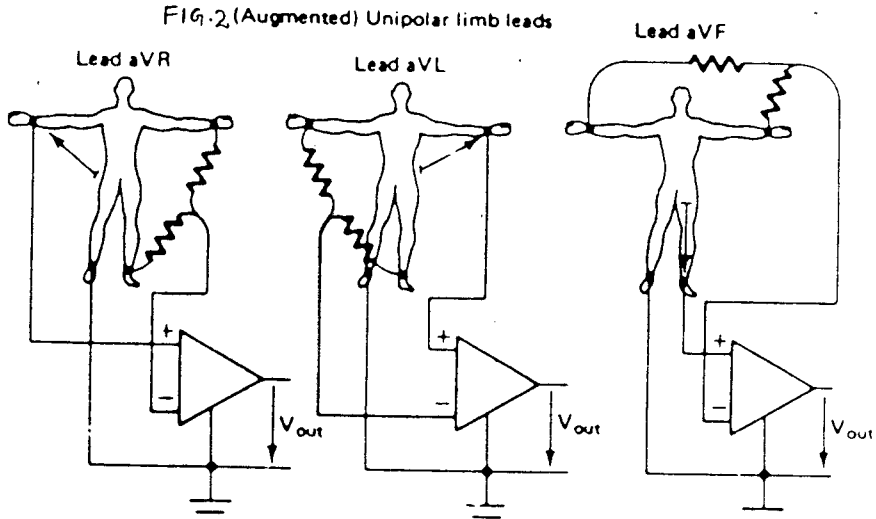
V5 : Anterior axilliary line.

V6 : Mid axillary line.

FIG·1 Bipolar limb leads



FIG·2 (Augmented) Unipolar limb leads



V_1 Fourth intercostal space, at right sternal margin.

V_2 Fourth intercostal space, at left sternal margin.

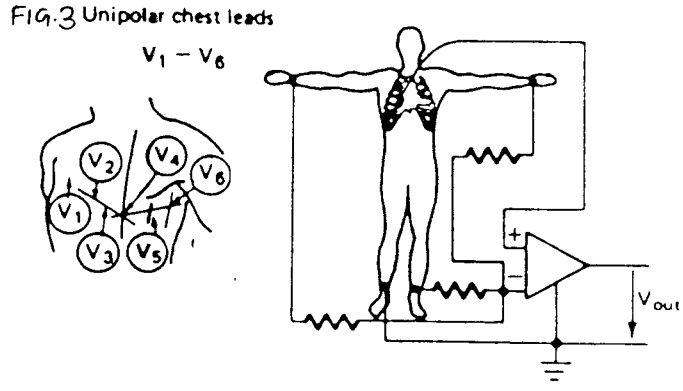
V_3 Midway between V_2 and V_4.

V_4 Fifth intercostal space, at mid-clavicular line.

V_5 Same level as V_4, on anterior axillary line.

V_6 Same level as V_4, on mid-axillary line.

FIG·3 Unipolar chest leads



ECG lead configurations.

Colour Code :

Normally, ECG potentials are measured with colour coded leads, according to convention, to facilitate their easy identification.The placement of electrodes as well as the colour codes used to identify each electrode is shown in fig.5.

White - Right Arm.

Black - Left Arm.

Green - Right Leg.

Red - Left Leg.

Brown - Chest.

BIOPOTENTIAL SENSORS

The most common type of electrodes used for recording ECG are rectangular or circular surface electrodes. The material used is german silver, nickel silver or nickel plated steel. They are applied to the surface of the body with electrode jelly. The typical value of contact impedance of these electrodes of normal sizes is nearly 2 to 5 kiloohms when measured at 10 Hz. The electrodes are held in position by elastic straps.They are also called limb electrodes as they are most suitable for applications on four limbs of the body.

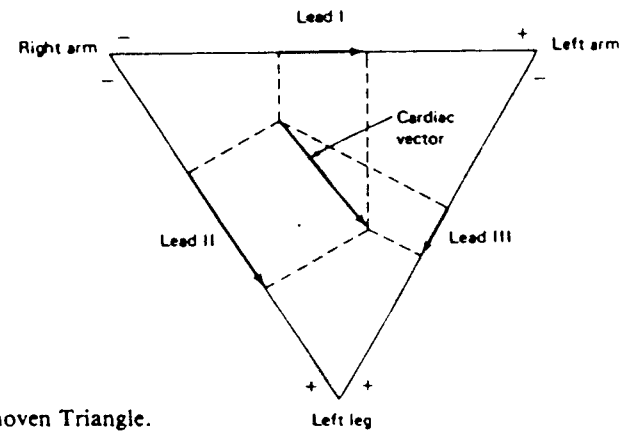


FIG. 4 The Einthoven Triangle.

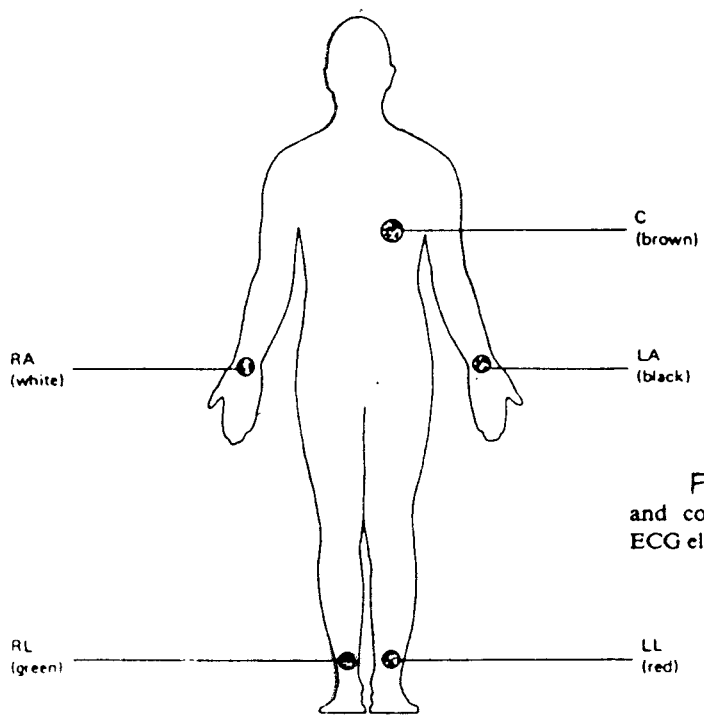


FIG. 5 Abbreviations and color codes used for ECG electrodes.

All types of biopotential electrodes have a metal - electrolyte interface. In each case, an electrode potential is developed across the interface proportional to the exchange of ions between the metal and electrolytes of the body. The potential across a membrane seperating two concentrations of an ion is given by Nernst equation:

$$E = -(RT/nF)\ln((C_1 f_1)/(C_2 f_2))$$

Where R - Gas constant ($8.315*10^7$ e/m/K).

T - Absolute Temperature (K).

n - Valence of the ion.

F - Faraday constant (96500 C).

C_1, C_2 - Two Concentrations of the ion on the two sides of the membrane.

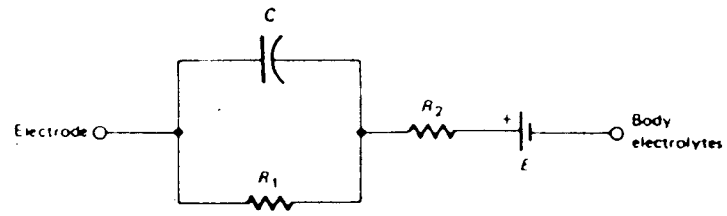
f_1, f_2 - Respective activity coeffients ofthe ion on the two sides of the membrane.

The double layer of charge at the interface acts as a charge. Since measurement of bioelectric potential requires two electrodes the voltage measured is really the difference between the instantaneous potentials of the two electrodes, as shown in fig8. If the two electrode are of the same type the output is the actual difference of ionic potential between the two points of the body. Mismatch of the two electrodes results in an electrode offset voltage, often mistaken for a true physilogical event. Also chemical activity within an electrode can cause voltage

fluctuations appering as noise on a biosignal. It is found that silver/silver-chloride electrode is very stable, so this is normally used for various applications.

The earliest bioelectric potential measurements used Immersion electrodes, which were simply buckets of saline solution, into which the subject placed his hands and feet. This type of electrode presented many difficulties, such as restricted position of the subject and danger of electrolyte spillage. A great improvement over the Immersion electrode was the Plate electrode. Originally, these electrodes were seperated from the subject skin by cotton pads, soaked in a strong saline solution. Later a conductive Jelly replaced the soaked pads. One of the difficulties in using plate electrodes was the possibility of electrode slippage or movement. Another type of electrode used today is the Suction-cup electrode. In this type, only the rim actually contacts the skin. All the preceeding electrodes suffer from a common problem. They are all sensitive to movement. Even the slightest movement changes the thickness of the thin film of electrolyte between the metal and the skin and thus causes change in the electrode potential and impedance.

Later a new type of electrode, the Floating electrode was introduced. The principle of this electrode is to practically eliminate movement artifacts by avoiding any direct contact of the metal with the skin. The only conductive path between metal and the skin is the



Equivalent circuit of biopotential electrode interface.

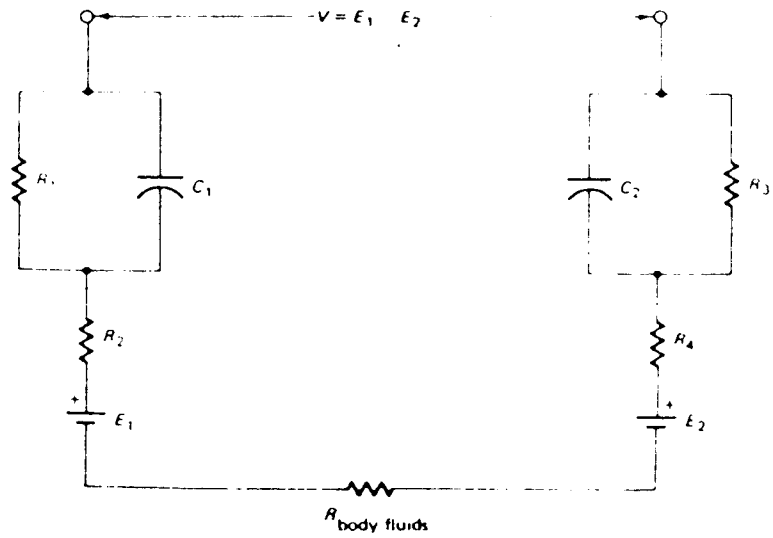
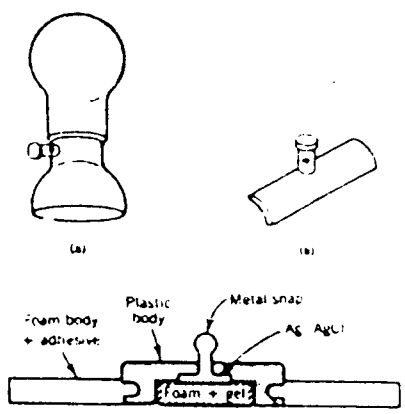


FIG. 8 Measurement of biopotentials with two electrodes—equivalent circuit



(c)

. Electrodes used in ECG recording (a) suction electrode, (b) plate electrode, (c) disposable foam electrode

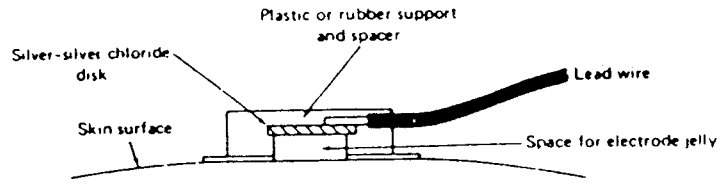


FIG. 9 Diagram of floating type skin surface electrode.

electrolyte paste or Jelly, which forms an electrlyte bridge. Fig.9. shows a cross section of the Floating electrode. Various types of Disposable electrodes have been introduced in recent years, to eliminate the requirement for cleaning and care after each use.

Purpose of Electrode Jelly:

The dry outer skin of the body, is highly non-conductive and will not establish a good electrical contact with an electrode. So the area of contact should be coated with an electrically conductive paste called the electrode Jelly. Thus the electrode jelly decreases the impedance of contact and also reduces the artifacts resulting from the movement of electrode or patient. Generally, the conductivity of the skin is directly proportional to the moisture on the skin. For example, the ECG electrode contact impedance on dry skin is about 100 kohms and the equivalent capacitance is about 0.01 microfarad. After the application of electrode paste, the contact impedance reduced to 10 kohms and the capacitance increased to 0.1 microfarad.

TYPICAL ELECTROCARDIOGRAM COMPLEX

Normal ECGs comprise a regular sequence of P, QRS, and T wave segments, as shown in fig.6. The P, QRS and T waves reflect the rhythmic electrical depolarisation and repolarisation of the heart muscles. The Electrocardiogram is used clinically in diagnosing various diseases and conditions associated with the heart. It also serves as a timing refernce for other measurements. To the clinician, the shape and duration of each feature of the ECG are significant. The waveform however, depends greatly upon the lead configuration used. In general, the Cardiologist looks critically, at the various time intervals, polarities and amplitudes to arrive at his diagnosis. The various functions represented by the segments are:

P wave : Depolarisation of the Atria.

QRS complex : This is generated by the depolarisation of the ventricles. The initial negative deflection resulting from ventricular depolarisation, is shown as the Q wave. The first posotive deflection, during venticular depolarisation is the R wave. The first negative deflection of venticular depolarisation that follows the first posotive deflection is shown as the S wave.

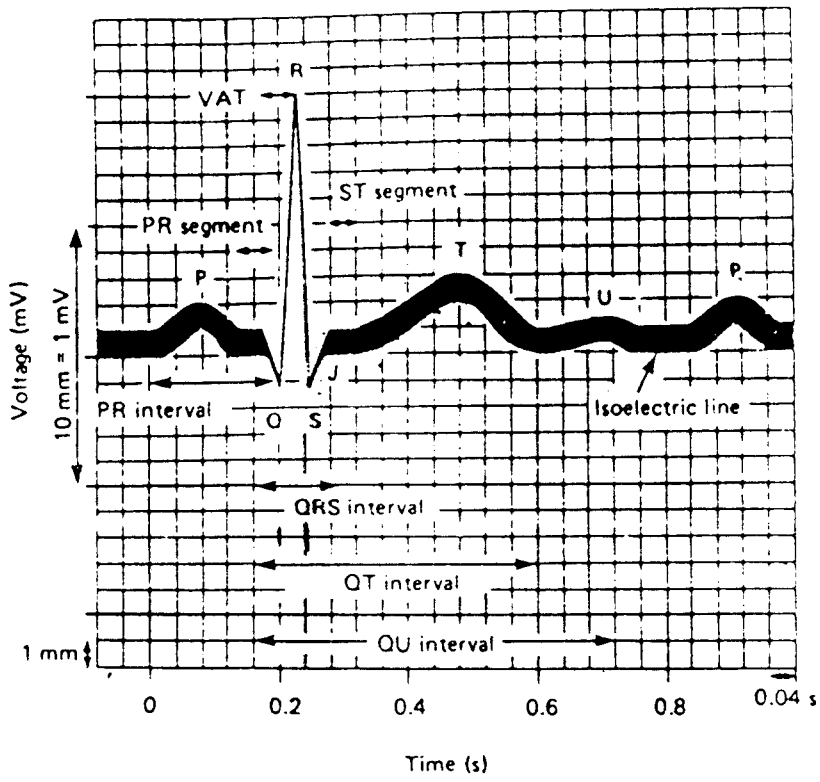


Diagram of electrocardiographic complexes, intervals, and segments

SA node

↓

Atrial myocardium: Depolarization (P); repolarization (T_a)

Internodal pathways

↓

AV node

↓

Bundle of His

↓

Bundle branches

↓

Purkinje system: Late repolarization (U)

↓

Ventricular myocardium: Depolarization (QRS); repolarization (T)

Pathway of conduction and excitation

FIG. 6

T wave : The T wave represents the repolarisation of the ventricles and follows the QRS complex, and the ST segment.

U wave : This represents the slow repolarisation of the Intra-venticular system, and preceeds the next P wave.

The typical amplitudes and time intervals of the various segments are indicated in fig.7.

FIG. 7 **Physiological Nature of ECG Waveform**

	Origin	Amplitude mV	Duration sec.
P Wave	Atrial depolarisation or contraction	0.25	0.12 to 0.22 (P-R interval)
R Wave (QRS complex)	Repolarisation of the atria and the depolarisation of the ventricles	1.60	0.07 to 0.1
T Wave	Ventricular repolarisation (Relaxation of myocardium)	0.1 to 0.5	0.05 to 0.15 (S-T interval)
S-T interval	Ventricular contraction		
U Wave	Slow repolarisation of the intraventricular (Purkinje fibers) system	< 0.1	0.2 (T-U interval)

The ECG Amplifier

THE ECG AMPLIFIER

BIO-Electric measurements are basically low level measurements, involving amplification of signals at microvolt levels. Also the time varying signals, cannot be fed to the microprocessor directly. Hence, for quality data acquisition, powerful high-gain amplifier with high Common Mode Rejection Ratio (CMRR) is to be used, which also serves to reject any incident Electromagnetic Interference (EMI). The bioelectric signal often contains components of extremely low frequency. For faithful reproduction of the signal, the amplifier must have excellent frequency response in the sub-audio frequency range.

In RC coupled amplifier, low frequency response is limited by the reactance of the coupling capacitors. To achieve the low frequency response, the amplifier must have large values of coupling capacitance. But large capacitors cause blocking of the amplifier, in cases of high level inputs, arising due to switching transients. Because of the long Time constant introduced by these capacitors, several seconds may elapse before the capacitors are discharged back to their normal levels. The amplifier therefore becomes momentarily unreceptive following each occourences of overdriving signals. Although, the Direct Coupled

(DC) amplifiers give an excellent frequency response at low frequencies, they tend to drift.

A Typical ECG Amplifier:

The most important consideration in ECG design is to provide amplification to the ECG signal without distorting it, and at the same time, to minimise all unwanted Artifacts. Consider the table given below:

GAIN	1000.
BANDWIDTH	0.05 TO 100 Hz.
INPUT IMPEDANCE	
DIFFERENTIAL	> 2.5 Mohms.
COMMON-MODE	> 100 Mohms.
CMRR	> 20,000.
INPUT RISK CURRENT	< 10 microamps.
OVER VOLTAGE PROTECTION	5,000 V (Defibrillator discharge).

It follows from the table that the ECG amplifier should have the following important features:

(1) Very high Input impedance.

(2) Rejection of Common-mode signals.

(3) Specified high Gain.

(4) Good low Frequency response.

The amplifying component is usually, an Operational Amplifier which uses resistors and capacitors to form a complete amplifier circuit. OPAMPs are used because of their following advantages:

(1) Infinite open-loop gain.

(2) Very high Input impedance and negligible Output impedance.

(3) Stability throught the range of operation.

(4) Infinite CMRR.

(5) Negligible d.c. offset.

(6) Negligible noise, drift and other temperature related effects.

Modern OPAMPs exhibit close to ideal performance and therefore make the task of designing an ECG amplifier somewhat easy. The IC design permits us to build to build amplifiers using very few

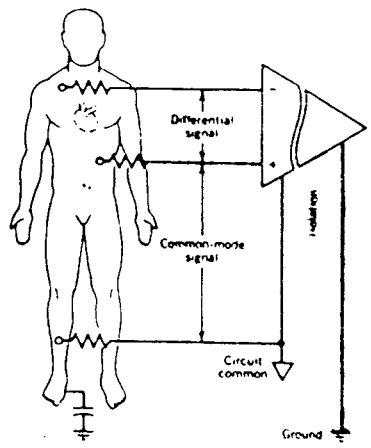
components and to attain a respectable performance, with some degree of assurance.

The signal from the heart is picked up by the two electrodes attached to the body, as shown in fig.10.

The ECG signal is obtained as a difference in potential, between the two electrodes. Consequently, we need a differential amplifier for recording ECG signals. The differential amplifier shown (fig.11.) feeds one input to the inverting side and another to the non-inverting side of the OPAMP. If the set of resistors are perfectly matched(i.e., $R_4/R_3 = R_4'/R_3'$), then the output of the differential amplifier is equal to:

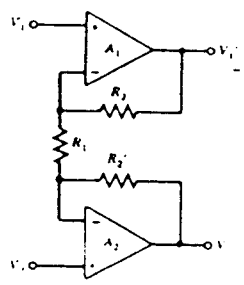
$$[R_4/R_3] * (V_2' - V_1')$$

that is, the difference between the two signals is amplified. One limitation of the circuit shown in fig.11. is that, its Input impedance is quite low. An altenative symmetric, double ended configuration shown in fig.12. presents the inputs directly to the non-inverting inputs of each OPAMP. Consequently, the input impedance remains extremely high. The output of this configuration is also differential. It can be fed to a second stage amplifier, similiar to the one shown in fig.11., to produce a single ended output. A three OPAMP configuration, comprising of the first stage in fig.12. and second stage in fig.11. is called an



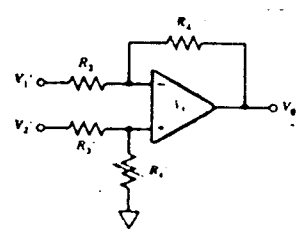
(a)

FIG. 10



(a)

FIG. 11



(b)

FIG. 12

Schematic showing differential and common mode voltages. (b) Op amp differential amplifier. (c) Double-ended front end of instrumentation amplifier.

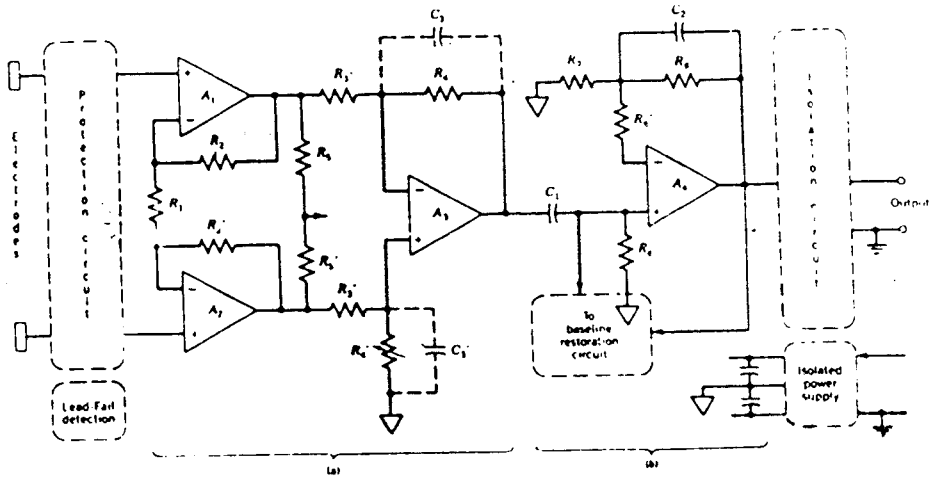


FIG. 13 Circuit of a complete ECG amplifier comprising (a) instrumentation amplifier and (b) second stage for additional gain and filtering

Instrumentation Amplifier.An Instrumentation amplifier along with the second stage for additional gain and filtering is shown in fig.13.

The INA102 Instrumentation Amplifier :

The INA102 is a high-accuracy monolithic instrumentation amplifer designed for signal conditioning applications where low quiescent power is desired. On chip thin film resistors provide excellent temperature and stability performance. State-of-the-art laser-trimming technology insures high-gain accuracy and common mode rejection while avoiding expensive components. These features make the INA102 ideally suited for battery operated and high volume applications. The INA102 is also convenient to use. A gain of 1,10,100 or 1000 may be selected by simply strapping the appropriate pins together. 5ppm/degC gain drift in low gains can be achieved without external adjustment.

A simplified schematic of INA102 is shown in fig.14. A three amplifier configuration is used. The input buffers A1 and A2 incorporate high performance, low drift amplifier circuitary. The amplifiers are connected in a non-inverting configuration to provide a high input impedance (10^{10} ohms). The output stage A3 is connected in a unity gain differential amplifier configuration. A critical part of this stage is the matching of the four 20 kohm resistors which provide the difference function. All the internal resistors are made of thin film

nichrome in the IC. The critical resistors are laser-trimmed to provide the desired accuracy and commom-mode rejection. Nichrome ensures long term stability. This provides Gain, Accuracy and CMRR when INA102 is operated over wide temperature ranges. Fig.15. shows the INA102 in a typical application for amplifying the ECG signal. Additional filtering to reduce noise outside the signal bandwidth can be accomplished by adding an external capacitor between pins 11 and 13. A small resistance can be added in series with pin no.10. to improve the CMRR above the specified value.

PRACTICAL CONSIDERATIONS FOR ECG RECORDING

Several practical aspects must be observed in order to obtain a useful Electrocardiogram.

Artifacts:

Since the ECG unit is a sensitive device, it can pick-up unwanted electrical signals which may modify the actual ECG. Therefore, the operator should check the following things before recording the ECG.

(1) Be sure that the patient does not touch any metal object.

(2) Remove any other electrical appliances in the vicinity of the patient.

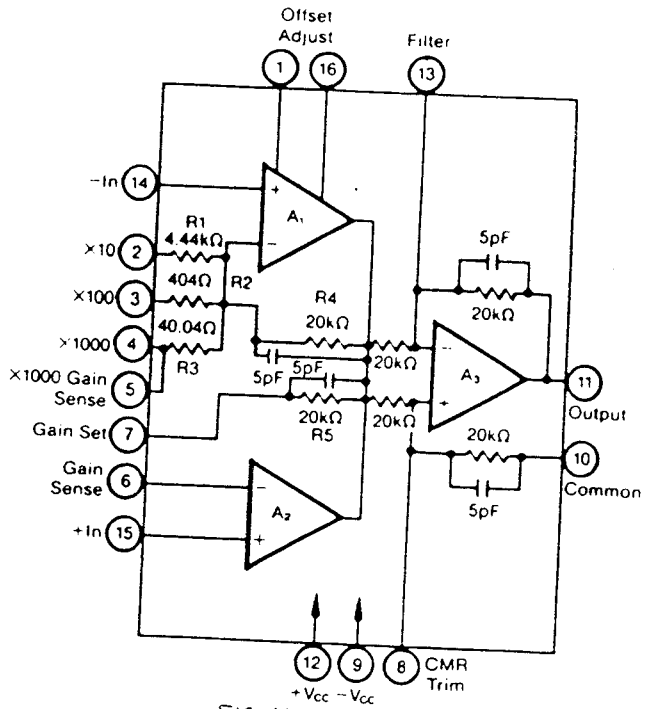


FIG. 14 INTERNAL CONFIGURATION OF INA102

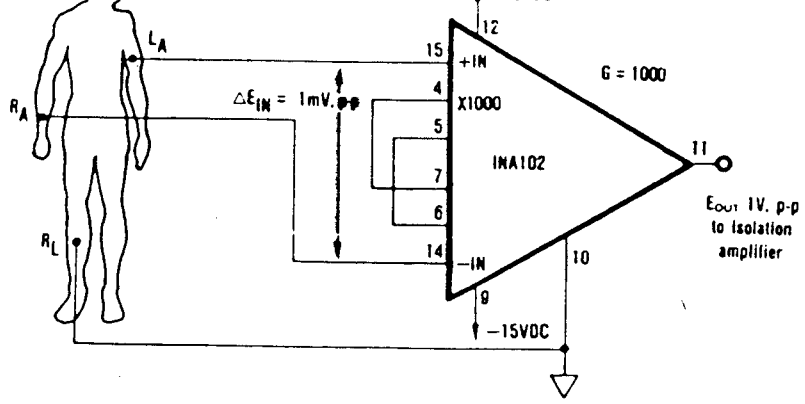


FIG. 15 ECG Amplifier or Recorder Preamp for Biological Signals.

(3) Make sure that all electrodes have been applied, with the right amount of jelly, and all electrode straps are tied.

(4) Be sure that the patient is in a comfortable and relaxed position. Otherwise, unsteady trace may be produced.

Base-line shift:

A wandering base-line is usually due to the gross movements of patients or from mechanical strain on the electrode wires. This can be eliminated, by insuring that the patient lies relaxed and the electrodes are properly placed.

The most critical component of the ECG recorder is the patient cable. Cables made of Silicon-rubber are used to provide better elasticity over longer periods of time.

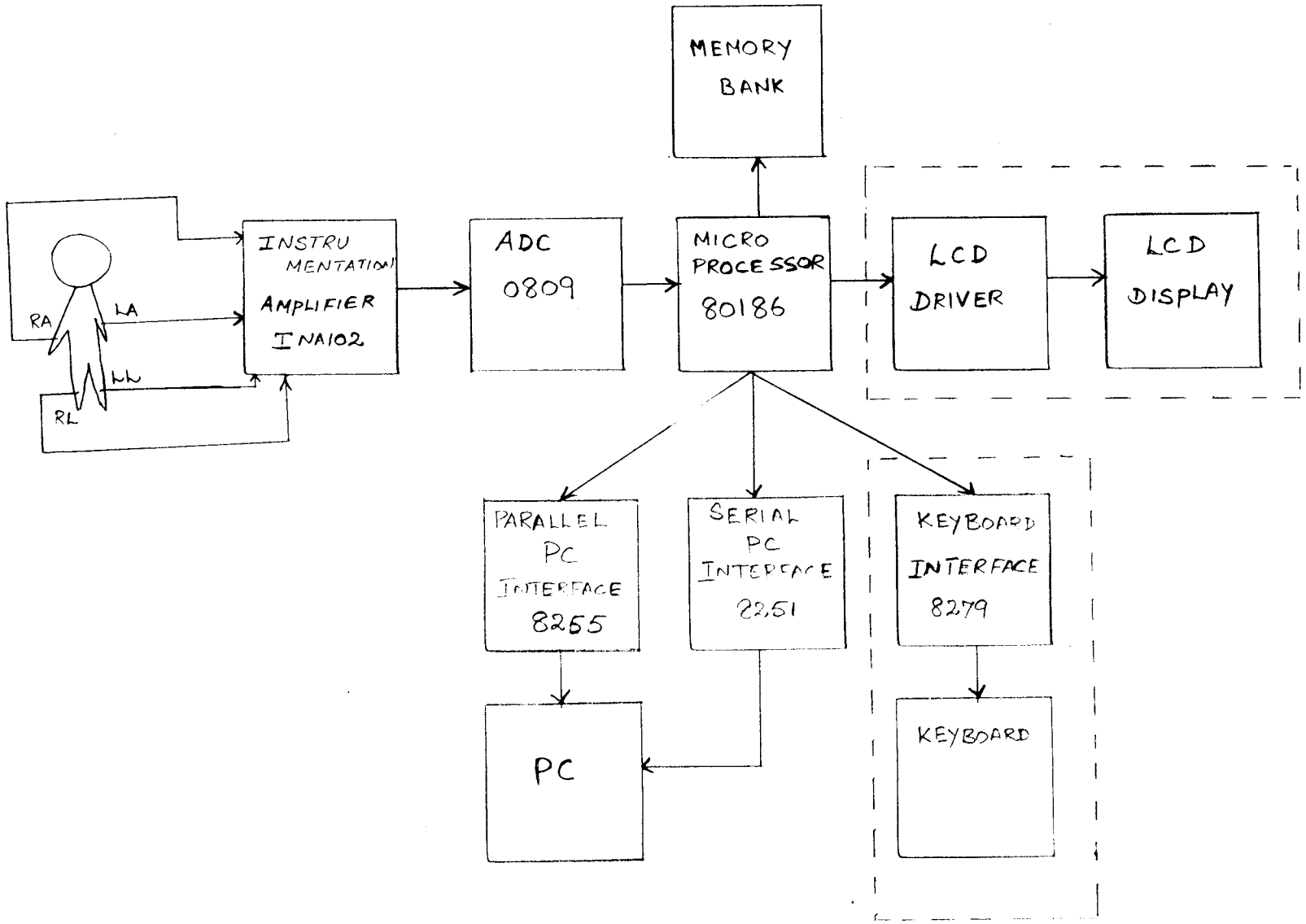
Data Processing System

DATA PROCESSING SYSTEM

The automatic analysis of electrocardigrams by computers requires that the ECG signal obtained from the standard leads is transmitted to the computer by some suitable means. The basic system block diagram used in our sytem is shown in fig.A. It consists of Data Acquistion, Processing and Display parts.

The Data Acquistion part as already described uses a high precision Instrumentation Amplifier - INA102 whose output is suffiently large enough for further Processing.This is now converted into digital form by sampling the analog wave at a few hundred samples per second. This digitised signal is stored and processed in a dedicated 80186 microprocessor system. The stored data is transported to a Personal Computer where Display and Analysis are done. An optional part (A Portable model) includes a Keyboard Interfacing and an LCD Display. The Microprocessor board designed, incorporates all required emulating facilities for the 80186 processor.

The Output of the INA102 is fed to ADC 0809, which contains an 8-channel multiplexer, controlled by the 80186 control processor, through a 3-bit address decoder. The ADC uses Successive Approximation technique with a conversion time of 100 microsec. The



SYSTEM BLOCK DIAGRAM

Sampling rate is fixed by the input given to the START pin, from the control processor. The sampling rate is chosen at about 800 samples/sec, which satisfies the Nyquist criterion, for a baseband ECG signal limited to 150 Hz.The Start-conversion pulse is sent through one of the lines of Port B of a peripheral 8255A. Valid data, after conversion is indicated by an EOC pulse, which is made to interrupt the processor.The output of ADC0809, which is a latched tri-state output is taken to the processor through a SN74245 Transceiver. The transciever is enabled by choosing Port 1 by the 80186. The DIR pin of the transceiver is also held to the same state thus making it uni-directional. The high current tri-state are connected directly to the system bus. Thus the data from the ADC is taken to the Microprocessor.

An LM308 based reference voltage is given to the ADC for stable operation. External signal inputs to the ADC0809 is provided through an LM358 OPAMP, suitably divided using IC 74173. The 74173 consits of 4-bit D type registers having tri-state outputs, which are used for dividing the input given from CLKOUT of the Processor. The 74173 also serves as clock source for the 8279 Keyboard/Display Controller.

The data and address lines of 80186 are multiplexed . So two IC SN74LS373s each containing eight transparent D type latches are used to seperate the data (not latched) and address (latched) lines .

The Memory bank has 64Kx16 bits both of Program (ROM) and Data (RAM) memory. The Program Memory consists of two TMS27256 (64Kx8) Ultraviolet Erasable Programable Read Only Memory.The two segements are arranged such that the lower order 8-bit bus goes to one chip and the remaining higher order bits to the next. The Data memory consists of two 62256 (64Kx8 bits) RAM chips organised in the same way as the ROM area. The ROM and RAM selections are done using the UCS and LCS (both Active low). The memory mapping of 80186 is shown in fig.B. At power-on Reset, the 80186 starts reading at FFFF0(H) automatically from where it is directed to other locations. The Digitised ECG waveform is stored in the RAM from where it is used for further processing and is also communicated to the PC. The lower data bus is also brought to two Berg sticks latched through two SN74HCT373 latches for on board trouble shooting and further enhancement of LCD drivers.

A parallel Centronics port for transfering byte length data to the PC is realised using an 8255A Programable Peripheral Interface. Port A of the 8255A is used as bi-directional data buffer for the Centronics port, with port C giving the necessary handshake signals. One of lines of port B is used to send the start of conversion pulse for the ADC 0809. A Serial EEPROM, 1Kbits long (64x16) IC 93C46 is used for non volatile storage of user parameters during power off conditions. This serial

fig.B.

Memory Selection

	A_0	BHE
LCS	RAM 1	RAM 2
UCS	RAM 1	ROM 2

Port Selection

Port line	Peripheral
PCS1	0809
PCS2	BERG STICKS
PCS3	8279
PCS4	8255A
PCS5	8251

EEPROM is accessed by three bits of port B . The 8255A is programmable, and can be operated as required by properly writing it's control word . The 8255A is connected to the system bus through a SN74HCT245, which is appropriately selected along with the 8255A, when the 80186 addresses Port0.

The Asynchronous Serial communication is achieved by 8251 Programmable Communication Interface .The clock for the 8251 is given from TIMER OUT pin of 80186, whose output is software programmable. The pin TxE of 8251 is sent as interrupt to the processor, during transmitting of data out. During input of data, the RxRDY pin serves to inform the MPU. The data bus of 8251 is latched by SN74HCT245 which serves as a bi-directional buffer. The buffer and the Interface is selected by PCS5 (active low) of the processor. The TxD and RxD of 8251 is connected to RS232 through MAX232. This MAX232 is a dual driver / receiver that includes a capacitive voltage generator to supply the RS232 voltage levels from a single 5 volt supply.

The 8279 Programmable Keyboard Controller is designed initially to drive a segmented LED display for onboard trouble shooting. The two 4-bit output ports is used to drive the LED segments of the

display through the low active SN74HCT244 . The scanned lines are decoded by SN74HCT238 , which drives the digits in the display through ULN2803. A decoded Keyboard output can also be include to provide for emulation facility. The overall schematic of the system designed is shown in fig.C.

Microprocessor - 80186

FEATURES OF 80186 PROCESSOR

The INTEL 80186 is a processor with Integrated Peripherals. The architecture and Instruction Set of 80186 are identical to those of 8088/8086. Infact, the Object code is completely compatible with all existing 8086/8088 software. In addition, it includes ten new instruction types.

The 80186 is a high performance processor, with 4MB/sec Bus bandwidth interface, at the rate of 8 MHz. This gives two times greater Throughput than the standard 5 MHz 8086. In addition the 80186 (80186 -10 version) can also be operated at 10 MHz.Unlike the 8086, 80186 has a built-in clock generator, which requires only a crystal to be added externally. The Integrated peripherals in the processor include a Programmable Interrupt Controller, a Programmable Timer, a Programmable DMA Controller, a programmable Wait state generator,Programmable Memory and Chip-select logic. It has a direct addressing capability of 1 MB of memory and 64 KB of I/O. It is available as 68 pin chip as Plastic Leaded Chip Carrier (PLCC), Ceramic Pin Grid Array (PGA), and Ceramic Leadless Chip Carrier (LCC).

80186 Internal Architecture:

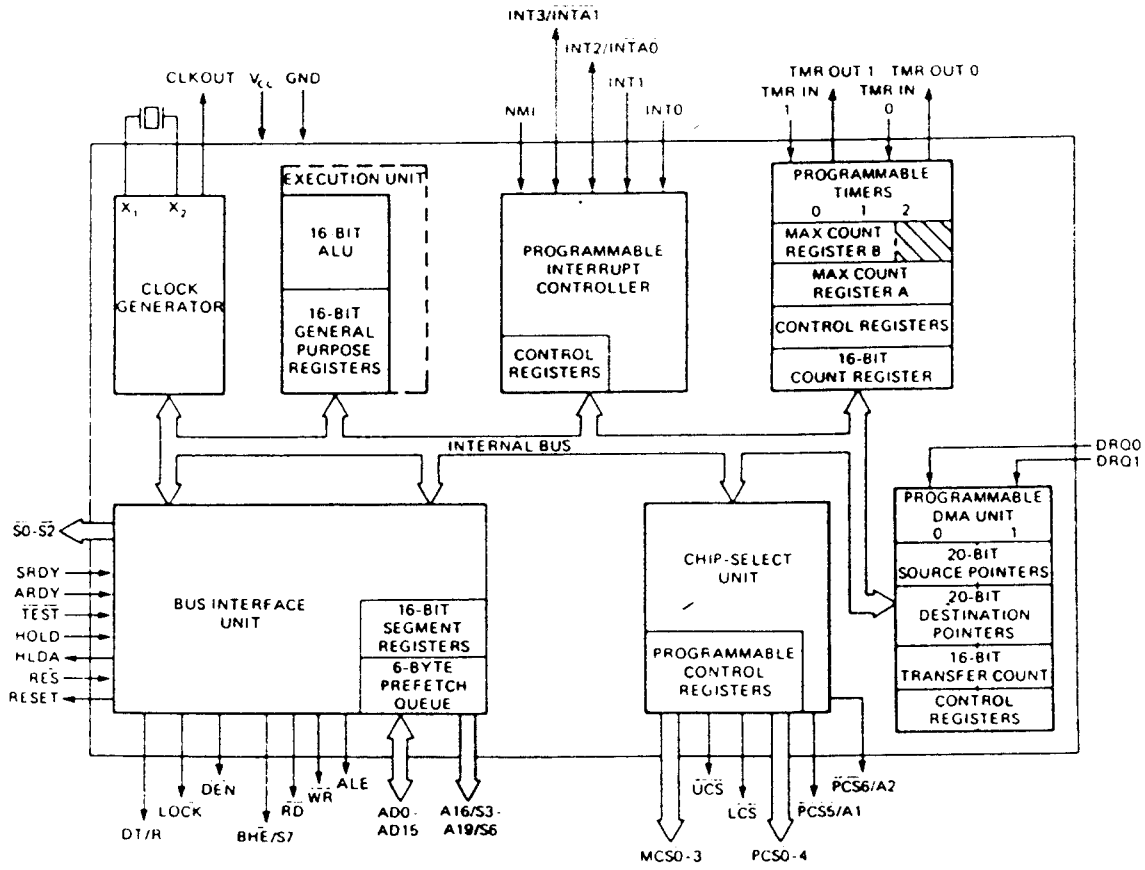
Internally, the 80186 consists of a Bus Interface Unit (BIU), an Execution Unit (EU), and four Peripheral Chip function blocks. Division among the independent functional parts speeds up processing . The various components are shown in fig.16. The 80186 has fourteen registers as shown in fig.17. including eight 16-bit general purpose registers. Some of the datatypes supported by 80186 are :

* Integers : A signed binary numeric value contained in a 8-bit byte or 16-bit word. All operations assume a two's complement representation. Signed 32 and 64-bit Integers are supported using a 8087 Numeric Data Coprocessor.

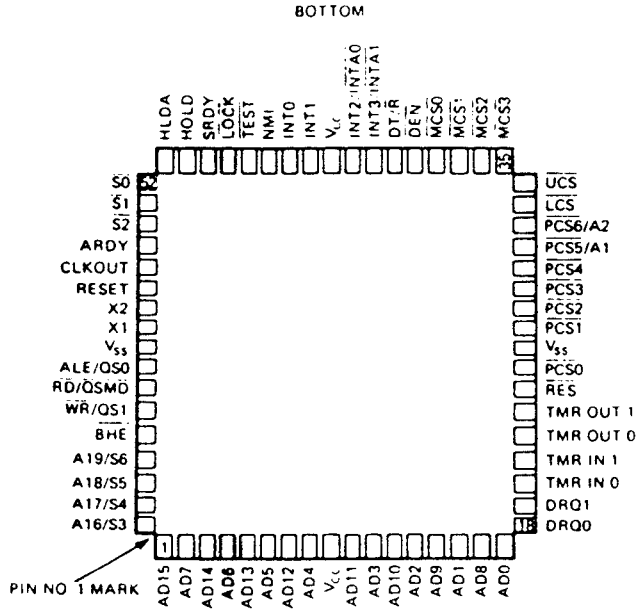
* Ordinal : An unsigned binary numeric value contained in an 8-bit Byte or a 16-bit Word.

* Pointer : A 16 or 32 bit Quantity, composed of a 16 bit offset component or a 16-bit Segment base component in addition to 16-bit offset component.

* String : A contigous Sequence of bytes or words. A string may contain from 1 to 64 KB.



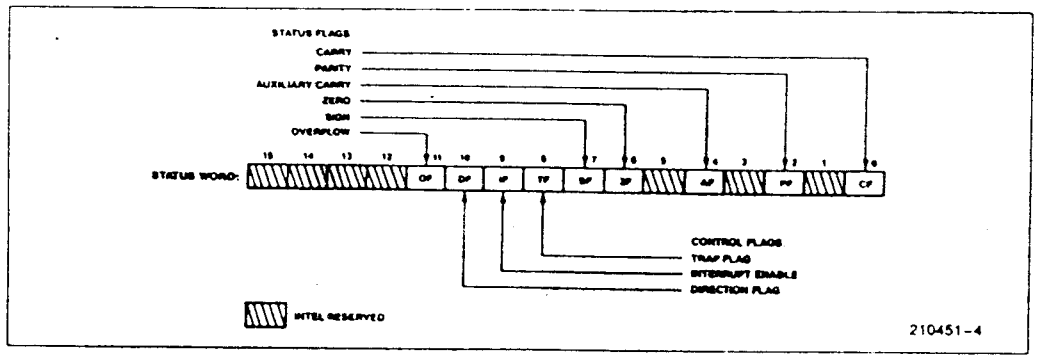
(a)



(b)

FIG. 16

80186. *(a)* Internal block diagram. *(b)* Pin diagram. *(Intel Corporation)*



Status Word Format

FIG. 17

Table 2. Status Word Bit Functions

Bit Position	Name	Function
0	CF	Carry Flag—Set on high-order bit carry or borrow; cleared otherwise
2	PF	Parity Flag—Set if low-order 8 bits of result contain an even number of 1-bits; cleared otherwise
4	AF	Set on carry from or borrow to the low order four bits of AL; cleared otherwise
6	ZF	Zero Flag—Set if result is zero; cleared otherwise
7	SF	Sign Flag—Set equal to high-order bit of result (0 if positive, 1 if negative)
8	TF	Single Step Flag—Once set, a single step interrupt occurs after the next instruction executes. TF is cleared by the single step interrupt.
9	IF	Interrupt-enable Flag—When set, maskable interrupts will cause the CPU to transfer control to an interrupt vector specified location.
10	DF	Direction Flag—Causes string instructions to auto decrement the appropriate index register when set. Clearing DF causes auto increment.
11	OF	Overflow Flag—Set if the signed result cannot be expressed within the number of bits in the destination operand; cleared otherwise

FIG. 19

* ASCII : A byte representation of alphanumeric and control characters using the ASCII standard.

* BCD : A Byte (Unpacked) Representation of decimal digits 0-9.

* Packed BCD : A Byte (Packed) representation of two decimal digits (0-9). One digit is stored in each nibble.

* Floating Point : A signed 32,64 or 80 bit real number representation using 8087 Coprocessor

THE BUS INTERFACE UNIT

The BIU sends out address , fetches instructions from memory, reads data from ports and memory and writes data to ports and memory. In other words the BIU handles all transfers of data and address on the buses for the processor. To speed up program execution, the BIU incorporates pipelining using a Queue. As many as six instruction bytes are fetched ahead of time from the memory. These are held in a group of FIFO registers. The BIU can be fetching instruction bytes while the EU is decoding an instruction or executing an instruction which does not require use of the buses. When the EU is ready for its next instruction, it

simply reads the instruction from the Queue inthe BIU.This is much faster than sending out an address to the system memory and waiting for it to send back the next instruction bytes.

The BIU contains four 16 bit Segemnt Registers they are Code Segment Register (CS), Stack Segment Register (SS), Extra Segment Register (ES) and Data Segment Register (DS). These segement Registers are used to hold the upper 16 bits of the starting addresses of four memory Segments that the 80186 is working at a particular time. The BIU Sends out 20 bit address capable of addressing 1 MB of Memory. However at any given time 80186 works only with four 64 KB segments, pointed to by base addresses in the four segment registers as shown in fig.18. An Instruction pointer (IP) register is used to hold an offset which must be added to the base address in CS to produce the 20-bit physical address. The two 16-bit numbers are not added directly in line. The contents of the CS Register are shifted left four bit positions before the contents of the IP are added to it.

Execution Unit:

The Execution unit of 80186 tells the BIU where to fetch the instruction or data from, Decodes instructions, and executes them. The EU contains control circuitry which directs internal operation. A Decoder in the EU translates instruction fetched from memory into a

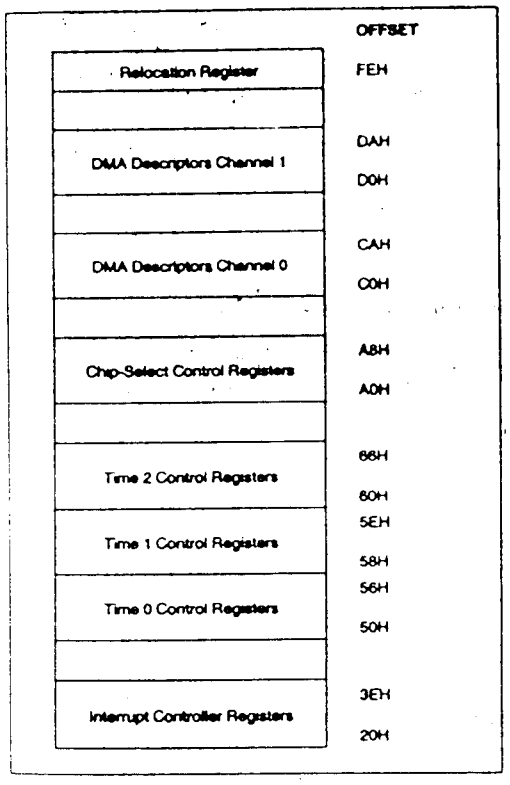


FIG. 22 Internal Register Map

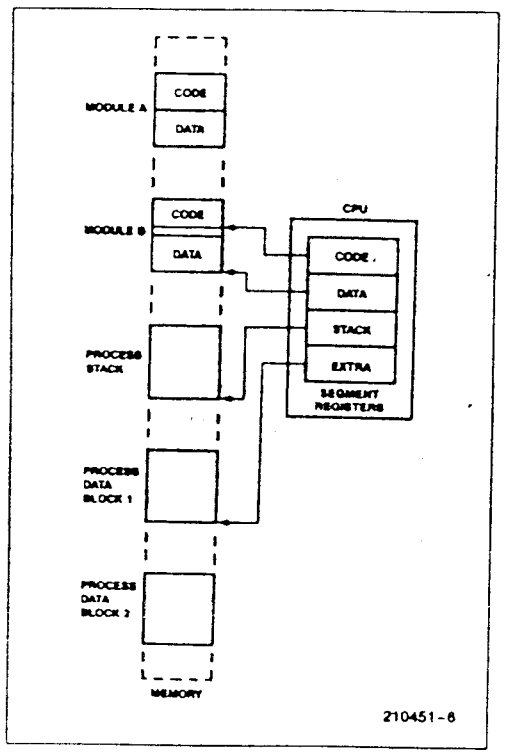


FIG. 18 Segmented Memory Helps Structure Software

series of actions, which the EU carries out. The EU has 16-bit Arithmetic Logic Unit Which performs arithmetic and logic operations. The Flag Register in the EU contains 9 active flags as shown in fig.19, out of which 6 indicates some condition produced by executing an instruction. The three remaining flags are used to control certain operations of the processor. The control flags are deliberately set or reset by specific instruction.

The EU has eight general purpose registers labelled AH,AL,BH,BL,CH,CL,DH,DL. These registers can be used individually for temporary storage of eight bit data. Some of these can be grouped to store 16-bit data. The advantage of using internal registers for the temproary storage of data is that, Since the data is already in the EU, it can be accessed much more quickly than it could be in external memory. The Stack Pointer Register contains the 16-bit offset from the start of the segment to the memory location where a word was most recently stored on the stack. The EU also contains 16-bit Base Pointer register, 16-bit Source Index register and 16-bit Destination Index Register. Their main use is to hold the 16-bit offset of the data word in one of the segments.

PERIPHERAL FUNCTIONAL BLOCKS

Interrupts:

The Priority Interrupt Controller is one of the four peripheral chip function blocks in the 80186. It consists of four interrups- INT0, INT1, INT2, INT3 as well as an NMI Interrupt input.An Interrupt transfers execution to a new program location and the old program address and status word are stored on the Stack. INT2 and INT3 pins can be programmed to function as Interrupt Acknowledge outputs. This mode is used to interface with external 8259s. 80186 can service interrupts generated by software also. All interrupt sources are serviced by an indirect call, through an element of a vector table. This table is indexed using the interrupt vector type, multiplied by 4 as shown in fig.20. The NMI interrupt is serviced regardless of the Interrupt Flag condition. A typical use of the NMI would be to activate a Power failure routine. The activation of this input causes an interrupt with an internally suplied value of 2 as shown in fig.20. The IF bit is cleared at the begining of an NMI to prevent maskable interrupts from being serviced.

Table 4. 80186 Interrupt Vectors

Interrupt Name	Vector Type	Vector Address	Default Priority	Related Instructions	Applicable Notes
Divide Error Exception	0	00H	1	DIV, IDIV	1
Single Step Interrupt	1	04H	1A	All	2
Non-Maskable Interrupt (NMI)	2	08H	1	All	
Breakpoint Interrupt	3	0CH	1	INT	1
INTO Detected Overflow Exception	4	10H	1	INTO	1
Array Bounds Exception	5	14H	1	BOUND	1
Unused Opcode Exception	6	18H	1	Undefined Opcodes	1
ESC Opcode Exception	7	1CH	1	ESC Opcodes (Coprocessor)	1, 3
Timer 0 Interrupt	8	20H	2A		4, 5
Timer 1 Interrupt	18	48H	2B		4, 5
Timer 2 Interrupt	19	4CH	2C		4, 5
Reserved	9	24H	3		
DMA 0 Interrupt	10	28H	4		5
DMA 1 Interrupt	11	2CH	5		
INT0 Interrupt	12	30H	6		
INT1 Interrupt	13	34H	7		
INT2 Interrupt	14	38H	8		
INT3 Interrupt	15	3CH	9		
Reserved	16, 17	40H, 44H			
Reserved	20–31	50H–7CH			

FIG. 20.

Memory chip-select logic:

80186 also has a built-in address decoder refered to as the Chip-select unit. This unit can be programmed to produce an active low chip-select signal when a memory address in the specified range or port address is sent out. Six memory address chip-select signals are available for three address areas; Upper memory, Lower memory and middle range memory. The range for each chip select is user programable. Only one chip select may be programmed to be active for any memory location at a time. The 80186 provides a chip select called UCS for the top of the memory , which is usually used as system memory because after reset the processor begins executing at memory location FFFF0H. The upper limit of memory defined by this chip select is always FFFFFH while the lower limit is programmable. THe lower limit is defined in the UMCS register (fig.21). This register is at offet value A0H in the internal control block (fig.22). The legal values for bits 6-13 and the resulting starting address and the memory block sizes are given in fig.23.

The 80186 provides LCS for low memory the bottom of the memory contains the interrupt vector table starting at location 00000H. The lower limit of the memory defined by this chip select is always 0H while the upper limit is programmable. Fig.24 shows the relation

between the upper address selected and the size of the memory block obtained. The upper limit of this memory block is defined in the LMCS register(fig.21) at offset A2H in the fig.22 . The legal value for bits 6-15 and the resulting upper address and memory block sizes are given in fig.24.

fig.21.a. UMCS register

offset: A0(H)	1	1	U	U	U	U	U	U	U	U	1	1	1	R2	R1	R0

fig.21.b. LMCS register

offset: A2(H)	0	0	U	U	U	U	U	U	U	U	1	1	1	R2	R1	R0

fig.23. UMCS Programming values

Starting Address (Base Address)	Memory Block size	UMCS Value (with R1=R2=R3=0)
FFC00	1K	FFF8(H)
FF800	2K	FFB8(H)
FF000	4K	FF38(H)
FE000	8K	FE38(H)
FC000	16K	FC38(H)
F8000	32K	F838(H)
F0000	64K	F038(H)
E0000	128K	E038(H)
C0000	256K	CO38(H)

fig.24. LMCS Programming values

Upper Address	Memory Block size	LMCS Value (with R1=R2=R3=0)
003FF	1K	0038(H)
007FF	2K	0078(H)
00FFF	4K	00F8(H)
01FFF	8K	01F8(H)
03FFF	16K	03F8(H)
07FFF	32K	07F8(H)
0FFFF	64K	OFF8(H)
1FFFF	128K	1FF8(H)
3FFFF	256K	3FF8(H)

After reset LMCS register value is not defined and will have to be programmed. Similiarly the 80186 provides four MCS lines which are active in the mid-range memory. All of these outputs are Active Low.

Peripheral chip-select logic:

80186 can generate chip-selects for upto seven peripheral devices. Seven chip select lines called PCS0 - PCS6 are generated. The base address is user programmable; however, it can only be a multiple of 1Kbytes. PCS5 and PCS6 can also be programmed to provide latched address bits A1 and A2. The starting address of the peripheral chip select block is defined by the PACS register, as shown in fig.25. This register is located at offset A4H in the Internal Control block (fig.22.). Bits 15-6 of PACS register correspond to bits 19-10 of the 20-bit Programmable Base Address (PBA) of the peripheral chip select block. Bits 9-0 of the PBA of the Peripheral Chip-select block are all zeros. Fig.26. shows the address range of each peripheral chip select, with respect to the PBA contained in the PACS register.

fig.25 PACS register

offset: A4(H)	U	U	U	U	U	U	U	U	U	U	1	1	1	R2	R1	R0

fig.26. PCS Address ranges

PCS LINE (Active Low)	Active between Locations
PCS0	PBA -PBA+127
PCS1	PBA+128-PBA+255
PCS2	PBA+256-PBA+383
PCS3	PBA+384-PBA+511
PCS4	PBA+512-PBA+639
PCS5	PBA+640-PBA+767
PCS6	PBA+768-PBA+895

Timers:

The 80186 provides three internal 16-bit Timers, as shown in fig.27. Two of these are highly flexible, and are connected to four external pins. They can be used to count external events, time external events, generate non-repetitive waveforms. The Timers are controlled by eleven 16-bit registers, located in the Peripheral control block. The configuration of these registers is shown in fig.28.

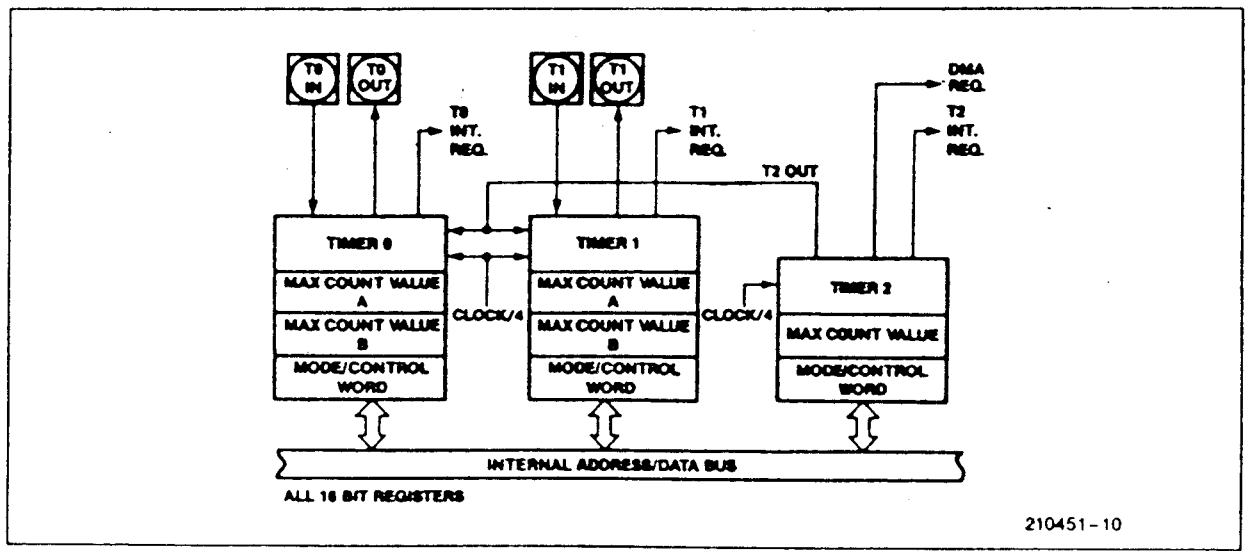


FIG. 27 Timer Block Diagram

fig.28. Timer Control block format

Register name	Register Offset		
	Tmr.0	Tmr.1	Tmr.2
Mode/Control word	56(H)	5E(H)	66(H)
Max Count B	54(H)	5C(H)	--
Max Count A	52(H)	5A(H)	62(H)
Count register	50(H)	58(H)	60(H)

fig.29. Timer Mode/ Control Register

EN	INH	INT	RIU	0	...	MC	RTG	P	EXT	ALT	CONT

The COUNT register contains the current value of the Timer. It can be read or written at any time, independent of wether the Timer is running or not, and the value will be incremented for each Timer event. Each of the Timers is equipped with a MAX-COUNT register, which defines the maximum count the Timer will reach. Timers 0 and 1 are in addition equipped with a second MAX-COUNT register, which enables the Timers to alternate their count between two different Max-count registers. The MODE/CONTROL register, shown in fig.29., allows the

user to program the specific mode of operation or check the current programmed status for any of the three integrated Timers.

Initialisation and Processor Reset:

Processor initialisation is accomplished by driving the RES (Active Low) input pin low. RES forces the 80186 to terminate all execution and local bus activity. After RES becomes inactive, and an internal processing interval elapses, the 80186 begins execution with the instruction at the physical location FFFF0H. RES also sets some registers to predefined values as shown in fig.30.

The 80186 also provides a RESET pin synchronised to RES for use with other system components.

fig.30. 80186 Initial Register state after RESET

Status Word	F002(H)
Instruction Pointer	0000(H)
Code Segment	FFFF(H)
Data Segment	0000(H)
Extra Segment	0000(H)
Stack Segment	0000(H)
Relocation register	20FF(H)
UMCS	FFFB(H)

Local Bus Controller:

The 80186 provides a local bus controller to generate the local bus control signals. It also provides outputs that can be used to enable external buffers and to direct flow of data on and off the local bus. The 80186 provides ALE, RD and WR (both Active Low) bus control signals for memory/peripheral control. The RD and WR signals are used to strobe data from memory or I/O to the 80186 or to strobe data from 80186 to memory or I/O. The ALE line provides a strobe to latch the address when it is valid. The 80186 generates two control signals to be connected to Transceiver chips. This capability allows the addition of transceivers for extra buffering without adding external logic. These control lines, DT/R and DEN(Active Low) are generated to control the flow of data through the transceivers. DEN enables the output drivers of the transceivers, and DT/R determines the direction of travel. A HIGH (DT) level directs data away from the processor during Write operations, while a LOW (R) level directs data towards the processor during a Read operation.

Clock Generator:

The 80186 provides an on-chip clock generator for both internal and external clock generation. The clock generator features a crystal oscillator, a divide-by-two counter, synchronous and asynchronous

ready inputs, and reset circuitary. The Oscillator crystal selected is double the CPU clock frequency. This is fed to the Clock generator which provides the 50% duty cycle processor clock for the 80186. The CLKOUT pin provides the processor clock signal for use outside the 80186. All timings are referenced to the output clock.

On Board Peripheral Interfaces

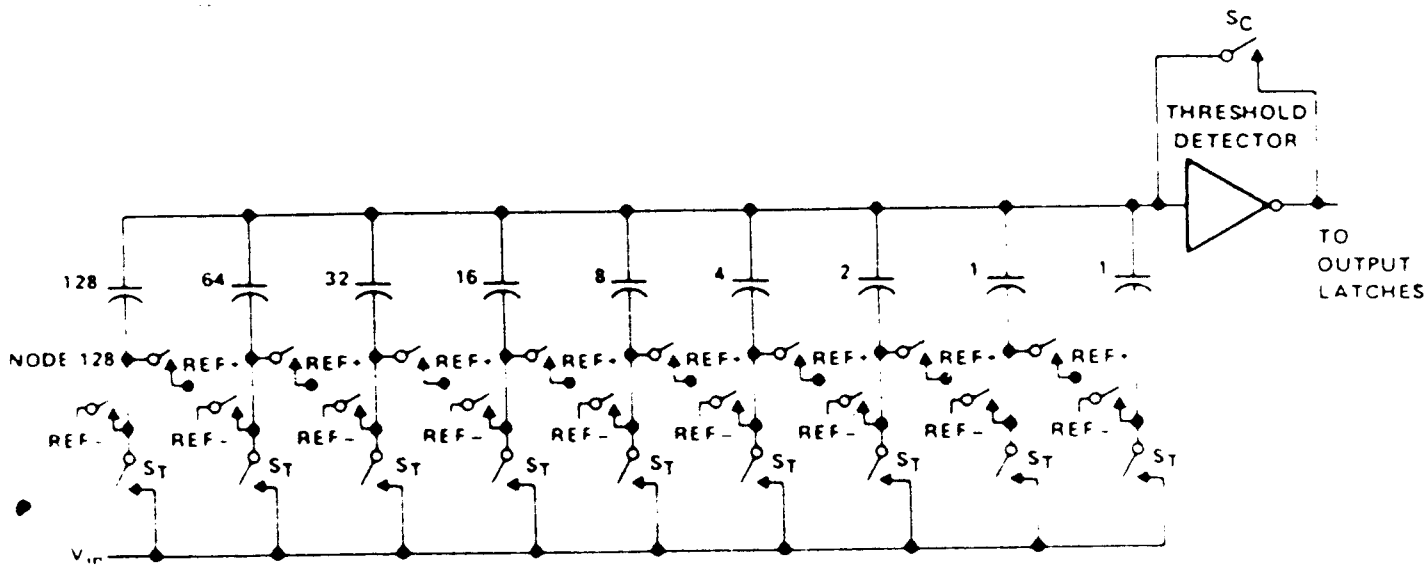
ON BOARD PERIPHERAL INTERFACES

Analog to Digital Converter - 0809 :

The A/D conversion is a quantising process whereby an analog signal is represented by equivalent binary states. ADCs can be classified into two general groups based on conversion technique. One technique involves comparing a given analog signal with an internally generated equivalent signal. This group includes Successive approximation, Counter and Flash type converters. The second technique involves changing an analog signal into time or frequency and comparing these new parameters against known values. This group includes Integrator converters and Voltage to Frequency converters. The trade off between the two is based on accuracy and speed.

The ADC 0809 consists of an analog signal multiplexer, an 8-bit successive approximation convertor and related control and output circuitry. The Analog Multiplexer selects one of 8 single ended input channels as determined by the address decoder . Address load control loads the address code into the decoder on a low to high transition, thus we see that the address inputs are latched. The output latch is reset by the positive going edge of the start pulse .

The CMOS threshold detector in the Successive Approximation Conversion System determines each bit by examining the charge on a series of binary-weighted capacitors as shown in fig.31. In the first phase of the conversion process, the analog input is sampled by closing switch Sc and all St switches, and by simultaneously charging all the capacitors to the input voltage. In the next phase of the conversion process, all St and Sc switches are opened and the threshold detector begins identifing bits by identifing the charge on each capacitors relative to the reference voltage. In the first step of conversion phase, the threshold detector looks at the first capacitor (weight=128) , which is switched to the reference voltage and the equivalent nodes of all other capacitors on the ladder are switched to negative reference. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately 1/2 Vcc), a bit is placed in the output register, and the 128-weight capactior is switched to REF-. If the voltage at the summing node is less than the trip point of the threshold detector this 128 capactior remains connected to REF+ throughout the remainder of the capactior sampling process. The process is repeated until all bits are counted. This successive approximation conversion process relies on charge distribution rather than a SAR register to count and weigh the bits from MSB to LSB.



SIMPLIFIED MODEL OF THE SUCCESSIVE-APPROXIMATION SYSTEM

FIG. 31

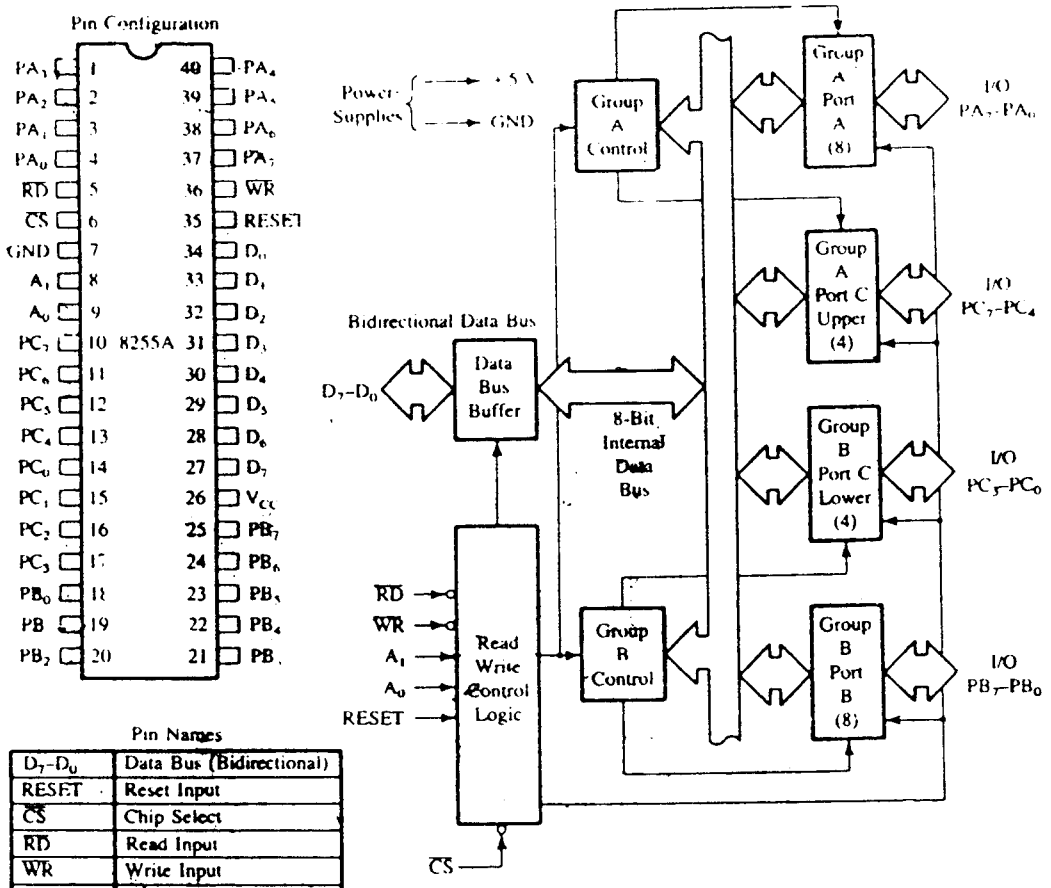
ADC 0809 has the following features :

* 100 micro sec conversion time.
* Easy interface with microprocessor.
* Low power consumption.
* Latched input and output.
* Total unadjusted error of + or - 1.25 LSB Max

Programmable Peripheral Interface-8255A :

The 8255A is widely used Programmable parallel I/O device. It can be programmed to transfer data under various condtions, from simple I/O to interrupt I/O. The 8255A has 24 I/O pins that can be grouped into two 8-bit parallel ports: A and B , with the remaning eight bits of port C can be used as individual bits or be grouped into two 4-bit port. The Block diagram in fig.32. shows ports A and B, two 4-bit ports, C_u and C_l, data bus buffer and Control logic.

All functions of 8255A are classified according to two modes : the Bit Set/Reset (BSR mode) and the I/O mode. The 8255A contains a control register, the contents of this register, shown in fig.33 called the control word specify an I/O function for each port . This register can be written to, but is not accessible to Read operation. The BSR mode is used to set or reset the bits in port C. When the 8255A is programmed to



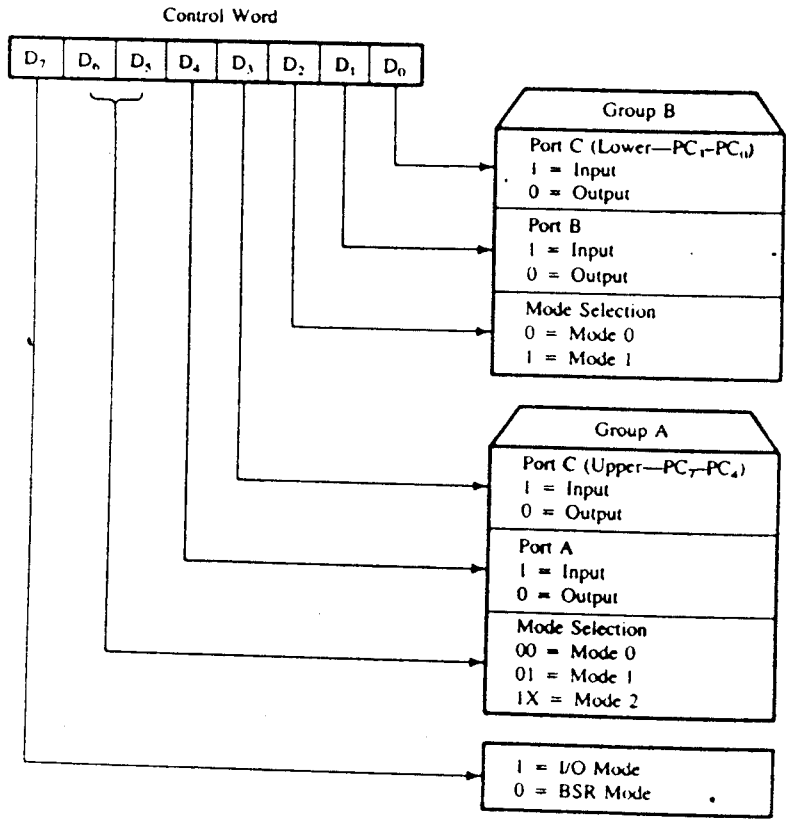
Pin Names

D_7–D_0	Data Bus (Bidirectional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0, A_1	Port Address
PA_7–PA_0	Port A (Bit)
PB_7–PB_0	Port B (Bit)
PC_7–PC_0	Port C (Bit)
V_{CC}	+5 Volts
GND	0 Volts

(a)

8255A Block Diagram (a) and an Expanded Version of the Control Logic and

FIG. 32



8255A Control Word Format for I/O Mode

FIG 33

operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop using the bit set/reset function of port C. This function allows the programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.The I/O mode is further divided into three modes: Mode 0,Mode 1,Mode 2. In Mode 0 all ports function as simple I/O ports.Mode 1 is a handshake mode in which port A and B use bits from port C as handshake signals. In Mode 2 port A can be set up for bidirectional data transfer .

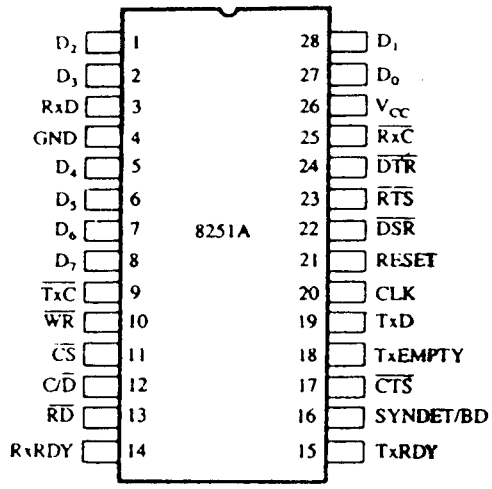
The 8255A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.In this system we use Mode 2 for bidirectional data transfer. through the Centronics port to the PC. Port C gives the necessary handshake signals. One bit of port B is used to send Start Of Conversion pulse to the ADC.Another three bits of port B is used to access the serial EEPROM.

Programmable Communication Interface-8251A :

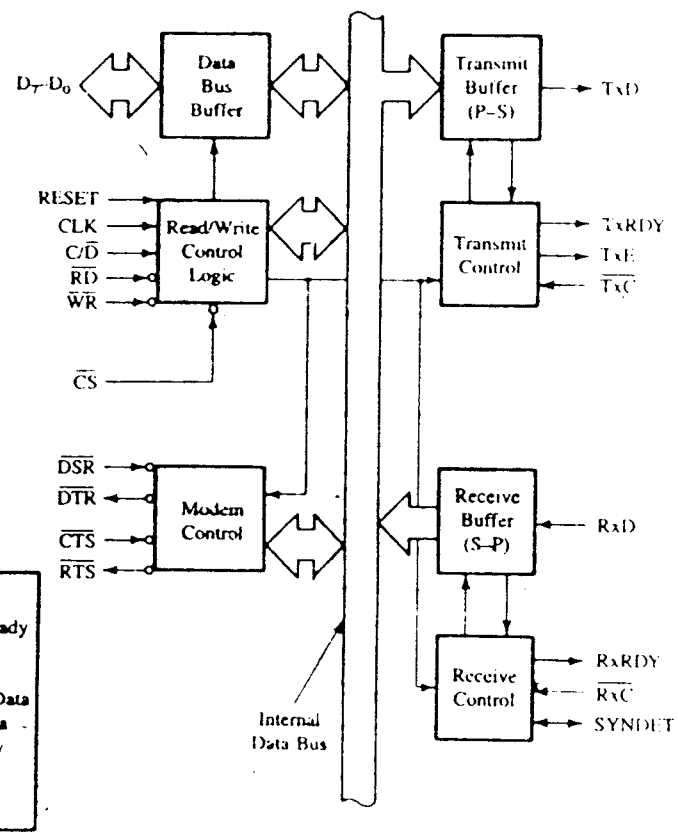
The 8251A is designed for Synchronous and Asynchronous data communication. It includes five sections: Read/Write, Control logic, Transmitter, Receiver, Data bus buffer and Modem control. The Control logic interfaces the chip with MPU, determines the functions of the chip according to the control word in its register, and monitors the data flow. The Transmitter section converts a Parallel word recieved from the MPU into Serial bits and transmits them over the TxD line to the PC. The Reciever section recieves Serial bits and converts them into a Parallel word, and transfers the word to the MPU. The Modem control is used to establish data communication through Modems, over Telephone lines.

The 8251A is a complex device, capable of performing various functions. In this project it is used as a means of achieving Asynchronous Communication between the MPU and the PC. Figure 34 shows an expanded version of the 8251A block diagram. The block diagram shows all the elements of a programmable chip; it includes the interfacing siganals, the Control register, and the Status register. To implement Serial communication, the MPU must inform the 8251A of all details such as Mode, Baud, Stop-bits, parity etc. Therefore prior to data transfer, a set of control words must be loaded into the 16-bit control register of the 8251A. In addition, the MPU must check the

Pin Configuration



Block Diagram



Pin Names

D_7–D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock
TxD	Transmitter Data
RxC	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready
TxRDY	Transmitter Ready

DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET/BD	Sync Detect/ Break Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxE	Transmitter Empty
V_{CC}	+5 Volt Supply
GND	Ground

The 8251A: Block Diagram, Pin Configuration, and Description

FIG. 34

readiness of a peripheral by reading the status register. The control words are divided into two formats: Mode words and Command words. This is shown in figure 35. The Mode word specifies the general characteristics of operations (Such as Baud, parity, Number of Stop bits), the Command word enables data transmission and/or reception and the Status word provides the information concerning register status and transmission errors.

The Shift registers in the USART require clocks to shift the serial data in and out. TxC is the Transmit Shift register clock input, and RxC is the recieved Shift register clock input. Usually, these two inputs are tied together. So they are driven by the same clock. The frequency of the applied clock signal must be 1, 16, or 64 times the transmit/recieve baud rate, depending on the mode in which the 8251A is initialised. Using a clock frequency higher than the baud rate allows the recieve shift register to be clocked at the center of a bit, rather than at a transition. This reduces chance of noise at a transition causing a Read error.

The 8251A is double buffered. This means that one character can be loaded into a holding buffer while another character is being shifted out of the actual transmit shift register. The TxRDY output from the 8251A will go high when the holding buffer is empty, and another character can be sent from the CPU. The TxEMPTY pin will go high,

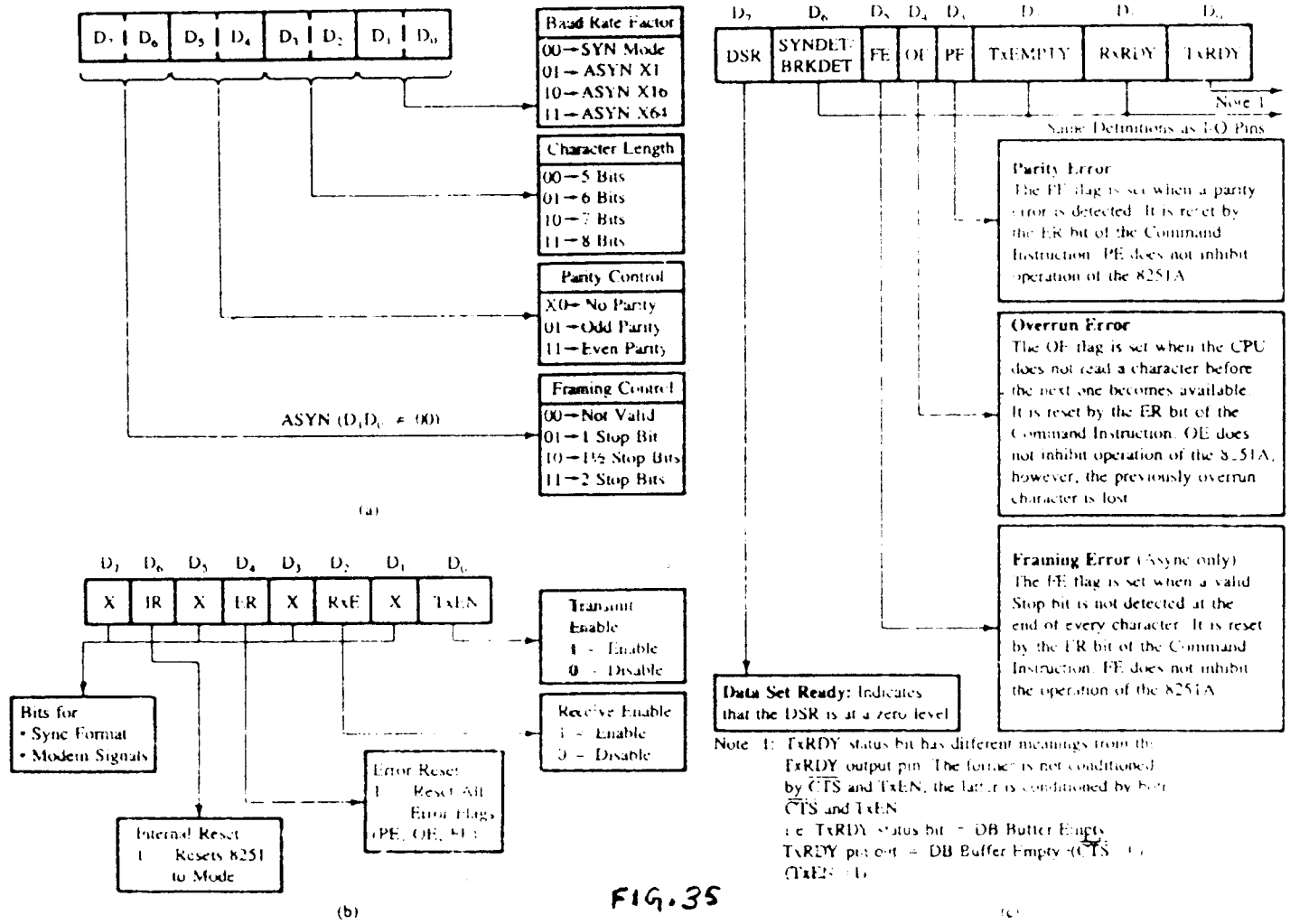


FIG. 35

Mode Word Format (a), Command Word Format (b), and Status Word Format (c)

when both holding buffer and transmit shift register are empty. The RxRDY will go high when a character has been shifted into the Reciever buffer, and is ready to be read out by the CPU. Incidentally, if a character is not read out, before another character is shifted in, the first character will be over-written and lost.

The Programmable Keyboard/Display Interface-8279 :

The Intel 8279 is a general purpose Programmable Keyboard and Display I/O interface device designed for use with Intel microprocessors. The keyboard portion can provide a scanned interface to a 64 - contact key matrix.

The keyboard portion will also interface to an array of sensors or a strobed interface keyboard, such as Hall effect and Ferrite variety. Key depressions can be a 2-key lockout or N-key rollover. Keyboard entries are debounced and strobed in an 8-character FIFO. If more than 8 characters are entered, overrun status is set. Key entries set the interrupt outptut line to the CPU.

The display portion provides a scanned display interface for LED, Incandescent, and other popular display technologies. Both numeric and alphanumeric Segment displays may be used as well as

simple indicators. The 8279 has 16x8 display RAM, which can be organised into dual 16x4. The RAM can be loaded or interrogated by the CPU. Both right entry, calculator and left entry typewriter display formats are possible. Both read and write of display RAM can be done with auto increment of display RAM address.

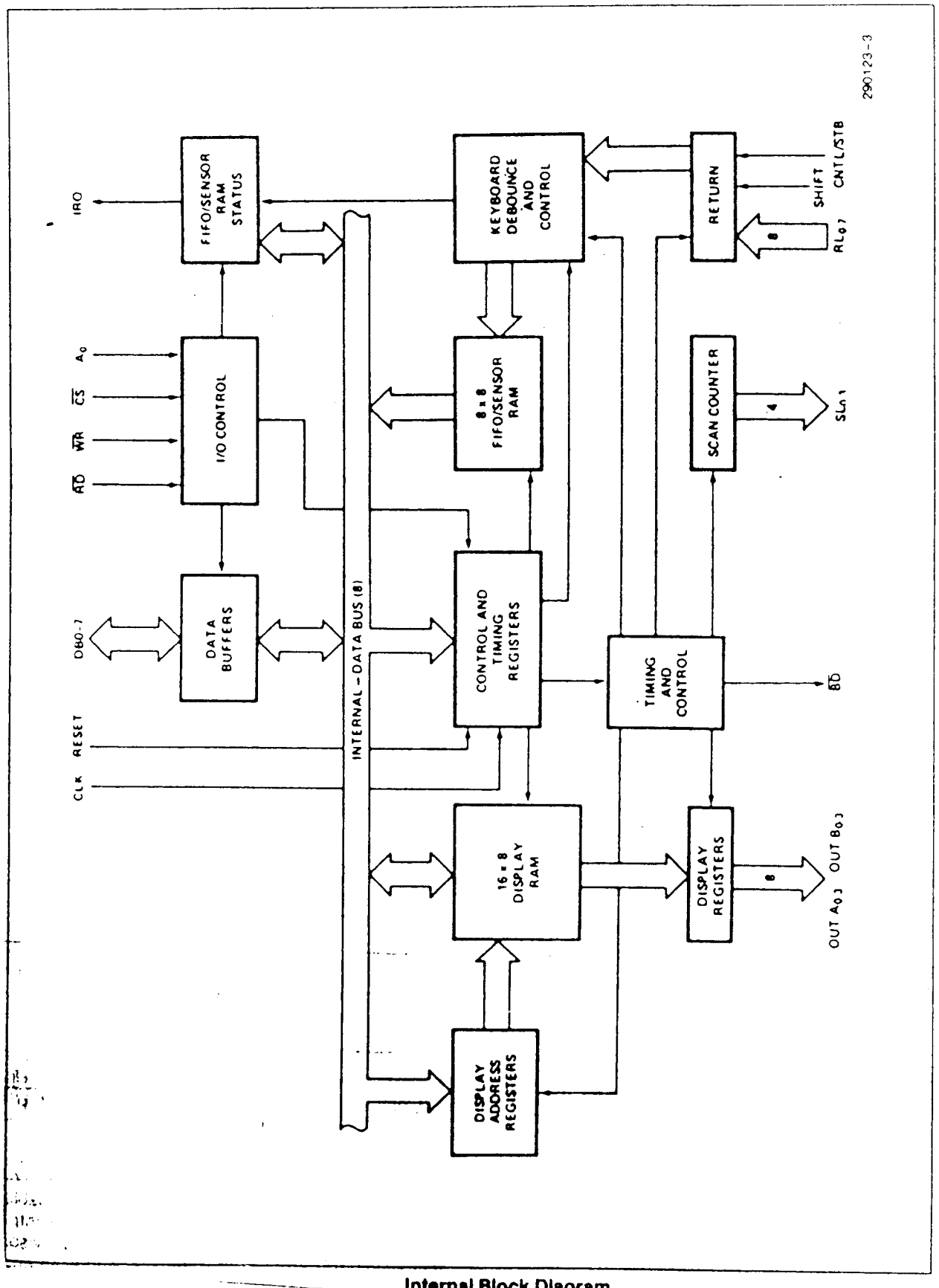
The 8279 provides an interface that can control data input and display for 8-bit microprocessors. It has two sections: Keyboard and Display. The Keyboard section can interface to regular typewriter style keyboards or random toggle or thumb switches. The display section drives alphanumeric displays or a bank of indicated lights. Thus the CPU is relieved from scanning the keyboard or refreshing the display. The 8279 is designed to directly connect to the microprocessor bus. The CPU can program all operating modes for the 8279.

The other features of 8279 include:

* Mode programming from a CPU.
* Clock Prescalar.
* Interrupt output to signal CPU when there is Keyboard or sensor data available.
* An 8-Byte FIFO to store keyboard information.
* 16-Byte internal Display RAM for display refresh. This RAM can also be read by the CPU.

The Internal block diagram of 8279 is shown in fig.36. It includes I/O control, data buffers, Timing and Control registers, Scan counter, return buffers, keyboard debounce and control, a FIFO/Sensor RAM and a Display RAM. The Control and timing registers store the keyboard and display modes and other operating conditions programmed by the CPU. The various formats used are shown in figure 37.

In our system the 8279 is used to interface an LED display array for on-board trouble shooting, which is to be modified to scan the keyboard in the Portable LCD Model.



Internal Block Diagram

8279/8279-5

FIG 36

Write Display RAM

Code: | 1 | 0 | 0 | AI | A | A | A | A |

The CPU sets up the 8279 for a write to the Display RAM by first writing this command. After writing the command with $A_0 = 1$, all subsequent writes with $A_0 = 0$ will be to the Display RAM. The addressing and Auto-Increment functions are identical to those for the Read Display RAM. However, this command does not affect the source of subsequent Data Reads; the CPU will read from whichever RAM (Display or FIFO/Sensor) which was last specified. If, indeed, the Display RAM was last specified, the Write Display RAM will, nevertheless, change the next Read location.

Display Write Inhibit/Blanking

				A	B	A	B
Code:	1	0	1	X	IW	IW	BL	BL

The IW Bits can be used to mask nibble A and nibble B in applications requiring separate 4-bit display ports. By setting the IW flag (IW = 1) for one of the ports, the port becomes marked so that entries to the Display RAM from the CPU do not affect that port. Thus, if each nibble is input to a BCD decoder, the CPU may write a digit to the Display RAM without affecting the other digit being displayed. It is important to note that bit B_0 corresponds to bit D_0 on the CPU bus, and that bit A_3 corresponds to bit D_7.

If the user wishes to blank the display, the BL flags are available for each nibble. The last Clear command issued determines the code to be used as a "blank." This code defaults to all zeros after a reset. Note that both BL flags must be set to blank a display formatted with a single 8-bit port.

Clear

Code: | 1 | 1 | 0 | C_D | C_D | C_D | C_F | C_A |

The C_D bits are available in this command to clear all rows of the Display RAM to a selectable blanking code as follows.

C_D C_D C_D

- 0 X — All Zeros (X = Don't Care)
- 1 0 — AB = Hex 20 (0010 0000)
- 1 1 — All Ones

└── Enable clear display when = 1 (or by C_A = 1)

During the time the Display RAM is being cleared (~160 μs), it may not be written to. The most significant bit of the FIFO status word is set during this time. When the Display RAM becomes available again, it automatically resets.

If the C_F bit is asserted (C_F = 1), the FIFO status is cleared and the interrupt output line is reset. Also, the Sensor RAM pointer is set to row 0.

C_A, the Clear All bit, has the combined effect of C_D and C_F; it uses the C_D clearing code on the Display RAM and also clears FIFO status. Furthermore, it resynchronizes the internal timing chain.

End Interrupt/Error Mode Set

Code: | 1 | 1 | 1 | E | X | X | X | X | X = Don't care

For the sensor matrix modes this command lowers the IRQ line and enables further writing into RAM. (The IRQ line would have been raised upon the detection of a change in a sensor value. This would have also inhibited further writing into the RAM until reset.)

For the N-key rollover mode — if the E bit is programmed to 1, the chip will operate in the special Error mode. (For further details, see Interface Considerations Section.)

Keyboard/Display Mode Set

	MSB							LSB
Code:	0	0	0	D	D	K	K	K

Where DD is the Display Mode and KKK is the Keyboard Mode.

DD

- 0 0 — 8 8-bit character display — Left entry
- 0 1 — 16 8-bit character display — Left entry
- 1 0 — 8 8-bit character display — Right entry
- 1 1 — 16 8-bit character display — Right entry

For description of right and left entry, see Interface Considerations. Note that when decoded scan is set in keyboard mode, the display is reduced to 4 characters independent of display mode set.

KKK

- 0 0 0 — Encoded Scan Keyboard — 2 Key Lockout*
- 0 0 1 — Decoded Scan Keyboard — 2-Key Lockout
- 0 1 0 — Encoded Scan Keyboard — N-Key Rollover
- 0 1 1 — Decoded Scan Keyboard — N-Key Rollover
- 1 0 0 — Encoded Scan Sensor Matrix
- 1 0 1 — Decoded Scan Sensor Matrix
- 1 1 0 — Strobed Input, Encoded Display Scan
- 1 1 1 — Strobed Input, Decoded Display Scan

Program Clock

Code: | 0 | 0 | 1 | P | P | P | P | P |

All timing and multiplexing signals for the 8279 are generated by an internal prescaler. This prescaler divides the external clock (pin 3) by a programmable integer. Bits PPPPP determine the value of this integer which ranges from 2 to 31. Choosing a divisor that yields 100 kHz will give the specified scan and debounce times. For instance, if Pin 3 of the 8279 is being clocked by a 2 MHz signal, PPPPP should be set to 10100 to divide the clock by 20 to yield the proper 100 kHz operating frequency.

Read FIFO/Sensor RAM

Code: | 0 | 1 | 0 | AI | X | A | A | A | X = Don't Care

The CPU sets up the 8279 for a read of the FIFO/Sensor RAM by first writing this command. In the Scan Keyboard Mode, the Auto-Increment flag (AI) and the RAM address bits (AAA) are irrelevant. The 8279 will automatically drive the data bus for each subsequent read (A_0 = 0) in the same sequence in which the data first entered the FIFO. All subsequent reads will be from the FIFO until another command is issued.

In the Sensor Matrix Mode, the RAM address bits AAA select one of the 8 rows of the Sensor RAM. If the AI flag is set (AI = 1), each successive read will be from the subsequent row of the sensor RAM.

Read Display RAM

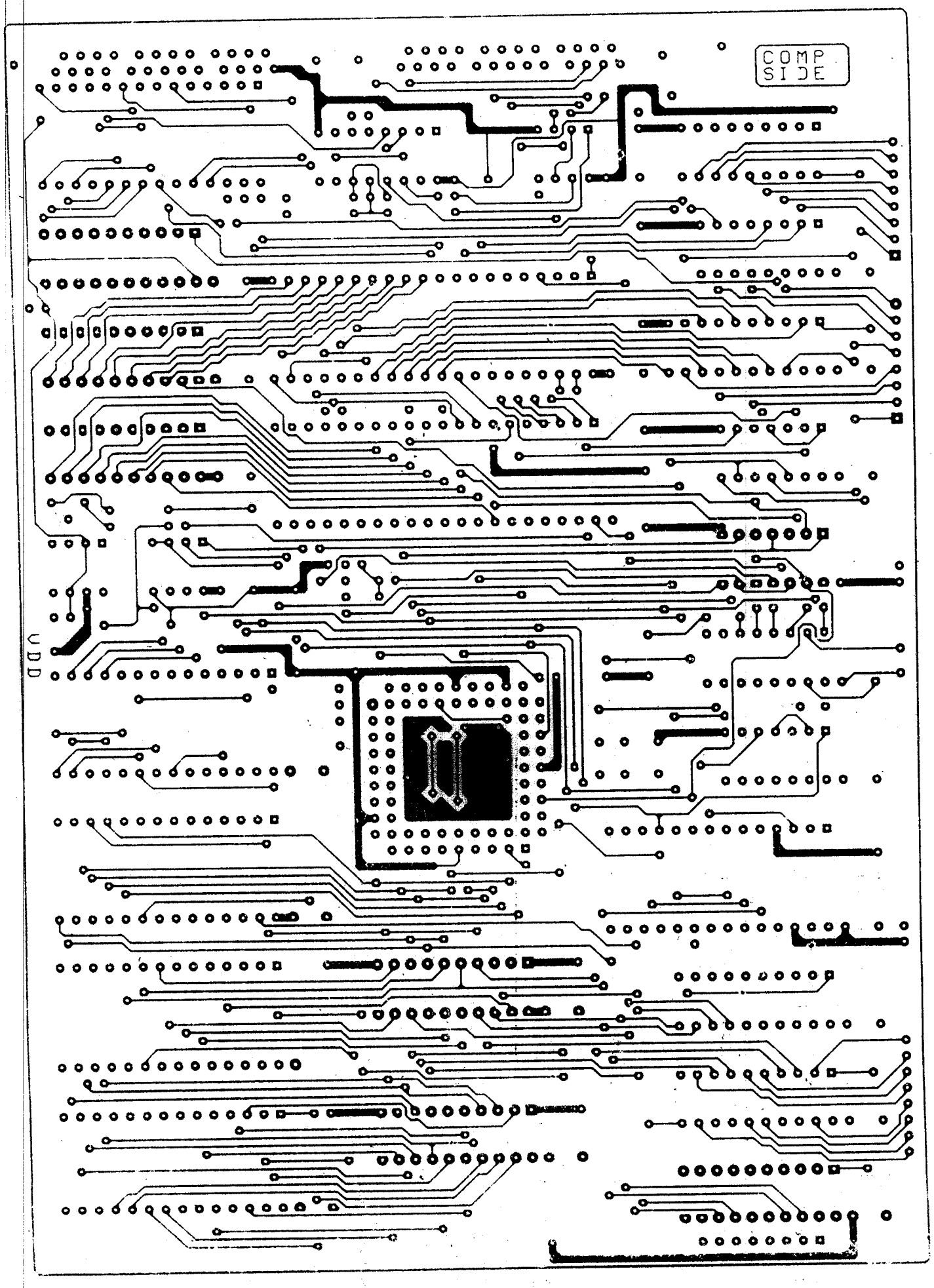
Code: | 0 | 1 | 1 | AI | A | A | A | A |

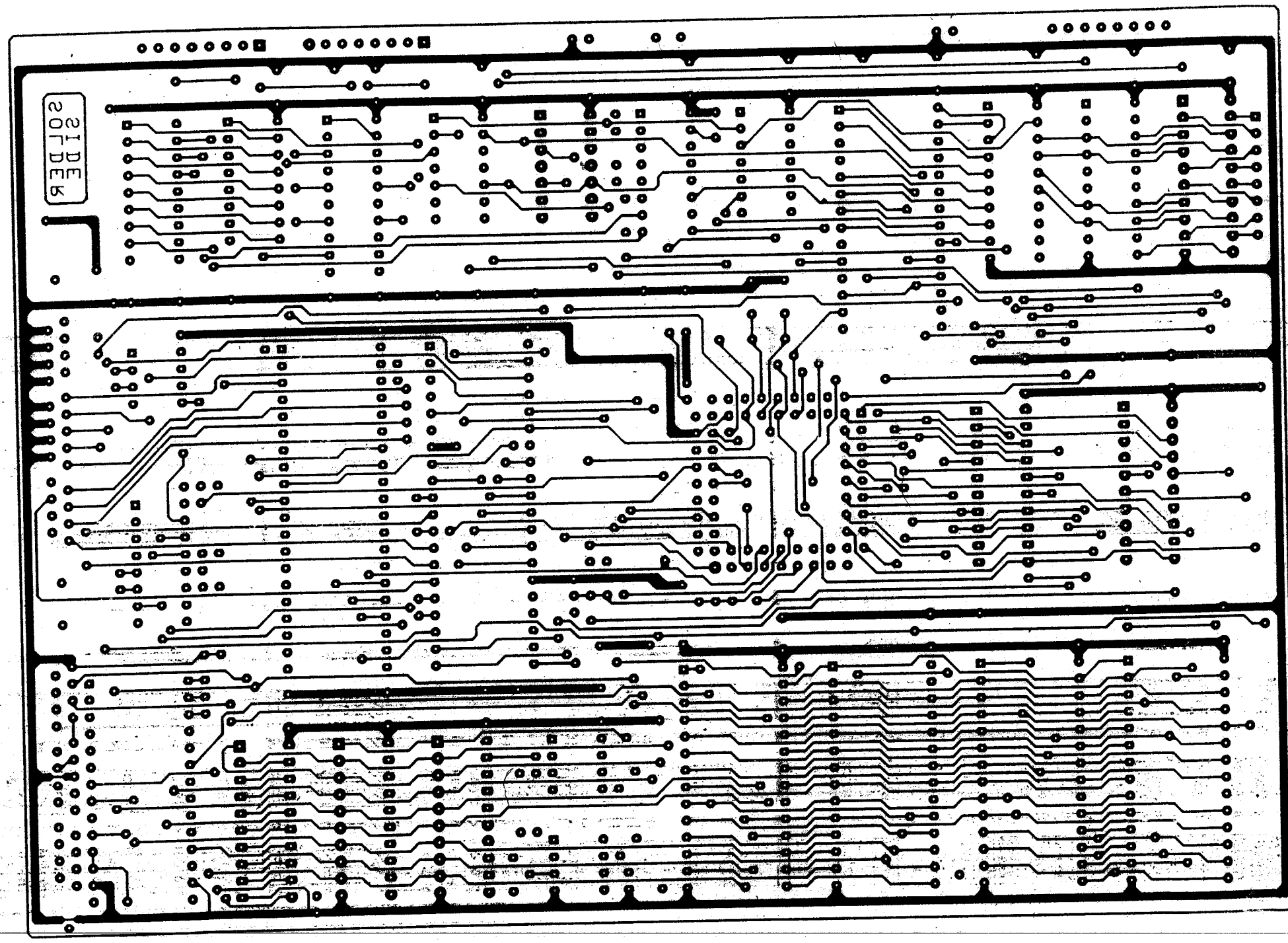
The CPU sets up the 8279 for a read of the Display RAM by first writing this command. The address bits AAAA select one of the 16 rows of the Display RAM. If the AI flag is set (AI = 1), this row address will be incremented after each following read *or write* to the Display RAM. Since the same counter is used for both reading and writing, this command sets the next read *or write* address and the sense of the Auto-Increment mode for both operations.

8279 command word formats and bit descriptions. *(Intel Corporation)*

FIG 37

Design Realisation


COMP
SIDE
VDD


SIDE
2 OF 2

System Software

Future Developments

FUTURE DEVELOPMENTS

As per our original plan, we intend to make a Portable ECG Analyser, with a graphic LCD Display and a Keyboard interface, capable of storing upto 10 seconds of ECG data, with an RS232 interface for PC communication.

Also the ADC0809 used in this system has an 8-channel analog multiplexer. So upto 8 channels of input data can be stored and analysed, thus being capable of forming a part of a Hospital Patient Monitoring system. Also the USART interface includes the capability of a Bio-telemetric interface.

Since the development is a generalised Data Acquisition and Processing module, any type of varying signals can be studied.

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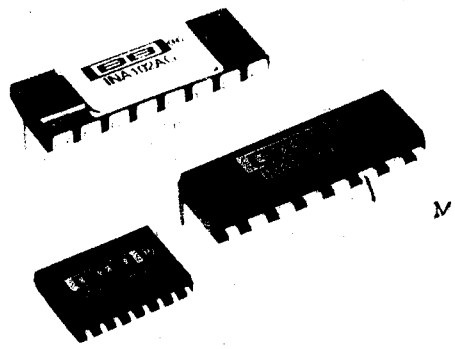
Appendix

BURR-BROWN®



INA102

Low-Power, High-Accuracy INSTRUMENTATION AMPLIFIER

FEATURES

- LOW-QUIESCENT POWER: 750μA, max
- INTERNAL GAINS: 1, 10, 100, 1000
- LOW-GAIN DRIFT: 5ppm/°C, max
- HIGH CMR: 90dB, min
- LOW-OFFSET VOLTAGE DRIFT: 2μV/°C, max
- LOW-OFFSET VOLTAGE: 100μV, max
- LOW NONLINEARITY: 0.01%, max
- HIGH-INPUT IMPEDANCE: $10^{10}\Omega$
- LOW COST

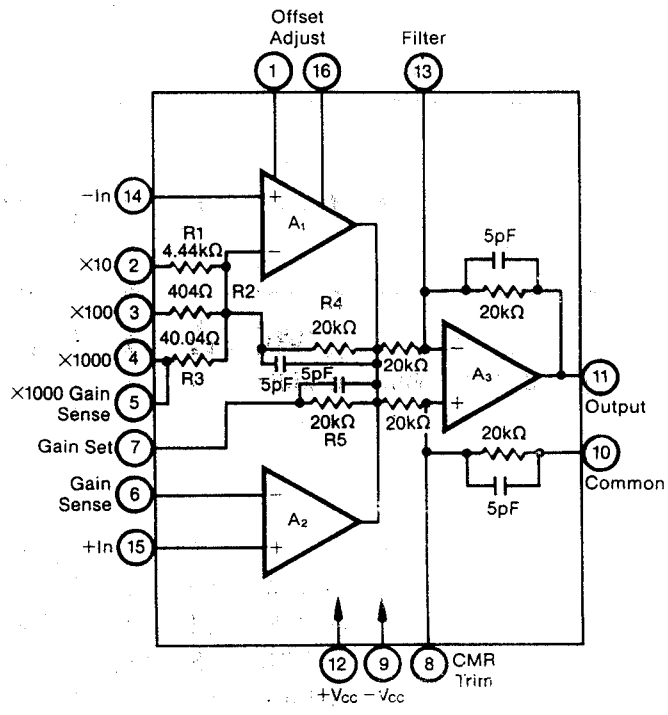
APPLICATIONS

- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS:
  - Strain Gauges
  - Thermocouples
  - RTDs
- REMOTE TRANSDUCER AMPLIFIER
- LOW-LEVEL SIGNAL AMPLIFIER
- MEDICAL INSTRUMENTATION
- MULTICHANNEL SYSTEMS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

The INA102 is a high-accuracy monolithic instrumentation amplifier designed for signal-conditioning applications where low-quiescent power is desired. On-chip thin-film resistors provide excellent temperature and stability performance. State-of-the-art laser-trimming technology insures high-gain accuracy and common-mode rejection while avoiding expensive external components. These features make the INA102 ideally suited for battery powered and high-volume applications.

The INA102 is also convenient to use. A gain of 1, 10, 100 or 1000 may be selected by simply strapping the appropriate pins together. 5ppm/°C gain drift in low gains can then be achieved without external adjustment. When higher than specified CMR is required, CMR can be trimmed using the pins provided. In addition, balanced filtering can be accomplished in the output stage.



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PDS-523E

Printed in U.S.A. December, 1988

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C with ±15VDC power supply and in circuit of Figure 2 unless otherwise noted.

MODEL	CONDITIONS	INA102AG			INA102CG			INA102KP/INA102AU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN											
Range of Gain		1		1000	*		*	*		*	V/V
Gain Equation, External, ±20%			G = 1 + (40k/R_G)[1]			*					V/V
Error, DC: G = 1	T_A = +25°C			0.1			0.05			0.15	%
G = 10	T_A = +25°C			0.1			0.05			0.35	%
G = 100	T_A = +25°C			0.25			0.15			0.4	%
G = 1000	T_A = +25°C			0.75			0.5			0.9	%
G = 1	T_A = T_{MIN} to T_{MAX}			0.16			0.08			0.21	%
G = 10	T_A = T_{MIN} to T_{MAX}			0.11			0.11			0.44	%
G = 100	T_A = T_{MIN} to T_{MAX}			0.37			0.21			0.52	%
G = 1000	T_A = T_{MIN} to T_{MAX}			0.93			0.62			1.08	%
Gain Temp. Coefficient											
G = 1				10			5			*	ppm/°C
G = 10				15			10			*	ppm/°C
G = 100				20			15			*	ppm/°C
G = 1000				30			20			*	ppm/°C
Nonlinearity, DC											
G = 1	T_A = +25°C			0.03			0.01			*	% of FS
G = 10	T_A = +25°C			0.03			0.01			*	% of FS
G = 100	T_A = +25°C			0.05			0.02			*	% of FS
G = 1000	T_A = +25°C			0.1			0.05			*	% of FS
G = 1	T_A = T_{MIN} to T_{MAX}			0.045			0.015			*	% of FS
G = 10	T_A = T_{MIN} to T_{MAX}			0.045			0.015			*	% of FS
G = 100	T_A = T_{MIN} to T_{MAX}			0.075			0.03			*	% of FS
G = 1000	T_A = T_{MIN} to T_{MAX}			0.15			0.1			*	% of FS
RATED OUTPUT											
Voltage	R_L = 10kΩ	±(|V_{CC}| −2.5)			*			*			V
Current		±1			*			*			mA
Short-Circuit Current[2]			2			*			*		mA
Output Impedance G = 1000			0.1			*			*		Ω
INPUT											
OFFSET VOLTAGE											
Initial Offset[3]	T_A = +25°C			±300			±100			*	μV
INA102AU				±300/G			±200/G			**±500** **±300/G**	μV
vs Temperature				±5			±2			*	μV/°C
				±10/G			±5/G				
vs Supply				±40			±10			*	μV/V
				±50/G			±20/G				
vs Time			±(20 +30/G)			*			*		μV/mo
BIAS CURRENT											
Initial Bias Current (each input)	T_A = T_{MIN} to T_{MAX}		25	50		6	30		*	*	nA
vs Temperature			±0.1			*			*		nA/°C
vs Supply			±0.1			*			*		nA/V
Initial Offset Current	T_A = T_{MIN} to T_{MAX}		±2.5	±15		±2.5	±10		*	*	nA
vs Temperature			±0.1			*			*		nA/°C
IMPEDANCE											
Differential			10^{10}||2			*			*		Ω || pF
Common-mode			10^{10}||2			*			*		Ω || pF
VOLTAGE RANGE											
Range, Linear Response	T_A = T_{MIN} to T_{MAX}	±(|V_{CC}| −4.5)			*			*			V
CMR with 1kΩ Source Imbalance											
G = 1	DC to 60 Hz	80	94		90	*		75	*		dB
G = 10	DC to 60 Hz	80	100		90	*		*	*		dB
G = 10 to 1000	DC to 60 Hz	80	100		90	*		*	*		dB
NOISE											
Input Voltage Noise											
f_B = 0.01Hz to 10Hz			1.0			*			*		μVp-p
Density, G = 1000											
f_o = 10Hz			30			*			*		nV/√Hz
f_o = 100Hz			25			*			*		nV/√Hz
f_o = 1kHz			25			*			*		nV/√Hz
Input Current Noise											
f_B = 0.01Hz to 10Hz			25			*			*		pA p-p
Density: f_o = 10Hz			0.3			*			*		pA/√Hz
f_o = 100Hz			0.2			*			*		pA/√Hz
f_o = 1kHz			0.15			*			*		pA/√Hz

ELECTRICAL (CONT)

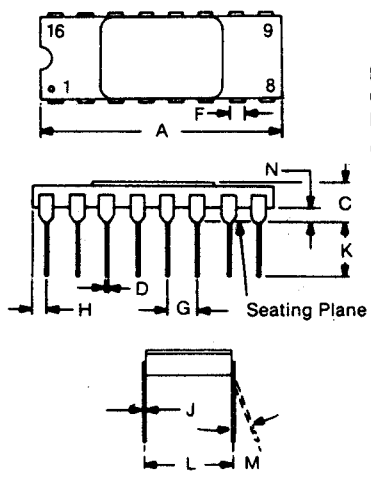
MODEL	CONDITIONS	INA102AG			INA102CG			INA102KP/INA102AU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC RESPONSE											
Small Signal											
±3dB Flatness	V_{OUT} = 0.1Vrms										
G = 1			300			*			*		kHz
G = 10			30			*			*		kHz
G = 100			3			*			*		kHz
G = 1000			0.3			*			*		kHz
Small Signal,											
±1% Flatness	V_{OUT} = 0.1Vrms										
G = 1			30			*			*		kHz
G = 10			3			*			*		kHz
G = 100			0.3			*			*		kHz
G = 1000			0.03			*			*		kHz
Full Power, G = 1 to 100	V_{OUT}=10V, R_L=10kΩ	1.7	2.5		*	*		*	*		kHz
Slew Rate, G = 1 to 100	V_{OUT}=10V, R_L=10kΩ	0.1	0.15		*	*		*	*		V/μs
Settling Time	R_L=10kΩ, C_L=100pF										
0.1%: G = 1	10V step		50			*			*		μs
G = 100			360			*			*		μs
G = 1000			3300			*			*		μs
0.01%: G = 1	10V step		60			*			*		μs
G = 100			500			*			*		μs
G = 1000			4500			*			*		μs
POWER SUPPLY											
Rated Voltage			±15			*			*		V
Voltage Range		±3.5		±18	*		*	*		*	V
Quiescent Current	V_O = 0V,										
	$T_A = T_{MIN}$ to T_{MAX}		±500	±750		*	*		*	*	μA
TEMPERATURE RANGE											
Specification		−25		+85	*		*	0		+70	°C
INA102AU								−25		+85	°C
Operation	$R_L > 50kΩ$[2]	−25		+85	*		*	−25		+85	°C
Storage		−65		+150	*		*	−55		+125	°C

*Specification same as for INA102AG.

NOTES: (1) The internal gain set resistors have an absolute tolerance of ±20%; however, their tracking is 50ppm/°C. R_G will add to the gain error if gains other than 1, 10, 100 or 1000 are set externally. (2) At high temperature, output drive current is limited. An external buffer can be used if required. (3) Adjustable to zero at any one time.

MECHANICAL

Hermetic

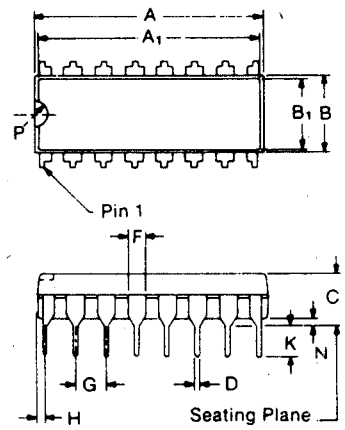


NOTE: Leads in true position within 0.10" (0.25mm) R at seating plane.
Pin numbers shown for reference only. Numbers are not marked on package.

CASE: Ceramic

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.048	.060	1.22	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

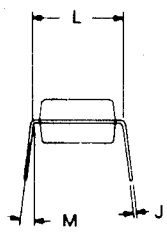
Plastic



NOTE: Leads in true position within 0.10" (0.25mm) R at seating plane.

PINS: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

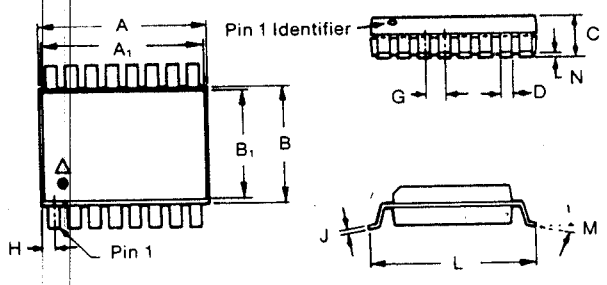
CASE: Plastic



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.740	.800	18.80	20.32
A_1	.725	.785	18.42	19.94
B	.230	.290	5.85	7.38
B_1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	0.02	0.05	0.51	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

IECHANICAL

SOIC



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.400	.416	10.16	10.57
A_1	.388	.412	9.86	10.46
B	.286	.302	7.26	7.67
B_1	.268	.286	6.81	7.26
C	.093	.109	2.36	2.77
D	.015	.020	0.38	0.51
G	.050 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.391	.421	9.93	10.69
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers are not marked on package.

RDERING INFORMATION

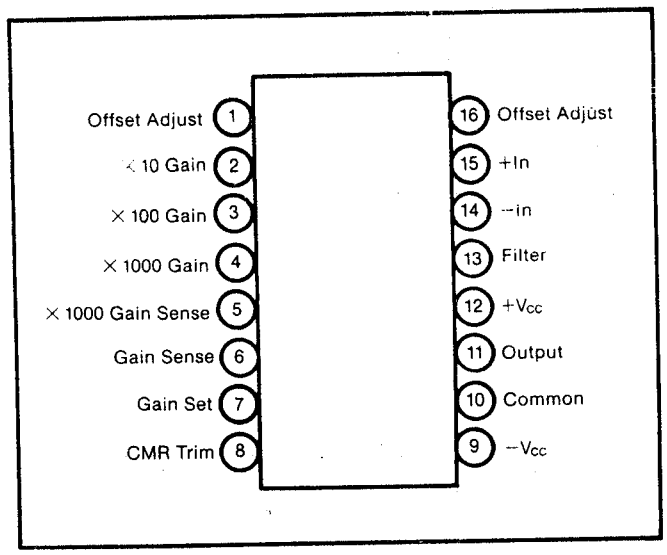
Model	Package	Temperature Range
NA102AG	Ceramic DIP	-25°C to +85°C
NA102CG	Ceramic DIP	-25°C to +85°C
NA102KP	Plastic DIP	0°C to +70°C
NA102AU	Plastic SOIC	-25°C to +85°C

BURN-IN SCREENING OPTION
See text for details.

Model	Package	Burn-In Temp. (160h)[1]
NA102AG-BI	Ceramic DIP	+125°C
NA102CG-BI	Ceramic DIP	+125°C
NA102KP-BI	Plastic DIP	+85°C
NA102AU-BI	Plastic SOIC	+85°C

OTE: (1) Or equivalent combination. See text.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply	±18V
Input Voltage Range	±Vcc
Operating Temperature Range	–25°C to +85°C
Storage Temperature Range: Ceramic	–65°C to +150°C
Plastic, SOIC	–55°C to +125°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-Circuit Duration	Continuous to ground

BURN-IN SCREENING

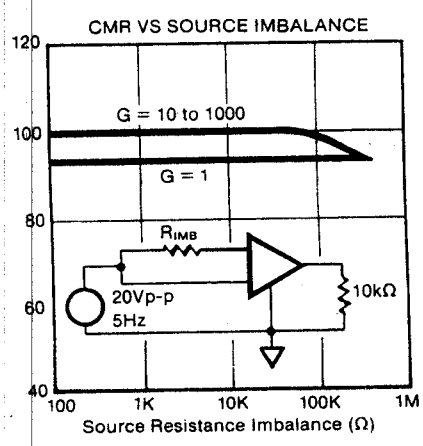
Burn-in screening is an option available for both plastic- and ceramic-packaged INA102s. Burn-in duration is 160 hours at the temperature shown below (or equivalent combination of time and temperature).

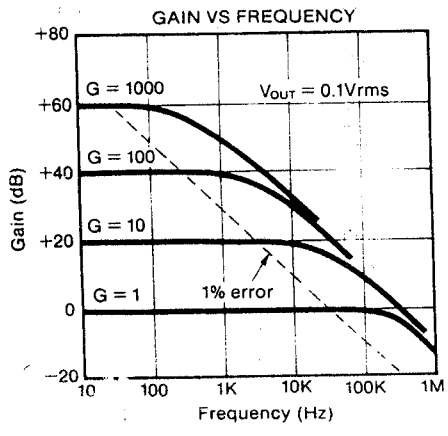
Plastic "-BI" models: +85°C
Ceramic "-BI" models: +125°C

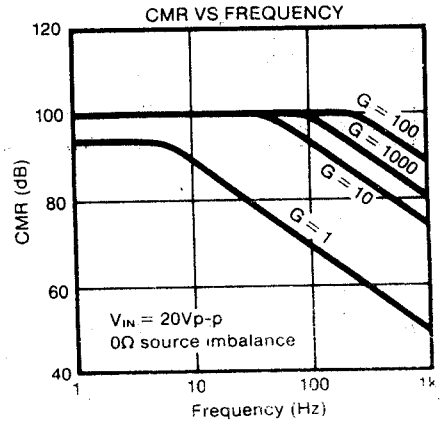
All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

YPICAL PERFORMANCE CURVES

+25°C and in circuit of Figure 2 unless otherwise noted.

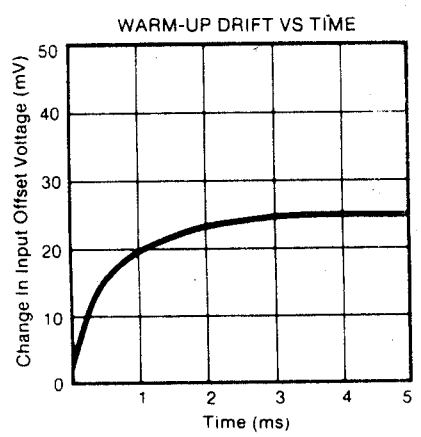


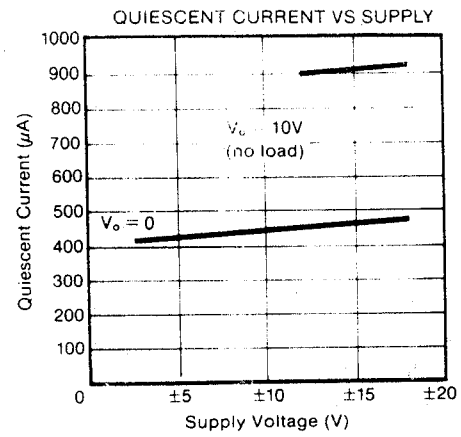


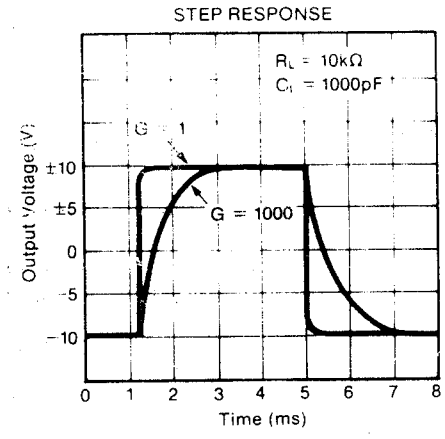


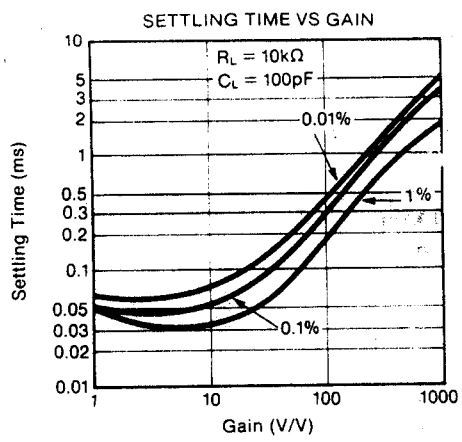
TYPICAL PERFORMANCE CURVES (CONT)

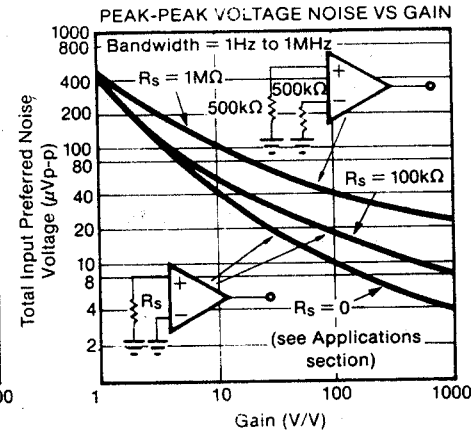
At +25°C and in circuit of Figure 2 unless otherwise noted.

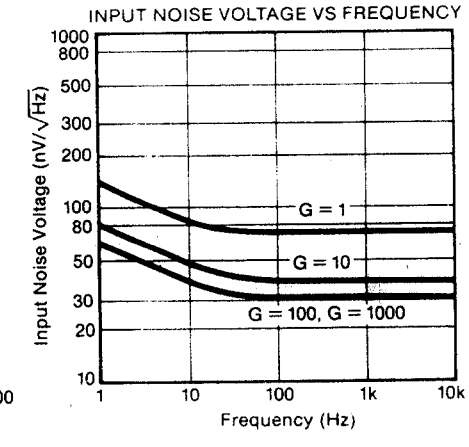


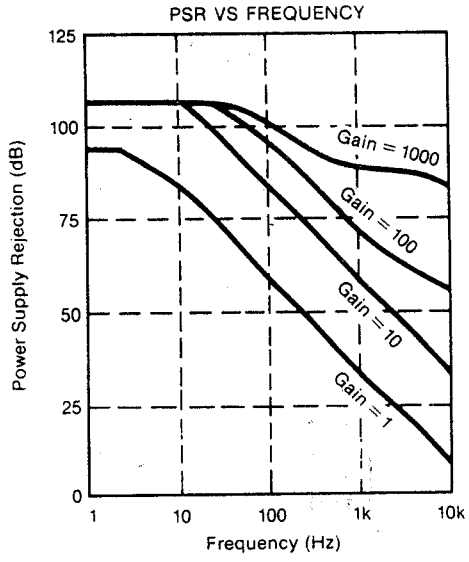












DISCUSSION OF PERFORMANCE

INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are differential input closed-loop gain blocks whose committed circuit accurately amplifies the voltage applied to their inputs. They respond mainly to the difference between the two input signals and exhibit extremely high input impedance, both differentially and common-mode. The feedback networks of this instrumentation amplifier is included on the monolithic chip. No external resistors are required for gains of 1, 10, 100, and 1000 in the INA102.

An operational amplifier, on the other hand, is an open-loop, uncommitted device that requires external networks to close the loop. While op amps can be used to achieve the same basic function as instrumentation amplifiers, it is very difficult to reach the same level of performance. Using op amps often leads to design tradeoffs when it is necessary to amplify low-level signals in the presence of common-mode voltages while maintaining high-input impedances. Figure 1 shows a simplified model of an instrumentation amplifier that eliminates most of the problems.

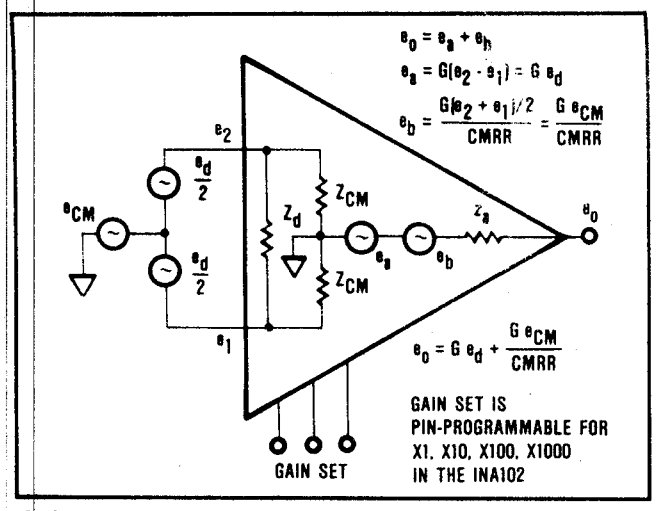


FIGURE 1. Model of an Instrumentation Amplifier.

THE INA102

A simplified schematic of the INA102 is shown on the first page. A three-amplifier configuration is used to provide the desirable characteristics of a premium performance instrumentation amplifier. In addition, it has features not normally found in integrated circuit instrumentation amplifiers.

The input buffers (A1 and A2) incorporate high performance, low-drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide the high input impedance ($10^{10}\Omega$) desirable in instrumentation amplifier applications. The offset voltage and offset voltage versus temperature are low due to the monolithic design, and improved even further by state-of-the-art laser-trimming techniques.

The output stage (A3) is connected in a unity-gain differential amplifier configuration. A critical part of this stage is the matching of the four 20kΩ resistors which provide the difference function. These resistors must be initially well matched and the matching must be maintained over temperature and time in order to retain good common-mode rejection.

All of the internal resistors are made of thin-film nichrome on the integrated circuit. The critical resistors are laser-trimmed to provide the desired high-gain accuracy and common-mode rejection. Nichrome ensures long-term stability and provides excellent TCR and TCR tracking. This provides gain accuracy and common-mode rejection when the INA102 is operated over wide temperature ranges.

USING THE INA102

Figure 2 shows the simplest configuration of the INA102. The output voltage is a function of the differential input voltage times the gain.

A gain of 1, 10, 100, or 1000 is selected by programming pins 2 through 7 (see Table I). Notice that for the gain of 1000, a special gain sense is provided to preserve accuracy. Although this is not always required, gain errors caused by external resistance in series with the low value 40.04Ω internal gain set resistor are thus eliminated.

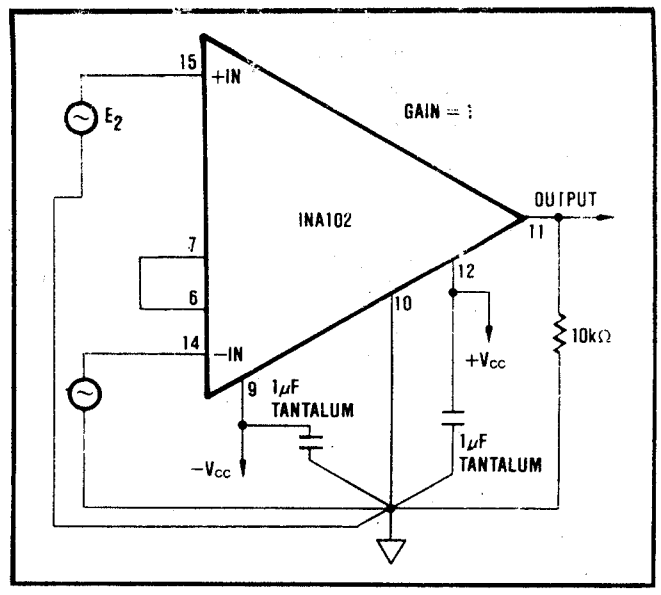


FIGURE 2. Basic Circuit Connection for the INA102.

Other gains between 1 and 10, 10 and 100, and 100 and 1000 can also be obtained by connecting an external resistor between pin 6 and either pin 2, 3, or 4, respectively (see Figure 6 for application).

$G = 1 + (40/R_G)$ where R_G is the total resistance between the two inverting inputs of the input op amps. At high gains, where the value of R_G becomes small, additional resistance (i.e., relays or sockets) in the R_G circuit will contribute to a gain error. Care should be taken to minimize this effect.

TABLE I. Pin-Programmable Gain Connections

GAIN	CONNECT PINS
1	6 to 7
10	2 to 6 and 7
100	3 to 6 and 7
1000	4 to 7 and separately 5 to 6

OPTIONAL OFFSET ADJUSTMENT PROCEDURE

It is sometimes desirable to null the input and/or output offset to achieve higher accuracy. The quality of the potentiometer will affect the results; therefore, choose one with good temperature and mechanical-resistance stability.

The optional offset null capabilities are shown in Figure 3. R_4 adjustment affects only the input stage component of the offset voltage. Note that the null condition will be disturbed when the gain is changed. Also, the input drift will be affected by approximately $0.31\mu V/°C$ per $100\mu V$ of input offset voltage that is trimmed. Therefore, care should be taken when considering use of the control for removal of other sources of offset. Output offset correction can be accomplished with A_1, R_1, R_2, and R_3, by applying a voltage to Common (pin 10) through a buffer amplifier. This buffer limits the resistance in series with pin 10 to minimize CMR error. Resistance above 0.1Ω will cause the common-mode rejection to fall below 100dB. Be certain to keep this resistance low.

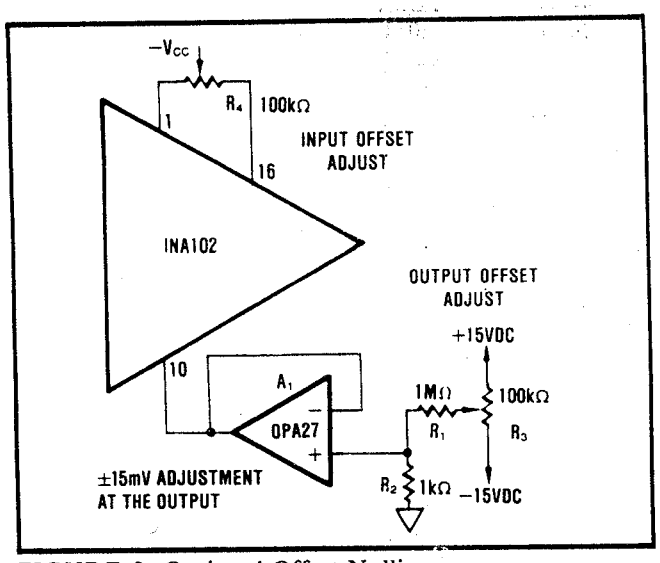


FIGURE 3. Optional Offset Nulling

It is important to not exceed the input amplifiers' dynamic range. The amplified differential input signal and its associated common-mode voltage should not cause the output of A_1 or A_2 to exceed approximately ±12V with ±15V supplies or nonlinear operation will result. To protect against moisture, especially in high gain, sealing compound may be used. Current injected into the offset pins should be minimized.

OPTIONAL FILTERING

The INA102 has provisions for accomplishing filtering with one external capacitor between pins 11 and 13. This single-pole filter can be used to reduce noise outside the signal bandwidth, but with some degradation to AC CMR.

When it is important to preserve CMR versus frequency (especially at 60Hz), two capacitors should be used. The additional capacitor is connected between pins 8 and 10. This will maintain a balance of impedances in the output stage. Either of these capacitors could also be trimmed slightly, to maximize CMR, if desired. Note that their ratio tracking will affect CMR over temperature.

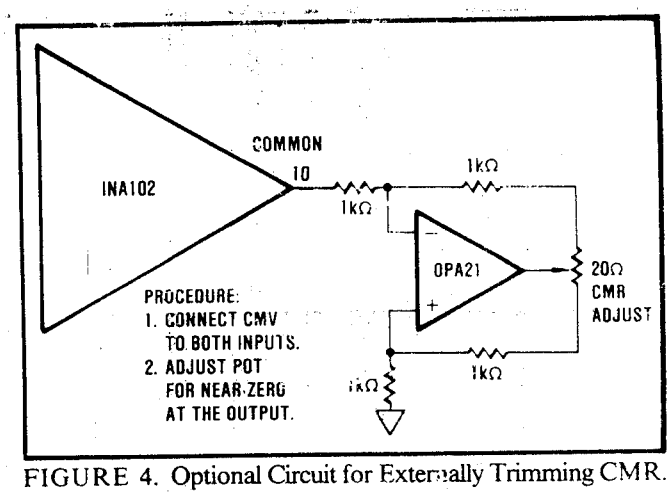


FIGURE 4. Optional Circuit for Externally Trimming CMR.

OPTIONAL COMMON-MODE REJECTION TRIM

The INA102 is laser-adjusted during manufacturing to assure high CMR. However, if desired, a small resistance can be added in series with pin 10 to trim the CMR to an improved level. Depending upon the nature of the internal imbalances, either a positive or negative resistance value could be required. The circuit shown in Figure 4 acts as a bipolar potentiometer and allows easy adjustment of CMR.

TYPICAL APPLICATIONS

Many applications of instrumentation amplifiers involve the amplification of low-level differential signals from bridges and transducers such as strain gauges, thermocouples, and RTDs. Some of the important parameters include common-mode rejection (differential cancellation of common-mode offset and noise, see Figure 1), input impedance, offset voltage and drift, gain accuracy, linearity, and noise. The INA102 accomplishes all of these with high precision at surprisingly low-quiescent current. However, in higher gains (>100), the bias current can cause a large offset error at the output. This can saturate the output unless the source impedance is separated, e.g., two 500kΩ paths instead of one 1MΩ unbalanced input.

Figures 5 through 16 show some typical applications circuits.

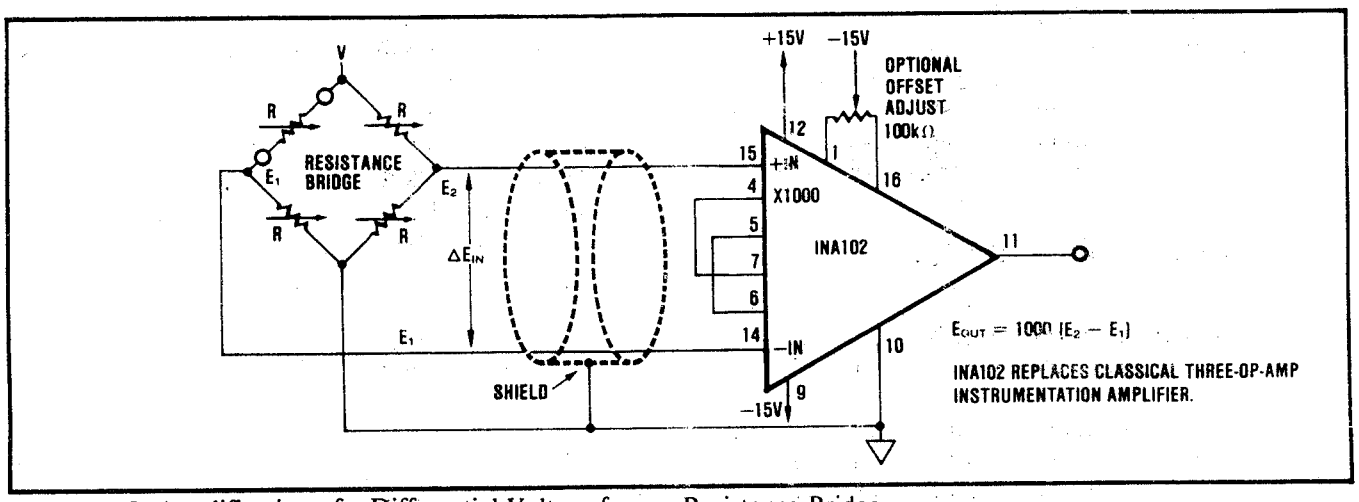


FIGURE 5. Amplification of a Differential Voltage from a Resistance Bridge.

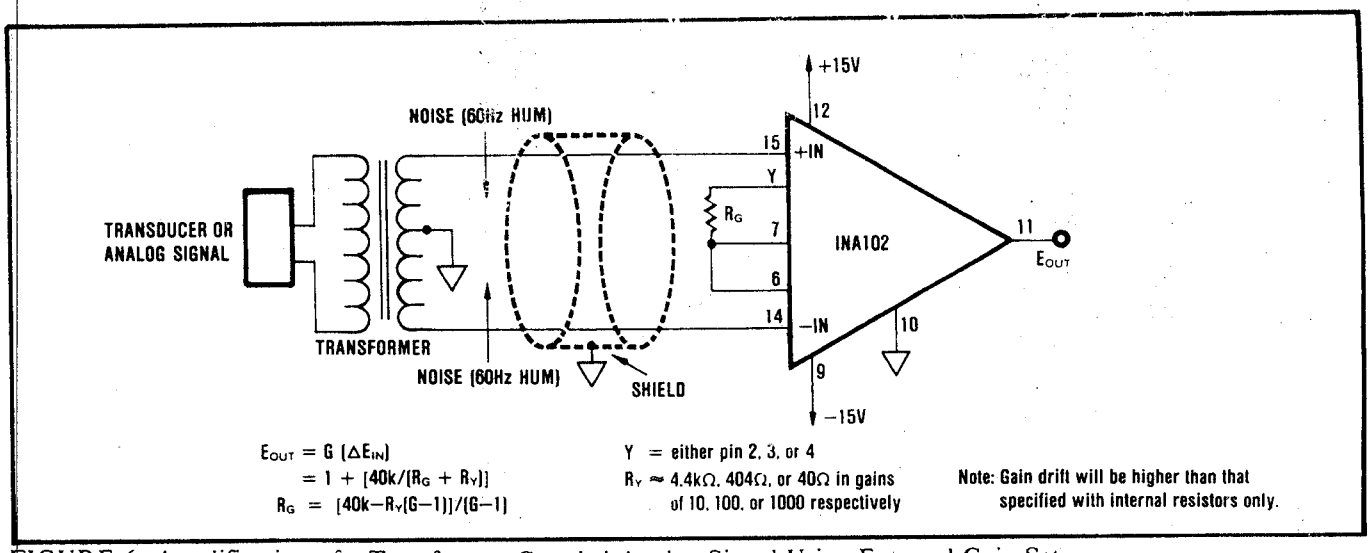


FIGURE 6. Amplification of a Transformer-Coupled Analog Signal Using External Gain Set.

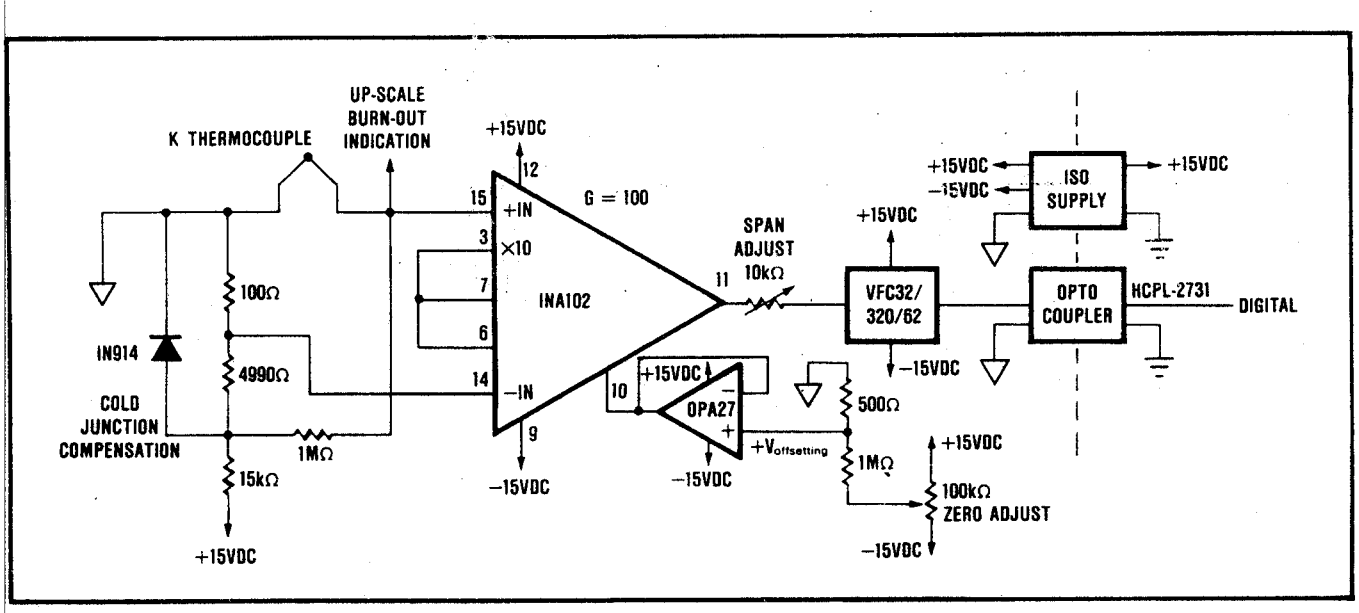


FIGURE 7. Isolated Thermocouple Amplifier with Cold Junction Compensation.

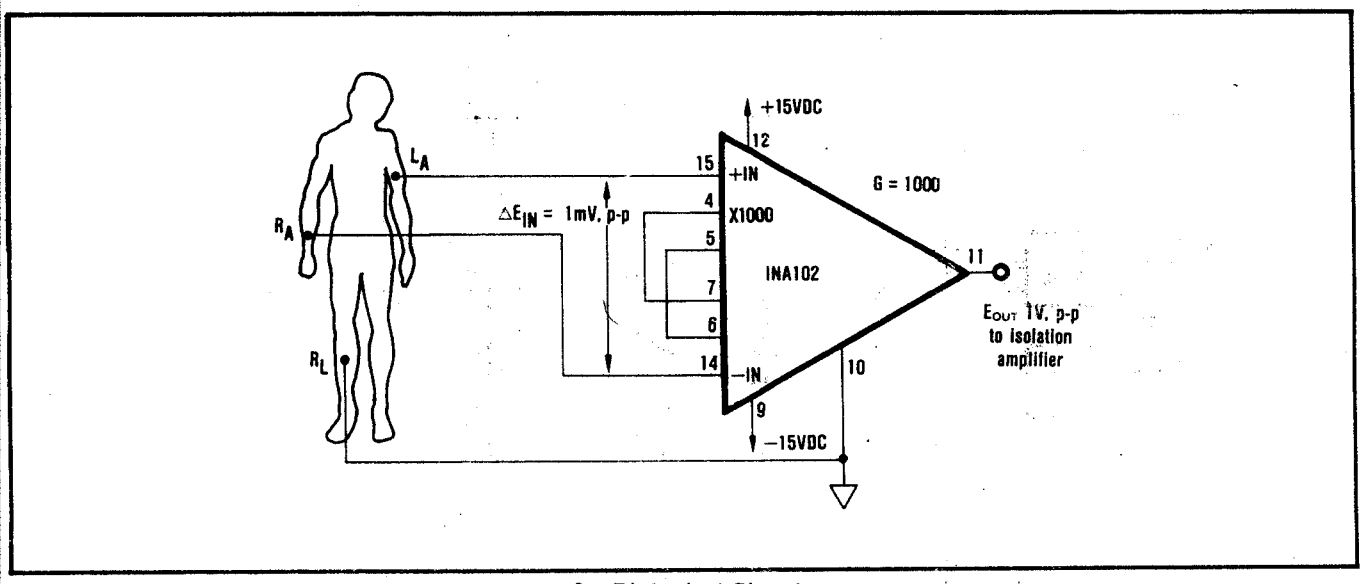


FIGURE 8. ECG Amplifier or Recorder Preamp for Biological Signals.

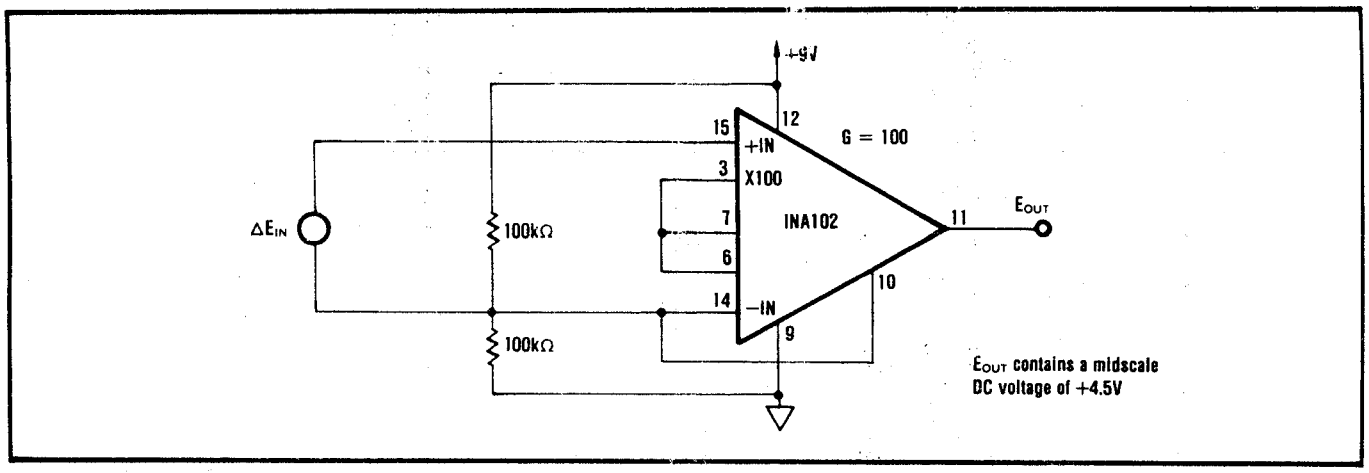


FIGURE 9. Single Supply Low Power Instrumentation Amplifier.

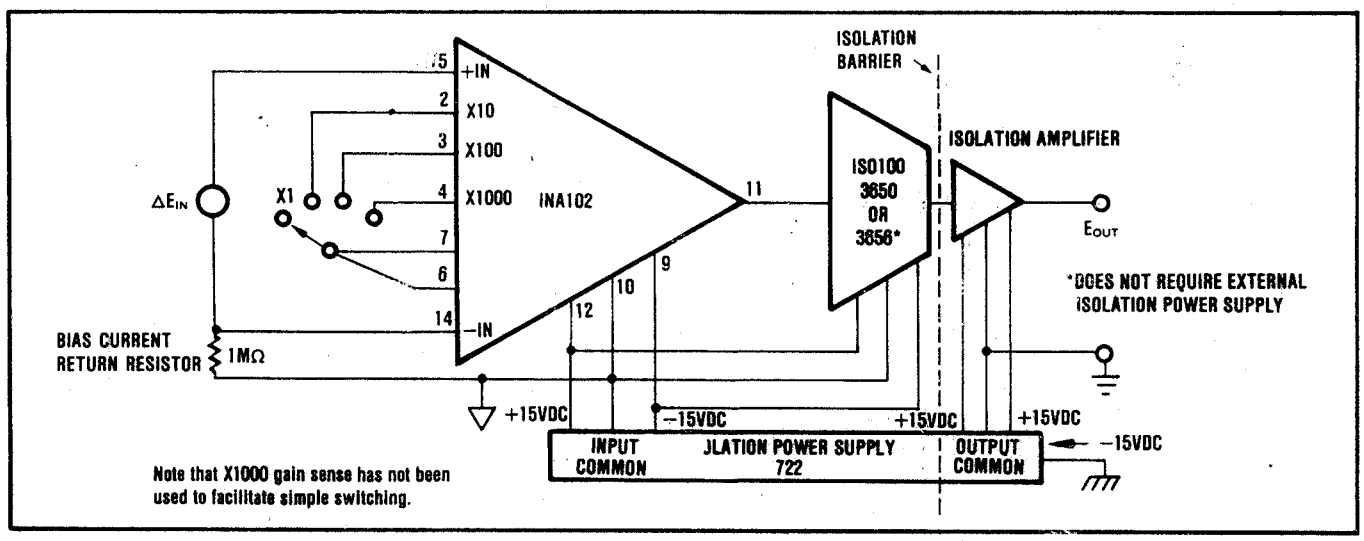


FIGURE 10. Precision Isolated Instrumentation Amplifier.

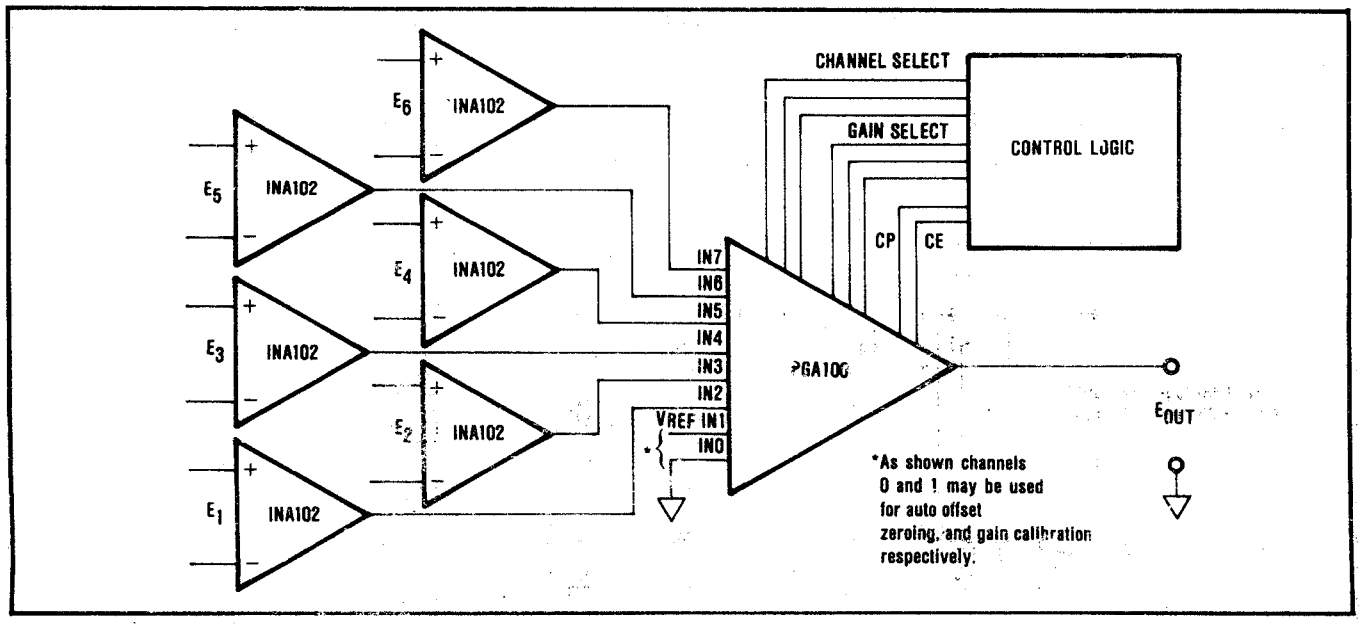


FIGURE 11. Multiple Channel Precision Instrumentation Amplifier with Programmable Gain.

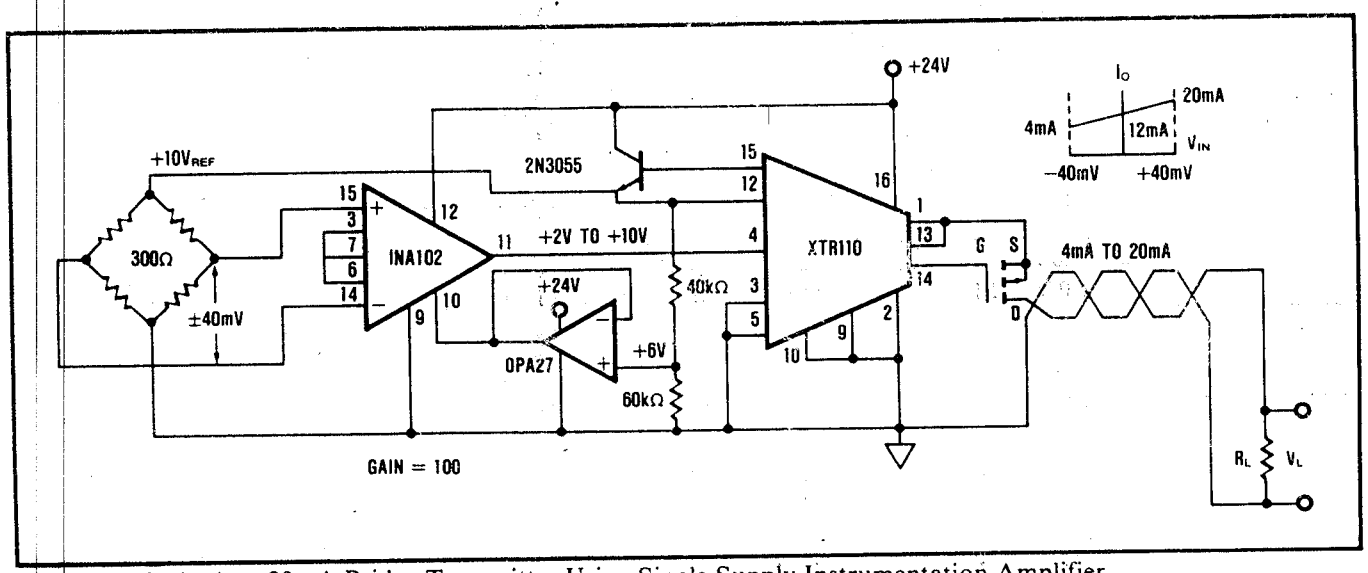


FIGURE 12. 4mA to 20mA Bridge Transmitter Using Single Supply Instrumentation Amplifier.

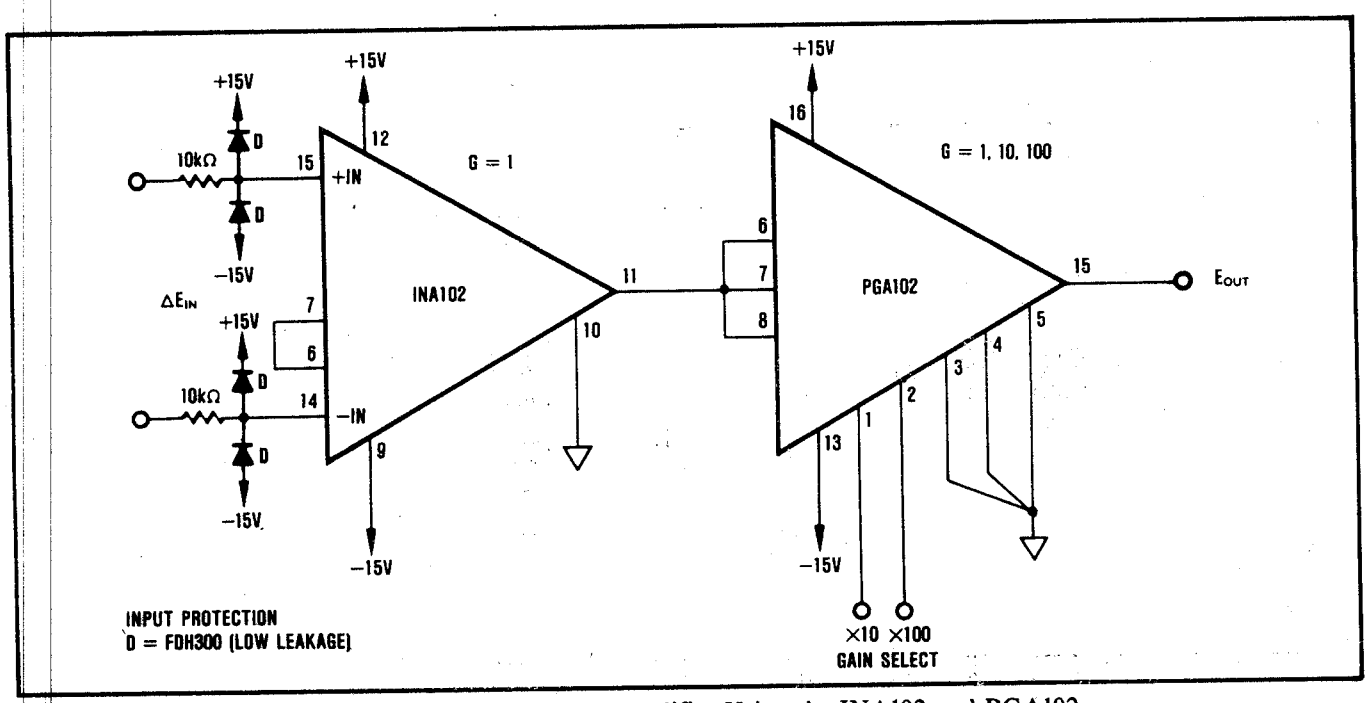


FIGURE 13. Programmable-Gain Instrumentation Amplifier Using the INA102 and PGA102.

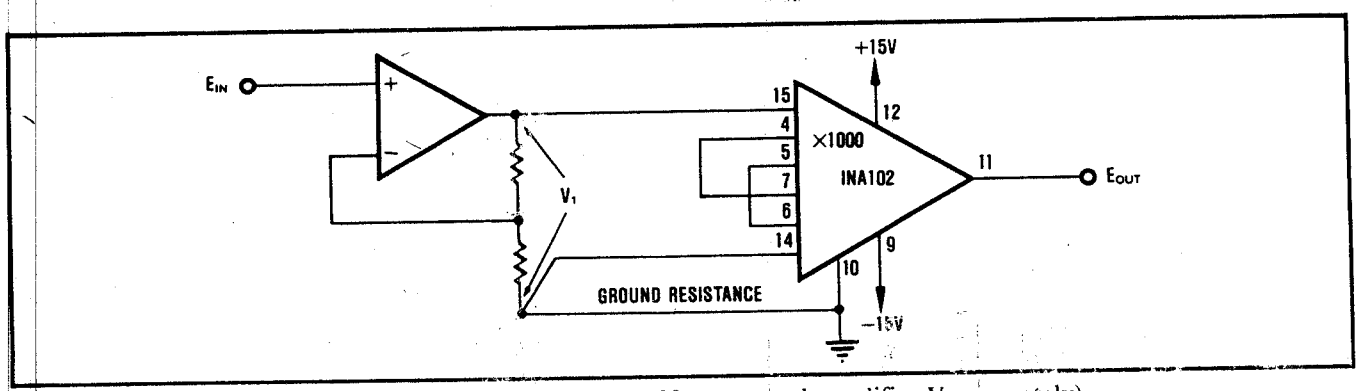


FIGURE 14. Ground Resistance Loop Eliminator (INA102 senses and amplifies V_1 accurately).

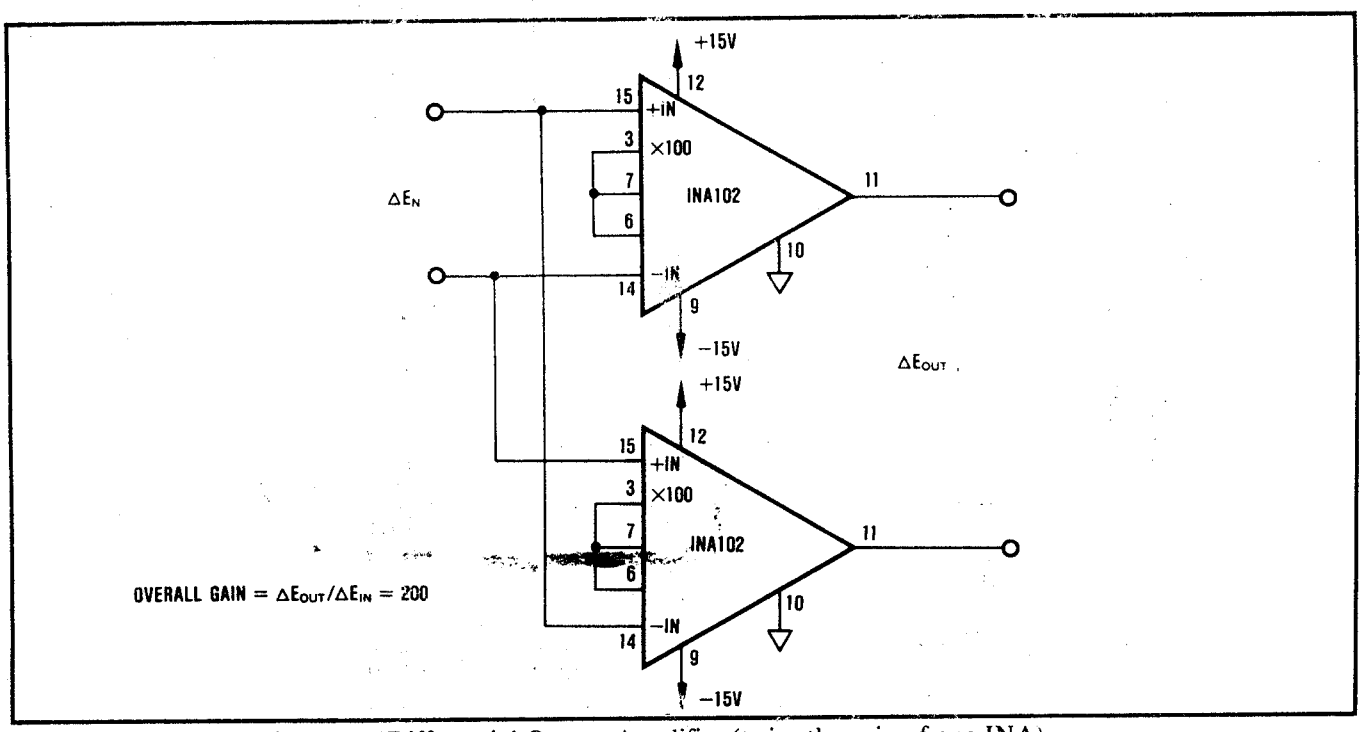
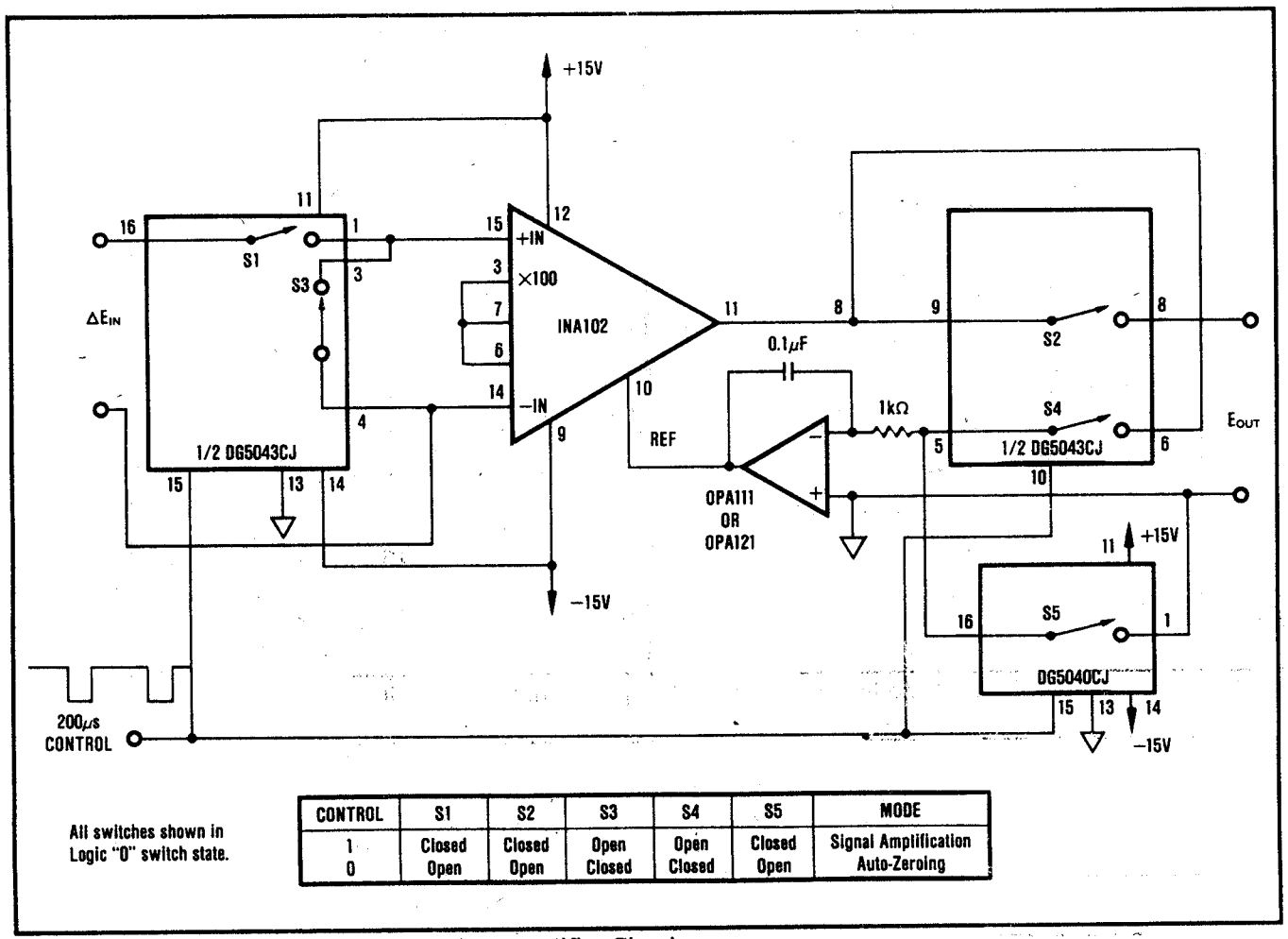


FIGURE 15. Differential Input/Differential Output Amplifier (twice the gain of one INA).



All switches shown in Logic "0" switch state.

CONTROL	S1	S2	S3	S4	S5	MODE
1	Closed	Closed	Open	Open	Closed	Signal Amplification
0	Open	Open	Closed	Closed	Open	Auto-Zeroing

FIGURE 16. Auto-Zeroing Instrumentation Amplifier Circuit.

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

93C06 -I /P

Package:	J	CERDIP
	P	Plastic DIP
	SN	Plastic SOIC (150 mil Body)
	SM	Plastic SOIC (207 mil Body)
Temperature Range:	Blank	0° C to +70° C
	I	-40° C to +85° C
	E	-40° C to +125° C
Device:	93C06	256-Bit CMOS Serial EEPROM
	93C06T	256-Bit CMOS Serial EEPROM (in Tape & Reel)

Microchip

93C46

1K (64 X 16) CMOS Serial Electrically Erasable PROM

FEATURES

- Low power CMOS technology
- 64 x 16 bit memory organization
- Single 5 volt only operation
- Self-timed ERASE and WRITE cycles
- Automatic ERASE before WRITE
- Power on/off data protection circuitry
- 1,000,000 ERASE/WRITE cycles (typical)
- Data Retention > 40 years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  - — Commercial: 0°C to +70°C
  - — Industrial: -40°C to +85°C
  - — Automotive: -40°C to +125°C
- 2 ms program cycle time

DESCRIPTION

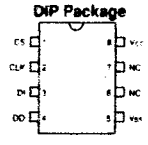
The Microchip Technology Inc. 93C46 is a 1K bit serial Electrically Erasable PROM. The device memory is configured as 64 x 16 bits. Advanced CMOS technology makes this device ideal for low-power non-volatile memory applications. The 93C46 is available in the standard 8-pin DIP and a surface mount SOIC package. The 93C46X comes as SOIC only.

This device offers fast (1 ms) byte write and extended (-40°C to 125°C) temperature operation. It is recommended that all other applications use Microchip's 93LC46.

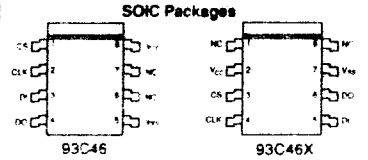
6

PIN CONFIGURATION

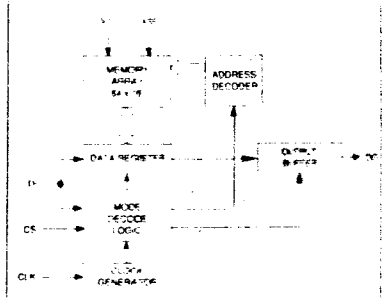
DIP Package



SOIC Packages



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. Vss ..... -0.3 V to +7.0 V
Storage temperature ..... -65°C to +150°C
Ambient temperature with power applied ..... -65°C to +125C
Soldering temperature of leads (10 seconds) ... +300°C
ESD protection on all pins ..... 4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Clock
DI	Data In
DO	Data Out
Vss	Ground
NC	No Connect; No Internal Connection
Vcc	+5 V Power Supply

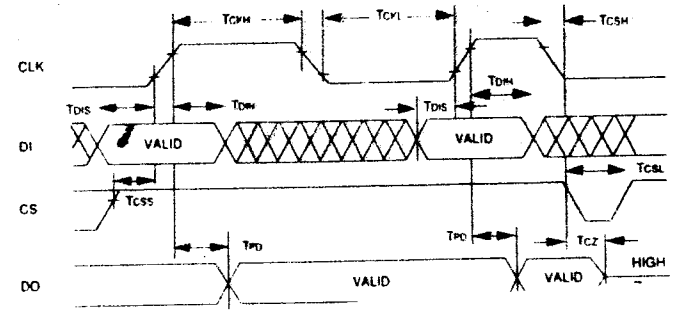
DC CHARACTERISTICS

Vcc = +5 V (±10%)
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = -40°C to +85°C
Automotive: Tamb = -40°C to +125°C (Note 3)

Parameter	Symbol	Min	Max	Units	Conditions
Vcc detector threshold	VTH	2.8	4.5	V	
High level input voltage	VIH	2.0	Vcc + 1	V	
Low level input voltage	VIL	-0.3	0.8	V	
High level output voltage	VOH	2.4		V	IOH = -400 µA
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA
Input leakage current	ILI		10	µA	VIN = 0 V to Vcc (Note 1)
Output leakage current	ILO		10	µA	VOUT = 0 V to Vcc (Note 1)
Internal capacitance (all inputs/outputs)	CINT		7	pF	VIN/VOUT = 0 V (Note 2) Tamb = +25°C, f = 1 MHz
Operating current (all modes)	ICC		4	mA	FCLK = 1 MHz, Vcc = 5.5 V
Standby current	ICCS		100	µA	CS = 0 V, Vcc = 5.5 V

Note 1: Internal resistor pull-up at Pin 6.
Note 2: This parameter is periodically sampled and not 100% tested.
Note 3: For operation above 85°C, endurance is rated at 10,000 ERASE/WRITE cycles.

SYNCHRONOUS DATA TIMING



AC CHARACTERISTICS

Parameter	Symbol	Min	Max	Units	Conditions
Clock frequency	FCLK		1	MHz	
Clock high time	TCKH	500		ns	
Clock low time	TCKL	500		ns	
Chip select setup time	TCSS	50		ns	
Chip select hold time	TCSH	0		ns	
Chip select low time	TCSL	100		ns	
Data input setup time	TDIS	100		ns	
Data input hold time	TDIH	100		ns	
Data output delay time	TPD		400	ns	CL = 100 pF
Data output disable time (from CS = low)	TCZ	0	100	ns	CL = 100 pF
Data output disable time (from last clock)	TDDZ	0	400	ns	CL = 100 pF
Status valid time	TSV		100	ns	CL = 100 pF
Program cycle time (Auto Erase & Write)	TWC		2 15	ms ms	for ERAL and WRAL
Erase cycle time	TEC		1	ms	
Endurance	---	100,000		E/W Cycles	

PIN DESCRIPTION

Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 100 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93C46. Op code, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime (with respect to clock HIGH time (TCKH) and clock LOW time (TCKL)). This gives the controlling master freedom in preparing opcode, address and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but START condition has not been detected, any number of [illegible]

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a start condition, the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become "Don't Care" inputs waiting for a new start condition to be detected.

Note: CS must go LOW between consecutive instructions.

Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/BUSY status information during ERASE and WRITE cycles. READY/BUSY status information is available on the DO pin if CS is brought HIGH after [illegible]

The status signal is not available on DO, if CS is held LOW or HIGH during the entire WRITE or ERASE cycle. In all other cases DO is in the HIGH-Z mode. If status is checked after the WRITE/ERASE cycle, a pull-up resistor on DO is required to read the READY signal.

DI and DO can be connected together to perform a 3-wire interface (CS, CLK, DI/DO).

Care must be taken with the leading dummy zero which is outputted after a READ command has been detected. Also, the controlling device must not drive the DI/DO bus during Erase and Write cycles if the READY/BUSY status information is outputted by the 93C46.

INSTRUCTION SET

Instruction	Start BIT	Opcode OP1 OP2	Address	Number of Data In	Data Out	Req. CLK Cycles
READ	1	1 0	A5 A4 A3 A2 A1 A0	—	D15 – D0	25
WRITE	1	0 1	A5 A4 A3 A2 A1 A0	D15 – D0	(RDY/$\overline{BSY}$)	25
ERASE	1	1 1	A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	9
EWEN	1	0 0	1 1 X X X X	—	High-Z	9
EWDS	1	0 0	0 0 X X X X	—	High-Z	9
ERAL	1	0 0	1 0 X X X X	—	(RDY/$\overline{BSY}$)	9
WRAL	1	0 0	0 1 X X X X	D15 – D0	(RDY/$\overline{BSY}$)	25

FUNCTIONAL DESCRIPTION

START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

Data Protection

During power-up, all modes of operation are inhibited until Vcc has reached 2.8 V. During power-down, the source data protection circuitry acts to inhibit all modes when Vcc has fallen below 2.8 V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed. After programming is completed, the EWDS instruction offers added protection against unintended data changes.

READ Mode

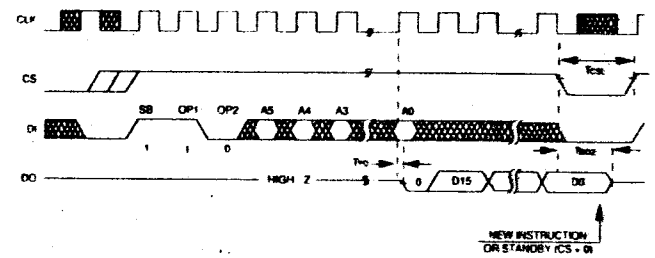
The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy bit (logical 0) precedes the 16-bit output string. The output data changes during the HIGH state of the system clock (CLK). The dummy bit is output TPD after the positive edge of CLK, which was used to clock in the last address bit (A0). Therefore, care must be taken if DI and DO are connected together as a bus contention will occur for one clock cycle if A0 has been a one.

DO will go into HIGH-Z mode with the positive edge of the next CLK cycle. This follows the output of the last data bit D0 or the low going edge of CS, which ever occurs first.

DO remains stable between CLK cycles for an unlimited time as long as CS stays HIGH.

The most significant data bit (D15) is always output first, followed by the lower significant bits (D14 - D0).

READ MODE

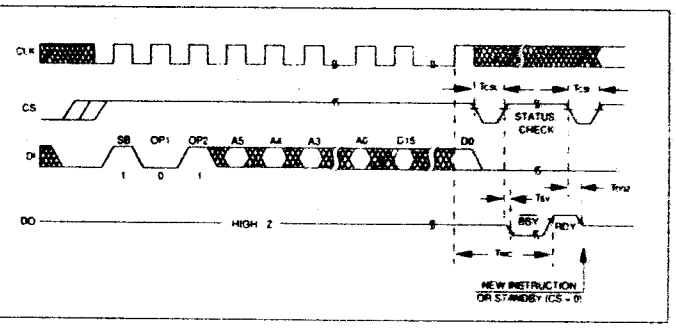


WRITE Mode

The WRITE instruction is followed by 16 bits of data which are written into the specified address. The most significant data bit (D15) has to be clocked in first, followed by the lower significant data bits (D14 – D0). If a WRITE instruction is recognized by the device and all data bits have been clocked in, the device performs an automatic ERASE cycle on the specified address before the data are written. The WRITE cycle is completely self-timed and commences automatically after the rising edge of the CLK for the last data bit (D0).

The WRITE cycle takes 2 ms max.

WRITE MODE

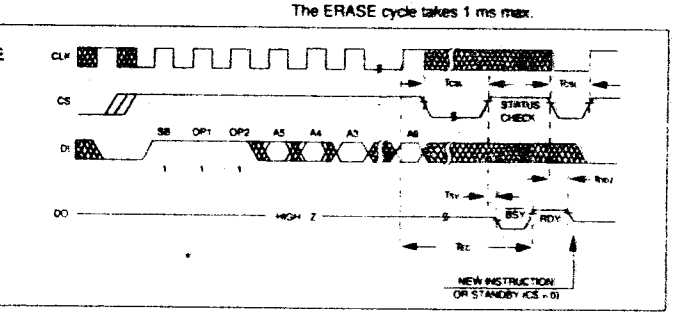


ERASE Mode

The ERASE instruction forces all the data bits of the specified address to logical "1s". The ERASE cycle is completely self-timed and commences automatically after the last address bit has been clocked in.

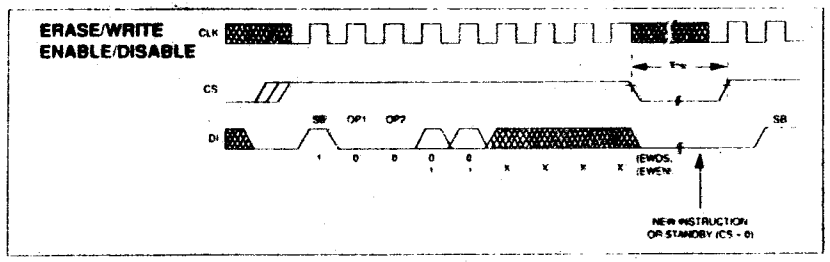
The ERASE cycle takes 1 ms max.

ERASE MODE



ERASE/WRITE Enable/Disable (EWEN, EWDS)

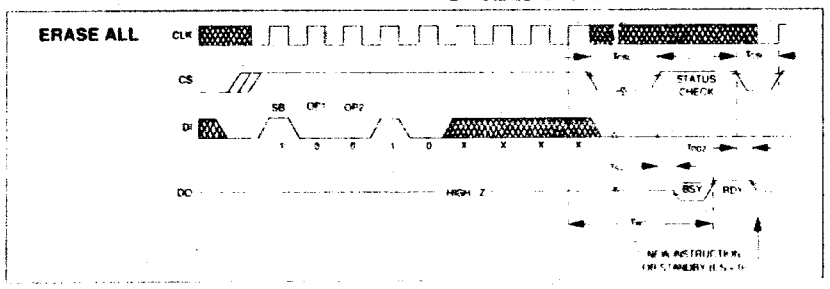
The device is automatically in the ERASE/WRITE Disable mode (EWDS) after power-up. Therefore, an EWEN instruction has to be performed before any ERASE, WRITE, ERAL, WRAL instruction is executed by the device. For added data protection, the device should be put in the ERASE/WRITE Disable mode (EWDS) after programming operations are completed.



ERASE All (ERAL)

The entire chip will be erased to logical "1s" if this instruction is received by the device and it is in the EWEN mode. The ERAL cycle is completely self-timed and commences after the last dummy address bit has been clocked in.

ERAL takes 15 ms max.

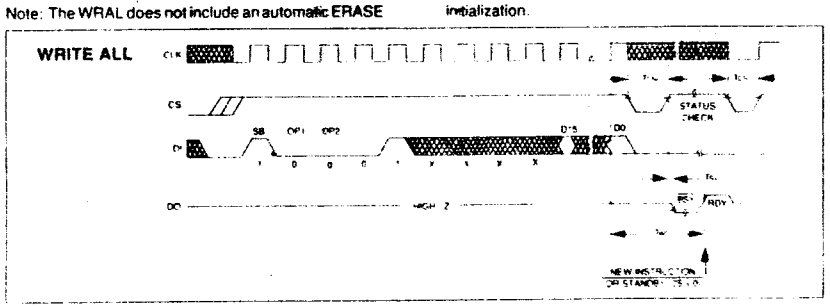


WRITE All (WRAL)

The entire chip will be written with the data specified in that command. The WRAL cycle is completely self-timed and commences after the rising edge of the CLK for the last data bit (DO). WRAL takes 15 ms max.

Note: The WRAL does not include an automatic ERASE cycle for the chip. Therefore, the WRAL instruction must be preceded by an ERAL instruction and the chip must be in the EWEN status in both cases.

The WRAL instruction is used for testing and/or device initialization.



NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g. on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

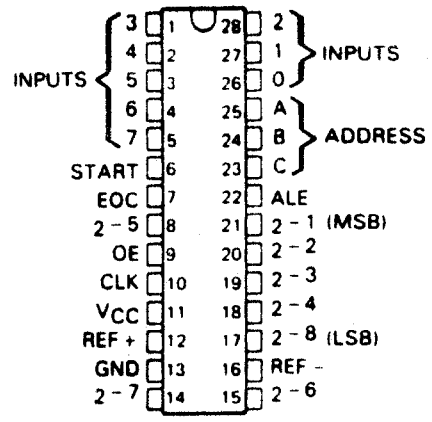
93C46 -I /P

Package:	J	CERDIP
	P	Plastic DIP
	SN	Plastic SOIC (150 mil Body)
	SM	Plastic SOIC (207 mil Body)
Temperature Range:	Blank	0° C to +70° C
	I	-40° C to +85° C
	E	-40° C to +125° C
Device:	93C46	1K CMOS Serial EEPROM
	93C46X	1K CMOS Serial EEPROM with alternate pinouts (in SN package only)
	93C46T	(in Tape & Reel)
	93C46XT	(in Tape & Reel)

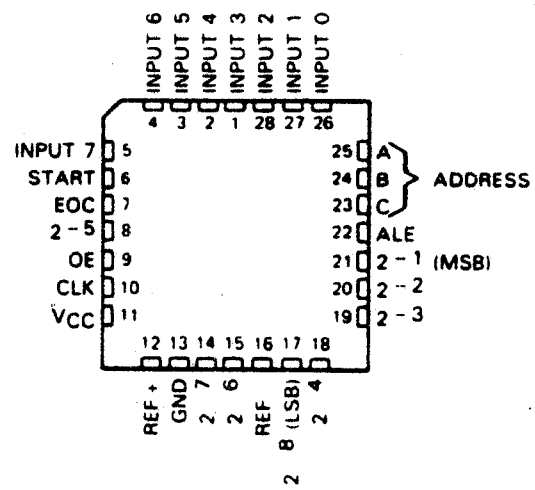
D2642, JUNE 1981 – REVISED MAY 1988

- **Total Unadjusted Error . . . ±0.75 LSB Max for ADC0808 and ±1.25 LSB Max for ADC0809**
- **Resolution of 8 Bits**
- **100 μs Conversion Time**
- **Ratiometric Conversion**
- **Monotonicity Over the Entire A/D Conversion Range**
- **No Missing Codes**
- **Easy Interface with Microprocessors**
- **Latched 3-State Outputs**
- **Latched Address Inputs**
- **Single 5-V Supply**
- **Low Power Consumption**
- **Designed to be Interchangeable with National Semiconductor ADC0808, ADC0809**

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



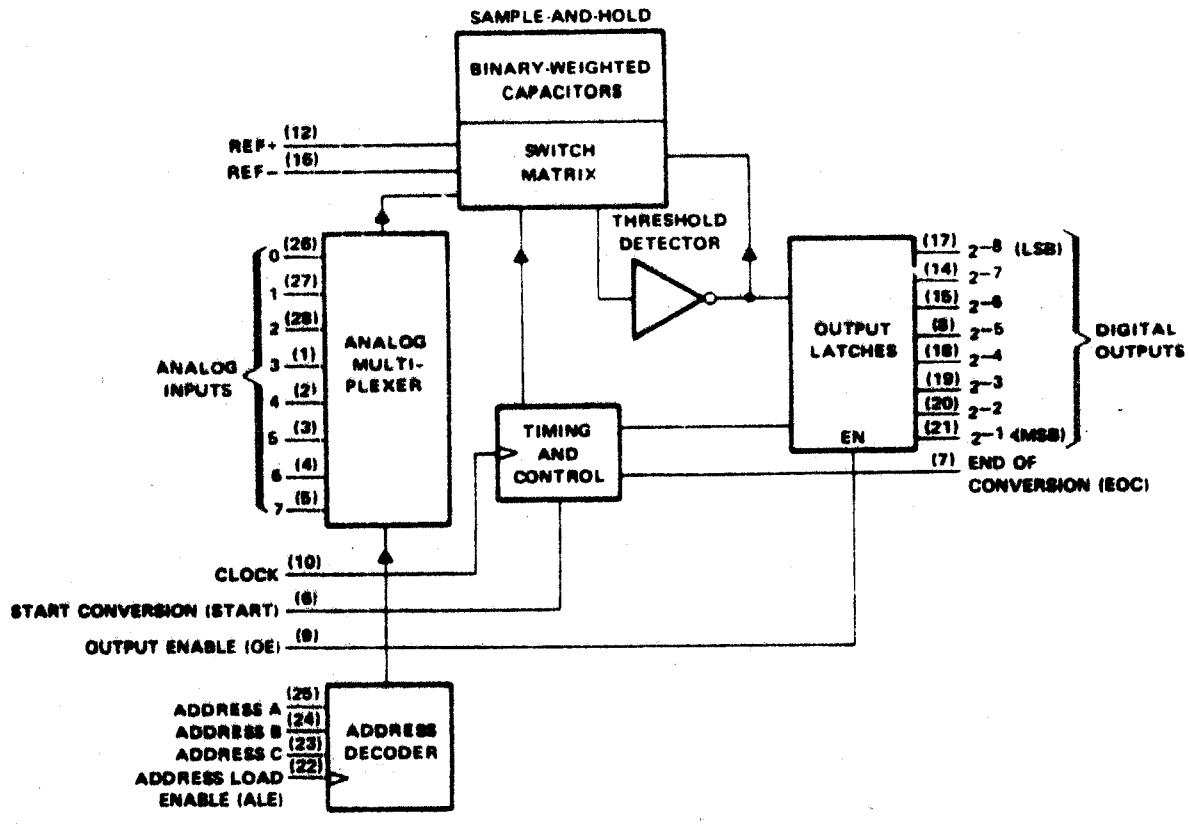
description

The ADC0808 and ADC0809 are monolithic CMOS devices with an 8-channel multiplexer, an 8-bit analog-to-digital (A/D) converter, and microprocessor-compatible control logic. The 8-channel multiplexer can be controlled by a microprocessor through a 3-bit address decoder with address load to select any one of eight single-ended analog switches connected directly to the comparator. The 8-bit A/D converter uses the successive-approximation conversion technique featuring a high-impedance threshold detector, a switched-capacitor array, a sample-and-hold, and a successive-approximation register (SAR). Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The comparison and converting methods used eliminate the possibility of missing codes, nonmonotonicity, and the need for zero or full-scale adjustment. Also featured are latched 3-state outputs from the SAR and latched inputs to the multiplexer address decoder. The single 5-V supply and low power requirements make the ADC0808 and ADC0809 especially useful for a wide variety of applications. Ratiometric conversion is made possible by access to the reference voltage input terminals.

The ADC0808 and ADC0809 are characterized for operation from −40°C to 85°C.

functional block diagram (positive logic)



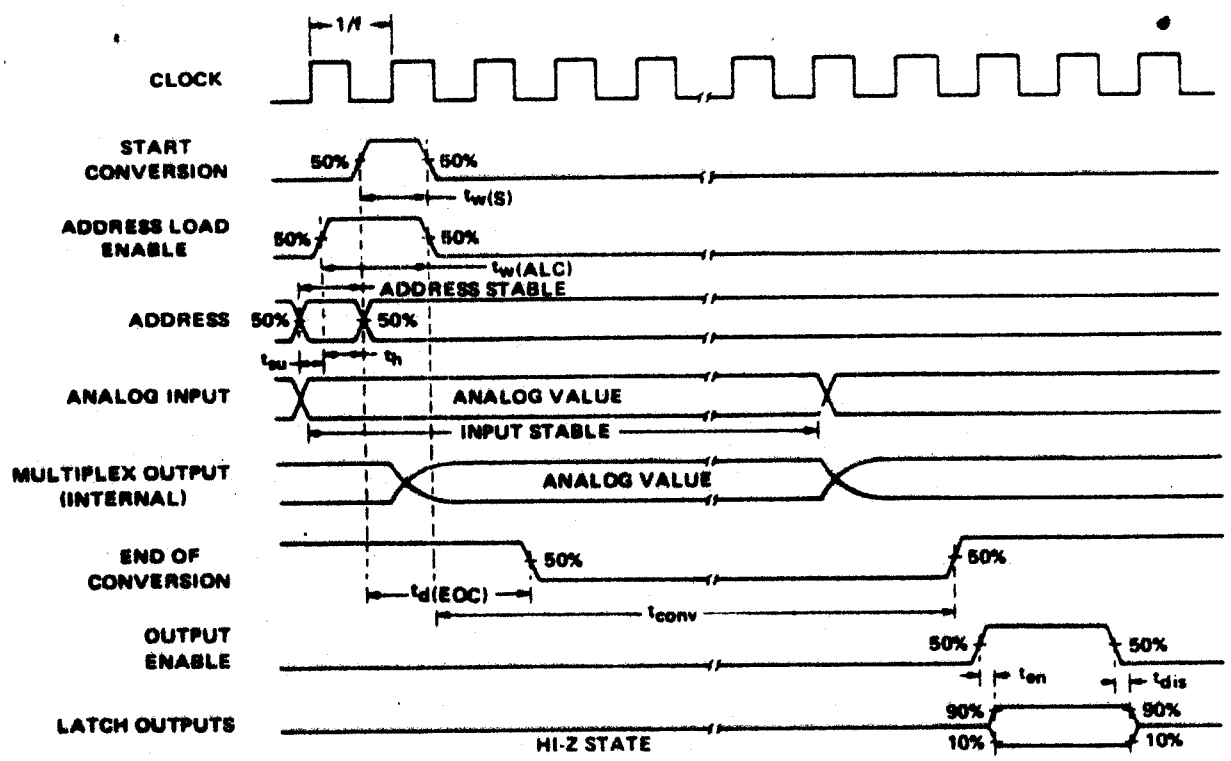
MULTIPLEXER FUNCTION TABLE

INPUTS				SELECTED
ADDRESS			ADDRESS	ANALOG
C	B	A	STROBE	CHANNEL
L	L	L	↑	0
L	L	H	↑	1
L	H	L	↑	2
L	H	H	↑	3
H	L	L	↑	4
H	L	H	↑	5
H	H	L	↑	6
H	H	H	↑	7

H = high level, L = low level
↑ = low-to-high transition

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS TEXAS 75265

operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range: control inputs . . . . . −0.3 to 15 V
all other inputs . . . . . −0.3 V to V_{CC} + 0.3 V
Operating free-air temperature range . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	6	V
Positive reference voltage, V_{ref+} (see Note 2)		V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{ref-}		0	−0.1	V
Differential reference voltage, $V_{ref+} - V_{ref-}$		5		V
High-level input voltage, V_{IH}	$V_{CC}-1.5$			V
Low-level input voltage, V_{IL}			1.5	V
Operating free-air temperature, T_A	−40		85	°C

NOTE 2: Care must be taken that this rating is observed even during power-up.

electrical characteristics over recommended operating free-air temperature range. V_{CC} = 4.75 V to 5.25 V (unless otherwise noted)

total device

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_O = −360 μA	$V_{CC}-0.4$			V
V_{OL}	Low-level output voltage	Data outputs	I_O = 1.6 mA			0.45	V
		End of conversion	I_O = 1.2 mA			0.45	
I_{OZ}	Off-state (high-impedance-state) output current		$V_O = V_{CC}$			3	μA
			V_O = 0			−3	
I_I	Control input current at maximum input voltage		V_I = 15 V			1	μA
I_{IL}	Low-level control input current		V_I = 0			−1	μA
I_{CC}	Supply current		f_{clock} = 640 kHz		0.3	3	mA
C_i	Input capacitance, control inputs		T_A = 25°C		10	15	pF
C_o	Output capacitance, data outputs		T_A = 25°C		10	15	pF
	Resistance from pin 12 to pin 16				1000		kΩ

analog multiplexer

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{on}	Channel on-state current (see Note 3)	$V_I = V_{CC}$,	f_{clock} = 640 kHz			2	μA
		V_I = 0.1 V,	f_{clock} = 640 kHz			−2	
I_{off}	Channel off-state current	V_{CC} = 5 V, T_A = 25°C	V_I = 5 V		10	200	nA
			V_I = 0		−10	−200	
		V_{CC} = 5 V	V_I = 5 V			1	μA
			V_I = 0			−1	

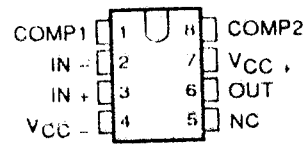
†Typical values are at V_{CC} = 5 V and T_A = 25°C.
NOTE 3: Channel on-state current is primarily due to the bias current into or out of the threshold detector, and it varies directly with clock frequency

LM108, LM108A, LM208, LM208A, LM308, LM308A
OPERATIONAL AMPLIFIERS

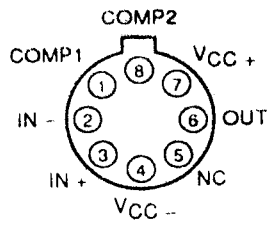
D2808, OCTOBER 1983 - REVISED FEBRUARY 1991

- Input Offset Current . . . 200 pA Max at 25°C for LM108, LM108A, LM208, LM208A
- Input Bias Current . . . 2 nA Max at 25°C for LM108, LM108A, LM208, LM208A
- Supply Current . . . 600 µA Max at 25°C for LM108, LM108A, LM208, LM208A
- Input Offset Voltage . . . 500 µV Max at 25°C for LM108A, LM208A, LM308A
- Offset Voltage Temperature Coefficient . . . 5 µV/°C Max for LM108A, LM208A, LM308A
- Supply Voltage Range . . . ±2 V to ±18 V
- Applications:
  - Integrators
  - Transducer Amplifiers
  - Analog Memories
  - Light Meters
- Designed To Be Interchangeable With National LM108 Series and Linear Technology LM108 Series

D, JG, OR P PACKAGE
(TOP VIEW)

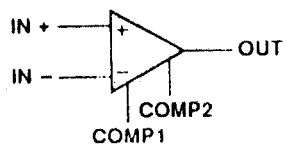


L PACKAGE
(TOP VIEW)



NC – No internal connection
Pin 4 (L package) is in electrical contact with the case.

symbol



description

The LM108 series of precision operational amplifiers is particularly well-suited for high-source-impedance applications requiring low input offset and bias currents as well as low power dissipation. Unlike FET input amplifiers, the input offset and bias currents of the LM108 series do not vary significantly with temperature. Advanced design, processing, and testing techniques make this series a superior choice over previous devices. For applications requiring higher performance, see the LT1008 and LT1012.

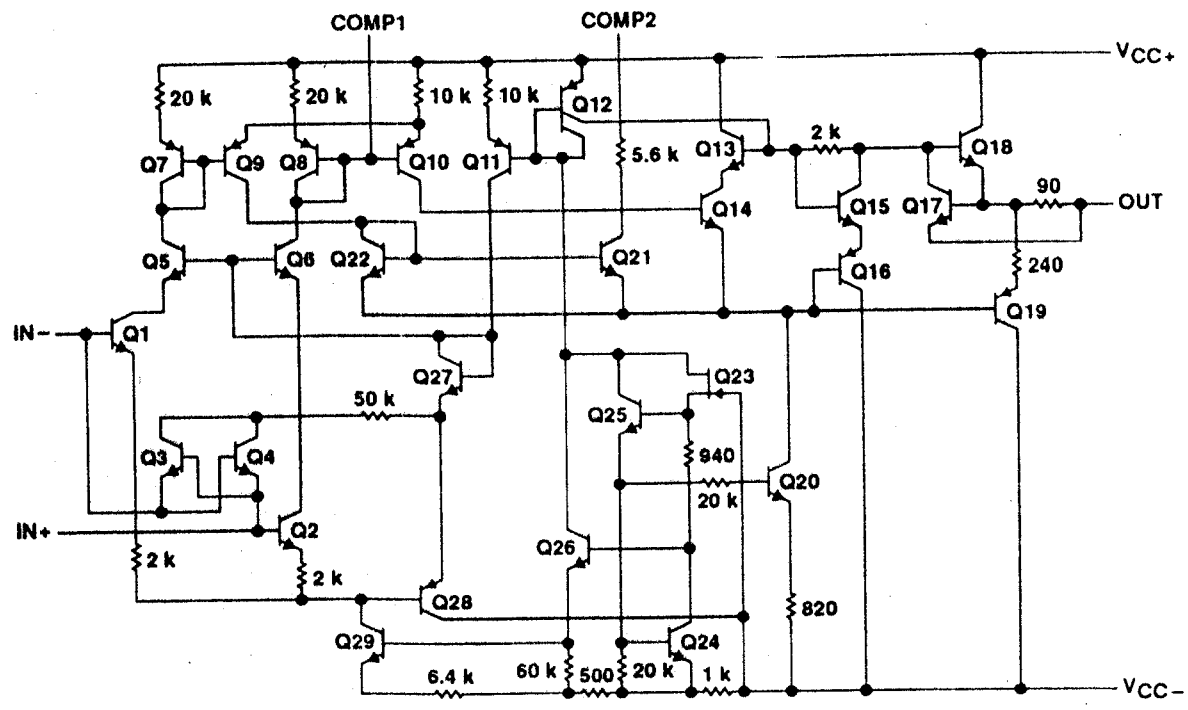
The LM108 and LM108A are characterized for operation over the full military temperature range of −55°C to 125°C. The LM208 and LM208A are characterized for operation from −40°C to 105°C. The LM308 and LM308A are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	0.5 mV	LM308AD	———	———	LM308AP
	7.5 mV	LM308D	———	———	LM308P
−40°C to 105°C	0.5 mV	LM208AD	———	———	LM208AP
	2 mV	LM208D	———	———	LM208P
−55°C to 125°C	0.5 mV	LM108AD	LM108AJG	LM108AL	LM108AP
	2 mV	LM108D	LM108JG	LM108L	LM108P

The D package is available taped and reeled. Add the suffix R to the device type (e.g., LM308ADR).

schematic



All resistor values shown are nominal and in ohms

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1): LM108, LM108A, LM208, LM208A . . . . . 20 V
LM308, LM308A . . . . . 18 V
Supply voltage, V_{CC-} (see Note 1): LM108, LM108A, LM208, LM208A . . . . . −20 V
LM308, LM308A . . . . . −18 V
Input voltage range, V_I (see Note 2) . . . . . ±15 V
Differential input current (see Notes 3 and 4) . . . . . ±10 mA
Duration of output short-circuit at (or below) 25°C (see Note 5) . . . . . unlimited
Operating free-air temperature range, T_A: LM108, LM108A . . . . . −55°C to 125°C
LM208, LM208A . . . . . −40°C to 105°C
LM308, LM308A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: JG or L package . . . . . 300°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
3. The inputs are shunted with two opposite-facing base-emitter diodes for over-voltage protection. Therefore, excessive current will flow if a differential input voltage in excess of approximately 1 V is applied between the inputs unless some limiting resistance is used.
4. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
5. The output may be shorted to ground or either power supply.

recommended operating conditions

	LM108, LM108A			LM208, LM208A			LM308, LM308A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+}	5		20	5		20	5		20	V
Supply voltage, V_{CC-}	-5		-20	-5		-20	-5		-20	V
Operating free-air temperature, T_A	-55		125	-40		85	0		70	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V to ±20 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LM108A, LM208A			LM108, LM208			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω	25°C		0.3	0.5		0.7	2	mV
			Full range			1			3	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1	5*		3	15*	µV/°C
I_{IO}	Input offset current		25°C		0.05	0.2		0.05	0.2	nA
			Full range			0.4			0.4	
α_{IIO}	Temperature coefficient of input offset current		Full range		0.5	2.5*		0.5	2.5*	pA/°C
I_{IB}	Input bias current		25°C		0.5	2		0.5	2	nA
			Full range			3			3	
V_{ICR}	Common-mode input voltage range	$V_{CC\pm}$ = ±15 V	Full range	±13.5			±13.5			V
V_{OM}	Maximum peak output voltage swing	$V_{CC\pm}$ = ±15 V, R_L = 10 kΩ	Full range	±13			±13			V
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, V_O = ±10 V, R_L ≥ 10 kΩ	25°C	80	300		50	300		V/mV
			Full range	40			25			
r_i	Input resistance		25°C	30*	70		30*	70		MΩ
CMRR	Common-mode rejection ratio		Full range	96			85			dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}$ / ΔV_{IO})		Full range	96			80			dB
I_{CC}	Supply current		25°C		0.3	0.6		0.3	0.6	mA
			105°C, 125°C			0.4			0.4	

*On products compliant to MIL-STD-883, Class B, these parameters are not production tested.
†Full range is −40°C to 105°C for the LM208 and LM208A and −55°C to 125°C for the LM108 and LM108A.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V to ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LM308A			LM308			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω	25°C		0.3	0.5		2	7.5	mV
			Full range			0.73			10	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2	5		6	30	µV/°C
I_{IO}	Input offset current		25°C		0.2	1		0.2	1	nA
			Full range			1.5			1.5	
α_{IIO}	Temperature coefficient of input offset current		Full range		2	10		2	10	pA/°C
I_{IB}	Input bias current		25°C		1.5	7		1.5	7	nA
			Full range			10			10	
V_{ICR}	Common-mode input voltage range	$V_{CC\pm}$ = ±15 V	Full range	±14			±14			V
V_{OM}	Maximum peak output voltage swing	$V_{CC\pm}$ = ±15 V, R_L = 10 kΩ	Full range	±13			±13			V
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, V_O = ±10 V, R_L ≥ 10 kΩ	25°C	80	300		25	300		V/mV
			Full range	60			15			
r_i	Input resistance		25°C	10	40		10	40		MΩ
CMRR	Common-mode rejection ratio		Full range	96			80			dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}$ / ΔV_{IO})		Full range	96			80			dB
I_{CC}	Supply current		25°C		0.3	0.8		0.3	0.8	mA

†Full range is 0°C to 70°C.

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT OFFSET VOLTAGE
vs
MATCHED SOURCE RESISTANCE

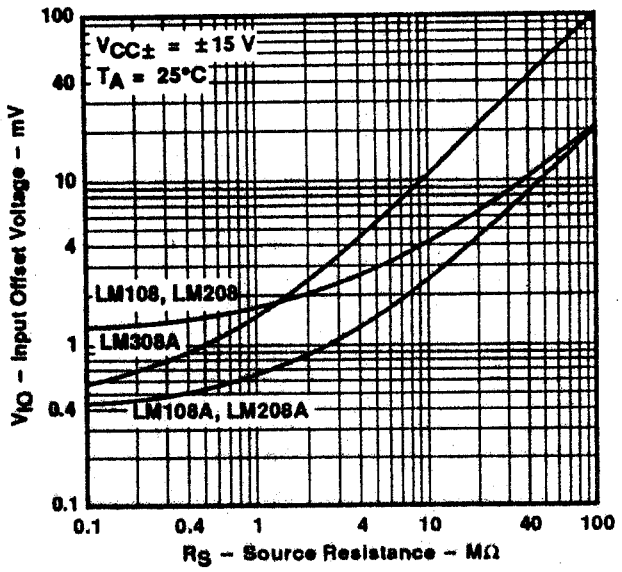


Figure 1

TEMPERATURE COEFFICIENT
OF EQUIVALENT INPUT OFFSET VOLTAGE
vs
MATCHED SOURCE RESISTANCE

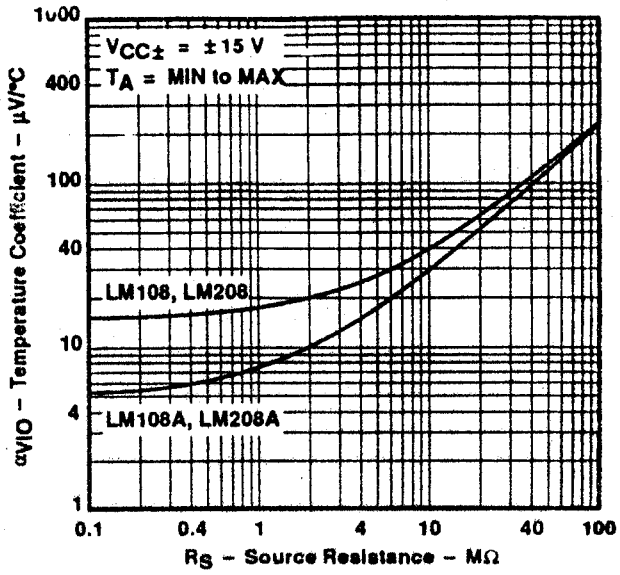


Figure 2

LM108, LM108A, LM208, LM208A
INPUT BIAS and OFFSET CURRENTS
vs
FREE-AIR TEMPERATURE

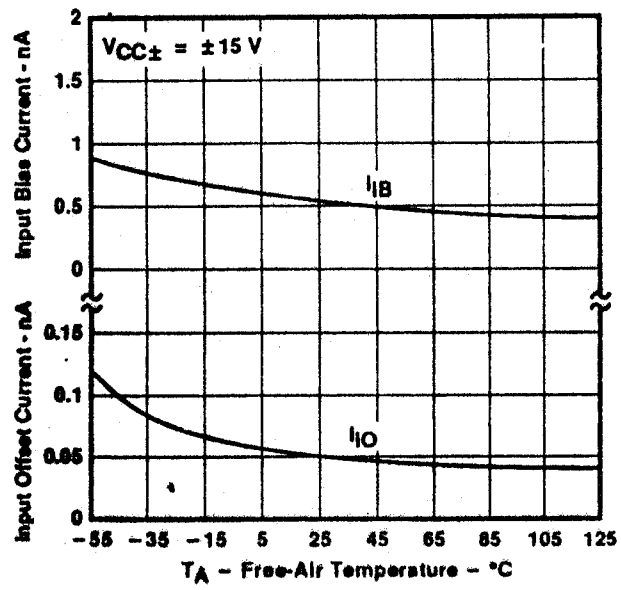


Figure 3

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

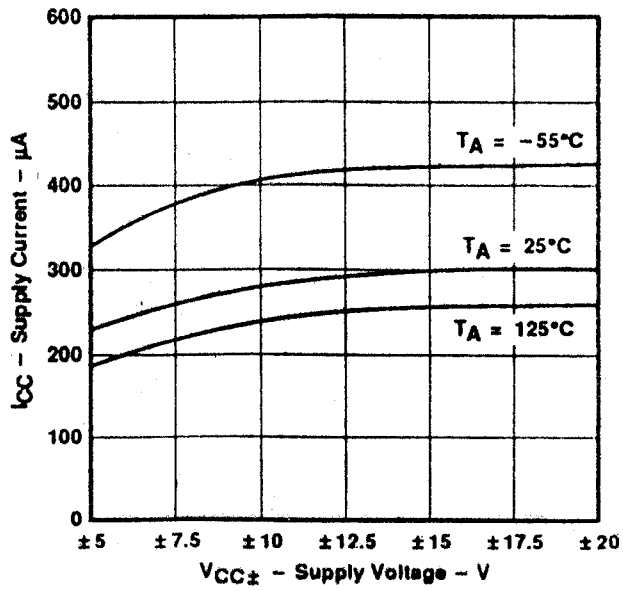


Figure 4

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE SWING
vs
FREQUENCY

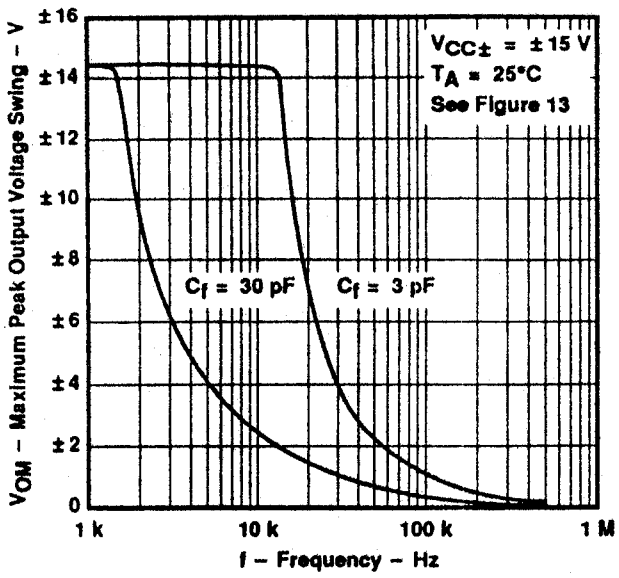


Figure 5

MAXIMUM PEAK OUTPUT VOLTAGE SWING
vs
OUTPUT CURRENT

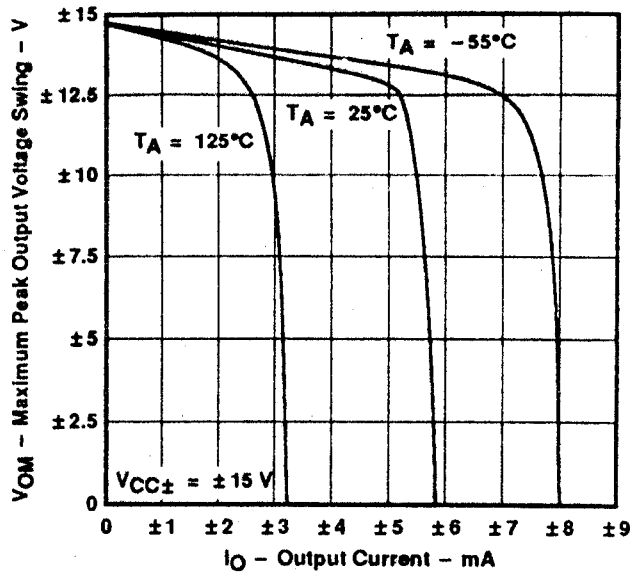


Figure 6

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

Figure 7

DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE DELAY
vs
FREQUENCY

Figure 8

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices

TYPICAL CHARACTERISTICS

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

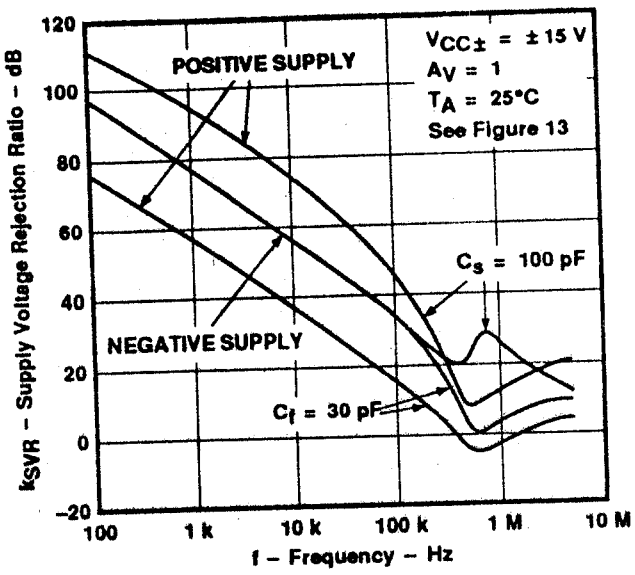


Figure 9

CLOSED-LOOP OUTPUT IMPEDANCE
vs
FREQUENCY

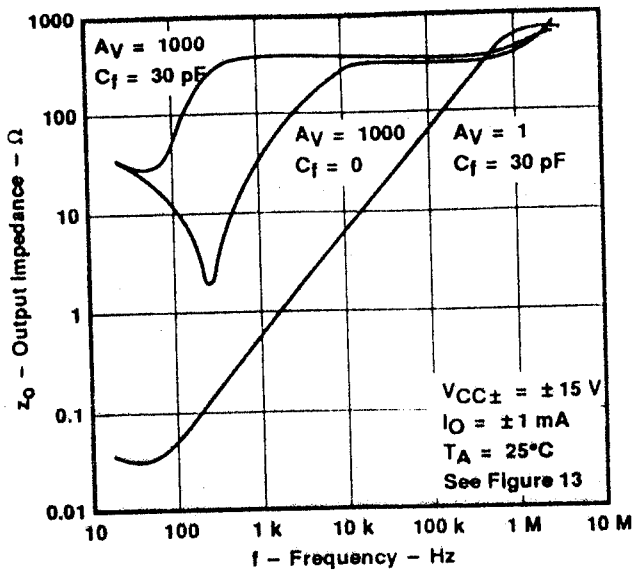


Figure 10

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

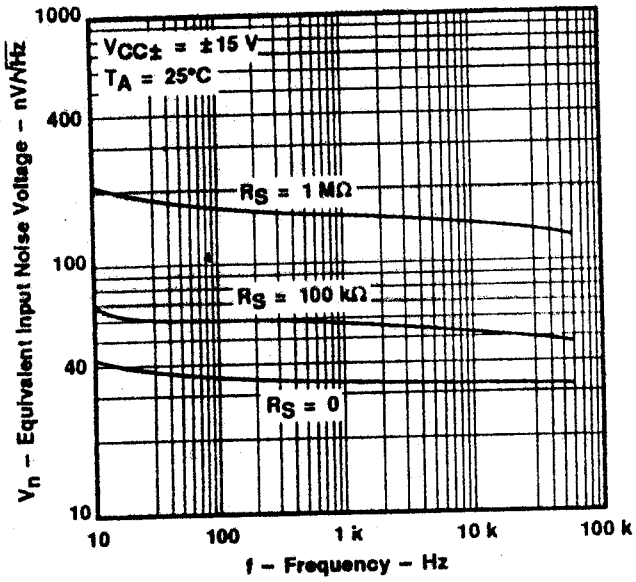


Figure 11

VOLTAGE FOLLOWER
PULSE RESPONSE

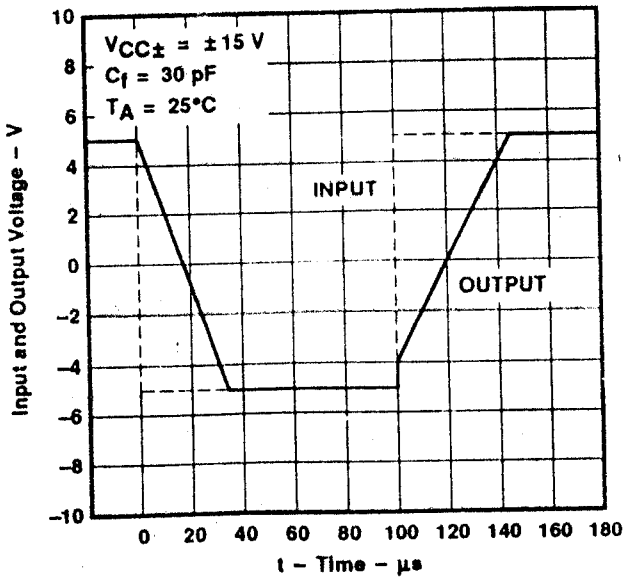
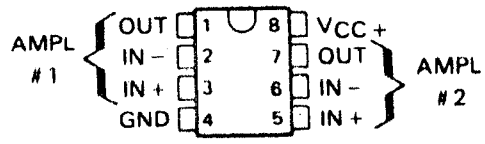


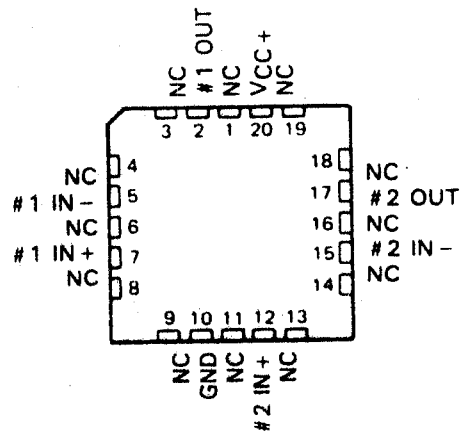
Figure 12

- **Wide Range of Supply Voltages:**
  Single Supply . . . 3 V to 30 V
  (LM2904 and LM2904Q
  3 V to 26 V) or Dual Supplies
- **Low Supply Current Drain Independent of Supply Voltage . . . 0.7 mA Typ**
- **Common-Mode Input Voltage Range Includes Ground Allowing Direct Sensing Near Ground**
- **Low Input Bias and Offset Parameters:**
  Input Offset Voltage . . . 3 mV Typ
  A Versions . . . 2 mV Typ
  Input Offset Current . . . 2 nA Typ
  Input Bias Current . . . 20 nA Typ
  A Versions . . . 15 nA Typ
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±32 V**
  (±26 V for LM2904 and LM2904Q)
- **Open-Loop Differential Voltage Amplification . . . 100 V/mV Typ**
- **Internal Frequency Compensation**

D, DB, JG, P, OR PW PACKAGE
(TOP VIEW)



LM158, LM158A
FK PACKAGE
(TOP VIEW)

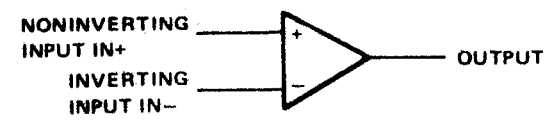


NC – No internal connection

description

These devices consist of two independent, high-gain, frequency-compensated operational amplifiers that were designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies is also possible so long as the difference between the two supplies is 3 V to 30 V (3 V to 26 V for the LM2904 and LM2904Q), and the V_{CC} pin is at least 1.5 V more positive than the input common-mode voltage. The low supply current drain is independent of the magnitude of the supply voltage.

symbol (each amplifier)



Applications include transducer amplifiers, d-c amplification blocks, and all the conventional operational amplifier circuits that now can be more easily implemented in single-supply-voltage systems. For example, these devices can be operated directly off of the standard 5-V supply that is used in digital systems and will easily provide the required interface electronics without requiring additional ±15-V supplies.

The LM158 and LM158A are characterized for operation over the full military temperature range of −55°C to 125°C. The LM258 and LM258A are characterized for operation from −25°C to 85°C, the LM358 and LM358A from 0°C to 70°C, and the LM2904 and LM2904Q from −40°C to 105°C.

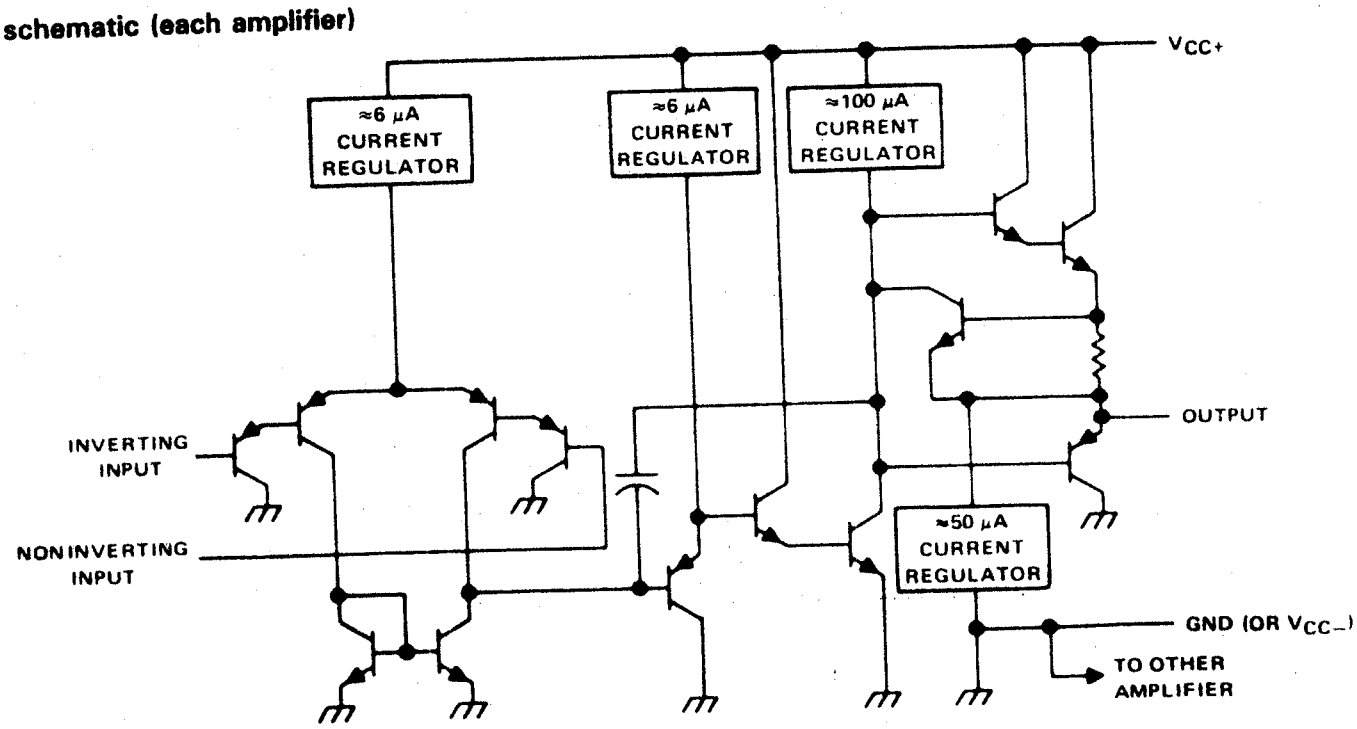
The LM2904Q is manufactured to demanding automotive requirements.

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE						
		SMALL OUTLINE (D)	SSOP (DB)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	CHIP FORM (Y)
0°C to 70°C	7 mV	LM358D	LM358DB			LM358P	LM358PW	LM358Y
	3 mV					LM358AP		
−25°C to 85°C	5 mV	LM258D				LM258P		
	3 mV					LM258AP		
−40°C to 105°C	7 mV	LM2904D	LM2904DB			LM2904P	LM2904PW	
	7 mV	LM2904QD				LM2904QP		
−55°C to 125°C	5 mV	LM158D		LM158FK	LM158JG	LM158P		
	2 mV			LM158AFK	LM158AJG			

The D package is available taped and reeled. Add the suffix R (e.g., LM358DR).
The DB and PW packages are only available left-end taped and reeled. Add the suffix LE (e.g., LM358DBLE).

schematic (each amplifier)



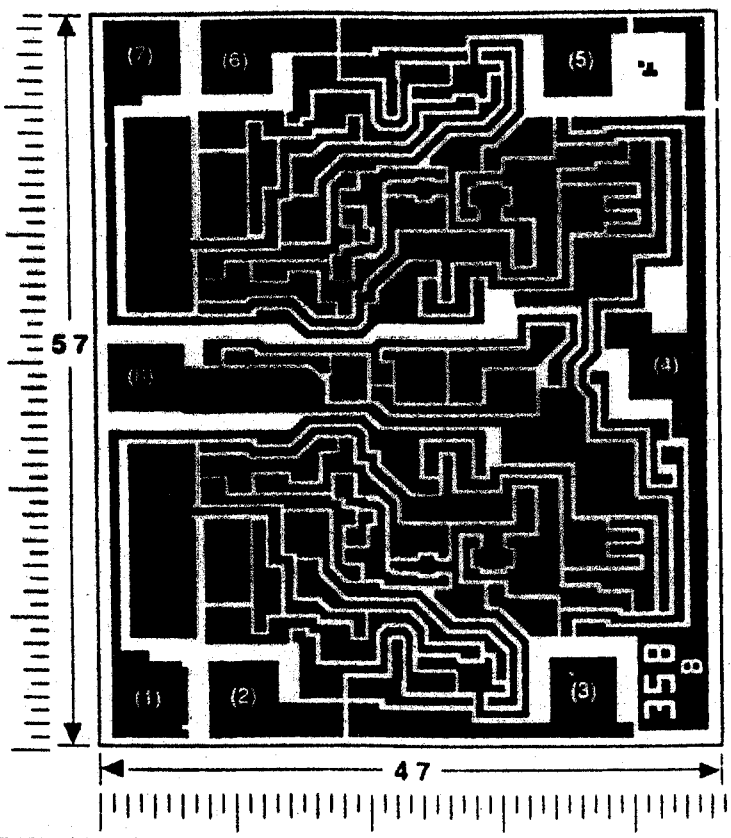
Component count (total device)

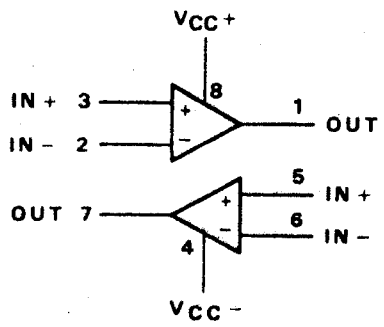
Epi-FET – 1
Diodes – 2
Resistors – 7
Transistors – 51
Capacitors – 2

chip information

These chips, properly assembled, display characteristics similar to the LM358. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 X 4 MINIMUM

T_J max = 150°C

TOLERANCES ARE ± 10%

ALL DIMENSIONS ARE IN MILS

NO BACKSIDE METALIZATION

PIN (4) INTERNALLY CONNECTED TO BACKSIDE OF CHIP

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM158, LM158A LM258, LM258A LM358, LM358A	LM2904, LM2904Q	UNIT
Supply voltage, V_{CC} (see Note 1)		32	26	V
Differential voltage (see Note 2)		± 32	± 26	V
Input voltage range (either input)		0.3 to 32	0.3 to 26	V
Duration of output short-circuit (one amplifier) to ground at (or below) 25°C free-air temperature (V_{CC} ≤ 15 V) (see Note 3)		unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table		
Operating free-air temperature range	LM158, LM158A	−55 to 125		°C
	LM258, LM258A	−25 to 85		
	LM358, LM358A	0 to 70		
	LM2904, LM2904Q		−40 to 105	
Storage temperature range		−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, DB, P, or PW package	260	260	°C

NOTES: 1. All voltage values, except differential voltages, and V_{CC} specified for measurement of I_{OS}, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
DB	525 mW	4.2 mW°C	336 mW	273 mW	
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW
PW	525 mW	4.2 mW/°C	336 mW	273 mW	

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

DECEMBER 1983 - REVISED MARCH 1988

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

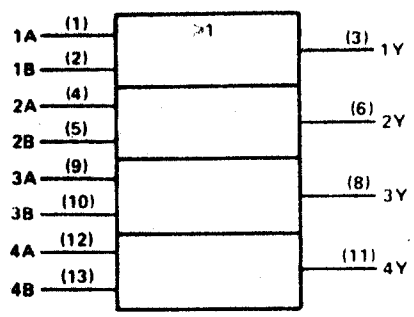
These devices contain four independent 2-input OR gates.

The SN5432, SN54LS32 and SN54S32 are characterized for operation over the full military range of −55°C to 125°C. The SN7432, SN74LS32 and SN74S32 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

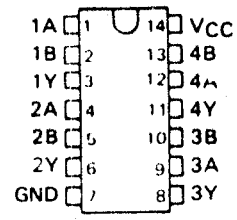
INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol†

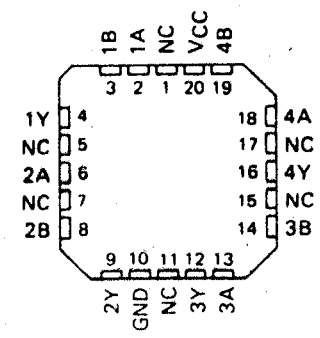


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, or W packages.

SN5432, SN54LS32, SN54S32 . . . J OR W PACKAGE
SN7432 . . . N PACKAGE
SN74LS32, SN74S32 . . . D OR N PACKAGE
(TOP VIEW)

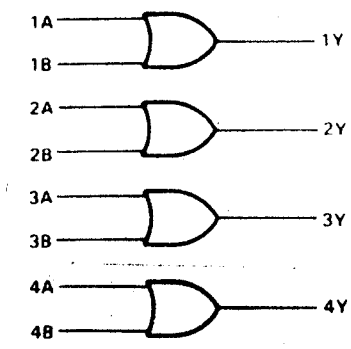


SN54LS32, SN54S32 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram

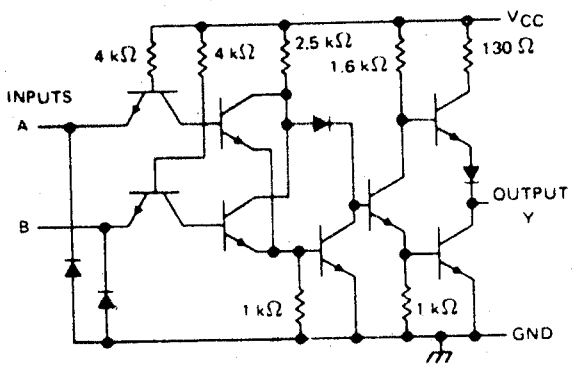


positive logic

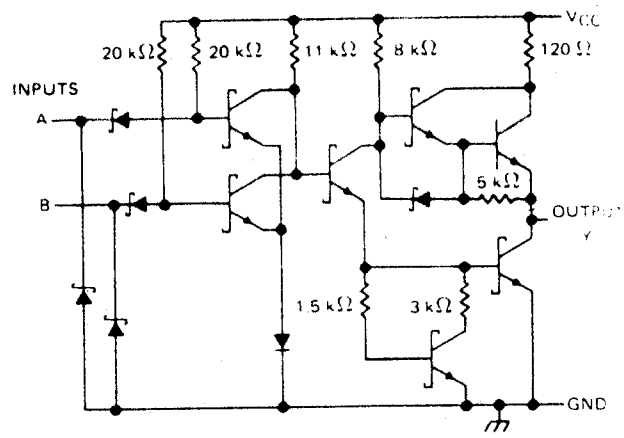
$Y = A + B$ or $Y = \overline{\overline{A} \cdot \overline{B}}$

schematics (each gate)

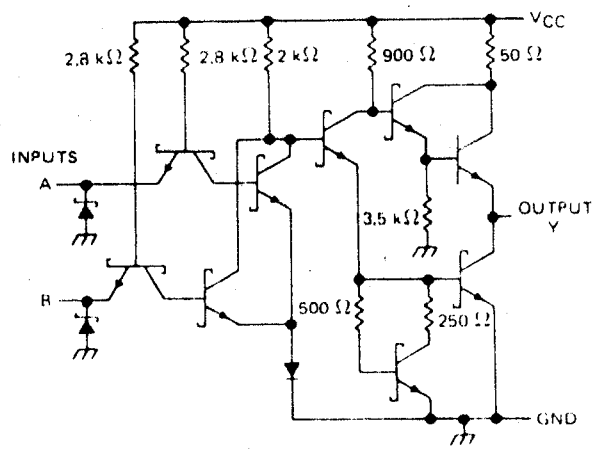
'32



'LS32



'S32



Resistor values shown are nominal

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage: '32, 'S32		5.5 V
'LS32		7 V
Operating free-air temperature:	SN54'	−55°C to 125°C
	SN74'	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal

recommended operating conditions

		SN5432			SN7432			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			0.8			−0.8	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			SN5432			SN7432			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −12 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OH} = −0.8 mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IL} = 0.8 V,	I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.4 V				40			40	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				−1.6			−1.6	mA
I_{OS}§	V_{CC} = MAX			−20		−55	−18		−55	mA
I_{CCH}	V_{CC} = MAX,	See Note 2			15	22		15	22	mA
I_{CCL}	V_{CC} = MAX,	V_I = 0 V			23	38		23	38	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time
NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 400 Ω,	C_L = 15 pF		10	15	ns
t_{PHL}						14	22	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54LS32			SN74LS32			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS32			SN74LS32			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN, V_{IL} = MAX, I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = MIN, V_{IL} = MAX, I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = MAX, V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX	−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX, See Note 2		3.1	6.2		3.1	6.2	mA
I_{CCL}	V_{CC} = MAX, V_I = 0 V		4.9	9.8		4.9	9.8	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 2 kΩ, C_L = 15 pF		14	22	ns
t_{PHL}					14	22	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54S32			SN74S32			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †			SN54S32			SN74S32			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IL} = 0.8 V,	I_{OL} = 20 mA			0.5			0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				50			50	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V				−2			−2	mA
I_{OS}§	V_{CC} = MAX			−40		−100	−40		−100	mA
I_{CCH}	V_{CC} = MAX,	See Note 2			18	32		18	32	mA
I_{CCL}	V_{CC} = MAX,	V_I = 0 V			38	68		38	68	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.
NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 280 Ω, C_L = 15 pF		4	7	ns
t_{PHL}					4	7	ns
t_{PLH}	A or B	Y	R_L = 280 Ω, C_L = 50 pF		5		ns
t_{PHL}					5		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982 – REVISED SEPTEMBER 1987

- **High-Current 3-State Outputs Interface Directly with System Bus or Can Drive Up to 15 LSTTL Loads**
- **Gated Output-Control Lines for Enabling or Disabling the Outputs**
- **Fully Independent Clock Virtually Eliminates Restrictions for Operating in One of Two Modes**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

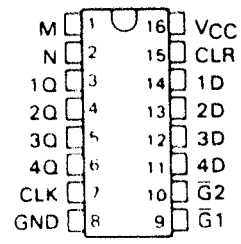
description

The 'HC173 4-bit registers include D-type flip-flops featuring totem-pole 3-state outputs capable of driving highly capacitive or relatively low-impedance loads. The high-impedence third state and increased drive provide these flip-flops with the capability of being connected directly to and driving the lines in a bus-organized system without need for interface or pull-up components.

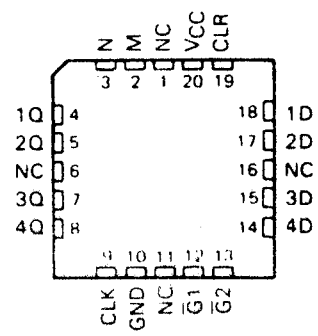
Gated enable inputs are provided on these devices for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the clock input. Gate output control inputs are also provided. When both are low, the normal logic states (high or low levels) of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output-control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

The SN54HC173 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC173 is characterized for operation from −40°C to 85°C.

SN54HC173 . . . J PACKAGE
SN74HC173 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC173 . . . FK PACKAGE
(TOP VIEW)



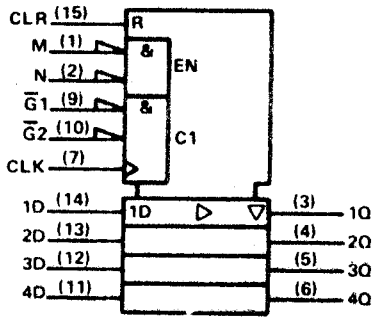
NC – No internal connection

FUNCTION TABLE

INPUTS					OUTPUT
CLEAR	CLOCK	DATA ENABLE		DATA	
		$\overline{G}1$	$\overline{G}2$	D	Q_A
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

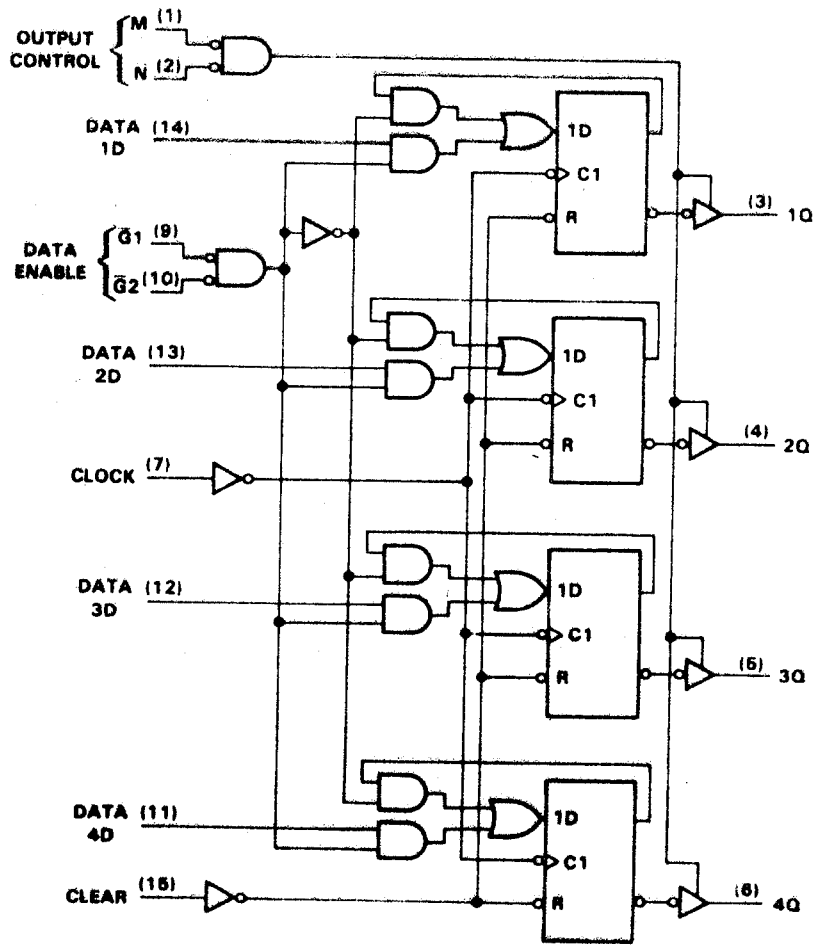
When either M or N (or both) is (are) high, the output is disabled to the high impedence state; however, sequential operation of the flip flops is not affected.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK}(V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK}(V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC173			SN74HC173			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC173		SN74HC173		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC173		SN74HC173		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock} Input clock frequency		2 V	0	6	0	4.2	0	5	MHz
		4.5 V	0	31	0	21	0	25	
		6 V	0	36	0	25	0	29	
t_w Pulse duration	CLK high or low	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
	CLR high	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su} Setup time before CLK↑	$\overline{G}1$ and $\overline{G}2$	2 V	100		150		125		ns
		4.5 V	20		30		25		
		6 V	17		25		21		
	Data	2 V	100		150		125		ns
		4.5 V	20		30		25		
		6 V	17		25		21		
	CLR inactive	2 V	90		135		115		ns
		4.5 V	18		27		23		
		6 V	15		23		19		
t_h Hold time after CLK↑	$\overline{G}1$ and $\overline{G}2$	2 V	0		0		0		
		4.5 V	0		0		0		
		6 V	0		0		0		
	Data	2 V	0		0		0		ns
		4.5 V	0		0		0		
		6 V	0		0		0		

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC173		SN74HC173		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	8		4.2		5		MHz
			4.5 V	31	46		21		25		
			6 V	36	55		25		29		
t_{PHL}	CLR	Any	2 V		78	150		225		190	ns
			4.5 V		21	30		45		38	
			6 V		20	26		38		32	
t_{pd}	CLK	Any	2 V		78	150		225		190	ns
			4.5 V		21	30		45		38	
			6 V		20	26		38		32	
t_{en}	M or N	Any	2 V		78	150		225		190	ns
			4.5 V		20	30		45		38	
			6 V		15	26		38		32	
t_{dis}	M or N	Any	2 V		40	150		225		190	ns
			4.5 V		18	30		45		38	
			6 V		16	26		38		32	
t_t		Any	2 V		20	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	29 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

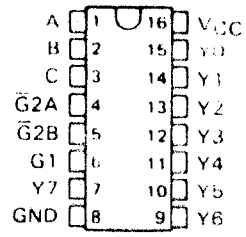
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC173		SN74HC173		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PHL}	CLR	Any	2 V		100	200		300		250	ns
			4.5 V		28	40		60		50	
			6 V		21	34		51		43	
t_{pd}	CLR	Any	2 V		100	200		300		250	ns
			4.5 V		28	40		60		50	
			6 V		21	34		51		43	
t_{en}	M or N	Any	2 V		100	200		300		250	ns
			4.5 V		28	40		60		50	
			6 V		21	34		51		43	
t_t		Any	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1

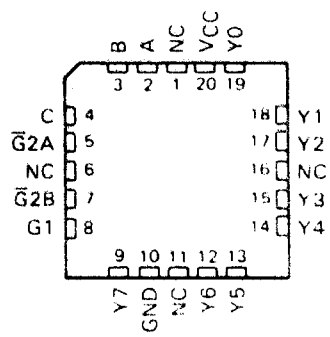
D2804, MARCH 1984 – REVISED JUNE 1989

- **Inputs are TTL-Voltage Compatible**
- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporates 3 Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HCT238 . . . J PACKAGE
SN74HCT238 . . . D† OR N PACKAGE
(TOP VIEW)



SN54HCT238 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

† Contact the factory for D availability.

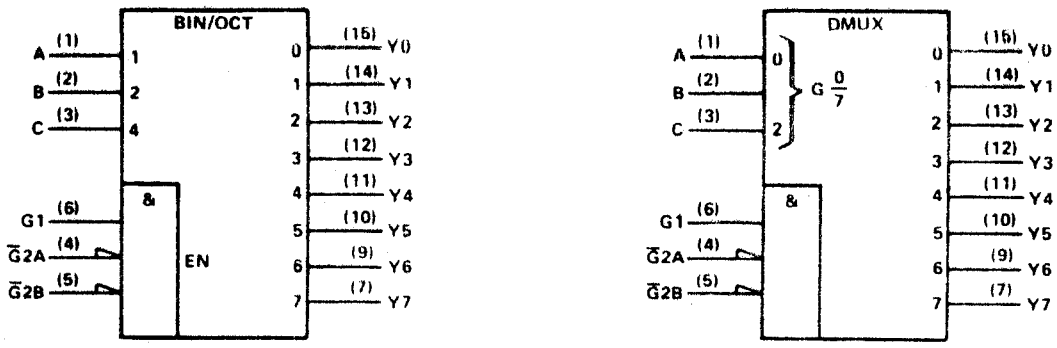
description

The 'HCT238 circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems this decoder can be used to minimize the effects of systems decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

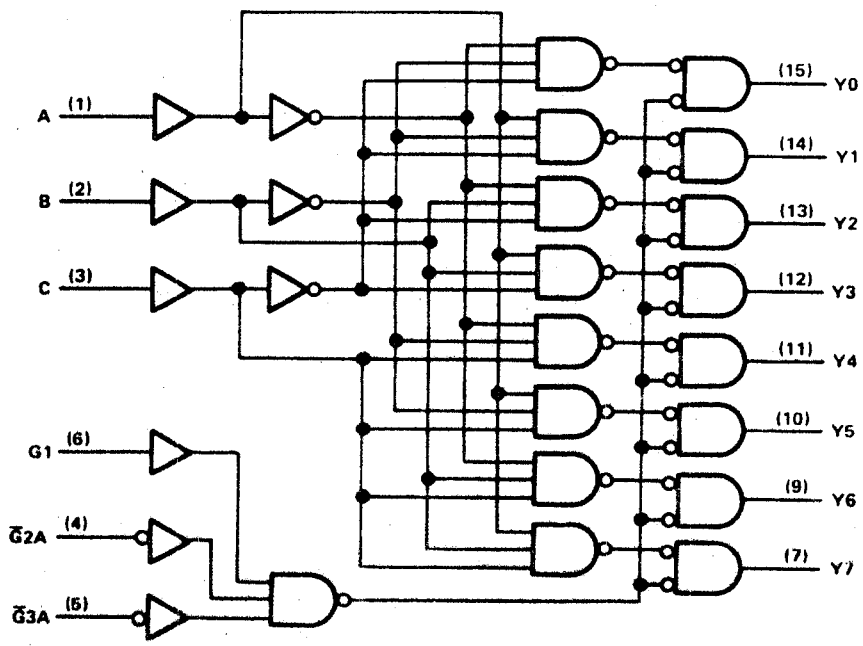
The SN54HCT238 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT238 is characterized for operation from −40°C to 85°C.

logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

TEXAS INSTRUMENTS
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FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	L	H	H	L	L	L	H	L	L	L	L
H	L	L	H	L	L	L	L	L	L	H	L	L	L
H	L	L	H	L	H	L	L	L	L	L	H	L	L
H	L	L	H	H	L	L	L	L	L	L	L	H	L
H	L	L	H	H	H	L	L	L	L	L	L	L	H

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HCT238			SN74HCT238			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT238		SN74HCT238		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}†	One input at 0.5 V or 2.4 V, Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3		2.9	mA
C_i		4.5 to 5.5 V		3	10		10		10	pF

†This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT238		SN74HCT238		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	Any	4.5 V		21	36		54		45	ns
			5.5 V		18	32		49		41	
t_{pd}	Enable	Any	4.5 V		21	33		50		42	
			5.5 V		17	30		45		38	
t_t		Any	4.5 V		11	15		22		19	ns
			5.5 V		9	14		20		17	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	85 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2804, MARCH 1984 – REVISED JUNE 1989

- **Inputs are TTL-Voltage Compatible**
- **High-Current 3-State Outputs Drive Bus Lines Directly or Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

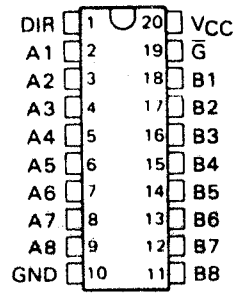
The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

The SN54HCT245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT245 is characterized for operation from −40°C to 85°C.

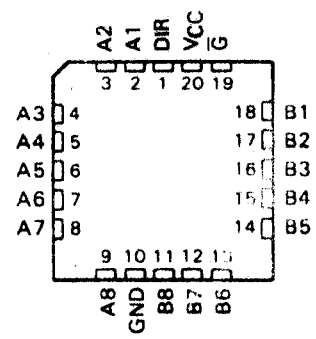
FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

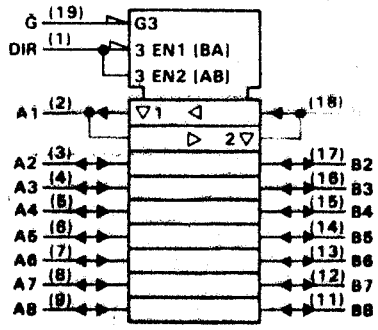
SN54HCT245 . . . J PACKAGE
SN74HCT245 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT245 . . . FK PACKAGE
(TOP VIEW)

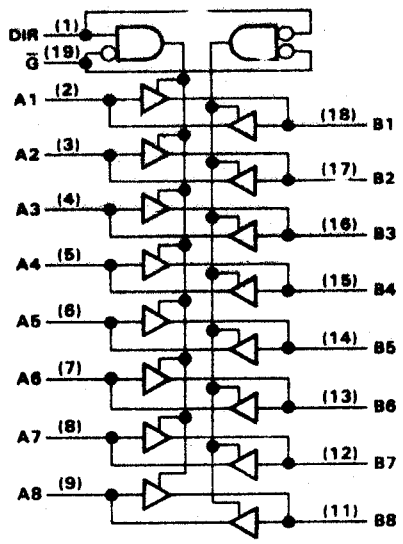


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HCT245			SN74HCT245			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT245		SN74HCT245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OL} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I DIR or $\overline{G}$	V_I = V_{CC} or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ} A or B	V_O = V_{CC} or 0	5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}†	One input at 0.5 V or 2.4 V Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3		2.9	mA
C_i DIR or $\overline{G}$‡		4.5 to 5.5 V		3	10		10		10	pF

†This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.
‡This parameter C_i does not apply to transceiver I/O ports.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT245		SN74HCT245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		16	22		33		28	ns
			5.5 V		14	20		30		25	
t_{en}	$\overline{G}$	A or B	4.5 V		25	46		69		58	ns
			5.5 V		22	41		62		52	
t_{dis}	$\overline{G}$	A or B	4.5 V		26	40		60		50	ns
			5.5 V		23	36		54		45	
t_t		A or B	4.5 V		9	12		18		15	ns
			5.5 V		8	11		16		14	

C_{pd}	Power dissipation capacitance per transceiver	No load, T_A = 25°C	40 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT245		SN74HCT245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		20	30		45		38	ns
			5.5 V		18	27		41		34	
t_{en}	$\overline{G}$	A or B	4.5 V		36	59		89		74	ns
			5.5 V		3^	53		80		67	
t_t		A or B	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

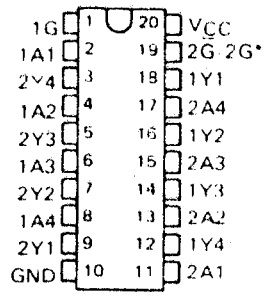
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244, SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

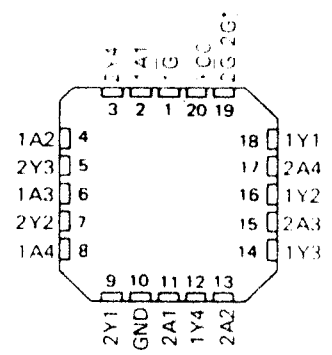
APRIL 1985 - REVISED MARCH 1988

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **PNP Inputs Reduce D-C Loading**
- **Hysteresis at Inputs Improves Noise Margins**

SN54LS', SN54S' . . . J OR W PACKAGE
SN74LS', SN74S' . . . DW OR N PACKAGE
(TOP VIEW)



SN54LS', SN54S' . . . FK PACKAGE
(TOP VIEW)



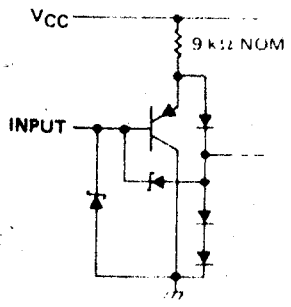
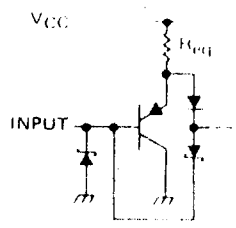
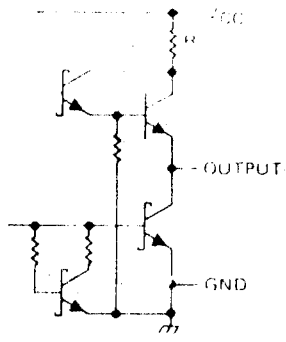
*2G for 'LS241 and 'S241 or 2G for all other drivers

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out, improved fan-in, and 400 mV noise margin. The SN74LS' and SN74S' can be used to drive terminated lines down to 133 ohms.

The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

'LS240, 'LS241, 'LS244	'S240, 'S241, 'S244	
EQUIVALENT OF EACH INPUT	EQUIVALENT OF EACH INPUT	TYPICAL OF ALL OUTPUTS
	 G and $\overline{G}$ inputs R_{eq} = 2 kΩ NOM A inputs R_{eq} = 28 kΩ NOM	 'LS240, 'LS241, 'LS244 R = 60 Ω NOM 'S240, 'S241, 'S244 R = 25 Ω NOM

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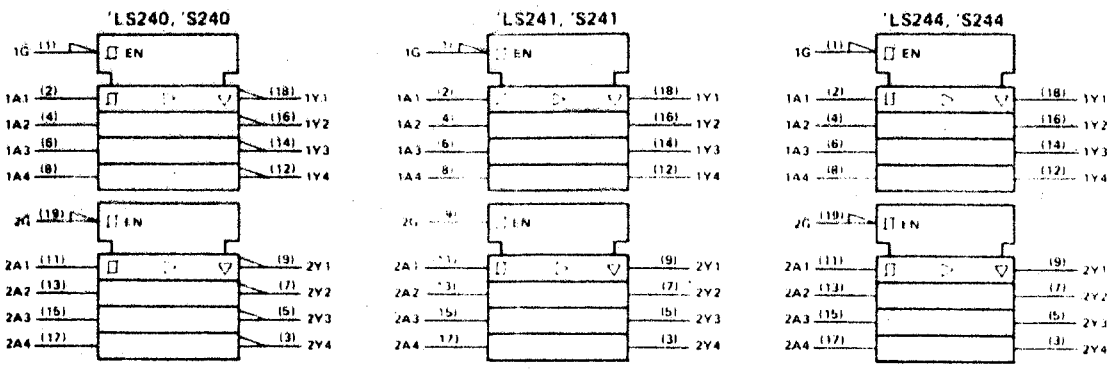
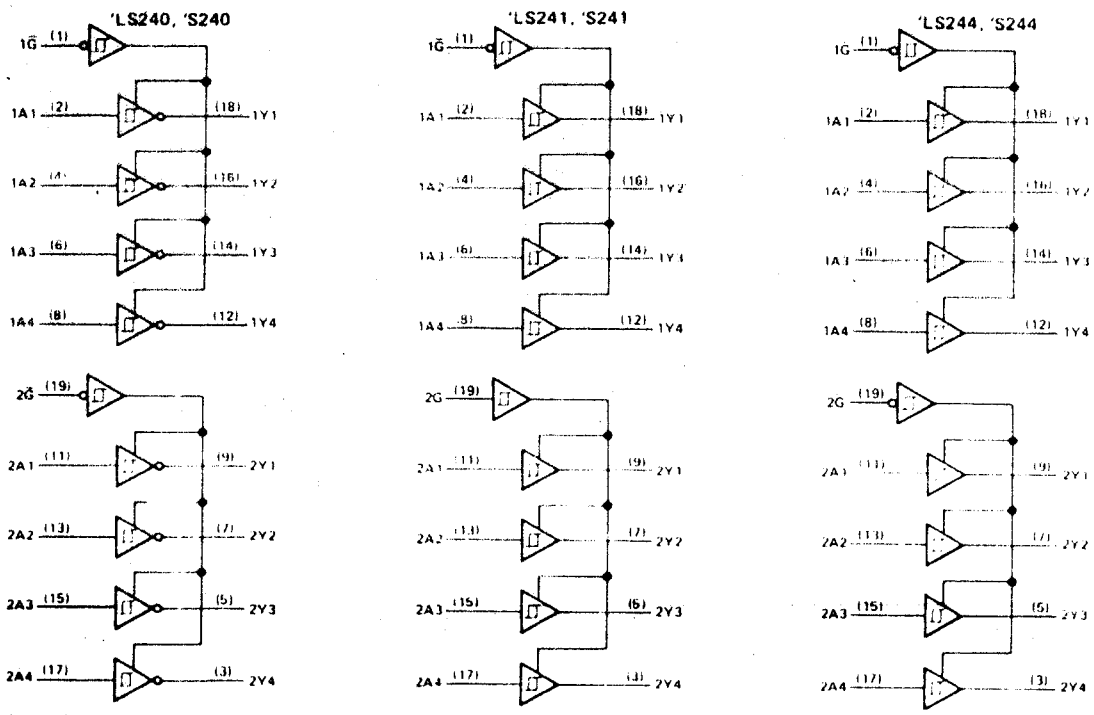
logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



Pin numbers shown are for DW, J, N, and W packages

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage: 'LS Circuits		7 V
'S Circuits		5.5 V
Off-state output voltage		5.5 V
Operating free-air temperature range	SN54LS', SN54S' Circuits	55°C to 125°C
	SN74LS', SN74S' Circuits	0°C to 70°C
Storage temperature range		65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal

recommended operating conditions

PARAMETER		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA					−1.5			1.5	V
Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = MIN			0.2	0.4		0.2	0.4		V
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX, I_{OH} = −3 mA			2.4	3.4		2.4	3.4		V
		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.5 V, I_{OH} = MAX			2			2			
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OL} = 12 mA				0.4			0.4	V
			I_{OL} = 24 mA							0.5	
I_{OZH}		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = MAX	V_O = 2.7 V				20			20	μA
I_{OZL}			V_O = 0.4 V				−20			−20	
I_I		V_{CC} = MAX, V_I = 7 V					0.1			0.1	mA
I_{IH}		V_{CC} = MAX, V_I = 2.7 V					20			20	μA
I_{IL}		V_{CC} = MAX, V_{IL} = 0.4 V					−0.2			−0.2	mA
I_{OS}§		V_{CC} = MAX			−40		−225	−40		−225	mA
I_{CC}	Outputs high	V_{CC} = MAX, Output open		All		17	27		17	27	mA
	Outputs low			'LS240		26	44		26	44	
				'LS241, 'LS244		27	46		27	46	
	All outputs disabled			'LS240		29	50		29	50	
				'LS241, 'LS244		32	54		32	54	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		'LS240			'LS241, 'LS244			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	R_L = 667 Ω, See Note 2	C_L = 45 pF,		9	14		12	18	ns
t_{PHL}				12	18		12	18	ns
t_{PZL}				20	30		20	30	ns
t_{PZH}				15	23		15	23	ns
t_{PLZ}	R_L = 667 Ω, See Note 2	C_L = 5 pF,		10	20		10	20	ns
t_{PHZ}				15	25		15	25	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

	PARAMETER	SN54S' MIN	SN54S' NOM	SN54S' MAX	SN74S' MIN	SN74S' NOM	SN74S' MAX	UNIT
V_{CC}	Supply voltage, (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
	External resistance between any input and V_{CC} or ground			40			40	kΩ
T_A	Operating free-air temperature (see Note 3)	−55		125	0		70	°C

NOTES 1. Voltage values are with respect to network ground terminal.
3. An SN54S241 operating at free-air temperature above 116 °C requires a heat sink that provides a thermal resistance from case to free-air $R_{\theta CA}$ of not more than 40 °C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

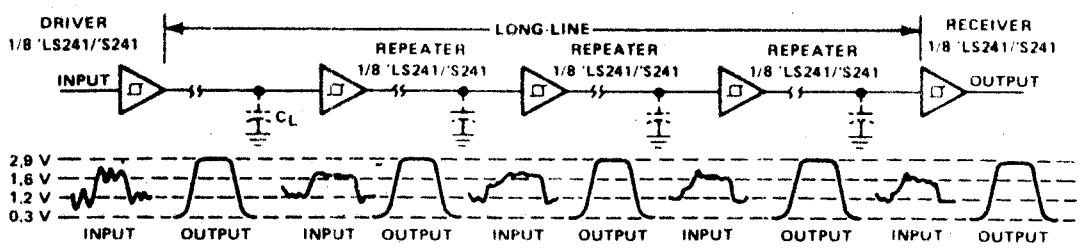
PARAMETER		TEST CONDITIONS†			SN54S' MIN	SN54S' TYP‡	SN54S' MAX	SN74S' MIN	SN74S' TYP‡	SN74S' MAX	UNIT
V_{IK}		V_{CC} = MIN, I_I = −18 mA					−1.2			−1.2	V
Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = MIN			0.2	0.4		0.2	0.4		V
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA						2.7			V
		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −3 mA			2.4	3.4		2.4	3.4		
		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.5 V, I_{OH} = MAX			2			2			
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX					0.55			0.55	V
I_{OZH}		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V,	V_O = 2.4 V				50			50	μA
I_{OZL}			V_O = 0.5 V				−50			−50	
I_I		V_{CC} = MAX, V_I = 5.5 V					1			1	mA
I_{IH}		V_{CC} = MAX, V_I = 2.7 V					50			50	μA
I_{IL}	Any A	V_{CC} = MAX, V_I = 0.5 V					−400			−400	μA
	Any G						−2			−2	mA
I_{OS}§		V_{CC} = MAX			−50		−225	−50		−225	mA
I_{CC}	Outputs high	V_{CC} = MAX, Outputs open		'S240		80	123		80	135	mA
				'S241, 'S244		95	147		95	160	
	Outputs low			'S240		100	145		100	150	
				'S241, 'S244		120	170		120	180	
	Outputs disabled			'S240		100	145		100	150	
				'S241, 'S244		120	170		120	180	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

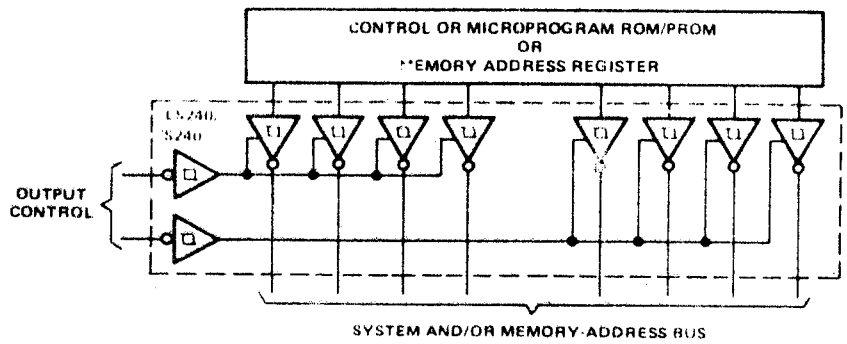
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		'S240			'S241, 'S244			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	R_L = 90 Ω, See Note 4	C_L = 50 pF,		4.5	7		6	9	ns
t_{PHL}				4.5	7		6	9	ns
t_{PZL}				10	15		10	15	ns
t_{PZH}				6.5	10		8	12	ns
t_{PLZ}	R_L = 90 Ω, See Note 4	C_L = 5 pF,		10	15		10	15	ns
t_{PHZ}				6	9		6	9	ns

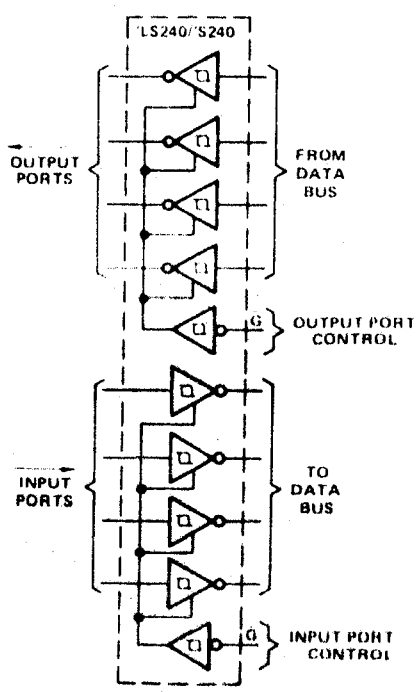
NOTE 4: Load circuits and voltage waveforms are shown in Section 1.



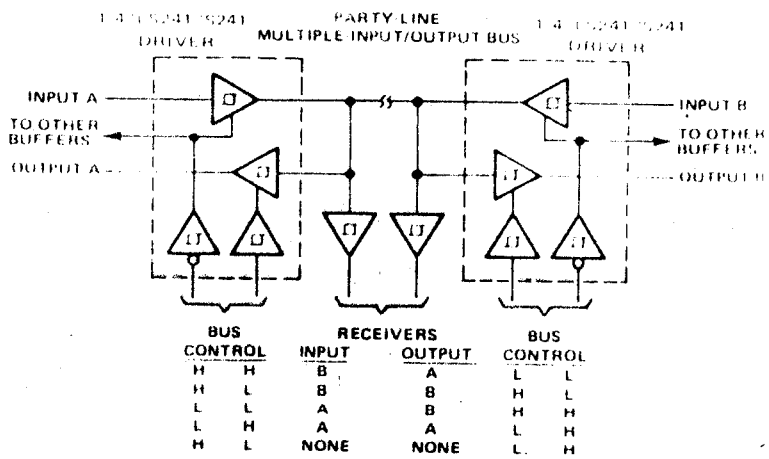
'LS241, 'S241 USED AS REPEATER/LEVEL RESTORER



'LS240, 'S240 USED AS SYSTEM AND/OR MEMORY BUS DRIVER. 4-BIT ORGANIZATION CAN BE APPLIED TO HANDLE BINARY OR BCD



INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS
IN A SINGLE PACKAGE



BUS CONTROL		RECEIVERS INPUT	OUTPUT	BUS CONTROL	
H	H	B	A	L	L
H	L	B	B	H	L
L	L	A	B	H	H
L	H	A	A	L	H
H	L	NONE	NONE	L	H

PARTY-LINE BUS SYSTEM
WITH MULTIPLE INPUTS, OUTPUTS, AND RECEIVERS

TEXAS INSTRUMENTS
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OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

OCTOBER 1975 · REVISED MARCH 1988

- **Choice of 8 Latches or 8 D-Type Flip-Flops In a Single Package**
- **3-State Bus-Driving Outputs**
- **Full Parallel-Access for Loading**
- **Buffered Control Inputs**
- **Clock/Enable Input Has Hysteresis to Improve Noise Rejection ('S373 and 'S374)**
- **P-N-P Inputs Reduce D-C Loading on Data Lines ('S373 and 'S374)**

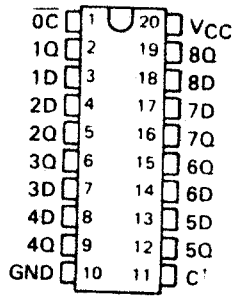
'LS373, 'S373
FUNCTION TABLE

OUTPUT ENABLE	ENABLE LATCH	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

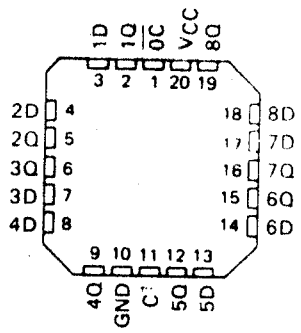
'LS374, 'S374
FUNCTION TABLE

OUTPUT ENABLE	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

SN54LS373, SN54LS374, SN54S373, SN54S374 . . . J OR W PACKAGE
SN74LS373, SN74LS374, SN74S373, SN74S374 . . . DW OR N PACKAGE
(TOP VIEW)



SN54LS373, SN54LS374, SN54S373, SN54S374 . . . FK PACKAGE
(TOP VIEW)



'C for 'LS373 and 'S373, CLK for 'LS374 and 'S374.

description

These 8-bit registers feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'LS373 and 'S373 are transparent D-type latches meaning that while the enable (C) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

2 TTL Devices

description (continued)

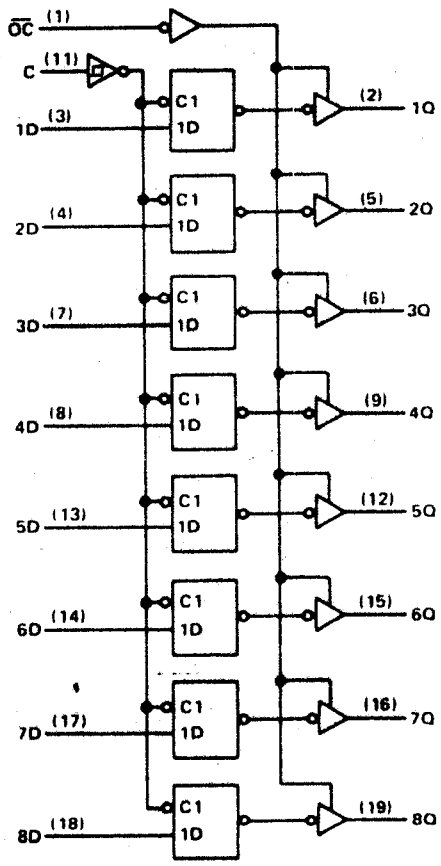
The eight flip-flops of the 'LS374 and 'S374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were setup at the D inputs.

Schmitt-trigger buffered inputs at the enable/clock lines of the 'S373 and 'S374 devices, simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

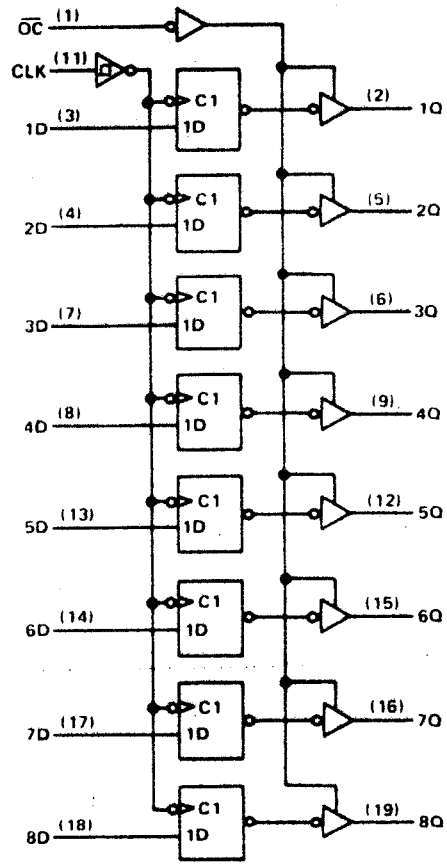
logic diagrams (positive logic)

'LS373, 'S373
TRANSPARENT LATCHES



for 'S373 only

'LS374, 'S374
POSITIVE-EDGE-TRIGGERED FLIP-FLOPS



for 'S374 only

Pin numbers shown are for DW, J, N, and W packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS' . . . . . −55°C to 125°C
SN74LS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54LS'			SN74LS'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{OH}	High-level output voltage				5.5			5.5	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Pulse duration	CLK high	15			15			ns
		CLK low	15			15			
t_{su}	Data setup time	'LS373	5↓			5↓			ns
		'LS374	20↑			20↑			
t_h	Data hold time	'LS373	20↓			20↓			ns
		'LS374↑	5↑			0↑			
T_A	Operating free-air temperature		−55		125	0		70	C

*The t_h specification applies only for data frequency below 10 MHz. Designs above 10 MHz should use a minimum of 5 ns. (Commercial only)

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max, I_{OH} = MAX		2.4	3.4		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.7 V				20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.4 V				−20			−20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX, Output control at 4.5 V	'LS373		24	40		24	40	mA
			'LS374		27	40		27	40	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

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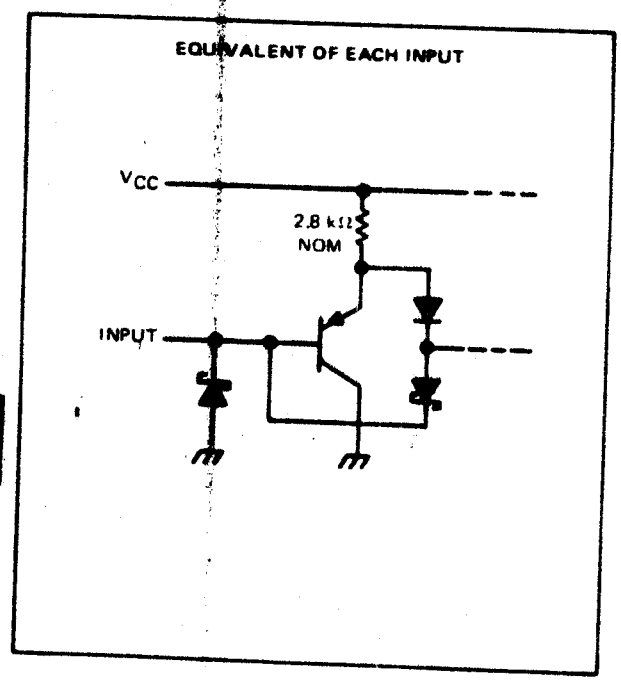
Switching characteristics, V_{CC} = 5 V, T_A = 25°C

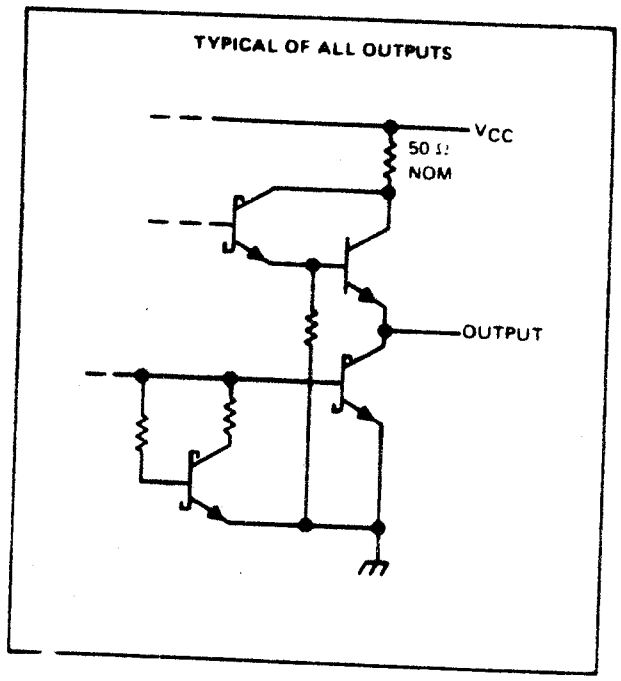
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS373			'LS374			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			C_L = 45 pF, R_L = 667 Ω, See Notes 2 and 3				35	50		MHz
t_{PLH}	Data	Any Q			12	18				ns
t_{PHL}					12	18				
t_{PLH}	Clock or enable	Any Q			20	30		15	28	ns
t_{PHL}					18	30		19	28	
t_{PZH}	Output Control	Any Q			15	28		20	26	ns
t_{PZL}					25	36		21	28	
t_{PHZ}	Output Control	Any Q	C_L = 5 pF, R_L = 667 Ω, See Note 3		15	25		15	28	ns
t_{PLZ}	Output Control	Any Q			12	20		12	20	ns

NOTES: 2. Maximum clock frequency is tested with all outputs loaded.
3. Load circuits and voltage waveforms are shown in Section 1.

f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{PZH} = output enable time to high level
t_{PZL} = output enable time to low level
t_{PHZ} = output disable time from high level
t_{PLZ} = output disable time from low level

schematic of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S' . . . . . −55°C to 125°C
SN74S' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S'			SN74S'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
High-level output current, I_{OH}				−2			−6.5	mA
Width of clock/enable pulse, t_w	High	6			6			ns
	Low	7.3			7.3			
Data setup time, t_{su}	'S373	0↓			0↓			ns
	'S374	5↑			5↑			
Data hold time, t_h	'S373	10↓			10↓			ns
	'S374	2↑			2↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

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intel

80186
HIGH INTEGRATION 16-BIT MICROPROCESSOR

- **Integrated Feature Set**
  - Enhanced 8086-2 CPU
  - Clock Generator
  - 2 Independent DMA Channels
  - Programmable Interrupt Controller
  - 3 Programmable 16-bit Timers
  - Programmable Memory and Peripheral Chip-Select Logic
  - Programmable Wait State Generator
  - Local Bus Controller
- **Available in 10 MHz (80186-10) and 8 MHz (80186) Versions**
- **High-Performance Processor**
  - 4 MByte/Sec Bus Bandwidth Interface @ 8 MHz
  - 5 MByte/Sec Bus Bandwidth Interface @ 10 MHz
- **Direct Addressing Capability to 1 MByte of Memory and 64 KByte I/O**
- **Completely Object Code Compatible with All Existing 8086, 8088 Software**
  - 10 New Instruction Types
- **Complete System Development Support**
  - Development Software: ASM 86 Assembler, PL/M-86, Pascal-86, Fortran-86, C-86, and System Utilities
  - In-Circuit-Emulator (I²ICE™-186)
- **Numerics Coprocessing Capability Through 8087 Interface**
- **Available in 68 Pin:**
  - Plastic Leaded Chip Carrier (PLCC)
  - Ceramic Pin Grid Array (PGA)
  - Ceramic Leadless Chip Carrier (LCC)

  (See Packaging Outlines and Dimensions, Order # 231369)
- **Available in EXPRESS**
  - Standard Temperature with Burn-In
  - Extended Temperature Range (−40°C to +85°C)

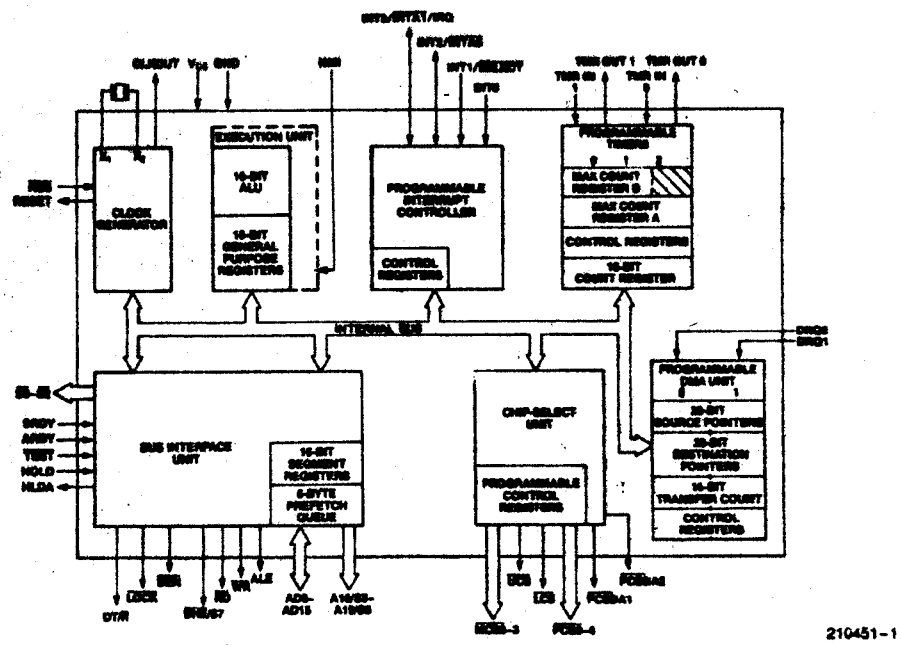
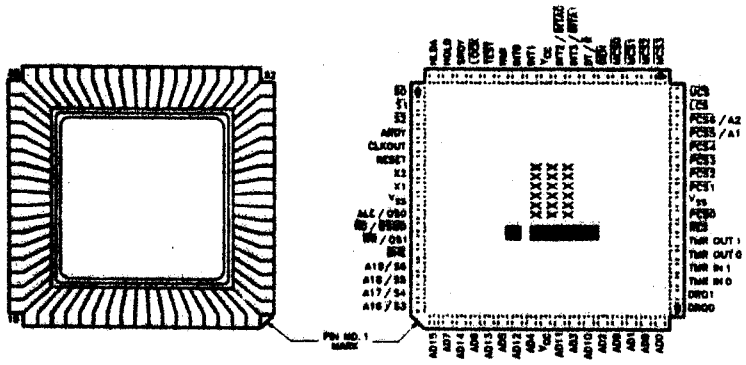


Figure 1. 80186 Block Diagram

The Intel 80186 is a highly integrated 16-bit microprocessor. The 80186 effectively combines 15–20 of the most common 8086 system components onto one. The 80186 provides two times greater throughput than the standard 5 MHz 8086. The 80186 is upward compatible with 8086 and 8088 software and adds 10 new instruction types to the existing set.

Ceramic Leadless Chip Carrier (JEDEC Type A)

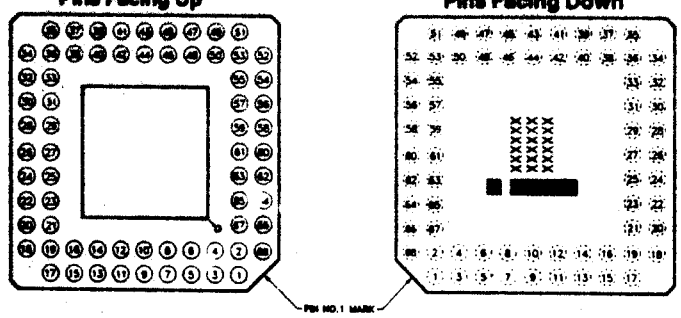
Contacts Facing Up **Contacts Facing Down**



210451-2

Ceramic Pin Grid Array

Pins Facing Up **Pins Facing Down**



210451-3

Plastic Leaded Chip Carrier

Leads Facing Up **Leads Facing Down**

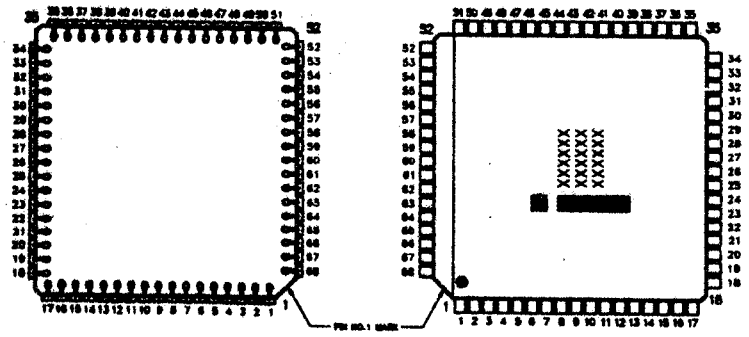


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Figure 2. 80186 Pinout Diagrams

Table 1. 80186 Pin Description

Symbol	Pin No.	Type	Name and Function
V_{CC}	9 43	I	**System Power:** +5 volt power supply.
V_{SS}	26 60	I	System Ground.
RESET	57	O	Reset Output indicates that the 80186 CPU is being reset, and can be used as a system reset. It is active HIGH, synchronized with the processor clock, and lasts an integer number of clock periods corresponding to the length of the $\overline{RES}$ signal.
X1 X2	59 58	I O	Crystal Inputs X1 and X2 provide external connections for a fundamental mode parallel resonant crystal for the internal oscillator. Instead of using a crystal, an external clock may be applied to X1 while minimizing stray capacitance on X2. The input or oscillator frequency is internally divided by two to generate the clock signal (CLKOUT).
CLKOUT	56	O	Clock Output provides the system with a 50% duty cycle waveform. All device pin timings are specified relative to CLKOUT.
$\overline{RES}$	24	I	An active $\overline{RES}$ causes the 80186 to immediately terminate its present activity, clear the internal logic, and enter a dormant state. This signal may be asynchronous to the 80186 clock. The 80186 begins fetching instructions approximately 6½ clock cycles after $\overline{RES}$ is returned HIGH. For proper initialization, V_{CC} must be within specifications and the clock signal must be stable for more than 4 clocks with $\overline{RES}$ held LOW. $\overline{RES}$ is internally synchronized. This input is provided with a Schmitt-trigger to facilitate power-on $\overline{RES}$ generation via an RC network.
$\overline{TEST}$	47	I/O	$\overline{TEST}$ is examined by the WAIT instruction. If the $\overline{TEST}$ input is HIGH when "WAIT" execution begins, instruction execution will suspend. $\overline{TEST}$ will be resampled until it goes LOW, at which time execution will resume. If interrupts are enabled while the 80186 is waiting for $\overline{TEST}$, interrupts will be serviced. During power-up, active $\overline{RES}$ is required to configure $\overline{TEST}$ as an input. This pin is synchronized internally.
TMR IN 0 TMR IN 1	20 21	I I	Timer Inputs are used either as clock or control signals, depending upon the programmed timer mode. These inputs are active HIGH (or LOW-to-HIGH transitions are counted) and internally synchronized.
TMR OUT 0 TMR OUT 1	22 23	O O	Timer outputs are used to provide single pulse or continous waveform generation, depending upon the timer mode selected.
DRQ0 DRQ1	18 19	I I	DMA Request is asserted HIGH by an external device when it is ready for DMA Channel 0 or 1 to perform a transfer. These signals are level-triggered and internally synchronized.
NMI	46	I	The Non-Maskable Interrupt input causes a Type 2 interrupt. An NMI transition from LOW to HIGH is latched and synchronized internally, and initiates the interrupt at the next instruction boundary. NMI must be asserted for at least one clock. The Non-Maskable Interrupt cannot be avoided by programming.
INT0 INT1/$\overline{SELECT}$ INT2/$\overline{INTA0}$ INT3/$\overline{INTA1}$/IRQ	45 44 42 41	I I I/O I/O	Maskable Interrupt Requests can be requested by activating one of these pins. When configured as inputs, these pins are active HIGH. Interrupt Requests are synchronized internally. INT2 and INT3 may be configured to provide active-LOW interrupt-acknowledge output signals. All interrupt inputs may be configured to be either edge- or level-triggered. To ensure recognition, all interrupt requests must remain active until the interrupt is acknowledged. When Slave Mode is selected, the function of these pins changes (see Interrupt Controller section of this data sheet).

Table 1. 80186 Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
$\overline{RD}$/QSMD	62	I/O	Read Strobe is an active LOW signal which indicates that the 80186 is performing a memory or I/O read cycle. It is guaranteed not to go LOW before the A/D bus is floated. An internal pull-up ensures that $\overline{RD}$ is HIGH during RESET. Following RESET the pin is sampled to determine whether the 80186 is to provide ALE, $\overline{RD}$, and $\overline{WR}$, or queue status information. To enable Queue Status Mode, $\overline{RD}$ must be connected to GND. $\overline{RD}$ will float during bus HOLD.
ARDY	55	I	Asynchronous Ready informs the 80186 that the addressed memory space or I/O device will complete a data transfer. The ARDY pin accepts a rising edge that is asynchronous to CLKOUT, and is active HIGH. The falling edge of ARDY must be synchronized to the 80186 clock. Connecting ARDY HIGH will always assert the ready condition to the CPU. If this line is unused, it should be tied LOW to yield control to the SRDY pin.
SRDY	49	I	Synchronous Ready informs the 80186 that the addressed memory space or I/O device will complete a data transfer. The SRDY pin accepts an active-HIGH input synchronized to CLKOUT. The use of SRDY allows a relaxed system timing over ARDY. This is accomplished by elimination of the one-half clock cycle required to internally synchronize the ARDY input signal. Connecting SRDY high will always assert the ready condition to the CPU. If this line is unused, it should be tied LOW to yield control to the ARDY pin.
$\overline{LOCK}$	48	O	$\overline{LOCK}$ output indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is requested by the LOCK prefix instruction and is activated at the beginning of the first data cycle associated with the instruction following the LOCK prefix. It remains active until the completion of that instruction. No instruction prefetching will occur while $\overline{LOCK}$ is asserted. When executing more than one LOCK instruction, always make sure there are 6 bytes of code between the end of the first LOCK instruction and the start of the second LOCK instruction. $\overline{LOCK}$ is driven HIGH for one clock during RESET and then floated.
$\overline{S0}$ $\overline{S1}$ $\overline{S2}$	52 53 54	O O O	Bus cycle status $\overline{S0}$–$\overline{S2}$ are encoded to provide bus-transaction information:

80186 Bus Cycle Status Information

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Bus Cycle Initiated
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

The status pins float during HOLD.
$\overline{S2}$ may be used as a logical M/$\overline{IO}$ indicator, and $\overline{S1}$ as a DT/$\overline{R}$ indicator.

Table 1. 80186 Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
A19/S6 A18/S5 A17/S4 A16/S3	65 66 67 68	O O O O	Address Bus Outputs (16–19) and Bus Cycle Status (3–6) indicate the four most significant address bits during T_1. These signals are active HIGH. During T_2, T_3, T_W, and T_4, the S6 pin is LOW to indicate a CPU-initiated bus cycle or HIGH to indicate a DMA-initiated bus cycle. During the same T-states, S3, S4, and S5 are always LOW. The status pins float during bus HOLD or RESET.
AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0	1 3 5 7 10 12 14 16 2 4 6 8 11 13 15 17	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	Address/Data Bus (0–15) signals constitute the time multiplexed memory or I/O address (T_1) and data (T_2, T_3, T_W, and T_4) bus. The bus is active HIGH. A_0 is analogous to $\overline{BHE}$ for the lower byte of the data bus, pins D_7 through D_0. It is LOW during T_1 when a byte is to be transferred onto the lower portion of the bus in memory or I/O operations.
$\overline{BHE}$/S7	64	O	During T_1 the Bus High Enable signal should be used to determine if data is to be enabled onto the most significant half of the data bus; pins D_{15}–D_8. $\overline{BHE}$ is LOW during T_1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the higher half of the bus. The S_7 status information is available during T_2, T_3, and T_4. S_7 is logically equivalent to $\overline{BHE}$. $\overline{BHE}$/S7 floats during HOLD.

$\overline{BHE}$ and A0 Encodings

$\overline{BHE}$ Value	A0 Value	Function
0	0	Word Transfer
0	1	Byte Transfer on upper half of data bus (D15–D8)
1	0	Byte Transfer on lower half of data bus (D_7–D_0)
1	1	Reserved

ALE/QS0	61	O	Address Latch Enable/Queue Status 0 is provided by the 80186 to latch the address. ALE is active HIGH. Addresses are guaranteed to be valid on the trailing edge of ALE. The ALE rising edge is generated off the rising edge of the CLKOUT immediately preceding T_1 of the associated bus cycle, effectively one-half clock cycle earlier than in the 8086. The trailing edge is generated off the CLKOUT rising edge in T_1 as in the 8086. Note that ALE is never floated.
$\overline{WR}$/QS1	63	O	Write Strobe/Queue Status 1 indicates that the data on the bus is to be written into a memory or an I/O device. $\overline{WR}$ is active for T_2, T_3, and T_W of any write cycle. It is active LOW, and floats during HOLD. When the 80186 is in queue status mode, the ALE/QS0 and $\overline{WR}$/QS1 pins provide information about processor/instruction queue interaction.

QS1	QS0	Queue Operation
0	0	No queue operation
0	1	First opcode byte fetched from the queue
1	1	Subsequent byte fetched from the queue
1	0	Empty the queue

Table 1. 80186 Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
HOLD HLDA	50 51	I O	HOLD indicates that another bus master is requesting the local bus. The HOLD input is active HIGH. HOLD may be asynchronous with respect to the 80186 clock. The 80186 will issue a HLDA (HIGH) in response to a HOLD request at the end of T_4 or T_i. Simultaneous with the issuance of HLDA, the 80186 will float the local bus and control lines. After HOLD is detected as being LOW, the 80186 will lower HLDA. When the 80186 needs to run another bus cycle, it will again drive the local bus and control lines.
$\overline{UCS}$	34	O	Upper Memory Chip Select is an active LOW output whenever a memory reference is made to the defined upper portion (1K–256K block) of memory. This line is not floated during bus HOLD. The address range activating $\overline{UCS}$ is software programmable.
$\overline{LCS}$	33	O	Lower Memory Chip Select is active LOW whenever a memory reference is made to the defined lower portion (1K–256K) of memory. This line is not floated during bus HOLD. The address range activating $\overline{LCS}$ is software programmable.
$\overline{MCS0}$ $\overline{MCS1}$ $\overline{MCS2}$ $\overline{MCS3}$	38 37 36 35	O O O O	Mid-Range Memory Chip Select signals are active LOW when a memory reference is made to the defined mid-range portion of memory (8K–512K). These lines are not floated during bus HOLD. The address ranges activating $\overline{MCS0}$–3 are software programmable.
$\overline{PCS0}$ $\overline{PCS1}$ $\overline{PCS2}$ $\overline{PCS3}$ $\overline{PCS4}$	25 27 28 29 30	O O O O O	Peripheral Chip Select signals 0–4 are active LOW when a reference is made to the defined peripheral area (64K byte I/O space). These lines are not floated during bus HOLD. The address ranges activating $\overline{PCS0}$–4 are software programmable.
$\overline{PCS5}$/A1	31	O	Peripheral Chip Select 5 or Latched A1 may be programmed to provide a sixth peripheral chip select, or to provide an internally latched A1 signal. The address range activating $\overline{PCS5}$ is software-programmable. $\overline{PCS5}$/A1 does not float during bus HOLD. When programmed to provide latched A1, this pin will retain the previously latched value during HOLD.
$\overline{PCS6}$/A2	32	O	Peripheral Chip Select 6 or Latched A2 may be programmed to provide a seventh peripheral chip select, or to provide an internally latched A2 signal. The address range activating $\overline{PCS6}$ is software programmable. $\overline{PCS6}$/A2 does not float during bus HOLD. When programmed to provide latched A2, this pin will retain the previously latched value during HOLD.
DT/$\overline{R}$	40	O	Data Transmit/Receive controls the direction of data flow through an external data bus transceiver. When LOW, data is transferred to the 80186. When HIGH the 80186 places write data on the data bus.
$\overline{DEN}$	39	O	Data Enable is provided as a data bus transceiver output enable. $\overline{DEN}$ is active LOW during each memory and I/O access. $\overline{DEN}$ is HIGH whenever DT/$\overline{R}$ changes state. During RESET, $\overline{DEN}$ is driven HIGH for one clock, then floated. $\overline{DEN}$ also floats during HOLD.

FUNCTIONAL DESCRIPTION

Introduction

The following Functional Description describes the base architecture of the 80186. The 80186 is a very high integration 16-bit microprocessor. It combines 15–20 of the most common microprocessor system components onto one chip while providing twice the performance of the standard 8086. The 80186 is object code compatible with the 8086/8088 microprocessors and adds 10 new instruction types to the 8086/8088 instruction set.

80186 BASE ARCHITECTURE

The 8086, 8088, 80186, and 80286 family all contain the same basic set of registers, instructions, and addressing modes.

Register Set

The 80186 base architecture has fourteen registers as shown in Figures 3a and 3b. These registers are grouped into the following categories.

General Registers

Eight 16-bit general purpose registers may be used for arithmetic and logical operands. Four of these (AX, BX, CX, and DX) can be used as 16-bit registers or split into pairs of separate 8-bit registers.

Segment Registers

Four 16-bit special purpose registers select, at any given time, the segments of memory that are immediately addressable for code, stack, and data. (For usage, refer to Memory Organization.)

Base and Index Registers

Four of the general purpose registers may also be used to determine offset addresses of operands in memory. These registers may contain base addresses or indexes to particular locations within a segment. The addressing mode selects the specific registers for operand and address calculations.

Status and Control Registers

Two 16-bit special purpose registers record or alter certain aspects of the 80186 processor state. These are the Instruction Pointer Register, which contains the offset address of the next sequential instruction to be executed, and the Status Word Register, which contains status and control flag bits (see Figures 3a and 3b).

Status Word Description

The Status Word records specific characteristics of the result of logical and arithmetic instructions (bits 0, 2, 4, 6, 7, and 11) and controls the operation of the 80186 within a given operating mode (bits 8, 9, and 10). The Status Word Register is 16-bits wide. The function of the Status Word bits is shown in Table 2.

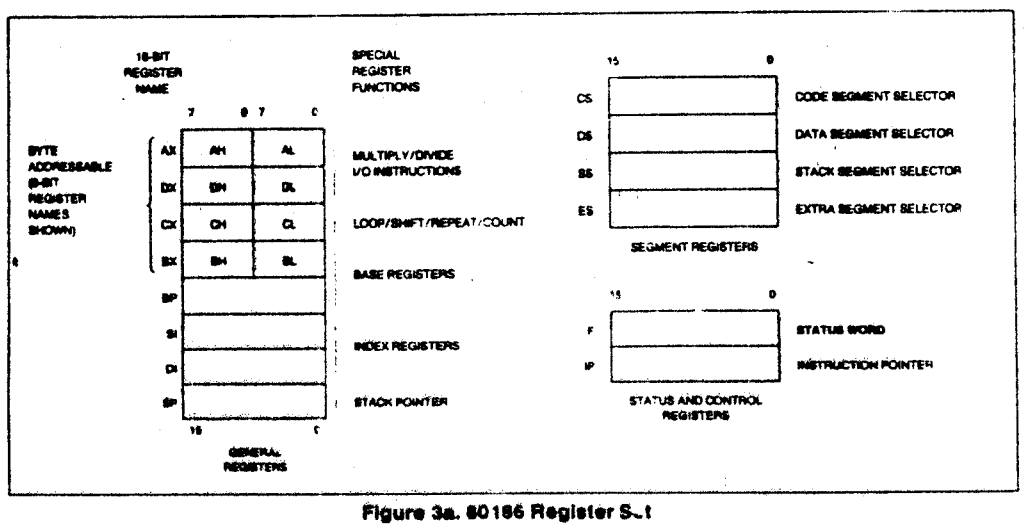

Figure 3a. 80186 Register Set

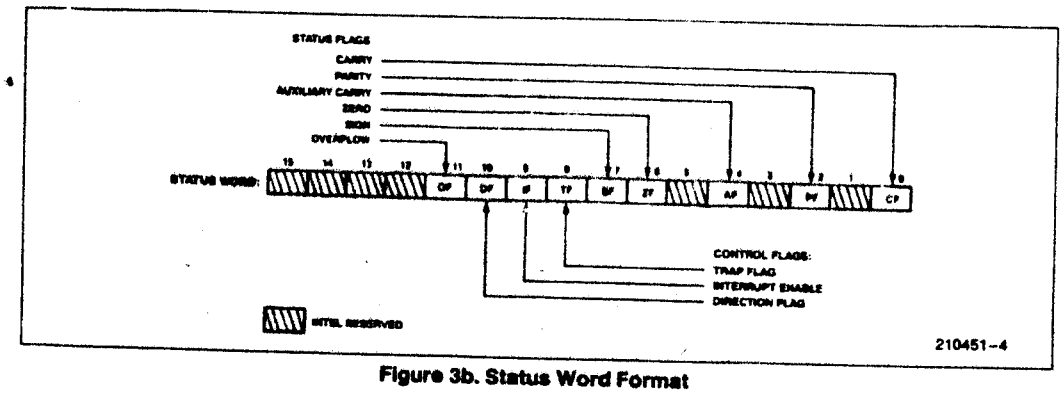

Figure 3b. Status Word Format

Table 2. Status Word Bit Functions

Bit Position	Name	Function
0	CF	Carry Flag—Set on high-order bit carry or borrow; cleared otherwise
2	PF	Parity Flag—Set if low-order 8 bits of result contain an even number of 1-bits; cleared otherwise
4	AF	Set on carry from or borrow to the low order four bits of AL; cleared otherwise
6	ZF	Zero Flag—Set if result is zero; cleared otherwise
7	SF	Sign Flag—Set equal to high-order bit of result (0 if positive, 1 if negative)
8	TF	Single Step Flag—Once set, a single step interrupt occurs after the next instruction executes. TF is cleared by the single step interrupt.
9	IF	Interrupt-enable Flag—When set, maskable interrupts will cause the CPU to transfer control to an interrupt vector specified location.
10	DF	Direction Flag—Causes string instructions to auto decrement the appropriate index register when set. Clearing DF causes auto increment.
11	OF	Overflow Flag—Set if the signed result cannot be expressed within the number of bits in the destination operand; cleared otherwise

Instruction Set

The instruction set is divided into seven categories: data transfer, arithmetic, shift/rotate/logical, string manipulation, control transfer, high-level instructions, and processor control. These categories are summarized in Figure 4.

An 80186 instruction can reference anywhere from zero to several operands. An operand can reside in a register, in the instruction itself, or in memory. Specific operand addressing modes are discussed later in this data sheet.

Memory Organization

Memory is organized in sets of segments. Each segment is a linear contiguous sequence of up to 64K (2^{16}) 8-bit bytes. Memory is addressed using a two-component address (a pointer) that consists of a 16-bit base segment and a 16-bit offset. The 16-bit base values are contained in one of four internal segment register (code, data, stack, extra). The physical address is calculated by shifting the base value LEFT by four bits and adding the 16-bit offset value to yield a 20-bit physical address (see Figure 5). This allows for a 1 MByte physical address size.

All instructions that address operands in memory must specify the base segment and the 16-bit offset value. For speed and compact instruction encoding, the segment register used for physical address generation is implied by the addressing mode used (see Table 3). These rules follow the way programs are written (see Figure 6) as independent modules that require areas for code and data, a stack, and access to external data areas.

Special segment override instruction prefixes allow the implicit segment register selection rules to be overridden for special cases. The stack, data, and extra segments may coincide for simple programs.

GENERAL PURPOSE	
MOV	Move byte or word
PUSH	Push word onto stack
POP	Pop word off stack
PUSHA	Push all registers on stack
POPA	Pop all registers from stack
XCHG	Exchange byte or word
XLAT	Translate byte
INPUT/OUTPUT	
IN	Input byte or word
OUT	Output byte or word
ADDRESS OBJECT	
LEA	Load effective address
LDS	Load pointer using DS
LES	Load pointer using ES
FLAG TRANSFER	
LAHF	Load AH register from flags
SAHF	Store AH register in flags
PUSHF	Push flags onto stack
POPF	Pop flags off stack
ADDITION	
ADD	Add byte or word
ADC	Add byte or word with carry
INC	Increment byte or word by 1
AAA	ASCII adjust for addition
DAA	Decimal adjust for addition
SUBTRACTION	
SUB	Subtract byte or word
SBB	Subtract byte or word with borrow
DEC	Decrement byte or word by 1
NEG	Negate byte or word
CMP	Compare byte or word
AAS	ASCII adjust for subtraction
DAS	Decimal adjust for subtraction
MULTIPLICATION	
MUL	Multiply byte or word unsigned
IMUL	Integer multiply byte or word
AAM	ASCII adjust for multiply
DIVISION	
DIV	Divide byte or word unsigned
IDIV	Integer divide byte or word
AAD	ASCII adjust for division
CBW	Convert byte to word
CWD	Convert word to doubleword

MOVS	Move byte or word string
INS	Input bytes or word string
OUTS	Output bytes or word string
CMPS	Compare byte or word string
SCAS	Scan byte or word string
LODS	Load byte or word string
STOS	Store byte or word string
REP	Repeat
REPE/REPZ	Repeat while equal/zero
REPNE/REPNZ	Repeat while not equal/not zero
LOGICALS	
NOT	"Not" byte or word
AND	"And" byte or word
OR	"Inclusive or" byte or word
XOR	"Exclusive or" byte or word
TEST	"Test" byte or word
SHIFTS	
SHL/SAL	Shift logical/arithmetic left byte or word
SHR	Shift logical right byte or word
SAR	Shift arithmetic right byte or word
ROTATES	
ROL	Rotate left byte or word
ROR	Rotate right byte or word
RCL	Rotate through carry left byte or word
RCR	Rotate through carry right byte or word
FLAG OPERATIONS	
STC	Set carry flag
CLC	Clear carry flag
CMC	Complement carry flag
STD	Set direction flag
CLD	Clear direction flag
STI	Set interrupt enable flag
CLI	Clear interrupt enable flag
EXTERNAL SYNCHRONIZATION	
HLT	Halt until interrupt or reset
WAIT	Wait for TEST pin active
ESC	Escape to extension processor
LOCK	Lock bus during next instruction
NO OPERATION	
NOP	No operation
HIGH LEVEL INSTRUCTIONS	
ENTER	Format stack for procedure entry
LEAVE	Restore stack for procedure exit
BOUND	Detects values outside prescribed range

Figure 4. 80186 Instruction Set

CONDITIONAL TRANSFERS	
JA/JNBE	Jump if above/not below nor equal
JAE/JNB	Jump if above or equal/not below
JB/JNAE	Jump if below/not above nor equal
JBE/JNA	Jump if below or equal/not above
JC	Jump if carry
JE/JZ	Jump if equal/zero
JG/JNLE	Jump if greater/not less nor equal
JGE/JNL	Jump if greater or equal/not less
JL/JNGE	Jump if less/not greater nor equal
JLE/JNG	Jump if less or equal/not greater
JNC	Jump if not carry
JNE/JNZ	Jump if not equal/not zero
JNO	Jump if not overflow
JNP/JPO	Jump if not parity/parity odd
JNS	Jump if not sign

JO	Jump if overflow
JP/JPE	Jump if parity/parity even
JS	Jump if sign
UNCONDITIONAL TRANSFERS	
CALL	Call procedure
RET	Return from procedure
JMP	Jump
ITERATION CONTROLS	
LOOP	Loop
LOOPE/LOOPZ	Loop if equal/zero
LOOPNE/LOOPNZ	Loop if not equal/not zero
JCXZ	Jump if register CX = 0
INTERRUPTS	
INT	Interrupt
INTO	Interrupt if overflow
IRET	Interrupt return

Figure 4. 80186 Instruction Set (Continued)

To access operands that do not reside in one of the four immediately available segments, a full 32-bit pointer can be used to reload both the base (segment) and offset values.

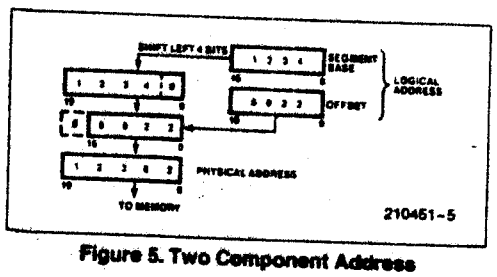

Figure 5. Two Component Address

Table 3. Segment Register Selection Rules

Memory Reference Needed	Segment Register Used	Implicit Segment Selection Rule
Instructions	Code (CS)	Instruction prefetch and immediate data.
Stack	Stack (SS)	All stack pushes and pops; any memory references which use BP Register as a base register.
External Data (Global)	Extra (ES)	All string instruction references which use the DI register as an index.
Local Data	Data (DS)	All other data references.

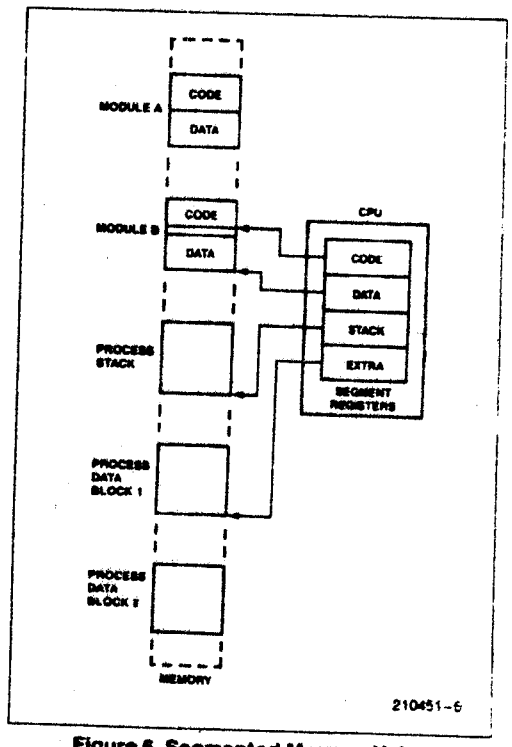

Figure 6. Segmented Memory Helps Structure Software

8279/8279-5
PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE

- **Simultaneous Keyboard Display Operations**
- **Scanned Keyboard Mode**
- **Scanned Sensor Mode**
- **Strobed Input Entry Mode**
- **8-Character Keyboard FIFO**
- **2-Key Lockout or N-Key Rollover with Contact Debounce**
- **Dual 8- or 16-Numerical Display**
- **Single 16-Character Display**
- **Right or Left Entry 16-Byte Display RAM**
- **Mode Programmable from CPU**
- **Programmable Scan Timing**
- **Interrupt Output on Key Entry**
- **Available in EXPRESS**
  - **— Standard Temperature Range**
  - **— Extended Temperature Range**

The Intel® 8279 is a general purpose programmable keyboard and display I/O interface device designed for use with Intel® microprocessors. The keyboard portion can provide a scanned interface to a 64-contact key matrix. The keyboard portion will also interface to an array of sensors or a strobed interface keyboard, such as the hall effect and ferrite variety. Key depressions can be 2-key lockout or N-key rollover. Keyboard entries are debounced and strobed in an 8-character FIFO. If more than 8 characters are entered, overrun status is set. Key entries set the interrupt output line to the CPU.

The display portion provides a scanned display interface for LED, incandescent, and other popular display technologies. Both numeric and alphanumeric segment displays may be used as well as simple indicators. The 8279 has 16x8 display RAM which can be organized into dual 16x4. The RAM can be loaded or interrogated by the CPU. Both right entry, calculator and left entry typewriter display formats are possible. Both read and write of the display RAM can be done with auto-increment of the display RAM address.

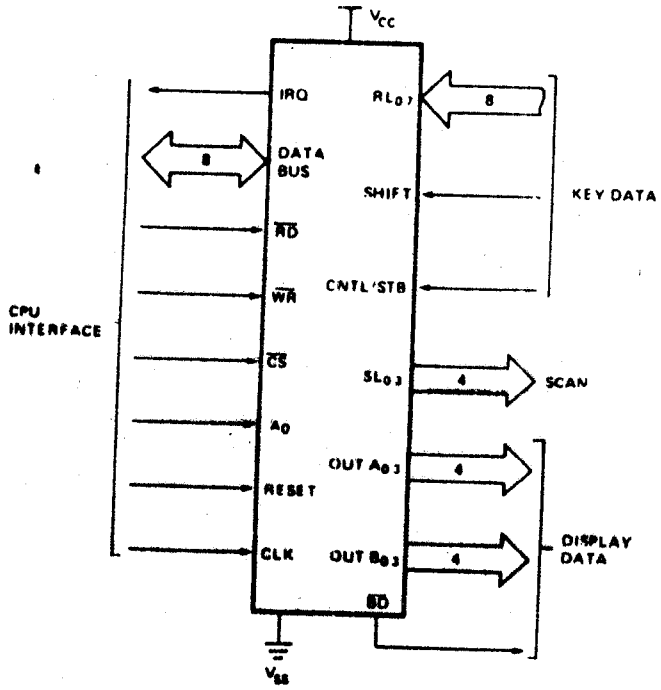

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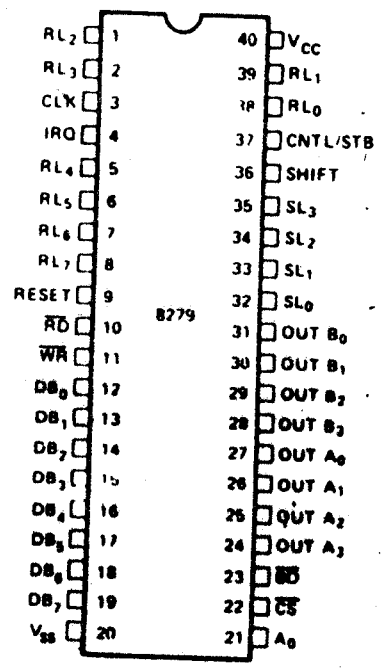
Figure 1. Logic Symbol



290123-2

Figure 2. Pin Configuration

HARDWARE DESCRIPTION

The 8279 is packaged in a 40 pin DIP. The following is a functional description of each pin.

Table 1. Pin Description

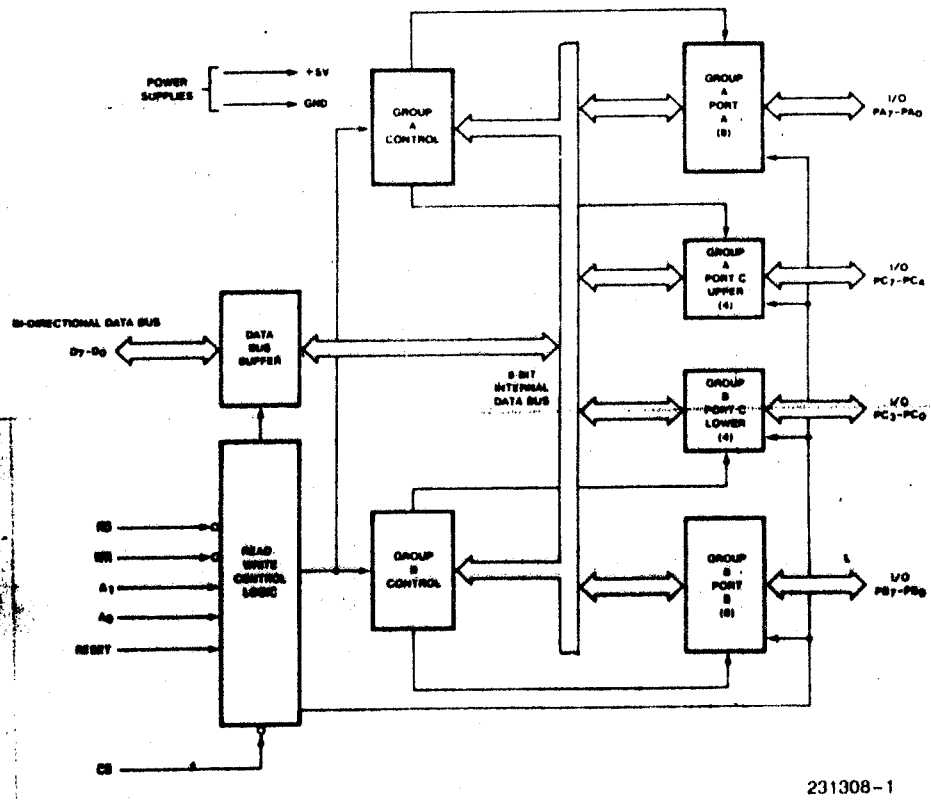
Symbol	Pin No.	Name and Function
DB_0–DB_7	19–12	**BI-DIRECTIONAL DATA BUS:** All data and commands between the CPU and the 8279 are transmitted on these lines.
CLK	3	**CLOCK:** Clock from system used to generate internal timing.
RESET	9	**RESET:** A high signal on this pin resets the 8279. After being reset the 8279 is placed in the following mode: 1) 16 8-bit character display—left entry. 2) Encoded scan keyboard—2 key lockout. Along with this the program clock prescaler is set to 31.
CS	22	**CHIP SELECT:** A low on this pin enables the interface functions to receive or transmit.
A_0	21	**BUFFER ADDRESS:** A high on this line indicates the signals in or out are interpreted as a command or status. A low indicates that they are data.
$\overline{RD}$, $\overline{WR}$	10–11	**INPUT/OUTPUT READ AND WRITE:** These signals enable the data buffers to either send data to the external bus or receive it from the external bus.
IRQ	4	**INTERRUPT REQUEST:** In a keyboard mode, the interrupt line is high when there is data in the FIFO/Sensor RAM. The interrupt line goes low with each FIFO/Sensor RAM read and returns high if there is still information in the RAM. In a sensor mode, the interrupt line goes high whenever a change in a sensor is detected.
V_{SS}, V_{CC}	20, 40	**GROUND AND POWER SUPPLY PINS.**
SL_0–SL_3	32–35	**SCAN LINES:** Scan lines which are used to scan the key switch or sensor matrix and the display digits. These lines can be either encoded (1 of 16) or decoded (1 of 4).
RL_0–RL_7	38, 39, 1, 2, 5–8	**RETURN LINE:** Return line inputs which are connected to the scan lines through the keys or sensor switches. They have active internal pullups to keep them high until a switch closure pulls one low. They also serve as an 8-bit input in the Strobed Input mode.
SHIFT	36	**SHIFT:** The shift input status is stored along with the key position on key closure in the Scanned Keyboard modes. It has an active internal pullup to keep it high until a switch closure pulls it low.
CNTL/STB	37	**CONTROL/STROBED INPUT MODE:** For keyboard modes this line is used as a control input and stored like status on a key closure. The line is also the strobe line that enters the data into the FIFO in the Strobed Input mode. (Rising Edge). It has an active internal pullup to keep it high until a switch closure pulls it low.
OUT A_0–OUT A_3 OUT B_0–OUT B_3	27-24 31–28	**OUTPUTS:** These two ports are the outputs for the 16 x 4 display refresh registers. The data from these outputs is synchronized to the scan lines (SL_0–SL_3) for multiplexed digit displays. The two 4 bit ports may be blanked independently. These two ports may also be considered as one 8-bit port.
$\overline{BD}$	23	**BLANK DISPLAY:** This output is used to blank the display during digit switching or by a display blanking command.

8255A/8255A-5
PROGRAMMABLE PERIPHERAL INTERFACE

- MCS-85™ Compatible 8255A-5
- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with Intel Microprocessor Families
- Improved Timing Characteristics
- Direct Bit Set/Reset Capability Easing Control Application Interface
- Reduces System Package Count
- Improved DC Driving Capability
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range
- 40 Pin DIP Package or 44 Lead PLCC

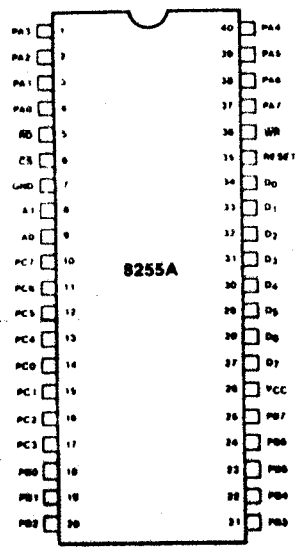
(See Intel Packaging: Order Number: 231369)

The Intel 8255A is a general purpose programmable I/O device designed for use with Intel microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.



231308-1

Figure 1. 8255A Block Diagram



231308-2

Figure 2. Pin Configuration

November 1987
Order Number: 231308-002

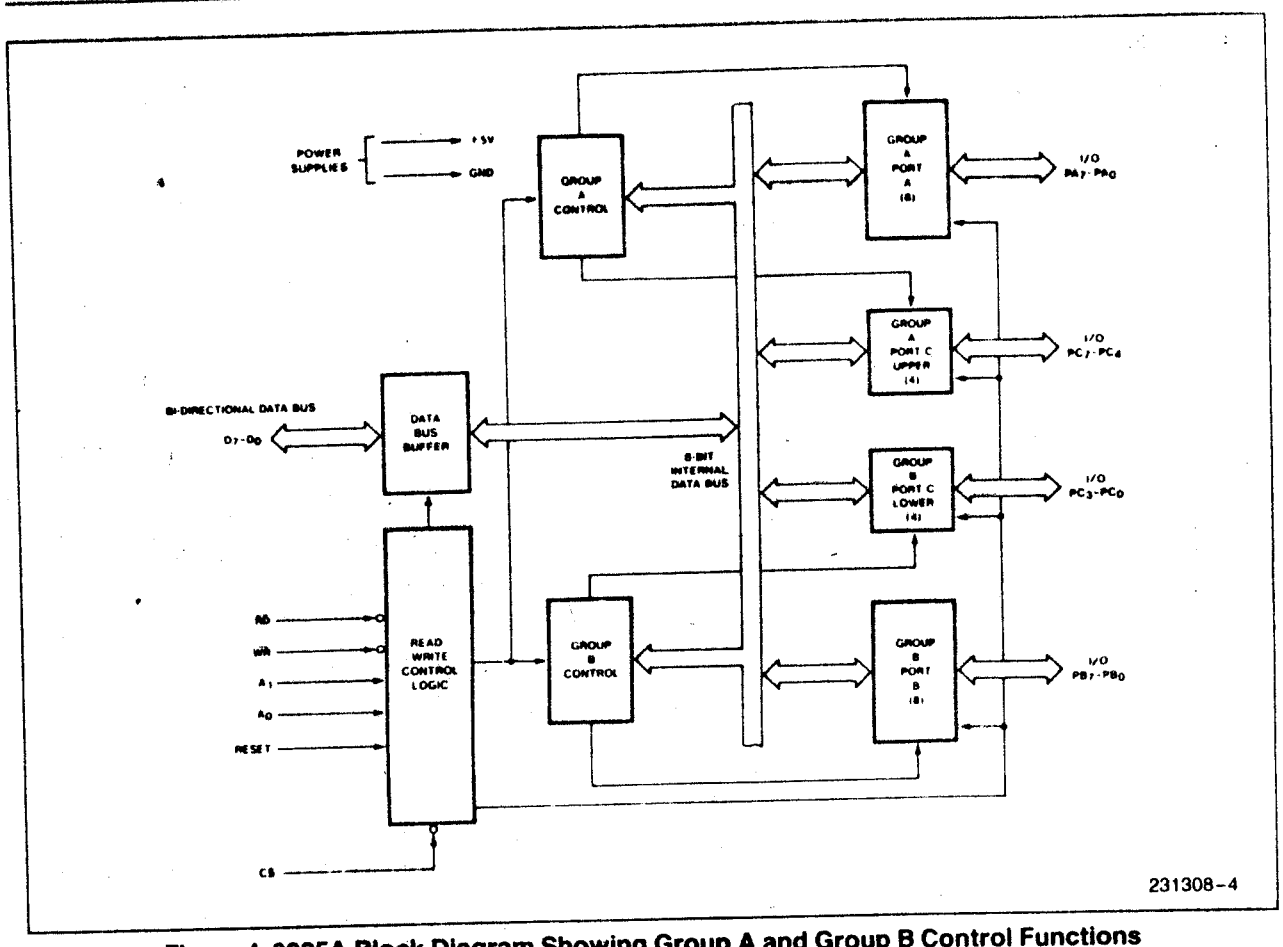


Figure 4. 8225A Block Diagram Showing Group A and Group B Control Functions

Pin Configuration

Pin Names

D_7-D_0	Data Bus (Bi-Directional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A0, A1	Port Address
PA7–PA0	Port A (BIT)
PB7–PB0	Port B (BIT)
PC7–PC0	Port C (BIT)
V_{CC}	+ 5 Volts
GND	0 Volts

CAPACITANCE T_A = 25°C, V_{CC} = GND = 0V

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	f_c = 1 MHz(4)
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND(4)

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = +5V ±10%, GND = 0V*

Bus Parameters

READ

Symbol	Parameter	8255A		8255A-5		Unit
		Min	Max	Min	Max	
t_{AR}	Address Stable before READ	0		0		ns
t_{RA}	Address Stable after READ	0		0		ns
t_{RR}	READ Pulse Width	300		300		ns
t_{RD}	Data Valid from READ(1)		250		200	ns
t_{DF}	Data Float after READ	10	150	10	100	ns
t_{RV}	Time between READs and/or WRITEs	850		850		ns

WRITE

Symbol	Parameter	8255A		8255A-5		Unit
		Min	Max	Min	Max	
t_{AW}	Address Stable before WRITE	0		0		ns
t_{WA}	Address Stable after WRITE	20		20		ns
t_{WW}	WRITE Pulse Width	400		300		ns
t_{DW}	Data Valid to WRITE (T.E.)	100		100		ns
t_{WD}	Data Valid after WRITE	30		30		ns

OTHER TIMINGS

Symbol	Parameter	8255A		8255A-5		Unit
		Min	Max	Min	Max	
t_{WB}	WR = 1 to Output(1)		350		350	ns
t_{IR}	Peripheral Data before RD	0		0		ns
t_{HR}	Peripheral Data after RD	0		0		ns
t_{AK}	ACK Pulse Width	300		300		ns
t_{ST}	STB Pulse Width	500		500		ns
t_{PS}	Per. Data before T.E. of STB	0		0		ns
t_{PH}	Per. Data after T.E. of STB	180		180		ns
t_{AD}	ACK = 0 to Output(1)		300		300	ns
t_{KD}	ACK = 1 to Output Float	20	250	20	250	ns

A.C. CHARACTERISTICS (Continued)

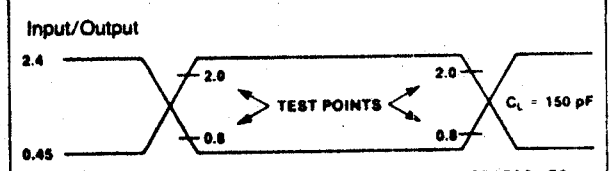
OTHER TIMINGS (Continued)

Symbol	Parameter	8255A		8255A-5		Unit
		Min	Max	Min	Max	
t_{WOB}	WR = 1 to OBF = 0(1)		650		650	ns
t_{AOB}	ACK = 0 to OBF = 1(1)		350		350	ns
t_{SIB}	STB = 0 to IBF = 1(1)		300		300	ns
t_{RIB}	RD = 1 to IBF = 0(1)		300		300	ns
t_{RIT}	RD = 0 to INTR = 0(1)		400		400	ns
t_{SIT}	STB = 1 to INTR = 1(1)		300		300	ns
t_{AIT}	ACK = 1 to INTR = 1(1)		350		350	ns
t_{WIT}	WR = 0 to INTR = 0(1, 3)		850		850	ns

NOTES:
1. Test Conditions: C_L = 150 pF.
2. Period of Reset pulse must be at least 50 μs during or after power on. Subsequent Reset pulse can be 500 ns min.
3. INTR ↑ may occur as early as $\overline{WR}$ ↓.
4. Sampled, not 100% tested.

*For Extended Temperature EXPRESS, use M8255A electrical parameters.

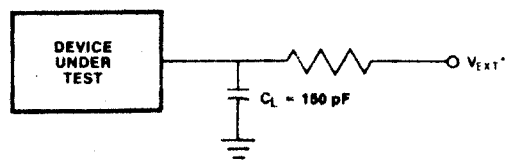
A.C. TESTING INPUT, OUTPUT WAVEFORM



231308-50

A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

A.C. TESTING LOAD CIRCUIT



231308-51

*V_{EXT} is set at various voltages during testing to guarantee the specification. C_L includes jig capacitance.

8251A
PROGRAMMABLE COMMUNICATION INTERFACE

- Synchronous and Asynchronous Operation
- Synchronous 5–8 Bit Characters; Internal or External Character Synchronization; Automatic Sync Insertion
- Asynchronous 5–8 Bit Characters; Clock Rate—1, 16 or 64 Times Baud Rate; Break Character Generation; 1, 1½, or 2 Stop Bits; False Start Bit Detection; Automatic Break Detect and Handling
- Synchronous Baud Rate—DC to 64K Baud
- Asynchronous Baud Rate—DC to 19.2K Baud
- Full-Duplex, Double-Buffered Transmitter and Receiver
- Error Detection—Parity, Overrun and Framing
- Compatible with an Extended Range of Intel Microprocessors
- 28-Pin DIP Package
- All Inputs and Outputs are TTL Compatible
- Available in EXPRESS
  —Standard Temperature Range
  —Extended Temperature Range

The Intel® 8251A is the enhanced version of the industry standard, Intel 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART), designed for data communications with Intel's microprocessor families such as MCS-48, 80, 85, and iAPX-86, 88. The 8251A is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM "bi-sync"). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPTY. The chip is fabricated using N-channel silicon gate technology.

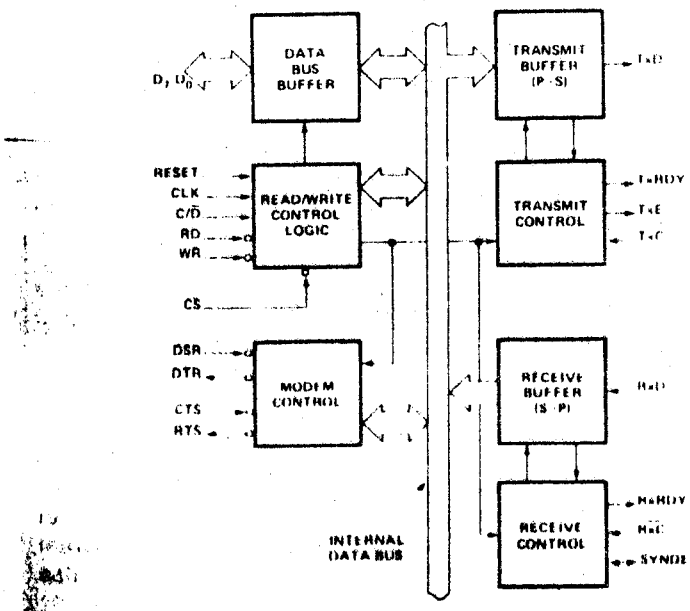


Figure 1. Block Diagram

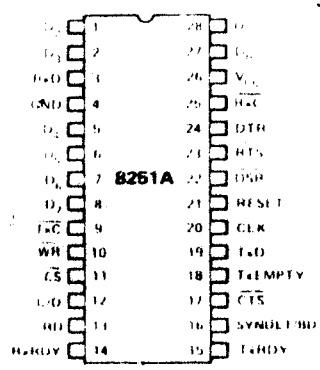


Figure 2. Pin Configuration

FEATURES AND ENHANCEMENTS

The 8251A is an advanced design of the industry standard USART, the Intel® 8251. The 8251A operates with an extended range of Intel microprocessors and maintains compatibility with the 8251. Familiarization time is minimal because of compatibility and involves only knowing the additional features and enhancements, and reviewing the AC and DC specifications of the 8251A.

The 8251A incorporates all the key features of the 8251 and has the following additional features and enhancements:

- 8251A has double-buffered data paths with separate I/O registers for control, status, Data In, and Data Out, which considerably simplifies control programming and minimizes CPU overhead.
- In asynchronous operations, the Receiver detects and handles "break" automatically, relieving the CPU of this task.
- A refined Rx initialization prevents the Receiver from starting when in "break" state, preventing unwanted interrupts from a disconnected USART.
- At the conclusion of a transmission, TxD line will always return to the marking state unless SBRK is programmed.
- Tx Enable logic enhancement prevents a Tx Disable command from halting transmission until all data previously written has been transmitted. The logic also prevents the transmitter from turning off in the middle of a word.
- When External Sync Detect is programmed, Internal Sync Detect is disabled, and an External Sync Detect status is provided via a flip-flop which clears itself upon a status read.
- Possibility of false sync detect is minimized by ensuring that if double character sync is programmed, the characters be contiguously detected and also by clearing the Rx register to all ones whenever Enter Hunt command is issued in Sync mode.
- As long as the 8251A is not selected, the $\overline{RD}$ and $\overline{WR}$ do not affect the internal operation of the device.
- The 8251A Status can be read at any time but the status update will be inhibited during status read.
- The 8251A is free from extraneous glitches and has enhanced AC and DC characteristics, providing higher speed and better operating margins.
- Synchronous Baud rate from DC to 64K.

FUNCTIONAL DESCRIPTION

General

The 8251A is a Universal Synchronous/Asynchronous Receiver/Transmitter designed for a wide range of Intel microcomputers such as 8048, 8080, 8085, 8086 and 8088. Like other I/O devices in a microcomputer system, its functional configuration is programmed by the system's software for maximum flexibility. The 8251A can support most serial data techniques in use, including IBM "bi-sync."

In a communication environment an interface device must convert parallel format system data into serial format for transmission and convert incoming serial format data into parallel system data for reception. The interface device must also delete or insert bits or characters that are functionally unique to the communication technique. In essence, the interface should appear "transparent" to the CPU, a simple input or output of byte-oriented system data.

Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the 8251A to the system Data Bus. Data is transmitted or received by the buffer upon execution of INput or OUTput instructions of the CPU. Control words, Command words and Status information are also transferred through the Data Bus Buffer. The Command Status, Data-In and Data-Out registers are separate, 8-bit registers communicating with the system bus through the Data Bus Buffer.

This functional block accepts inputs from the system Control bus and generates control signals for overall device operation. It contains the Control Word Register and Command Word Register that store the various control formats for the device functional definition.

RESET (Reset)

A "high" on this input forces the 8251A into an "Idle" mode. The device will remain at "Idle" until a new set of control words is written into the 8251A to program its functional definition. Minimum RESET pulse width is 6 t_{CY} (clock must be running).

A command reset operation also puts the device into the "Idle" state.

AFN-01573D

CLK (Clock)

The CLK input is used to generate internal device timing and is normally connected to the Phase 2 (TTL) output of the Clock Generator. No external inputs or outputs are referenced to CLK but the frequency of CLK must be greater than 30 times the Receiver or Transmitter data bit rates.

$\overline{WR}$ (Write)

A "low" on this input informs the 8251A that the CPU is writing data or control words to the 8251A.

$\overline{RD}$ (Read)

A "low" on this input informs the 8251A that the CPU is reading data or status information from the 8251A.

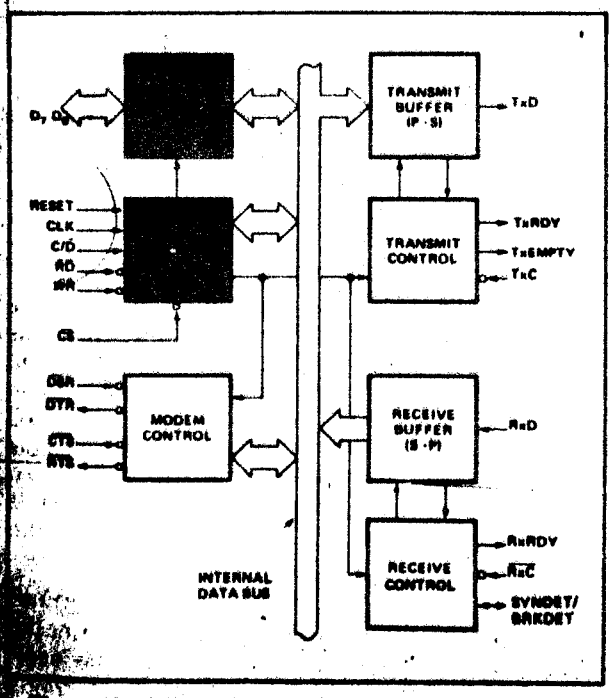


Figure 3. 8251A Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	8251A DATA → DATA BUS
0	1	0	0	DATA BUS → 8251A DATA
1	0	1	0	STATUS → DATA BUS
1	1	0	0	DATA BUS → CONTROL
X	1	1	0	DATA BUS → 3-STATE
X	X	X	1	DATA BUS → 3-STATE

C/$\overline{D}$ (Control/Data)

This input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs the 8251A that the word on the Data Bus is either a data character, control word or status information.

1 = CONTROL/STATUS; 0 = DATA.

$\overline{CS}$ (Chip Select)

A "low" on this input selects the 8251A. No reading or writing will occur unless the device is selected. When $\overline{CS}$ is high, the Data Bus is in the float state and $\overline{RD}$ and $\overline{WR}$ have no effect on the chip.

Modem Control

The 8251A has a set of control inputs and outputs that can be used to simplify the interface to almost any modem. The modem control signals are general purpose in nature and can be used for functions other than modem control, if necessary.

$\overline{DSR}$ (Data Set Ready)

The $\overline{DSR}$ input signal is a general-purpose, 1-bit inverting input port. Its condition can be tested by the CPU using a Status Read operation. The $\overline{DSR}$ input is normally used to test modem conditions such as Data Set Ready.

$\overline{DTR}$ (Data Terminal Ready)

The $\overline{DTR}$ output signal is a general-purpose, 1-bit inverting output port. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{DTR}$ output signal is normally used for modem control such as Data Terminal Ready.

$\overline{RTS}$ (Request to Send)

The $\overline{RTS}$ output signal is a general-purpose, 1-bit inverting output port. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{RTS}$ output signal is normally used for modem control such as Request to Send.

$\overline{CTS}$ (Clear to Send)

A "low" on this input enables the 8251A to transmit serial data if the Tx Enable bit in the Command byte is set to a "one." If either a Tx Enable off or $\overline{CTS}$ off condition occurs while the Tx is in operation, the Tx will transmit all the data in the USART, written prior to Tx Disable command before shutting down.

Transmitter Buffer

The Transmitter Buffer accepts parallel data from the Data Bus Buffer, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin on the falling edge of $\overline{TxC}$. The transmitter will begin transmission upon being enabled if $\overline{CTS}$ = 0. The TxD line will be held in the marking state immediately upon a master Reset or when Tx Enable or $\overline{CTS}$ is off or the transmitter is empty.

Transmitter Control

The Transmitter Control manages all activities associated with the transmission of serial data. It accepts and issues signals both externally and internally to accomplish this function.

TxRDY (Transmitter Ready)

This output signals the CPU that the transmitter is ready to accept a data character. The TxRDY output pin can be used as an interrupt to the system, since it is masked by TxEnable; or, for Polled operation, the CPU can check TxRDY using a Status Read operation. TxRDY is automatically reset by the leading edge of $\overline{WR}$ when a data character is loaded from the CPU.

Note that when using the Polled operation, the TxRDY status bit is *not* masked by TxEnable, but will only indicate the Empty/Full Status of the Tx Data Input Register.

TxE (Transmitter Empty)

When the 8251A has no characters to send, the TxEMPTY output will go "high." It resets upon receiving a character from CPU if the transmitter is enabled. TxEMPTY remains high when the transmitter is disabled. TxEMPTY can be used to indicate the end of a transmission mode, so that the CPU "knows" when to "turn the line around" in the half-duplex operational mode.

In the Synchronous mode, a "high" on this output indicates that a character has not been loaded and the SYNC character or characters are about to be or are being transmitted automatically as "fillers." TxEMPTY does not go low when the SYNC characters are being shifted out.

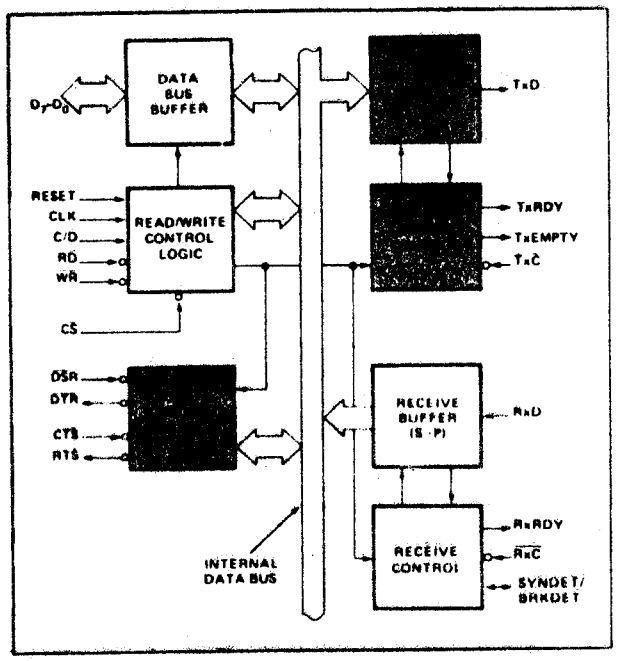


Figure 4. 8251A Block Diagram Showing Modem and Transmitter Buffer and Control Functions

$\overline{TxC}$ (Transmitter Clock)

The Transmitter Clock controls the rate at which the character is to be transmitted. In the Synchronous transmission mode, the Baud Rate (1x) is equal to the $\overline{TxC}$ frequency. In Asynchronous transmission mode, the baud rate is a fraction of the actual $\overline{TxC}$ frequency. A portion of the mode instruction selects this factor; it can be 1, 1/16 or 1/64 the $\overline{TxC}$.

For Example:
If Baud Rate equals 110 Baud,
$\overline{TxC}$ equals 110 Hz in the 1x mode.
$\overline{TxC}$ equals 1.72 kHz in the 16x mode.
$\overline{TxC}$ equals 7.04 kHz in the 64x mode.

The falling edge of $\overline{TxC}$ shifts the serial data out of the 8251A.

Receiver Buffer

The Receiver accepts serial data, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU. Serial data is input to RxD pin, and is clocked in on the rising edge of $\overline{RxC}$.

Receiver Control

This functional block manages all receiver-related activities which consists of the following features.

The RxD initialization circuit prevents the 8251A from mistaking an unused input line for an active low data line in the "break condition." Before starting to receive serial characters on the RxD line, a valid "1" must first be detected after a chip master Reset. Once this has been determined, a search for a valid low (Start bit) is enabled. This feature is only active in the asynchronous mode, and is only done once for each master Reset.

The False Start bit detection circuit prevents false starts due to a transient noise spike by first detecting the falling edge and then strobing the nominal center of the Start bit (RxD = low).

Parity error detection sets the corresponding status bit.

The Framing Error status bit is set if the Stop bit is absent at the end of the data byte (asynchronous mode).

RxRDY (Receiver Ready)

This output indicates that the 8251A contains a character that is ready to be input to the CPU. RxRDY can be connected to the interrupt structure of the CPU or, for polled operation, the CPU can check the condition of RxRDY using a Status Read operation.

RxEnable, when off, holds RxRDY in the Reset Condition. For Asynchronous mode, to set RxRDY, the Receiver must be enabled to sense a Start Bit and a complete character must be assembled and transferred to the Data Output Register. For Synchronous mode, to set RxRDY, the Receiver must be enabled and a character must finish assembly and be transferred to the Data Output Register.

Failure to read the received character from the Rx Data Output Register prior to the assembly of the next Rx Data character will set overrun condition and the previous character will be written over it. If the Rx Data is being read by the CPU during internal transfer is occurring, overrun error will be set and the old character will be lost.

RxC (Receiver Clock)

The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the Baud Rate (1x) is equal to the actual frequency of $\overline{RxC}$. In Asynchronous Mode, the Baud Rate is a fraction of the actual $\overline{RxC}$ frequency. A portion of the mode instruction selects this factor: 1, 1/16 or 1/64 the $\overline{RxC}$.

For example:

Baud Rate equals 300 Baud, if
$\overline{RxC}$ equals 300 Hz in the 1x mode;
$\overline{RxC}$ equals 4800 Hz in the 16x mode;
$\overline{RxC}$ equals 19.2 kHz in the 64x mode.

Baud Rate equals 2400 Baud, if
$\overline{RxC}$ equals 2400 Hz in the 1x mode;
$\overline{RxC}$ equals 38.4 kHz in the 16x mode;
$\overline{RxC}$ equals 153.6 kHz in the 64x mode.

Data is sampled into the 8251A on the rising edge of $\overline{RxC}$.

NOTE: In most communications systems, the 8251A will be handling both the transmission and reception operations of a single link. Consequently, the Receive and Transmit Baud Rates will be the same. Both $\overline{TxC}$ and $\overline{RxC}$ will require identical frequencies for this operation and can be tied together and connected to a single frequency source (Baud Rate Generator) to simplify the interface.

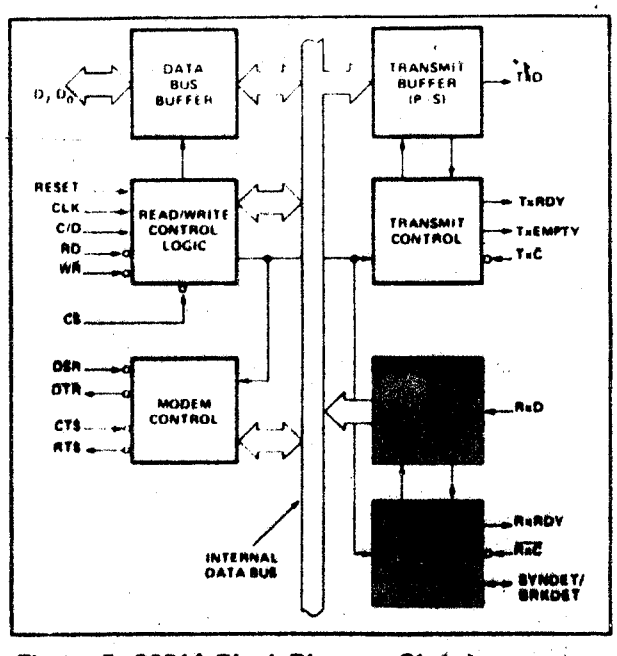


Figure 5. 8251A Block Diagram Showing Receiver Buffer and Control Functions

SYNDET (SYNC Detect/ BRKDET Break Detect)

This pin is used in Synchronous Mode for SYNDET and may be used as either input or output, programmable through the Control Word. It is reset to output mode low upon RESET. When used as an output (internal Sync mode), the SYNDET pin will go "high" to indicate that the 8251A has located the SYNC character in the Receive mode. If the 8251A is programmed to use double Sync characters (bisync), then SYNDET will go "high" in the middle of the last bit of the second Sync character. SYNDET is automatically reset upon a Status Read operation.

When used as an input (external SYNC detect mode), a positive going signal will cause the 8251A to start assembling data characters on the rising edge of the next $\overline{RxC}$. Once in SYNC, the "high" input signal can be removed. When External SYNC Detect is programmed, Internal SYNC Detect is disabled.

BREAK (Async Mode Only)

This output will go high whenever the receiver remains low through two consecutive stop bit sequences (including the start bits, data bits, and parity bits). Break Detect may also be read as a Status bit. It is reset only upon a master chip Reset or Rx Data returning to a "one" state.

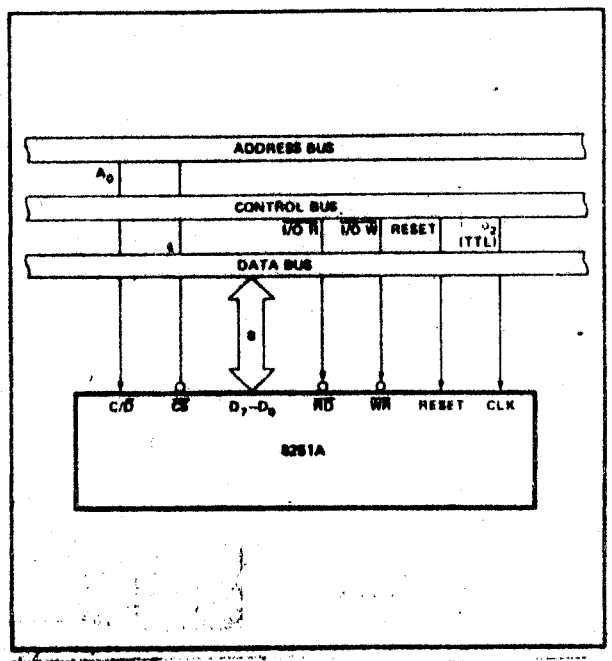


Figure 6. 8251A Interface to 8080 Standard System Bus

DETAILED OPERATION DESCRIPTION

General

The complete functional definition of the 8251A is programmed by the system's software. A set of control words must be sent out by the CPU to initialize the 8251A to support the desired communications format. These control words will program the: BAUD RATE, CHARACTER LENGTH, NUMBER OF STOP BITS, SYNCHRONOUS or ASYNCHRONOUS OPERATION, EVEN/ODD/OFF PARITY, etc. In the Synchronous Mode, options are also provided to select either internal or external character synchronization.

Once programmed, the 8251A is ready to perform its communication functions. The TxRDY output is raised "high" to signal the CPU that the 8251A is ready to receive a data character from the CPU. This output (TxRDY) is reset automatically when the CPU writes a character into the 8251A. On the other hand, the 8251A receives serial data from the MODEM or I/O device. Upon receiving an entire character, the RxRDY output is raised "high" to signal the CPU that the 8251A has a complete character ready for the CPU to fetch. RxRDY is reset automatically upon the CPU data read operation.

The 8251A cannot begin transmission until the Tx Enable (Transmitter Enable) bit is set in the Command Instruction and it has received a Clear To Send ($\overline{CTS}$) input. The TxD output will be held in the marking state upon Reset.

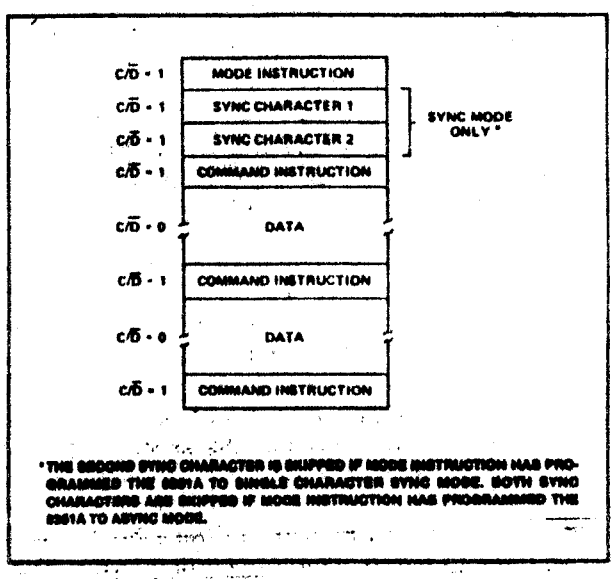


Figure 7. Typical Data Block

TYPICAL CHARACTERISTICS

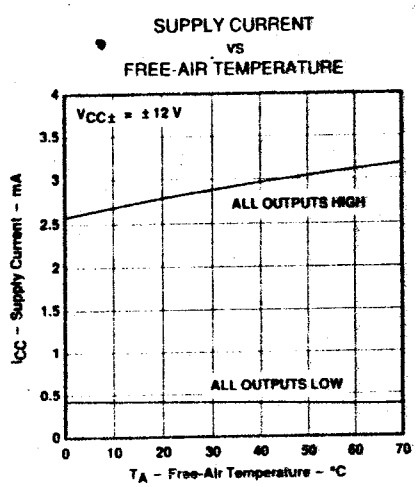


FIGURE 9

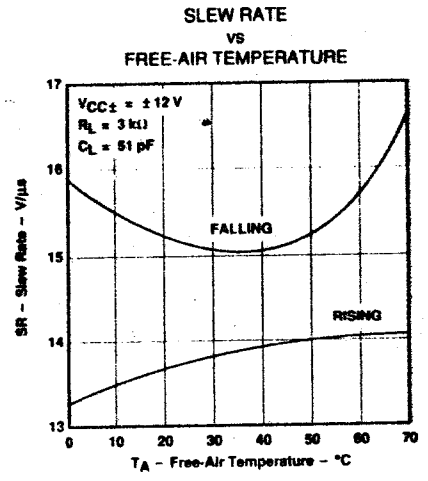


FIGURE 10

TYPICAL APPLICATION DATA

forward biasing the substrate

As with other bipolar integrated circuits, forward biasing the substrate diode can cause problems. The LT1030 will draw high current from V_{CC+} to ground if the V_{CC-} terminal is open-circuited or pulled above ground. If this is possible, connecting a diode from V_{CC-} to ground will prevent the high-current state. Any low-cost diode can be used (see Figure 11).

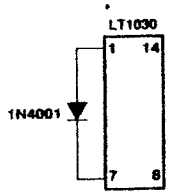


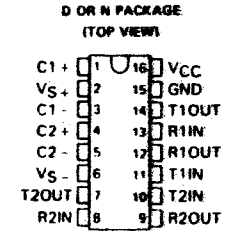
FIGURE 11. CONNECTING A DIODE FROM V_{CC-} TO GROUND

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

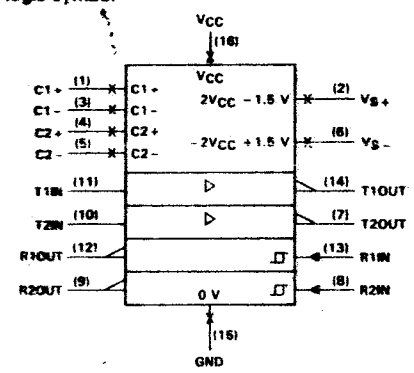
D3120, FEBRUARY 1989 REVISED JUNE 1989

- Operates with Single 5-V Power Supply
- LinBiCMOS™ Process Technology
- Two Drivers and Two Receivers
- ±30-V Input Levels
- Low Supply Current . . . 8 mA Typ
- Meets ANSI/EIA-232-D-1986 Specifications (Revision of EIA Standard RS-232-C)
- Designed to be Interchangeable with Maxim MAX232
- Applications
  - EIA-232 Interface
  - Battery-Powered Systems
  - Terminals
  - Modems
  - Computers

D OR N PACKAGE
(TOP VIEW)



logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The MAX232 is a dual driver/receiver that includes a capacitive voltage generator to supply EIA-232 voltage levels from a single 5-V supply. Each receiver converts EIA-232 inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V and a typical hysteresis of 0.5 V, and can accept ±30-V inputs. Each driver converts TTL/CMOS input levels into EIA-232 levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASIC™ library.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Input supply voltage, V_{CC} (see Note 1)	−0.3 V to 6 V
Positive output supply voltage, V_{S+}	V_{CC} −0.3 V to 15 V
Negative output supply voltage, V_{S-}	0.3 V to −15 V
Input voltage range: Driver	−0.3 V to V_{CC} + 0.3 V
Receiver	±30 V
Output voltage range: T1OUT, T2OUT	V_{S-} − 0.3 V to V_{S+} + 0.3 V
R1OUT, R2OUT	−0.3 V to V_{CC} + 0.3 V
Short-circuit duration: V_{S+}	30 s
V_{S-}	30 s
T1OUT, T2OUT	unlimited
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: All voltage values are with respect to network ground terminal.

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TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High level input voltage, V_{IH} (T1IN, T2IN)	2			V
Low level input voltage, V_{IL} (T1IN, T2IN)			0.8	V
Receiver input voltage, R1IN, R2IN			±30	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High level output voltage	T1OUT, T2OUT	R_L = 3 kΩ to GND	5	7		V
		R1OUT, R2OUT	I_{OH} = −1 mA	3.6			
V_{OL}	Low level output voltage‡	T1OUT, T2OUT	R_L = 3 kΩ to GND		−7	−5	V
		R1OUT, R2OUT	I_{OL} = 3.2 mA			0.4	
V_{T+}	Receiver positive going input threshold voltage	R1IN, R2IN	V_{CC} = 5 V, T_A = 25°C		1.7	2.4	V
V_{T-}	Receiver negative going input threshold voltage	R1IN, R2IN	V_{CC} = 5 V, T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis	R1IN, R2IN	V_{CC} = 5 V	0.2	0.5	1	kΩ
r_i	Receiver input resistance	R1IN, R2IN	V_{CC} = 5 V, T_A = 25°C	3	5	7	kΩ
r_o	Output resistance	T1OUT, T2OUT	V_{S+} = V_{S-} = 0, V_O = ±2 V	300			Ω
I_{OS}§	Short-circuit output current	T1OUT, T2OUT	V_{CC} = 5.5 V, V_O = 0		±10		mA
I_{IS}	Short-circuit input current	T1IN, T2IN	V_I = 0			200	µA
I_{CC}	Supply current		V_{CC} = 5.5 V, All outputs open, T_A = 25°C		8	10	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH(R)}$	Receiver propagation delay time, low-to-high-level output	See Figure 2		500		ns
$t_{PHL(R)}$	Receiver propagation delay time, high-to-low-level output	See Figure 2		500		ns
SR	Driver slew rate	R_L = 3 kΩ to 7 kΩ, See Figure 3			30	V/µs
SR(tr)	Driver transition region slew rate	See Figure 4		3		V/µs

TYPICAL APPLICATION DATA

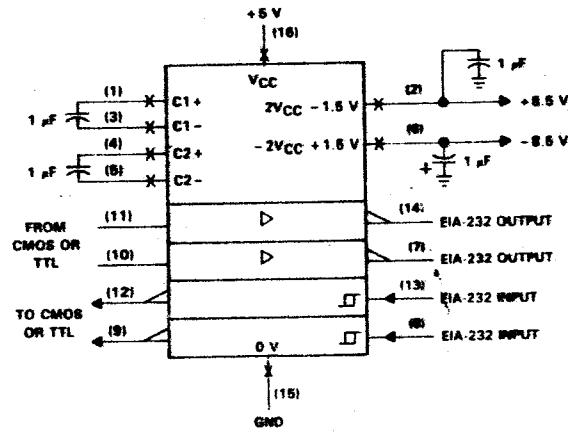
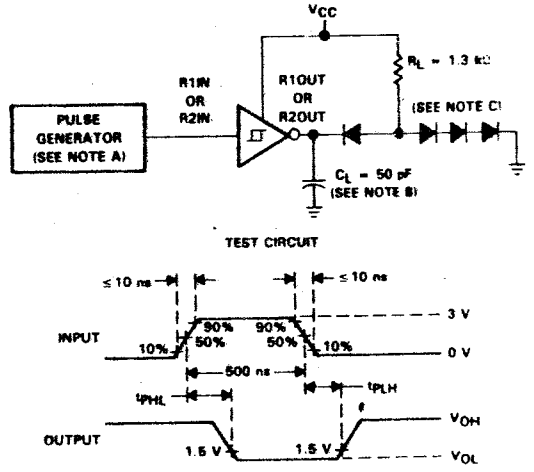


FIGURE 1. TYPICAL OPERATING CIRCUIT

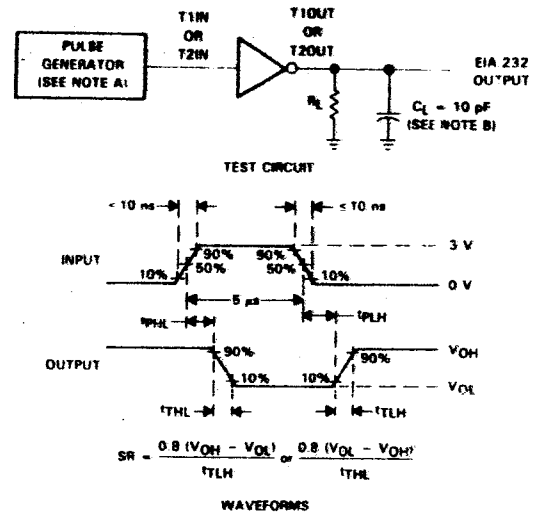
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, Duty Cycle ≤ 50%
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

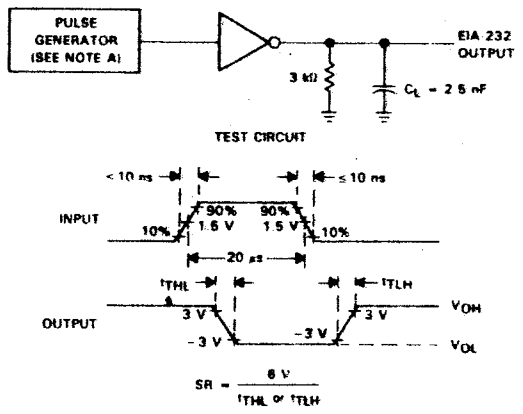
FIGURE 2. RECEIVER TEST CIRCUIT AND WAVEFORMS FOR t_{PHL} AND t_{PLH} MEASUREMENT

PARAMETER MEASUREMENT INFORMATION



NOTES A. The pulse generator has the following characteristics: Z_{OUT} = 50 Ω, Duty Cycle ≤ 50%.
B. C_L includes probe and jig capacitance.

FIGURE 3. DRIVER TEST CIRCUIT AND WAVEFORMS FOR t_{PHL} AND t_{PLH} MEASUREMENT (5-μs INPUT)



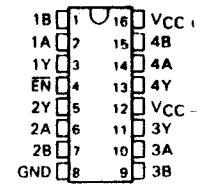
NOTE A. The pulse generator has the following characteristics: Z_{OUT} = 50 Ω, Duty Cycle ≤ 50%.

FIGURE 4. TEST CIRCUIT AND WAVEFORMS FOR t_{THL} AND t_{TLH} MEASUREMENT (20-μs INPUT)

D3006, FEBRUARY 1986 - REVISED OCTOBER 1988

- Four Independent Receivers with Common Enable Input
- High Input Sensitivity . . . 25 mV Max
- High Input Impedance
- MC3450 has Three-State Outputs
- MC3452 has Open-Collector Outputs
- Glitch-Free Power-Up/Power-Down Operation

D, J, OR N PACKAGE
(TOP VIEW)



description

The MC3450 and MC3452 are quadruple differential line receivers designed for use in balanced and unbalanced digital data transmission. The MC3450 and MC3452 are the same except that the MC3450 has three-state ouputs whereas the MC3452 has open-collector outputs, which permit the wire-AND function with similar output devices. Three-state and open-collector outputs permit connection directly to a bus-organized system.

The MC3450 and MC3452 are designed for optimum performance when used with either the MC3453 quadruple differential line driver or SN75109A, SN75110A, and SN75112 dual differential drivers.

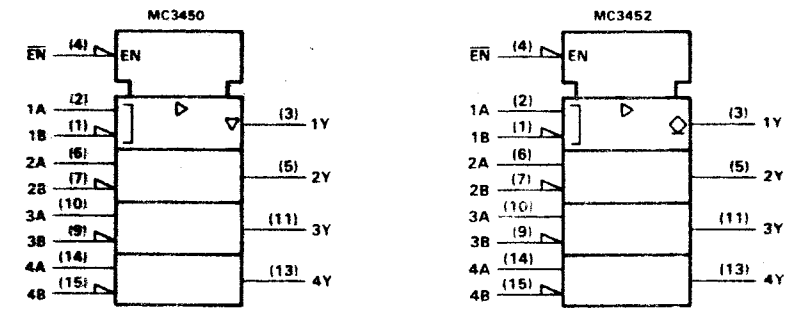
The MC3450 and MC3452 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

DIFFERENTIAL INPUTS A-B	ENABLE $\overline{EN}$	OUTPUT Y
$V_{ID} \geq 25$ mV	L	H
-25 mV < V_{ID} < 25 mV	L	?
$V_{ID} \leq -25$ mV	L	L
X	H	Z

H = high level, L = low level, ? = indeterminate,
Z = impedance (off)

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

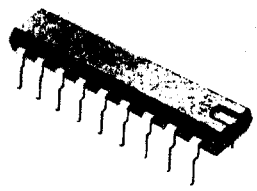
IGHT DARLINGTON ARRAYS

- EIGHT DARLINGTONS WITH COMMON EMITTERS
- OUTPUT CURRENT TO 500mA
- OUTPUT VOLTAGE TO 50V
- INTEGRAL SUPPRESSION DIODES
- VERSIONS FOR ALL POPULAR LOGIC FAMILIES
- OUTPUT CAN BE PARALLELED
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY BOARD LAYOUT

he ULN2801A -ULN2805A each contain eight arlington transistors with common emitters and tegral suppression diodes for inductive loads. ach darlington features a peak load current ting of 600mA (500mA continuous) and can ithstand at least 50V in the off state. Outputs ay be paralleled for higher current capability.

ive versions are available to simplify interfacing standard logic families: the ULN2801A is designed for general purpose applications with a current limit resistor; the ULN2802A has a 10.5KΩ input resistor and zener for 14-25V PMOS; the ULN2803A has a 2.7KΩ input resistor for 5V TTL and CMOS; the ULN2804A has a 10.5KΩ input resistor for 6-15V CMOS and the ULN2805A is designed to sink a minimum of 350mA for standard and Schottky TTL where higher output current is required.

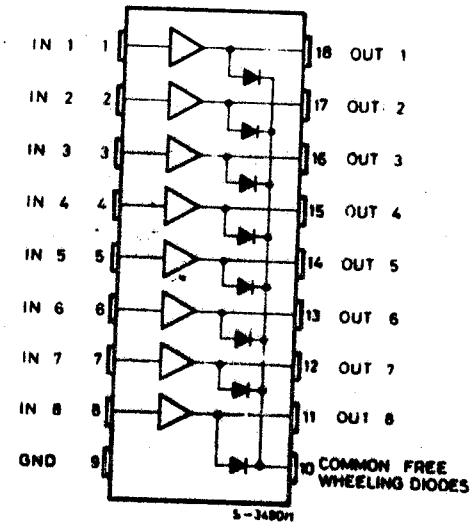
All types are supplied in a 18-lead plastic DIP with a copper lead from and feature the convenient input-opposite-output pinout to simplify board layout.



DIP-18 Plastic

CONNECTION DIAGRAM

(top view)

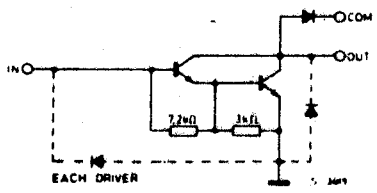


ABSOLUTE MAXIMUM RATINGS

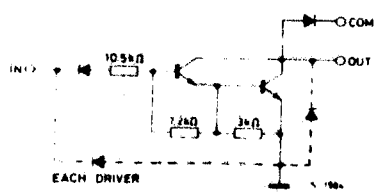
V_o	Output voltage	50	V
V_i	Input voltage for ULN 2802A, 2803A, 2804A	30	V
	for ULN 2805A	15	V
I_C	Continuous collector current	500	mA
I_B	Continuous base current	25	mA
P_{tot}	Power dissipation (one Darlington pair)	1.0	W
	(total package)	2.25	W
T_{amb}	Operating ambient temperature range	-20 to 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C

SCHEMATIC DIAGRAMS

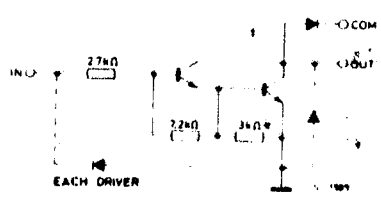
For ULN 2801A (each driver for PMOS-CMOS)



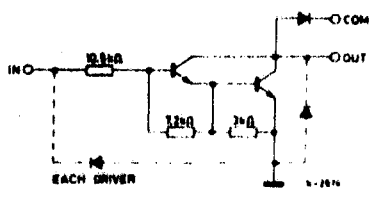
For ULN 2802A (each driver for 14-15V PMOS)



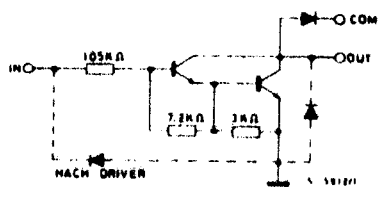
For ULN 2803A (each driver for 5V, TTL/CMOS)



For ULN 2804A (each driver for 6-15V CMOS/PMOS)



For ULN 2805A (each driver for high out TTL)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	55	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output leakage current	V_{CE} = 50V T_{amb} = 70°C V_{CE} = 50V T_{amb} = 70°C for **ULN 2802A** V_{CE} = 50V V_I = 6V for **ULN 2804A** V_{CE} = 50V V_I = 1V			50 100 500 500	µA µA µA µA	1a 1a 1b 1b
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 100 mA I_B = 250 µA I_C = 200 mA I_B = 350 µA I_C = 350 mA I_B = 500 µA		0.9 1.1 1.3	1.1 1.3 1.6	V V V	2
$I_{I(on)}$	Input current	for **ULN 2802A** V_I = 17V for **ULN 2803A** V_I = 3.85V for **ULN 2804A** V_I = 5V V_I = 12V for **ULN 2805A** V_I = 3V		0.82 0.93 0.35 1 1.5	1.25 1.35 0.5 1.45 2.4	mA mA mA mA mA	3
$I_{I(off)}$	Input current	T_{amb} = 70°C I_C = 500 µA	50	65		µA	4
$V_{I(on)}$	Input voltage	for **ULN 2802A** V_{CE} = 2V I_C = 300 mA for **ULN 2803A** V_{CE} = 2V I_C = 200 mA V_{CE} = 2V I_C = 250 mA V_{CE} = 2V I_C = 300 mA for **ULN 2804A** V_{CE} = 2V I_C = 125 mA V_{CE} = 2V I_C = 200 mA V_{CE} = 2V I_C = 275 mA V_{CE} = 2V I_C = 350 mA for **ULN 2805A** V_{CE} = 2V I_C = 350 mA			13 2.4 2.7 3 5 6 7 8 2.4	V V V V V V V V V	5
h_{FE}	DC forward current gain	for **ULN 2801A** V_{CE} = 2V I_C = 350 mA	1000			-	2
C_I	Input capacitance			15	25	pF	–
t_{PLH}	Turn-on delay time	0.5 V_I to 0.5 V_o		0.25	1	µs	–
t_{PHL}	Turn-off delay time	0.5 V_I to 0.5 V_o		0.25	1	µs	–
I_R	Clamp diode leakage current	V_R = 50V T_{amb} = 70°C V_R = 50V			50 100	µA µA	6
V_F	Clamp diode forward voltage	I_F = 350 mA		1.7	2	V	7

TEST CIRCUITS

Fig. 1a

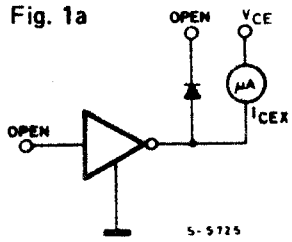


Fig. 1b

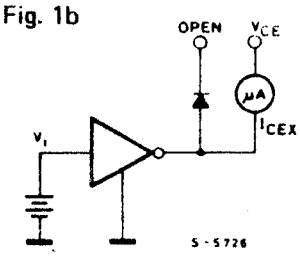


Fig. 2

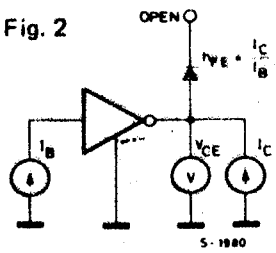


Fig. 3

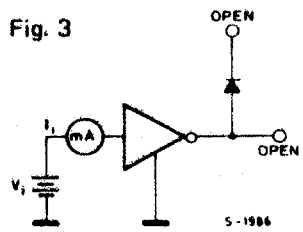


Fig. 4

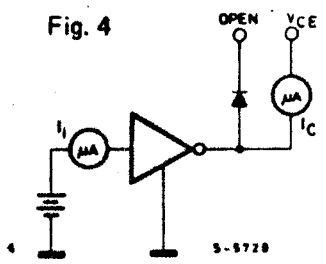


Fig. 5

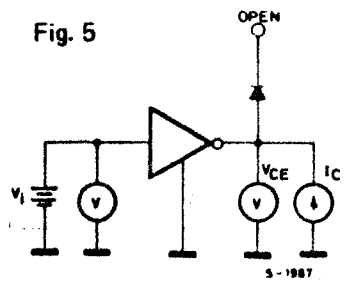


Fig. 6

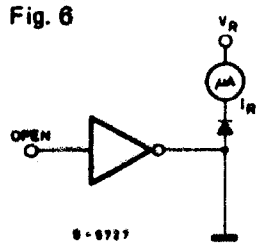


Fig. 7

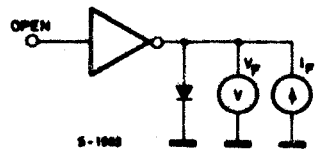


Fig. 8 - Collector current as a function of saturation voltage

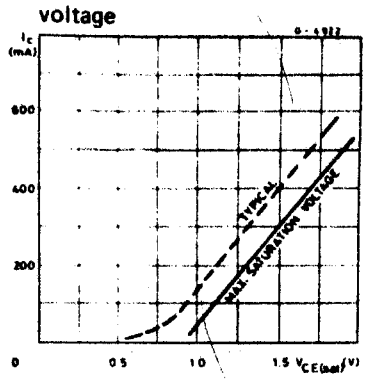


Fig. 9 - Collector current as a function of input current

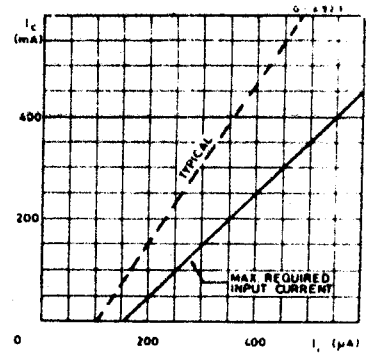


Fig. 10 - Allowable average power dissipation as a function of ambient temperature

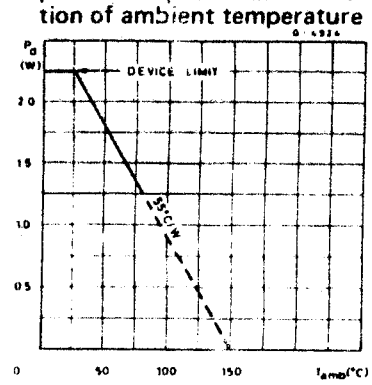


Fig. 11 - Peak collector current as a function of duty cycle

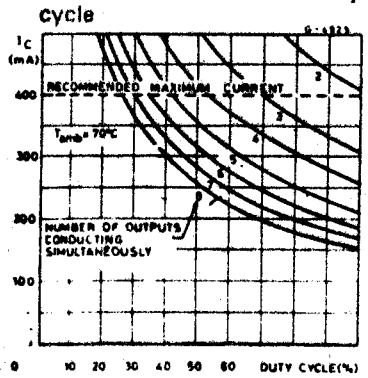


Fig. 12 - Peak collector current as a function of duty cycle

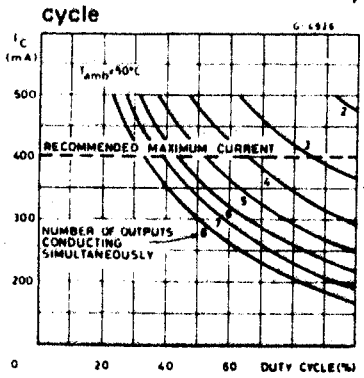


Fig. 13 - Input current as a function of input voltage (for ULN 2802A)

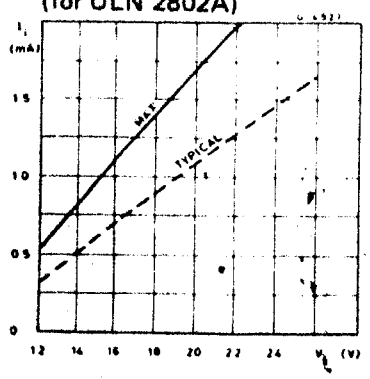


Fig. 14 - Input current as a function of input voltage (for ULN 2804A)

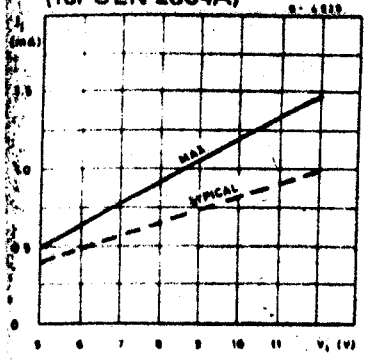


Fig. 15 - Input current as a function of input voltage (for ULN 2803A)

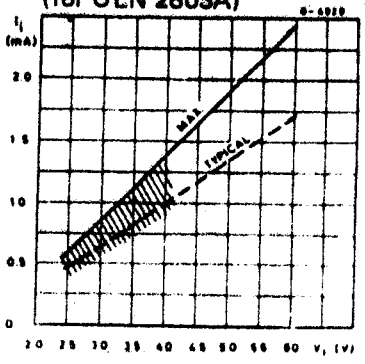


Fig. 16 - Input current as a function of input voltage (for ULN 2805A)