DIRECT SEQUENCE SPREAD SPECTRUM MULTIPLE ACCESS

P-1310

PROJECT REPORT

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COIMBATORE - 641 006

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DIRECT SEQUENCE SPREAD SPECTRUM MULTIPLE ACCESS

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in partial fulfilment for the award of the Degree of Bachelor of Engineering in Electronics and Communication Engineering Branch of the Bharathiar University, Coimbatore - 641 046 during the academic year 1994 - 95

GUIDE

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CONTENTS

CONTENTS

SYNOPSIS

SYNOPSIS

Spread Spectrum Communications are one of the vital areas of communication. The DSSS systems involves the Direct Sequence type of modulation. The Spreading of data signal is achieved by EX-OR addition with a randomly generated code sequence with a rate of 1 Mbs of length 63 bits. The code is generated with a shift register IC 74164. The data of length 15 bits and rate 16 Kbs is generated with IC 7495. The special feature of the code and data generator is that the zero avoiding logic is incorporated in both.

The performance of the system is analysed in the presence of interference in the DS-SS Receiver. A threshold logic is used to detect received bit in the presence of interference. The signal despreading is achieved by an EX-OR gate. The salient feature of the DS-SS receiver designed is that it incorporates an error detecting logic and the error is indicated by a frequency counter.

Hence here several users can occupy the same bandwidth simultaneously. Each user uses a distinct PN code sequence which allows only tthe receiver with an identically synchronised code sequence to receive the message. Any interfering signal or transmission using a different sequence will be rejected.

INTRODUCTION

CHAPTER ONE

INTRODUCTION

Normally, the communication systems are concerned with the efficiency of utilizing the signal energy and bandwidth. These are legitimate concerns, and in most communication systems, are of paramount importance. There are situations, however, in which it is necessary for the system to resist external interference, to operate with a low energy spectral density, to provide multiple access capability without external control, or to make it difficult for unauthorized receivers to observe the message. In such a situation, it may be appropriate to sacrifice the efficiency aspects of the system in order to enhance these features. Spread spectrum techniques offer one way to accomplish these objectives.

1.1 DEFINITION

The spread spectrum system is one, in which the transmitted signal is spread over a wide frequency band, much wider, infact, than the minimum bandwidth required to transmit the information. In other words spread spectrum system takes a base band signal with a band width of only few KHZ and distributes it over a band that may be many MHZ wide. This spreading is accomplished by means of a spreading signal, oftenly called a code signal which is independent of the data. Thus the spread spectrum technique is simply the

CODE DIVISION MULTIPLE ACCESS TECHNIQUE . A typical example of the spread spectrum modulation is that of conventional frequency modulation in which deviation ratios greater than one are used. The RF spectrum product is much wider than the transmitted information. At the receiving side of the spread spectrum system, despreading (recovering the original data) is accomplished by the correlation of the received signal with a synchronized replica of the spreading signal used to spread the information.

1.2 ADVANTAGES

There are many reasons for spreading the spectrum, and if done properly, a multiplicity of benefits can occur simultaneously. Some of these are,

* **Anti-jam capability - Particularly for narrow band jamming.**
* **Interference rejection.**
* **Multiple access capability.**
* **Covert operation or low probability of interrupt.**
* **Secure communication.**
* **Improved spectral efficiency - in special circumstances.**
* **Ranging.**

Although the current applications for spread spectrum continue to be primarily for military communications, there is a growing interest in the use of this technique for mobile

radio networks (Radio Telephony, Packet Radio and Amateur Radio), timing and positioning systems, some specialised applications in satellites etc., While the use of spread spectrum, naturally means, that each transmission utilizes a large amount of spectrum, this may be compensated for by interference reduction capability inherent in the use of spread spectrum techniques, so that a considerable number of users might share the same spectral band.

Types

Spread spectrum techniques can be broadly classified into four main types.

They are

* **Direct Sequence Technique**
* **Frequency Hopping Technique**
* **Time Hopping Technique**
* **Hybrid Systems**

1.3 DIRECT SEQUENCE TECHNIQUE

Direct sequence spread spectrum (DS-SS) system is a system, in which, a fast pseudo randomly generated sequence causes phase transitions in the carrier, containing data. These systems are the best known and most widely used ones. This is, because, of their relative simplicity, from the stand point, that they do not require a high speed, fast-settling frequency synthesizer. This system is an example of averaging system. An Averaging system is one, in which a

reduction of interference takes place, because the interference can be averaged over a large time interval.

Today, direct sequence modulation is being used for communication systems and test systems, and even laboratory test equipment capable of producing a choice of a number of code sequences or operating modes are available. It is reasonable to expect, that direct sequence modulation will become a familiar form of modulation in many areas in future. Even now, commercial applications of such systems are being contemplated.

1.4 FREQUENCY HOPPING TECHNIQUE

Frequency hopping is a method in which the carrier is caused to shift frequency in a pseudo random way. Frequency hoping modulation is more accurately termed as "**Multiple - Frequency, Code - Selected, Frequency Shift Keying**". It is nothing more than FSK (Frequency Shift Keying), except that the set of frequency choices is greatly expanded. Simple FSK uses only two frequencies; for example f1 is sent to signify a "mark", f2 to signify a "space". Frequency hoppers on the other hand often have thousands of frequencies available. One real system has 2^{20} discrete frequency choices, randomly chosen, each selected on the basis of a code in combination with the information transmitted. The number of frequency choices and the rate of hopping from frequency to frequency in any frequency hopper is governed by the requirements

placed on it for a particular use.

1.5 TIME HOPPING TECHNIQUE

Time Hopping system is a system,in which bursts of signal are initiated at pseudo random times. Time hopping is the familiar pulse modulation ie, the code sequence is used to key the transmitter ON and OFF. Transmitter ON and OFF times are therefore pseudo random,like the code, which can give an average transmit duty cycle of as much as 50%. The fine point of difference separating time-frequency and plain-frequency hoppings is that in frequency hopping systems, the transmitted frequency is changed at each code chip time, whereas a time - frequency hopping system may change frequency only at one or zero transitions in the code sequence. Any signal source that can pulse modulate, capable of following code waveforms, is eligible as a time hopping modulator.

Time hopping may be used to aid in reducing interference between systems in time division multiplexing. This time hopping system is also an avoidance system. Hence, reduction of interference occurs as the signal is made to avoid the interference for a large fraction of time.

1.6 HYBRID SYSTEMS

In Hybrid spread spectrum systems,a combination of CDMA and TDMA is used. The messages are sent through a SSMA modulator where messages are coded, encrypted, added and

correlated to another signal such that messages acquire a larger bandwidth. The codes which generate the encrypted messages are of equal length, energy and are distinct. The encrypted messages are sent to the receiver using TDMA. The received signal is processed through a band of spread spectrum demodulators, where the exact replica of the code is stored to make the inverse operation to extract the message. The encrypted message is processed through the TDMA demodulator. The hybrid system may use either a frequency hopping system or a direct sequence. The direct sequence hybrid system provides the message privacy while the frequency hopping hybrid system would ensure antijamming. Thus a combination of these two methods would provide a secure, reliable and efficient system. In particular, it provides antijamming capabilities of the commercial satellites as well as the data security of the military satellites.

DS-SS TECHNIQUE

CHAPTER TWO

DS-SS TECHNIQUE

In the DS-SS system, several users occupy the same bandwidth simultaneously. However, each user uses distinct pseudo noise (PN) code sequence which allows only the receiver with an identically synchronized code sequence to receive the message. Any interfering signal or transmission using a different sequence will be rejected. The working principle of a DS-SS transmitter and receiver is given below.

2.1 WORKING PRINCIPLE

A typical direct sequence transmitter is illustrated in fig.2.1. Note that, it contains a PN code generator which generates the pseudo noise sequence. The binary output of this code generator is added to the binary message (modulo - 2 addition) and the sum is used to modulate the carrier. The modulation in this case is biphase or phase reversal modulation so that the output is simply a phase shift keyed signal.

Pseudo noise generators are periodic, in that, the sequence that is produced, repeats itself after some period of time. Such a periodic sequence is portrayed in fig.2.2. The smallest time increment in the sequence of duration t1, is known as a 'time chip'. The total period consists of N time

chips. When the code is generated by a maximal linear PN code generator, the value of N is $2^n - 1$, where n is the number of stages in the code generator. An important reason for using shift register codes is that they have very desirable auto correlation properties. The auto correlation function of a typical PN sequence is shown in Fig.2.3. Note that on a normalized basis, it has a maximum value of one, that repeats itself every period, but in between these peaks, the level is at a constant value of -(1/N). If N is a very large number, the auto correlation function will be very small in this region. Another reason for using shift register codes is that the period of PN sequence can easily be made very large.

The receiver for a PN signal must perform three different functions, namely, detect signal presence, despread the signal, and demodulate the message. The detection and despreading operations can be either active or passive. Active methods involve searching for the signal presence in both time and frequency, tracking and sequencing after it has been acquired, despreading the signal with a correlator, and then demodulating the message in the usual way. Passive methods, on the other hand only require that the signal be searched for in frequency, only as the passive system will respond to the signal whenever it occurs. The despreading is accomplished in a matched filter, rather than a correlator

and the demodulation is again performed in the usual manner.

Fig.2.4 illustrates the essential parts of a direct sequence receiver. The despreader accomplishes the task of multiplying the incoming signal with a locally generated PN sequence, when these are aligned in time, the output is simply the message, which is at a much lower frequency and thus can be filtered in narrow band filter. This is followed by the message demodulation. The output of the narrow band filter can also be used as a means of controlling the clock that drives the PN generator to make sure, that, it stays in step with the incoming signal.

2.2 ADVANTAGES OVER OTHER TYPES

DS-SS technique explained above has a lot of advantages over the other two types, namely, frequency hopping and time hopping. Some of them are listed below:

* **Hardware implementation is simple.**
* **Best noise and anti-jam performance.**
* **Most difficult to detect.**
* **Best discrimination against multipath.**
* **Do not require a high speed - fast settling frequency synthesizer.**

Because of these advantages, today, direct sequence modulation is being used for communication systems and test systems.

2.3 DESIGN PARAMETERS

In designing the DS-SS system, many factors have to be considered. Some of them are given below.

An asynchronous system model was assumed ie, communication was assumed to be between independent users. It was also further assumed that the channel was a additive white Gaussian noise channel. From the stand point of error - rate performance, the number of users is the limiting factor. This is due to the effect of other users on the receiver, matched to the desired signal.

In order to conceal the information data spectrum of pseudo random code, the condition $Ts < NTc$ had to be satisfied, where N is the length of the pseudo random code, and Tc and Ts are the chip and data periods, respectively. Satisfying this condition, also ensures, that the spectral density of the data and code modulated signals would have smooth spectral envelope, thus concealing certain characteristics of the pseudo random code used.

An important parameter, that is, sometimes useful in specifying the performance of a spread spectrum signal in the presence of interference, is known as the processing gain.

The processing gain (PG) is frequently defined as the ratio of the signal bandwidth to the message bandwidth. Thus,

$$PG = \frac{Bs}{Bm} = \frac{2tm}{t1}$$

Some authors prefer to define the processing gain of the DS-SS as, a ratio of chip rate to the message bit rate ie, PG = C/R. This value is just one half of that given in the above equation.

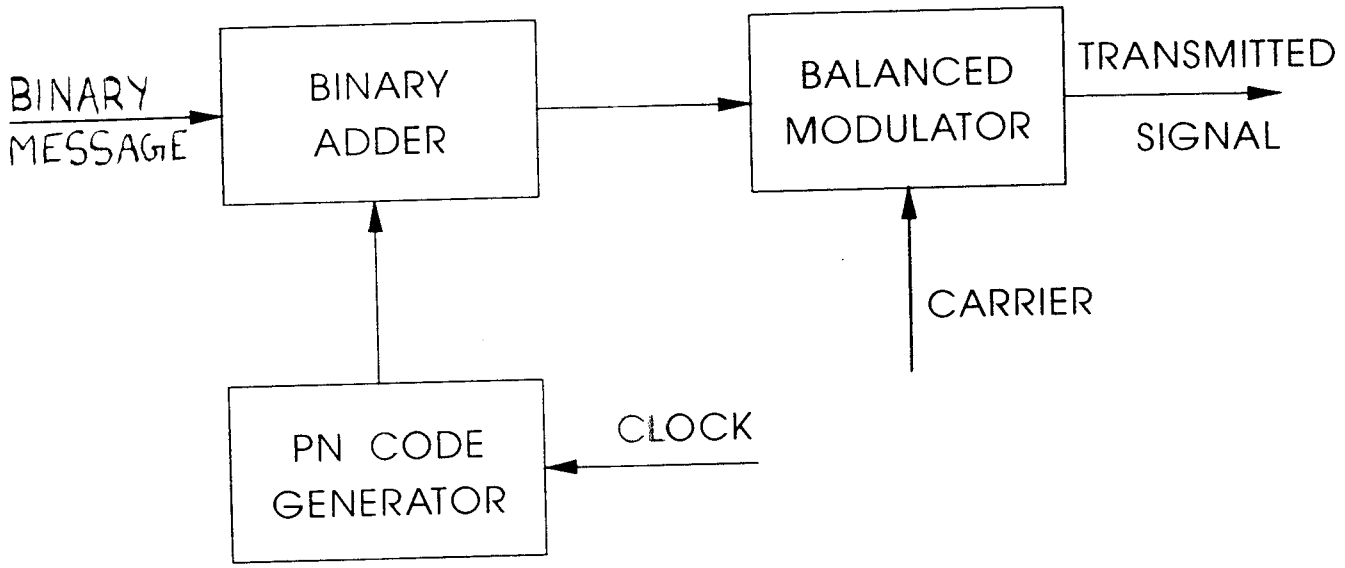


FIGURE - 2.1
DIRECT SEQUENCE TRANSMITTER

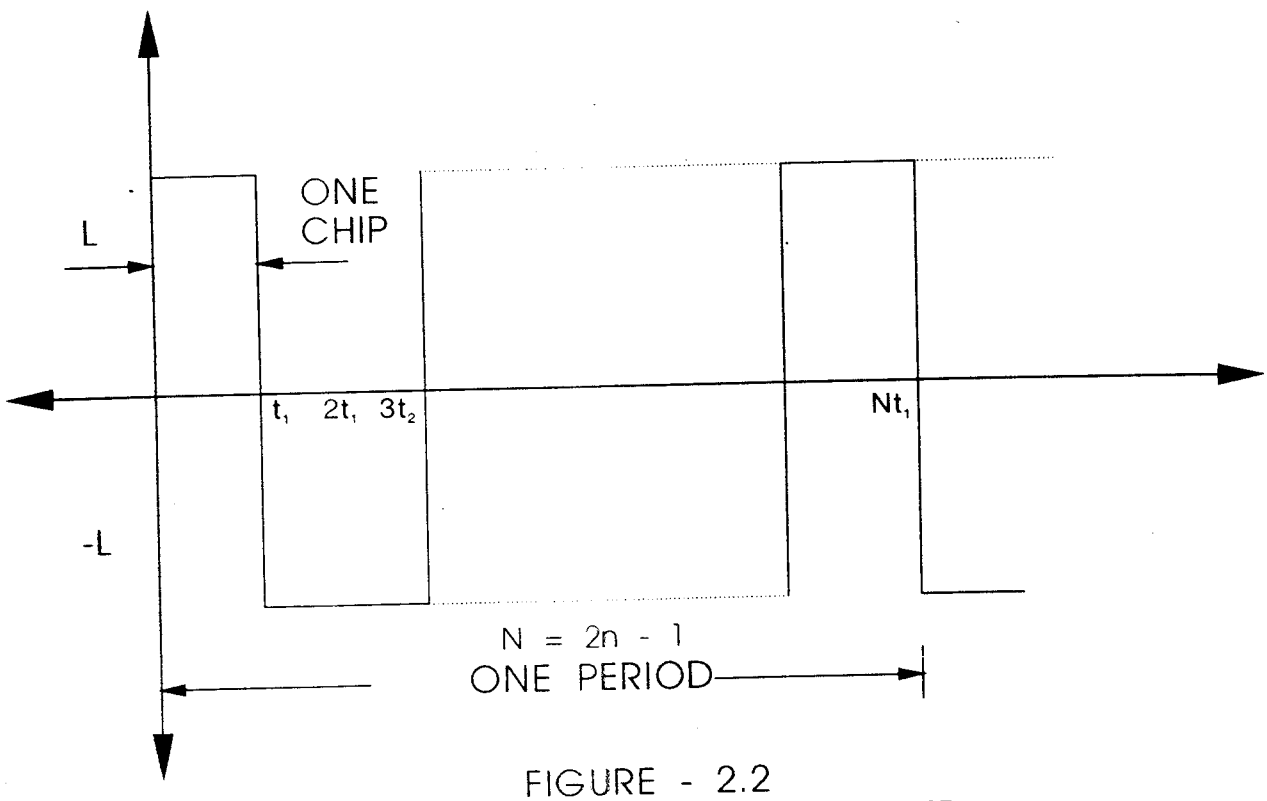


FIGURE - 2.2
DIRECT SEQUENCE TRANSMITTER

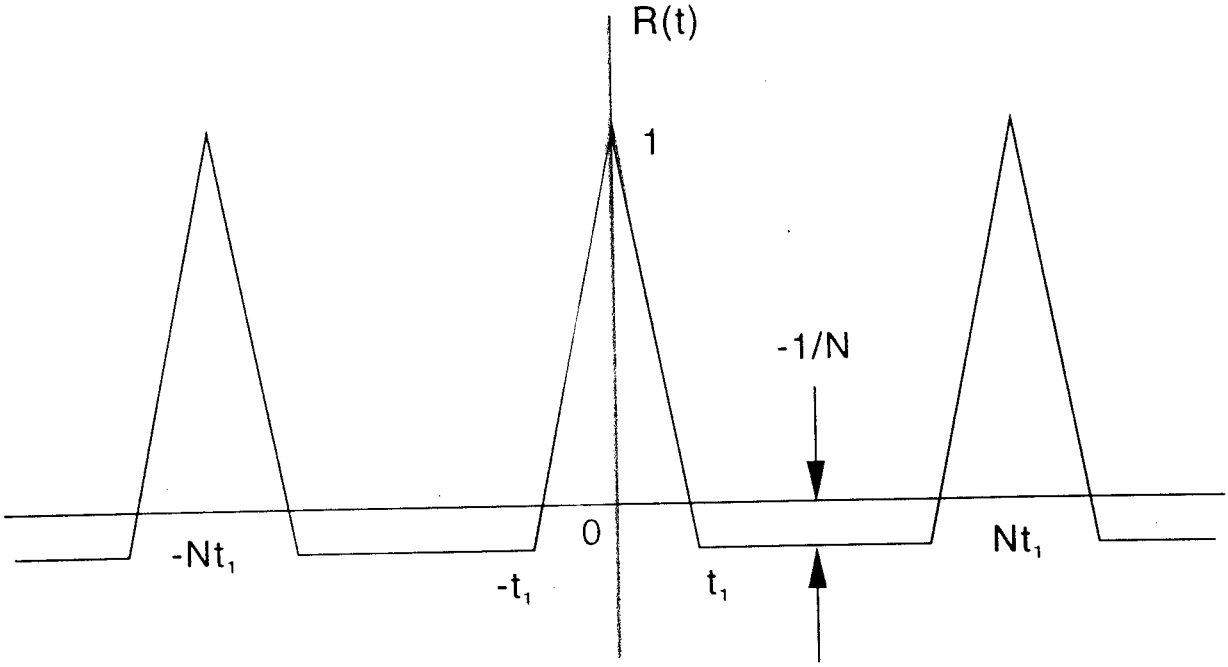


FIGURE - 2.3
AUTO-CORRELATION FUNCTION OF PN SEQUENCE

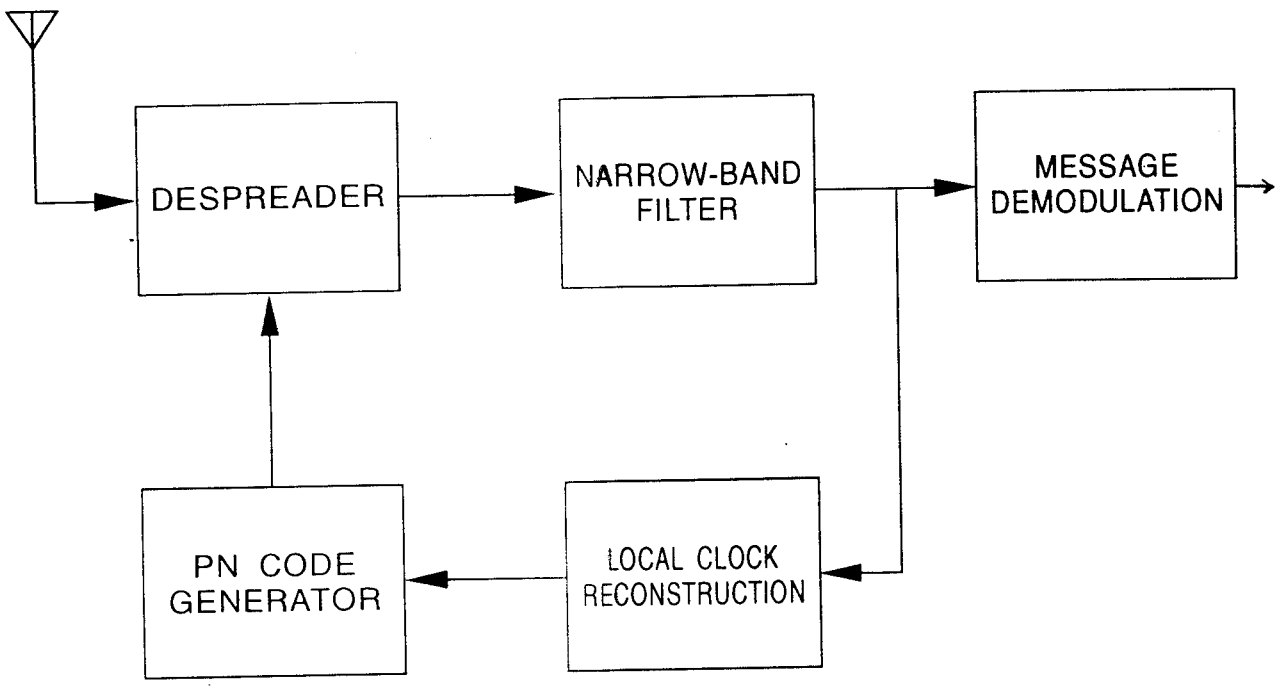


FIGURE 2.4
DIRECT SEQUENCE RECEIVER

DS-SS TRANSMITTER

CHAPTER THREE

DS-SS TRANSMITTER

DS-SS Transmitter consists of four main blocks. They are

* **Clock Generator**
* **Code Generator**
* **Data Generator**
* **Spreader**

These four blocks are connected as shown in the block diagram in Fig.3.1 to form the DS-SS transmitter.

The design and implementation of various blocks are as follows:

3.1 DESIGN

According to the design parameters illustrated in the previous chapter, we have to design the DS-SS transmitter.

One important design parameter mentioned in the previous chapter is the processing gain. To provide a good antijam performance, the system is designed with a processing gain of 18 dB.

$$PG = \frac{\text{code rate}}{\text{Data rate}} = \frac{C}{R}$$

Another condition to be satisfied is Ts <= NTc where Ts and Tc are data and chip periods respectively. N is the length of the code.

Let the Code Rate C = 1 Mbs

Since, PG = 10log(C/R) = 18, R = 16 KHZ

Therefore, Ts = 1/16K = 62.5 microsec.

Since, Ts <= NTc,

$62.5 * 10^{-6} <= N * 1$ microsec.

$N >= 62.5$

Therefore, Let $N = 2^m - 1 = 2^6 - 1 = 63$

Satisfying the above two conditions we have designed.

a. Code Rate C = 1 Mbps

b. Data Rate R = 16 Kbps

c. Length of the code N = 63

d. Length of the data L = 15

Now both the conditions mentioned above are satisfied.

IMPLEMENTATION:

Block diagram of the DS-SS transmitter is given in Fig.3.2 . The block diagram is self explanatory. A 2 MHZ clock is first generated and then divided by two to get 1 MHZ clock. This is given as the clock to the code generator. In the code generator, a zero - avoiding logic is incorporated. From the code, a particular sequence is detected. The sequence repeats itself at a frequency of 16 KHZ. This is given as the clock to the data generator. Here also a zero avoiding logic is incorporated. Code generated from the code generator and data generated from the data generator are given to the spreader. The output of the

spreader is the transmitted DS-SS signal. The detailed explanation of various blocks the DS-SS transmitter are as follows:

3.2 CLOCK GENERATOR

A 2 MHZ clock is generated using an Astable Multivibrator. The astable multivibrator is designed using NAND gates (7400) and suitable values of resistors and capacitors. The frequency of the clock is given by the formula,

$$f = \frac{1}{2RC}$$

The values of R and C are determined to be

R = 220 ohms

C = 1 nf

This is illustrated in Fig. 3.3

This 2 MHZ clock is divided by 2 to get 1 MHZ clock. This is done by using a 'D' flip flop (7474). Here 'Q' output is given to the 'D' input. pins CLR' and RSET' are left unused. We get 1 MHZ clock at the 'Q' output. This 'D' flip-flop is positive edge triggered, that is, the transfer of information from data input to the output occurs at the positive edge of the clock pulse. This is given in Fig.3.4.

3.3 CODE GENERATOR

We are using maximal - Length Linear Shift Register Sequence (m sequence) as the code sequence. The m sequences,

3.4 DATA GENERATOR

Here also 'm' sequence is generated and used as the data. For our purpose, we need a data of length 15 at a rate of 16 Kbps. Therefore the length of the shift register is to be 4.

Here we have chosen 7495 which is a 4 bit shift register with serial and parallel synchronous operating modes. It has serial data (Ds) and four parallel data (D0 - D3) inputs and four parallel outputs. The serial or parallel mode of operation is controlled by mode select input (s) and two clock inputs (CP1' and CP2'). The pin diagram, logic diagram and characteristics are given in Appendix.

Number of sequences possible is two. Tappings from 1st and 4th are taken and EXored. The output is given as the serial input. Here also a zero avoiding circuit is incorporated. The circuit is given in Fig.3.6.

For getting data at a rate of 16 Kbps, we have to use a clock of 16 KHZ. This is generated from the code itself. In the code we are detecting a particular sequence, in our case 111 111. This sequence repeats itself at a frequency of 16 KHZ. The sequence detecting circuit is given in Fig.3.7. The output of this circuit is given as clock to the shift register. Thus we are getting a data of length 15 at a rate of 16 Kbps.

have a length that is defined by,

$$N = 2^{m} - 1 \quad m = 1,2,3,.....$$

Thus some typical short - Length sequences are

$$N = 7,15,31,63,127,255,....$$

The m sequences are most commonly used because they are easily generated in shift registers with the relatively small number of stages. It requires only m stages of shift registers to generate an N sequence.

In our design we are choosing m = 6. Hence N = 63. There are six different sequences possible by taking different tapings.

Here we are using 74164 serial in parallel out shift register. The pin configuration, logic diagram and characteristics of 74164 are given in Appendix. 74164 is an 8 bit shift register. Since we need only 6 bits, the last 2 bits are left unused. The first and sixth bits are Ex-ored and given as serial input.

When all the bits in the shift register becomes zero, circuit won't work. To avoid this condition, zero avoiding logic is included. The purpose of this circuit is to introduce a 'one' as serial input when all outputs are zero. This circuit is given in Fig.3.5.

1 MHZ clock generated is given as the clock to the shift register. The output is the required code of length 63 and rate 1 Mbps.

3.5 SPREADER

The spreader is nothing but an EX-OR gate. The code at the rate of 1 Mbps and the data at the rate of 16 Kbps are given as two inputs. These two are modulo - 2 added. The output is the DS-SS signal. The circuit is given in Fig.3.8. Pin configuration, logic diagram and characteristics of 7486 EX-OR gate are given in Appendix.

These various parts of the transmitter are suitably interconnected to form the DS-SS transmitter. . The whole circuit diagram is given in Fig.3.9.

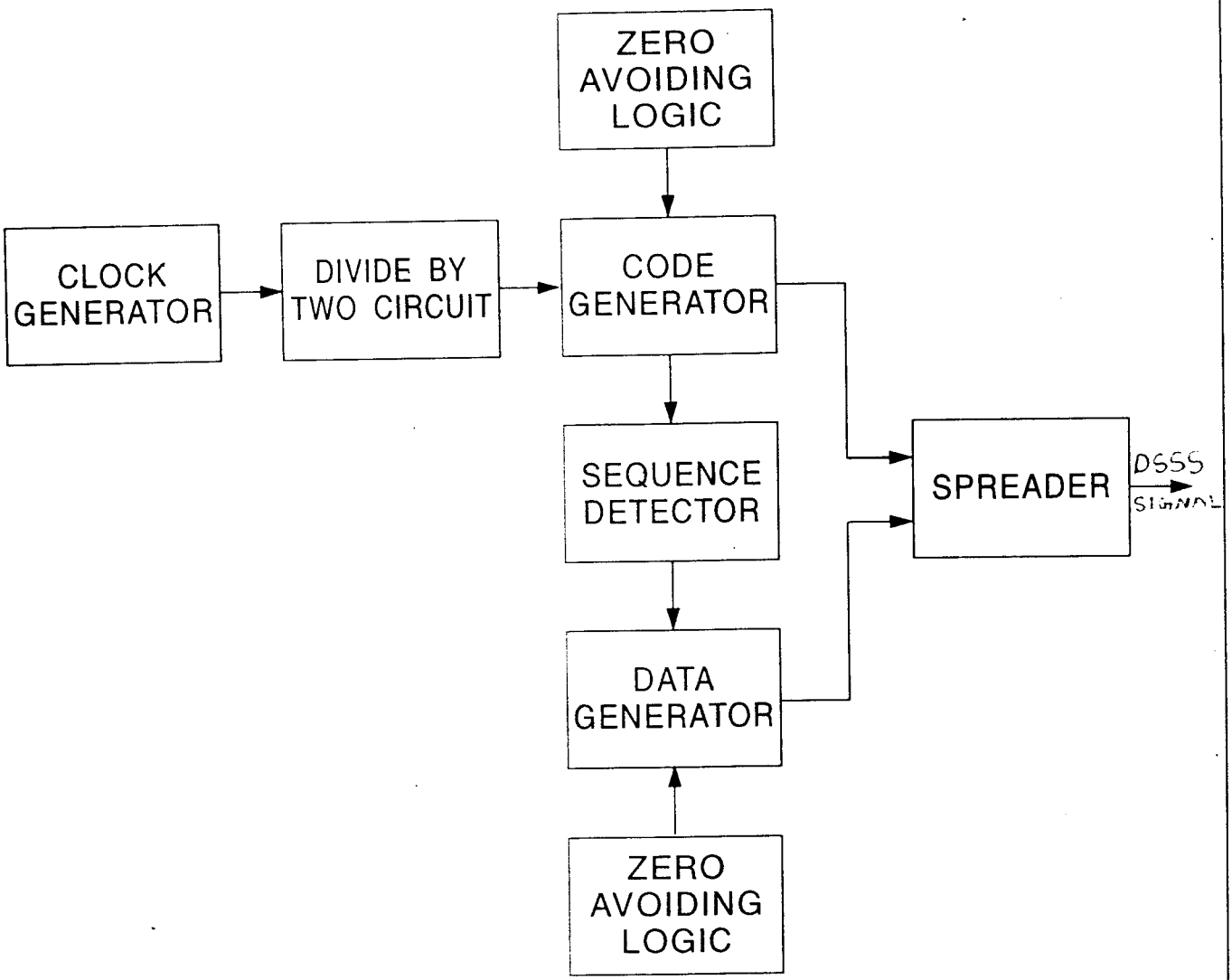


FIGURE - 3.1

DS-SS TRANSMITTER :- BLOCK DIAGRAM

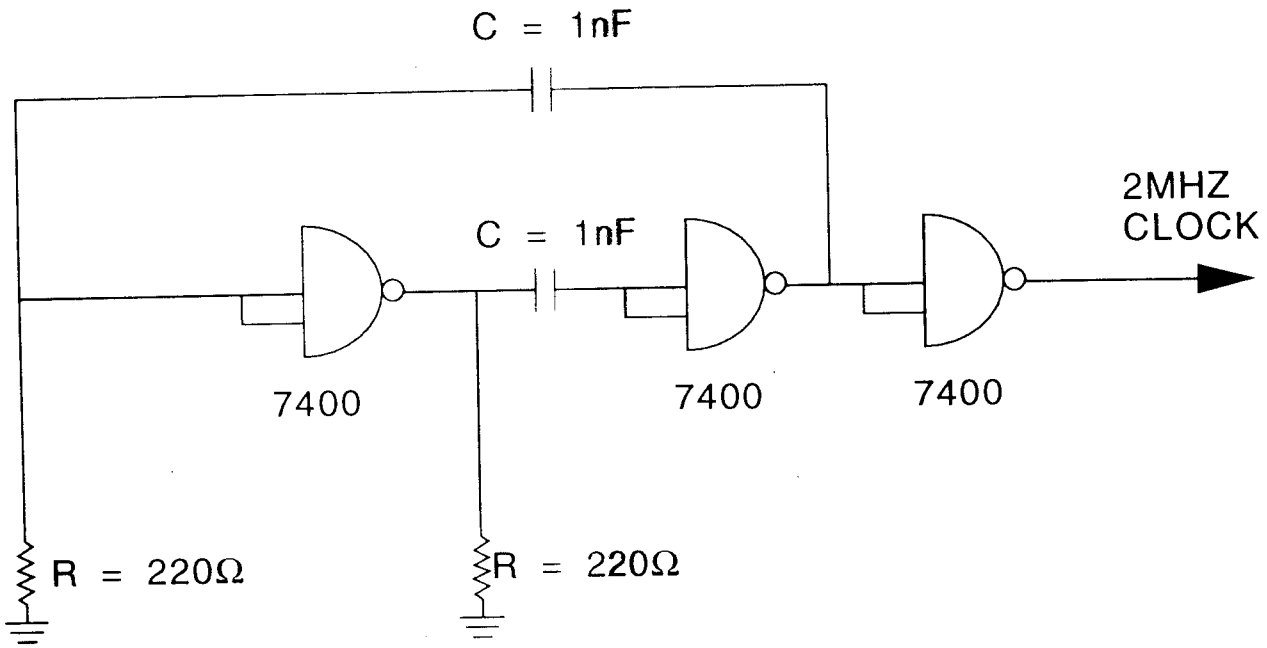


FIGURE - 3.3
CLOCK GENERATOR

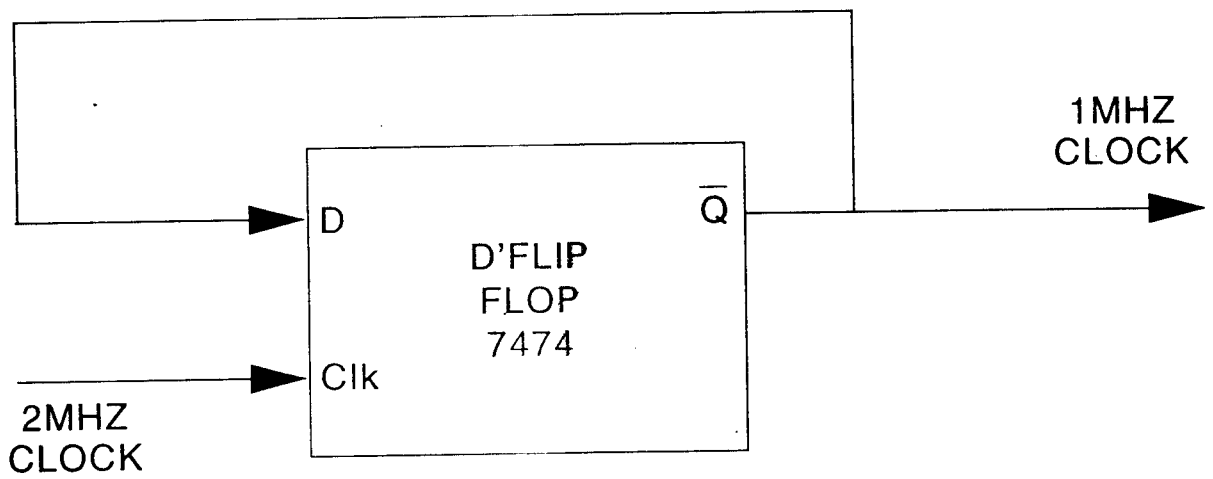


FIGURE - 3.4
DIVIDE BY TWO CIRCUIT

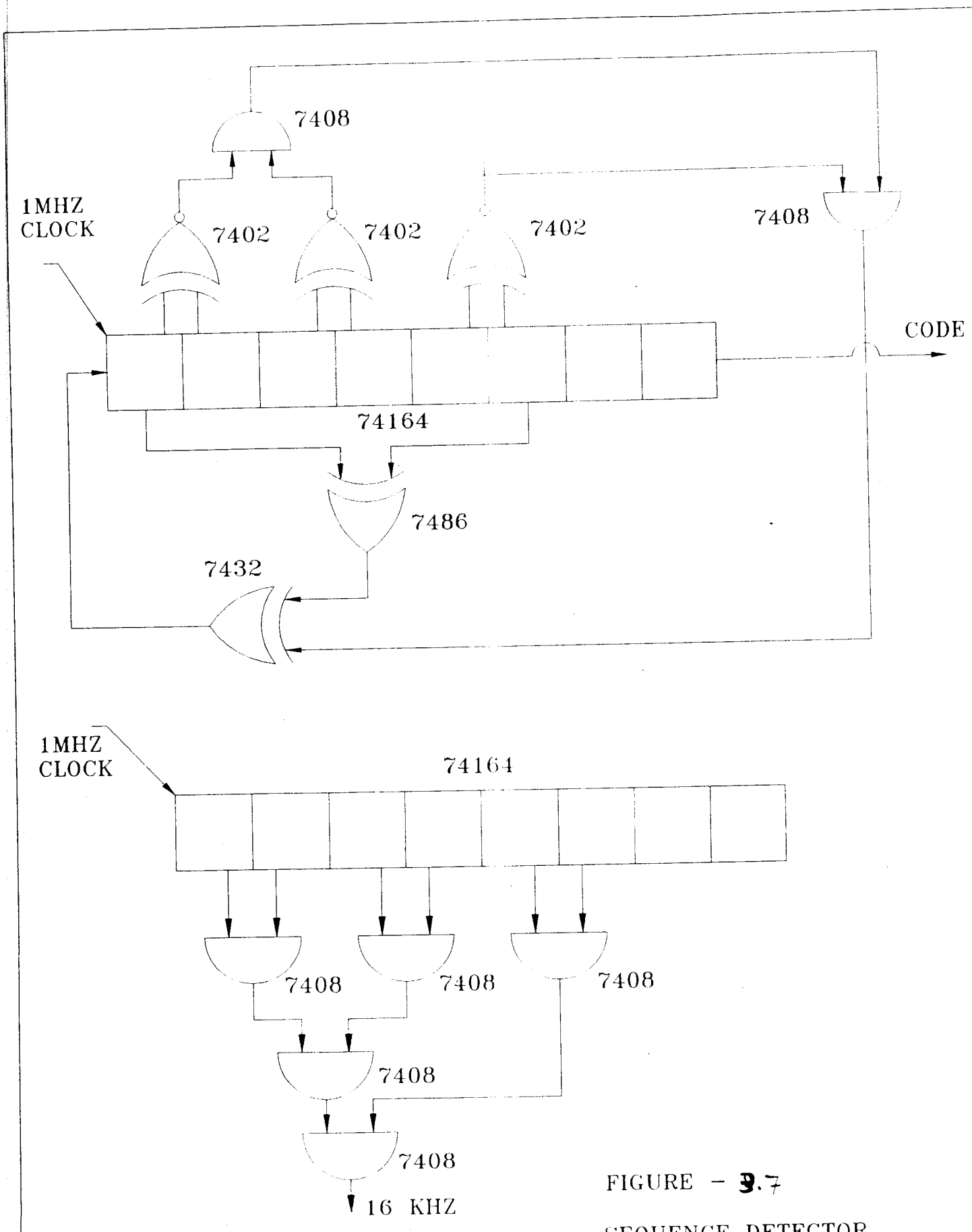


FIGURE – 3.7

SEQUENCE DETECTOR

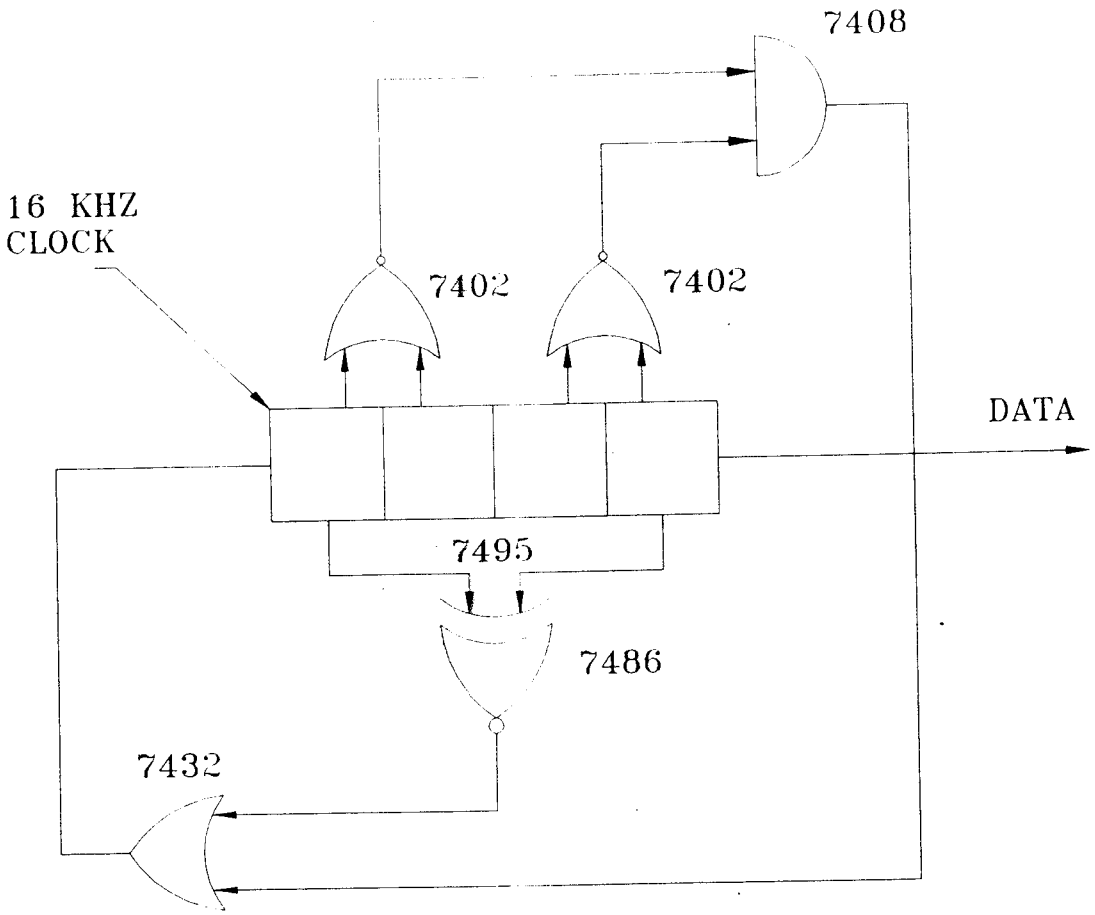


FIGURE – 3.6
DATA GENERATOR

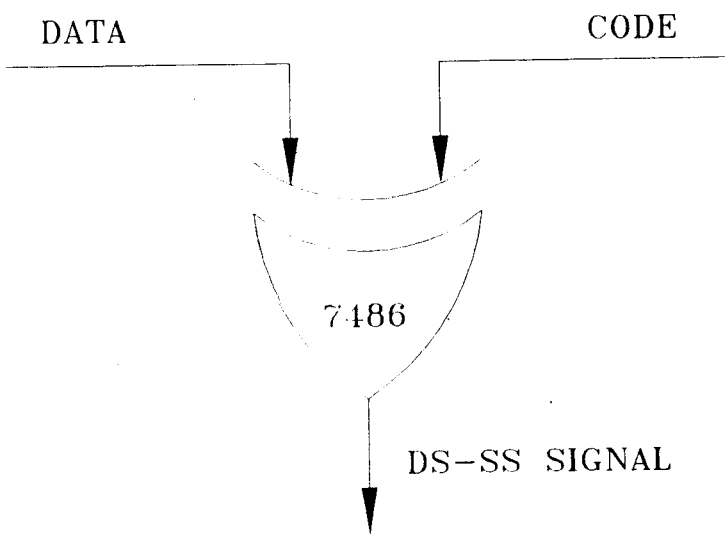


FIGURE – 3.8
SPREADER

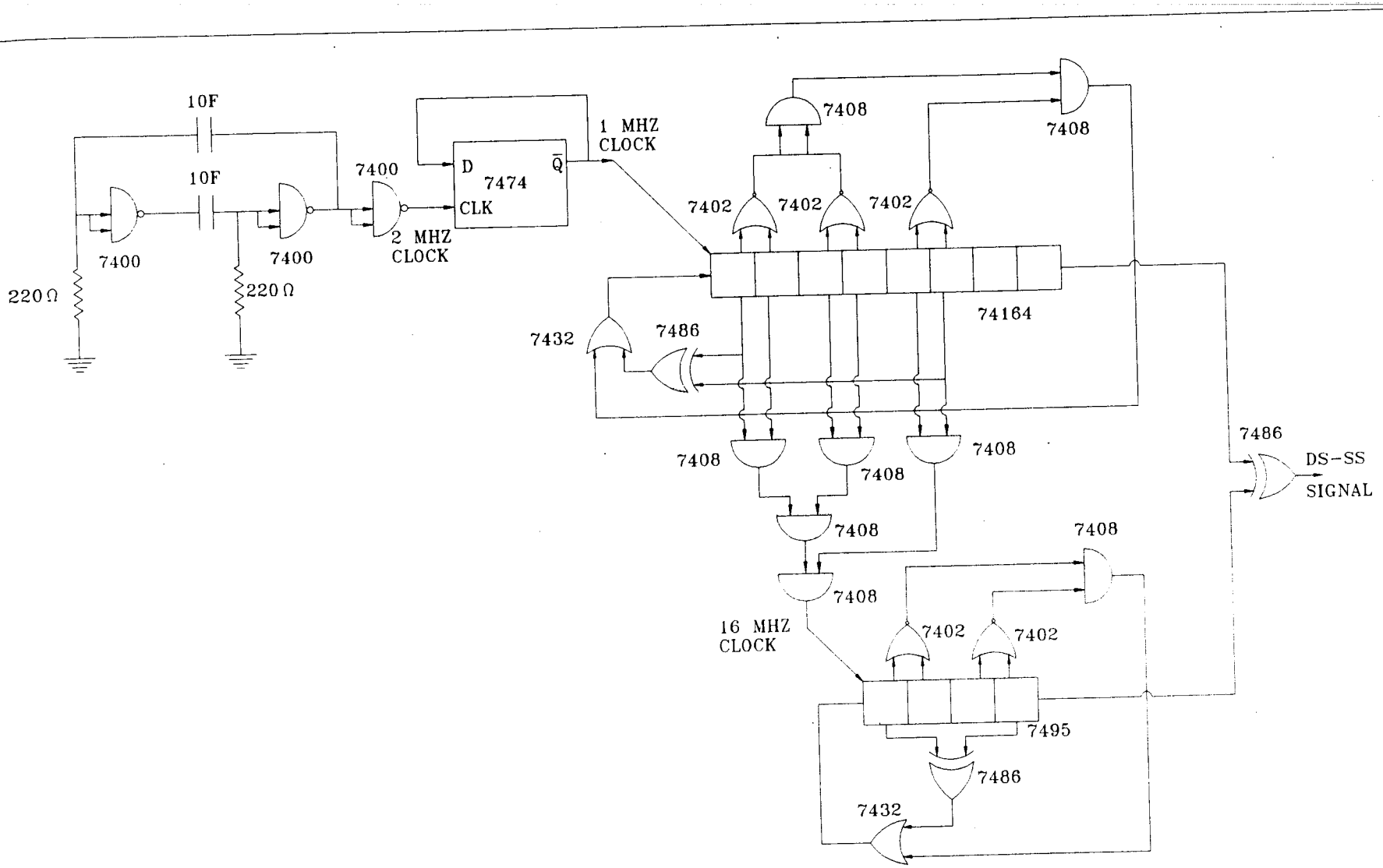


FIGURE - 3.9

DS-SS TRANSMITTER :- CIRCUIT DIAGRAM

DS-SS RECEIVER

CHAPTER FOUR

DS-SS RECEIVER

In the receiver, we are not generating a separate code. Instead, we are using the same code which is used in the transmitter for despreading. This is because, if we generate a separate code in the receiver, the synchronization is very difficult to achieve. We have to use acquistion and tracking techniques to achieve synchronization. This involves a lot of hardware. Hence we are using the same code which is used in the transmitter for despreading.

DS-SS receiver consists of five main blocks.

They are

* **Interference Generator**
* **Liner op-amp adder**
* **Comparator**
* **Despreader**
* **Frequency counter**

The design and implementation of various blocks are given below:

4.1 DESIGN

In the receiver, we are mainly analyzing the performance of system in the presence of interference. For this, an interference code of suitable length and rate should be designed. Let,

Length of interference code = 63

Rate of interference code = 1 Mbps

For adding this signal with the received DS-SS signal, an adder should be designed. We can use 741 op-amp adder working in Non-inverting mode.

$$\text{Output } Vo = \left(\frac{E1 + E2}{2}\right) * \left(1 + \frac{Rf}{R1}\right)$$

We need Vo = E1 + E2.

E1 ---> Received DS-SS signal

E2 ---> Interfering signal

For designing the comparator, we have to choose a suitable comparator IC, which is capable of comparing at a rate of 1 Mbps. LM 311 is such a comparator. We need a threshold voltage of 2.5 V. This can be derived from a suitable resistor network.

These are all the design parameters to be considered in designing the receiver. The block diagram of DS-SS receiver is given in Fig.4.1.

IMPLEMENTATION

The received DS-SS signal is added with the interference signal generated from an interference generator. This signal is compared with the threshold of 2.5 V in a comparator. If the signal is above threshold, output is '1'. If it is below the threshold, output is '0'. For making this signal suitable for despreading, it has to be passed through a 'D' flip-flop fed by a clock of 1 MHZ. The signal is

despread using the code which is used in the transmitter, using EX-OR gate. This received data must be compared with the original transmitted data to find out any error. For this, both data should be at synchronization. For making this, both data are passed through two 'D' flip flops having the same clock of 16 KHZ. These data are then compared using an EX-OR gate. The output is given to the frequency counter. The counter increments by '1' whenever an error occurs. The detailed explanation of various blocks are as follows:

4.2 INTERFERENCE GENERATOR

Interference generator is similar to the code generator used in the transmitter, except, that the tappings are taken from 5th and 6th outputs of the shift register 74164.

(Note that six different sequences can be generated using a six stage shift register).

These two outputs from the tappings are EXored and given as serial input data to the shift register. Here also, a zero - avoiding logic circuit is incorporated to avoid the condition of continuous zeroes. A clock of 1 MHZ is given to 74164. Now length of the interference code is 63 and rate is 1 Mbps. This circuit is shown in Fig.4.2.

4.3 ADDER

The interference code from the interference generator is added linearly in a linear adder with the received DS-SS signal. We are using 741 op-amp adder. Here the two inputs are given via suitable resistors (10K) to the non-inverting input. We have to use Rf = R1 = 10K to get Vo = E1 + E2 as it was mentioned in the design. The supply for this op-amp adder 15 V is given by an op-amp supply. The output of this adder is the added signal and is given to the next stage which is the comparator. The circuit diagram of op-amp adder is given in Fig.4.3. The pin diagram and characteristics of 741 are given in Appendix.

4.4 COMPARATOR

In the comparator, we have to compare the added signal with a threshold of 2.5 V. This 2.5 V is generated using a resistor network. 5 V supply is given to a series combination of two 2.2 K resistors. We get 2.5 V at the middle of the resistor connection.

We are using LM 311 as the comparator. This is capable of comparing signals at high frequency. The supply voltage may be either 5 V or 15 V. The added signal is given to the input 2. The threshold is given to input 3. If the added signal is greater than the threshold, the output of the comparator is high. If it is less than the threshold, the output is low. The pin diagram and characteristics of LM 311

are given in Appendix.

This comparator output is not suitable for despreading. Hence, it is given to a 'D' flip-flop (7474) which is fed by 1 MHZ clock. Now the output of 'D' flip-flop becomes suitable for despreading, since it is at a frequency of 1 MHZ.

The circuit diagram of comparator with 'D' flip-flop is given in Fig.4.4.

4.5 DESPREADER:

Despreader is nothing but an EX-OR gate (7486). One input is the output of 'D' flip-flop (7474). Other input is the code which is used in the transmitter. Both the signals are MOD 2 added in the EX-OR gate. The output is the received data. The circuit is given in Fig.4.5.

4.6 FREQUENCY COUNTER:

The received data and the original data transmitted must be compared to find the error in the system. For this, both the data must be at the same frequency and at synchronization. To achieve this,they are passed through two 'D' flip-flops fed by the same clock of 16 KHZ. We get the synchronized outputs from the two flip-flops. Then they are again passed through an EX-OR gate for comparison. The output of EX-OR gate is '1', when the inputs are not equal. Thus, it is used to find out the error. This is given to the frequency counter instrument.

The frequency counter increments by one whenever an error occurs. Frequency counter value is a measure of the performance of the system in the presence of interference. The amplitude of the interference code is varied by varying the supply voltage and in each case the performance is studied using the frequency counter.

The various blocks mentioned above are interconnected as shown in the complete circuit diagram of Fig.4.6. This is the DS-SS receiver.

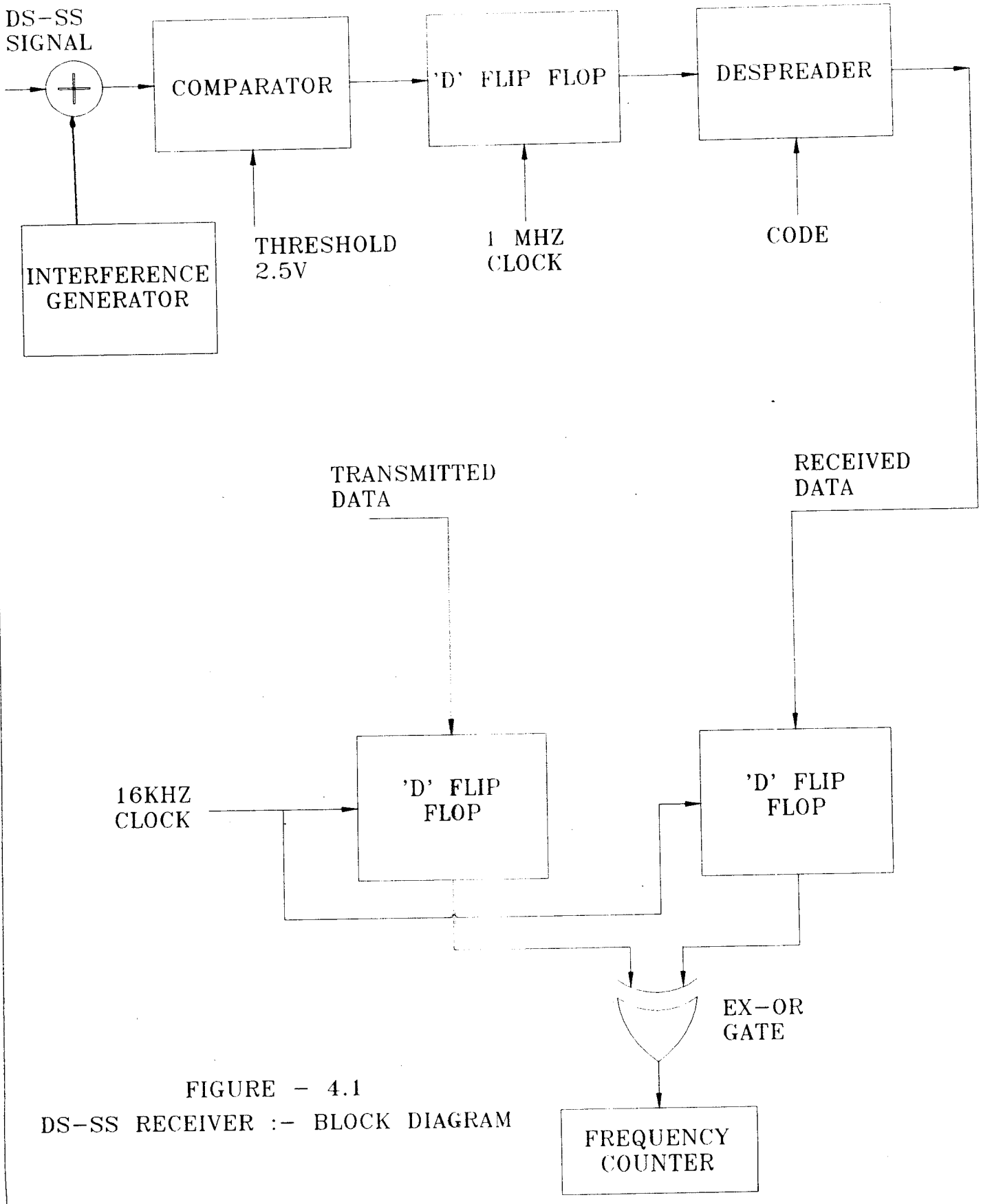


FIGURE - 4.1

DS-SS RECEIVER :- BLOCK DIAGRAM

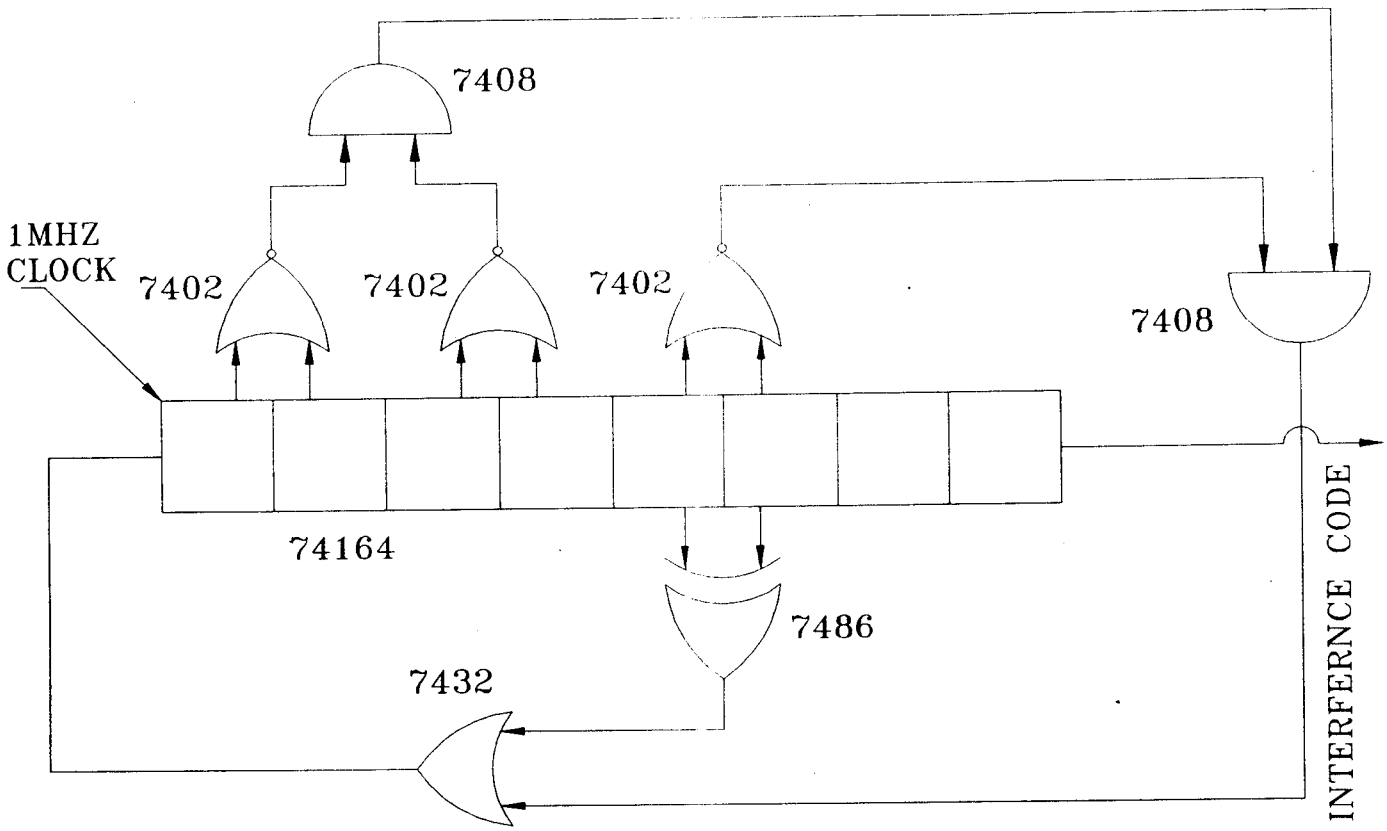


FIGURE – 4.2
INTERFERENCE GENERATOR

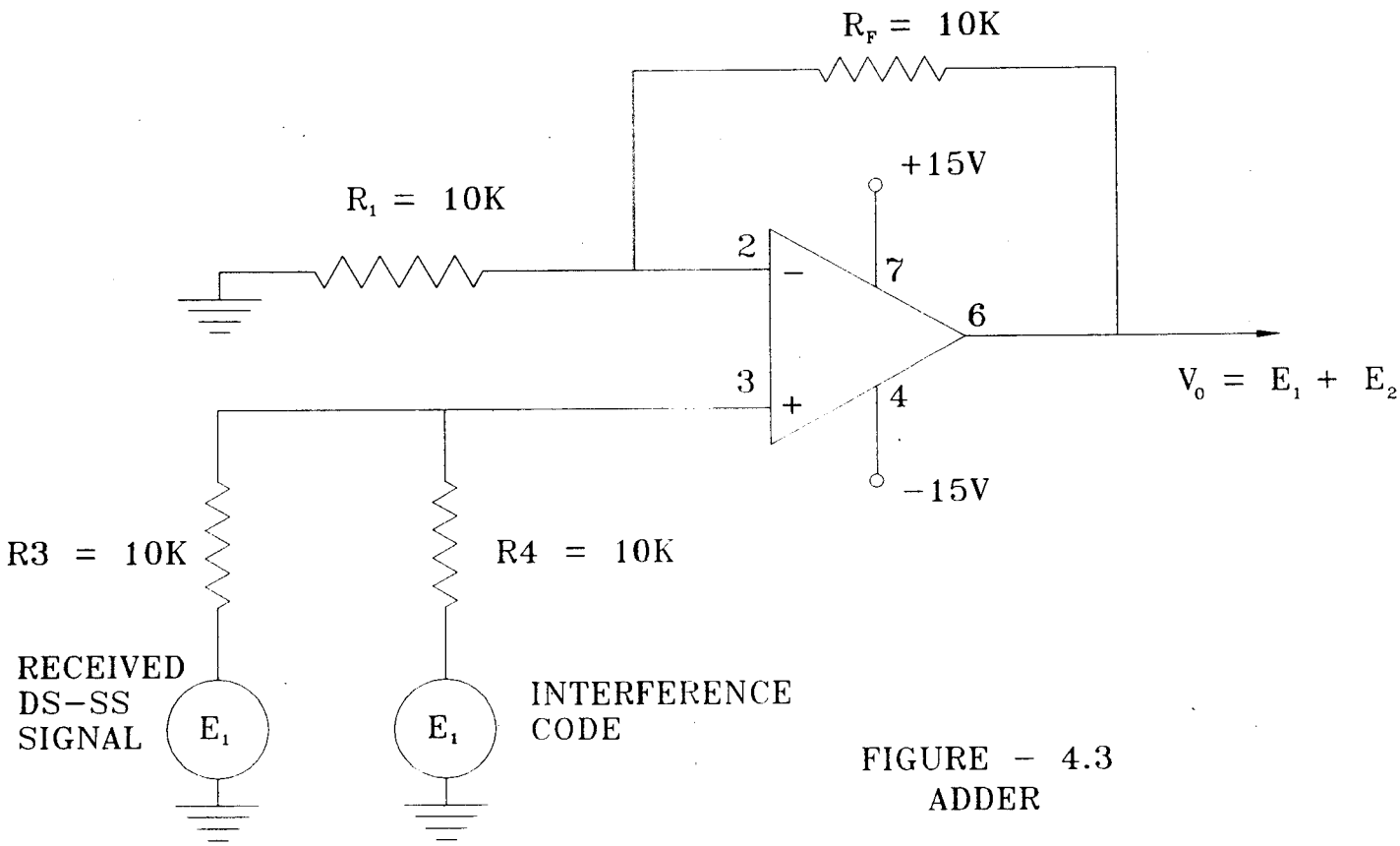


FIGURE – 4.3
ADDER

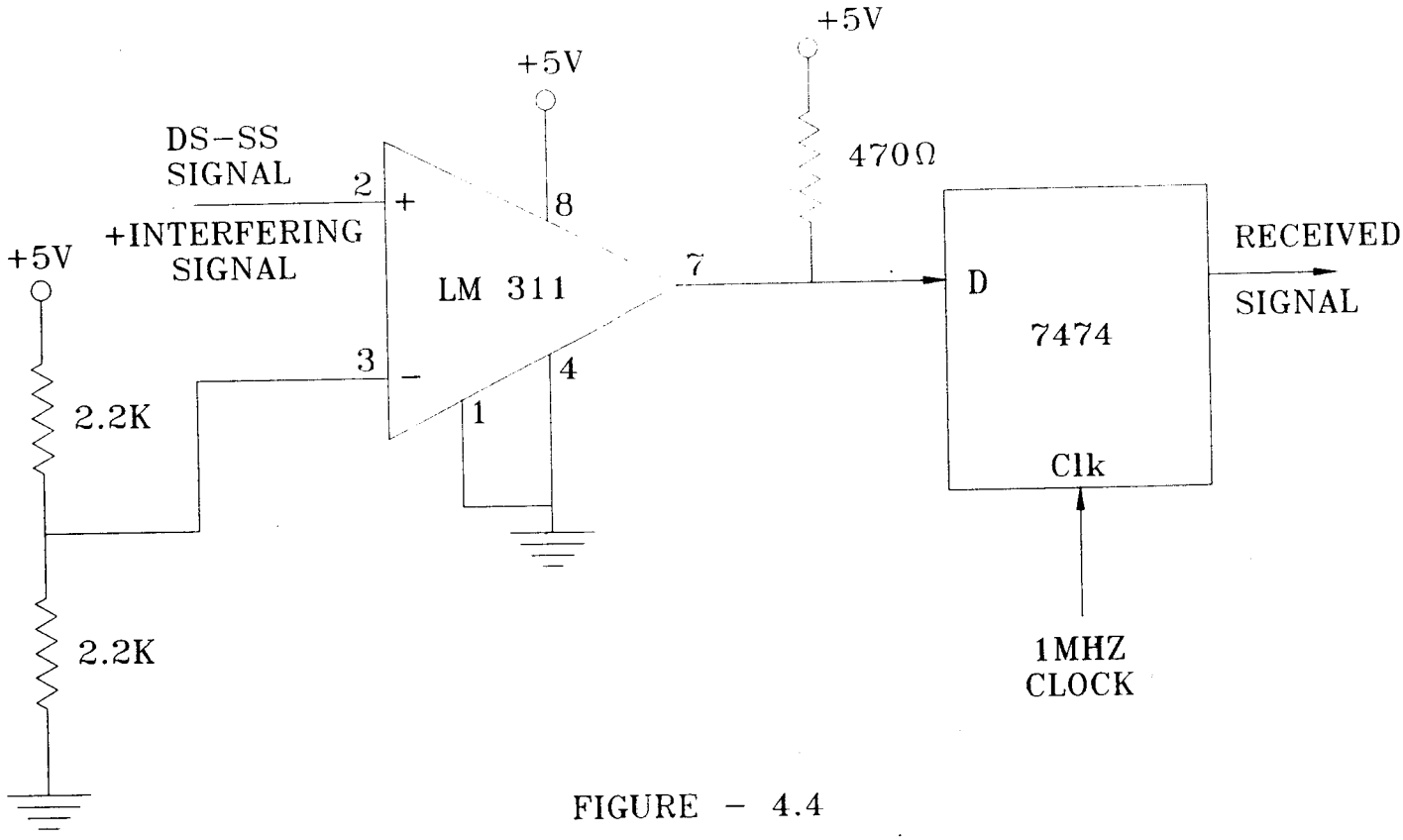


FIGURE – 4.4
COMPARATOR

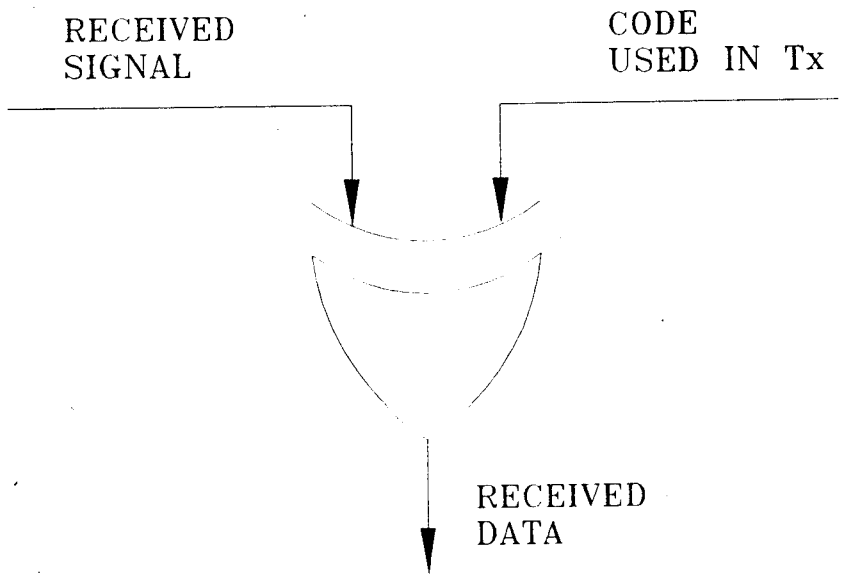


FIGURE – 4.5
DESPREADER

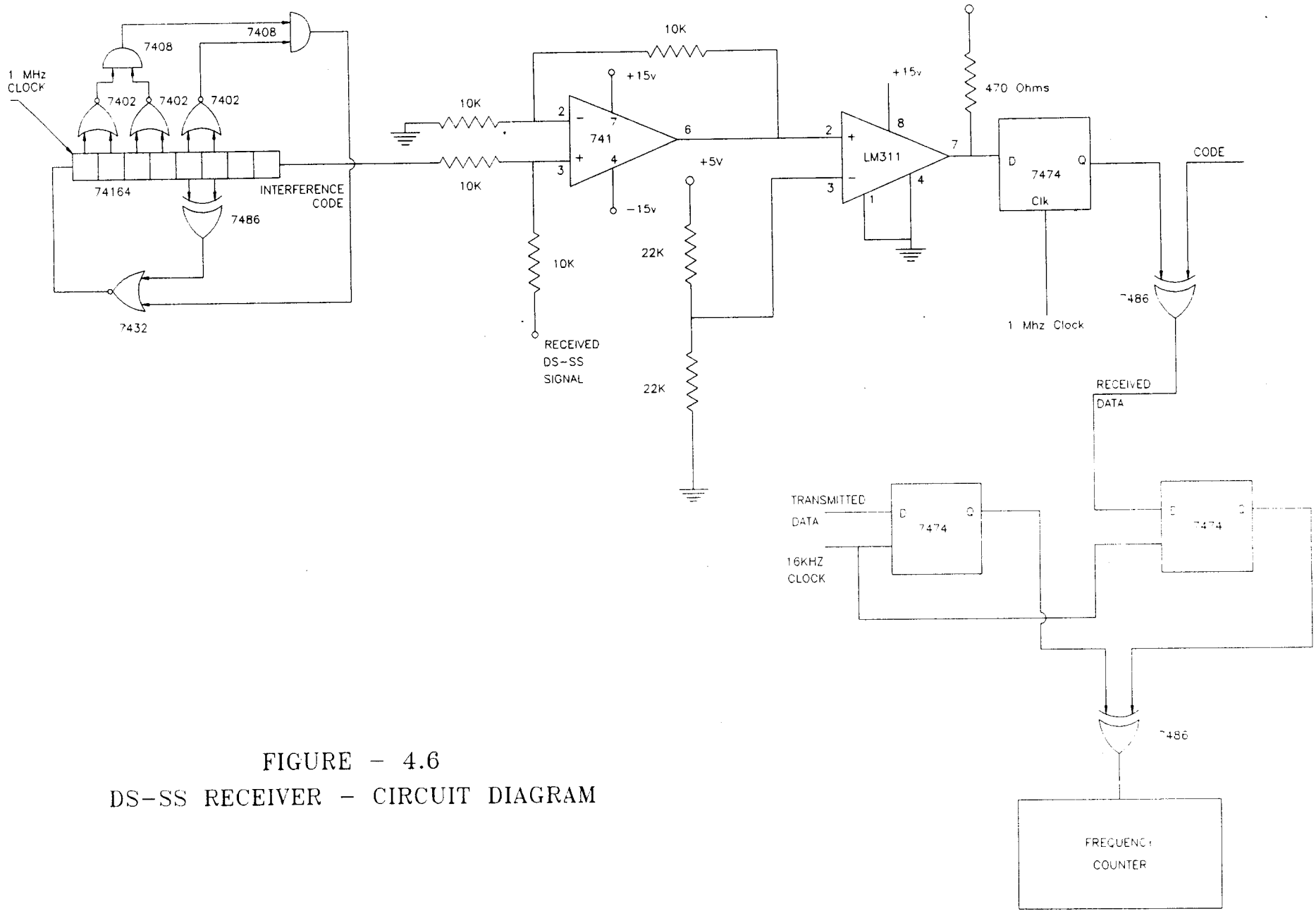


FIGURE − 4.6

DS−SS RECEIVER − CIRCUIT DIAGRAM

CONCLUSION

CONCLUSION

The DS-SS transmitter and receiver discussed in the earlier sections were implemented. Both of them are found to work satisfactorily. For various amplitudes of the interfering signal, the performance of the system in the presence of interference was studied.

This DS-SS system can be further improved by incorporating the acquisition and tracking loops in the receiver ie., generating the code in the receiver itself. We can also incorporate BPSK modulation and demodulation schemes to make this system a more practical one.

Another progress that can be made is, by using the Hybrid method of spread spectrum where the disadvantages encountered in the pseudo noise method can be overcome.

BIBLIOGRAPHY

APPENDIX

8-Bit Serial-In Parallel-Out Shift Register

- Gated serial Data Inputs
- Typical shift frequency of 36MHz
- Asynchronous Master Reset
- Fully buffered Clock and Data Inputs

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74164	36MHz	37mA
74LS164	36MHz	16mA

DESCRIPTION

The '164 is an 8 bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (D_{sa} or D_{sb}); either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the Clock (CP) input, and enters into Q_0 the logical AND of the two Data inputs ($D_{sa} \cdot D_{sb}$) that existed one setup time before the rising clock edge. A LOW level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

ORDERING CODE

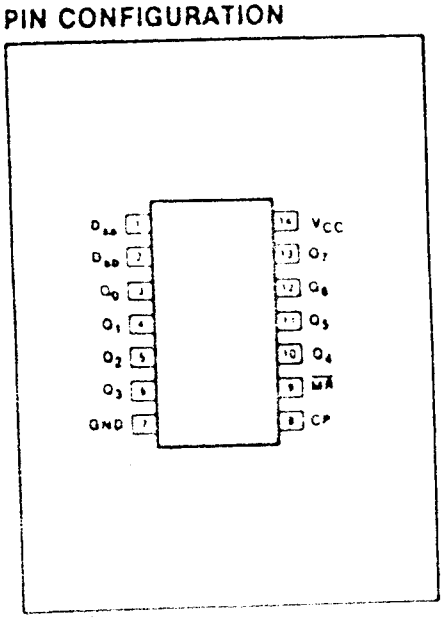
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74164N • N74LS164N	
Ceramic DIP	N74164F • N74LS164F	S54164F • S54LS164F
Flatpack		S54LS164W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

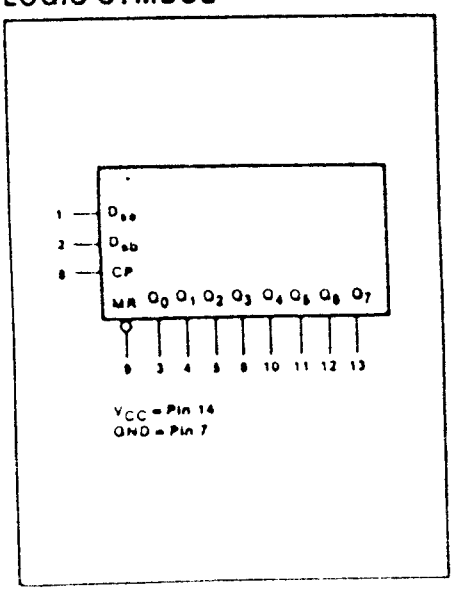
PINS	DESCRIPTION	54/74	54/74LS
All	Inputs	1ul	1LSul
All	Ouputs	5ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

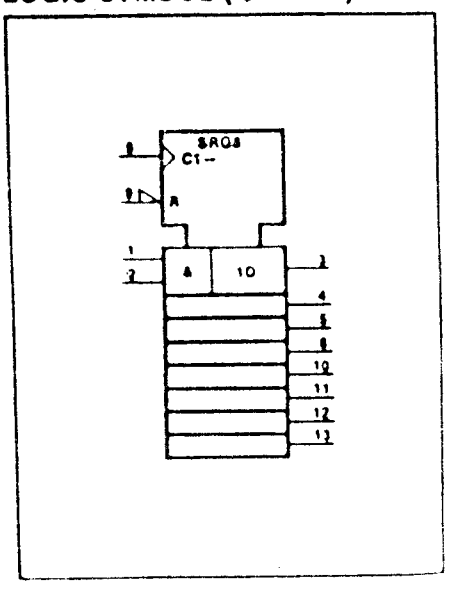
PIN CONFIGURATION



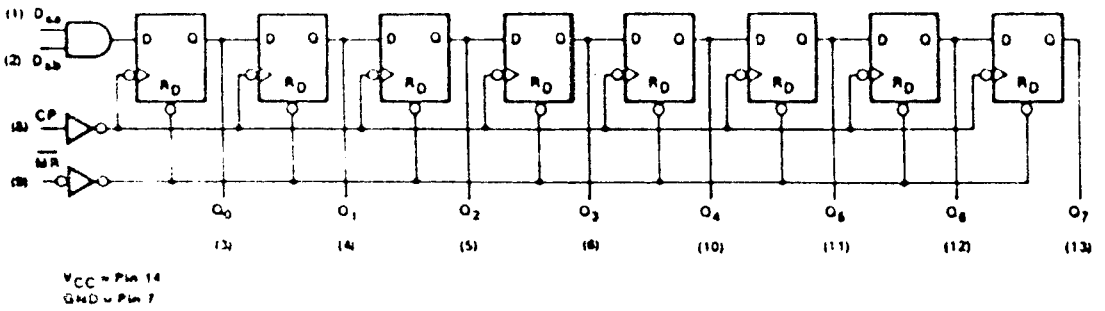
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS			
	$\overline{MR}$	CP	D_{sa}	D_{sb}	Q_0	Q_1	—	Q_7
Reset (Clear)	L	X	X	X	L	L	—	L
Shift	H	↑	l	l	L	q_0	—	q_6
	H	↑	l	h	L	q_0	—	q_6
	H	↑	h	l	L	q_0	—	q_6
	H	↑	h	h	H	q_0	—	q_6

H = HIGH voltage level.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH Clock transition.
L = LOW voltage level.
l = LOW voltage level one setup time prior to the LOW-to-HIGH Clock transition.
q = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH Clock transition.
X = Don't care.
↑ = LOW-to-HIGH Clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

	PARAMETER	54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER		54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−400			−400	µA
I_{OL}	LOW-level output current	Mil			8			4	mA
		Com'l			8			8	mA
T_A	Operating free air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

4-Bit Shift Register

- Separate negative-edge-triggered shift and parallel load clocks
- Common mode control input
- Shift right serial input
- Synchronous shift or load capabilities

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
7495	36MHz	39mA
74LS95B	36MHz	13mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N7495N • N74LS95BN	
Ceramic DIP	N7495F • N74LS95BF	S5495F • S54LS95BF
Flatpack		S5495W • S54LS95BW

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
S	Input	2ul	1LSul
Other	Inputs	1ul	1LSul
Q	Output	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40µA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20µA I_{IH} and −0.4mA I_{IL}

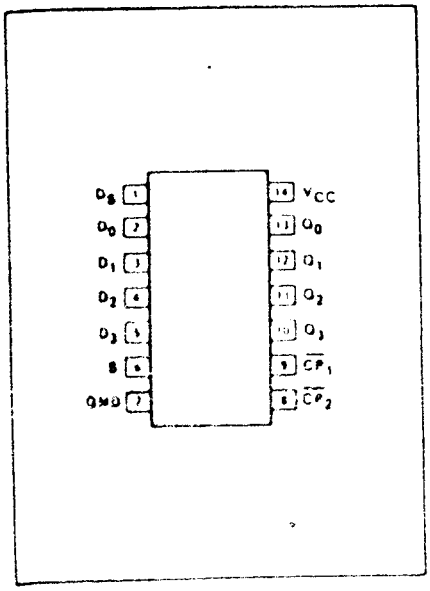
DESCRIPTION

The '95 is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has serial Data (D_S) and four parallel Data (D_0-D_3) inputs and four Parallel outputs (Q_0-Q_3). The serial or parallel mode of operation is controlled by a Mode Select input (S) and two Clock inputs ($\overline{CP}_1$ and $\overline{CP}_2$). The serial (shift right) or parallel data transfers occur synchronously with the HIGH-to-LOW transition of the selected Clock input

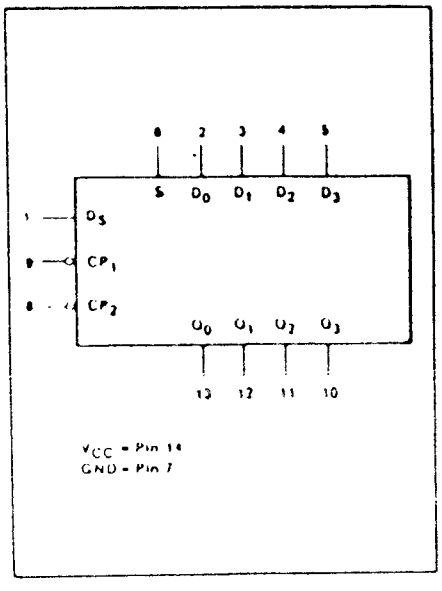
When the Mode Select input (S) is HIGH, $\overline{CP}_2$ is enabled. A HIGH to LOW transition on enabled $\overline{CP}_2$ loads parallel data from the D_0-D_3 inputs into the register. When S is LOW, CP_1 is enabled. A HIGH-to-LOW transition on enabled $\overline{CP}_1$ shifts the data from Serial input D_S to Q_0 and transfers the data in Q_0 to Q_1, Q_1 to Q_2, and Q_2 to Q_3 respectively (shift right). Shift left is accomplished by externally connecting Q_3 to D_2, Q_2 to D_1, Q_1 to D_0, and operating the '95 in the parallel mode (S = HIGH).

In normal operations the Mode Select (S) should change states only when both Clock inputs are LOW. However, changing S from HIGH-to-LOW while $\overline{CP}_2$ is LOW, or changing S from LOW-to-HIGH while $\overline{CP}_1$ is LOW will not cause any changes on the register outputs.

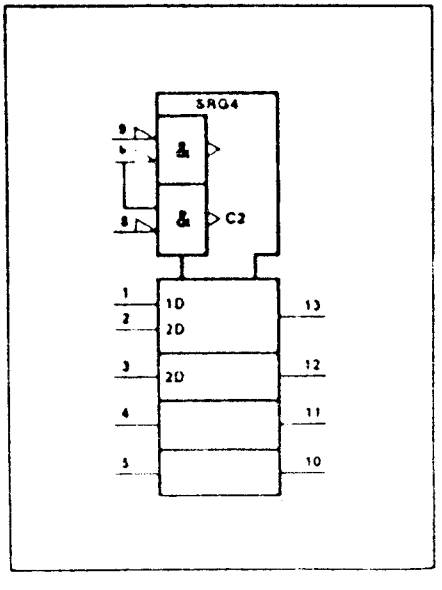
PIN CONFIGURATION



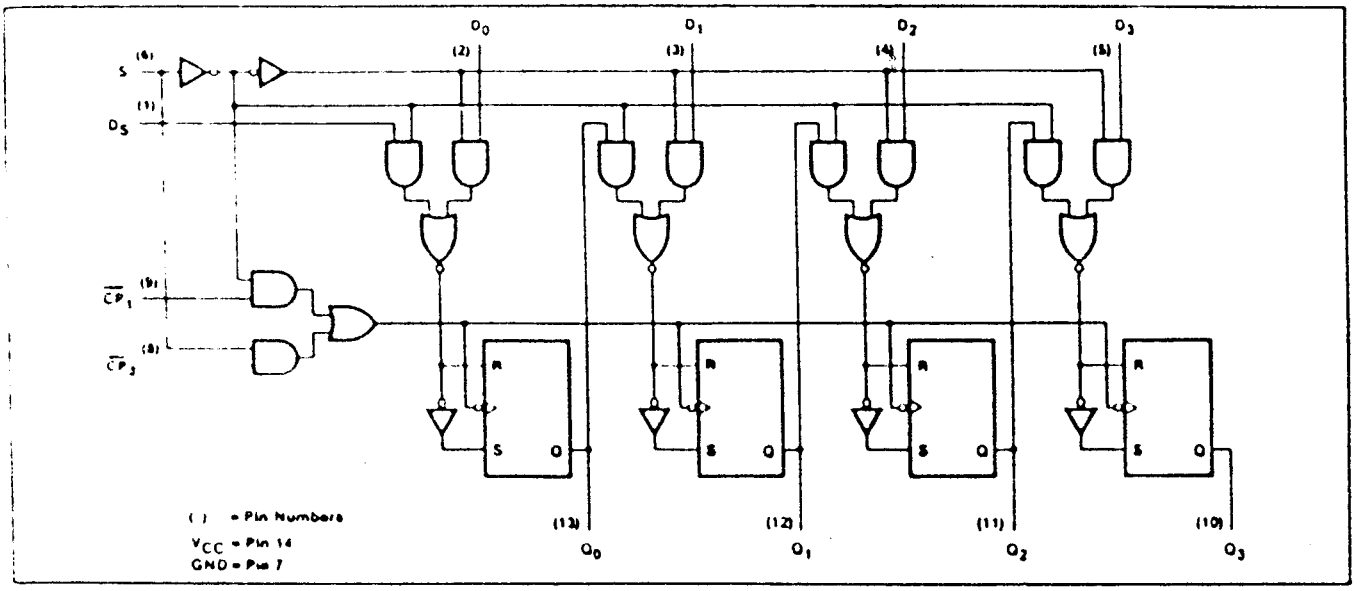
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
$V_{(OUT)}$	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	+0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS			
	S	CP_1	CP_2	D_S	D_N	Q_0	Q_1	Q_2	Q_3
Parallel load	H	X	↓	X	↓	L	L	L	L
	H	X	↓	X	h	H	H	H	H
Shift right	L	↓	X	↓	X	L	q_0	q_1	q_2
	L	↓	X	h	X	H	q_0	q_1	q_2
Mode change	↓	L	X	X	X	no change			
	↓	H	X	X	X	undetermined			
	↑	X	L	X	X	no change			
	↑	X	H	X	X	undetermined			

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the HIGH-to-LOW clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the HIGH-to-LOW clock transition.
q = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW clock transition.
X = Don't care.
↓ = HIGH-to-LOW transition of Clock or Mode Select
↑ = LOW-to-HIGH transition of Mode Select

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−800			−400	µA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

Quad Two-Input Exclusive-OR Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7486	14ns	30mA
74LS86	10ns	6.1mA
74S86	7ns	50mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N7486N • N74LS86N N74S86N	
Ceramic DIP	N7486F • N74LS86F N74S86F	S5486F • S54LS86F S54S86F
Flatpack		S5486W • S54LS86W S54S86W

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

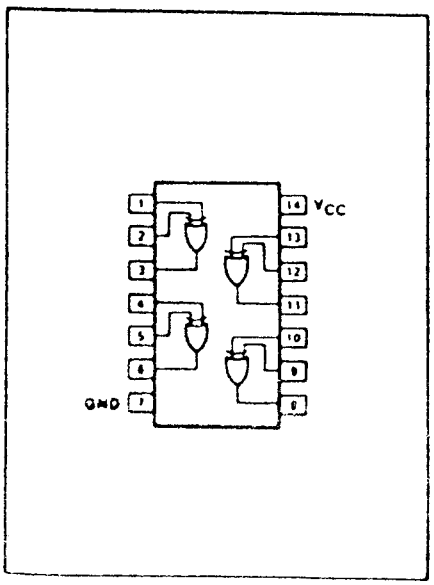
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

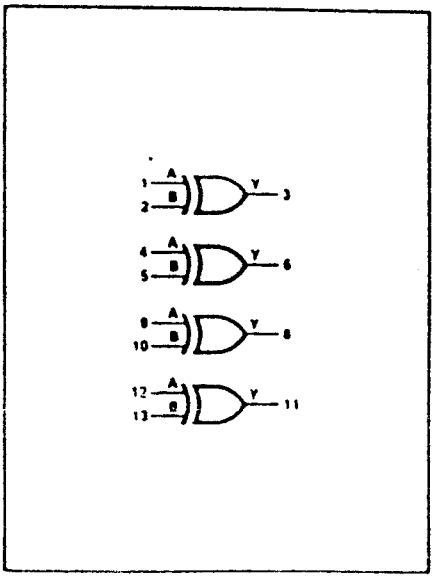
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1ul	1Sul	1LSul
Y	Output	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

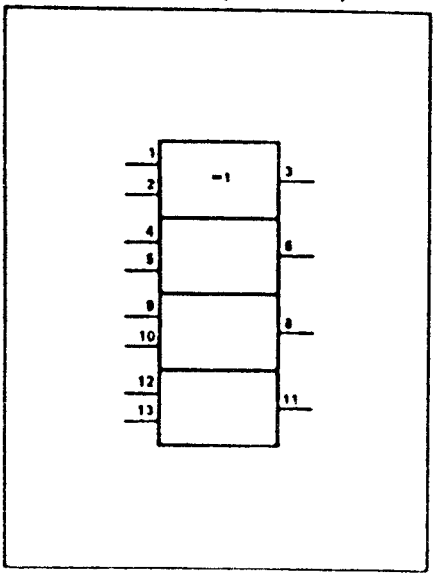
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

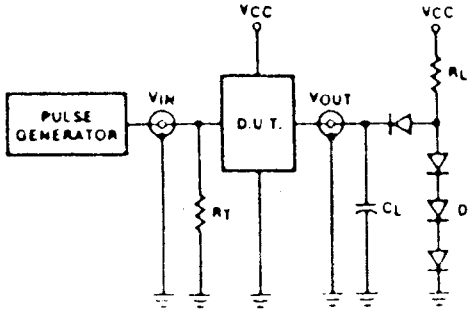
RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current				−800			−400			−1000	µA
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

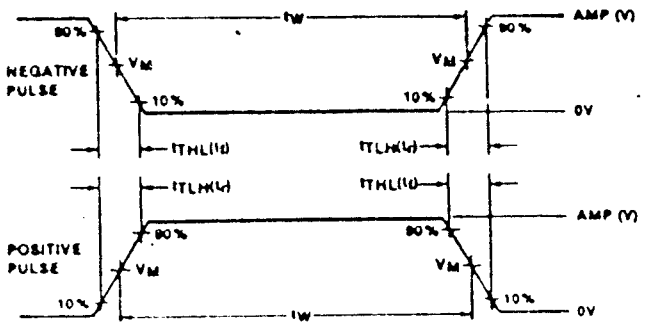
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}, see AC CHARACTERISTICS for value
C_L = Load capacitance includes jig and probe capacitance, see AC CHARACTERISTICS for value
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators
D = Diodes are 1N916, 1N3064, or equivalent
t_{TLH}, t_{THL} Values should be less than or equal to the table entries

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

μA741

FREQUENCY-COMPENSATED OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

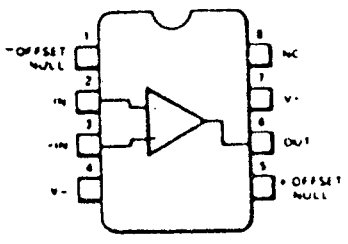
GENERAL DESCRIPTION – The μA741 is a high performance monolithic Operational Amplifier constructed using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of latch-up tendencies make the μA741 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications.

- NO FREQUENCY COMPENSATION REQUIRED
- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH-UP

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
μA741A, μA741, μA741E	±22 V
μA741C	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Molded and Hermetic DIP	670 mW
Mini DIP	310 mW
Flatpak	570 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Can, Hermetic DIP, and Flatpak	−65°C to +150°C
Mini DIP, Molded DIP	−55°C to +125°C
Operating Temperature Range	
Military (μA741A, μA741)	−55°C to +125°C
Commercial (μA741E, μA741C)	0°C to +70°C
Pin Temperature (Soldering)	
Metal Can, Hermetic DIPs, and Flatpak (60 s)	300°C
Molded DIPs (10 s)	260°C
Output Short Circuit Duration (Note 3)	Indefinite

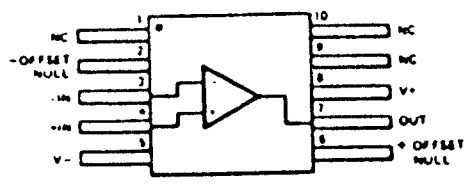
8-PIN MINI DIP
(TOP VIEW)
PACKAGE OUTLINES 6T 9T
PACKAGE CODES H T



ORDER INFORMATION

TYPE	PART NO.
μA741C	μA741TC
μA741C	μA741HC

10-PIN FLATPAK
(TOP VIEW)
PACKAGE OUTLINE 3F
PACKAGE CODE F

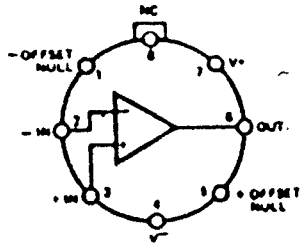


ORDER INFORMATION

TYPE	PART NO.
μA741A	μA741AFM
μA741	μA741FM

CONNECTION DIAGRAMS

8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5B
PACKAGE CODE H

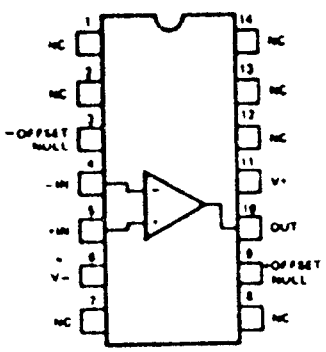


Note: Pin 4 connected to case

ORDER INFORMATION

TYPE	PART NO.
μA741A	μA741AHM
μA741	μA741HM
μA741E	μA741EHC
μA741C	μA741HC

14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6A, 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA741A	μA741ADM
μA741	μA741DM
μA741E	μA741EDC
μA741C	μA741DC
μA741C	μA741PC

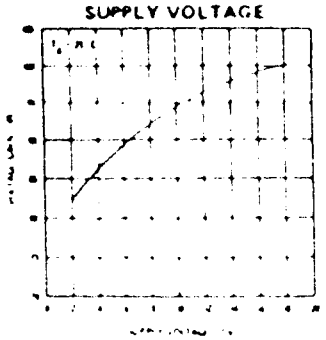
μA741C

ELECTRICAL CHARACTERISTICS: V_S = ±15 V, T_A = 25°C unless otherwise specified.

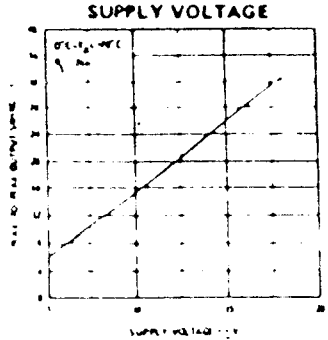
CHARACTERISTICS (see definitions)		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 10$ kΩ		2.0	6.0	mV
Input Offset Current				20	200	nA
Input Bias Current				80	500	nA
Input Resistance			0.3	2.0		MΩ
Input Capacitance				1.4		pF
Offset Voltage Adjustment Range				±15		mV
Input Voltage Range			±12	±13		V
Common Mode Rejection Ratio		$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio		$R_S \leq 10$ kΩ		30	150	μV/V
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	20,000	200,000		
Output Voltage Swing		$R_L \geq 10$ kΩ	±12	±14		V
		$R_L \geq 2$ kΩ	±10	±13		V
Output Resistance				75		Ω
Output Short Circuit Current				25		mA
Supply Current				1.7	2.8	mA
Power Consumption				50	85	mW
Transient Response (Unity Gain)	Rise time	V_{IN} = 20 mV, R_L = 2 kΩ, $C_L \leq$ 100 pF		0.3		μs
	Overshoot			5.0		%
Slew Rate		$R_L \geq 2$ kΩ,		0.5		V/μs
The following specifications apply for 0°C ≤ T_A ≤ +70°C						
Input Offset Voltage					7.5	mV
Input Offset Current					300	nA
Input Bias Current					800	nA
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	15,000			
Output Voltage Swing		$R_L \geq 2$ kΩ	±10	±13		V

TYPICAL PERFORMANCE CURVES FOR μA741E AND μA741C

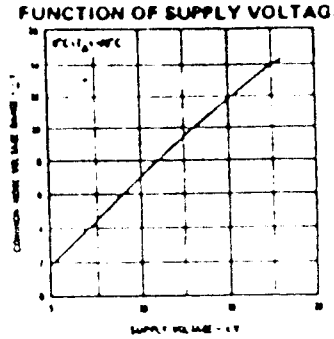
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



National Semiconductor Corporation

LM111/LM211/LM311 Voltage Comparator

General Description

The LM111, LM211 and LM311 are voltage comparators that have input currents nearly a thousand times lower than devices like the LM106 or LM710. They are also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50 mA.

Both the inputs and the outputs of the LM111, LM211 or the LM311 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM106 and LM710 (200 ns response time vs 40 ns) the devices are also much less prone to spurious oscillations. The LM111 has the same pin configuration as the LM106 and LM710.

The LM211 is identical to the LM111, except that its performance is specified over a −25°C to +85°C temperature range instead of −55°C to +125°C. The LM311 has a temperature range of 0°C to +70°C.

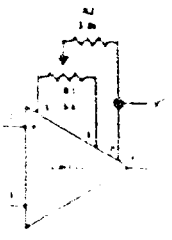
Features

- Operates from single 5V supply
- Input current: 150 nA max. over temperature
- Offset current: 20 nA max. over temperature
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

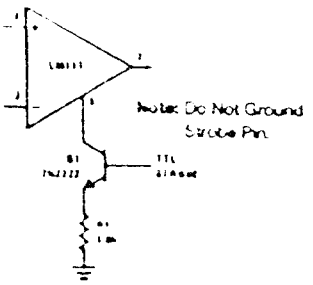
Typical Applications**

**Note: Pin connections shown on schematic diagram and typical applications are for TO-5 package.

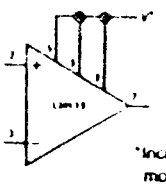
Offset Balancing



Strobing

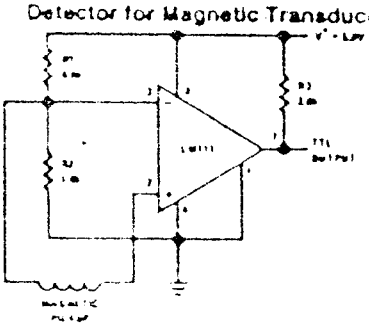


Increasing Input Stage Current*

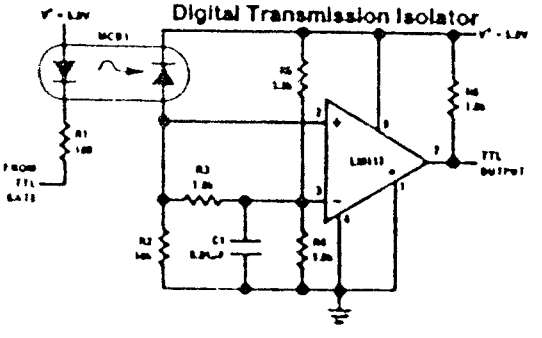


*Increases typical common mode slew from 7.0V/μs to 18V/μs.

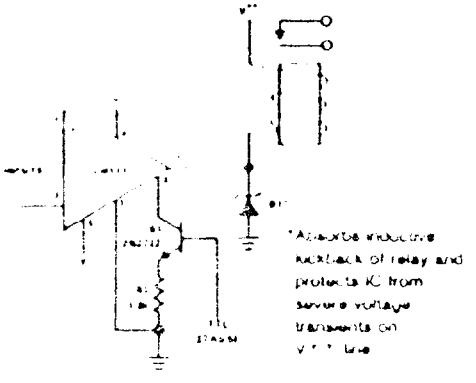
Detector for Magnetic Transducer



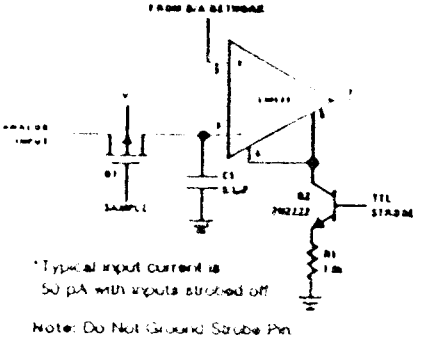
Digital Transmission Isolator



Relay Driver with Strobe



Strobing off Both Input* and Output Stages



TL/H/5704–1

Absolute Maximum Ratings for the LM111/LM211

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 7)

Total Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage (V_{74})	50V
Ground to Negative Supply Voltage (V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec

Operating Temperature Range LM111	−55°C to 125°C
LM211	−25°C to 85°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	260°C
Voltage at Strobe Pin	V+ −5V

Soldering Information
- Dual-In-Line Package
  - Soldering (10 seconds) ..... 260°C
- Small Outline Package
  - Vapor Phase (60 seconds) ..... 215°C
  - Infrared (15 seconds) ..... 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

Electrical Characteristics for the LM111 and LM211 (Note 3)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$		0.7	3.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$		4.0	10	nA
Input Bias Current	$T_A = 25°C$		60	100	nA
Voltage Gain	$T_A = 25°C$	40	200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$		0.75	1.5	V
Strobe ON Current (Note 6)	$T_A = 25°C$	2.0	3.0	5.0	mA
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$ $T_A = 25°C$, $I_{STROBE} = 3$ mA		0.2	10	nA
Input Offset Voltage (Note 4)	$R_S \leq 50$ k			4.0	mV
Input Offset Current (Note 4)				20	nA
Input Bias Current				150	nA
Input Voltage Range	$V^+ = 15V$, $V^- = -15V$, Pin 7 Pull-Up May Go To 5V	−14.5	13.8,-14.7	13.0	V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -6$ mV, $I_{SINK} \leq 8$ mA		0.23	0.4	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$		0.1	0.5	μA
Positive Supply Current	$T_A = 25°C$		5.1	6.0	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15 supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LM111 is 150°C, while that of the LM211 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 110°C/W, junction to ambient.

Note 3: These specifications apply for V_S = ±15V and Ground pin at ground, and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. With the LM211, however, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Note 6: Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

Note 7: Refer to RETS111X for the LM111H, LM111J and LM111J-8 military specifications.

National Semiconductor Corporation

LM111/LM211/LM311 Voltage Comparator

General Description

The LM111, LM211 and LM311 are voltage comparators that have input currents nearly a thousand times lower than devices like the LM106 or LM710. They are also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50 mA.

Both the inputs and the outputs of the LM111, LM211 or the LM311 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM106 and LM710 (200 ns response time vs 40 ns) the devices are also much less prone to spurious oscillations. The LM111 has the same pin configuration as the LM106 and LM710.

The LM211 is identical to the LM111, except that its performance is specified over a −25°C to +85°C temperature range instead of −55°C to +125°C. The LM311 has a temperature range of 0°C to +70°C.

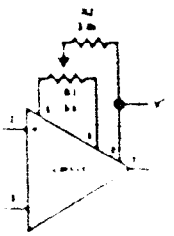
Features

- Operates from single 5V supply
- Input current: 150 nA max. over temperature
- Offset current: 20 nA max. over temperature
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

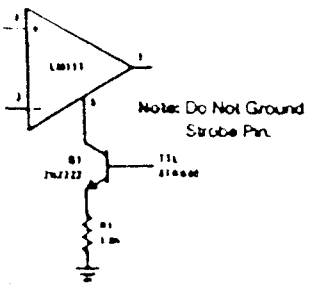
Typical Applications**

**Note: Pin connections shown on schematic diagram and typical applications are for TO-5 package.

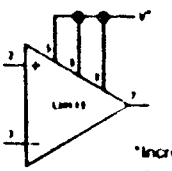
Offset Balancing



Strobing

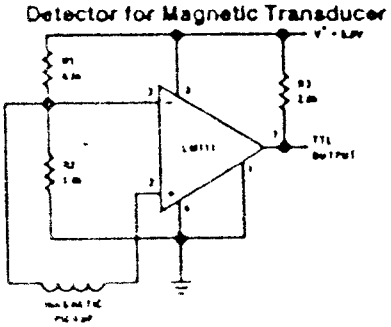


Increasing Input Stage Current*

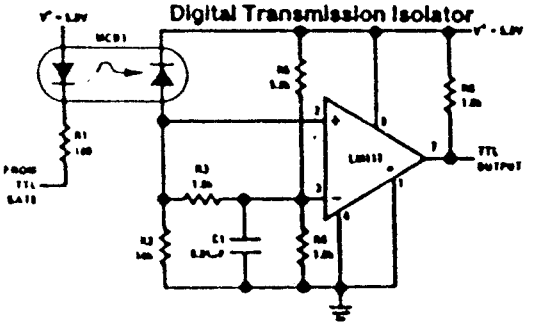


*Increases typical common mode slew from 7.0V/μs to 18V/μs.

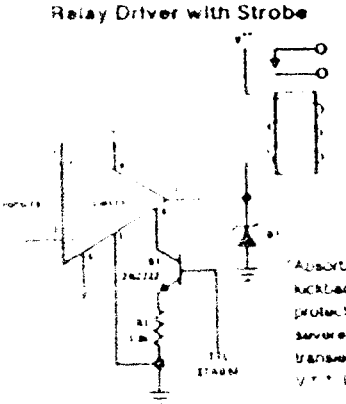
Detector for Magnetic Transducer



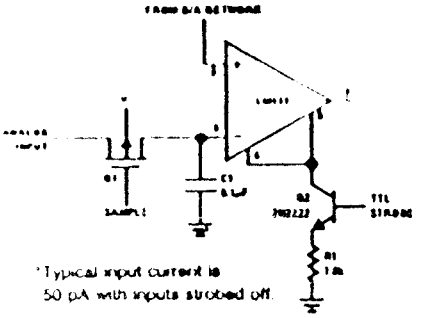
Digital Transmission Isolator



Relay Driver with Strobe



Strobing off Both Input* and Output Stages



TL/H/5704-1

Absolute Maximum Ratings for the LM111/LM211

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 7)

Total Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage (V_{74})	50V
Ground to Negative Supply Voltage (V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec

Operating Temperature Range LM111 −55°C
LM211 −25°C
Storage Temperature Range −65°C
Lead Temperature (Soldering, 10 sec)
Voltage at Strobe Pin V
Soldering Information
Dual-In-Line Package
Soldering (10 seconds) .....
Small Outline Package
Vapor Phase (60 seconds) .....
Infrared (15 seconds) .....

See AN-450 "Surface Mounting Methods and Their on Product Reliability" for other methods of solderir face mount devices.

ESD rating to be determined.

Electrical Characteristics for the LM111 and LM211 (Note 3)

Parameter	Conditions	Min	Typ	Max	U
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$		0.7	3.0	
Input Offset Current (Note 4)	$T_A = 25°C$		4.0	10	
Input Bias Current	$T_A = 25°C$		60	100	
Voltage Gain	$T_A = 25°C$	40	200		V
Response Time (Note 5)	$T_A = 25°C$		200		
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$		0.75	1.5	
Strobe ON Current (Note 6)	$T_A = 25°C$	2.0	3.0	5.0	m
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$ $T_A = 25°C$, $I_{STROBE} = 3$ mA		0.2	10	
Input Offset Voltage (Note 4)	$R_S \leq 50$ k			4.0	m
Input Offset Current (Note 4)				20	n
Input Bias Current				150	n
Input Voltage Range	$V^+ = 15V$, $V^- = -15V$, Pin 7 Pull-Up May Go To 5V	−14.5	13.8,-14.7	13.0	
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -6$ mV, $I_{SINK} \leq 8$ mA		0.23	0.4	
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$		0.1	0.5	μ
Positive Supply Current	$T_A = 25°C$		5.1	6.0	m
Negative Supply Current	$T_A = 25°C$		4.1	5.0	m

Note 1: This rating applies for ±15 supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal t negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LM111 is 150°C, while that of the LM211 is 110°C. For operating at elevated temperatures, devices in the package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-i package is 110°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and Ground pin at ground, and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. With the LM211, howeve temperature specifications are limited to $-25°C \leq T_A \leq +85°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage fr single 5V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. T these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Note 6: Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

Note 7: Refer to RETS111X for the LM111H, LM111J and LM111J-8 military specifications.