Variable Frequency Inverter for AC Drives

PROJECT REPORT 1996 - 97

Submitted by

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IN PARTIAL FULFILMENT OF THE REQUIREMENTS
FOR THE AWARD OF THE DEGREE OF
BACHELOR OF ENGINEERING IN
ELECTRONICS AND COMMUNICATION ENGINEERING
OF THE BHARATHIAR UNIVERSITY, COIMBATORE

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

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Department of Electronics and Communication Engineering

Certificate

This is to Certify that this Project Entitled

VARIABLE FREQUENCY INVERTER FOR AC DRIVES

Has been submitted by

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in partial fulfilment of the requirements for the award of Degree of Bachelor of Engineering in the Electronics and Communication Engineering Branch of the Bharathiar University, Coimbatore-641046 during the academic year 1996-'97.

(Guide)

(Head of Department)

Certified that the Candidate was Examined by us in the Project Work.

Viva-Voce Examination held on _____

University Register Number _____

(Internal Examiner)

(External Examiner)

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April 2, 1997

TOWHOM SO EVER IT MAY CONCERN

The following students of **Kumaraguru college of Technology,** carried out their Project Work for partial fullfilment of B.E. in the field of Electronics from September '96 to March "97.

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Thier title of Project is 'Variable Frequency inverter for AC Drives"

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ACKNOWLEDGEMENTS

At the outset, we wish to express our gratitude to our principal, **Dr. S.Subramaniam**, B.E., M.Sc.(ENGG); Ph.D,S.M.IEEE, M.I.S.T.E for his kind blessings.

We extend our warm thanks to the beloved Head of the Department Prof. **M. Ramaswamy**, M.E., M.I.S.T.E., M.I.E., C.Engg(I), M.IEEE, for the technical advice and untiring encouragement that he gave throughout this project and also for the belief he had on all of us.

We are very thankful for our external guide **Mr. G. Murugesan**, General Manager of ElGI Electric & Industries Limited, Pollachi who were our Sponsors, for his technical advice as well as material help that he offered and importantly his benovalent attitude towards us.

We would be ungreatful if we leave out **Mr.R.Hariharan**, M.E., of Electrical and Electronics Department, who has always been critically helpful and a source of encouragement.

SYNOPSIS

It had been long since we started using the standard voltage of 50 hz AC for all applications whether it is domestic or industrial. So the AC machines that were produced so far was operated at 50 hz. With 50 hz ac mains , We have no problem in handling these machines.

But if the ac mains were to fail we have to go in for an alternative source. Here comes the need for the circuit that can convert dc power into ac power. And suppose if we take a further step and produce machines that can be operated at a frequency other than 50hz or between a range of frequencies we can't rely on the ac mains available. So we have to go in for the alternative source, the inverter, that can produce a variable frequency ac output power when fed with a constant dc power.

Freqeuncy is one of the parameters that plays an important role in the control of an induction motor. With the inverter output frequency in our hands the motor control especially speed control can be achieved effectively

and efficiently. Also the inverter eliminates the usage of dc motors, induction and synchronous generators, that are costly and bulky, for motor control.

ACKNOWLEDGEMENTS
SYNOPSIS

CONTENTS

INTRODUCTION

Inverter is the alternative source of ac power that comes into use of the ac mains comes into use if the ac mains were to fail and in motor control applications.

The inverter that we design can operate on a load of 600W. Here the process of dc-ac convertion simulates a pulsewidth modulation technique. The inverter designed is a specialised form of PWM inverter, as the constant dc power gets modulated through the switching action of the switching section. The modulated pulse width depends on the on-off time of switches and it determines the output frequency

INVERTERS IN GENERAL

1. BASIC INVERTER

Inverter is the circuit used to convert dc input into ac output. Theoritically inverter is a power oscillator. The basic inverter consists of the dc power source, a switch and the inverter transformer . The basic inverter operation involves the opening and closure of the switch that either connects or disconnects the supply and transformer primary.

When the switch is closed, Vcc is applied to the primary and the flux produces a resultant induced flux on the secondary winding ie, at the output.

When the switch is opened, the primary winding dont receive any supply but its inductance causes a flux in the opposite direction. So now the induced secondary output gets reversed.

Thus the transformer outputs turns out to be ac.

BASIC CIRCUIT

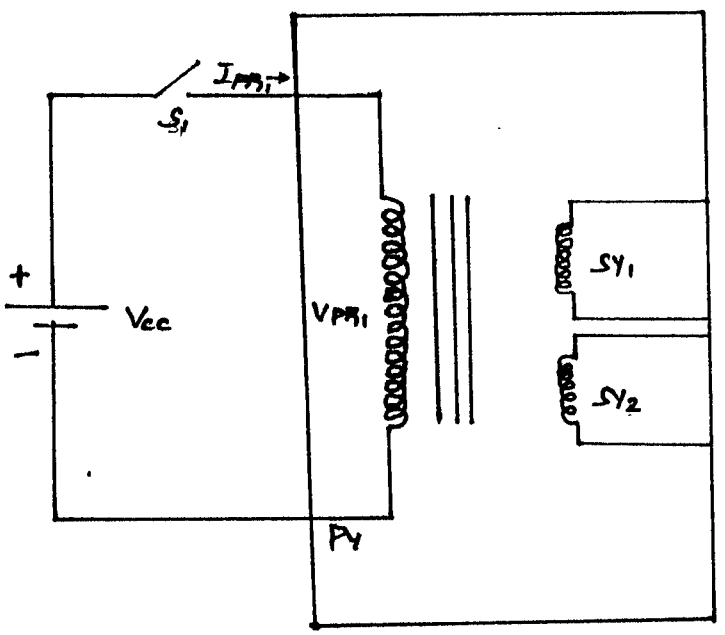


FIG I.1.

TYPES OF INVERTER

I.2 Voltage Driven Inverter:

In a Voltage driven inverter Dc voltage source is connected directly through semiconductor device to primary of transformer. S_1 and S_2 are generally driven by an stable multivibrator operating at a desired frequency.

When S_1 isclosed, source voltage appears across primary of transformer between X and Y. Then after a time period S_1 opens and S_2 closes. Now source voltage is impressed across Y and Z.

Thus an alternating voltage is generated across primary and delivers power to load through secondary.

I.2 CURRENT DRIVEN INVERTER

Works in the same principle as the Voltage driven inverter. But here the input is a current source. Driven inverters are more common than self oscillating ones.

Driven inverters has better frequency stability as a separate master oscillator is used.

VOLTAGE DRIVEN INVERTER

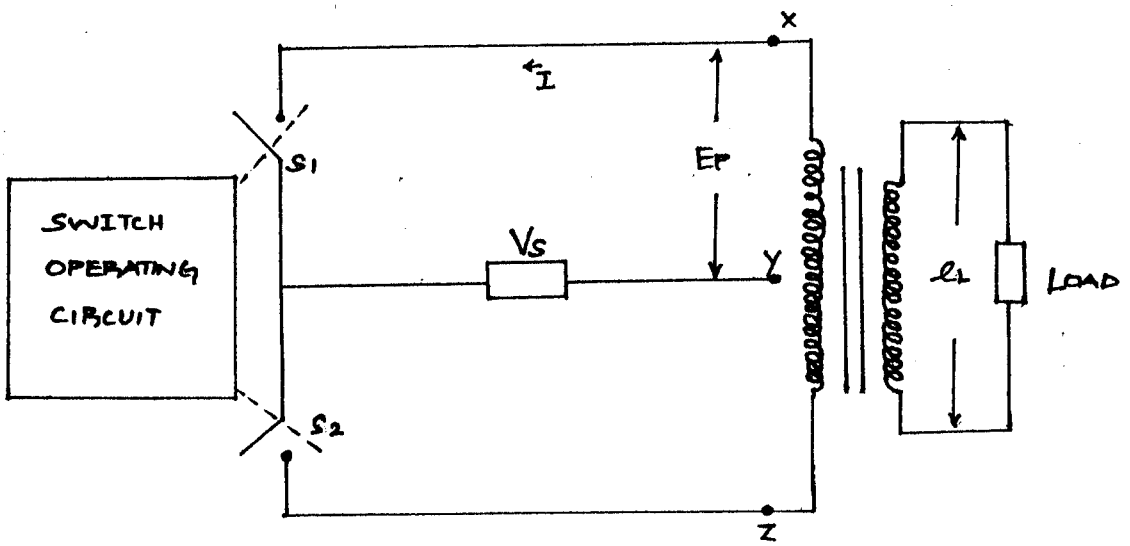


FIG I.2.A

CURRENT DRIVEN INVERTER.

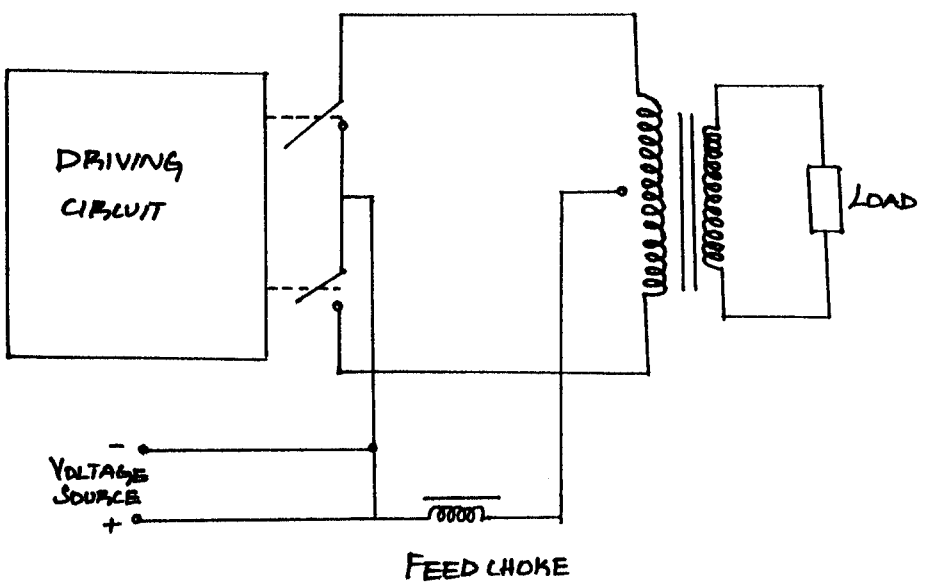


FIG II.22B

Whereas a self oscillating one has its output fed back to transistor.

Advantages of driven inverter.

Accuracy	as interaction b/w
Frequency stability	b/w oscillator andload is
Reliability	practically zero.

These advantages are due to the fact that the interaction between oscillator and load is practically zero.

I.2.1 VOLTAGE SOURCE INVERTER

Principle of operation:

The principle of single-phase inverter can be explained with figure I.2.1

Transistor Q_1 is turned on for a time To/2, the instantaneous voltage across the load is $Vs/_2$. If the transistor Q_2 alone is turned on for a time $To/_2$, $-VS/_2$ appears across the load. The logic circuit should be designed such that Q_1 and Q_2 are not turned on at the same time.

I.2.2 CURRENT SOURCE INVERTERS

To cope with the inductive loads, the power switches with the free wheeling device are required, where - as in a current source inverter, the input behaves as a current source. The output current is maintained constant irrespective of load on the single-phase transistionized inverter. The circuit is represented in figure I.2.3.

I.3. VOLTAGE CONTROL OF SINGLE PHASE INVERTERS

In many industrial applications,it is often required to control the output voltage of inverter because of the following reasons

TRANSISTORISED INVERTERS

VOLTAGE SOURCE INVERTER.

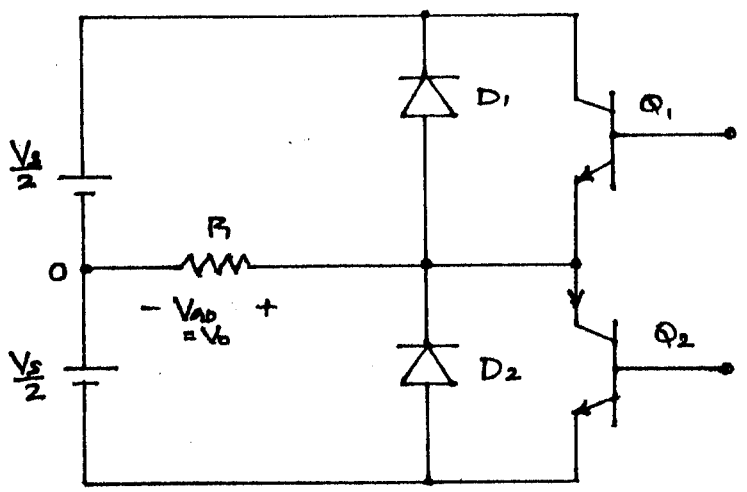


Fig I.2.1.

ASSOCIATED WAVEFORM.

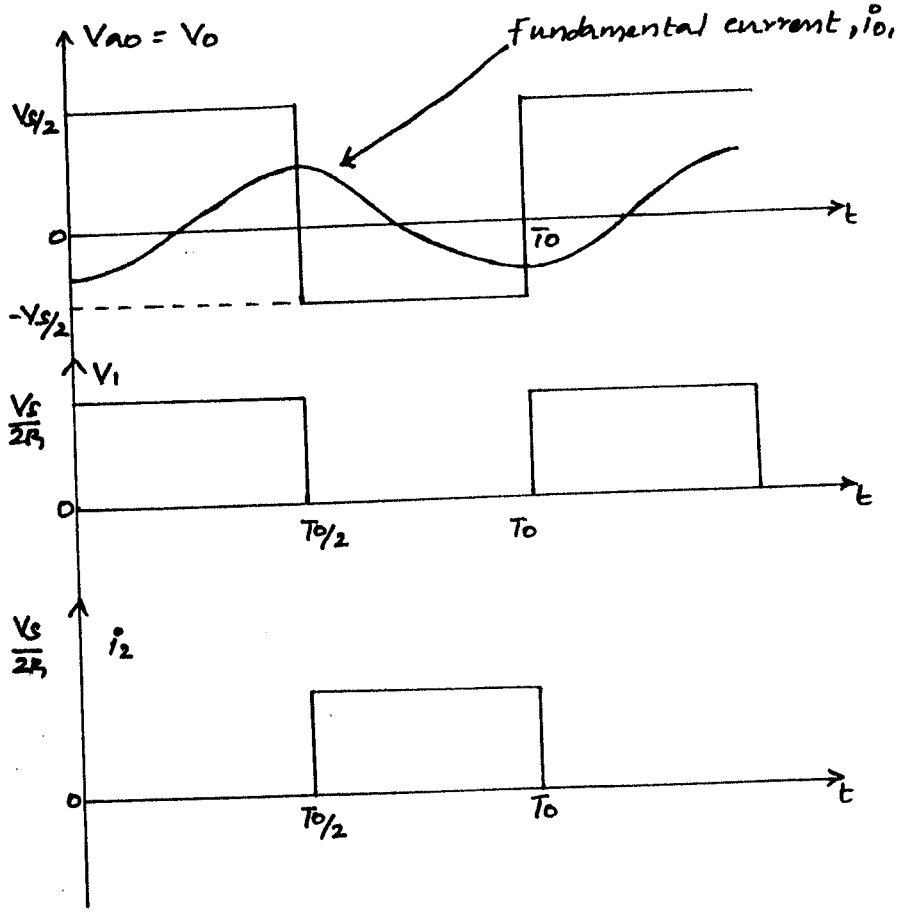


FIG I. 2. 2.

CURRENT SOURCE INVERTER.

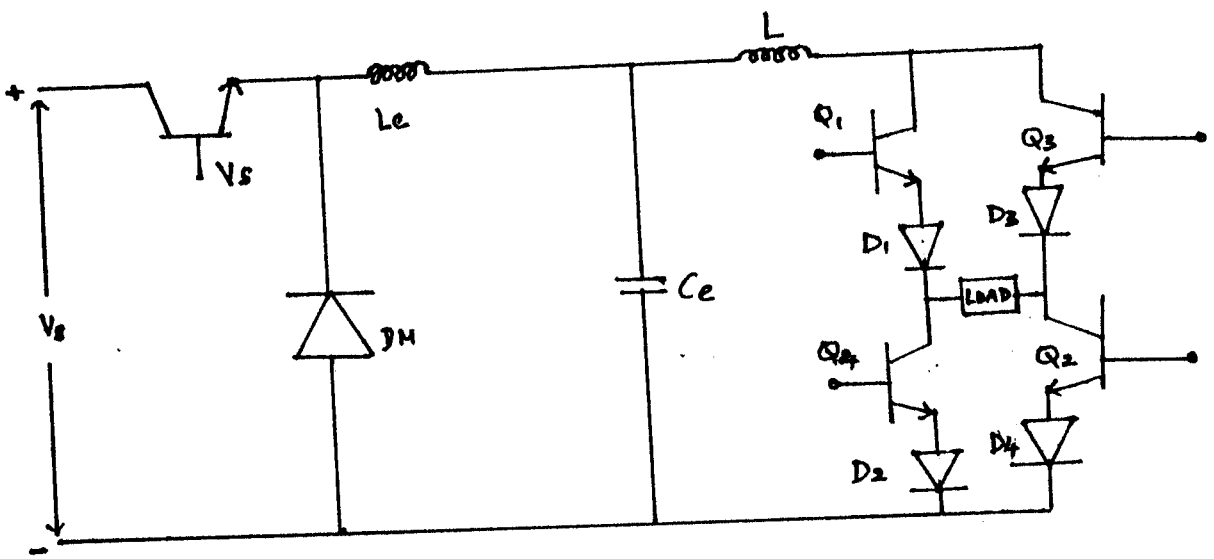


FIG I.2.3.

(1) To cope with the variations of dc input voltage.

(2) For voltage regulations.

(3) Forthe constant Volts/Frequency control requirement.

There are various techniques available to vary the inverters gain. The most efficient method of controlling the gain is to incorporate pulsewidth modulation control within the inverter.

The common techniques are

1. The Single - phase width modulation.
2. Multiple pulse width modulation.
3. Sinusoidally pulse-width modulation.
4. Modified sinosoidally pulse-width modulation.
5. Phase - displacement control.

I.4. CONCEPT OF PWM INVERTERS (Thyristorised)

The output voltage of an inverter can be varied by changing the pulse width of each half-cycle of the inverter output voltage.

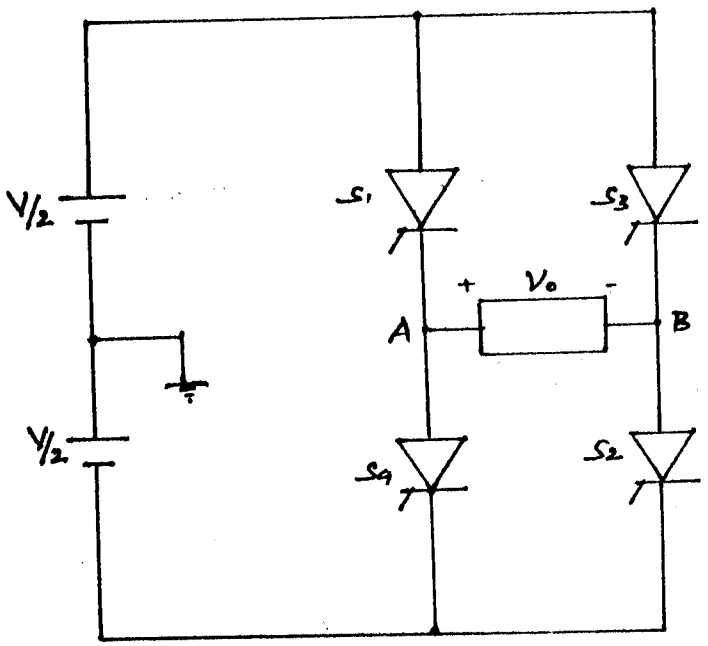
The firing switches S_3 and S_2 are swifted by an angle 'γ^0 with respect to firing of S_1 and S_4.

So pole voltages γAo and γBo as above result.

γAB has pulse width γ^0

By changing shift angle 'γ' the inverter output can be changed.

PULSE WIDTH MODULATION INVERTER.



ASSOCIATED WAVEFORMS.

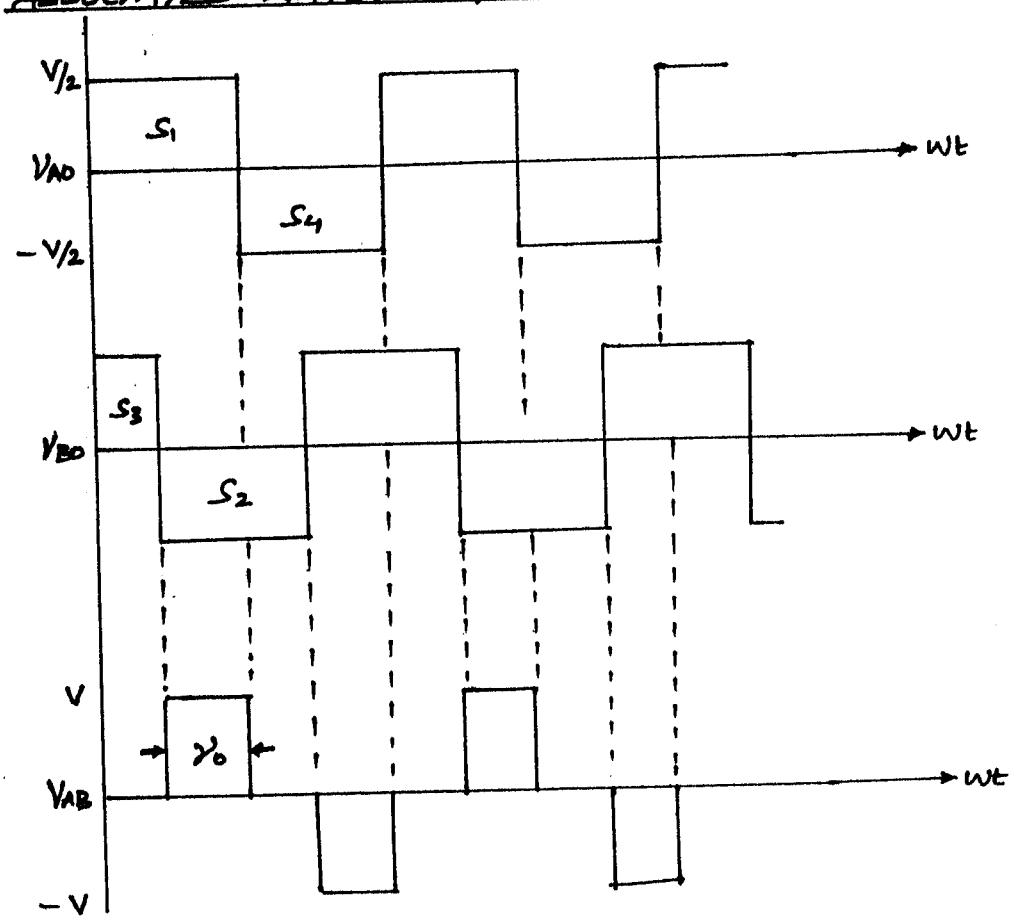


FIG I.2.4.1.

SINUSOIDAL PWM TECHNIQUE

A triangular carrier of frequency fc and a modulating wave of frequency fm , same as inverter output, are used to modulate the pole voltage.

Pole voltage γAo ismodulated by carrier and modulating wave γA and γBo by γB.

The pulses in each half cycle have different widths.

Carrier ratio fc/fm determines the number of pulses in each half-cycle of inverter output voltage.

Modulation index A_m/A_c determines the width of the pulses and hence rms value of inverter output voltage.

1.5 NEED FOR PWM INVERTER

The speed control typically beyond 10:1 range becomes a problem with stepped inverters as at low voltage harmonic currents become excessive causing machine heating and torque pulsation problems. Also utility line

SINUSOIDAL PWM TECHNIQUE.

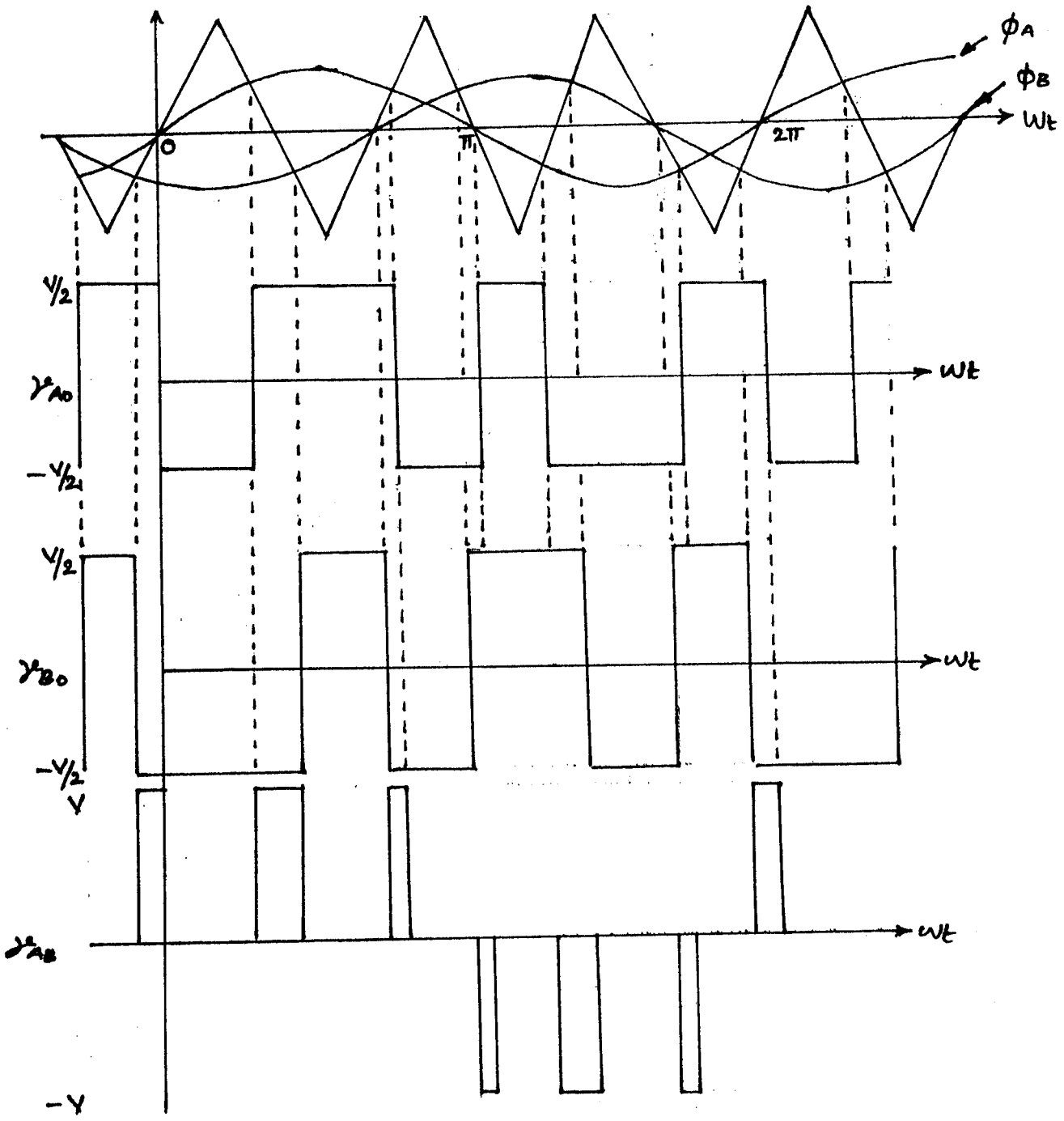


FIG I.2.4.3

power factor deteriorates due to phase shift control and system stability may get affected.

A PWM inverter solves above problems the fundamental frequency output voltage is controlled electronically within inverter by PWM technique.

AC MOTOR DRIVES

II.1 INDUCTION MOTOR CHARATERISTICS

The stator when supplied with voltage produces a rotating air gap flux that rotates at a speed depending on supply freqeuncy.

Torque is produced by interaction of stator rotating field and rotor current induced by it.

Current in rotor is induced due to speed difference between the rotating field and rotor.

Rotor current depends on this speed difference i.e,the slip

Synchronous Speed, $N_s = 120f1/P$

f1 - supply frequency

P - No of poles.

Slip = $(N_s-N)/N_s$

N - actual rotor speed.

Rotor frequency, f2 = (Ns-N)P/120 = Sf1.

Torque speed characteristics (figure II.1) shows that at synchronous speed, torque is Zero. i.e, at S = 0, T =0.

Motor operates at s=so developing T=To

At critical slip sc1 motor operates at stalling torque Tmax (motoring).

When S>1, the rotor operates in counter current braking condition and running motor comes to rest.

If supply is maintained motor rotates in opposite direction(plugging).

Slip becomes -Ve when motor runs above synchronous speed and the motor operates in a regenerative braking condition (generator region).

INDUCTION MOTOR CHARACTERISTICS.

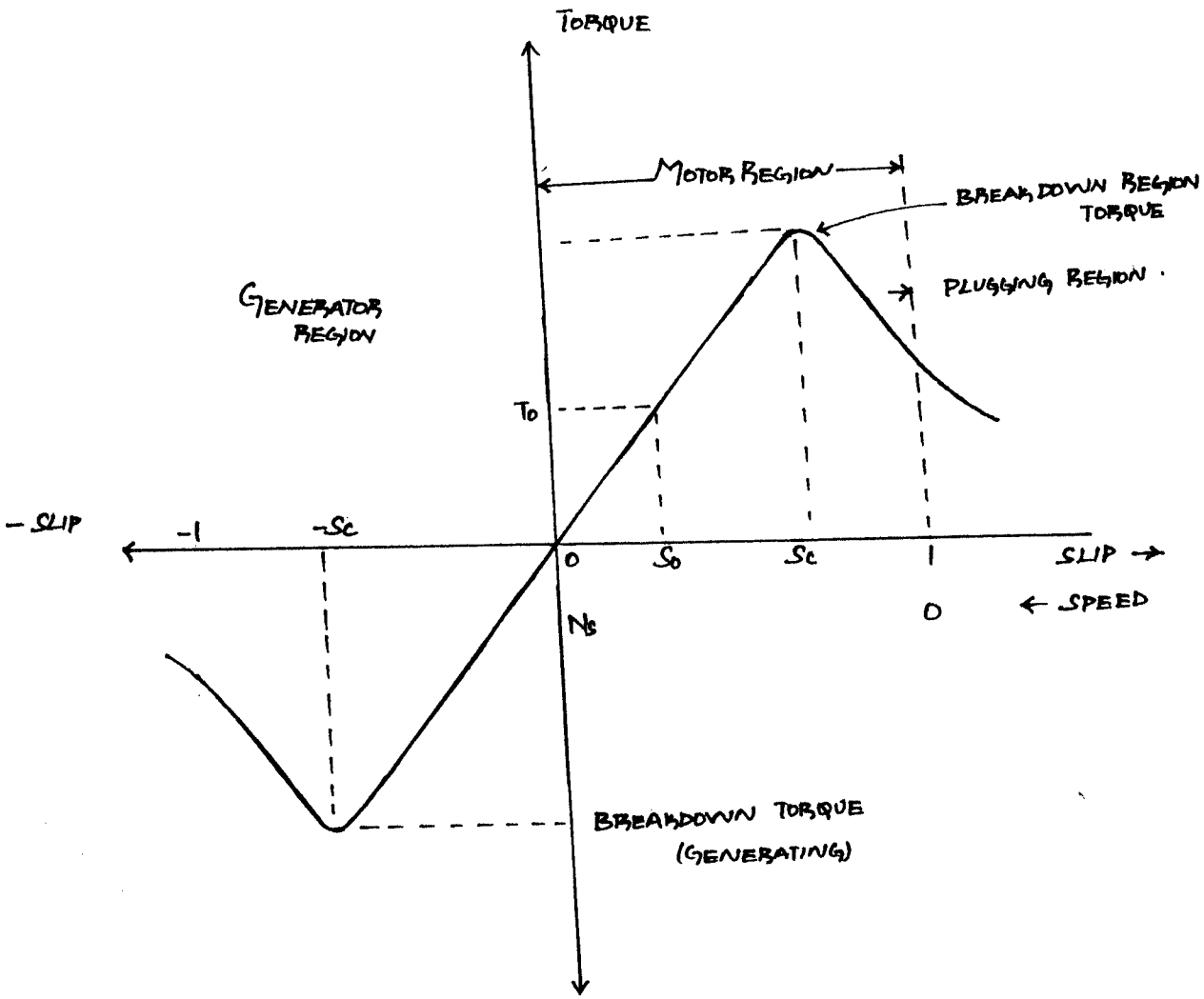


FIG II.1.

II.2. MOTOR REQUIREMENTS WHEN FED BY AN INVERTER:

* For a voltage fed inverter a high leakage inductance is preferred in the machine so that resulting harmonic currents are low.

* With inverter supply, the rotor can use copper bars so that copper loss is reduced substantially.

* The skin effect due to harmonic in the stator can be ignored but may be substantial in the rotor due to bar structure. So the bars may be designed as coffin shaped with wider area on top.

* Hysterisis and eddy-current losses are to be designed to be lower so that the machine operates at high efficiency.

* For a PWM inverter drive, the switching frequency can be adapted so that the composite inverter loss and machine loss are minimum in the whole range.

* Other effects namely harmonic torque pulsation , dc offset, shoot - through fault and so on should receive proper consideration in machine design.

The inverter has to be designed for nearly peak power rating without leaving a margin for short-time increase in the power rating as the thermal time constant of power semiconductor elements is much shorter than that of machine.

II.3. ADJUSTABLE SPEED AC DRIVES

A combination of power electronic system such as a Voltage/Frequency controller and an eletric motor with associated control mechanism is referred as an adjustable speed drive.

There are various frequency conversion equipments that can be used for adjustable frequency AC drives such as adjustable frequency generators, rotating frequency changers, cyclo convertors and variable frequency inverters.

ROTATING FREQUENCY SUPPLY UNITS

Induction and synchronous generators:

The synchronous generators speed is varied by a variable speed dc motor coupled to it. By varying generation speed if it's frequency is varied to a wide range.

In induction generators output freqeuncy is equal to frequency of rotor supply in standstill condition. But when rotor is rotated in direction of revolution of its own field the output frequency of generator increases above

rotor supply frequency. If rotor is reversed output frequency decreases below rotor frequency.

The above frequency - conversion system is costly and bulky and efficiency is naturally low.

* Inverters have now replaced these motor generator sets. The choice of power semiconductor driving system depends on the available power supply and load characteristics.

MOTOR CONTROL

III.1. OPEN LOOP VOLTS/HERTZ SPEED CONTROL METHOD

In the open loop motor control method shown in figure III 1, the power circuit consists of a phase controlled rectifier with single or 3 phase AC supply, LC filter, (six-stepped) inverter.

* We* is the command variable that determines motor speed.

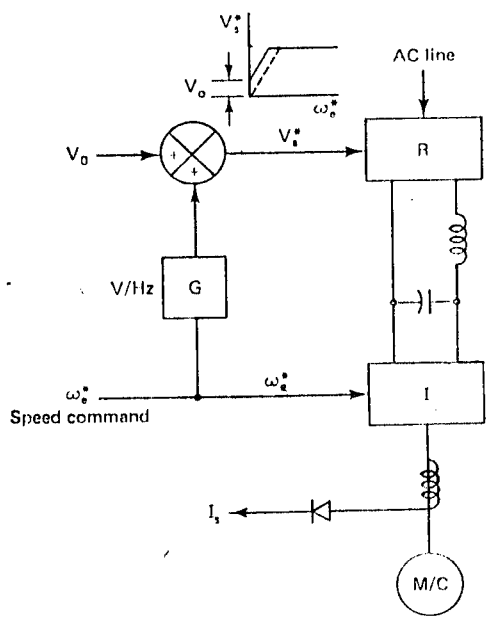
* Vs* is the vottage command to rectifier generated from frequency signal through a volts/Hertz gain constant G

* In this system the speed will tend to drift with variation in load Torque and fluctuations is supply.

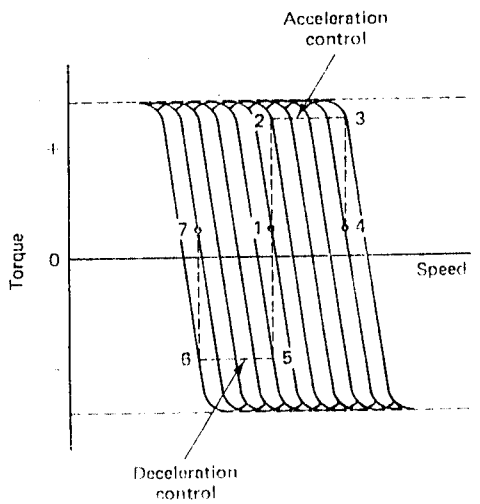
III.2 CLOSED LOOP CONTROL

The open-loop control of a motor in variable frequency-variable voltage mode is satisfactory for long term steady state operation. But it operating conditions demand rapid loop acceleration and deceleration, open

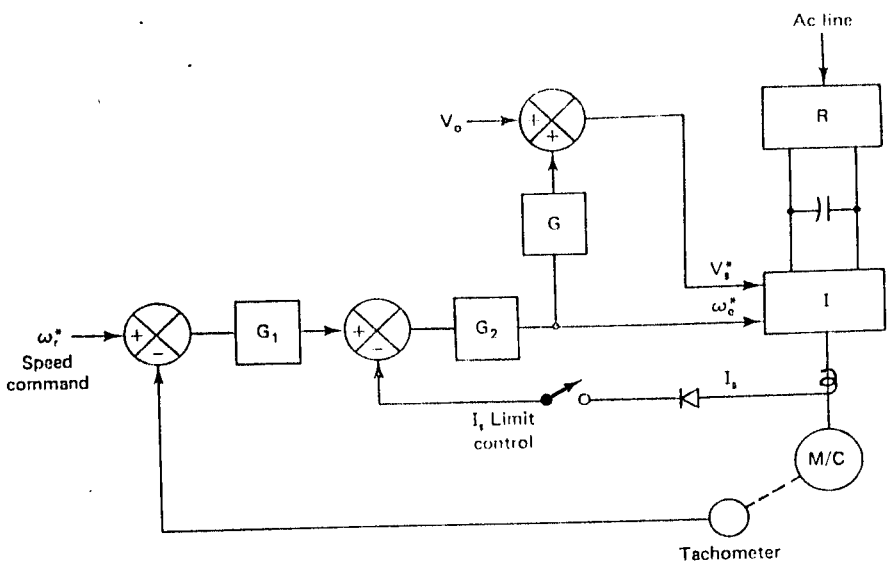
OPEN LOOP VOLTS/HERTZ CONTROL



ACCELERATION AND DECELERATION CHARACTERISTICS.



CLOSED LOOP VOLTS/HERTZ SPEED CONTROL.



loop control becomes unsatisfactory because frequency and voltage cannot be altered rapidly.

Therefore for fast dynamic response, closed loop control is essential to achieve optimum operating conditions. It offers speed control with high torgue, power factor and efficiency.

* The speed loop error signal controls the PWM inverter frequency and voltage through the current-limit controller.

III.3 VECTOR CONTROL METHODS (Advanced methods)

An AC machine is controlled like a separatory excited dc machine.

In a dc machine, torque is

$$Te = K'_t + I_a + I_f$$

Ia - armature or forgue component of current

If - field or flux component

The control variable Ia and If can be considered as orthogoral or decoupled `Vectors'

In normal operation, the field current I_f is set to maintain rated field flux and torque is changed by changing the armature current. As I_f and I_a are decoupled, torque sensitivity is maximum in both transient and steady state operations.

The above mode of control can be extended to induction motors, its operation is considered in a synchronously rotating frame where sinusoidal variables appear as dc quantities.

Currents i_{ds} and i_{qs} are direct-axis component and quadrature-axis components of stator current where both are in a synchronously rotating reference frame.

The concept of how i_{ds} and i_{qs} can be established as controlvector in vector control method is explained with phasor diagrams in a synchronously rotating $d_e q_e$ reference frame as shown.

The phasor is drawn taking air gap voltage $\hat{V}_g$ along q_e axis.

Stator current $I^{\wedge}_s$ lags the voltage $V^{\wedge}_g$ by (90-0) ie, $i_{qs} = I^{\wedge}_s$. sin in phase with $V^{\wedge}_g$ and $i_{ds} = I^{\wedge}_s$ cos in quadrature with V_g.

i_{qs} is the active or torque compoent of stator current.

i_{ds} is reactive or field component of stator current and is responsible for establishing air gap flux $*_m$.

From the Phasor diagram, the torgue developed across the air gap is

$Te = Kt /*m/iqs = K'_t i_{qs} i_{ds}$

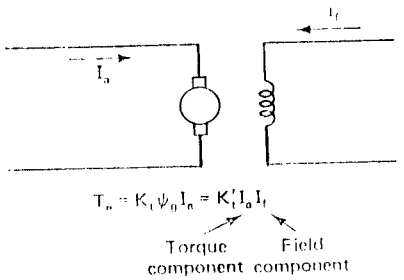
The variables i_{qs} and i_{ds} are mutually decoupled and can be independently varied without affecting orthogonal component.

i_{qs} varied to vary torque.

Advantages

* In addition to fast transient response due to decoupling control high stability is offered to an induction motor.

* The control can easily be designed to have a 4 quadrant operation.



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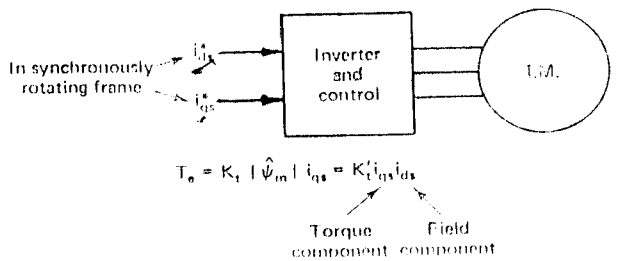
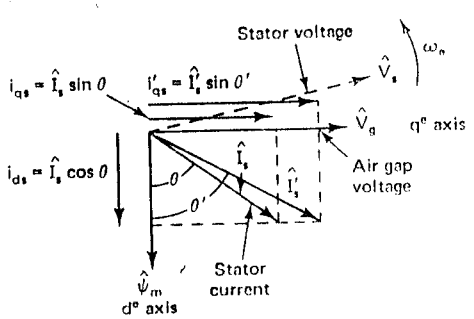
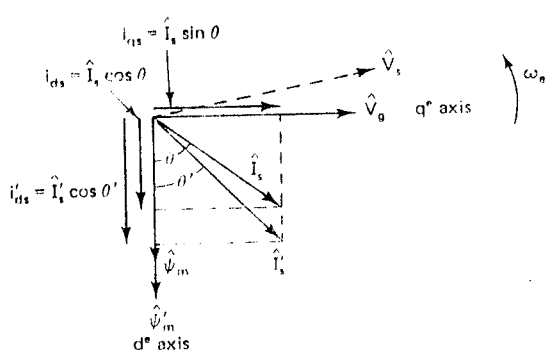


INDUCTION MOTOR AND DC MACHINE ANALOGY IN VECTOR CONTROL.



Increase of Torque Component



Increase of Field Component

PHASOR DIAGRAM IN DIRECT VECTOR CONTROL

Applications (High performances applications):

Servo drives

Steel mill controls,etc

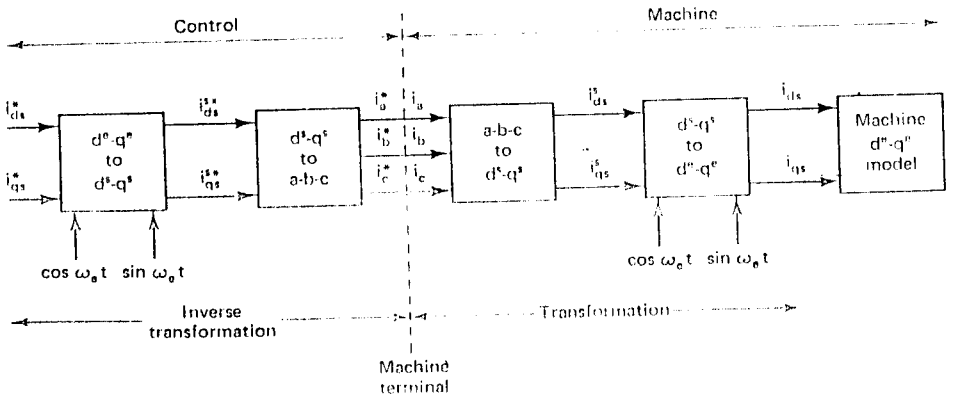
VECTOR CONTROL IMPLEMENTATION WITH MACHINE MODEL

Inverter is assumed to generate the ideal phase current waves i_a , i_b , i_c as dictated by corresponding reference waves generated by controller.

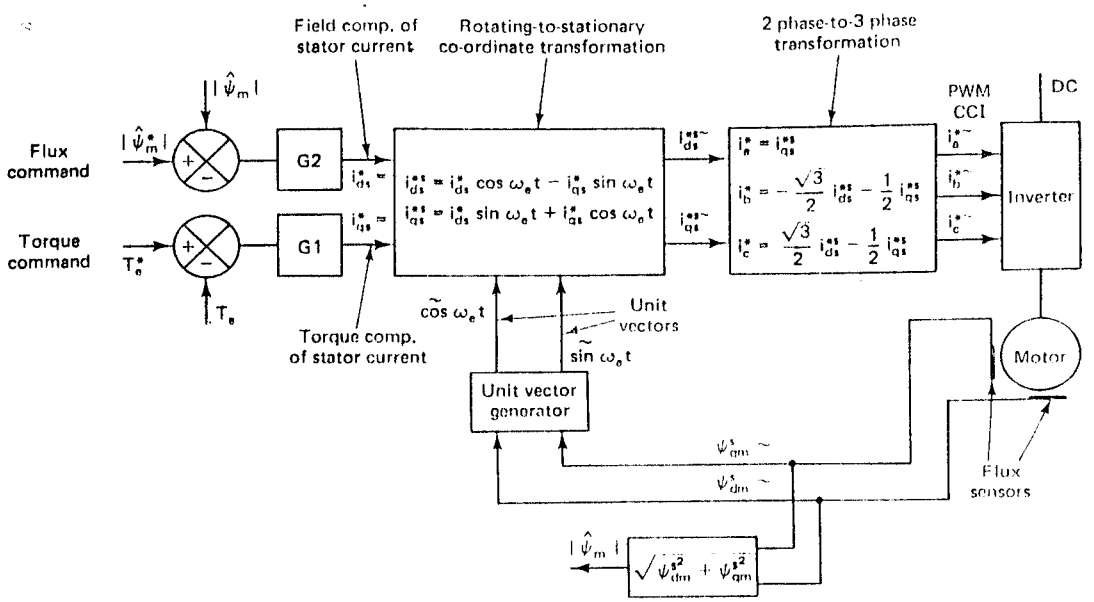
i_a , i_b and i_c are converted to i^s_{qs} gs and i^s_{ds} components by three phase / two phase transformation.

These are then converted to a synchronously rotating reference frame by unit vectors coswet and sinwet before being applied to machine model. The unit vectors assume the alignment of ids with the $\varphi^\wedge_m$ phasor and i_{qs} with V_g Phasor.

The controller makes two inverse transformations so that control parameters i_{ds}^* aand i_{gs}^* correspond to machine variables i_{ds} and i_{gs}.



VECTOR CONTROL IMPLEMENTATION WITH MACHINE MODEL.



DIRECT METHOD OF VECTOR CONTROL OF A VOLTAGE FED INVERTER.

BASIC BLOCK DIAGRAM OF VECTOR CONTROL METHOD FOR A PWM CURRENT CONTROLLED INVERTER

As shown in figure the principal control parameters i_{ds}^* and i_{qs}^*, which are dc quantifies, are converted to a stationary reference frame with the help of coswet and sinwet signals generated from flux signals.

Resulting stationary frame signals are converted to phase current commands for inverter.

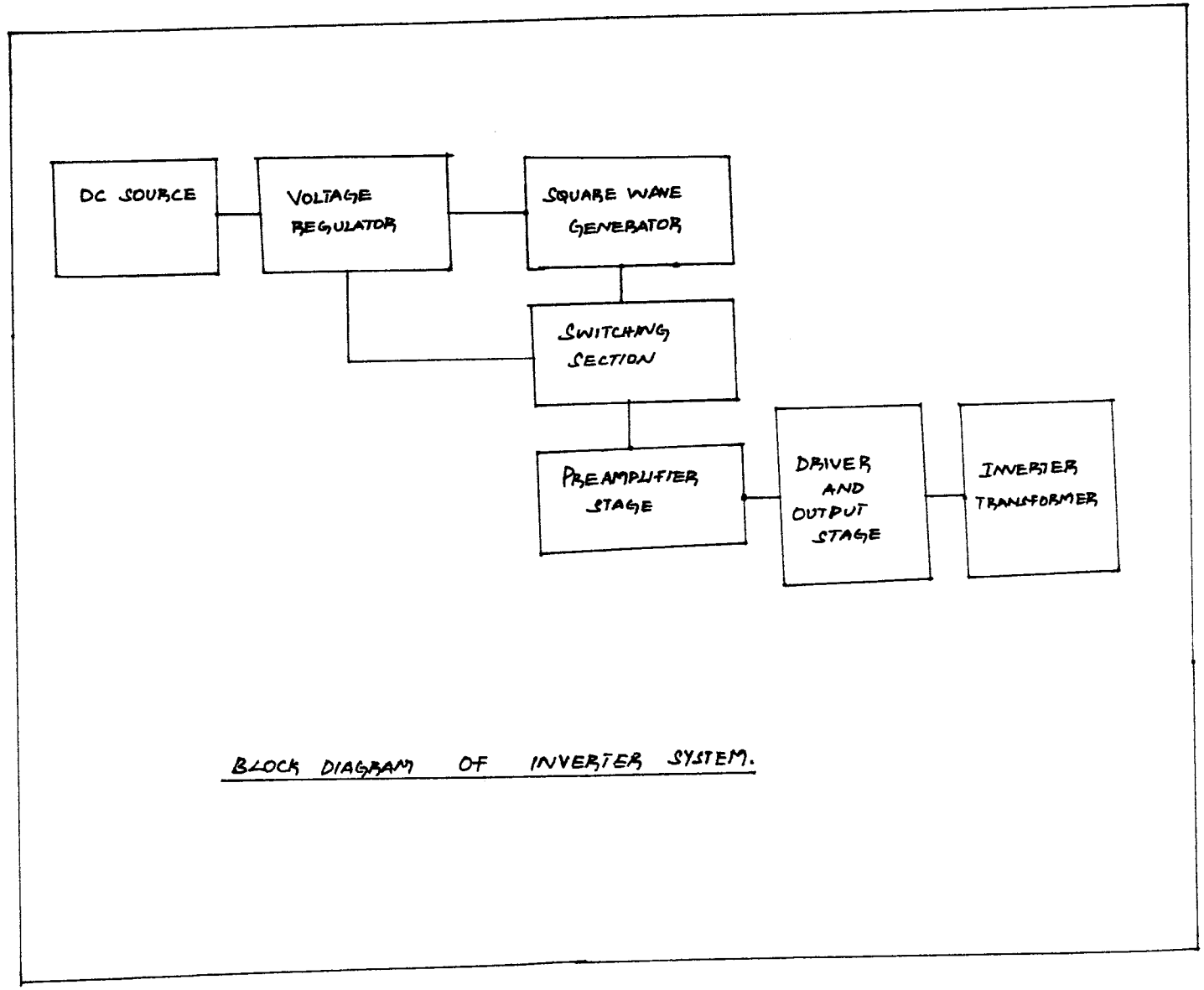
Current i_{qs}^* is generated from a torgue control loop.

Airgap fluxes φ^sdm and φ^sqm can be measured from stator voltage and current.

INVERTER SYSTEM

IV.1. BLOCK DIAGRAM DESCRIPTION

The dc battery source is the first andforemost block of the inverter system. The voltage regulatorthat follows the source is used to convert the high voltage dc supply into a lower value so as provide the required supply to the subsequent sections. The squarewave generator that follows the regulator converts the constant dc into a square wave. The switching sections consists of j - k flipflops which get triggered by the square wave clock pulses thus acting as switches. The Pre amplifier section is responsible for amplifying the switched signal that acts as the input for the driver stage which in turn drives the output power amplifier stage. This power amplifier stage is responsible for the amplification of power. The Invertor Transformer is the last stage that proviodes a stepped up ac output at designed frequency and wattage.



BLOCK DIAGRAM OF INVERTER SYSTEM.

IV.2. INVERTER CIRCUIT DESCRIPTION

BATTERY

It is the source of dc power that is to be inverted into a.c power. Usually the battery sources a high dc power that can't directly be applied to the subsequent IC stages that follow.

IC REGULATOR

The Ic regulator section incorporates IC7805 that regulates the input dc power from battery to a value of +5volts. The input d.c has to be applied to pin 1 to get output at pin 3 , pin2 has to be grounded.

SQUARE WAVE GENERATOR (IC555)

IC555 is a timer IC that works on the 5V from regulator. The 5v dc is given to pins 4 and 8. A trigger input at pin 2 will generate a square wave output at pin 3. The width of the square pulse is adjustable and this enables output frequency variations.

SWITCHING SECTION (IC 7473)

IC 7473 that performs the switching operation has two J-K flipflops with one input and two outputs. But we use only one flipflop. When the ouput of the square wave generator is applied to pin 1, We get outputs through pins 8 and 9.

The input from timer IC acts as clock input to the switching J-K flipflops. The clock input causes a positive pulse output at pin 8 and a negative pulse at pin 9. When the next clock pulsė arrives at pin 1,the reverse action happens ie,at pin8 we get a negative pulse and at pin 9 we get a positive pulse. Thus this section acts as on and off switch.

PRE AMPLIFIER SECTION

This section consists of two stages of transistor amplifiers. The first stage includes D100 (NPN) and the second stage comprises of C100 (PNP).

DRIVER AND POWER AMPLIFIER STAGE

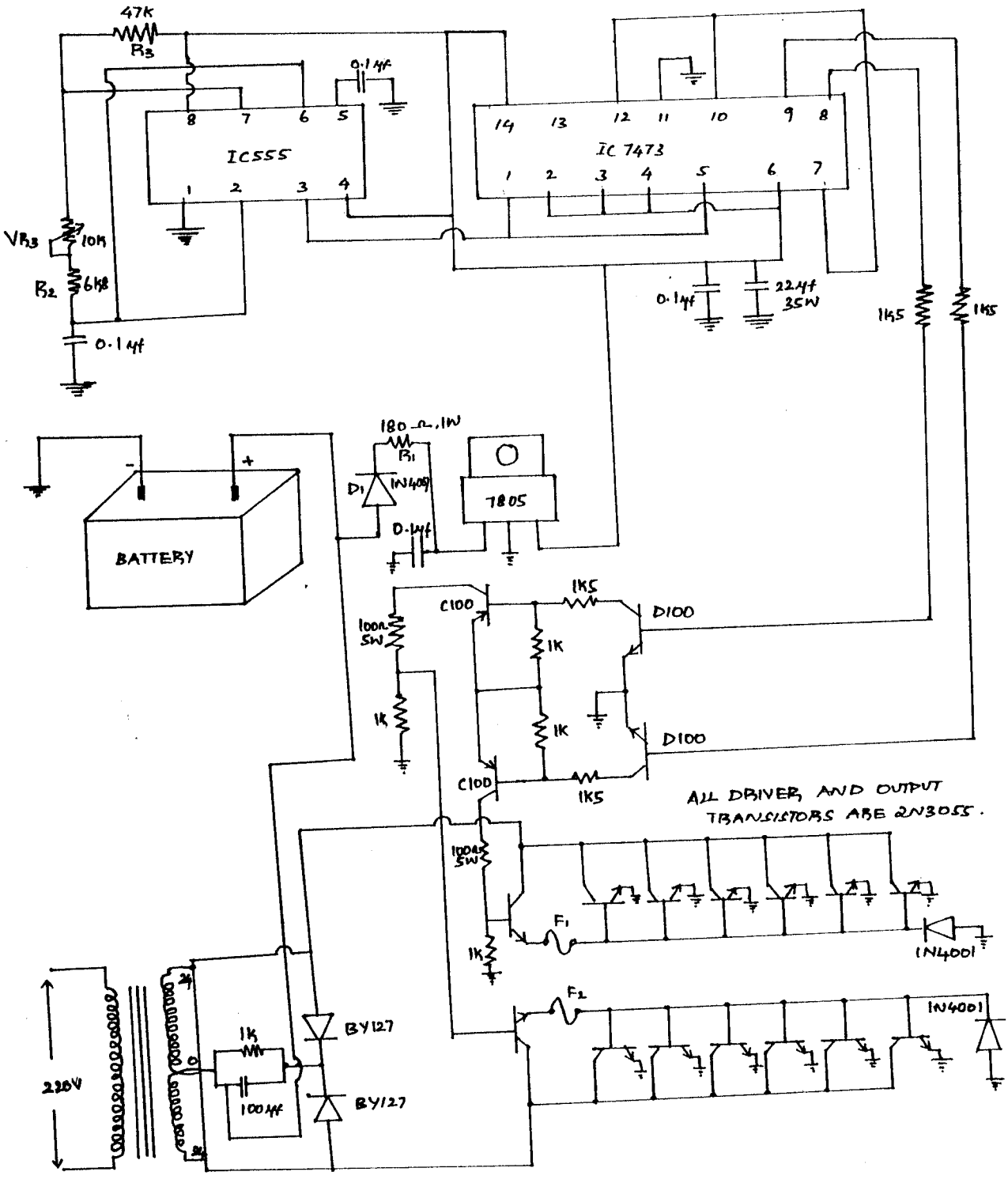
The driver stage consisting of 2N3055 provides base drive for the power amplifier stage that comprises of six 2N3055 power transistors in parallel. The number of output power transistors depend on the load.

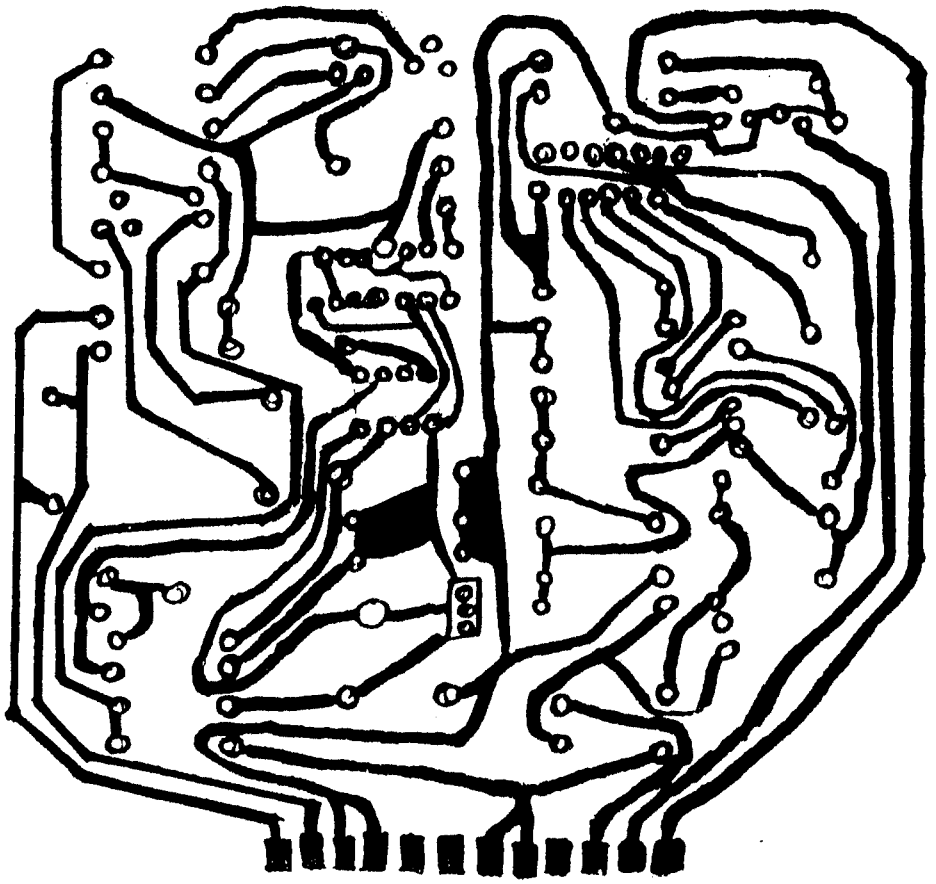
INVERTER TRANSFORMER

The Invertor transformer is basically a step up transformer. The 24vac from the output section is stepped up to 230V. Cold rolled Grain oriented stampings are used for core with the primary having 57 turns and secondary 264 turns.

The Zener diodes that are grounded in the output section are to present the output transistors from the high voltage that might reach than due to output transformers inductive nature.

INVERTER CIRCUIT





IV.3. SELECTION OF TRANSISTOR

Parameters to be considered:

Max C - E voltage V_{cco}

Max collector current

Max power dissipation

Collector volt-second breakdown rating, junction - case thermal resistance,

Min current gain at max load current storage times.

* In a push-pull inverter, voltage across total primary winding is $2(V_{cc}-V_{ce\ sat})$ due to autotransformer action.

VCEsat of two transistors should be equal ,else the voltage across py will not be equal and hence the core will move either into +ve or -ve saturation.

Transformer py should bifiliar, So that flux swing during +ve and -ve cycles is the same.

C-E voltage of each transistor must be higher than twice the supply voltage. Again due to transformer leakage and lead inductances incollector leads , there are voltage spikes whose magnitude may be as high as 20% of transformer primary voltage.

The collector emitter voltage should be atleast 2x1.2 (1+x) Vcc, where x is per unit fluctuation of supply voltage.

The C-E voltage rating be chosen after considering B-E circuit impedance. If off period base - circuit impedance is above 150 ohm, Vceo rating be taken. If it is less than 50 ohm Vceo rating be considered. But, if it lies between 50 ohm and 150 ohm the Vcer rating that lies between

* Current rating of transistor should be selected from magnitude of load current reflected on primary of transformer and its magnetising current. Peak current rating should be atleast 50% higher than peak load current. Also the main value of hFE at peak load current should be sufficiently high to drive the transistor well into saturation.

* Max permissible power dissipation in a transistor depends on thermal impedance.

$p = T_{jmax} - T_{cmax}$

T_{jmax} - max junction temperature

T_{cmax} - Thermal resistance between junction and case.

T_{jmax} for Si power transistor is 175°C or 200°C. But for safe operation T_{jmax} should be 130°C to 140°C.

* To ensure fast turn on, base-drive current be more than required Icmax/B. Large storage time will lead to simultaneous conduction of transistor.

IV.4. TRANSFORMER DESIGN

Preliminary Design:

As the first step tp design of transoformer, the primary and secondary voltage ratings and the primary current ratings and the secondary current rating must be clearly stated. Then decide on the core material to be used: Ordinary steel stampings (or) cold rolled grain oriented (CRGO) stampings. CRGO has a higher allowable flux density and lower losses.

The optimum cross-sectional area of the core is approximately given by:

Core area = $1.152\sqrt{\text{output}}$ voltage x output current sq.cm

For transformers with multiplle secondaries, the sum of the output volt-ampere product of each winding is to be used.

The number of turns on the primary and secondary windings is decided by the turns per volt ratio as

Turns per volt = $1/(4.44 \times 10^{-4} \times \text{frequency} \times \text{corearea} \times \text{flux density})$

Frequency = 50 Hz

Flux density = 1.0 weber/Sq.m for ordinary steel stampings ,

and 1.3 Weber /sq.m for CRGO stampings.

PRIMARY WINDING DESIGN

The current in the primary winding is given by primary

current = output volts x output amps/ primary volts x efficieny

The efficiency of small transformers varies between 0.8 to 0.96. A valve of 0.87 can be used for ordinary transformers.

The proper wire size has to be selected for the winding. The wire diameter depends on the current to be supplied by the winding and the allowable current density of the wire.

Usually, a valve of 200 amps /sq.cm can be taken , on whose basis table I is given.

The number of turns in the primary winding is given by primary turns = Turns per volt x primary volts.

The space taken up by the winding will depend on the insulation thickness, method of winding and the wire diameter. Table I gives the approximate value of the turns per square and from which we can estimate the window area occupied by the primary winding.

Primary winding area = primary turns/Turns per sq.cm from table I

SECONDARY WINDING AREA

Since we have assumed that we know the secondary current rating, we can find out the wire size for the secondary winding by referring to Table I directly.

The number of turns on the secondary is calculated in the same way as for the primary, but about 3% extra turns are to be added to compensate for the internal drop of secondary voltage of the transformer, upon loading.

Thus secondary turns = 1.03(turns per volt x secondary voltage)

The window area required for secondary winding is found from Table I as

Secondary window area = secondary turns/Turns per sq.cm from

CORE SIZE

The main criterion in selecting the core is the total window area of winding space available.

Total window area = primary window area + sum of secondary window areas + space for former and insulation.

Some extra area is required to accomodate the former and insulation between windings. The actual amount of extra varies, although 30% may be taken to start with but may have to modified later. The suitable core sizes having a larger window area are selected from Table II

Taking into account the gap between laminations while stacking them, we have Gross core area = core area /0.9 sq.cm

In general, a square central limb is preferred for this, the width of tongue of lamination is

Tongue width = $\sqrt{\ }$ gross core area cm

Table 1 : WINDING DATA ON ENAMELLED COPPER WIRE (@ 200 Amp/sq. cm.)

SWG	Max. current capacity (Amp)	Turns per sq. cm.	SWG	Max. current capacity (Amp)	Turns per sq. cm.
10	16.60	8.7	30	0.1558	881
11	13.638	10.4	31	0.1364	997
12	10.961	12.8	32	0.1182	1137
13	8.579	16.1	33	0.1013	1308
14	6.487	21.5	34	0.0858	1608
15	5.254	26.8	35	0.0715	1902
16	4.151	35.2	36	0.0586	2286
17	3.178	45.4	37	0.0469	2800
18	2.335	60.8	38	0.0365	3507
19	1.622	87.4	39	0.0274	4838
20	1.313	106	40	0.0233	5595
21	1.0377	137	41	0.0197	6543
22	0.7945	176	42	0.0162	7755
23	0.5838	42	43	0.0131	9337
24	0.4906	286	44	0.0104	11457
25	0.4054	341	45	0.0079	14392
26	0.3284	415	46	0.0059	20223
27	0.2726	504	47	0.0041	27546
28	0.2219	609	48	0.0026	39706
29	0.1874	711	49	0.0015	62134
			50	0.0010	81242

Table 2 :
TABLE DIMENSIONS OF TRANSFORMER STAMPINGS

Type No.	Tongue width (cm.)	Window area (sq. cm.)	Type No.	Tongue width (cm.)	Window area (sq. cm.)
17 (E-I)	1.270	1.213	9 (U-T)	2.223	7.865
12A (E-I)	1.588	1.897	9A (U-T)	2.223	7.865
74 (E-I)	1.748	2.284	11 A (E-I)	1.905	9.072
23 (E-I)	1.905	2.723	4A (E-I)	3.335	10.284
30 (E-I)	2.000	3.000	2 (E-I)	1.905	10.891
21 (E-I)	1.588	3.329	16 (E-I)	3.810	10.891
31 (E-I)	2.223	3.703	5 (E-I)	3.810	12.704
10 (E-I)	1.588	4.439	4AX (U-T)	2.383	13.039
15 (E-I)	2.540	4.839	13 (E-I)	3.175	14.117
33 (E-I)	2.800	5.880	75 (U-T)	2.540	15.324
1 (E-I)	2.461	6.555	4 (E-I)	2.540	15.865
14 (E-I)	2.540	6.555	7 (E-I)	5.080	18.969
11 (E-I)	1.905	7.259	6 (E-I)	3.810	19.356
34 (U-T)	1/588	7.259	35A (U-T)	3.810	39.316
3 (E-I)	3.175	7.562	8 (E-I)	5.080	49.803

Now refer to table II again and finally select the proper core size, with sufficient window area and a dose value of the tongue width as calculated. Adjust the stack height as required to obtain the required core section

Stack height = Cross core area/actual tongue width cm

The stack should not be much less than the tongue width but may be more. However, it should not be more than 11/2 times the tongue.

TRANSFORMER DESIGN

The design of 600 watts transformer, which is used in our application is as follows

core area = 1.152 x $\sqrt{output\ voltage}$ x $\sqrt{output\ current}$
= 1.152 x $\sqrt{230x2.6}$ = 28.17 Sq.Cm

Gross Core Area = 28.17sq.cm/0.9 = 31.3 Sq.Cm.

Tongue Width = 31.3 Sq.Cm = 5.59 cm.

PRIMARY WINDING

Primary Voltage = 24V

Primary current = (230x2.6/24x0.87) = 28.64A

Turn per volt = $1/(4.44x10^{-4}x50x28.17x1.3)$ = 1.2

Primary Turns = 48 x 1.2 = 57 turns

The wire selected is 7SWG x 2.

SECONDARY WINDING

Secondary Voltage = 220V

Secondary Current = 2.6A

Turn per Volt = $1/(4.44 \times 10^{-4} \times 50 \times 28.17 \times 1.3) = 1.2$

Secondary Turns = 1.03(220x 1.2)

= 264 Turns.

The wire selected is 17SWG.

IV.5. WORKING PRINCIPLE:

The dc supply from battery is regulated by the voltage regulator to around 5 volts. This 5 volts is applied to IC 555 and IC 7473. When triggered at Pin 2, IC 555 produces a square wave.

The trigger pulse is produced through 100k potential divider and capacitor C4. The width of the square wave can be djusted by varying the 100K potentiometer. Thus the output frequency can be varied. The square wave generated acts as clock, input to the switching J-K flipflops of IC 7473. Due to the square wave clock, the outputs at pin 8 and pin 9 of IC 7473 continuously reverses in polarity. ie it acts as a switch. This switching action switches ON and OFf the subsequent transistor stages and is thus responsible for the production of ac output. The inverter transformer steps up the ac power thus produced to the required value.

CONCLUSION

Inverter motors are having a very good future in India. In textile machine tool and cement industries specific applications. The possibility of manufacturing inverters are good only for small ratings. PWM, constant current inverters, constant voltage inverter with high capacity are done only with imported components. The companies like Mitsubishi, siemens, AMTECH, kirloskar are doing the same thing with imported components. Because of globilisation so many companies from U.S, Europe and Japan have also starting their branches. Hence the future for inverter with variable frequency for induction motor drive looks bright.

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National Semiconductor

555/LM555C Timer

ral Description

555 is a highly stable device for generating ...ise delays or oscillation. Additional terminals ...ided for triggering or resetting if desired. In the ...ay mode of operation, the time is precisely con... by one external resistor and capacitor. For astable ...on as an oscillator, the free running frequency and ...ty cycle are accurately controlled with two external ...s and one capacitor. The circuit may be triggered ...set on falling waveforms, and the output circuit ...rce or sink up to 200 mA or drive TTL circuits.

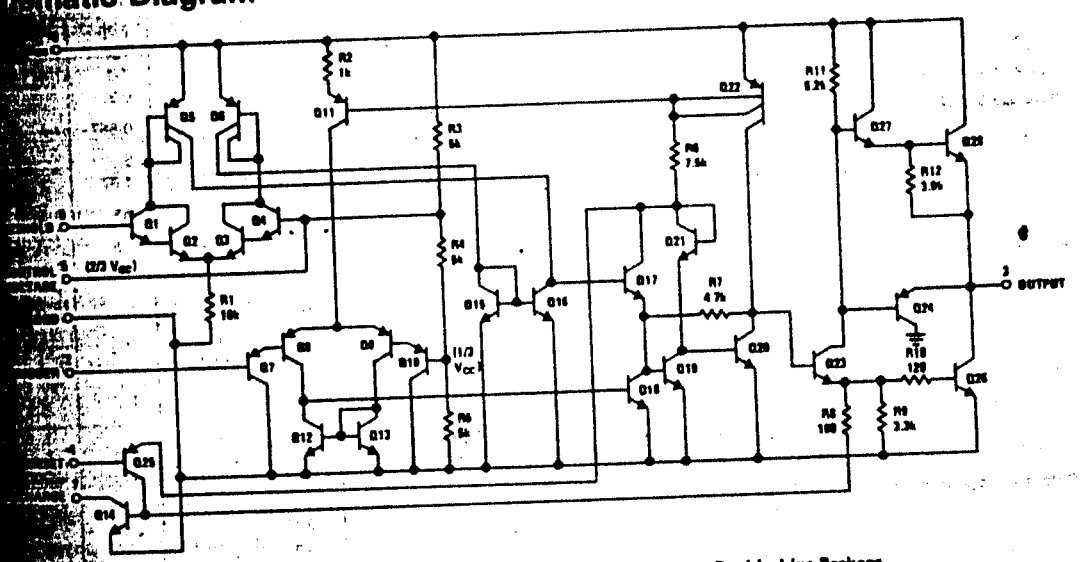
tures

- ...replacement for SE555/NE555
- ...ing from microseconds through hours
- ...ates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

Applications

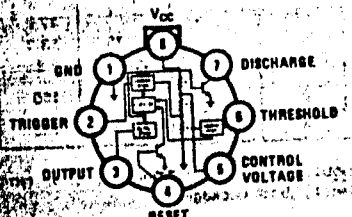
- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

matic Diagram



nnection Diagrams

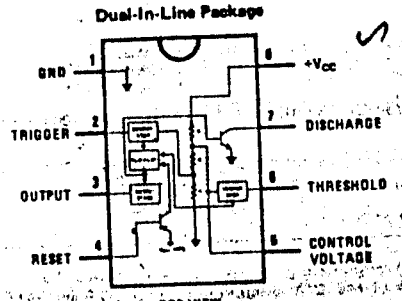
Metal Can Package



TOP VIEW

Order Number LM555H, LM555CH
See NS Package H08C

Dual-In-Line Package



TOP VIEW

Order Number LM555CN
See NS Package N08B
Order Number LM555J or LM555CJ
See NS Package J08A

Absolute Maximum Ratings

Supply Voltage	+18V
Power Dissipation (Note 1)	600 mW
Operating Temperature Ranges	
LM555C	0°C to +70°C
LM555	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LM555			LM555C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	5		3	6	mA
	V_{CC} = 15V, R_L = ∞ (Low State) (Note 2)		10	12		10	15	mA
Timing Error, Monostable								
Initial Accuracy			0.5			1		%
Drift with Temperature	R_A, R_B = 1k to 100 k, C = 0.1μF, (Note 3)		30			50		ppm/°C
Accuracy over Temperature			1.5			1.5		%
Drift with Supply			0.05			0.1		%/V
Timing Error, Astable								
Initial Accuracy			1.5			2.25		%
Drift with Temperature			90			150		ppm/°C
Accuracy over Temperature			2.5			3.0		%
Drift with Supply			0.15			0.30		%/V
Threshold Voltage			0.667			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2		5		V
	V_{CC} = 5V	1.45	1.67	1.9		1.67		V
Trigger Current			0.01	0.5		0.5	0.9	μA
Reset Voltage		0.4	0.5	1	0.4	0.5	1	V
Reset Current			0.1	0.4		0.1	0.4	mA
Threshold Current	(Note 4)		0.1	0.25		0.1	0.25	μA
Control Voltage Level	V_{CC} = 15V	9.6	10	10.4	9	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Pin 7 Leakage Output High			1	100		1	100	nA
Pin 7 Sat (Note 5)								
Output Low	V_{CC} = 15V, I_7 = 15 mA		150			180		Ω
Output Low	V_{CC} = 4.5V, I_7 = 4.5 mA		70	100		80	200	Ω
Output Voltage Drop (Low)	V_{CC} = 15V							
	I_{SINK} = 10 mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50 mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100 mA		2	2.2		2	2.5	V
	I_{SINK} = 200 mA		2.5			2.5		V
	V_{CC} = 5V							
	I_{SINK} = 8 mA		0.1	0.25				V
	I_{SINK} = 5 mA					0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200 mA, V_{CC} = 15V		12.5			12.5		V
	I_{SOURCE} = 100 mA, V_{CC} = 15V	13	13.3		12.75	13.3		V
	V_{CC} = 5V	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns

Note 1: For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of +45°C/W junction to case for TO-5 and +150°C/W junction to ambient for both packages.

Note 2: Supply current when output high typically 1 mA less at V_{CC} = 5V.

Note 3: Tested at V_{CC} = 5V and V_{CC} = 15V.

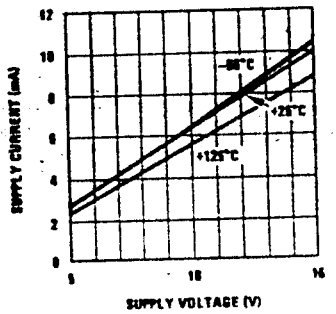
Note 4: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20 MΩ.

Note 5: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

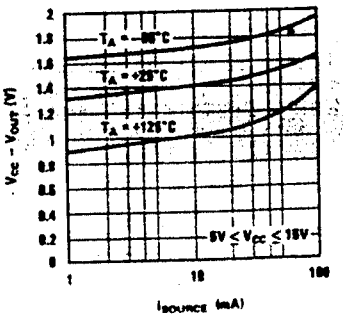
Performance Characteristics

LEVEL OF TRIGGER PULSE (X V_{CC})

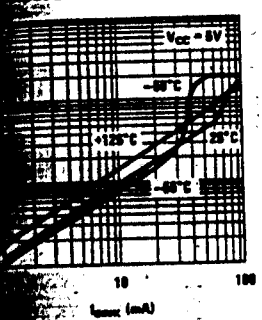
Supply Current vs
Supply Voltage



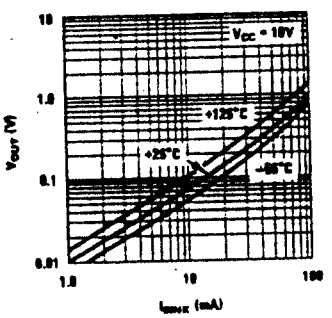
High Output Voltage vs
Output Source Current



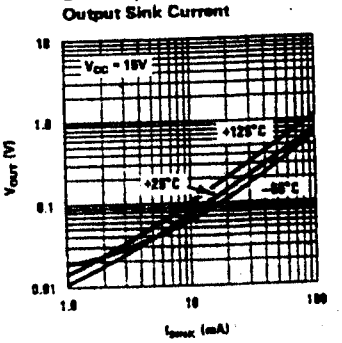
Output Voltage vs
Sink Current



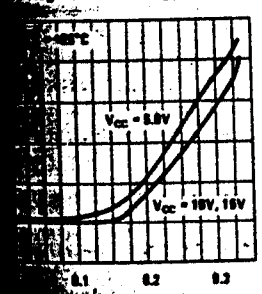
Low Output Voltage vs
Output Sink Current



Low Output Voltage vs
Output Sink Current

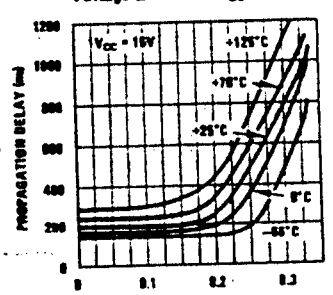


Output Propagation Delay vs
Voltage Level of Trigger Pulse

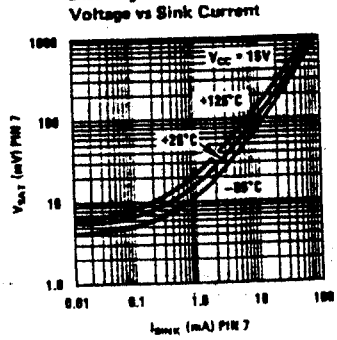


LEVEL OF TRIGGER PULSE (X V_{CC})

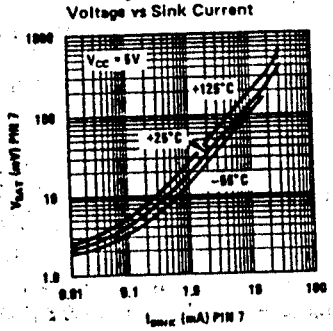
Output Propagation Delay vs
Voltage Level of Trigger Pulse



Discharge Transistor (Pin 7)
Voltage vs Sink Current



Discharge Transistor (Pin 7)
Voltage vs Sink Current



Applications Information

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (*Figure 1*). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative-trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

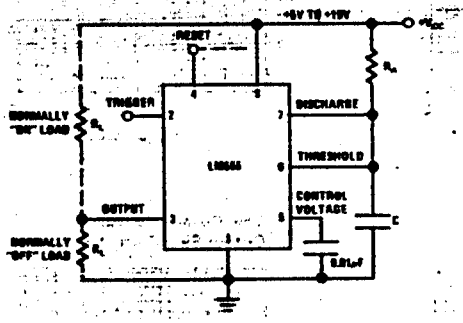


FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of $t = 1.1\ R_A C$, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.

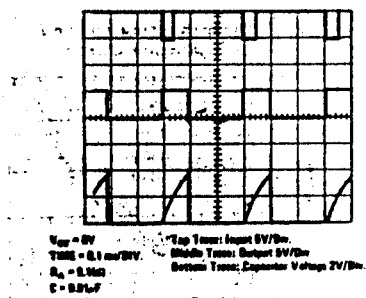


FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

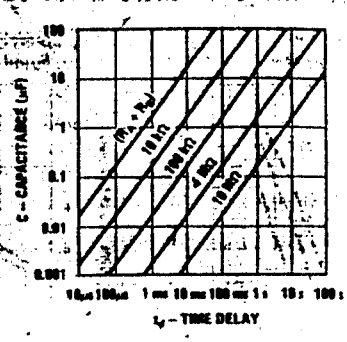


FIGURE 3. Time Delay

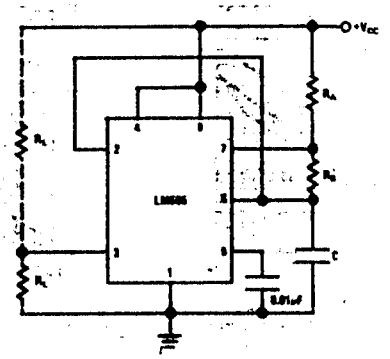


FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 5 shows the waveforms generated in this mode of operation.

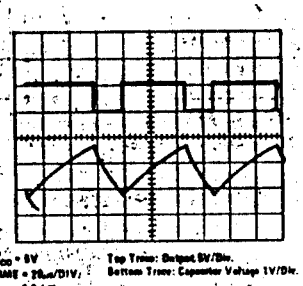


FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$$

...cations Information (Continued)

...quency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C}$$

...may be used for quick determination of these

...duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B}$$

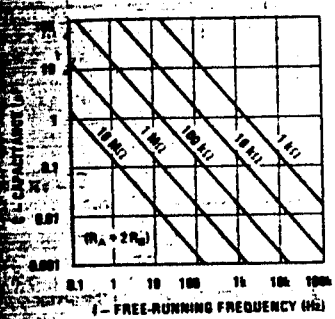


FIGURE 6. Free Running Frequency

...QUENCY DIVIDER

...monostable circuit of *Figure 1* can be used as a ...uency divider by adjusting the length of the timing ... *Figure 7* shows the waveforms generated in a ...ide by three circuit.

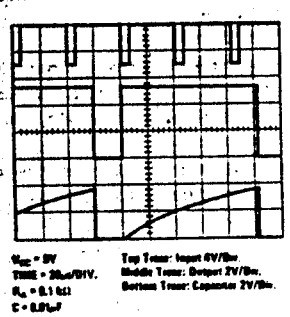


FIGURE 7. Frequency Divider

PULSE WIDTH MODULATOR

...the timer is connected in the monostable mode ...triggered with a continuous pulse train, the output ...width can be modulated by a signal applied to pin ... *Figure 8* shows the circuit, and in *Figure 9* are some ...veform examples.

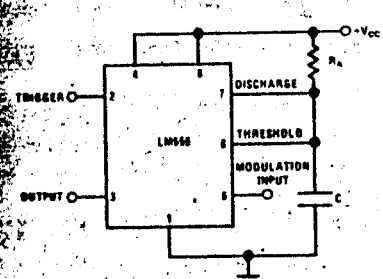


FIGURE 8. Pulse Width Modulator

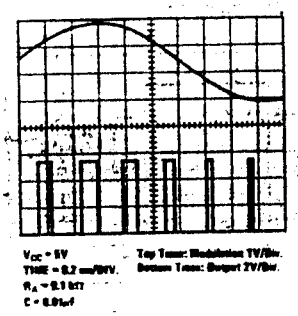


FIGURE 9. Pulse Width Modulator

PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in *Figure 10*, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.

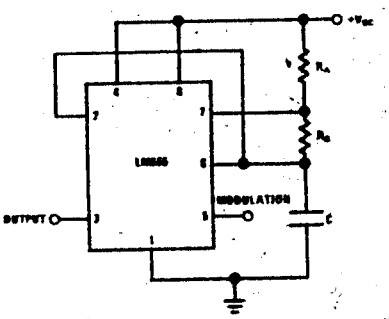


FIGURE 10. Pulse Position Modulator

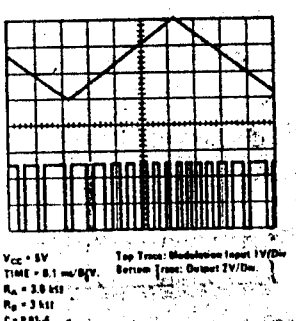


FIGURE 11. Pulse Position Modulator

LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is

Applications Information (Continued)

generated. *Figure 12* shows a circuit configuration that will perform this function.

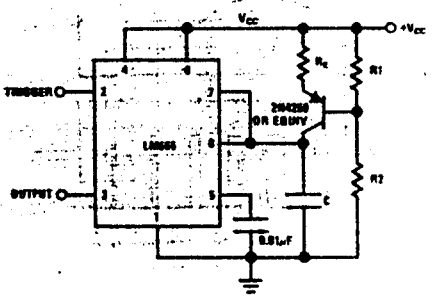


FIGURE 12.

Figure 13 shows waveforms generated by the linear ramp.

The time interval is given by:

$$T = \frac{2/3\ V_{CC}\ R_E\ (R_1 + R_2)\ C}{R_1\ V_{CC} - V_{BE}\ (R_1 + R_2)}$$

$V_{BE} \simeq 0.6V$

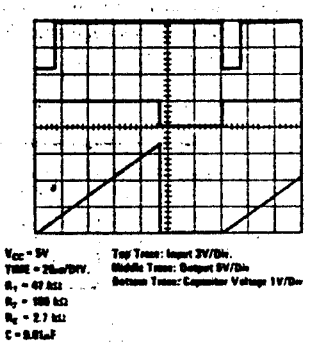


FIGURE 13. Linear Ramp

50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14*. The time period for the output high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is $t_2 =$

$$[(R_A\ R_B)/(R_A + R_B)]\ C \ln \left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is $f = \frac{1}{t_1 + t_2}$

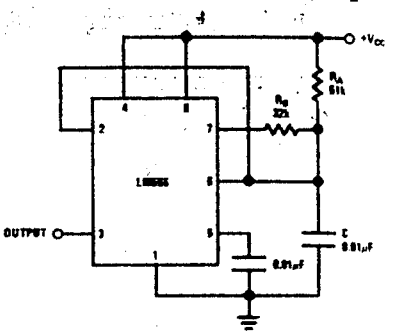


FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1μF in parallel with 1μF electrolytic.

Lower comparator storage time can be as long as 10μs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10μs minimum.

Delay time reset to output is 0.47μs typical. Minimum reset pulse width must be 0.3μs, typical.

Pin 7 current switches within 30 ns of the output (pin 3) voltage.

National Semiconductor

LM124/LM224/LM324, LM124A/LM224A/LM324A, LM2902 Low Power Quad Operational Amplifiers

General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5 V_{DC} power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15 V_{DC} power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

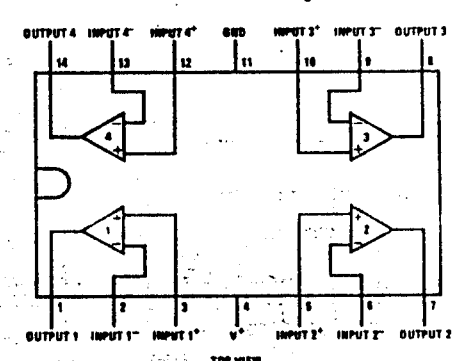
- Eliminates need for dual supplies
- Four internally compensated op amps in a sing package
- Allows directly sensing near GND and V_{OUT} al goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Internally frequency compensated for unity gain
- Large dc voltage gain 100 d
- Wide bandwidth (unity gain) (temperature compensated) 1 MH
- Wide power supply range:
  - Single supply .3 V_{DC} to 30 V_D
  - or dual supplies ±1.5 V_{DC} to ±15 V_D
- Very low supply current drain (800μA) — essentiall independent of supply voltage (1 mW/op amp +5 V_{DC})
- Low input biasing current 45 nA_D (temperature compensated)
- Low input offset voltage 2 mV_D and offset current 5 nA_D
- Input common-mode voltage range includes groun
- Differential input voltage range equal to the powe supply voltage
- Large output voltage swing 0 V_{DC} to V^+ − 1.5 V_D

Connection Diagram

Dual-In-Line Package

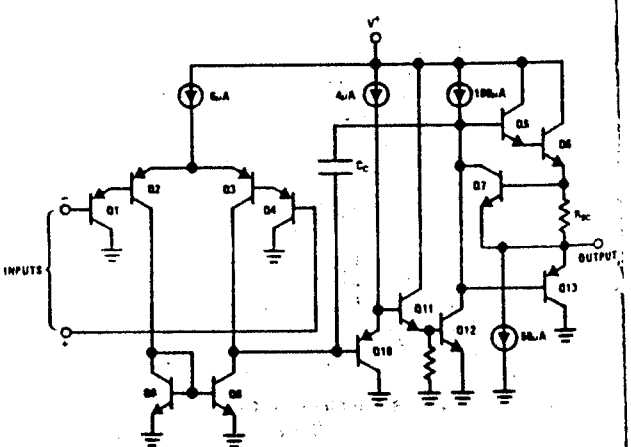


TOP VIEW

Order Number LM124J, LM124AJ, LM224J, LM224AJ, LM324J, LM324AJ or LM2902J
See NS Package J14A

Order Number LM324N, LM324AN or LM2902N
See NS Package N14A

Schematic Diagram (Each Amplifier)



Differential Input Voltage	32 V_{DC}	26 V_{DC}	
Input Voltage	−0.3 V_{DC} to +26 V_{DC}	−0.3 V_{DC} to +26 V_{DC}	
Power Dissipation (Note 1)			
Molded DIP	570 mW	570 mW	
Cavity DIP	900 mW		
Flat Pack	800 mW		
Output Short-Circuit to GND (One Amplifier) (Note 2) $V^+ \leq 15\ V_{DC}$ and $T_A = 25°C$	Continuous	Continuous	
Operating Temperature Range			−40°C to +85°C
LM324/LM324A	0°C to +70°C		
LM224/LM224A	−25°C to +85°C		
LM124/LM124A	−55°C to +125°C		
Storage Temperature Range	−65°C to +150°C		−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C		300°C

Electrical Characteristics ($V^+ = +5.0\ V_{DC}$, Note 4)

PARAMETER	CONDITIONS	LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, (Note 5)		1	2		1	3		2	3		±2	±5		±2	±7		±2	±7	mV_{DC}
Input Bias Current (Note 6)	$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25°C$		20	50		40	80		45	100		45	150		45	250		45	250	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $T_A = 25°C$		2	10		2	15		5	30		±3	±30		±5	±50		±5	±50	nA_{DC}
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30\ V_{DC}$, $T_A = 25°C$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V_{DC}
Supply Current	$R_L = \infty$, $V_{CC} = 30V$, (LM2902 $V_{CC} = 26V$)		1.5	3		1.5	3		1.5	3		1.5	3		1.5	3		1.5	3	mA_{DC}
	$R_L = \infty$ On All Op Amps Over Full Temperature Range		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2	mA_{DC}
Large Signal Voltage Gain	$V^+ = 15\ V_{DC}$ (For Large V_O Swing) $R_L \geq 2\ k\Omega$, $T_A = 25°C$	50	100		50	100		25	100		50	100		25	100			100		V/mV
Output Voltage Swing	$R_L = 2\ k\Omega$, $T_A = 25°C$ (LM2902 $R_L \geq 10\ k\Omega$)	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V_{DC}
Common-Mode Rejection Ratio	DC, $T_A = 25°C$	70	85		70	85		65	85		70	85		65	70		50	70		dB
Power Supply Rejection Ratio	DC, $T_A = 25°C$	65	100		65	100		65	100		65	100		65	100		50	100		dB
Amplifier-to-Amplifier Coupling (Note 8)	f = 1 kHz to 20 kHz, $T_A = 25°C$ (Input Referred)		−120			−120			−120			−120			−120			−120		dB
Output Current Source	$V_{IN}^+ = 1\ V_{DC}$, $V_{IN}^- = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $T_A = 25°C$	20	40		20	40		20	40		20	40		20	40		20	40		mA_{DC}
Sink	$V_{IN}^- = 1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $T_A = 25°C$	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
	$V_{IN}^- = 1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $T_A = 25°C$, $V_O = 200\ mV_{DC}$	12	50		12	50		12	50		12	50		12	50					μA_{DC}
Short Circuit to Ground	$T_A = 25°C$, (Note 2)		40	60		40	60		40	60		40	60		40	60		40	60	mA_{DC}

Electrical Characteristics (Continued)

PARAMETER	CONDITIONS	LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	(Note 5)			4			4			5			±7			±9			±10	mV_{DC}
Input Offset Voltage Drift	$R_S = 0\Omega$		7	20		7	20		7	30		7			7			7		$\mu V/°C$
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			30			30			75			±100			±150		45	±200	nA_{DC}
Input Offset Current Drift			10	200		10	200		10	300		10			10			10		$pA_{DC}/°C$
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	100		40	200		40	300		40	500		40	500	nA_{DC}
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30\ V_{DC}$	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	V_{DC}
Large Signal Voltage Gain	$V^+ = +15\ V_{DC}$ (For Large V_O Swing) $R_L \geq 2\ k\Omega$	25			25			15			25			15			15			V/mV
Output Voltage Swing V_{OH}	$V^+ = +30\ V_{DC}$, $R_L = 2\ k\Omega$	26			26			26			26			26			22			V_{DC}
	$R_L \geq 10\ k\Omega$	27	28		27	28		27	28		27	28		27	28		23	24		V_{DC}
V_{OL}	$V^+ = 5\ V_{DC}$, $R_L \leq 10\ k\Omega$		5	20		5	20		5	20		5	20		5	20		5	100	mV_{DC}
Output Current Source	$V_{IN}^+ = +1\ V_{DC}$, $V_{IN}^- = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
Sink	$V_{IN}^- = +1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	15		5	8		5	8		5	8		5	8		5	8		mA_{DC}
Differential Input Voltage	(Note 7)			32			32			32			32			32			28	V_{DC}

Note 1: For operating at high temperatures, the LM324/LM324A, LM2902 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM224/LM224A and LM124/LM124A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15 V_{DC}, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3\ V_{DC}$ (at 25°C).

Note 4: These specifications apply for $V^+ = +5\ V_{DC}$ and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. With the LM224/LM224A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM324/LM324A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2902 specifications are limited to $-40°C \leq T_A \leq +85°C$.

Note 5: $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from 5 V_{DC} to 30 V_{DC}; and over the full input common-mode range (0 V_{DC} to $V^+ - 1.5\ V_{DC}$).

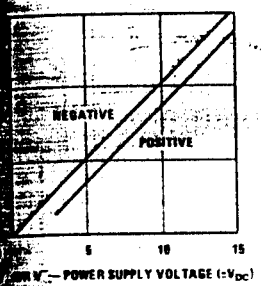
Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 7: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is $V^+ - 1.5V$, but either or both inputs can go to +32 V_{DC} without damage (+26 V_{DC} for LM2902).

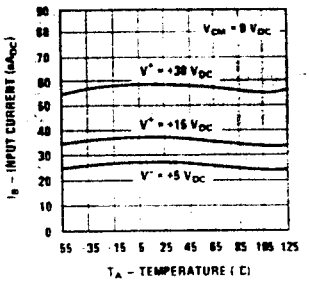
Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.

Performance Characteristics

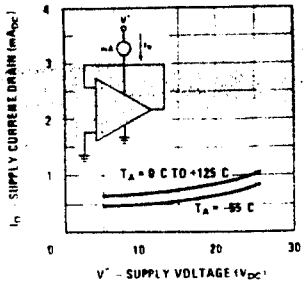
Input Voltage Range



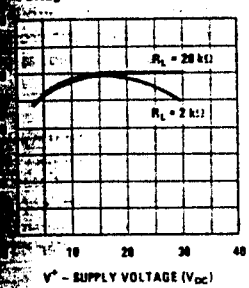
Input Current



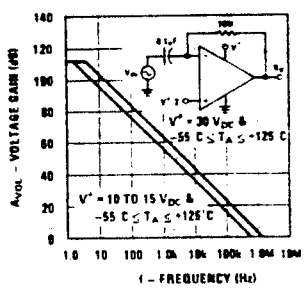
Supply Current



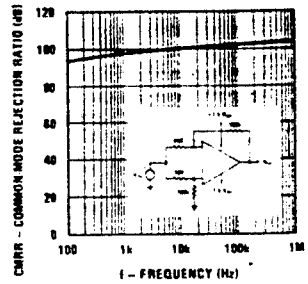
Voltage Gain



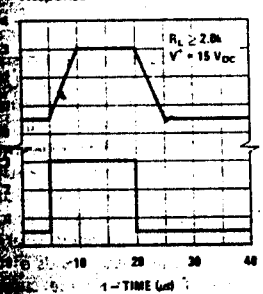
Open Loop Frequency Response



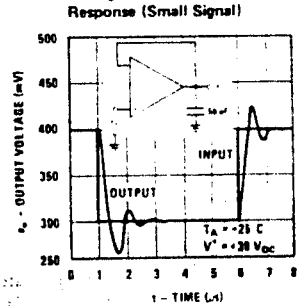
Common Mode Rejection Ratio



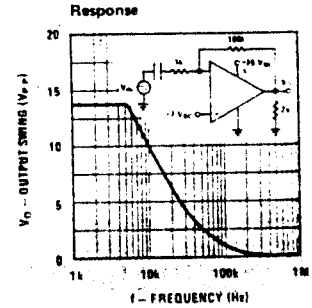
Voltage Follower Pulse Response



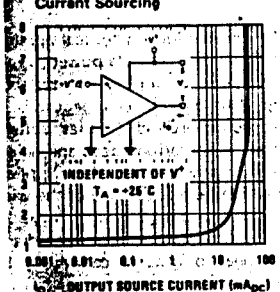
Voltage Follower Pulse Response (Small Signal)



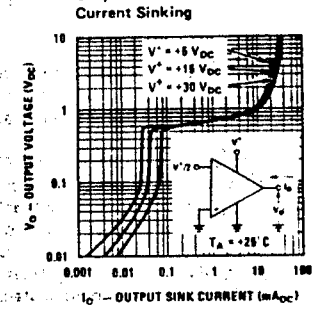
Large Signal Frequency Response



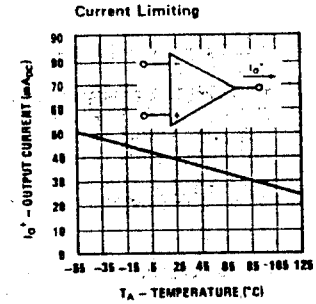
Output Characteristics Current Sourcing



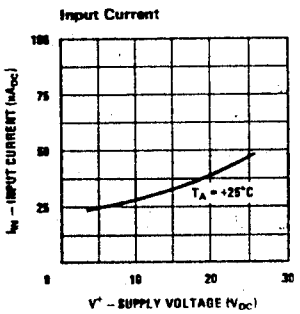
Output Characteristics Current Sinking

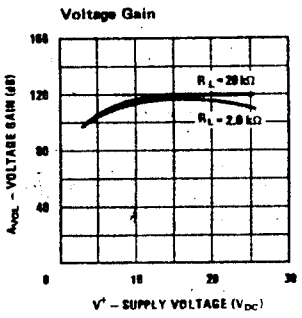


Current Limiting



Typical Performance Characteristics (LM2902 only)





Application Hints

The LM124 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

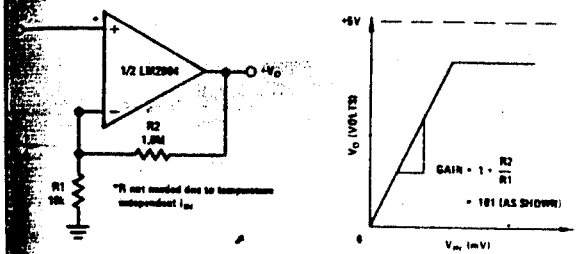
The bias network of the LM124 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

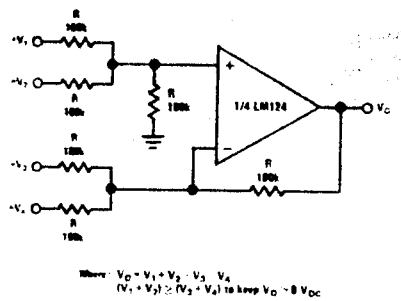
The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

cal Single-Supply Applications (V^+ = 5.0 V_{DC})

Non-Inverting DC Gain (0V Input = 0V Output)

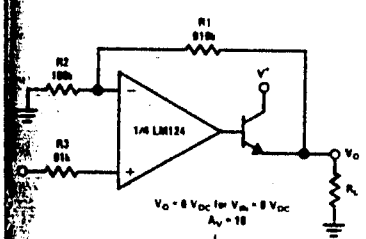


DC Summing Amplifier
(V_{IN}'S ≥ 0 V_{DC} AND V_O ≥ 0 V_{DC})

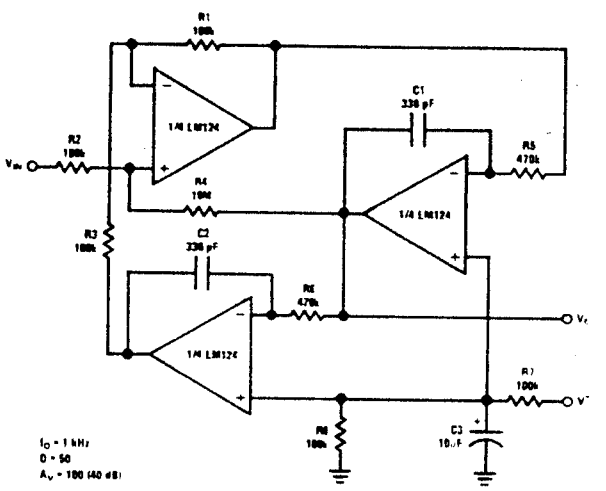


Where: $V_O = V_1 + V_2 - V_3 - V_4$
$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O \geq 0$ V_{DC}

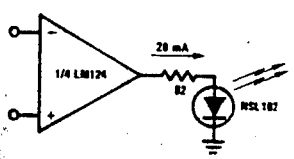
Power Amplifier



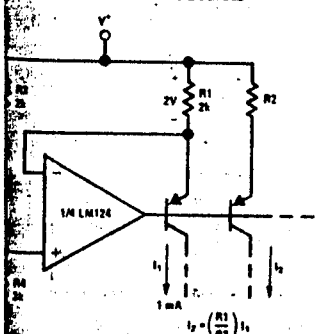
"BI-QUAD" RC Active Bandpass Filter



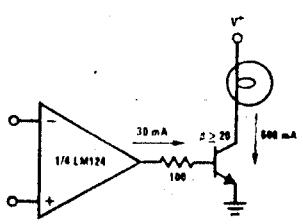
LED Driver



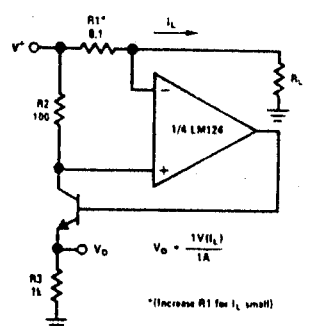
Fixed Current Sources



Lamp Driver

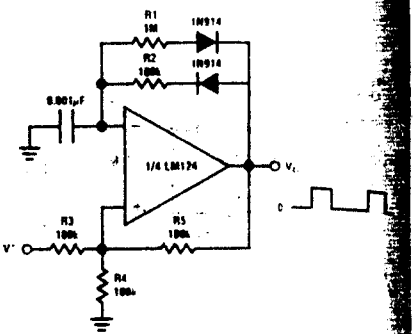


Current Monitor

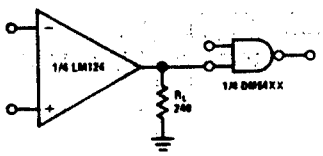


Typical Single-Supply Applications (Continued) ($V^+ = 5.0\ V_{DC}$)

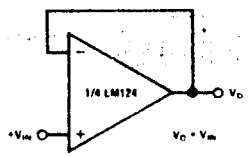
Pulse Generator



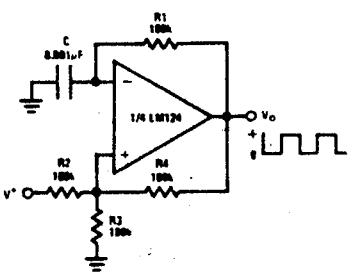
Driving TTL



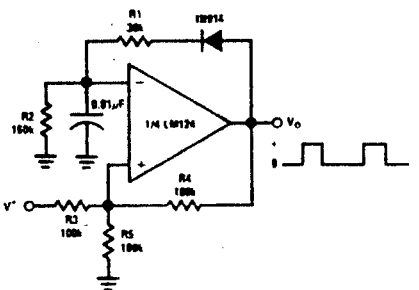
Voltage Follower



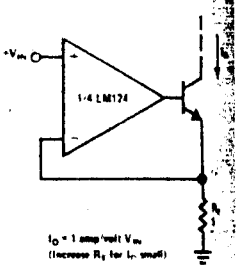
Squarewave Oscillator



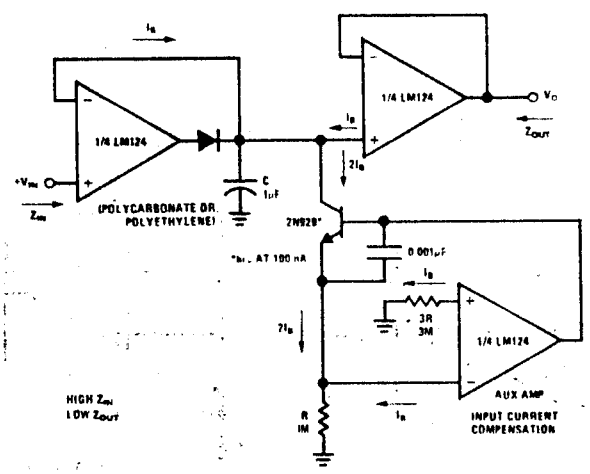
Pulse Generator



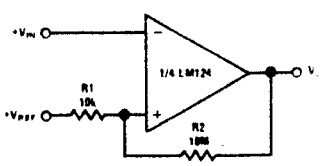
High Compliance Current Sink



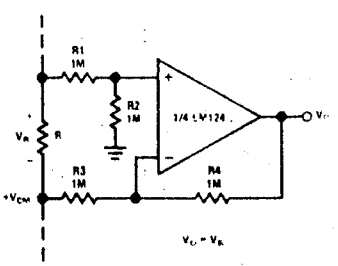
Low Drift Peak Detector



Comparator with Hysteresis



Ground Referencing A Differential Input Signal



...ical Single-Supply Applications (Continued) (V^+ = 5.0 V_{DC})

Voltage Controlled Oscillator Circuit

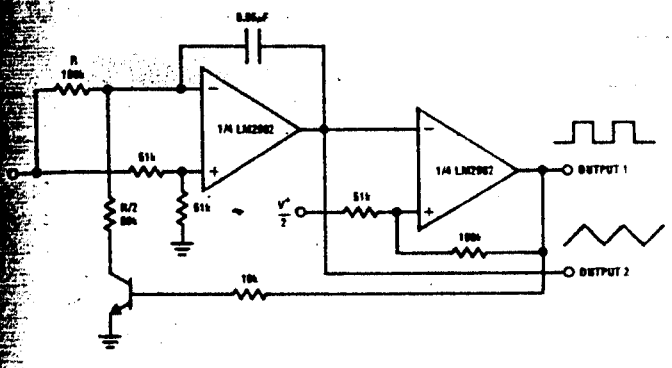
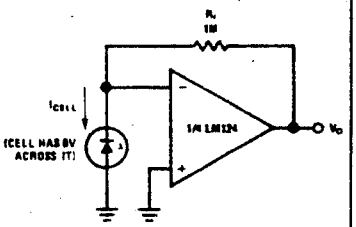
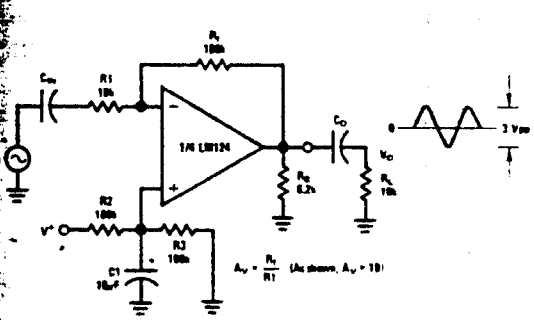


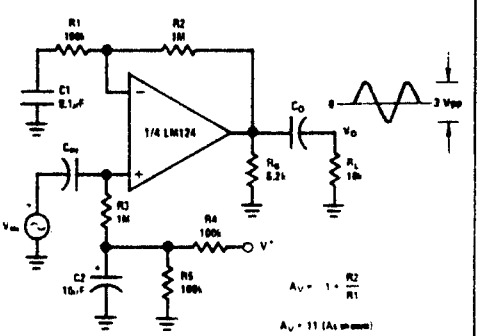
Photo Voltaic-Cell Amplifier



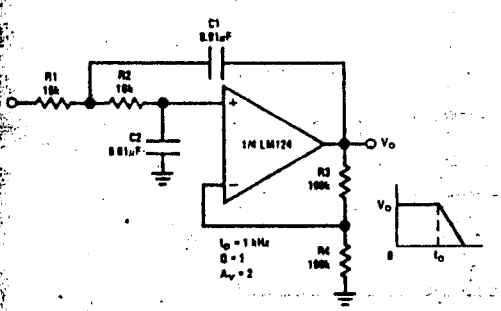
AC Coupled Inverting Amplifier



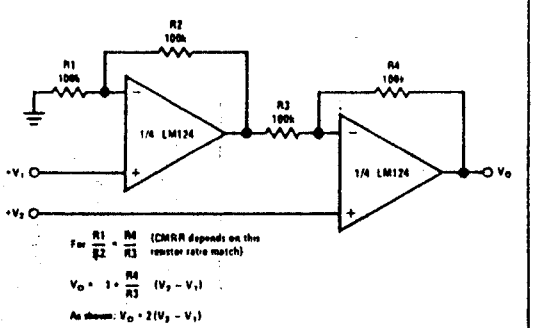
AC Coupled Non-Inverting Amplifier



DC Coupled Low-Pass RC Active Filter

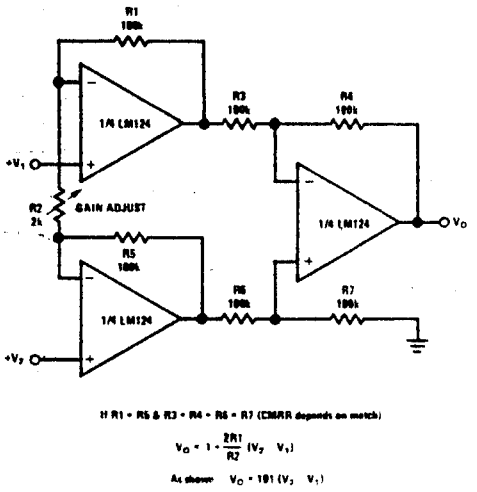


High Input Z, DC Differential Amplifier



Typical Single-Supply Applications (Continued) ($V^+ = 5.0\ V_{DC}$)

High Input Z Adjustable-Gain DC Instrumentation Amplifier

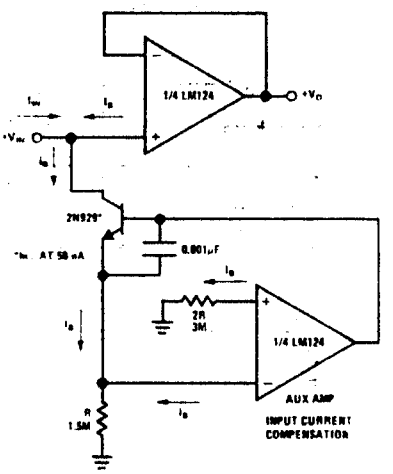


If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

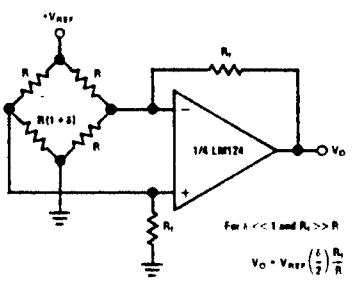
$$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$$

As shown $V_O = 101(V_2 - V_1)$

Using Symmetrical Amplifiers to Reduce Input Current (General Concept)



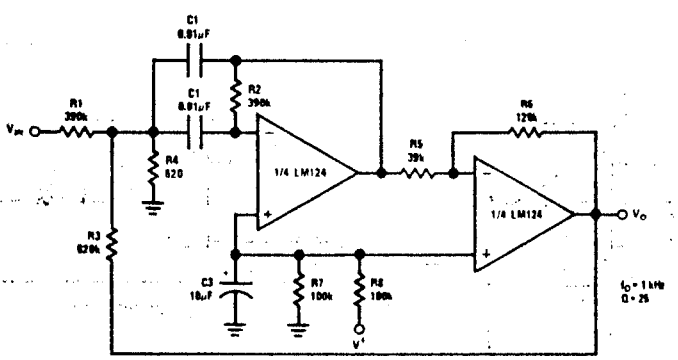
Bridge Current Amplifier



For $\delta << 1$ and $R_L >> R$

$$V_O = V_{REF}\left(\frac{\delta}{2}\right)\frac{R_L}{R}$$

Bandpass Active Filter



TYPES SN5473, SN54H73, SN54L73, SN54LS73A, SN7473, SN74H73, SN74LS73A
DUAL J-K FLIP-FLOPS WITH CLEAR

REVISED DECEMBER 1983

...ge Options Include Plastic and ...mic DIPs

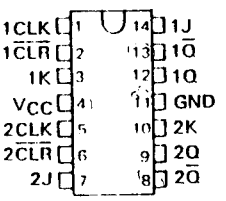
...ndable Texas Instruments Quality ...Reliability

...73, ...H73, and 'L73 contain two independent ...flops with individual J-K, clock, and direct clear ... The '73, 'H73, and 'L73 are positive pulse ...ed flip-flops. J-K input is loaded into the master ...the clock is high and transferred to the slave on ...-to-low transition. For these devices the J and K ...must be stable while the clock is high.

...LS73A contain two independent negative-edge ...ed flip-flops. The J and K inputs must be stable ...up time prior to the high-to-low clock transition ...dictable operation. When the clear is low, it ...s the clock and data inputs forcing the Q output ...the $\overline{Q}$ output high.

...SN5473, SN54H73, SN54L73, and the ...LS73A are characterized for operation over the ...ary temperature range of −55°C to 125°C. ...SN7473, SN74H73, and the SN74LS73A are ...rized for operation from 0°C to 70°C.

SN5473, SN54H73, SN54LS73A . . . J OR W PACKAGE
SN54L73 . . . J PACKAGE
SN7473, SN74H73 . . . J OR N PACKAGE
SN74LS73A . . . D, J OR N PACKAGE
(TOP VIEW)



'73, 'H73, 'L73
FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	

'LS73A
FUNCTION TABLE

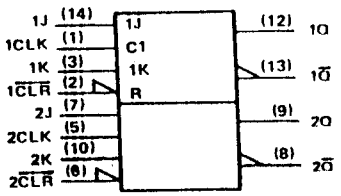
INPUTS				OUTPUTS	
$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0'	Q_0

FOR CHIP CARRIER INFORMATION, CONTACT THE FACTORY

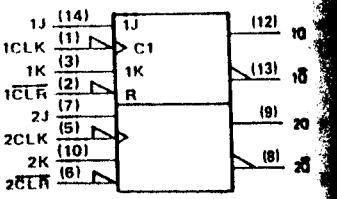
TTL DEVICES

logic symbols

'73, 'H73, 'L73



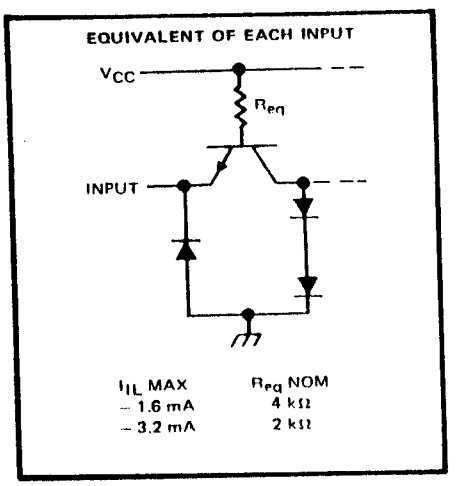
'LS73A

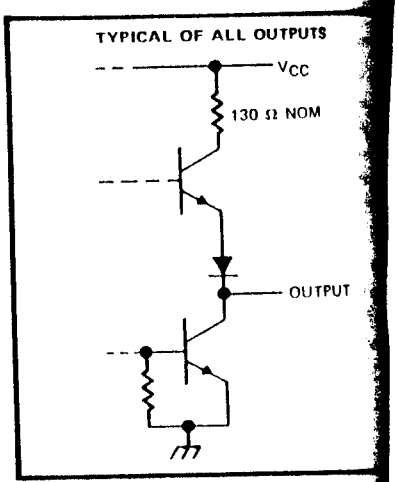


Pin numbers shown on logic notation are for D, J or N packages.

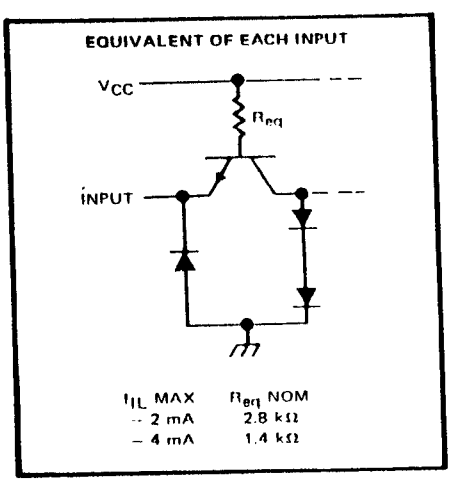
schematics of inputs and outputs

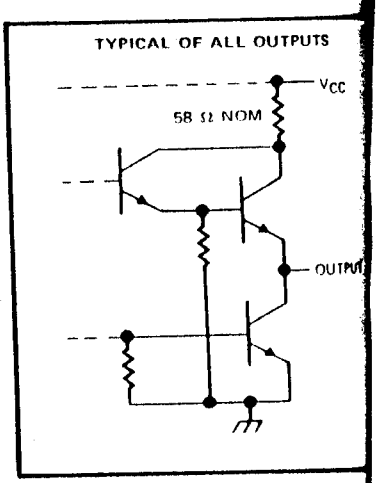
'73





'H73





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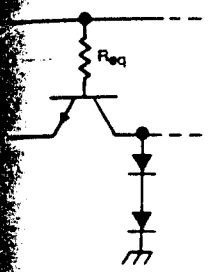
...s and outputs (continued)

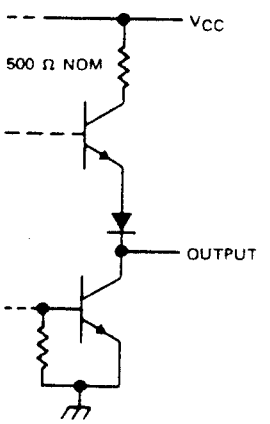
'L73

...QUIVALENT OF
...EACH INPUT



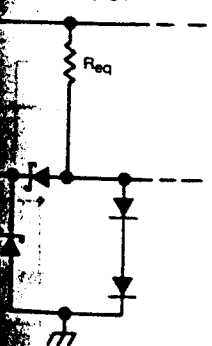
...MAX	R_{eq} NOM
...18 mA	40 kΩ
...36 mA	20 kΩ

TYPICAL OF
ALL OUTPUTS



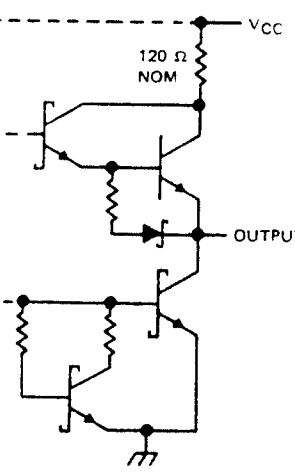
'LS73A

EQUIVALENT OF
EACH INPUT



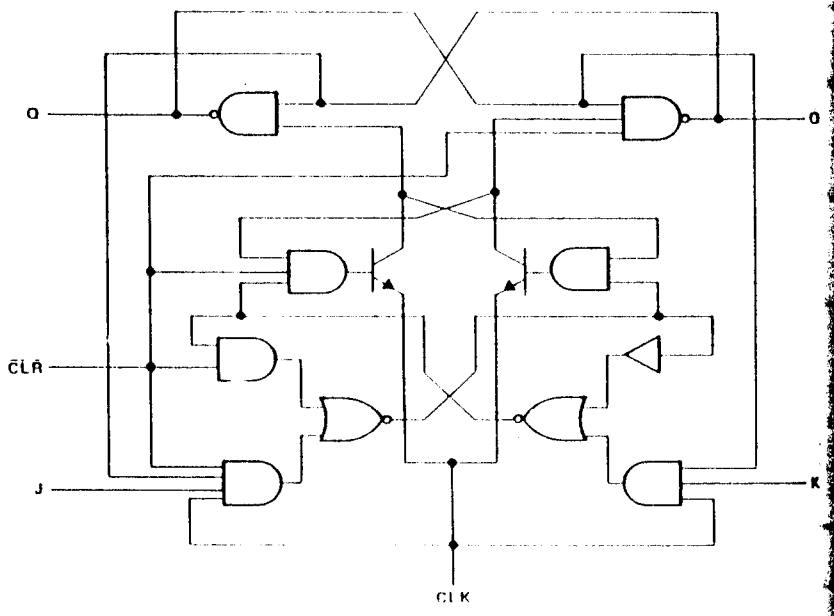
	R_{eq} NOM
...X	30 kΩ
...A	8.25 kΩ

TYPICAL OF
ALL OUTPUTS

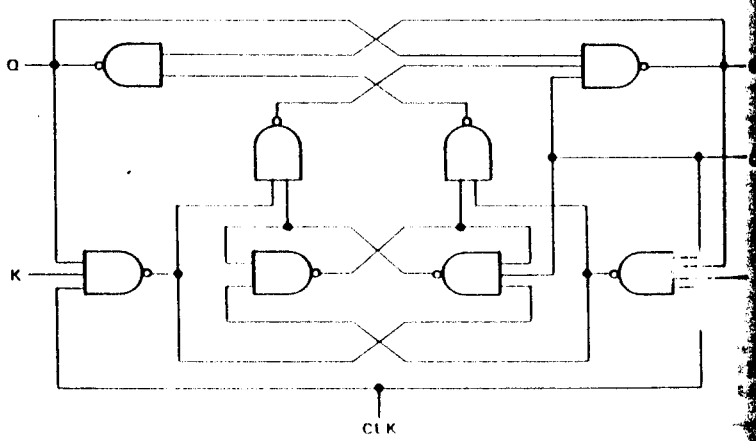


logic diagrams

'73



'H73



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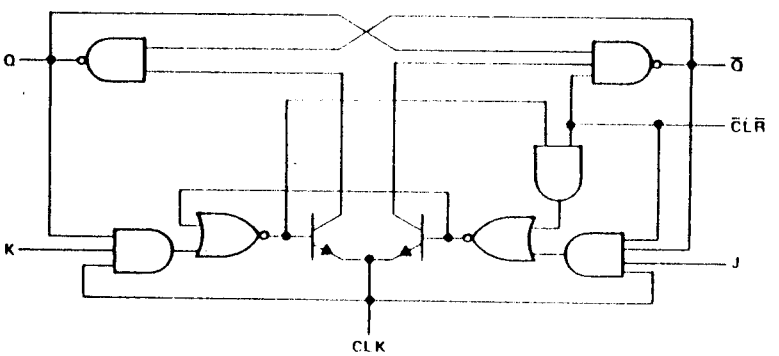
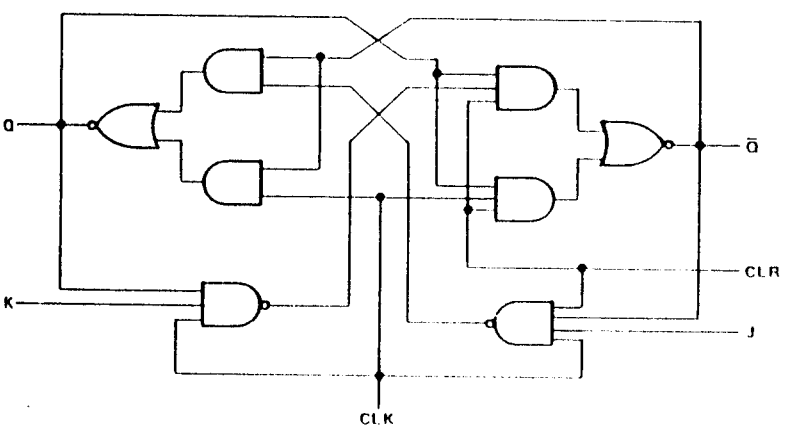
ms (continued)

'L73



'LS73A



imum ratings over operating free-air temperature range (unless otherwise noted)

oltage, V_{CC} (see Note 1) . . . . . 7 V
ltage: '73, 'H73, 'L73 . . . . . 5.5 V
'LS73A . . . . . 7 V
ree-air temperature range: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0°C to 70°C
mperature range . . . . . −65°C to 150°C

alues are with respect to network ground terminal

recommended operating conditions

			SN5473			SN7473	
			MIN	NOM	MAX	MIN	NOM
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5
V_{IH}	High-level input voltage		2			2	
V_{IL}	Low-level input voltage				0.8		
I_{OH}	High-level output current				−0.4		
I_{OL}	Low-level output current				16		
t_w	Pulse duration	CLK high	20			20	
		CLK low	47			47	
		$\overline{CLR}$ low	25			25	
t_{su}	Input setup time before CLK↑		0			0	
t_h	Input hold time data after CLK↓		0			0	
T_A	Operating free-air temperature		−55		125	0	

electrical characteristics over recommended operating free-air temperature range (unless other

PARAMETER		TEST CONDITIONS†			SN5473			SN7473	
					MIN	TYP‡	MAX	MIN	TYP‡
V_{IK}		V_{CC} = MIN,	I_I = −12 mA				−1.5		
V_{OH}		V_{CC} = MIN, I_{OH} = −0.4 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,	2.4	3.4		2.4	3.4
V_{OL}		V_{CC} = MIN, I_{OL} = 16 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,		0.2	0.4		0.2
I_I		V_{CC} = MAX,	V_I = 5.5 V				1		
I_{IH}	J or K	V_{CC} = MAX,	V_I = 2.4 V				40		
	$\overline{CLR}$ or CLK						80		
I_{IL}	J or K	V_{CC} = MAX,	V_I = 0.4 V				−1.6		
	$\overline{CLR}$						−3.2		
	CLK						−3.2		
I_{OS}§		V_{CC} = MAX			−20		−57	−18	
I_{CC}		V_{CC} = MAX,	See Note 2			10	20		10

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP
f_{max}			R_L = 400 Ω, C_L = 15 pF		
t_{PLH}	$\overline{CLR}$	$\overline{Q}$		15	20
t_{PHL}		Q			18
t_{PLH}	CLK	Q or $\overline{Q}$			20
t_{PHL}					18
					20

¶ f_{max} = maximum clock frequency; t_{PLH} = propagation delay time, low-to-high level output; t_{PHL} = propagation delay ti
level output.
NOTE 3: See General Information Section for load circuits and voltage waveforms.

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operating conditions

		SN54H73			SN74H73			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
voltage		4.5	5	5.5	4.75	5	5.25	V
input voltage		2			2			V
input voltage				0.8			0.8	V
output current				−0.5			−0.5	mA
output current				20			20	mA
ration	$\overline{CLK}$ high	12			12			ns
	CLK low	28			28			
	$\overline{CLR}$ low	16			16			
up time before CLK↑	High-level data	0			0			ns
	Low-level data	0			0			
d time, data after CLK↓		0			0			ns
free-air temperature		−55		125	0		70	°C

racteristics over recommended operating free-air temperature range (unless otherwise noted)

TER	TEST CONDITIONS†			SN54H73			SN74H73			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
	V_{CC} = MIN,	I_I = −8 mA				−1.5			−1.5	V
	V_{CC} = MIN, I_{OH} = −0.5 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V	2.4	3.4		2.4	3.4		V
	V_{CC} = MIN, I_{OL} = 20 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,		0.2	0.4		0.2	0.4	V
	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
or CLK	V_{CC} = MAX,	V_I = 2.4 V				50			50	μA
						100			100	
or CLK	V_{CC} = MAX,	V_I = 0.4 V				−2			−2	mA
						−4			−4	
	V_{CC} = MAX			−40		−100	−40		−100	mA
	V_{CC} = MAX,	See Note 2			16	25		16	25	mA

shown as MIN or MAX, use the appropriate value specified in recommended operating conditions.
are at V_{CC} = 5 V, T_A = 25°C.
one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is

racteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
		R_L = 280 Ω, C_L = 25 pF	25	30		MHz
$\overline{CLR}$	$\overline{Q}$			6	13	ns
	Q			12	24	ns
CLK	Q or $\overline{Q}$			14	21	ns
				22	27	ns

al Information Section for load circuits and voltage waveforms

TTL DEVICES

...d operating conditions

		SN54LS73A			SN74LS73A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
...y voltage		4.5	5	5.5	4.75	5	5.25	V
...level input voltage		2			2			V
...level input voltage				0.7			0.8	V
...level output current				−0.4			−0.4	mA
...frequency				4			8	mA
...duration	CLK high	0		30	0		30	MHz
	$\overline{CLR}$ low	20			20			ns
...time before CLK↓	data high or low	25			20			
	$\overline{CLR}$ inactive	20			20			ns
...time data after CLK↓		20			20			
...ing free-air temperature		0			0			ns
		−55		125	0		70	°C

...acteristics over recommended operating free-air temperature range (unless otherwise noted)

...TER	TEST CONDITIONS†			SN54LS73A			SN74LS73A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
	V_{CC} = MIN, I_{OH} = −0.4 mA	V_{IH} = 2 V,	V_{IL} = MAX,	2.5	3.4		2.7	3.4		V
	V_{CC} = MIN, I_{OL} = 4 mA	V_{IL} = MAX,	V_{IH} = 2 V,		0.25	0.4		0.25	0.4	V
	V_{CC} = MIN, I_{OL} = 8 mA	V_{IL} = MAX,	V_{IH} = 2 V,					0.35	0.5	
...K	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
...						0.3			0.3	
...K	V_{CC} = MAX,	V_I = 2.7 V				0.4			0.4	
...						20			20	µA
...K						60			60	
...r CLK	V_{CC} = MAX,	V_I = 0.4 V				80			80	
...	V_{CC} = MAX,	See Note 4				−0.4			−0.4	mA
...	V_{CC} = MAX,	See Note 2				−0.8			−0.8	
				−20		−100	−20		−100	mA
					4	6		4	6	mA

...own as MIN or MAX, use the appropriate value specified under recommended operating conditions.
...are at V_{CC} = 5 V, T_A = 25°C.
...one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
...outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is ...

...e devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed ...e 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced ...t of their stated values.

...cteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
...							
...	$\overline{CLR}$ or CLK	Q or $\overline{Q}$	R_L = 2 kΩ, C_L = 15 pF	30	45		MHz
...					15	20	ns
...					15	20	ns

...l Information Section for load circuits and voltage waveforms