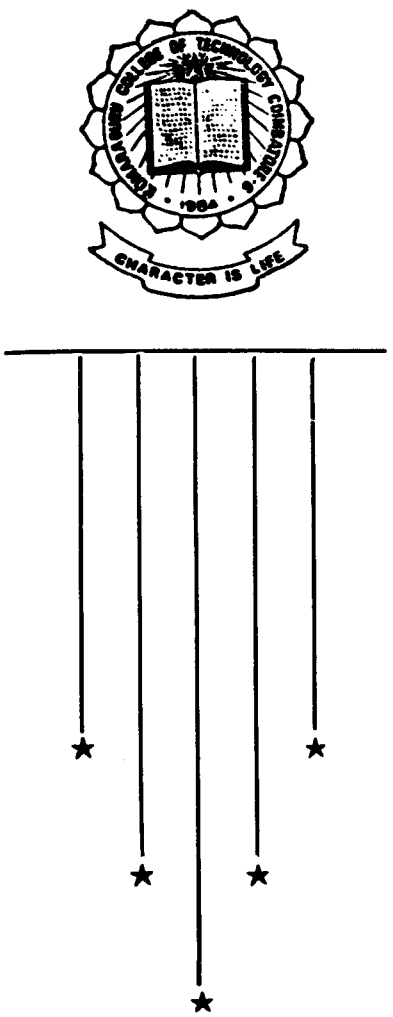
ART Automatic RPM Meter Tester

P-1320

PROJECT REPORT 1996 - 97



Submitted By

R. ASOKAN

C. R. BALAKRISHNAN

BIJAY SELVARAJ

R. MADHUMOHAN

MATHEW PHILIPOSE

Under the guidance of

Mr. MUTHURAMAN RAMASWAMY

M.E., M.I.S T.E., M.I.E., C.Engg(I), M.IEEE (USA)

IN PARTIAL FULFILMENT OF THE REQUIREMENTS

FOR THE AWARD OF THE DEGREE OF

BACHELOR OF ENGINEERING IN

ELECTRONICS AND COMMUNICATION ENGINEERING

OF THE BHARATHIAR UNIVERSITY, COIMBATORE

Department of Electronics and Communication Engineering

Kumaraguru College of Technology

Coimbatore - 641 006.

Kumaraguru College of Technology

Coimbatore - 641 006.

Department of Electronics and Communication Engineering

Certificate

This is to Certify that this Project Entitled

ART
AUTOMATIC RPM METER TESTER

Has been submitted by

Mr. R. ASOKAN, C.R BALAKRISHNAN, BIJAY SELVARAJ
R. MADHUMOHAN, MATHEW PHILIPOSE.

in partial fulfilment of the requirements for the award of Degree of Bachelor of Engineering in the Electronics and Communication Engineering Branch of the Bharathiar University, Coimbatore-641046 during the academic year 1996-'97.

(Guide)

(Head of Department)

Certified that the Candidate was Examined by us in the Project Work.

Viva-Voce Examination held on 10-04-97

University Register Number _____

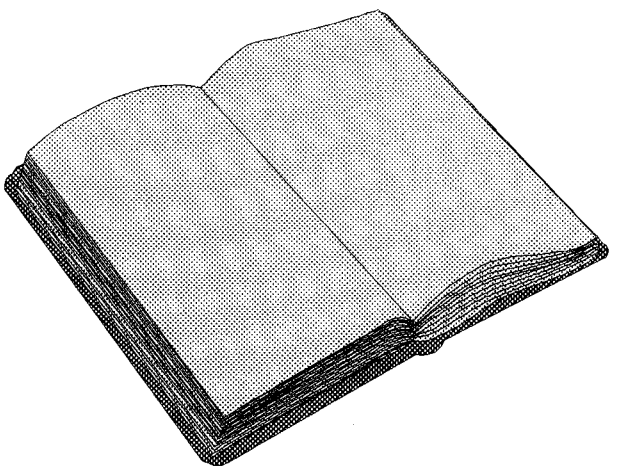
(Internal Examiner)

(External Examiner)

Dedicated

to our

Beloved parents



Contents

CONTENTS

Acknowledgement

ACKNOWLEDGEMENT

We wish to express our regards and sincere thanks to the management of Kumaraguru College of Technology and to **Dr. S.Subramanian**, M.Sc.(ENGG); Ph.D,S.M.IEEE, M.I.S.T.E principal, Kumaraguru College of Technology, for providing necessary facilities to carry out this project work.

We feel highly elated in manifesting our deep sense of thankfulness to our project guides **Mr.Muthuraman Ramaswamy**, M.E;M.I.S.T.E,M.I.E, C.Engg (I), M.IEEE, Head of the Department, and **Mr. E. Mathivanan** for their keen interest, valuable guidance, useful suggestions and constant help during the course of this project work. We can say with utmost confidence that they were the backbone of this project. We also thank **Mr. Hariharan** of Electrical and Electronics Department for providing us with his valuable suggestions during the course of this project work.

We take great pleasure in expressing our sinciere thanks to **Shri Vijay Mohan,** Managing Director and to the Management of M/s Premier

Instruments and Controls Ltd., and to **Mr. Balasubramaniam**, Manager, Electronics Quality Assurance Department for permitting us to undertake this project. We also thank **Mr. Ramakrishnan** for providing us with valuable facilities and taking great pains to help us while we were in the company.

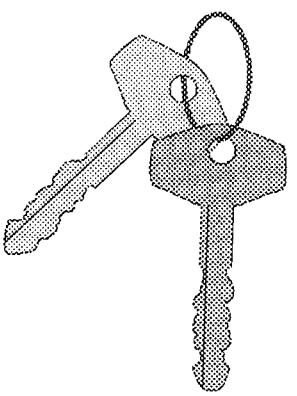
We acknowledge, with thanks the very useful suggestion and guidance given by **Mr. Sivakumar**, Research and Development, Electronic Division PRICOL. His contribution to the work together with valuable help given by other staffs are highly appreciated and acknowledged.

We also are thanks to our teaching and non teaching staffs of Electronics and communication Engineering department, Kumaraguru College of Technology. We also thank our friends in the Mechanical department, Kumaraguru College of Technology for providing us with valuable tips on the project.

We also express our sincere gratitude to our parents without whose co-operation we wouldn't have completed this project. They provided us with

the much needed inspiration and al other help throught the course of the project work.

Last but not least we express our sincere gratitude to our classmates, for all of them have been a source of encouragement, and most of them have come out with useful ideas and suggestions about our project. We also thank all other people who are not mentioned here for their bits and pieces of advice.



Synopsis

SYNOPSIS

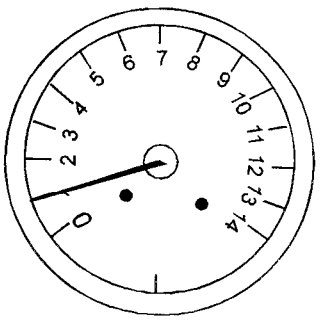
Of late a RPM meter has become an integral accessory of most of the automobiles. The RPM meters essentially serves as an indicator as to whether the Engine functioning is alright.

Ideally the power generated by the engine should be transferred completely to the wheels. The RPM meter indicates the number of rotations made by the flywheel which forms part of the engine.

Hence it is essential that the RPM meter be accurate as well as trustworthy. So a testing method should be deviced which is really effective. The purpose of this project work is to design and fabricate a testing circuit for testing RPM meters.

This testing circuit is designed for RPM meters and is a Microprocessor based testing method. This project involves the design and development of a prototype and development of assembly language programs

to be used in the prototype. This testing circuitry has a number of advantages over the testing method presently in use. The performance of this testing circuit is quite robust, rugged and is insensitive to operating condition changes.



Introduction to ART

INTRODUCTION TO ART

Our project work ART comprises of the design and fabrication of a testing circuit. The present testing method i.e Manual testing is not very accurate and is also time consuming. Since our testing circuit is a microprocessor based testing circuit we can expect speed and the same level of accuracy for all the Meters. Our project work has been sponsored by PRICOL - PREMIER INSTRUMENTS AND CONTROLS PRIVATE LIMITED. It is one of the leading Industry in Coimbatore. Our main objective is the Automization of the testing procedure. This testing precedure does not aim to replace the human beings by machines. This project is built with the firm belief that machines cn at best support a human being and not replace him. Ofcourse we have strived to reduce the errors due to human factor our project has ben broadly classiffied.

Chapter 1 gives the introduction to ART.

Chapter 2 gives an Idea of the testing method that is presently employed. IT gives us an idea about the disadvantages of the present testing method.

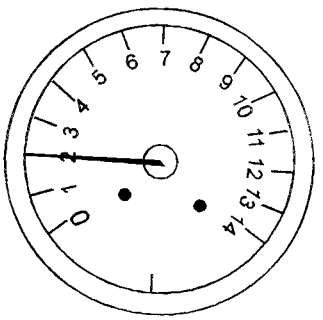
Chapter 3 gives us the circuit diagram and block diagram of ART.

In chapter 4 the description of the individual blocks that are employed are given, with block diagram as well as circuit diagram's.

The next three chapters gives the results of ART, various graphs associated with it, the advantages as well as the limitations. It also gives idea about the software and the assembly level language program associated with it and also the flow charts and algorithms.

The next chapter gives the details of the Printed Circuit Board design and the various on board connections.

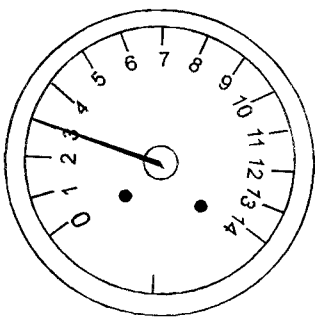
The last chapter gives the conclusion of the ART.



Present Testing Method

PRESENT TESTING METHOD

The testing method that is currently employed in PRICOL is manual testing. In the manual testing procedure the meter is fed with a positive going pulse of amplitude of 25V and frequencies varying between 0-466 Hz. The meter is calibrated so that it advances one step at a time for a frequency change of 33 Hz. The Main disadvantage of this procedure is that it is completely left upto the testing staff to decide upon the accuracy of the meter. Moreover all the meters cannot have the same accuracy. Hence accuracy cannot be guaranteed in the manual testing procedure.



ART Circuit Diagram & Block Diagram

ART CIRCUIT DIAGRAM AND BLOCK DIAGRAM

BLOCK DIAGRAM DESCRIPTION

Block diagram of the automatic RPM meter tester is shown above. As seem in the block the Microprocessor - 8085 simulates an engine and applies positive going pulse to the meter. Since the output of the microprocessor is digital and the meter an anolog device, a digital to analog converter is employeed at the output of the microprocessor. The Digital to analog converter used is DAC 0808. The analog signal applied to the meter drives the coils. The F/V output pin is tapped and the output is converted back to digital form using an Analog to digital converter namely ADC 0808. The microprocessor compares the theoretical and the practical value that have been obtained for each frequency. Depending upon the tolerance level it either checks the next frequency and so on and indicates that the meter is working, or it rejects the meter and indicates at which frequency it is not working.

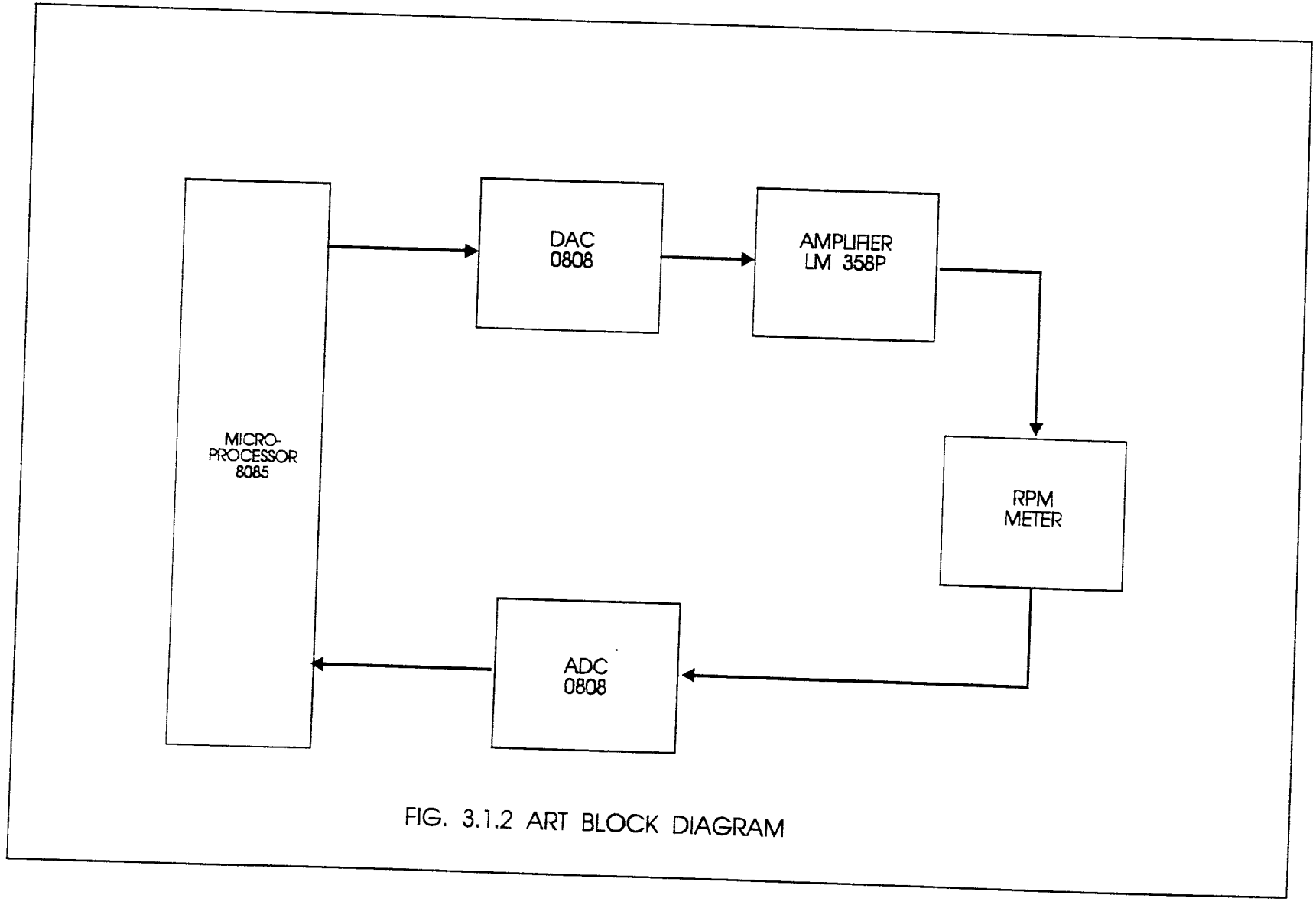


FIG. 3.1.2 ART BLOCK DIAGRAM

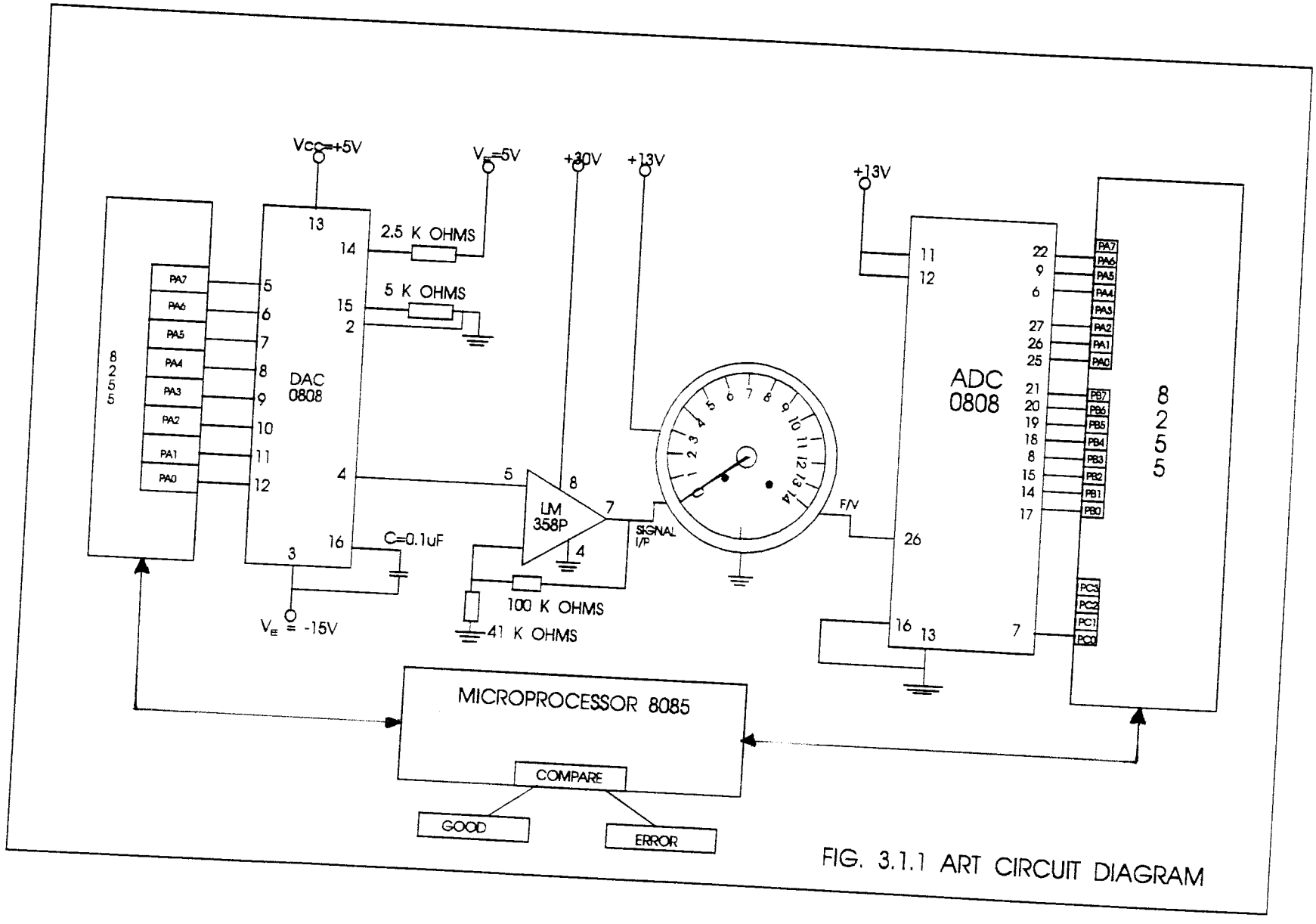
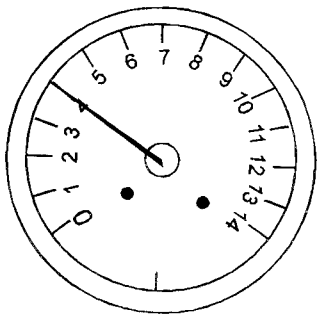


FIG. 3.1.1 ART CIRCUIT DIAGRAM



Hardware Components Block Diagram

HARDWARE COMPONENTS BLOCKDIAGARM

MICROPROCESSOR 8085

The 8085 microprocessor includes on its chip most of the logical circuitry for performing computing tasks and for communicating with peripherals we define the microprocessor as a device or group of devices that can communicate with the peripherals, provide timing signals, direct data flow and perform computing task as specified by the instruction in memory.

The 8085 is an 8-bit general purpose microprocessor. It is capable of addressing 64 Kbytes of memory. The device has 40 pins. It requires a + 5V single supply.

All the signals of the microprocessor can be classified into 6 groups, they are

* Address bus,
* Data bus
* Control and Status signal
* Power supply and Frequency signal
* Externally Initiated signal
* Serial I/O ports

The 8085 Microprocessor has eight signal lines A15-A8 which are all unidirectional and they are used as the higher order address bus. The signal lines AD7-AD0 are bidirectional. They serve dual purpose. They are used as the lower order address bus as well as data bus. In executing an instruction, during the earlier part of the cycle these lines are used as the lower order address bus, during the later part of the cycle these lines are used as the data bus. This is known as multiplexing.

There are two control signals namely RD and WR. The RD control signal is an active low signal. This signal indicates that the selected I/O or memory device is to be read and data are available on the databus. The WR control signal is an active low signal This indicates that the data in the data bus are to be written into selected memory or I/O location.

The IO/M is a status signal used to differentiate between I/O and memory operations. When the signal is high, it indicates an I/O operation or else it indicates a memory operation. The other status signals like S1 S0 are simillar to IO/M and can identify various operations. The ALE signal is a special signal It is a positive going pulse generated ever time the 8085

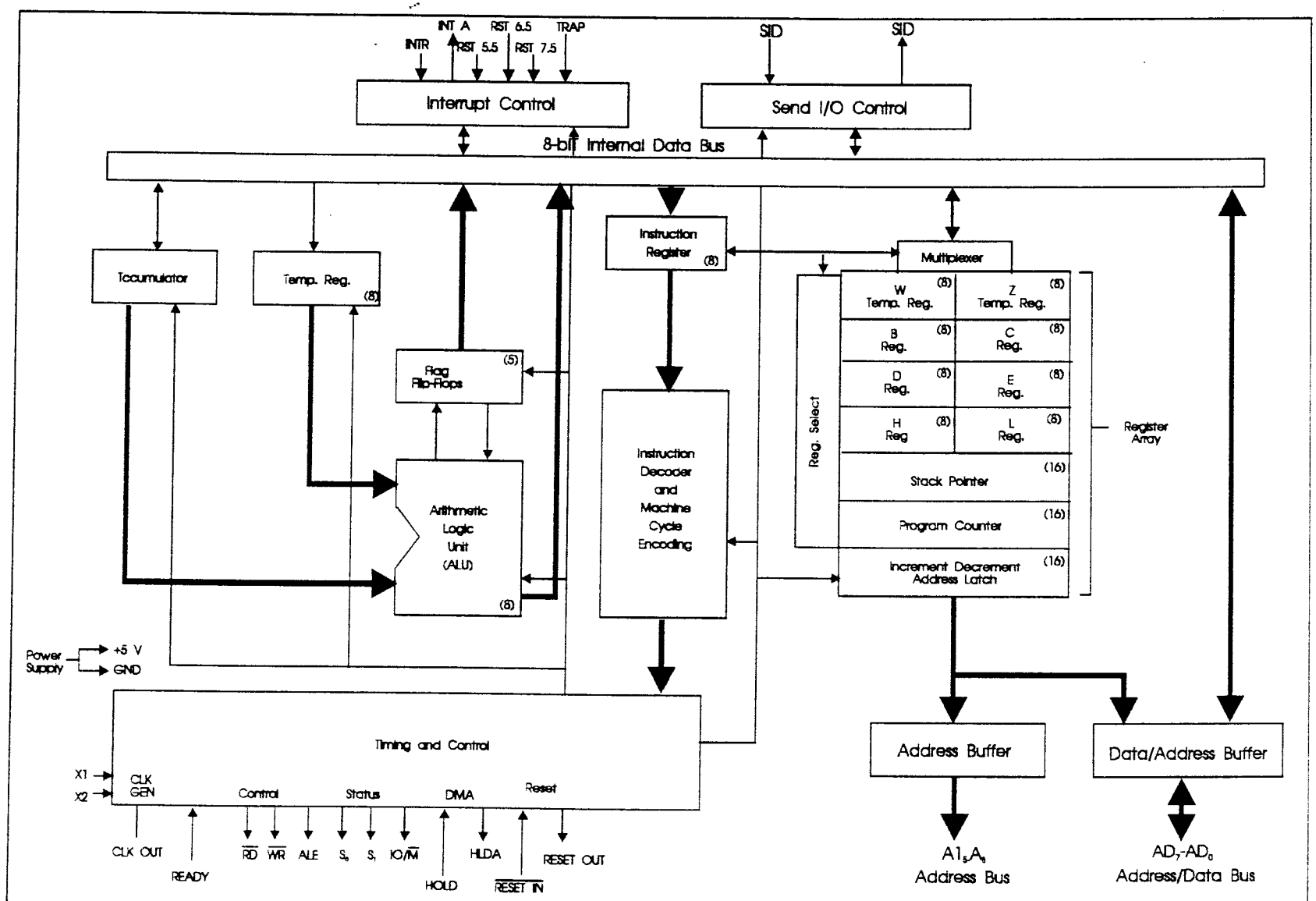


Figure 4.1.1 THE 8085A MICROPROCESSOR FUNCTIONAL BLOCK DIAGRAM

microprocessor begins an operation. It indicates that the bit on AD7 - AD0 are address bits. This signal is used primarily to latch the lower order address from the multiplexed bus and generate a separate set of eight address lines A7-A0.

FUNCTIONAL BLOCK DIAGRAM

The Internal architecture of the microprocessor 8085 includes the ALU (Arithematic /Logic unit), Timing and control unit. Instruction Register and decoder, Register array, Interrupt control and serial I/O control.

The ALU performs the computing functions. It includes the accumulator, the temporary register, the arthmetic and logic circuits, and five flags. The temporary register is used to hold data during an arthmetic/logic operation. The result is stored in the accumulator, and flags are set or reset according to the result of the operation.

The flag are affected by the arithmetic and logic operations in the ALU. In most of these operations in the ALU. In most of these operations the result

is stored in accumulator. The various flags are sign flag, zero flag, Auxillary carry flag, parity flag, carry flag.

The timing unit synchronises all the microprocessor operation with the clock and generates the control signals necessary for communications between the microprocessor and the peripherals.

When an instruction is fetched from memory it is located in the Instruction register. The decoder decodes the instruction and establishes the sequence of events to follow. The instruction register is not programmable and cannot be accessed through any instruction.

8255A PROGRAMMABLE PERIPHERAL INTERFACE

The 8255A is a widely used programmable, parrallel I/O device. It can be programmed to transfer data under various conditions, from simple I/O to interupt I/O. It is an important general purpose I/O device that can be used with almost any microprocessor.

The 8255A is a 40pin IC chip and has 24 I/O pins that can be grouped primarily into two 8 bit parallel port's, port A and portB,with the remaining 8 bits as port c. The 8 bits ofportC can either be used as individual bits or grouped intotwo 4 bits: (upper(Ch) and (lower(Cl). The function of these port's are defined by writing a control word in the control register.

The control word of the 8255A has 8 bits. The Bit D7 is either a Bitset/Reset mode or I/O mode according to the contents of D7. If the contents of D7 is O then 8255 is in Bit Set/Reset mode. If the contents of D7 is `1' then 8255 is in I/O mode.

The BSR mode is used to set or reset the bits in port C/D. The I/O mode is further divided into three modes: Mode 0, Mode 1, Mode 2. In mode 0, all

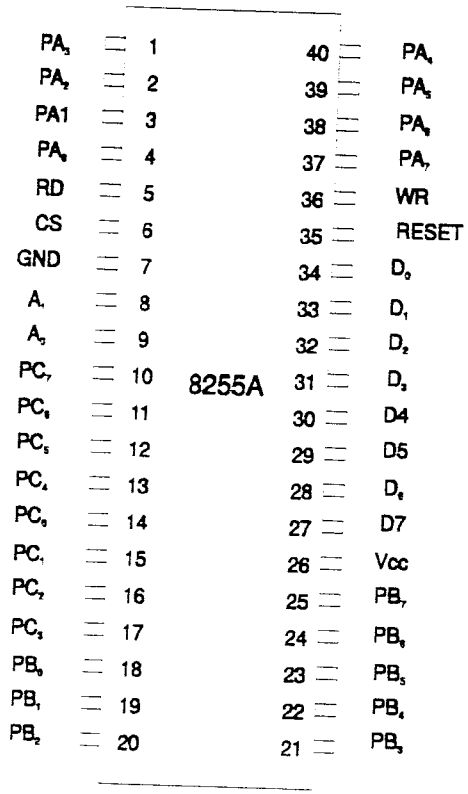


Figure 4.2.1
8255 A PIN CONFIGURATION

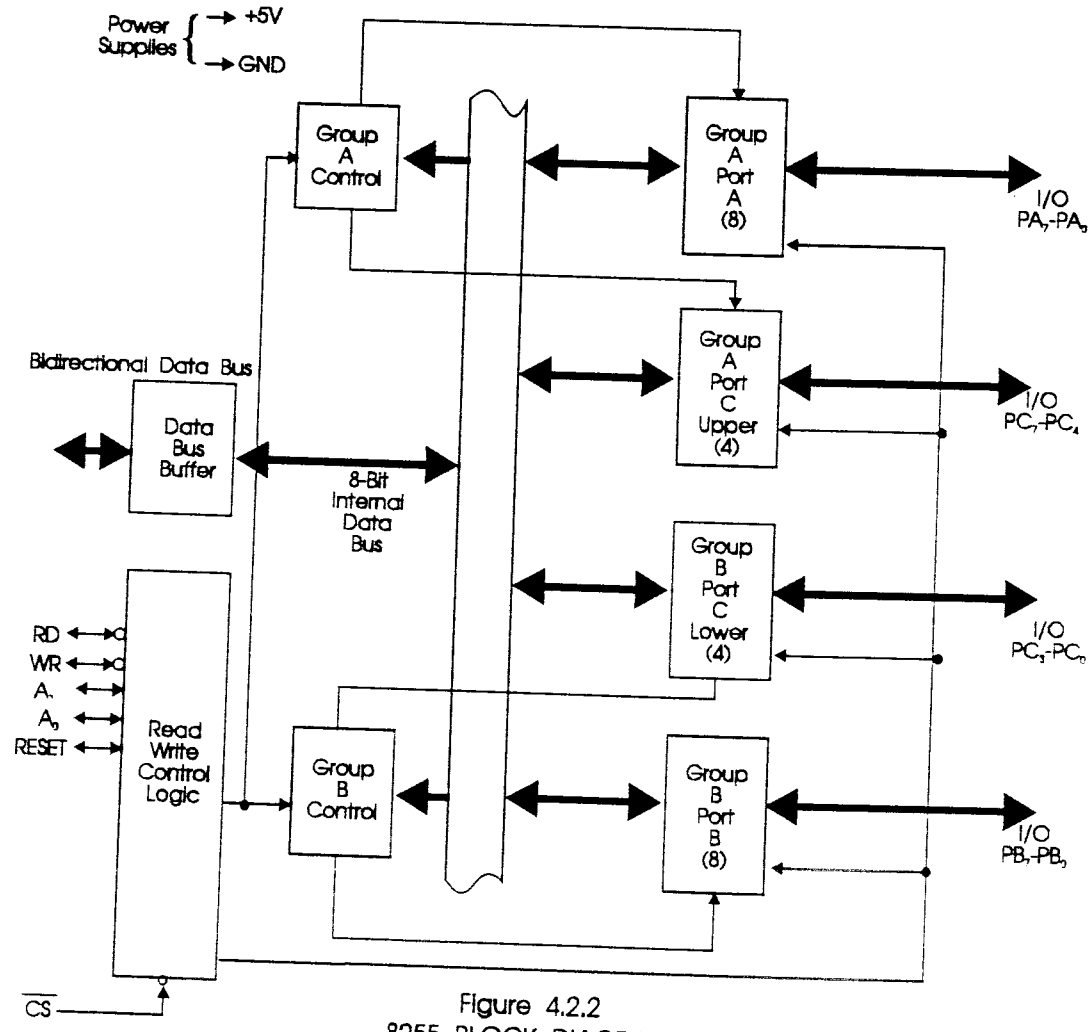


Figure 4.2.2
8255 BLOCK DIAGRAM

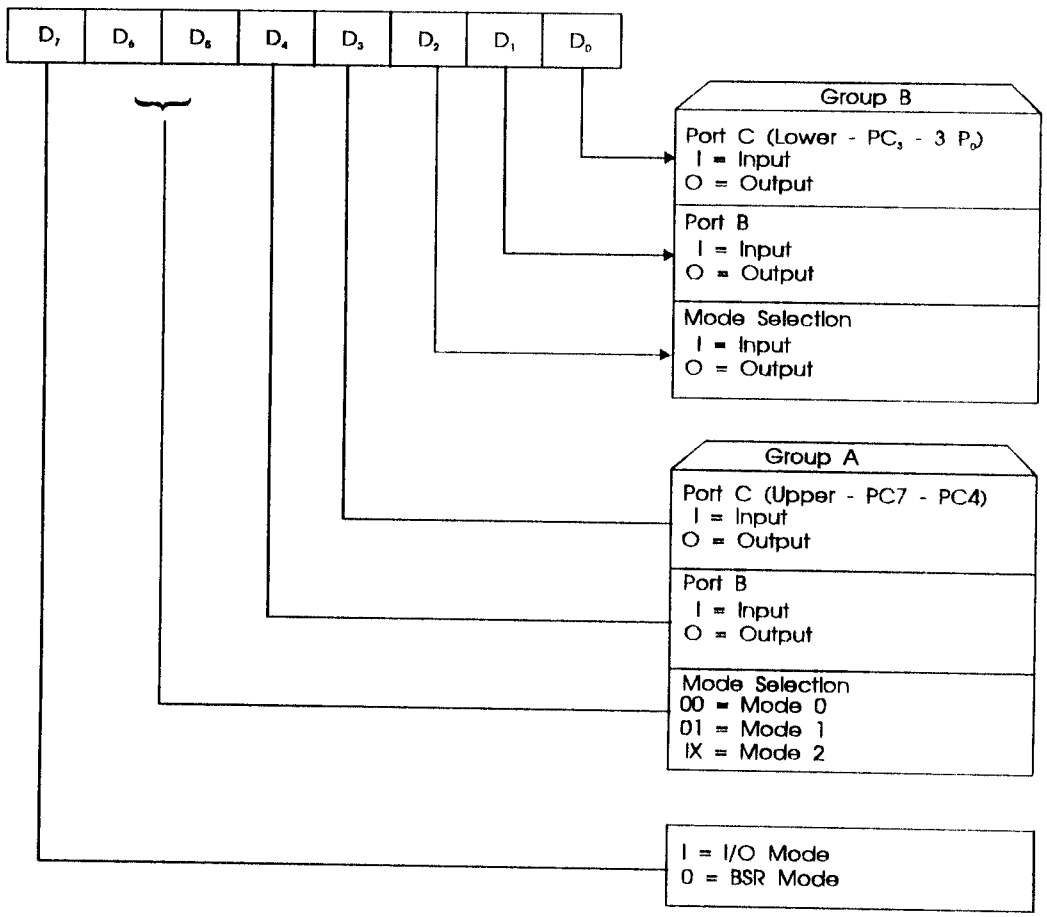


FIGURE 4.2.3
CONTROL WORD FORMAT

port's function as simple I/O port's. Mode1 is a handshake mode whereby port A and/or B use bits from portc as ahndshake signals. In mode 2 port A can be set up for bidirectional data transfer using handshake signals from port C, and port B can be set up either in mode o and mode 1. The bits D6 + D5 are used for mode selection.

The port D4 is used to indicate whether port A is employed if an I/P port or an O/P port. If D4 is 1 it is an I/P port or else it is an O/P port. The bit D3 is used to indicate whether port C (upper) is used as an input or O/P port. If it is 1 then it isI/P or else it is O/P. The Bit D2 is used for mode selection of port B. O is mode O and 1 is mode 1. The bit D1, is used to indicate whether port B is used as an input or output port. The bit Do is also to indicate which the port C (lower) bits are used as I/P or O/P port.

DAC 0808

The purpose of a digital to Analog converter is to convert a binary word to a proportional current or voltage. The DAC 0808 server is an 8 bit monolithic digital to analog converter (DAC) featuring a fullscale output current settling time of 150ns while dissipating only 33mw with ±5V supplies.

D/A CHARACTERISTICS AND SPECIFICATIONS.

The first characteristics of a DAC to consider is the resolution. This is determined by the number of bits in the I/P binary word. A converter with eight binary inputs such as the DAC 0808 has 2^8 or 256 possible O/P levels. So its resolution is 1 part in 256. Resolution is sometimes expressed in percentage. The resolution of an 8 bit converter is about 0.39%. No reference current trimiing is required for most application since the fullscale O/P current is typically ± 1 LSB of 255 IREF/256. The power supply surrents of the DAC 0808 series are independent of bit codes & exhibits essentially constant device characteristics over the entire supply voltage range.

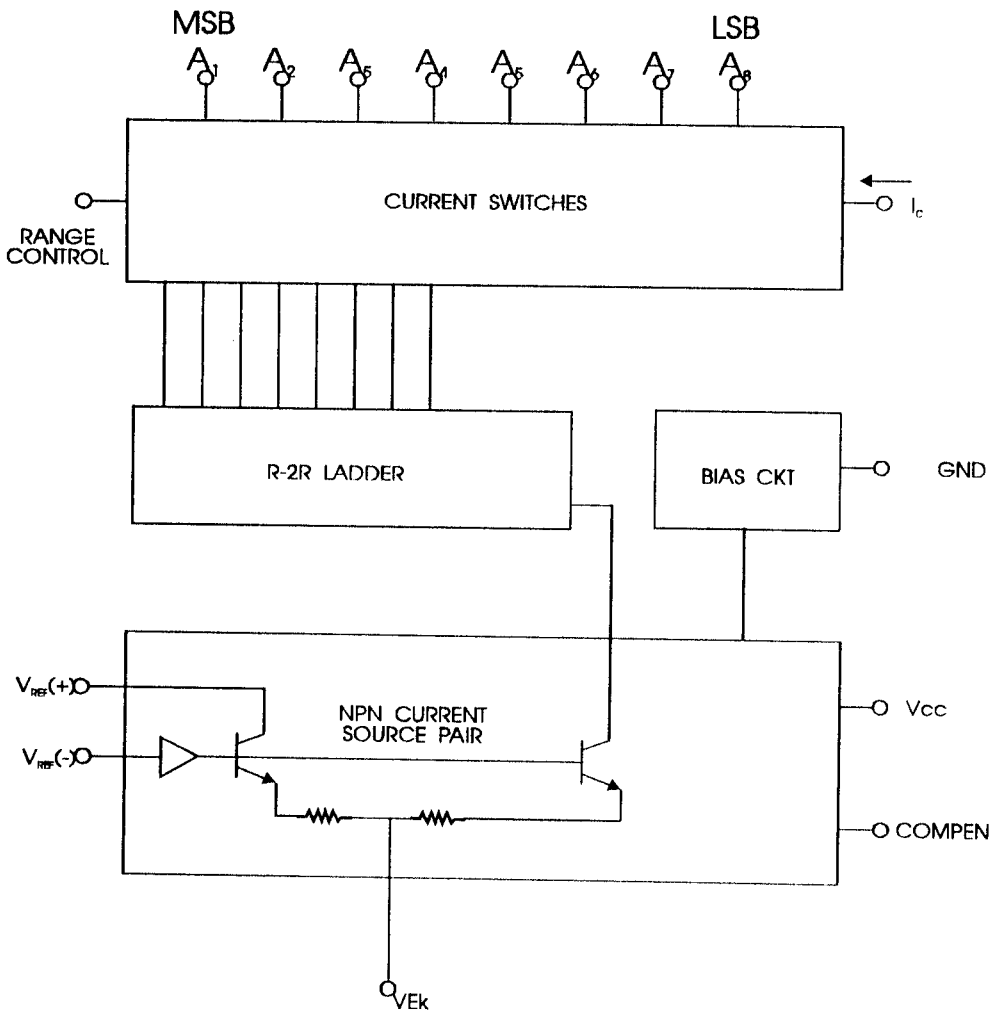


FIGURE 4.3.1
DAC 0808 BLOCK DIAGRAM

Another important specification for D/A converter is linearity. Linearity is the measure of how much the output ramp deviates from a straight line as the converter is stepped from no switches on. Ideally the deviation of the O/P from a straight line should not be greater than ±1/2 Least Significant Bit to maintain overall accuracy.

Still another specification for the D/A converter to be looked upon is settling time. When the binary word applied to the input of the converter is changed, the O/P will change appropriately to the need value. The O/P however may overshoot the correct value and ring for a while, before finally setting down to the correct value. The time taken by the O/P to get within ±1/2 Least Significant Bit of the final value is called on setting time. As mentioned earlier the setting time for DAC 0808 is 150 ns.

The DAC 0808 will interface directly with popular TTL DTL or CMOS logic levels.

DAC 0808 IMPORTANT FEATURES

The supply voltage ranges from $\pm$ 4.5V to $\pm$ 15V. ADC 0808 has a low power consumption and has a fast settling time of typically 150 ns. The O/P voltage is restricted to a range of -0.6 to 0.5v when V_{EE} = -5V. The relative accuracy of the DAC 0808 is essentially constant with temperature due to excellent temperature tracking of the monolothic resister ladder.

ADC 0808

The function of an ADC is to produce a digital word which represents the magnitude of some analog voltage or current. The specification ofan ADC is similar to that of the DAC's. The resolution of an ADC is defined as the number of bits in the output binary word. An 8 bit converter has a resolution of 1 part in 256. Linearity of an ADC is defined as how much the output ramp deviates from the straight line. Another important specification of the ADC is its conversion time. The conversion time is defined as the time taken by the converter to produce a valid output binary code for an applied input voltage. When we refer to a converter as a high speed, we mean it has a short conversion time. There are four commonly employed methods to do Analog to digital conversion. They are single slope ADC, dual slope ADC, parallel comparator ADC and succesive approximation ADC. The ADC 0808 employed here uses the successive approximation method to do the conversion.

ADC 0808 is a monolithic CMOS device with an 8 bit analog to digital converter. 8 Channel multtiplexer and microprocessor compatible control logic. The 0808 DC uses sucessive approximation as the convertion

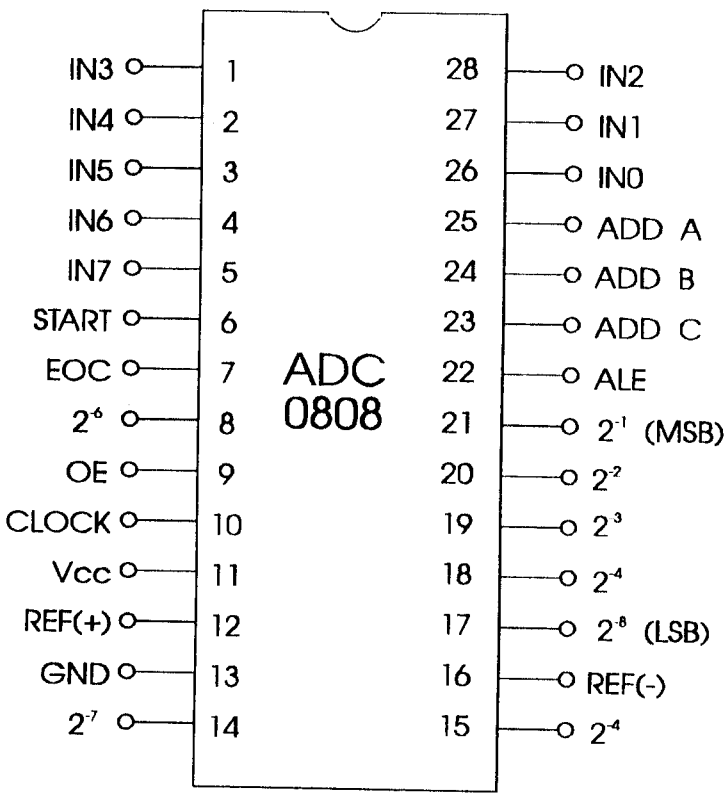


FIGURE 4.5.1
ADC 0808 PIN CONFIGURATION

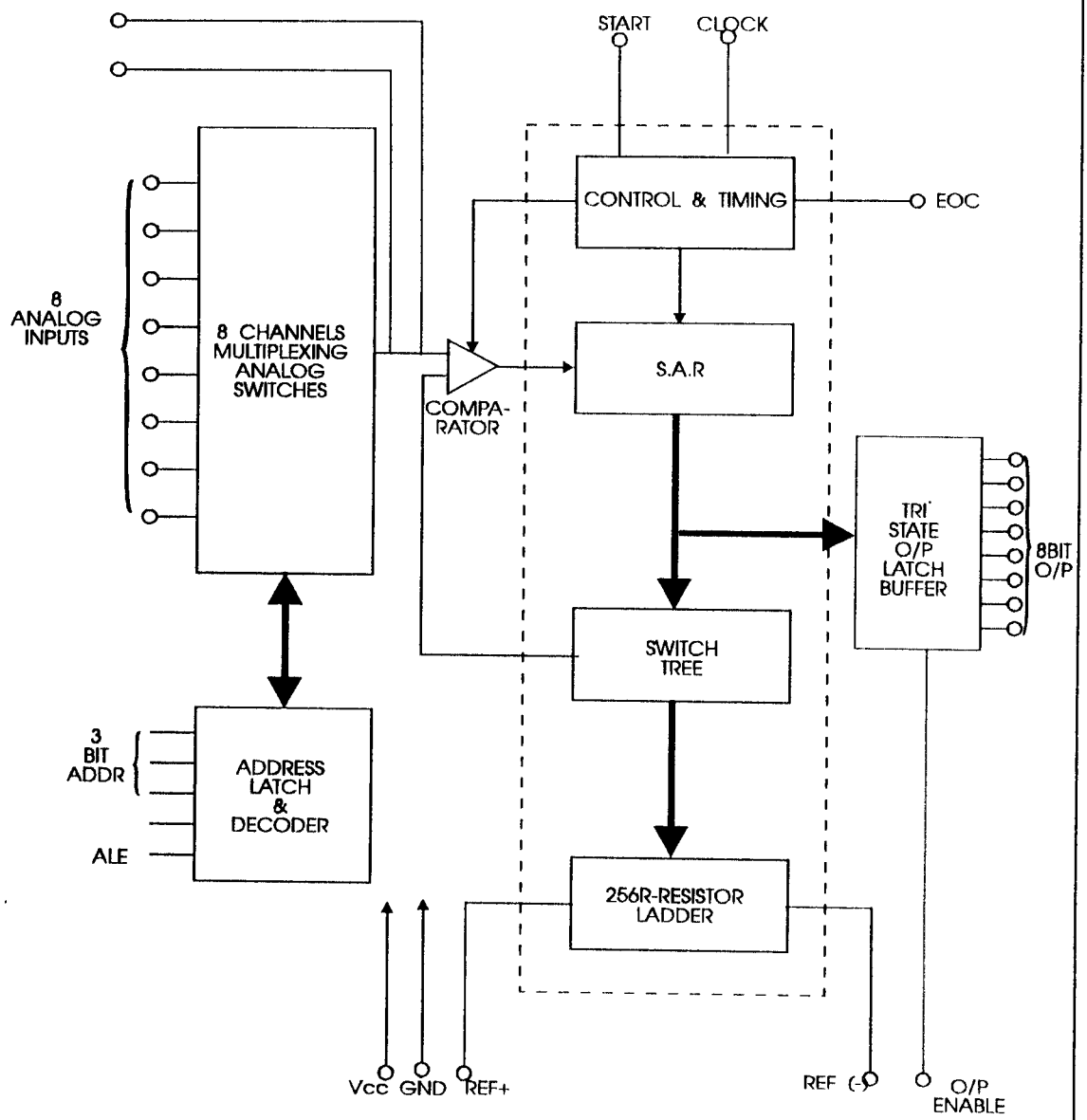


FIGURE 4.5.2
ADC 0808 BLOCK DIAGRAM

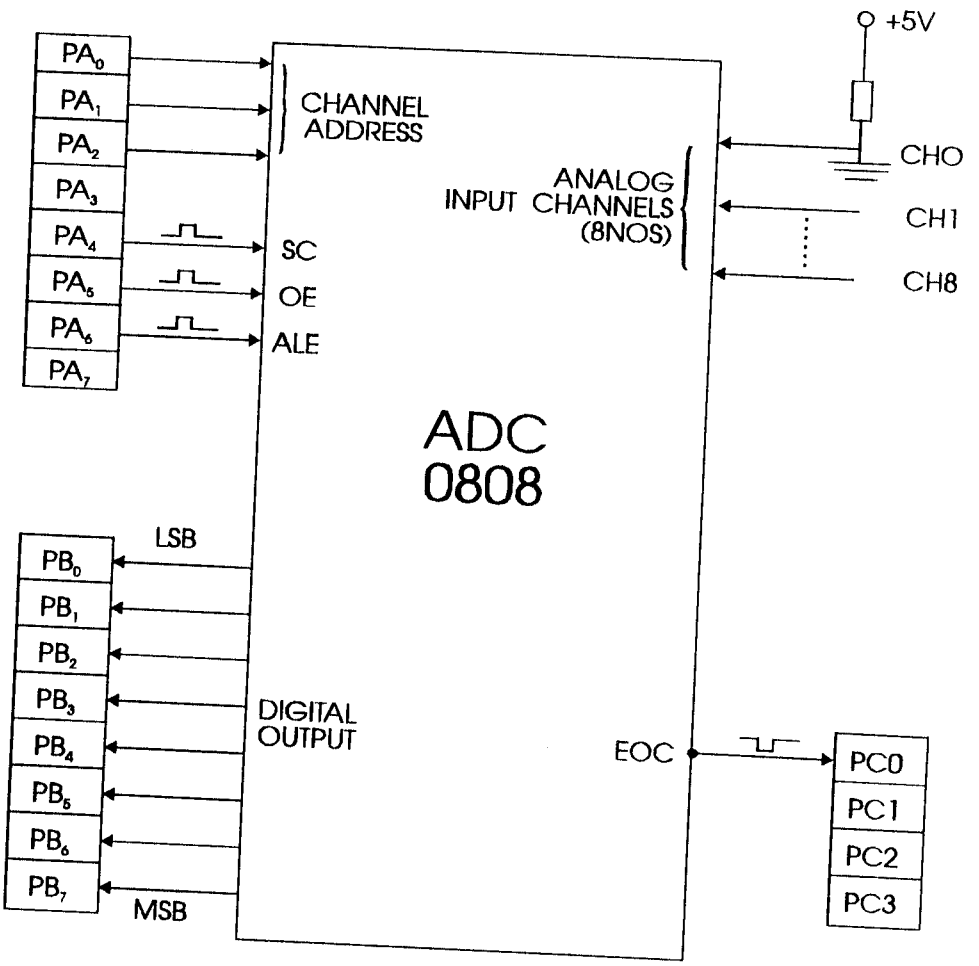


FIGURE 4.5.3
BLOCK DIAGRAM OF ADC SHOWING THE HARDWARE DETAILS

technique. The converter features a high impedence chopper stabilized comparator, a 256 R voltage divider with analog switch tree and a sucessive approximation register. The 8 channel multiplier can directly access any of 18 single ended analog signals.

ADC 0808 can easily be interfaced to microprocessor because of the latched and decoded multiplexer inputs and latched TTL tri state outputs.

Successive aproximation ADC's usually have outputs for each bits. The code output on these bits are usually straight binary or offset binary. You can simply connect the parallel output port pins and read the converter output in under program control. In addition to the data lines, there are two other successive approximation ADC signal lines you need to interface to the microcomputer for data Transfer. The first of these signal line is the START CONVERT (SC) signal. The SC signal is outputted from the Microcomputer to the ADC, to tell it to start doing the conversions. The second signal is a status signal which the ADC outputs to indicate that the conversion is complete and that the word on the outputs is valid. The signal is also called on END OF CONVERSION (EOC).

ADC 0808 FUNCTIONAL DESCRIPTION

MULTIPLEXER

The device contain a 8 channel single ended signal multiplexer. A particular I/P channel is selected by using the address decoder. The address is latched into the decoder on the low to high traansisttion of the ALE signal. Table 1 shows the I/P states for the address lines to select any channel.

THE CONVERTER

The heart of the ADC 0808 is its 8 bit analog to Digital converter. The converter is designed to give fast,accurate and repeatable conversions over a wide range of temperature. The converter is partitioned into 3 major sections. The 256R Ladder network, the successive approximation register and the comparator.

The ADC's successive approximation register is reset on the positive edge of the start conversion pulse. The conversion is began on the falling edge of the start conversion pulse.

The most important section of ADC is the comparator. It determines the accuracy of the entire converter.

AMPLIFIERS

The LM158 series consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include trasducer amplifiers,dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM158 series can be directly operated off of the standard +5 V_{DC} power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional $\pm$ 15 V_{DC} power supplies.

UNIQUE CHARACTERISTICS

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

The unity gain cross frequency is temperature compensated.

The input bias current is also temperature compensated.

ADVANTAGES

Eliminates need for dual supplies.

Two internally compensated op amps in a single package.

Allows directly sensing near GND and V_{OUT} also goes to GND.

Compatible with all forms of logic.

Power drain suitable for battery operation

FEATURES

Internally frequency compensated for unity gain. Large dc voltage gain 100 db.Wide bandwidth (Unity Gain) 1MHZ (temperature compensated) wide power supply range: Single Supply 3 V_{dc} to 30 V_{DC} or dual supplies +1.5 V_{DC} to +15 V_{DC}. Very low supply current drain (500*A) - essentially independent of supply voltage (1 mW/op amp at +5 V_{DC}). Low input biasing current (temperature compensated) 45nA_{DC}. Low input offset voltage 2mV_{DC} and offset current 5 nA_{DC}. Input common-mode voltage range includes

ground . Differential input voltage range equal to the power supply voltage. Large output voltage swing $0V_{DC}$ to V_+ -1.5 V_{DC}.

ABOUT THE METER

The meter based on which we have fabricated the prototype is RPM meter presently used in all suzuki vehicles. The outstnading feature of this meter is that it uses an IC CS8190, which provides all the functions necesary for an analog Tachometer. Also the coil used for deflection is of the cross coil type.

C S 8190: PRECISION AIR CORE TACHO/SPEEDO DRIVER

CS 8190 manufactured by cherry semiconductors corporation is a dedicated IC specifically designed for use with air core meter movements. This IC provides all the functions necessary for an analog Tachometer or speedometer. The CS -8190 takes a speed sensor input and generates sine and cosine related output, to differentially drive an aircore meter.

This CS 8190 IC is an enhanced version of the previously used industry standards like CS. 289 or LM 1819. The output utilizes differential driver's which eliminates the need for a zever referenceand offers more fortue. The device withstands 60v tranciets which decreases the protection circuitry

required. The device is also more precise than existing devices allowing for fewer trims and for use in a speedometer.

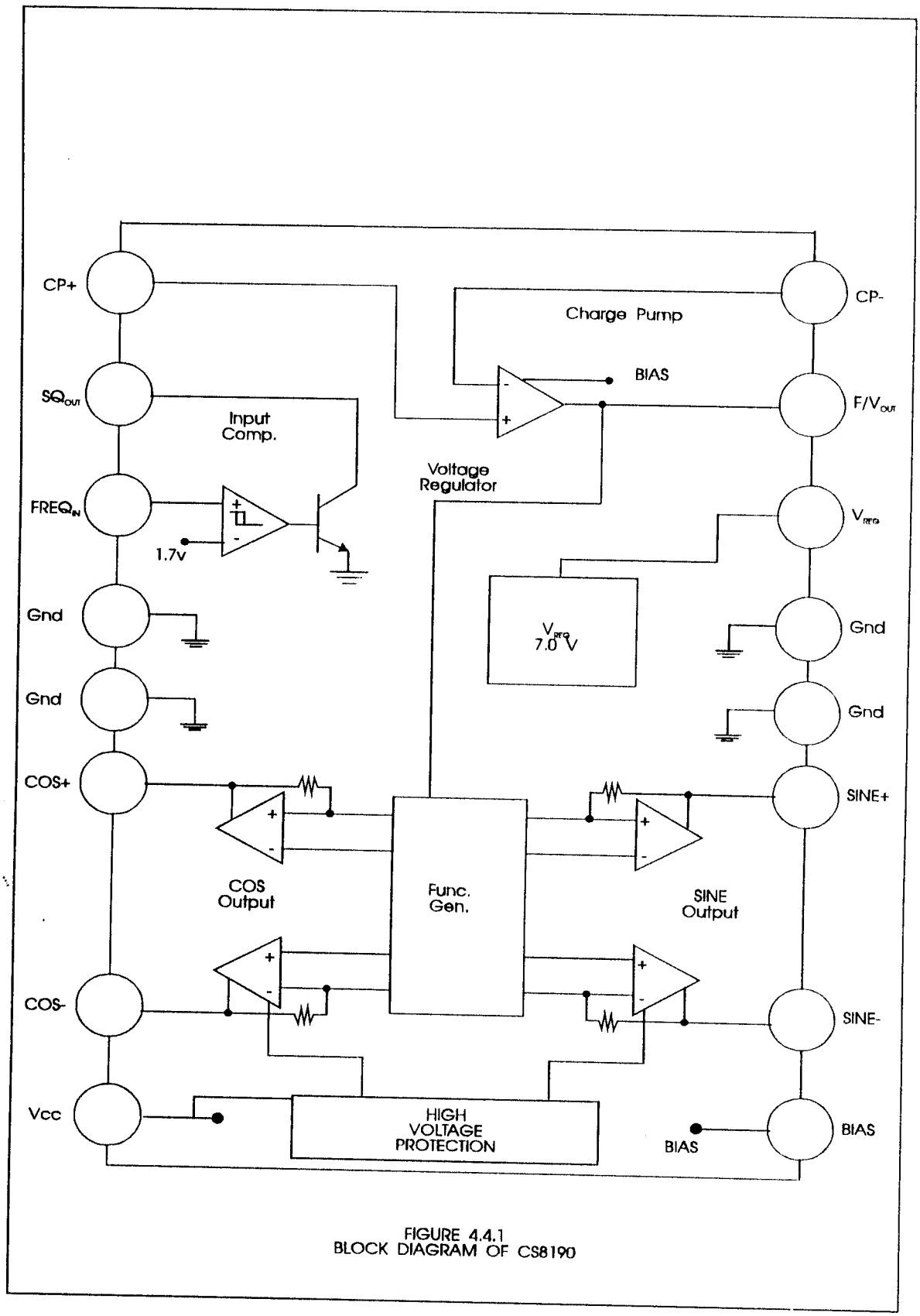
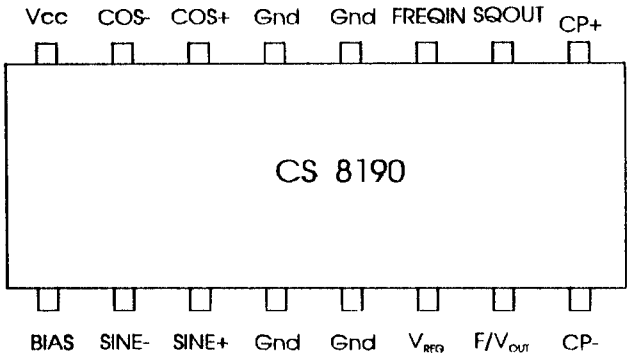


FIGURE 4.4.1
BLOCK DIAGRAM OF CS8190

FIGURE 4.4.2
PINCONFIGURATION OF CS8190



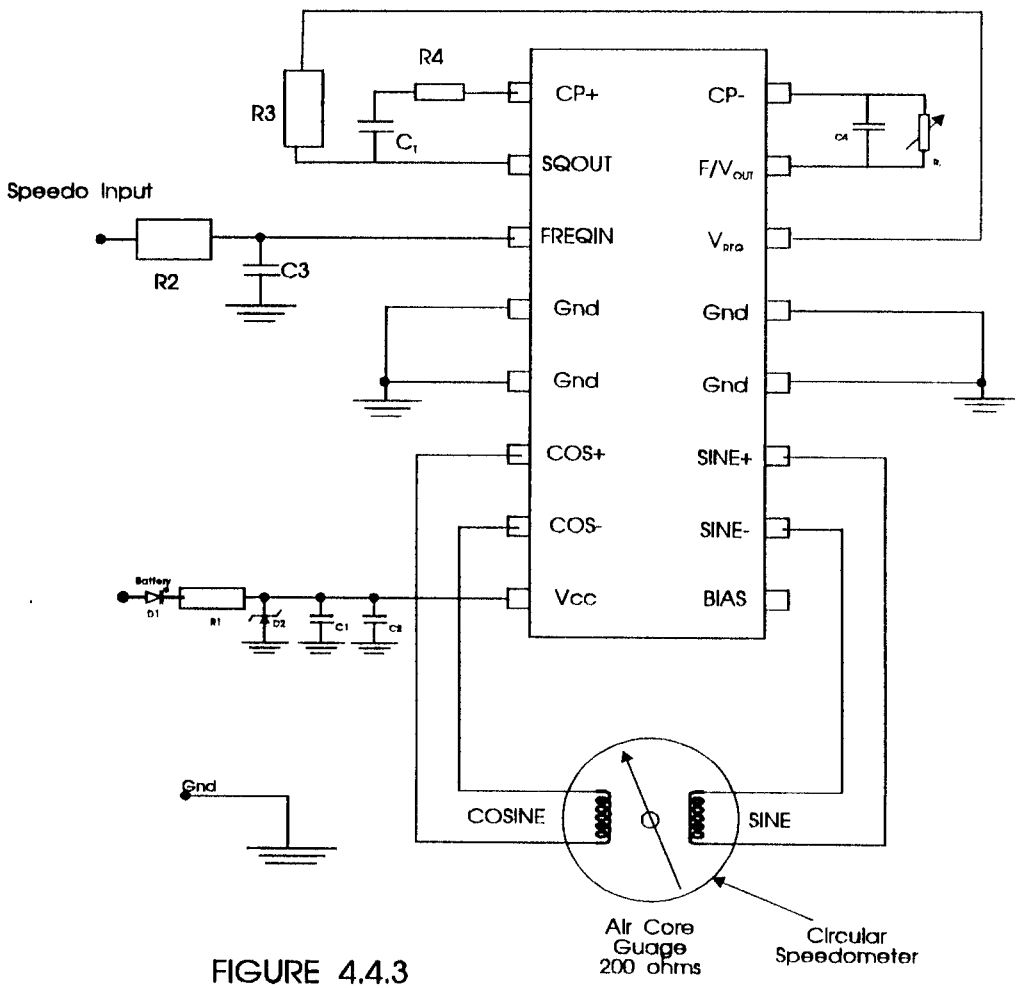


FIGURE 4.4.3
CIRCUIT DIAGRAM FOR
TACHO METER APPLICATION

BLOCK DIAGRAM DESCRIPTION

CS 8190 is specifically designed for use with aircore movements. The IC includes an input comparator using input frequency such as a vehicle speed or RPM, a charge pump for frequency to voltage conversions, a band gap voltage regulators for stable operation, a function generation with sine and cosine amplifiers differentially driving the motor coils.

INPUT COMPARATOR SECTION

The frequency input is to a high impedance comparator with a typical positive input threshold of 2.0v and typical negative threshold of 1.5v small signals possibly from the reluctance coil can be directly input to the device eliminating the need for external buffer circuitry.

CHARGE PUMP SECTION

The charge pump section uses the output of the comparator for frequency to voltage conversions. The charge pump output voltage range from 2v (0=0°) to 6.V (0 = 305°). The charge accumulated on Ct is mirrored to (outtry the Norton Amplifier. An internal full Wave current rectifier doubles the input

frequency, halves the valve of output voltage ripple. Due to IC and external component tolerance, each module will require trimming of RT.

The frequency to voltage conversion is given by the expression.

$$V = 2f C_T R_T (V_{REG} - V_D + V_{CL}) + 2.0V$$

(for derivation please refer Appendix)

RETURN TO ZERO

The IC has onboard circuitry which when taken advantage of will return the pointer to Zero when power is removed. A large external Capacitor (C4) is required to take advantage of this feature. The value must be approximately 2000 µf on the IC there are two undervoltage detectors which control the position of the pointer on the dial when the power is off. As the supply is dacaying the first detector suppression the input signal which starts the needle moving counter clockwise, the second detector forces '0' Volts across sine coil and maximum allowable positive voltage across the cosine coil.

FUNCTION GENERATOR: SINE AND COSINE GENERATOR

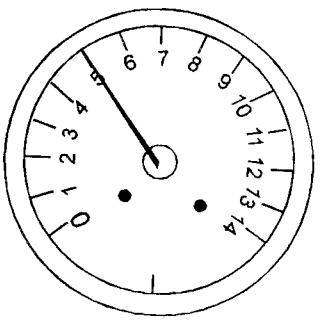
The output wave forms of the sine and cosine amplifiers are derived from on chip amplifier and function generator circuitry. The various trip points for the circuit are determined by an internal resistance divider and bandgap voltage reference. The coil differentially driven allows bidirectional current in the output thus attaining 305° meter movememt. Differentially driving the coils after faster response time, higher current capability, higher output voltage swings and reduced external component count. The advantage is a higher torque output for the pointer.

METER COIL

The coil that is employed in the RPM meter is a cross coil air core type coil. Aircore meters are often favoured over other movements as a result of their mechanical ruggedness.

There are three basic pieces they are, a Magnet, a Pointer attached to a freely rotating axle oriented at right angles to each other. The only other moving part in the meter is the axle assembly. The Magnet will tend to align itself with the vector sum of the M-fields of each coil where M is the

magnetic field strength vector. In an air core meter the axle assembly is supported by two nylon bushings. The torque exerted on the pointer is much greater than found in a typical D'arsonval movement. In constant to D'arsonval movement where calibration is a function of spring and magnet characteristics, air core meter calibration is affected only by mechanical alignment of the drive coils.



Advantages & Limitations

ADVANTAGES AND LIMITATIONS

ADVANTAGES

ART boasts of many an advantage over the present testing method. The foremost advantages of our method is that the tolerance level once set by the Testing staff remain the same through out all the frequencies whereas in the Manual testing procedure it is left to the discretion of the testing staff and the tolerance level depends only upon the judgement of the staff.

The time taken to test a meter by our method is very much faster than to test a meter by ther Manual testing method. It has been estimated that to test a Meter by Manual testing procedure. It takes atleast 5 Minutes whereas by our Method it takes utmost 1 minute. If in a day we are able to test about 50 RPM meters by the manual procedure, we can test around 250-300 RPM meters by employing Automatic testing procedure.

Our testing method ie ART can be test different Meters with diofferent ranges whereas the Manual testing procedure is also to test only one type of

RPM meter. To test any other RPM meter of different ranges the component values have to be changed.

Since our method is a microprocessor based testing Method there are added advantages of a microprocessor like.

(i) Stability

(ii) Accuracy of control.

(iii) Flexibility

(iv) Greater reliability and equipment life.

(v) Human factor favouring digital interface.

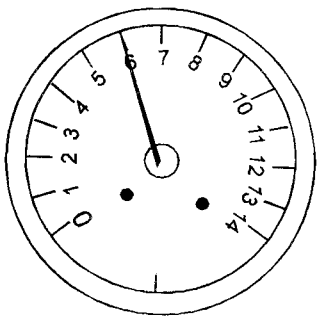
Our testing method ie. ART is able to detect whether the fault lies in the IC or the meter Coil, whereas in the Manual procedure we are just able to know that an error is present and not the location of the error.

LIMITATION

The initial cost for constructing the tester is high.

Testing method just detect an error but error correction is not possible.

There is also some limitation due to approximation in the software listings.



Software Listings

SOFTWARE LISTINGS

ALGORITHM

1. Using the DAC a positive going pulse of frequency 33Hz is generated.

2. This waveform is fed to the meter.

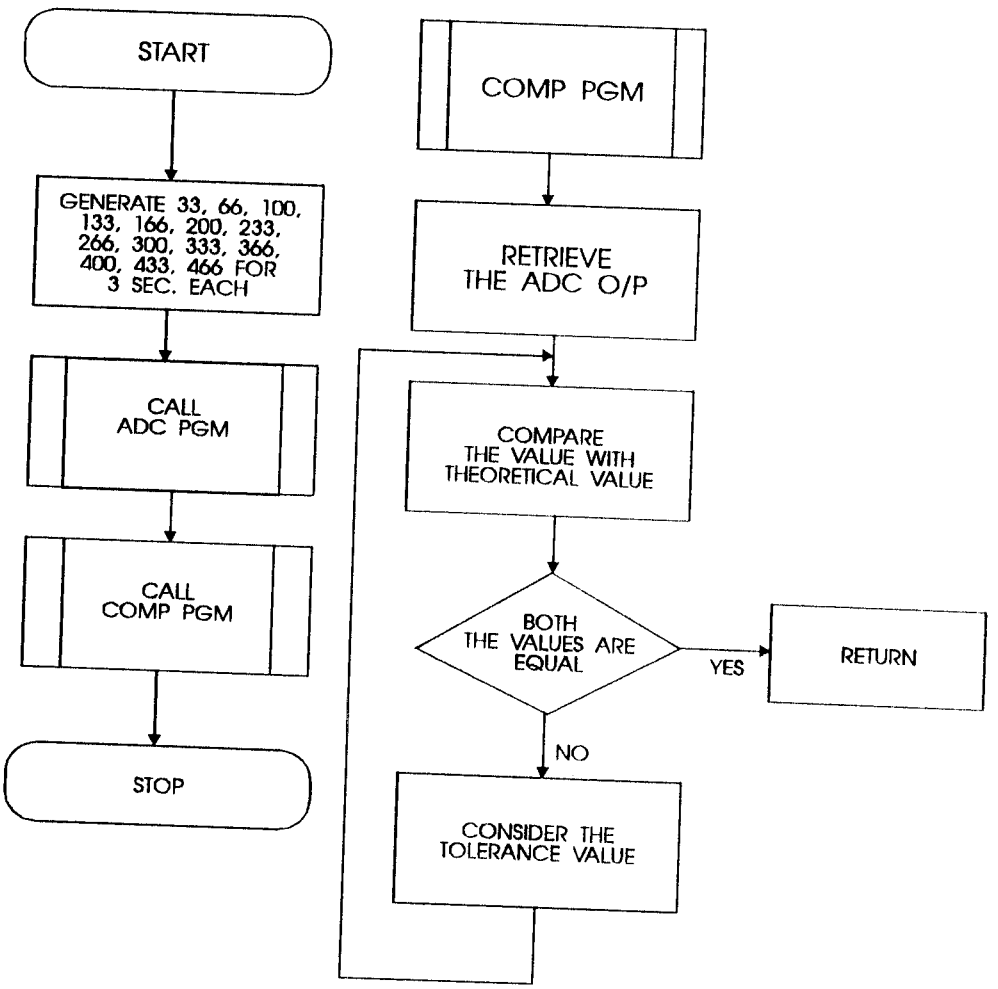
3. From the F/V pin of IC CS8190 of meter voltage is taken and fed to the ADC.

4. The ADC O/P is compared with the theoretical value stored in the microprocessor 8085 memory considering the tolerance into account.

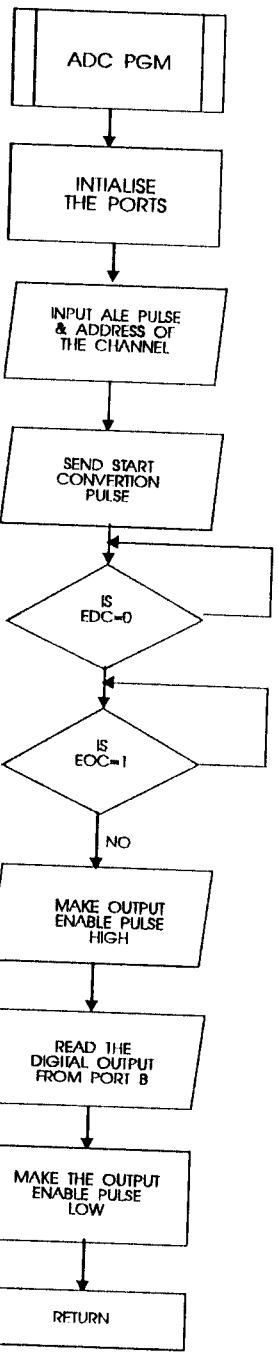
5. This is repeated for frequencies up to 466 Hz.

6. For every frequency if the values are correct display good else display error.

FLOW CHART


START
GENERATE 33, 66, 100, 133, 166, 200, 233, 266, 300, 333, 366, 400, 433, 466 FOR 3 SEC. EACH
CALL ADC PGM
CALL COMP PGM
STOP
COMP PGM
RETRIEVE THE ADC O/P
COMPARE THE VALUE WITH THEORETICAL VALUE
BOTH THE VALUES ARE EQUAL
YES
RETURN
NO
CONSIDER THE TOLERANCE VALUE

FLOW CHART


ADC PGM
INTIALISE THE PORTS
INPUT ALE PULSE & ADDRESS OF THE CHANNEL
SEND START CONVERTION PULSE
IS EDC=0
IS EOC=1
NO
MAKE OUTPUT ENABLE PULSE HIGH
READ THE DIGITAL OUTPUT FROM PORT B
MAKE THE OUTPUT ENABLE PULSE LOW
RETURN

MAIN PROGRAM

	MVI A, 80	COMMAND WORD FOR DAC
	OUT 03	
	MVI A,83	COMMAND WORD FOR ADC
	OUT 43	
	LXI D, 0012C	
L1	MVI A,00	
	OUT 00	
	CALL DELAY 1	
	MVI A, FF	PROGRAM FOR GENERATING 100Hz
	OUT 00	FOR 3 SECONDS
	CALL DELAY 1	
	DCX D	
	JNZ L1	
	CALL ADC PGM	
	CALL COMP PGM	
	LXI D, 0258	
L2	MVI A,00	
	OUT 00	
	CALL DELAY 2	
	MVI A, FF	PROGRAM FOR GENERATING 200Hz
	OUT 00	FOR 3 SECONDS
	CALL DELAY 2	
	DCX D	
	JNZ L2	
	CALL ADC PGM	
	CALL COMP PGM	
	LXI D, 0384	

L3	MVI A,00	
	OUT 00	
	CALL DELAY 3	
	MVI A, FF	PROGRAM FOR GENERATING 300Hz
	OUT 00	FOR 3 SECONDS
	CALL DELAY 3	
	DCX D	
	JNZ L3	
	CALL ADC PGM	
	CALL COMP PGM	
	LXI D, 0460	
L4	MVI A,00	
	OUT 00	
	CALL DELAY 4	
	MVI A, FF	PROGRAM FOR GENERATING 400Hz
	OUT 00	FOR 3 SECONDS
	CALL DELAY 4	
	DCX D	
	JNZ L4	
	CALL ADC PGM	
	CALL COMP PGM	
	LXI D, 0576	
L5	MVI A,00	
	OUT 00	
	CALL DELAY 5	
	MVI A, FF	PROGRAM FOR GENERATING 466Hz
	OUT 00	FOR 3 SECONDS
	CALL DELAY 5	
	DCX D	

	JNZ L5	
	CALL ADC PGM	
	CALL COMP PGM	
	DISPLAY `GOOD'	
	STOP	

SUBPROGRAM FOR DELAYS

DELAY 1	PUSH B
	PUSH H
	MVI B, 04
L2	LXI H, A500
L1	MOV A,L
	ORA H
	DCR H
	JNZ L1
	DCR B
	JNZ L2
	POP H
	POP B
	RET
DELAY 2	PUSH B
	PUSH H
	MVI B, 04
L2	LXI H, 5200
L1	MOV A,L
	ORA H
	DCR H
	JNZ L1
	DCR B
	JNZ L2
	POP H
	POP B
	RET
DELAY 3	PUSH B
	PUSH H
	MVI B, 04

L2	LXI H, 3700
L1	MOV A,L
	ORA H
	DCR H
	JNZ L1
	DCR B
	JNZ L2
	POP H
	POP B
	RET
DELAY 4	PUSH B
	PUSH H
	MVI B, 04
L2	LXI H, 2990
L1	MOV A,L
	ORA H
	DCR H
	JNZ L1
	DCR B
	JNZ L2
	POP H
	POP B
	RET
DELAY 5	PUSH B
	PUSH H
	MVI B, 04
L2	LXI H, 2490
L1	MOV A,L
	ORA H
	DCR H
	JNZ L1
	DCR B

	JNZ L2
	POP H
	POP B
	RET

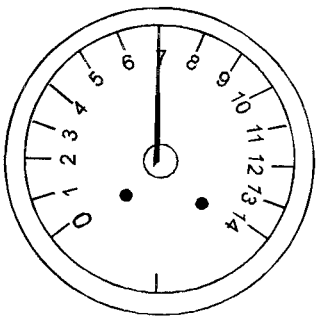
SUBPROGRAM FOR ADC

ADC PGM:	MVI A, 00	
	OUT 40	
	MVI A, 40	SENDING ALE PULSE
	OUT 40	AND ADDRESS
	MVI A, 00	
	OUT 40	
	MVI A, 10	
	OUT 40	SENDING START CONVERSION
	MVI A, 00	PULSE
	OUT 40	
L1	IN 42	
	ANI 01	
	RAR	
	JC L1	TO CHECK THE EOC PULSE HAS
L2	IN 42	BEEN RECEIVED
	ANI 01	
	RAR	
	JC L2	
	MVI A,20	SENDING READ PULSE
	OUT 40	
	IN 41	
	MOV C,A	
DELAY	PUSH B	
	PUSH D	
	MVI B, F1	
L2	LXI D, 01E9	
L1	DCX D	

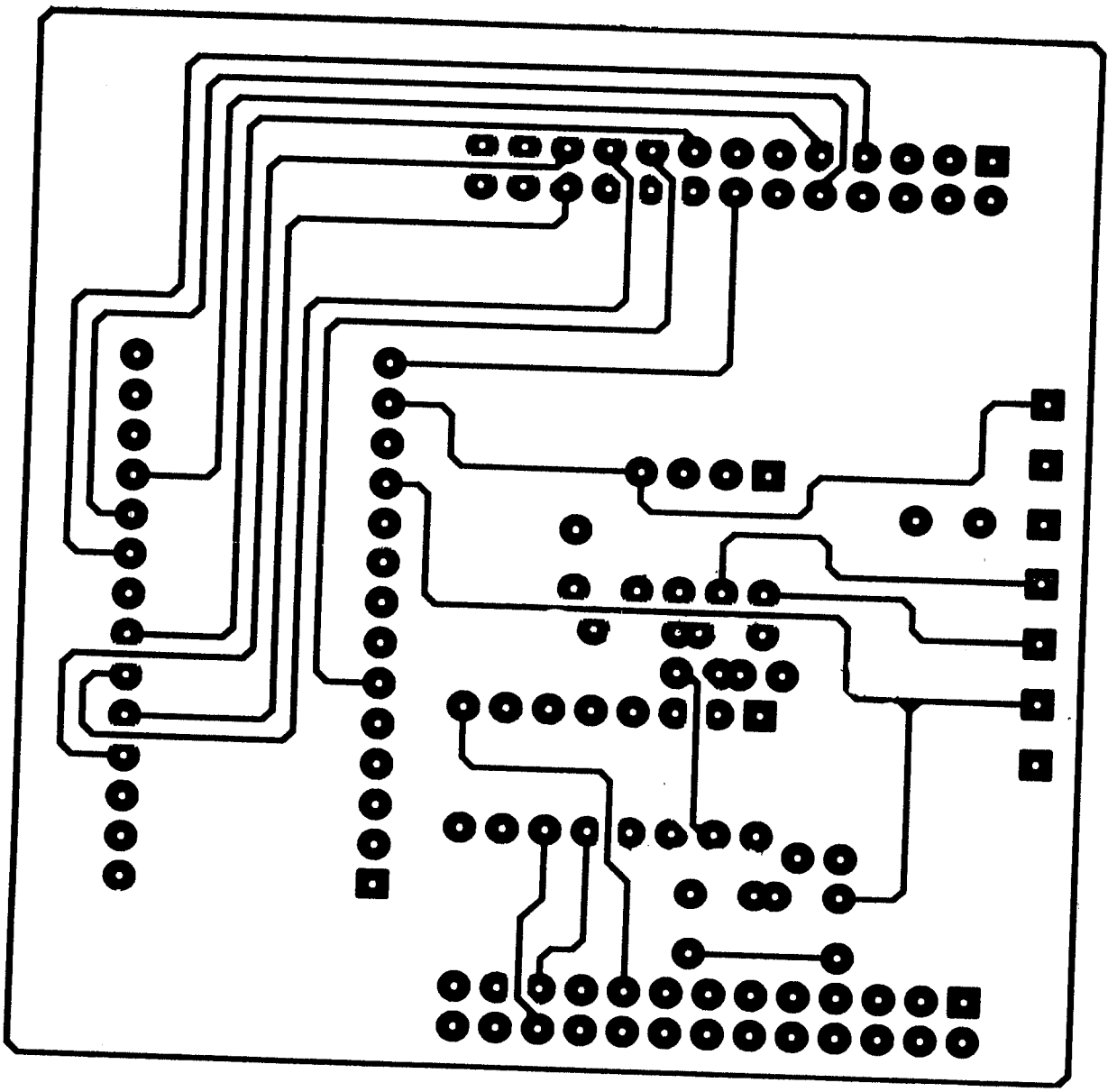
	MOV, A,E	
	ORA D	
	JNZ L1	
	DCR B	
	JNZ L2	
	POP D	
	POP B	
	RET	

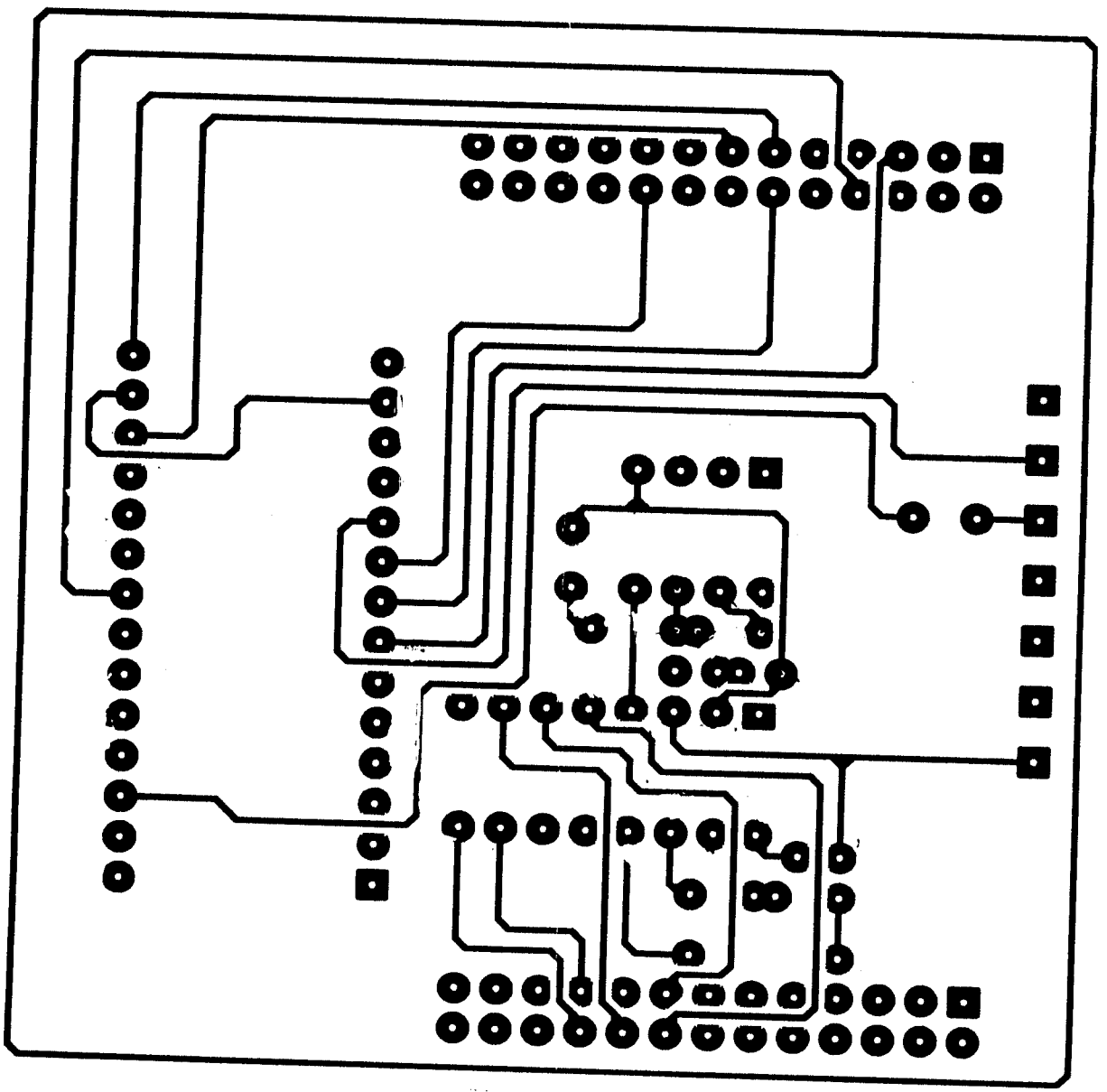
SUBPROGRAM FOR COMPARING

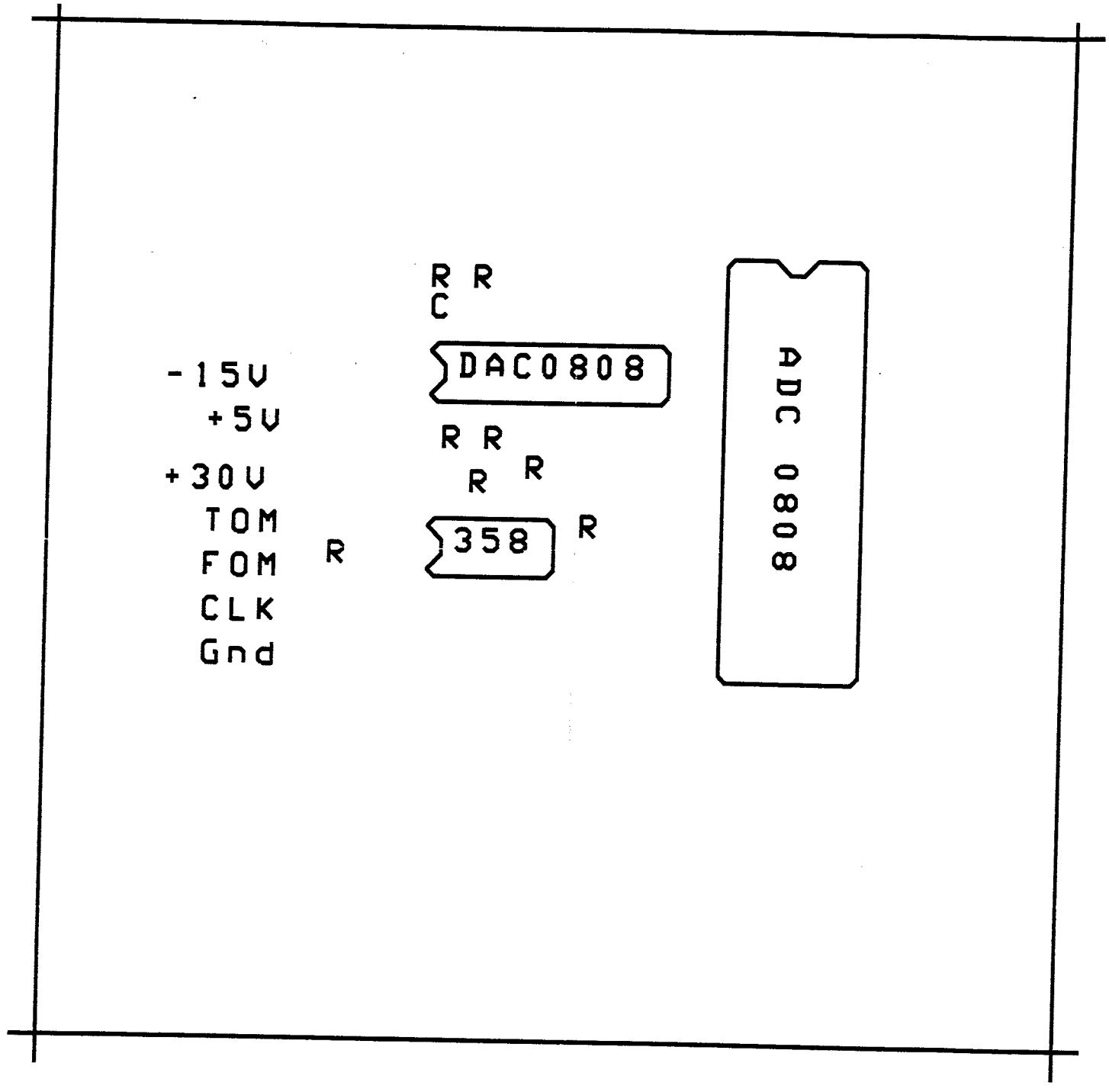
COMP PGM	LXI H, 9000
	MVI B
	MVI A,C
L1	CMP M
	RZ
	INX M
	DCR B
	JNZ L1
	DISPLAY `ERROR'
	STOP

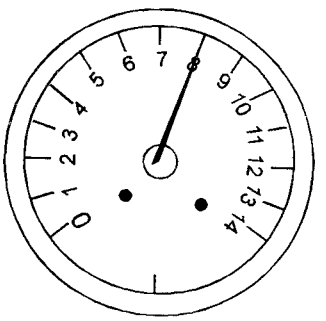


PCB Design






R R
C
-15V
DAC0808
+5V
R R
+30V
R R
TOM
358
R
FOM
R
CLK
Gnd
ADC 0808



Conclusion

CONCLUSION

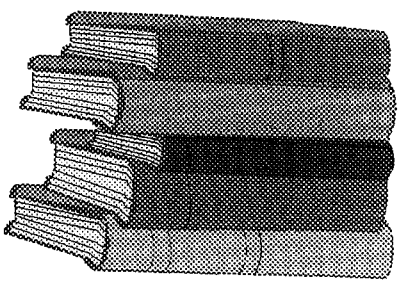
The testing circuit designed by us was after looking into all the constraints posed. The tester was designed by us taking into consideration the need for an accurate testing method.

Even though the initial cost is high, taking into account the various advantages that ART holds over the other method these expenses are worth incurring.

With the stride and advancement in the field of electronics and IC technology we should look in for an ideal system to avoid losses as wastage of time.

The discrete model of this system was tested in the laboratory environment and their characteristics were studied. Based on this protype model the system was tested successfully.

PRICOL is assisting us to technically promote the system and to further increase it sophistication.



Bibliography

BIBLIOGRAPHY

1. Microprocessor Architecture programming and Applications
   - ***Ramesh S. Gaonkar***

2. Microprocessor Interfacing Techniques Techniques & Applications
   - ***Douglas V. hall***

3. Digital Principles & Applications
   - ***Albert Paul Malvino***
   Donald P. Leach.

4. Linear Applications Handbook
   - National Semiconductor Corporation, Santa Clara.

5. Digital & Analog systems, Circuits and Devices
   - ***Belove & Schilling***

6. Digital instrumentation
   - ***Bouwens***

7. Electronics in industry
   - ***Chute***

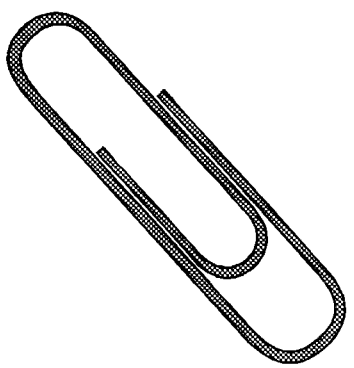
8. Microprocessors and Digital Systems
   - ***Douglas V. Hall***

9. Electronics Fundamentals and applications for Engineers and scientists
   - ***Millman & Halkias***

10. Digital Integrated Electronics
    - ***Taub and Schilling***

11. Microelectronics Digital and Analog Circuit and systems
    - ***Millman .J***

12. Electronics Devices and Circuits
    - ***G.K. Mithal***



Appendix

CS-8190

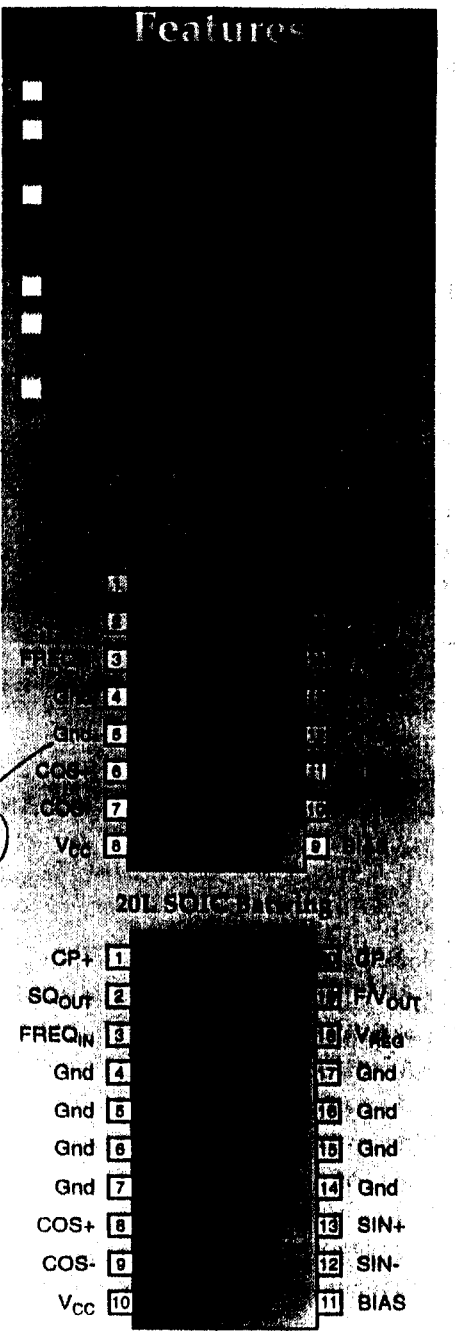
Precision Air-Core Tach/Speedo Driver

Description

The CS-8190 is specifically designed for use with air core meter movements. The IC provides all the functions necessary for an analog tachometer or speedometer. The CS-8190 takes a speed sensor input and generates a sine and cosine related output to differentially drive an air core motor.

Many enhancements have been added over industry standard tachometer drivers such as the CS-289 or LM1819. The output utilizes differential drivers which eliminates the need for a zener reference and offers more torque. The device withstands 60V transients which decreases the protection circuitry required. The device is also more precise than existing devices allowing for fewer trims and for use in a speedometer.

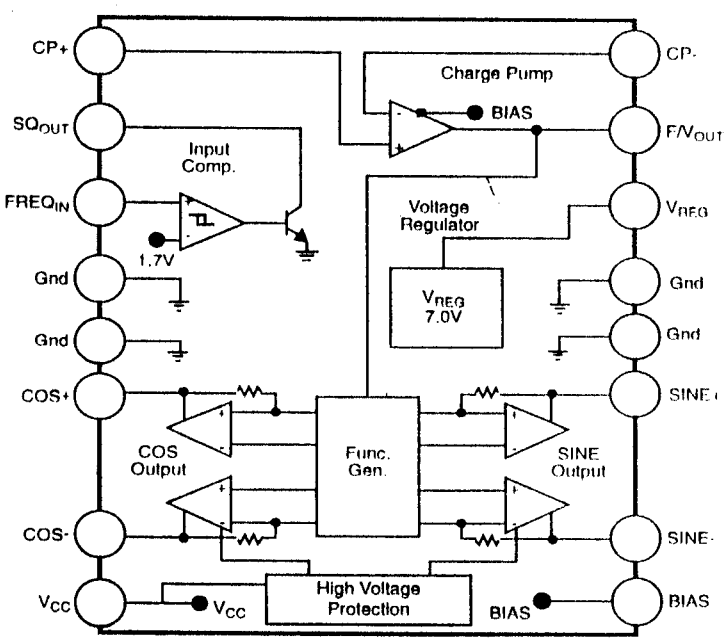
Features



Absolute Maximum Ratings

Supply Voltage (<100ms pulse transient) ..... V_{CC} = 60V
(continuous) ..... V_{CC} = 24V
Operating Temperature ..... -40°C to +105°C
Storage Temperature ..... -40°C to +165°C
Junction Temperature ..... -40°C to +150°C
ESD (Human Body Model) 4kV

Block Diagram



CSC™ CHERRY SEMICONDUCTOR

Cherry Semiconductor Corporation
2000 South County Trail
East Greenwich, Rhode Island 02818-1530
Tel: (401)885-3600 Fax (401)885-5786
Telex WUI 6817157

Electrical Characteristics: -40°C ≤ T_A ≤ 85°C, 8.5V ≤ V_{CC} ≤ 15V unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage Section					
I_{CC} Supply Current	V_{CC} = 16V, -40°C, No Load		50	125	mA
V_{CC} Normal Operation Range		8.5	13.1	16.0	V
Input Comparator Section					
Positive Input Threshold		1.0	2.0	3.0	V
Input Hysteresis		200	500		mV
Input Bias Current **	0V≤V_{IN}≤8V		-10	-80	µA
Input Frequency Range		0		20	KHz
Input Voltage Range	in series with 1kΩ	-1		V_{CC}	V
Output V_{SAT}	I_{CC} = 10mA		0.15	0.40	V
Output Leakage	V_{CC} = 7V			10	µA
Low V_{CC} Disable Threshold		7.0	8.0	8.5	V
Logic 0 Input Voltage		1			V
Voltage Regulator Section					
Output Voltage		6.25	7.00	7.50	V
Output Load Current				10 /	mA
Output Load Regulation	0 to 10 mA		10	50	mV
Output Line Regulation	8.5V≤V_{CC}≤16V		20	150	mV
Power Supply Rejection	V_{CC} = 13.1V, 1Vp/p 1kHz		46	34	dB
Charge Pump Section					
Inverting Input Voltage		1.5	2.0	2.5	V
Input Bias Current			40	150	nA
V_{bias} Input Voltage		1.5	2.0	2.5	V
Non Invert. Input Voltage	I_{IN} = 1mA		0.7	1.1	V
Linearity	@ 0, 87.5, 175, 262.5, + 350Hz	-0.10	0.28	+0.70	%
F/V_{OUT} Gain	@ 350Hz	7	10	13	mV/Hz
Norton Gain, Positive	I_{IN} = 15µA	0.9	1.0	1.1	I/I
Norton Gain, Negative	I_{IN} = 15µA	0.9	1.0	1.1	I/I
Function Generator Section: T_A = 25°C, V_{CC} = 13.1V unless otherwise noted.					
Differential Drive Voltage (V_{COS+} - V_{COS-})	8.5V≤V_{CC}≤16V, Θ = 0°	6.0	6.5	7.0	V
Differential Drive Voltage (V_{SIN+} - V_{SIN-})	8.5V≤V_{CC}≤16V, Θ = 90°	6.0	6.5	7.0	V
Differential Drive Voltage (V_{COS+} - V_{COS-})	8.5V≤V_{CC}≤16V, Θ = 180°	-6.0	-6.5	-7.0	V
Differential Drive Voltage (V_{SIN+} - V_{SIN-})	8.5V≤V_{CC}≤16V, Θ = 270°	-6.0	-6.5	-7.0	V
Differential Drive Current	8.5V≤V_{CC}≤16V		33	42	mA
Zero Hertz Output Angle		-1.5	0.0	1.5	deg
Function Generator Error * Reference Figures 1,2,3,4	V_{CC} = 13.1V, Θ = 0° to 305°	-2	0	+2	deg

Electrical Characteristics: continued

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Function Generator Section: continued					
Function Generator Error	$13.1V \le V_{CC} \le 16V$	-1	0	+1	deg
Function Generator Error	$13.1V \le V_{CC} \le 11V$	-1	0	+1	deg
Function Generator Error	$13.1V \le V_{CC} \le 9V$	-3	0	+3	deg
Function Generator Error	$25°C \le T_A \le 80°C$	-2	0	+2	deg
Function Generator Error	$25°C \le T_A \le 105°C$	-4	0	+4	deg
Function Generator Error	$-40°C \le T_A \le 25°C$	-3	0	+3	deg
Function Generator Gain	$T_A = 25°C$ Θ vs F/V_{OUT}	60	77	95	°/V

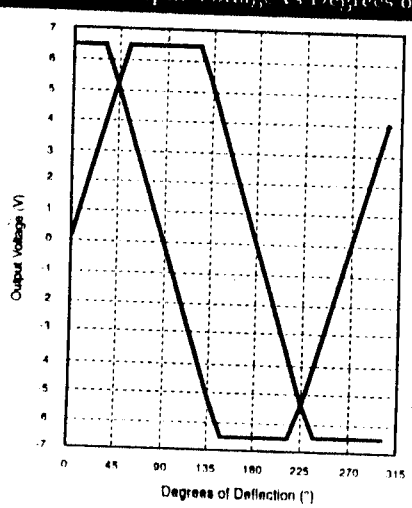
Note 1: Deviation from nominal per Table 1 after calibration at 0 and 270°.
Note 2: Input is clamped by an internal 12V Zener.

Package Pin Description

PACKAGE PIN #		PIN SYMBOL	FUNCTION
16L	20L		
1	1	CP+	Positive input to charge pump.
2	2	SQ_{OUT}	Buffered square wave output signal
3	3	$FREQ_{IN}$	Speed or rpm input signal.
4, 5, 12, 13	4-7, 14-17	Gnd	Ground Connections.
6	8	COS+	Positive cosine output signal.
7	9	COS-	Negative cosine output signal.
8	10	V_{CC}	Ignition or battery supply voltage.
9	11	BIAS	Test point or Zero adjustment.
10	12	SIN-	Negative sine output signal.
11	13	SIN+	Positive sine output signal.
14	18	V_{REG}	Voltage regulator output.
15	19	F/V_{OUT}	Output voltage proportional to input signal frequency.
16	20	CP-	Negative input to charge pump.

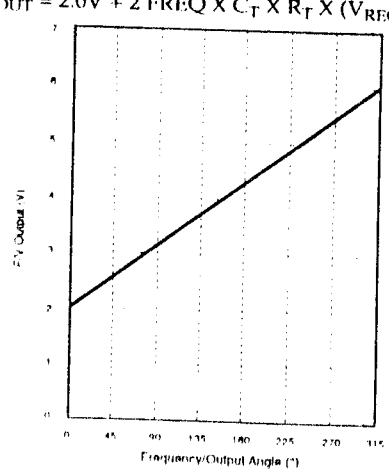
Typical Performance Characteristics

Function Generator Output Voltage vs Degrees of Deflection



Charge Pump Output Voltage vs Output Angle

$F/V_{OUT} = 2.0V + 2\ FREQ \times C_T \times R_T \times (V_{REG} - 0.7)$



Typical Performance Characteristics continued

Figure 4: Output Angle in Polar Form

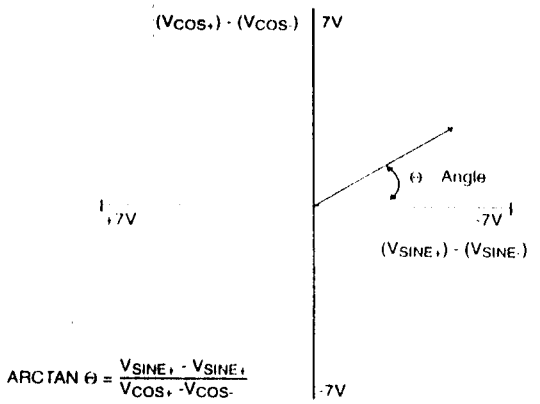
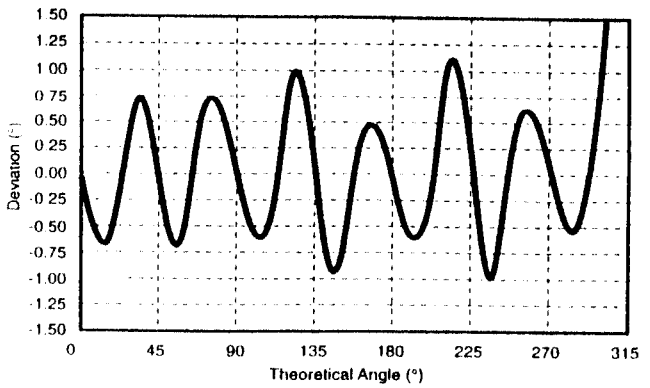
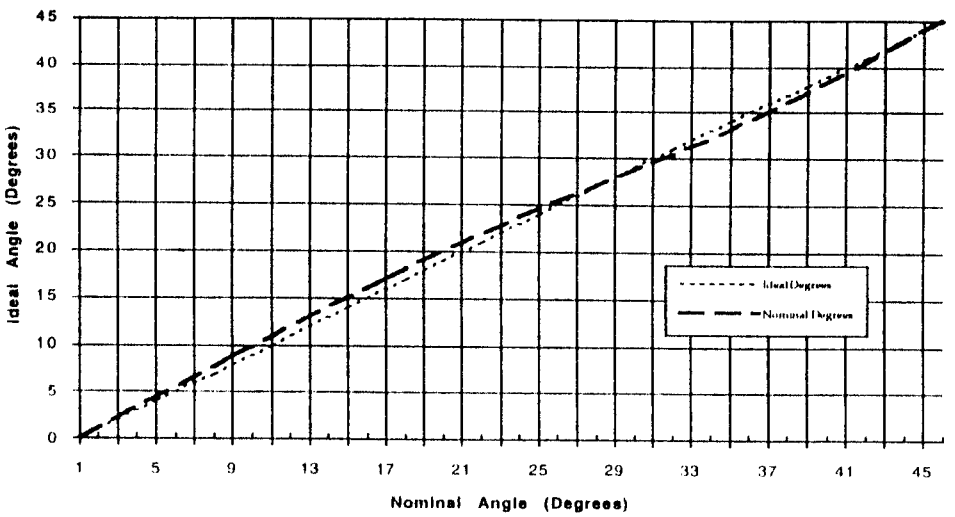


Figure 5: Nominal Output Deviation



Nominal Angle vs. Ideal Angle (After calibrating at 180°)



able 1: Nominal Angle vs. Ideal Angle (After calibrating at 270°)

Ideal Θ Degrees	Nominal Θ Degrees	Ideal Θ Degrees	Nominal Θ Degrees	Ideal Θ Degrees	Nominal Θ Degrees	Ideal Θ Degrees	Nominal Θ Degrees	Ideal Θ Degrees	Nominal Θ Degrees	Ideal Θ Degrees	Nominal Θ Degrees
0	0	17	17.98	34	33.04	75	74.00	160	159.14	245	244.63
1	1.09	18	18.96	35	34.00	80	79.16	165	164.00	250	249.14
2	2.19	19	19.92	36	35.00	85	84.53	170	169.16	255	254.00
3	3.29	20	20.86	37	36.04	90	90.00	175	174.33	260	259.16
4	4.38	21	21.79	38	37.11	95	95.47	180	180.00	265	264.53
5	5.47	22	22.71	39	38.21	100	100.84	185	185.47	270	270.00
6	6.56	23	23.61	40	39.32	105	106.00	190	190.84	275	275.47
7	7.64	24	24.50	41	40.45	110	110.86	195	196.00	280	280.84
8	8.72	25	25.37	42	41.59	115	115.37	200	200.86	285	286.00
9	9.78	26	26.23	43	42.73	120	119.56	205	205.37	290	290.86
10	10.84	27	27.07	44	43.88	125	124.00	210	209.56	295	295.37
11	11.90	28	27.79	45	45.00	130	129.32	215	214.00	300	299.21
12	12.94	29	28.73	50	50.68	135	135.00	220	219.32	305	303.02
13	13.97	30	29.56	55	56.00	140	140.68	225	225.00		
14	14.99	31	30.39	60	60.44	145	146.00	230	230.58		
15	16.00	32	31.24	65	64.63	150	150.44	235	236.00		
16	17.00	33	32.12	70	69.14	155	154.63	240	240.44		

Circuit Description

Block Diagram Description

The CS-8190 is specifically designed for use with air-core meter movements. The IC includes an input comparator for sensing input frequency such as vehicle speed or engine RPM, a charge pump for frequency to voltage conversion, a bandgap voltage regulator for stable operation, and a function generator with sine and cosine amplifiers which differentially drive the motor coils.

Input Comparator and Charge Pump

The frequency input is a high impedance comparator with a typical positive input threshold of 2.0V and typical negative threshold of 1.5V. Small signals, possibly from the reluctance coil, can be directly input to the device, eliminating the need for external buffer circuitry.

The charge pump uses the output of the comparator for frequency to voltage conversion. The charge pump output voltage, F/V_{OUT}, ranges from 2V with no input (Θ = 0°)to 6.3V at (Θ = 305°). The charge accumulated on C_T is mirrored to C_{OUT} by the Norton Amplifier. An internal full wave current rectifier doubles the input frequency, and halves the output voltage ripple. Due to IC and external component tolerance, each module will require trimming of R_T.

The circuit shown in Figure 1 averages a relatively fixed amount of charge over a period of time that is determined by the frequency of the buffered input signal. The average current is converted to an output voltage that is equal to

$$V_{OUT} = I_{AVE} \times R_T + 2.0V$$

The resistors R3 and R4 determine the rate of the C_T capacitor charge and discharge. The capacitor C4 is used to average the input current pulses shown above. R_T sets the gain of the closed loop system.

The input of the Norton amplifier Q1, mirrors the positive input current pulses through Q2 and through the feedback network R_{TOT} and C4. Likewise Q3 pulls the negative going pulses through the same network.

Derivation of the F to V Converter

The derivation can be simplified by making the following assumptions and approximations:

$V_{SQUARE(SAT)} \approx 0V$

$V_{CL} = 0.25V - V_{BE3}$

$\tau_N = C_T R_4; \tau_N = C_T(R_3 + R_4) = C_T R_{TOT}$

$PW > 10\tau_N; T - PW > 10\tau_P$

$V_{CT}(t) = V_F + (V_I - V_F)e^{t/\tau}$

$R_{TOT} = R_3 + R_4$

For the positive going pulse:

$$V_F = V_{REG} - V_D$$
$$V_I = -V_{CL}$$
$$I_{CT}(t) = \frac{V_F - V_C(t)}{R_{TOT}}$$

therefore:

$$I_{AVE(P)} = \frac{1}{T}\int_0^T \left(\frac{V_F - V_C(t)}{R_{TOT}}\right) dt$$
$$= \frac{1}{TR_{TOT}} \left[R_{TOT} C_T (V_I - V_F) e^{t/R_{TOT}C_T}\right]_0^T$$

but $e^{-T}/R_{TOT}C_T = 0$

$$I_{AVE(P)} = \frac{(V_F - V_I)}{T} C_T$$
$$= \frac{(V_{REG} - V_D + V_{CL})}{T} C_T$$

for the negative going pulse:

$$V_F = -V_{CL}$$
$$V_I = V_{REG} - V_D$$
$$I_{AVE(N)} = \frac{(V_F - V_I)}{T} C_T$$
$$= \frac{(-V_{CL} - V_{REG} + V_D) C_T}{T}$$
$$= \frac{(V_{REG} + V_{CL} - V_D)}{T} C_T$$
$$I_{RT(N)} = -I_{AVE(N)}$$

average current for the circuit:

$$I_{AVE(TOTAL)} = I_{AVE(P)} + I_{RT(N)}$$
$$= \frac{C_T}{T}(V_{REG} - V_D + V_{CL} + V_{REG} + V_{CL} - V_D)$$
$$\frac{C_T}{T}(2V_{REG} - 2V_D + 2V_{CL})$$
$$\frac{2C_T}{T}(V_{REG} - V_D + V_{CL})$$
$$I_{AVE}(T) = 2fC_T(V_{REG} - V_D + V_{CL})$$

F to V Output Voltage:

$$V = 2fC_T R_T (V_{REG} - V_D + V_{CL}) + 2.0V$$

F to V Output Ripple Voltage:

$$Q_{C16} = Q_{DSCG6}$$

$$0.5C_T (V_{REG} - V_D + V_{CL}) = C_4 \Delta V$$
$$\Delta V = \frac{C_T (V_{REG} - V_D + V_{CL})}{2C_4}$$

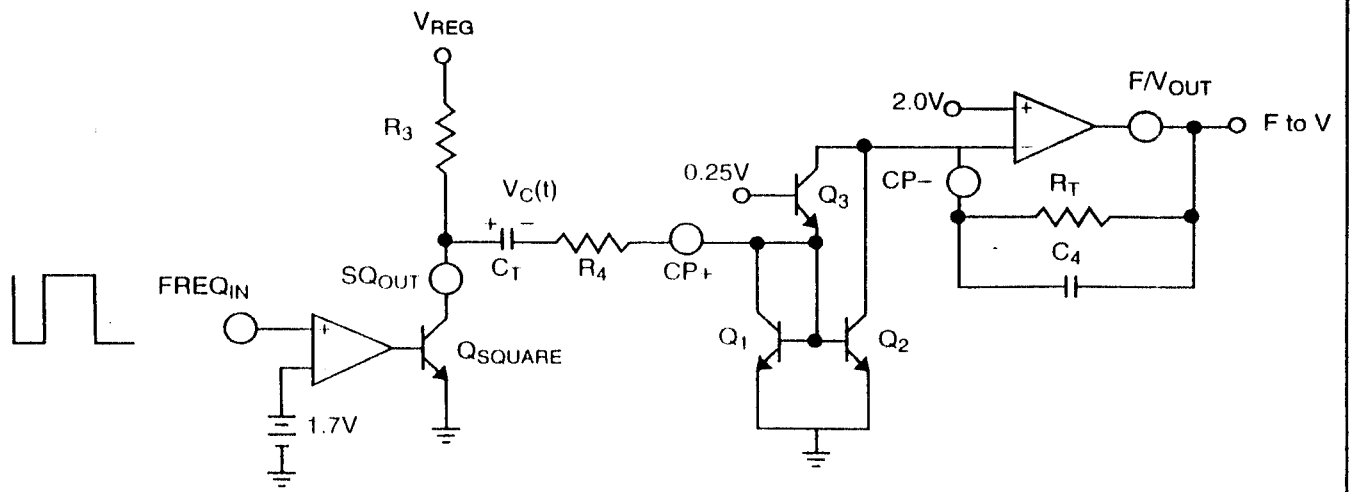


Figure 1A: Partial Schematic of Input and Charge Pump

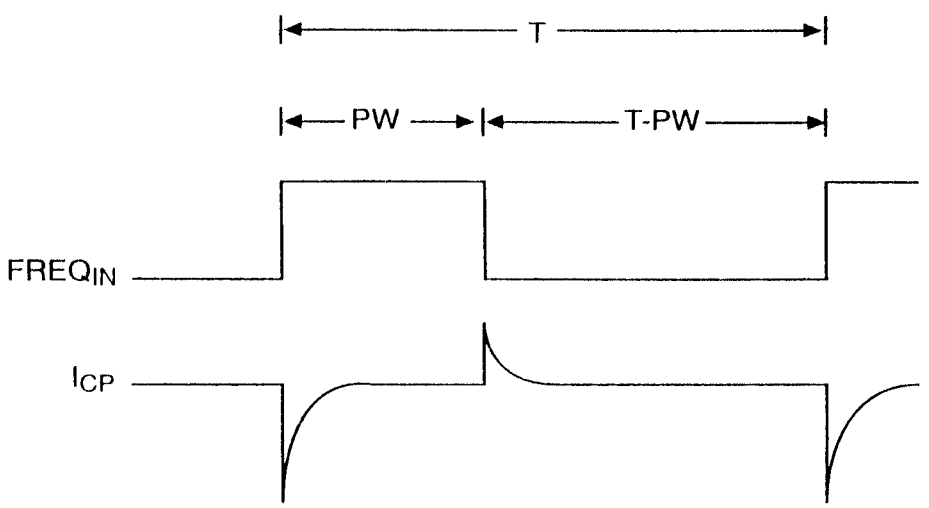


Figure 1B: Timing Diagram of $FREQ_{IN}$ and I_{CP}

Return to Zero

The IC has on board circuitry, which when taken advantage of, will return the pointer to zero when power is removed. A large external capacitor (C4) is required to take advantage of this feature. The value must be approximately 2000µF. A lower value may be used, depending upon the full scale deflection of the needle, and the mechanical characteristics of the gauge. On the IC there are two undervoltage detectors which control the position of the pointer on the dial when power is removed. As the supply is decaying, the first detector suppresses the input signal, which starts the needle moving counterclockwise, the second detector forces zero volts across the sine coil, and the maximum allowable positive voltage across the cosine coil.

Function Generator: Sine and Cosine Generators

The output waveforms of the sine and cosine amplifiers are derived from on-chip amplifier and function generator circuitry. The various trip points for the circuit (i.e., 0°, 90°, 180°, 270°) are determined by an internal resistor divider, and the bandgap voltage reference. The coils are differentially driven, allowing bidirectional current flow in the outputs, thus attaining 305° meter movements. Differentially driving the coils offers faster response time, higher current capability, higher output voltage swings, and reduced external component count. The key advantage is a higher torque output for the pointer.

Speedometer/Odometer or Tachometer Application

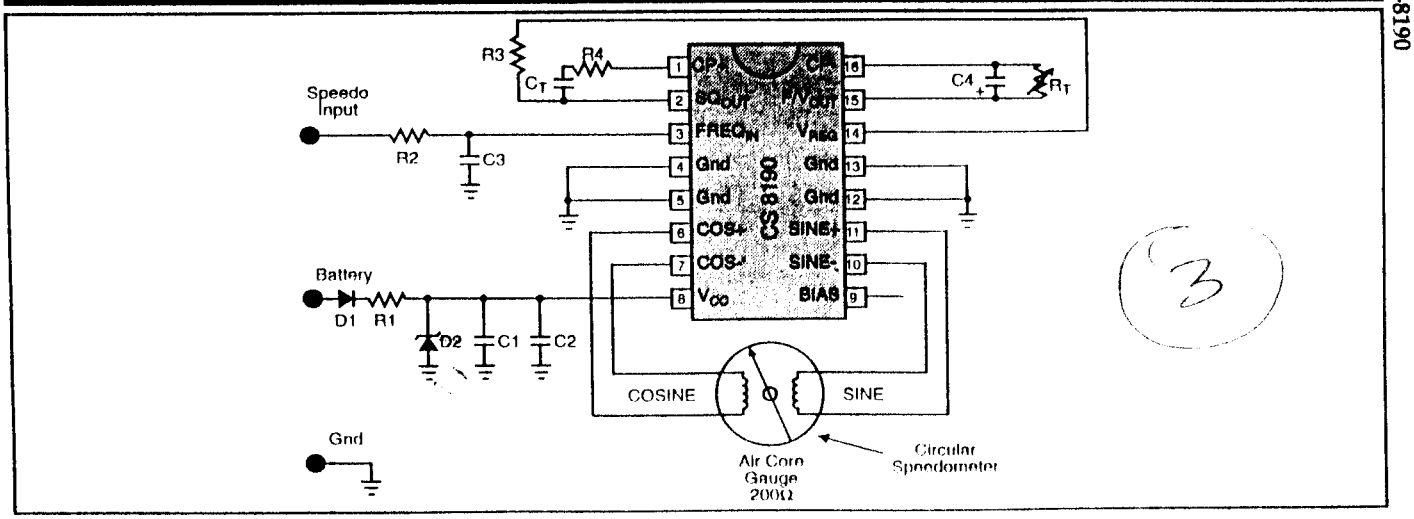


Figure 2:

R1 - 3.9, 500mW
R2 - 10kΩ
R3 - 3kΩ
R4 - 1kΩ
R_T - Trim Resistor +/- 20 PPM/DEG. C
C1 - 0.1μF
C2 - 1. Stand alone Speedo or Tach "0" μF
2. Stand alone Speedo or Tach with return to Zero, 2000μF
3. With CS-8441 application, 10μF
C3 - 0.1μF
C4 - 0.47μF
C_T - 0.0033μF, +/- 30 PPM/°C
D1 - 1A, 600 PIV
D2 - 50V, 500mW Zener
Note 1: For 58% Speed Input $T_{MAX} \leq 5/f_{MAX}$ where
$T_{MAX} = C_T(R_3+R_4)$
f_{MAX} = maximum speed input frequency

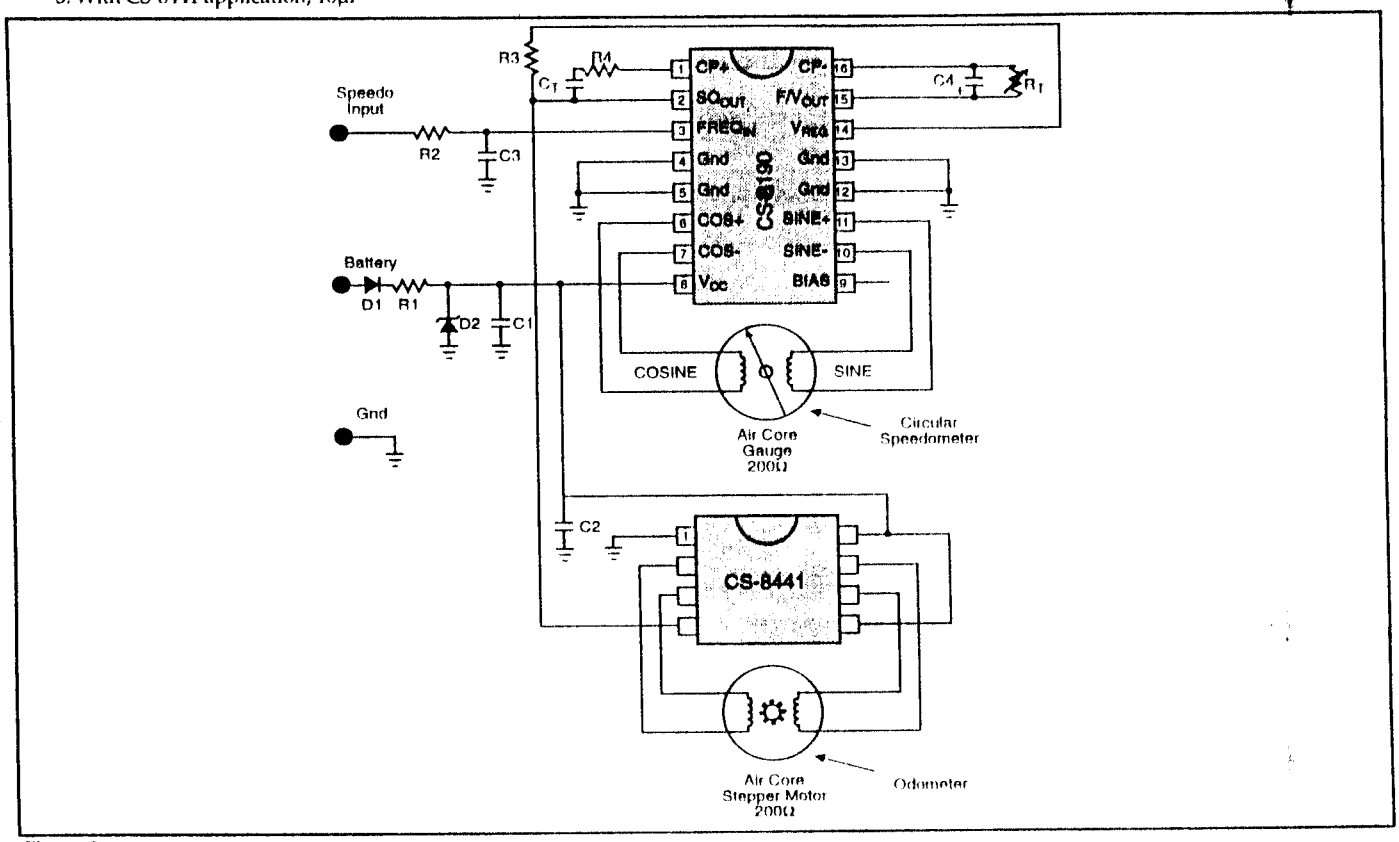


Figure 3:

Note 1: The product of C4 and R4 have a direct effect on gain and therefore directly effect temperature compensation
Note 2: C4 Range; 20pF to .2μF
Note 3: R4 Range; 100kΩ to 500kΩ
Note 4: The IC must be protected from transients above 60V and reverse battery conditions
Note 5: Additional filtering on $FREQ_{IN}$ pin may be required

Package Specification

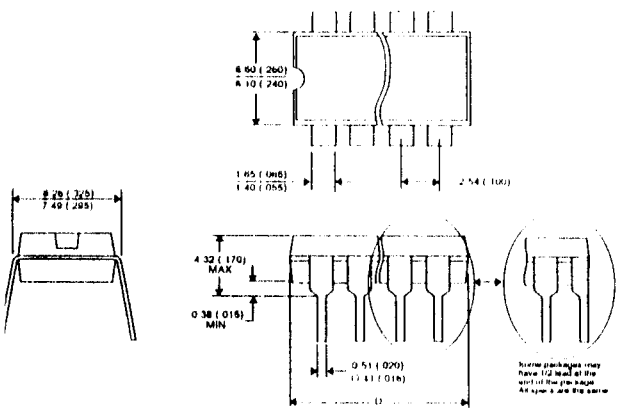
PACKAGE DIMENSIONS IN mm (INCHES)

ad Count	D			
	Metric		English	
	Max	Min	Max	Min
16	19.18	18.92	.755	.745
20	12.95	12.70	.510	.500

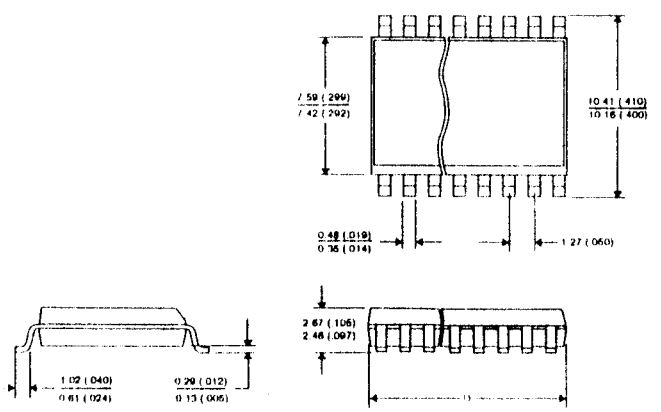
PACKAGE THERMAL DATA

Thermal Data		16L PDIP	20L SOIC	
$R\Theta_{JC}$	typ	15	9	°C/W
$R\Theta_{JA}$	typ	50	55	°C/W

16L PDIP



20L SO Wide Batwing



Ordering Information

Part Number	Description
CS-8190N16	16L PDIP
CS-8190DW20	20L SO Wide Batwing

Cherry Semiconductor Corporation
2000 South County Trail
East Greenwich, Rhode Island 02818-1530
Tel: (401)885-3600 Fax (401)885-5786
Telex WUI 6817157

2/14/93

LM158A/LM358A, LM2904

National Semiconductor

Operational Amplifiers/Buffers

LM158/LM258/LM358, LM158A/LM258A/LM358A, LM2904 Low Power Dual Operational Amplifiers

General Description

The LM158 series consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM158 series can be directly operated off of the standard +5 V_{DC} power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15 V_{DC} power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

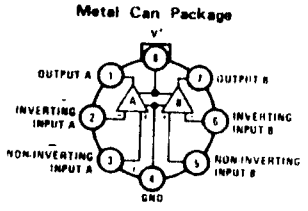
- Eliminates need for dual supplies
- Two internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation
- Pin-out same as LM1558/LM1458 dual operational amplifier

Features

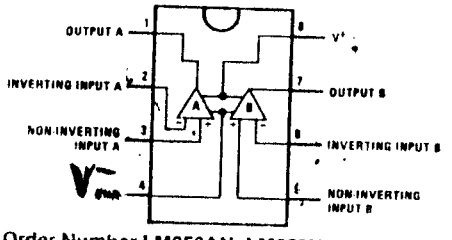
- Internally frequency compensated for unity gain
- Large dc voltage gain — 100 dB
- Wide bandwidth (unity gain) (temperature compensated) — 1 MHz
- Wide power supply range:
  - Single supply — 3 V_{DC} to 30 V_{DC}
  - or dual supplies — ±1.5 V_{DC} to ±15 V_{DC}
- Very low supply current drain (500μA) – essentially independent of supply voltage (1 mW/op amp at +5 V_{DC})
- Low input biasing current (temperature compensated) — 45 nA_{DC}
- Low input offset voltage — 2 mV_{DC}
- and offset current — 5 nA_{DC}
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing — 0 V_{DC} to V^+ − 1.5 V_{DC}

Connection Diagrams (Top Views)

Metal Can Package

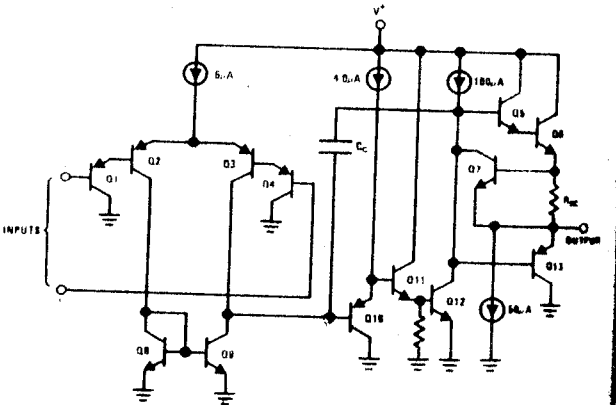


Order Number LM158AH, LM158H, LM258AH, LM258H, LM358AH or LM358H
See NS Package H08C



Order Number LM358AN, LM358N or LM2904N
See NS Package N08B

Schematic Diagram (Each Amplifier)



	LM158/LM258/LM358 LM158A/LM258A/LM358A	LM2904
Supply Voltage, V^+	32 V_{DC} or ±16 V_{DC}	26 V_{DC} or ±13 V_{DC}
Differential Input Voltage	32 V_{DC}	26 V_{DC}
Input Voltage	−0.3 V_{DC} to +32 V_{DC}	−0.3 V_{DC} to +26 V_{DC}
Power Dissipation (Note 1)		
Molded DIP (LM358N)	570 mW	570 mW
Metal Can (LM158H/LM258H/LM358H)	830 mW	
Output Short-Circuit to GND (One Amplifier) (Note 2)	Continuous	Continuous
$V^+ \leq 15$ V_{DC} and $T_A = 25°C$		
Input Current ($V_{IN} < -0.3$ V_{DC}) (Note 3)	50 mA	50 mA
Operating Temperature Range		
LM358	0°C to +70°C	−40°C to +85°C
LM258	−25°C to +85°C	
LM158	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

Electrical Characteristics ($V^+ = +5.0$ V_{DC}, Note 4)

PARAMETER	CONDITIONS	LM158A			LM258A			LM358A			LM158/LM258			LM358			LM2904			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, (Note 5)		1	2		1	3		2	3		±2	±5		±2	±7		±2	±7	mV_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25°C$, (Note 6)		20	50		40	80		45	100		45	150		45	250		45	250	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $T_A = 25°C$		2	10		2	15		5	30		±3	±30		±5	±50		±5	±50	nA_{DC}
Input Common-Mode Voltage Range	$V^+ = 30$ V_{DC}, $T_A = 25°C$ (Note 7)	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V_{DC}
Supply Current	$R_L = \infty$, $V_{CC} = 30V$ (LM2904 $V_{CC} = 26V$)		1	2		1	2		1	2		1	2		1	2		1	2	mA_{DC}
	$R_L = \infty$ On All Op Amps		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2	mA_{DC}
	Over Full Temperature Range																			
Large Signal Voltage Gain	$V^+ = 15$ V_{DC} (For Large V_O Swing)	50	100		50	100		25	100		50	100		25	100			100		V/mV
	$R_L \geq 2$ kΩ, $T_A = 25°C$																			
Output Voltage Swing	$R_L = 2$ kΩ, $T_A = 25°C$ (LM2904 $R_L \geq 10$ kΩ)	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V_{DC}
Common-Mode Rejection Ratio	DC, $T_A = 25°C$	70	85		70	85		65	85		70	85		65	70		50	70		dB
Power Supply Rejection Ratio	DC, $T_A = 25°C$	65	100		65	100		65	100		65	100		65	100		50	100		dB
Amplifier-to-Amplifier Coupling	f = 1 kHz to 20 kHz, $T_A = 25°C$ (Input Referred), (Note 8)		−120			−120			−120			−120			−120			−120		dB
Output Current Source	$V_{IN}^+ = 1$ V_{DC}, $V_{IN}^- = 0$ V_{DC}, $V^+ = 15$ V_{DC}, $T_A = 25°C$	20	40		20	40		20	40		20	40		20	40		20	40		mA_{DC}

Electrical Characteristics (Continued) (V^+ = +5.0 V_{DC}, Note 4)

PARAMETER	CONDITIONS	LM158A			LM258A			LM358A			LM158/LM258			LM358			LM2904			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Sink	V_{IN}^- = 1 V_{DC}, V_{IN}^+ = 0 V_{DC} V^+ = 15 V_{DC}, T_A = 25°C	10	20		10	20		10	20		10	20		10	20		10	20		mA$_{DC}$
	V_{IN}^- = 1 V_{DC}, V_{IN}^+ = 0 V_{DC} T_A = 25°C, V_O = 200 mV_{DC}	12	50		12	50		12	50		12	50		12	50					µA$_{DC}$
Short Circuit to Ground	T_A = 25°C, (Note 2)		40	60		40	60		40	60		40	60		40	60		40	60	mA$_{DC}$
Input Offset Voltage	(Note 5)			4			4			5			±7			±9			±10	mV_{DC}
Input Offset Voltage Drift	R_S = 0Ω		7	15		7	15		7	20		7			7			7		µV/°C
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			30			30			75			100			±150		45	±200	nA$_{DC}$
Input Offset Current Drift			10	200		10	200		10	300		10			10			10		pA$_{DC}$/°C
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	100		40	200		40	300		40	500		40	500	nA$_{DC}$
Input Common-Mode Voltage Range	V^+ = 30 V_{DC}, (Note 7)	0		V^+ −2	0		V^+ −2	0		V^+ −2	0		V^+ −2	0		V^+ −2	0		V^+ −2	V_{DC}
Large Signal Voltage Gain	V^+ = +15 V_{DC} (For Large V_O Swing) $R_L \geq$ 2 kΩ	25			25			15			25			15			15			V/mV
Output Voltage Swing																				
V_{OH}	V^+ = +30 V_{DC}, R_L = 2 kΩ	26			26			26			26			26			22			V_{DC}
	$R_L \geq$ 10 kΩ	27	28		27	28		27	28		27	28		27	28		23	24		V_{DC}
V_{OL}	V^+ = 5 V_{DC}, $R_L \leq$ 10 kΩ		5	20		5	20		5	20		5	20		5	20		5	100	mV_{DC}
Output Current																				
Source	V_{IN}^+ = +1 V_{DC}, V_{IN}^- = 0 V_{DC}, V^+ = 15 V_{DC}	10	20		10	20		10	20		10	20		10	20		10	20		mA$_{DC}$
Sink	V_{IN}^- = +1 V_{DC}, V_{IN}^+ = 0 V_{DC}, V^+ = 15 V_{DC}	10	15		5	8		5	8		5	8		5	8		5	8		mA$_{DC}$
Differential Input Voltage	(Note 7)			32			32			32			32			32			26	V_{DC}

Note 1: For operating at high temperatures, the LM358/LM358A, LM2904 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM258/LM258A and LM158/LM158A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15 V_{DC}, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V_{DC} (at 25°C).

Note 4: These specifications apply for V^+ = +5 V_{DC} and −55°C ≤ T_A ≤ +125°C, unless otherwise stated. With the LM258/LM258A, all temperature specifications are limited to −25°C ≤ T_A ≤ +85°C, the LM358/LM358A temperature specifications are limited to 0°C ≤ T_A ≤ +70°C, and the LM2904 specifications are limited to −40°C ≤ T_A ≤ +85°C.

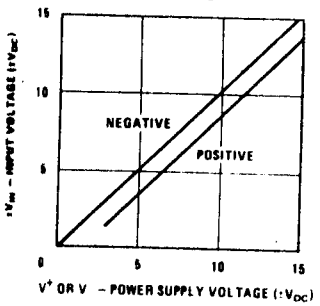
Note 5: V_O ≅ 1.4 V_{DC}, R_S = 0Ω with V^+ from 5 V_{DC} to 30 V_{DC}; and over the full input common-mode range (0 V_{DC} to V^+ − 1.5 V_{DC}).

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

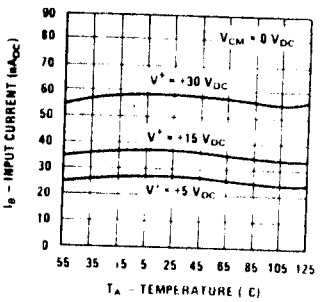
Note 7: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is V^+ −1.5V, but

Typical Performance Characteristics

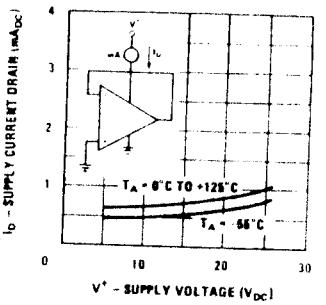
Input Voltage Range



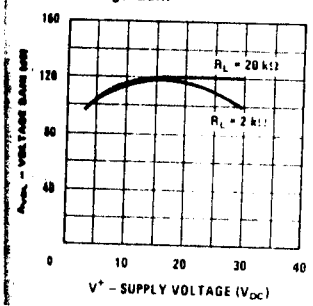
Input Current



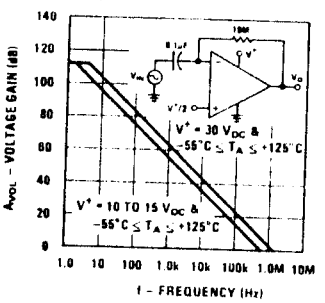
Supply Current



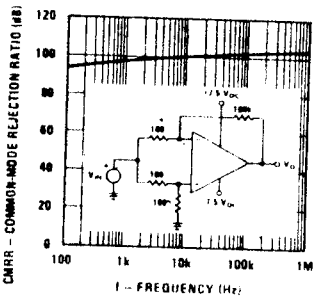
Voltage Gain



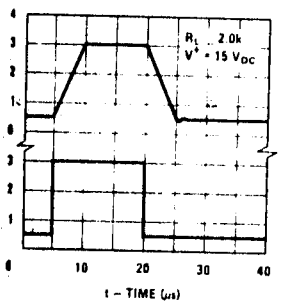
Open Loop Frequency Response



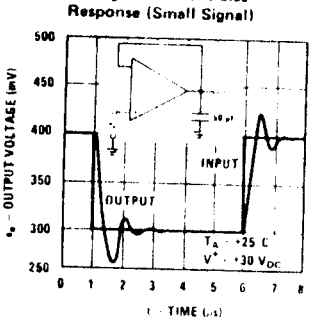
Common Mode Rejection Ratio



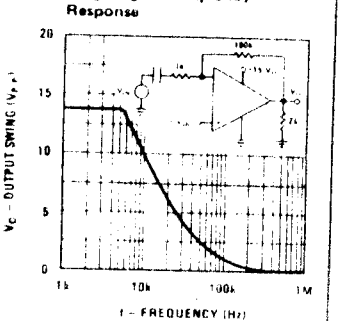
Voltage Follower Pulse Response



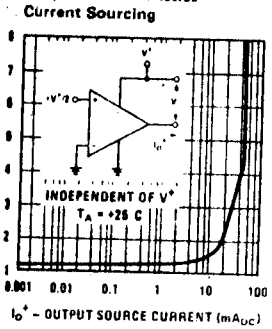
Voltage Follower Pulse Response (Small Signal)



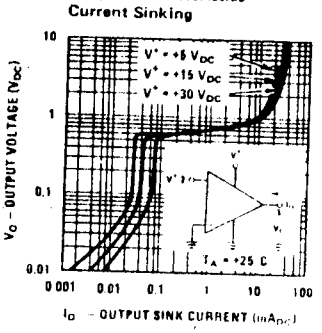
Large Signal Frequency Response



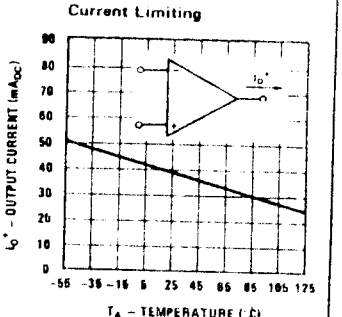
Output Characteristics Current Sourcing



Output Characteristics Current Sinking

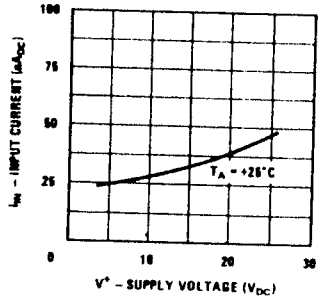


Current Limiting

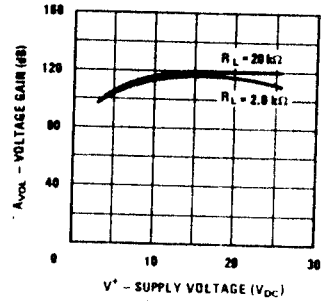


Typical Performance Characteristics (Continued) (LM2902 only)

Input Current



Voltage Gain



Application Hints

The LM158 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

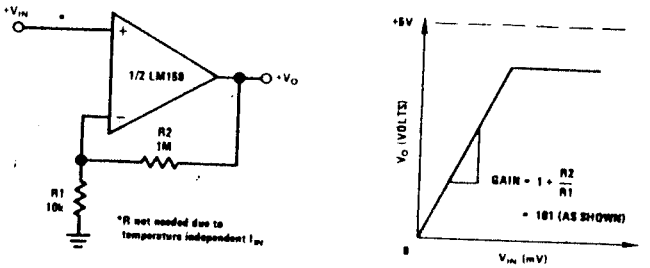
The bias network of the LM158 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

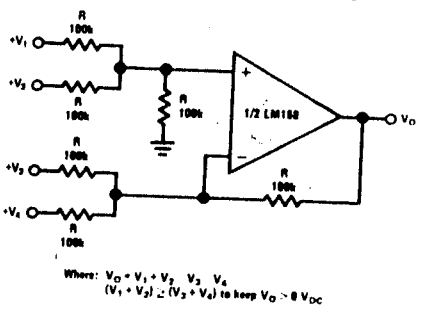
The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

Non-Inverting DC Gain (0V Input = 0V Output)

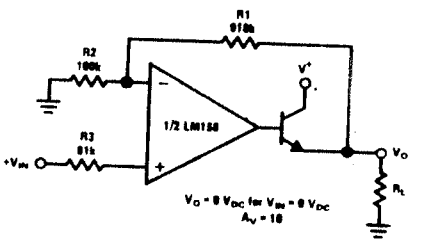


DC Summing Amplifier
(V_{IN}'S $\geq$ 0 V_{DC} AND $V_O \geq$ 0 V_{DC})

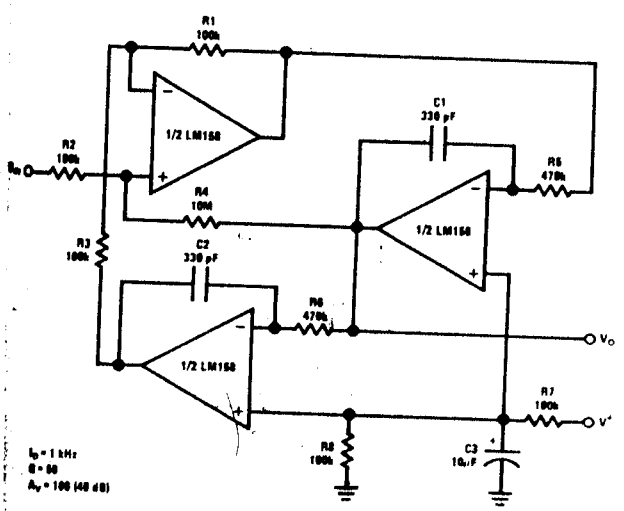


Where: $V_O = V_1 + V_2 \quad V_3 \quad V_4$
$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0\ V_{DC}$

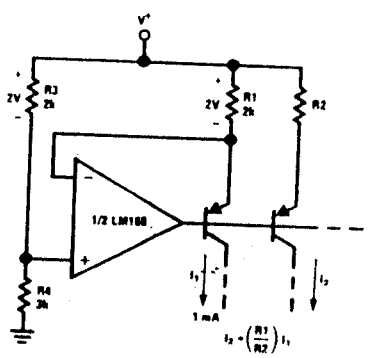
Power Amplifier



"BI-QUAD" RC Active Bandpass Filter

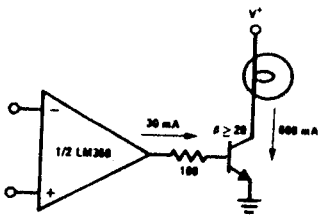


Fixed Current Sources

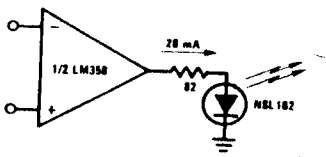


Typical Single-Supply Applications (Continued) ($V^+ = 5.0\ V_{DC}$)

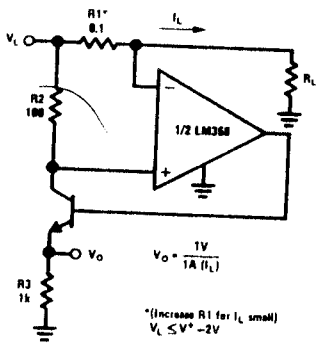
Lamp Driver



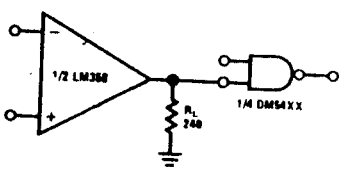
LED Driver



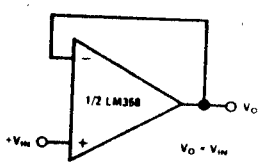
Current Monitor



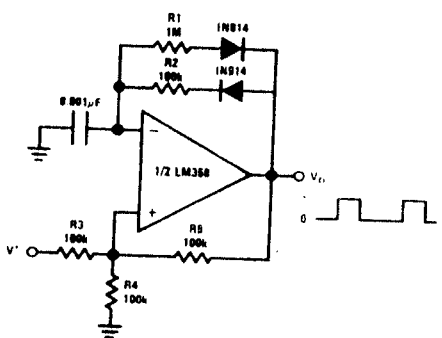
Driving TTL



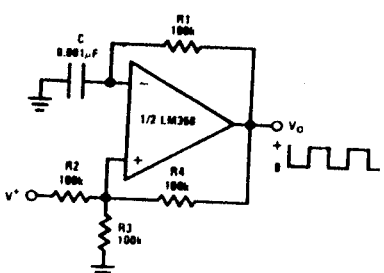
Voltage Follower



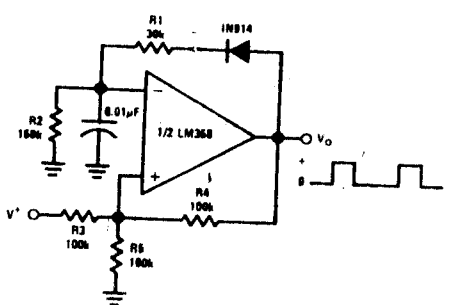
Pulse Generator



Squarewave Oscillator

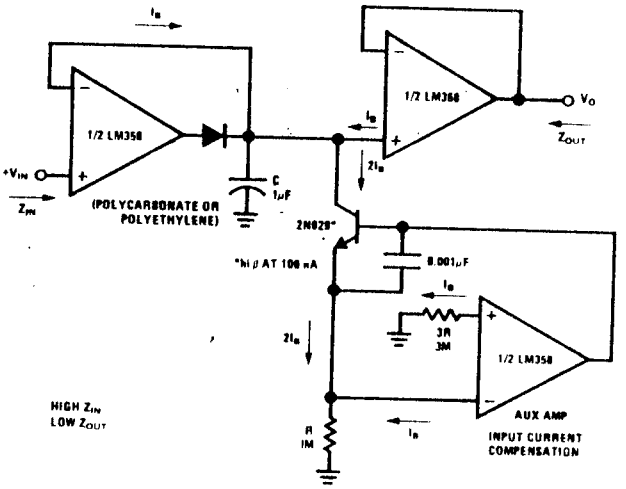


Pulse Generator

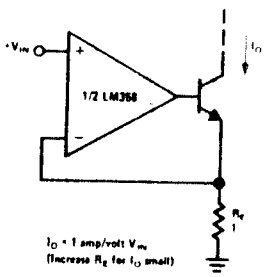


Typical Single-Supply Applications (Continued) (V^+ = 5.0 V_{DC})

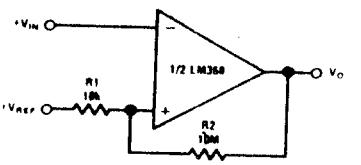
Low Drift Peak Detector



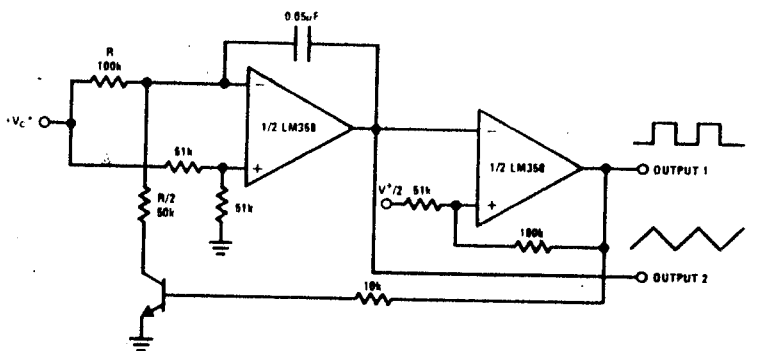
High Compliance Current Sink



Comparator with Hysteresis

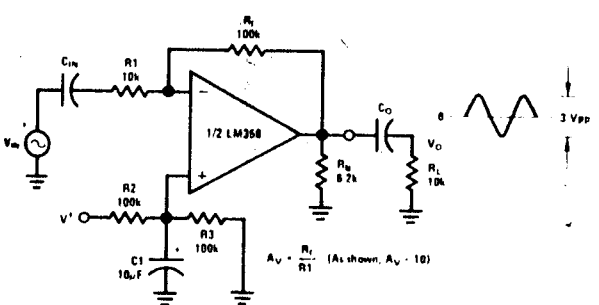


Voltage Controlled Oscillator (VCO)

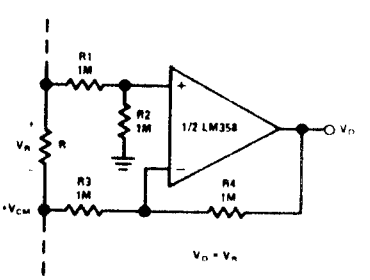


*WIDE CONTROL VOLTAGE RANGE: 0 V_{DC} ≤ V_C ≤ 2(V^+ − 1.5 V_{DC})

AC Coupled Inverting Amplifier

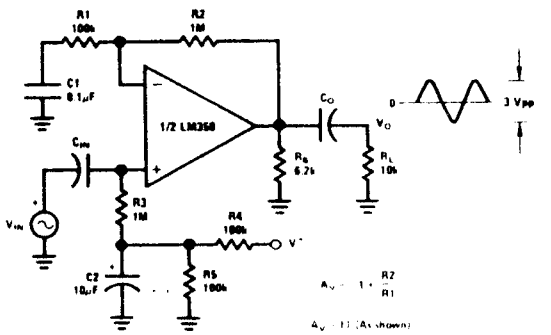


Ground Referencing A Differential Input Signal

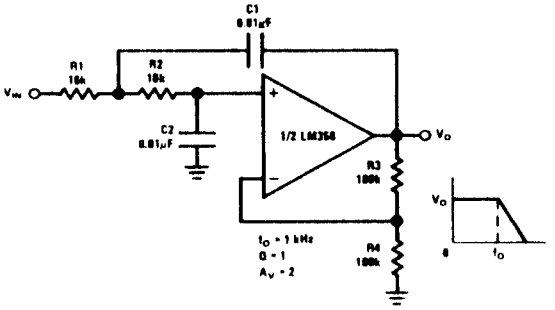


Typical Single-Supply Applications (Continued) ($V^+ = 5.0\ V_{DC}$)

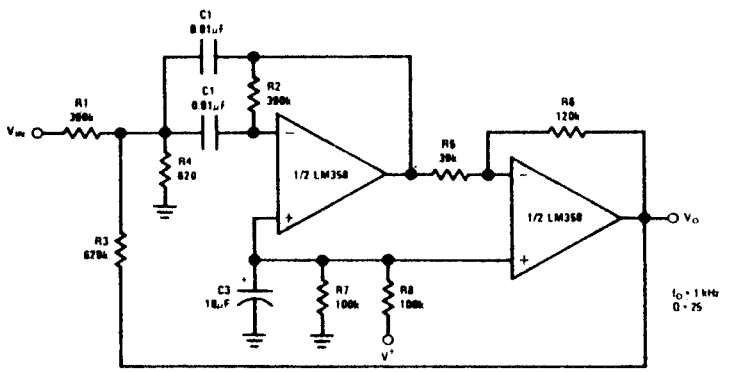
AC Coupled Non-Inverting Amplifier



DC Coupled Low-Pass RC Active Filter



Bandpass Active Filter



High Input Z, DC Differential Amplifier

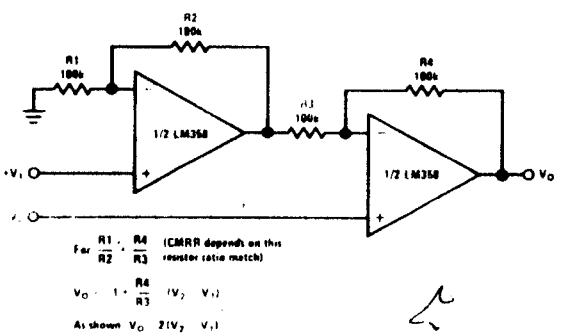
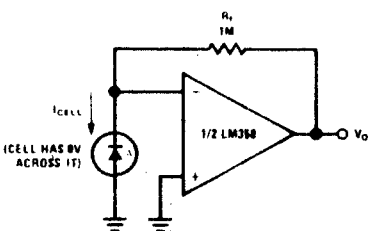
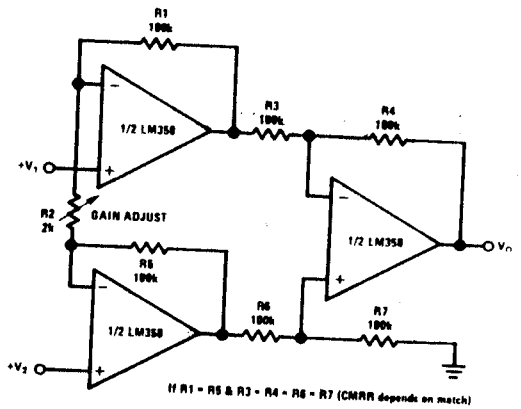


Photo Voltaic-Cell Amplifier



Typical Single-Supply Applications (Continued) ($V^+ = 5.0\ V_{DC}$)

High Input Z Adjustable-Gain DC Instrumentation Amplifier

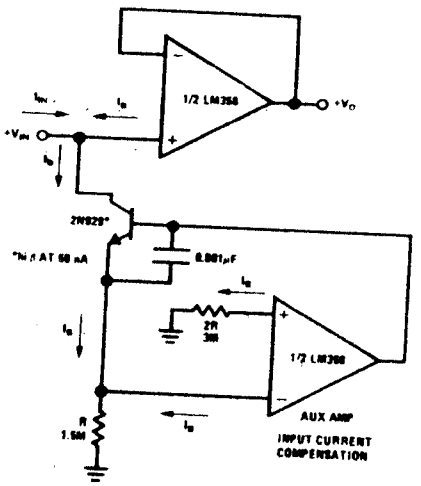


If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

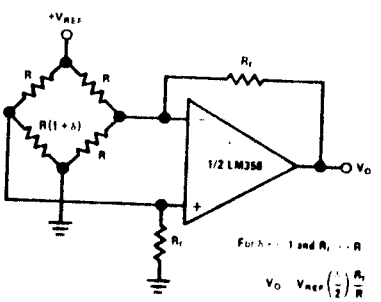
$$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$$

As shown $V_O = 101\,(V_2 - V_1)$

Using Symmetrical Amplifiers to Reduce Input Current (General Concept)



Bridge Current Amplifier



For Δ = 1 and $R_f = R$

$$V_O = V_{REF}\left(\frac{\Delta}{2}\right)\frac{R_f}{R}$$

National Semiconductor

DAC0808, DAC0807, DAC0806 8-Bit D/A Converters

General Description

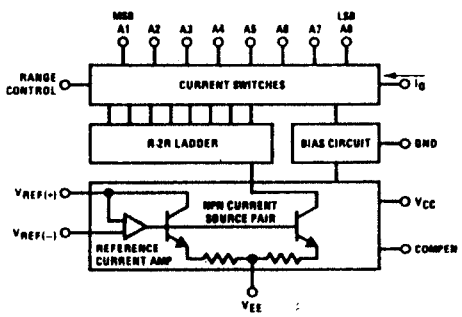
The DAC0808 series is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 I_{REF}/256. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 series are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC0808 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the MC1508/MC1408. For higher speed applications, see DAC0800 data sheet.

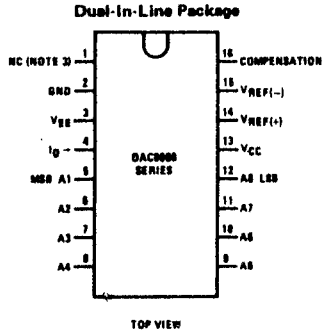
Features

- Relative accuracy: ±0.19% error maximum (DAC0808)
- Full scale current match: ±1 LSB typ
- 7 and 6-bit accuracy available (DAC0807, DAC0806)
- Fast settling time: 150 ns typ
- Noninverting digital inputs are TTL and CMOS compatible
- High speed multiplying input slew rate: 8 mA/μs
- Power supply voltage range: ±4.5V to ±18V
- Low power consumption: 33 mW @ ±5V

Block and Connection Diagrams



Dual-In-Line Package



Typical Application

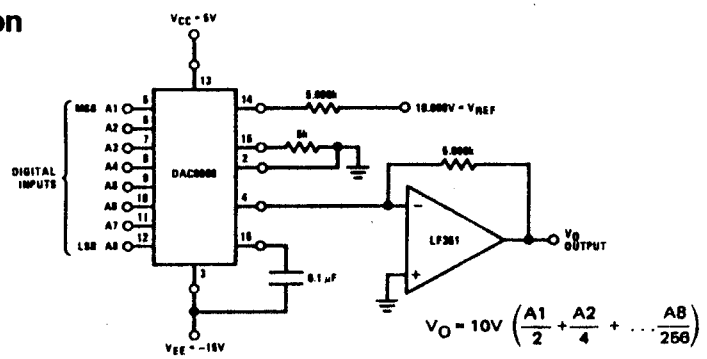


FIGURE 1. +10V Output Digital to Analog Converter

Ordering Information

ACCURACY	OPERATING TEMPERATURE RANGE	ORDER NUMBERS*					
		D PACKAGE (D16C)		J PACKAGE (J16A)		N PACKAGE (N16A)	
8-bit	$-55°C \leq T_A \leq +125°C$	DAC0808LD	MC1508L8				
8-bit	$0°C \leq T_A \leq +75°C$			DAC0808LCJ	MC1408L8	DAC0808LCN	MC1408P8
7-bit	$0°C \leq T_A \leq +75°C$			DAC0807LCJ	MC1408L7	DAC0807LCN	MC1408P7
6-bit	$0°C \leq T_A \leq +75°C$			DAC0806LCJ	MC1408L6	DAC0806LCN	MC1408P6

*Note. Devices may be ordered by using either order number.

olute Maximum Ratings

Supply Voltage	
V_{CC}	+18 V_{DC}
V_{EE}	−18 V_{DC}
Input Voltage, V5–V12	−10 V_{DC} to +18 V_{DC}
Output Voltage; V_O	−11 V_{DC} to +18 V_{DC}
Current, I_{14}	5 mA
Amplifier Inputs, V14, V15	V_{CC}, V_{EE}

Power Dissipation (Package Limitation)	1000 mW
Derate above T_A = 25°C	6.7 mW/°C
Operating Temperature Range	
DAC0808L	−55°C ≤ T_A ≤ +125°C
DAC0808LC Series	0 ≤ T_A ≤ +75°C
Storage Temperature Range	−65°C to +150°C

ctrical Characteristics

= 5V, V_{EE} = −15 V_{DC}, $V_{REF}/R14$ = 2 mA, DAC0808: T_A = −55°C to +125°C, DAC0808C, DAC0807C, 806C, T_A = 0°C to +75°C, and all digital inputs at high logic level unless otherwise noted.)

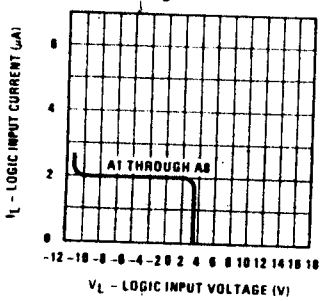
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Relative Accuracy (Error Relative to Full Scale I_O)	*(Figure 4)*				%
DAC0808L (LM1508-8), DAC0808LC (LM1408-8)				±0.19	%
DAC0807LC (LM1408-7), (Note 1)				±0.39	%
DAC0806LC (LM1408-6), (Note 1)				±0.78	%
Settling Time to Within 1/2 LSB (Includes t_{PLH})	T_A = 25°C (Note 2), *(Figure 5)*		150		ns
Propagation Delay Time	T_A = 25°C, *(Figure 5)*		30	100	ns
Output Full Scale Current Drift			±20		ppm/°C
Digital Input Logic Levels	*(Figure 3)*				
High Level, Logic "1"		2			V_{DC}
Low Level, Logic "0"				0.8	V_{DC}
Digital Input Current	*(Figure 3)*				
High Level	V_{IH} = 5V		0	0.040	mA
Low Level	V_{IL} = 0.8V		−0.003	−0.8	mA
Reference Input Bias Current	*(Figure 3)*		−1	−3	μA
Output Current Range	*(Figure 3)*				
	V_{EE} = −5V	0	2.0	2.1	mA
	V_{EE} = −15V, T_A = 25°C	0	2.0	4.2	mA
Output Current	V_{REF} = 2.000V, R14 = 1000Ω, *(Figure 3)*	1.9	1.99	2.1	mA
Output Current, All Bits Low	*(Figure 3)*		0	4	μA
Output Voltage Compliance	$E_r \leq 0.19\%$, T_A = 25°C				
Pin 1 Grounded, V_{EE} Below −10V				−0.55, +0.4	V_{DC}
				−5.0, +0.4	V_{DC}
Reference Current Slew Rate	*(Figure 6)*	4	8		mA/μs
Output Current Power Supply Sensitivity	−5V ≤ V_{EE} ≤ −16.5V		0.05	2.7	μA/V
Power Supply Current (All Bits Low)	*(Figure 3)*				
			2.3	22	mA
			−4.3	−13	mA
Power Supply Voltage Range	T_A = 25°C, *(Figure 3)*				
		4.5	5.0	5.5	V_{DC}
		−4.5	−15	−16.5	V_{DC}
Power Dissipation					
All Bits Low	V_{CC} = 5V, V_{EE} = −5V		33	170	mW
	V_{CC} = 5V, V_{EE} = −15V		108	305	mW
All Bits High	V_{CC} = 15V, V_{EE} = −5V		90		mW
	V_{CC} = 15V, V_{EE} = −15V		160		mW

1: All current switches are tested to guarantee at least 50% of rated current.
2: All bits switched.
3: Range control is not required.

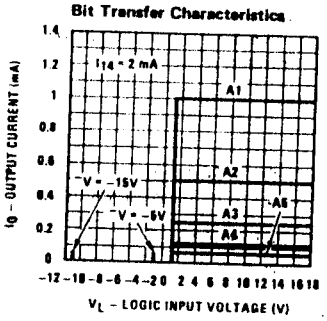
Typical Performance Characteristics

V_{CC} = 5V, V_{EE} = −15V, T_A = 25°C, unless otherwise noted

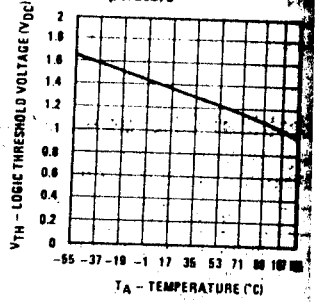
Logic Input Current vs Input Voltage



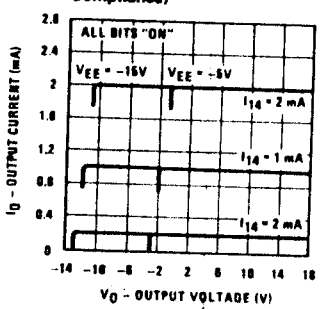
Bit Transfer Characteristics



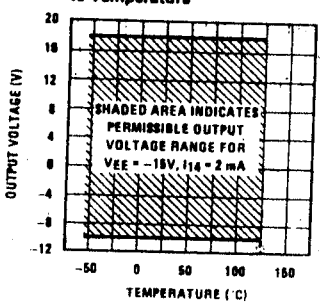
Logic Threshold Voltage vs Temperature



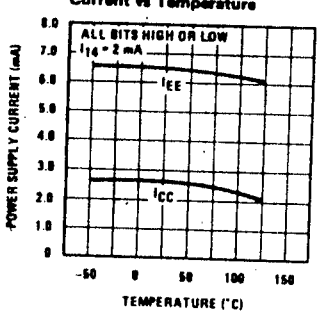
Output Current vs Output Voltage (Output Voltage Compliance)



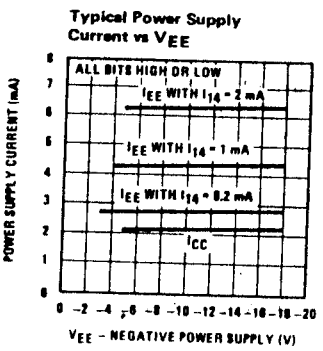
Output Voltage Compliance vs Temperature



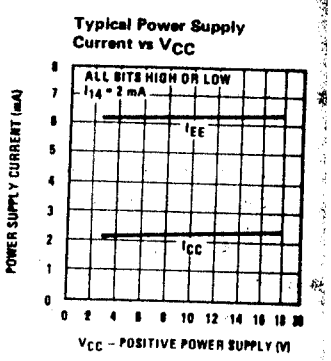
Typical Power Supply Current vs Temperature



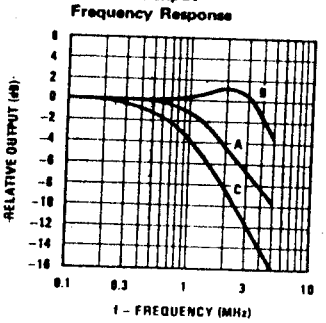
Typical Power Supply Current vs V_{EE}



Typical Power Supply Current vs V_{CC}



Reference Input Frequency Response



Unless otherwise specified: R14 = R15 = 1 kΩ, C = 15 pF, pin 16 to V_{EE}; R_L = 50Ω, pin 4 to ground.

Curve A: Large Signal Bandwidth Method of *Figure 7*, V_{REF} = 2 Vp-p offset 1 V above ground

Curve B: Small Signal Bandwidth Method of *Figure 7*, R_L = 250Ω, V_{REF} = 50 mVp-p offset 200 mV above ground.

Curve C: Large and Small Signal Bandwidth Method of *Figure 9* (no op amp, R_L = 50Ω), R_S = 50Ω, V_{REF} = 2V, V_S = 100 mVp-p centered at 0V.

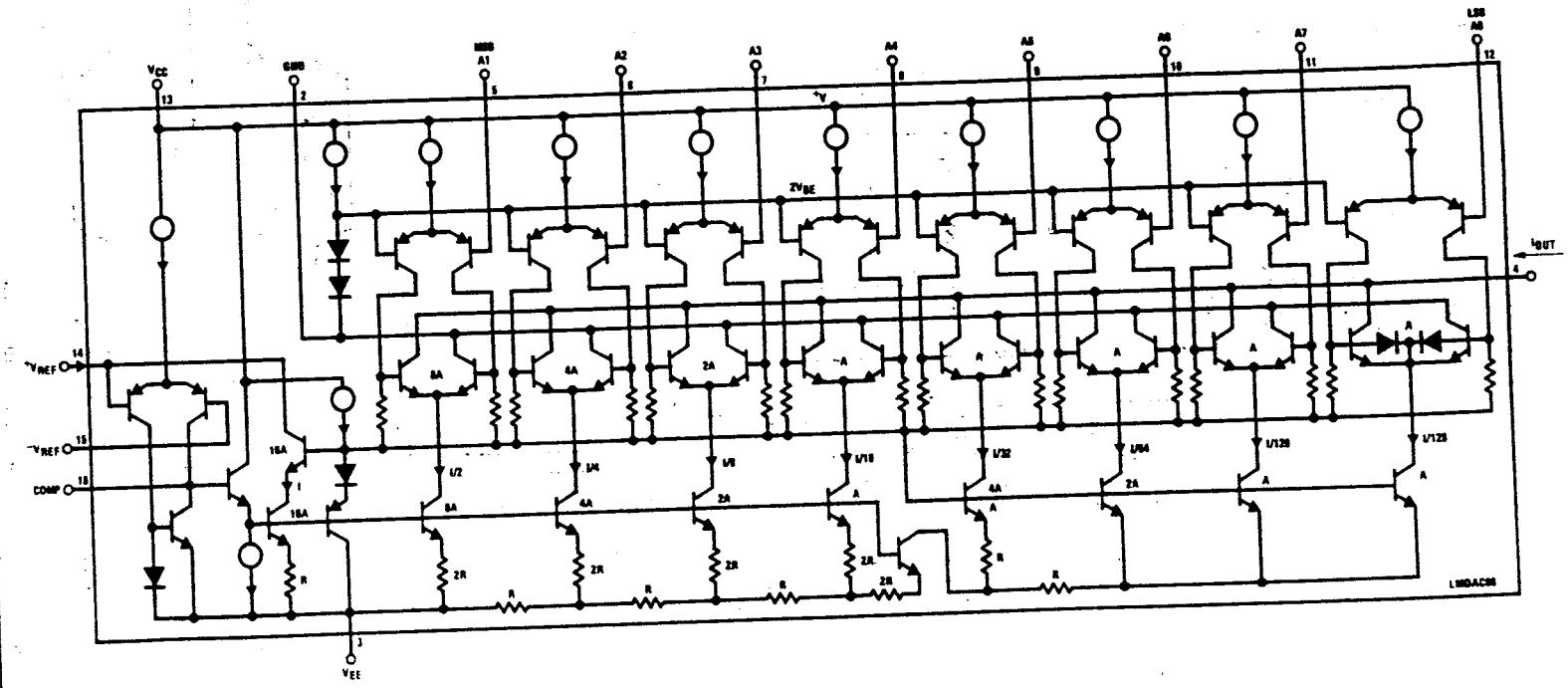
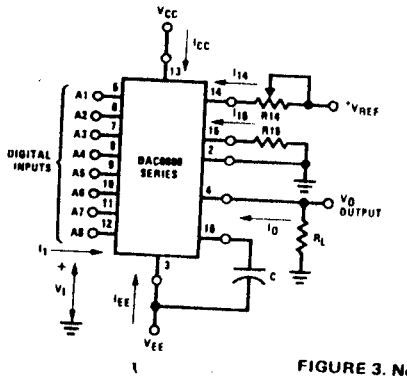


FIGURE 2. Equivalent Circuit of the DAC0808 Series

Test Circuits



V_I and I_I apply to inputs A1–A8.

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right)$$

where $K = \frac{V_{REF}}{R14}$

and A_N = "1" if A_N is at high level
A_N = "0" if A_N is at low level

FIGURE 3. Notation Definitions Test Circuit

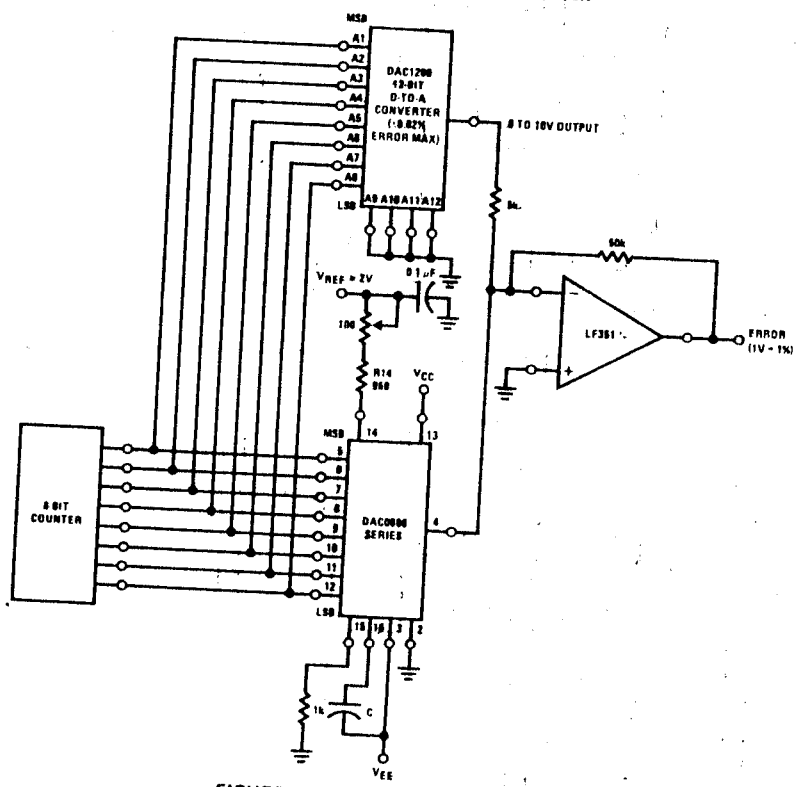


FIGURE 4. Relative Accuracy Test Circuit

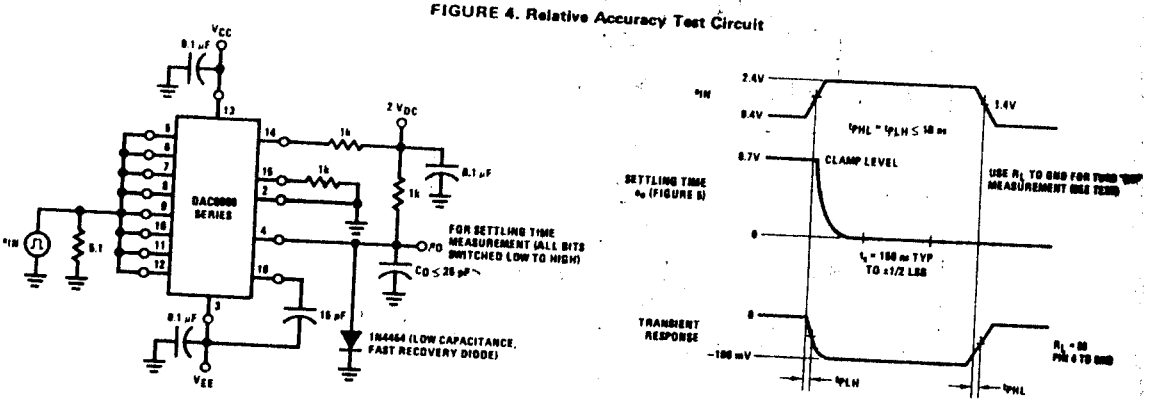


FIGURE 5. Transient Response and Settling Time

Circuits (Continued)

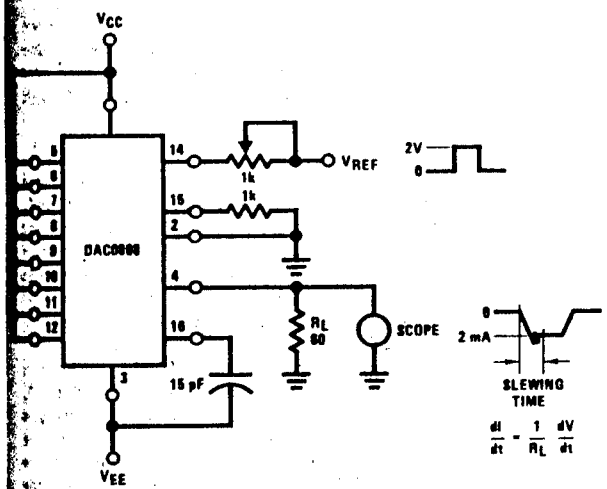


FIGURE 6. Reference Current Slew Rate Measurement

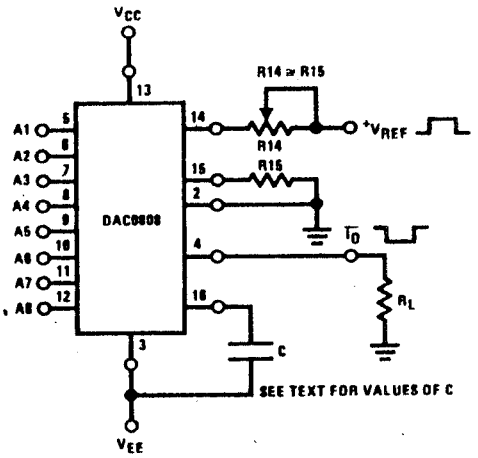


FIGURE 7. Positive V_{REF}

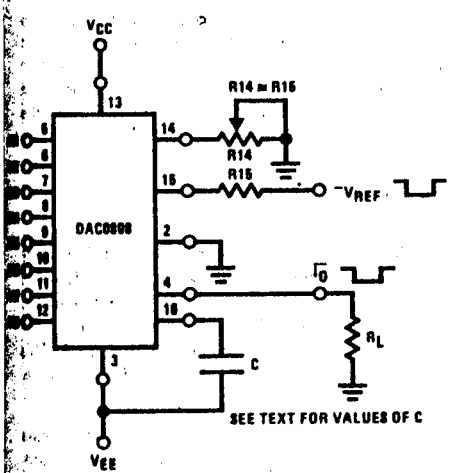


FIGURE 8. Negative V_{REF}

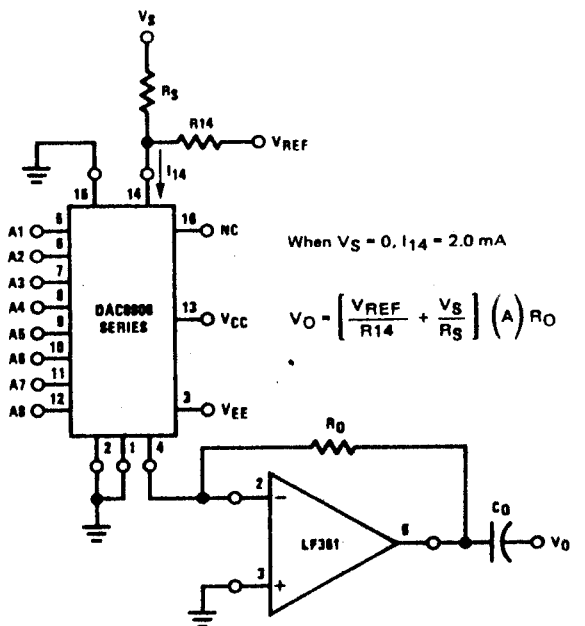


FIGURE 9. Programmable Gain Amplifier or Digital Attenuator Circuit

Application Hints

REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I_{14}, must always flow into pin 14, regardless of the set-up method or reference voltage polarity.

Connections for a positive voltage are shown in *Figure 7*. The reference voltage source supplies the full current I_{14}. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1, 2.5 and 5 kΩ, minimum capacitor values are 15, 37 and 75 pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

Application Hints (Continued)

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in *Figure 8*. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 4V above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to 5V through another resistor and bypassing the junction of the 2 resistors with 0.1 μF to ground. For reference voltages greater than 5V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

OUTPUT VOLTAGE RANGE

The voltage on pin 4 is restricted to a range of −0.6 to 0.5V when V_{EE} = −5V due to the current switching methods employed in the DAC0808.

The negative output voltage compliance of the DAC0808 is extended to −5V where the negative supply voltage is more negative than −10V. Using a full-scale current of 1.992 mA and load resistor of 2.5 kΩ between pin 4 and ground will yield a voltage output of 256 levels between 0 and −4.980V. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500Ω do not significantly affect performance, but a 2.5 kΩ load increases worst-case settling time to 1.2 μs (when all bits are switched ON). Refer to the subsequent text section on Settling Time for more details on output loading.

OUTPUT CURRENT RANGE

The output current maximum rating of 4.2 mA may be used only for negative supply voltages more negative than −7V, due to the increased voltage drop across the resistors in the reference current amplifier.

ACCURACY

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current. The relative accuracy of the DAC0808 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in absolute accuracy of output current. However, the DAC0808 has a very low full-scale current drift with temperature.

The DAC0808 series is guaranteed accurate to within ±1/2 LSB at a full-scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2 mA, with the loss of 1 LSB (8 μA) which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in *Figure 4*. The 12-bit converter is calibrated for a full-scale output current of 1.992 mA. This is an optional step since the DAC0808 accuracy is essentially the same between 1.5 and 2.5 mA. Then the DAC0808 circuits' full-scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accuracy D-to-A converter. 16-bit accuracy implies a total error of ±1/2 of one part in 65,536, or ±0.00076%, which is much more accurate than the ±0.019% specification provided by the DAC0808.

MULTIPLYING ACCURACY

The DAC0808 may be used in the multiplying mode with 8-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from 16 μA to 4 mA, the additional error contributions are less than 1.6 μA. This is well within 8-bit accuracy when referred to full-scale.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the DAC0808 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a DC reference current is 0.5 to 4 mA.

SETTLING TIME

The worst-case switching condition occurs when all bits are switched ON, which corresponds to a low-to-high transition for all bits. This time is typically 150 ns for settling to within ±1/2 LSB, for 8-bit accuracy, and 100 ns to 1/2 LSB for 7 and 6-bit accuracy. The turn OFF is typically under 100 ns. These times apply when $R_L \leq 500\Omega$ and $C_O \leq 25$ pF.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactoy test results when measuring settling time. Short leads, 100 μF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

National Semiconductor

ADC0808, ADC0809 8-Bit μP Compatible A/D Converters With 8-Channel Multiplexer

General Description

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

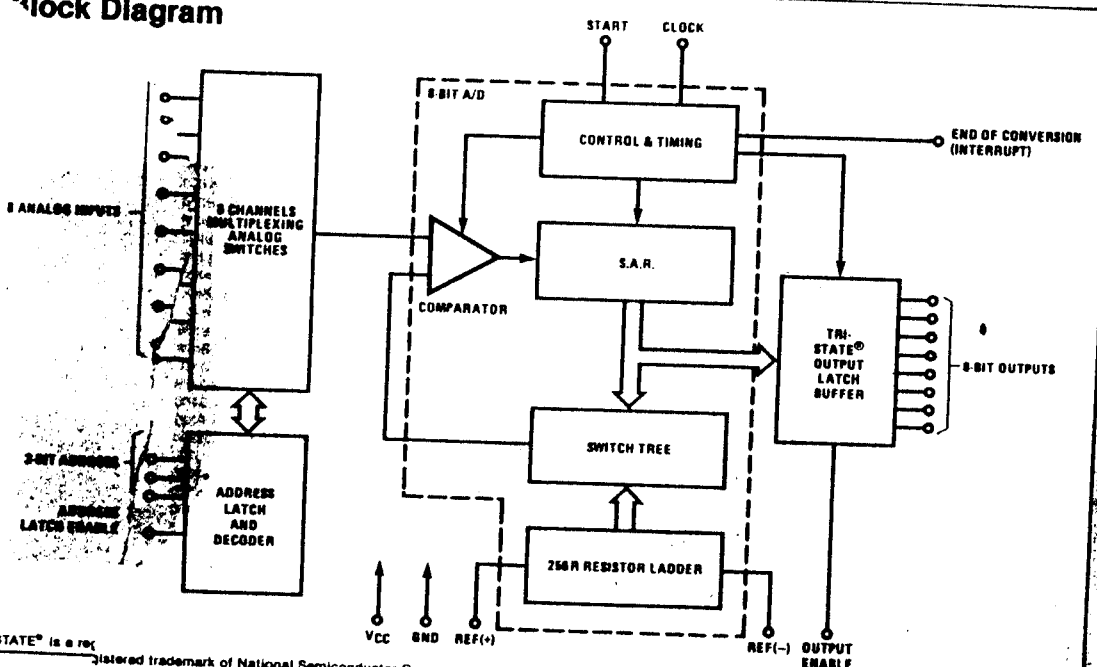
The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet. (See AN-247 for more information.

Features

- Resolution — 8-bits
- Total unadjusted error — ±1/2 LSB and ±1 LSB
- No missing codes
- Conversion time — 100 μs
- Single supply — 5 V_{DC}
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- 8-channel multiplexer with latched control logic
- Easy interface to all microprocessors, or operates "stand alone"
- Outputs meet T^2L voltage level specifications
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Standard hermetic or molded 28-pin DIP package
- Temperature range −40°C to +85°C or −55°C to +125°C
- Low power consumption — 15 mW
- Latched TRI-STATE® output

Block Diagram



TRI-STATE® is a re[gistered trademark of National Semiconductor Corp.

olute Maximum Ratings (Notes 1 and 2)

Voltage (V_{CC}) (Note 3)	6.5V
at Any Pin	−0.3V to (V_{CC} + 0.3V)
Control Inputs	
Control Inputs	−0.3V to +15V
, OE, CLOCK, ALE, ADD A, ADD B, ADD C)	
Temperature Range	−65°C to +150°C
Dissipation at T_A = 25°C	875 mW
Temperature (Soldering, 10 seconds)	300°C

Operating Ratings (Notes 1 and 2)

Temperature Range (Note 1)	$T_{MIN} \le T_A \le T_{MAX}$
ADC0808CJ	−55°C ≤ T_A ≤ +125°C
ADC0808CCJ, ADC0808CCN, ADC0809CCN	−40°C ≤ T_A ≤ +85°C
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.0 V_{DC}

ctrical Characteristics

erter Specifications: V_{CC} = 5 V_{DC} = $V_{REF(+)}$, $V_{REF(-)}$ = GND, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK} = 640 kHz
s otherwise stated.

	Parameter	Conditions	Min	Typ	Max	Units
	ADC0808					
	Total Unadjusted Error	25°C			±1/2	LSB
	(Note 5)	T_{MIN} to T_{MAX}			±3/4	LSB
	ADC0809					
	Total Unadjusted Error	0°C to 70°C			±1	LSB
	(Note 5)	T_{MIN} to T_{MAX}			±1 1/4	LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	2.5		kΩ
	Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.10		V_{CC}+0.10	V_{DC}
(+)	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	V_{CC}+0.1	V
$\frac{(+)+V_{REF(-)}}{2}$	Voltage, Center of Ladder		V_{CC}/2−0.1	V_{CC}/2	V_{CC}/2+0.1	V
(−)	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V
	Comparator Input Current	f_c = 640 kHz, (Note 6)	−2	±0.5	2	μA

ctrical Characteristics

l Levels and DC Specifications: ADC0808CJ 4.5V ≤ V_{CC} ≤ 5.5V, −55°C ≤ T_A ≤ +125°C unless otherwise noted
0808CCJ, ADC0808CCN, and ADC0809CCN 4.75 ≤ V_{CC} ≤ 5.25V, −40°C ≤ T_A ≤ +85°C unless otherwise noted

	Parameter	Conditions	Min	Typ	Max	Units
LOG MULTIPLEXER						
(+)	OFF Channel Leakage Current	V_{CC} = 5V, V_{IN} = 5V,				
		T_A = 25°C		10	200	nA
		T_{MIN} to T_{MAX}			1.0	μA
(−)	OFF Channel Leakage Current	V_{CC} = 5V, V_{IN} = 0,				
		T_A = 25°C	−200	−10		nA
		T_{MIN} to T_{MAX}	−1.0			μA
NTROL INPUTS						
	Logical "1" Input Voltage		V_{CC}−1.5			V
	Logical "0" Input Voltage				1.5	V
	Logical "1" Input Current (The Control Inputs)	V_{IN} = 15V			1.0	μA
	Logical "0" Input Current (The Control Inputs)	V_{IN} = 0	−1.0			μA
	Supply Current	f_{CLK} = 640 kHz		0.3	3.0	mA

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0808CJ $4.5V \le V_{CC} \le 5.5V$, $-55°C \le T_A \le +125°C$ unless otherwise noted
ADC0808CCJ, ADC0808CCN, and ADC0809CCN $4.75 \le V_{CC} \le 5.25V$, $-40°C \le T_A \le +85°C$ unless otherwise noted

Parameter		Conditions	Min	Typ	Max	Units
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O = -360\ \mu A$	$V_{CC}-0.4$			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O = 1.6$ mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	$I_O = 1.2$ mA			0.45	V
I_{OUT}	TRI-STATE® Output Current	$V_O = 5V$			3	μA
		$V_O = 0$	−3			μA

Electrical Characteristics

Timing Specifications: $V_{CC} = V_{REF(+)} = 5V$, $V_{REF(-)} = GND$, $t_r = t_f = 20$ ns and $T_A = 25°C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	*(Figure 5)*		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	*(Figure 5)*		100	200	ns
t_s	Minimum Address Set-Up Time	*(Figure 5)*		25	50	ns
t_H	Minimum Address Hold Time	*(Figure 5)*		25	50	ns
t_D	Analog MUX Delay Time From ALE	$R_S = 0\Omega$ *(Figure 5)*		1	2.5	μs
t_{H1}, t_{H0}	OE Control to Q Logic State	$C_L = 50$ pF, $R_L = 10$k *(Figure 8)*		125	250	ns
t_{1H}, t_{0H}	OE Control to HI-Z	$C_L = 10$ pF, $R_L = 10$k *(Figure 8)*		125	250	ns
t_c	Conversion Time	$f_c = 640$ kHz, *(Figure 5)* (Note 7)	90	100	116	μs
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	*(Figure 5)*	0		8 + 2 μs	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE® Output Capacitance	At TRI-STATE® Outputs, (Note 12)		10	15	pF

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors. See *Figure 3*. None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13*.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence *(Figure 6)*. See paragraph 4.0.

Note 7: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

nctional Description

plexer: The device contains an 8-channel single-ed analog signal multiplexer. A particular input chan-is selected by using the address decoder. Table I s the input states for the address lines to select any nel. The address is latched into the decoder on the o-high transition of the address latch enable signal.

TABLE I

SELECTED ANALOG CHANNEL	ADDRESS LINE		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

VERTER CHARACTERISTICS

Converter

heart of this single chip data acquisition system is its analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach *(Figure 1)* was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +1/2 LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0808, ADC0809, the approximation technique is extended to 8 bits using the 256R network.

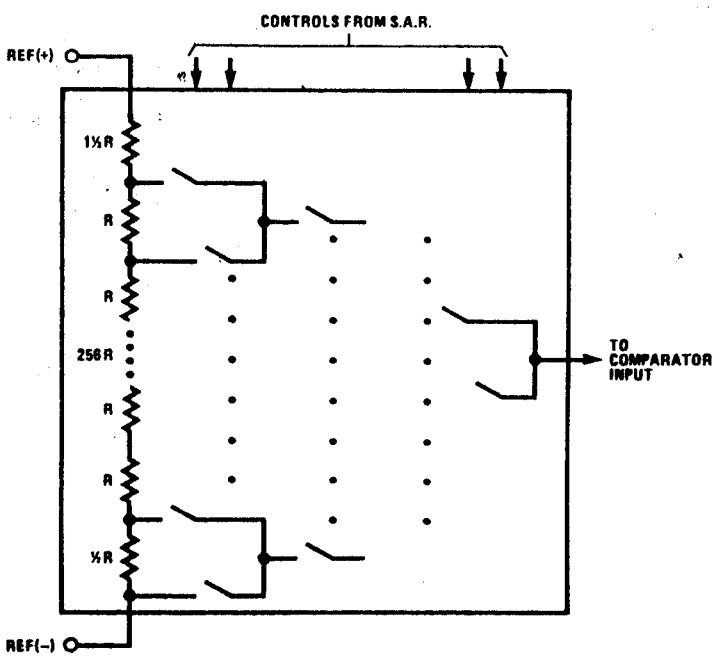


FIGURE 1. Resistor Ladder and Switch Tree

Functional Description (Continued)

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0808 as measured using the procedures outlined in AN-170.

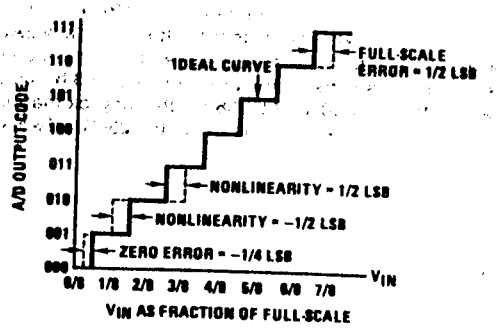


FIGURE 2. 3-Bit A/D Transfer Curve

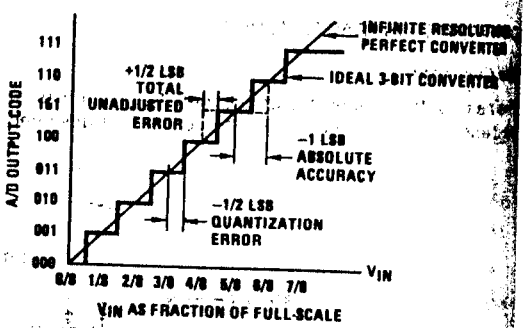


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

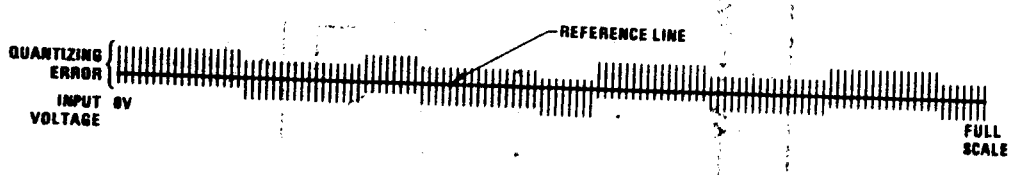
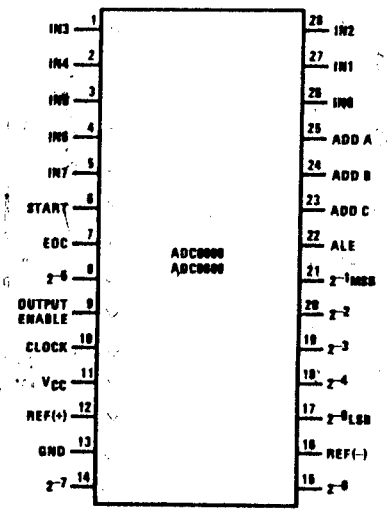


FIGURE 4. Typical Error Curve

on Diagram

Dual-In-Line Package



TOP VIEW

) Diagram

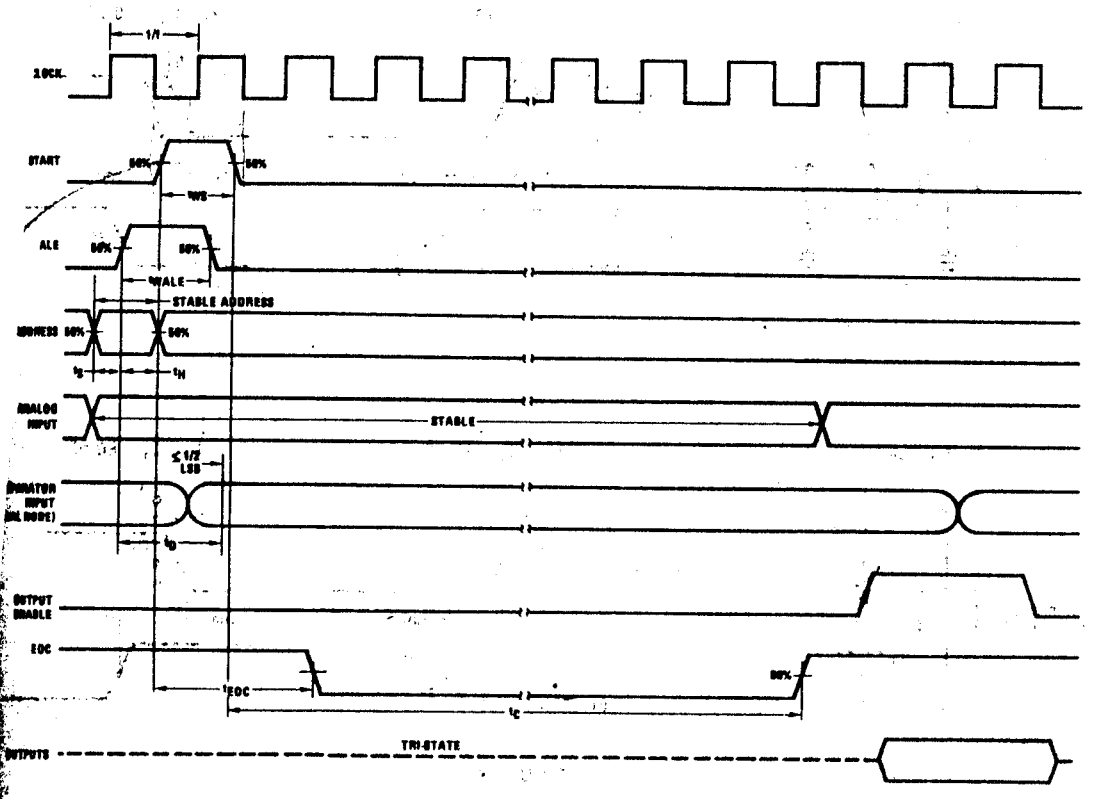


FIGURE 5

Typical Performance Characteristics

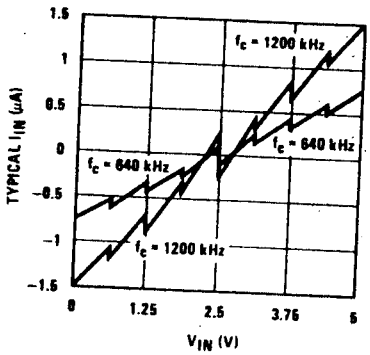


FIGURE 6. Comparator I_{IN} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

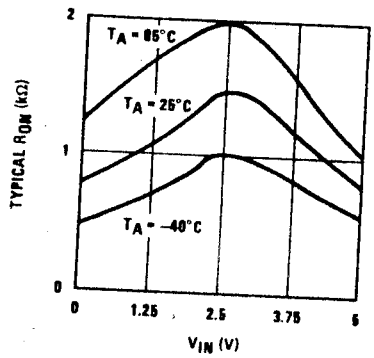


FIGURE 7. Multiplexer R_{ON} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

TRI-STATE® Test Circuits and Timing Diagrams

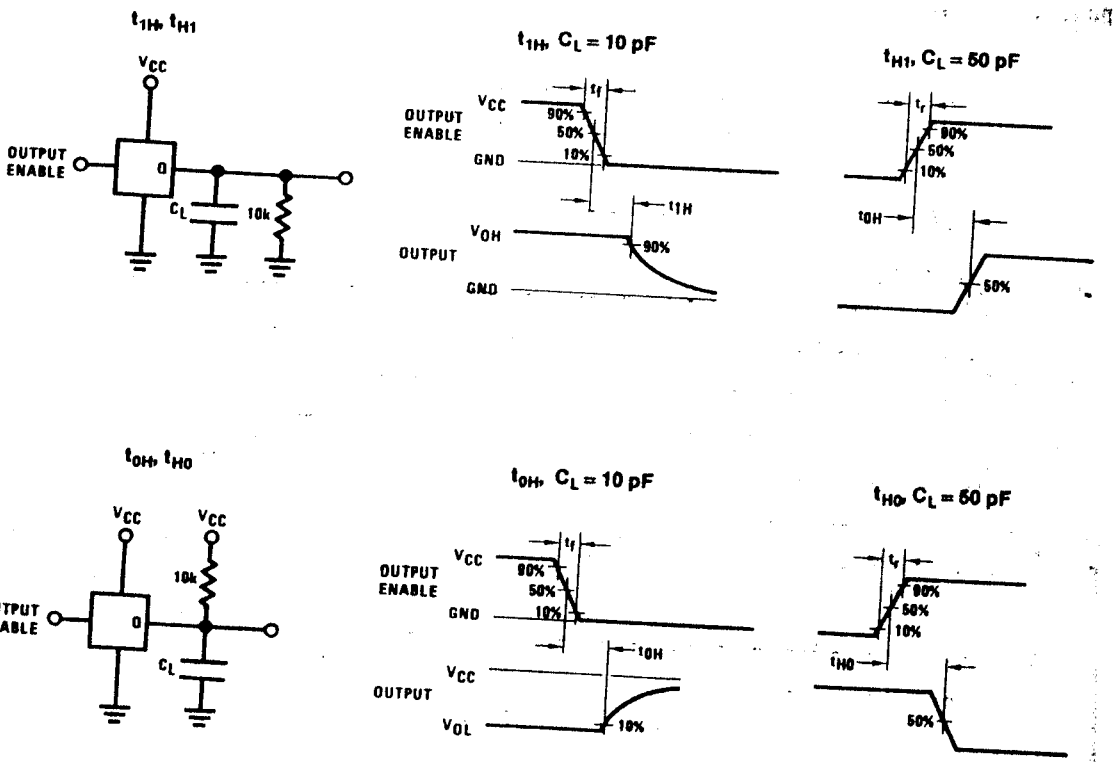


FIGURE 8

plications Information

RATION

tiometric Conversion

ADC0808, ADC0809 is designed as a complete Data isition System (DAS) for ratiometric conversion ms. In ratiometric systems, the physical variable measured is expressed as a percentage of full-scale is not necessarily related to an absolute standard. voltage input to the ADC0808 is expressed by the ion

$$\frac{V_{IN}}{V_{FS} - V_Z} = \frac{D_X}{D_{MAX} - D_{MIN}} \quad (1)$$

= Input voltage into the ADC0808
= Full-scale voltage
= Zero voltage
= Data point being measured
= Maximum data limit
= Minimum data limit

d example of a ratiometric transducer is a poten- ter used as a position sensor. The position of the r is directly proportional to the output voltage which tio of the full-scale voltage across it. Since the data resented as a proportion of full-scale, reference ments are greatly reduced, eliminating a large e of error and cost for many applications. A major tage of the ADC0808, ADC0809 is that the input ge range is equal to the supply range so the ducers can be connected directly across the supply their outputs connected directly into the multiplexer s, *(Figure 9)*.

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC} = V_{REF} = 5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

2.0 Resistor Ladder Limitations

The voltages from the resistor ladder are compared to the selected input 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(−), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V is used, the supply should be adjusted to the same voltage within 0.1V.

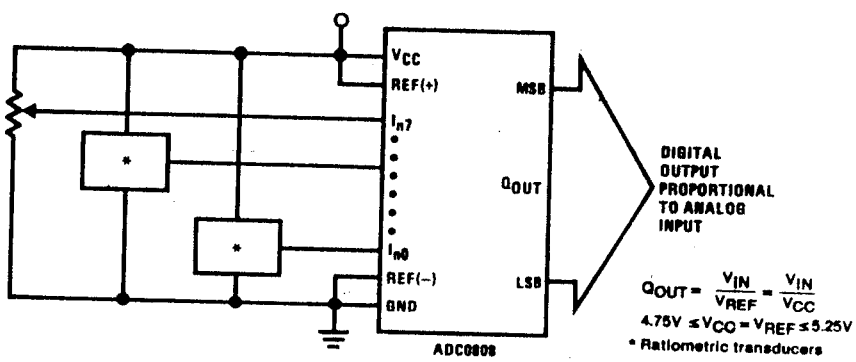


FIGURE 9. Ratiometric Conversion System

Applications Information (Continued)

The ADC0808 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 11* a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 12*. The LM301 is overcompensated to insure stability when loaded by the 10 μF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrical less than V_{CC} and greater than ground. The center of ladder voltage should always be near the center of supply. The sensitivity of the converter can be increased (i.e., size of the LSB steps decreased) by using a ratiometrical reference system. In *Figure 13*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with 2.5V reference allows the LSB bit to be half the size of 5V reference system.

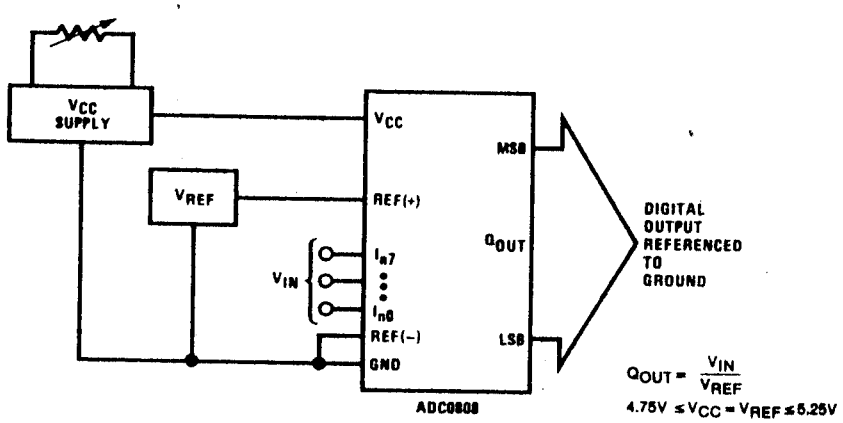


FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply

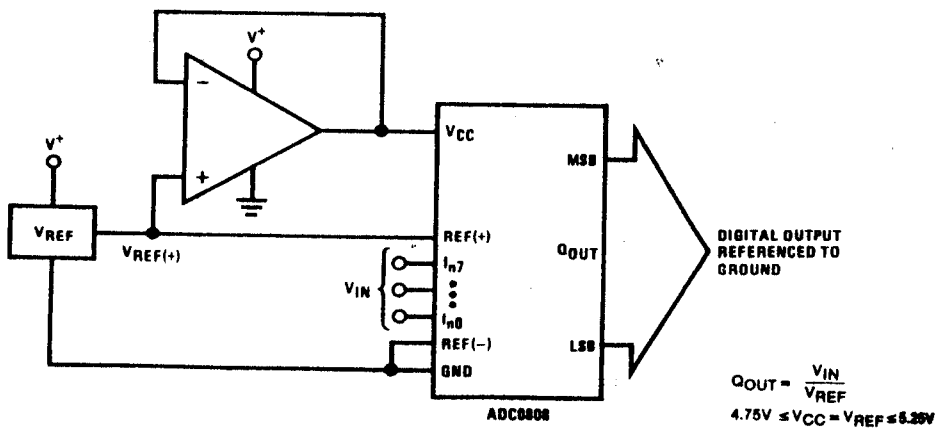
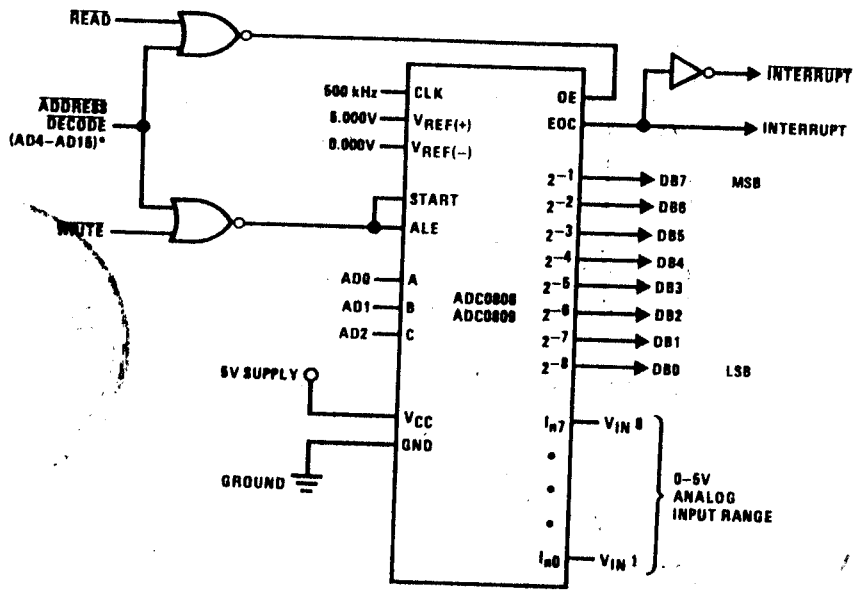


FIGURE 11. Ground Referenced Conversion System with Reference Generating V_{CC} Supply

Typical Application



* Address latches needed for 8085 and SC/MP interfacing the ADC0808 to a microprocessor

MICROPROCESSOR INTERFACE TABLE

PROCESSOR	$\overline{\text{READ}}$	$\overline{\text{WRITE}}$	INTERRUPT (COMMENT)
8080	$\overline{\text{MEMR}}$	$\overline{\text{MEMW}}$	INTR (Thru RST Circuit)
8085	$\overline{\text{RD}}$	$\overline{\text{WR}}$	INTR (Thru RST Circuit)
Z-80	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{INT}}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA·Φ2·R/W	VMA·Φ2·$\overline{\text{R/W}}$	$\overline{\text{IRQA}}$ or $\overline{\text{IRQB}}$ (Thru PIA)

Ordering Information

TEMPERATURE RANGE		−40°C to +85°C		−55°C to +125°C
Error	± 1/2 Bit Unadjusted	ADC0808CCN	ADC0808CCJ	ADC0808CJ
	± 1 Bit Unadjusted	ADC0809CCN		
Package Outline		N28A Molded DIP	J28A Hermetic DIP	J28A Hermetic DIP