TELEPHONE TRACKING SYSTEM

PROJECT REPORT P-1327

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for the award of the Degree of

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Department of Electronics and Communication Engineering

Kumaraguru College of Technology

Coimbatore - 641 006.

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Kumaraguru College of Technology

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Department of Electronics and Communication Engineering

Certificate

This is to certify that the Report entitled

" TELEPHONE TRACKING SYSTEM "

has been submitted by

Mr. _____

in partial fulfilment of the requirements for the Degree of Bachelor of Engineering in the Electronics and Communication Engineering Branch of the Bharathiar University, Coimbatore - 641 006 during the academic year 1996 - '97.

(Guide)

(Head of Department) 9/4

Certified that the candidate was Examined by us in the Project Work Viva - Voce Examination held on _____ *and the University Register Numbare is* _____

(Internal Examiner) 10/4

10/4/97

(External Examiner)

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CONTENTS

SYNOPSIS

This system presented in this project gives the user an unique facility of viewing the calling subscriber telephone number while answering the telephone. The system works on the Dual Tone Multi Frequency (DTMF) principle.

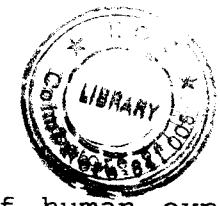
The system consists of a transmitter and a receiver. The telephone number is stored in the transmitter. Since the use of microprocessor / microcontroller is avoided, the cost is drastically reduced.

Some extra features such as memory for storing the incoming call numbers can be added on the existing system. The circuit is completely designed, fabricated and tested.

The system proposed in this project is a novel idea. This facility is first of its kind and is not available elsewhere.

INTRODUCTION...

INTRODUCTION



Speech is the most natural means of human expressions and that explains why telephones have become an indispensable part in our day to day life.

Advancement in the telecommunication is at its zenith with the introduction of Cellular telephones and digital telephony (ISDN). It only goes on to prove that there are still many areas in telecommunications left open to the researcher and even slight modifications performed on existing system would result in a consumer endurable product.

In the present system, the tracing of a call is a tedious process. The process involves the subscriber giving his number to the telecom department and requesting them to monitor his number for incoming calls. The authorities monitor the subscribers number for anonymous calls and give report on the incoming calls after a period of time, say one week.

With the introduction of our system, The Telephone Tracking System (TTS) as we call it, the subscriber can view

the telephone number of the calling subscriber while answering the phone and thus anonymous calls can be noted down.

Our system consists of a transmitter and receiver. The transmitter is carefully designed so that all the extra costs are cut and the net transmitter is cheap and easy to install in all telephones. The receiver which is also comparatively cheaper, one can be had as an extra attachment. The transmitter alone transmits the telephone numbers of the telephone to which it is attached. If the called subscriber has the facility of a receiver, then he can decode the transmitted information and view the telephone numbers of the calling subscriber.

In addition to this obvious advantage, the receiver can also be made to provide the following special features.

a. Storage of the incoming calls (10 numbers can be stored and reviewed later)

b. View Dial - This is an unique facility which the user can view the called numbers and dial that number by simply pressing a button.

CONSUMER TELEPHONE EQUIPMENT...

THE CONSUMER TELEPHONE EQUIPMENT

A telephone system must be capable of transmitting and receiving voice or other sounds. The system must also be capable of addressing or indicating the person or location you wish to call. Generally addressing is referred as Dialing function. Next, the system must be able to Alert the person or station addressed. Generally, alerting function is done by Ringing the telephone. Finally the system must supervise all of these functions and continuously scan the circuits to determine when someone wishes to place a call. Lifting the telephone off-hook indicates this request to call condition to the switching equipment. The exchange responds to the request by transmitting a dial tone back to off hook.

a. OFF HOOK IMPEDENCE AND BANDWIDTH OR FREQUENCY RESPONSE

The typical off-hook impedence of a standard telephone is about 600 ohms at frequencies between 300 and 3000Hz. Most standard telephones have a frequency response of about 300 to 3000Hz. Within 6dB of 1KHz response. The typical DC resistance of an OFF-HOOK telephone is about 250 ohms.

b. BATTERY VOLTAGE (D.C OPERATING VOLTAGE)

The telephone exchange continuously applies a DC voltage to the telephone line through a series impedence. Typically this voltage is -48V and is produced by a giant bank of batteries connected in parallel.

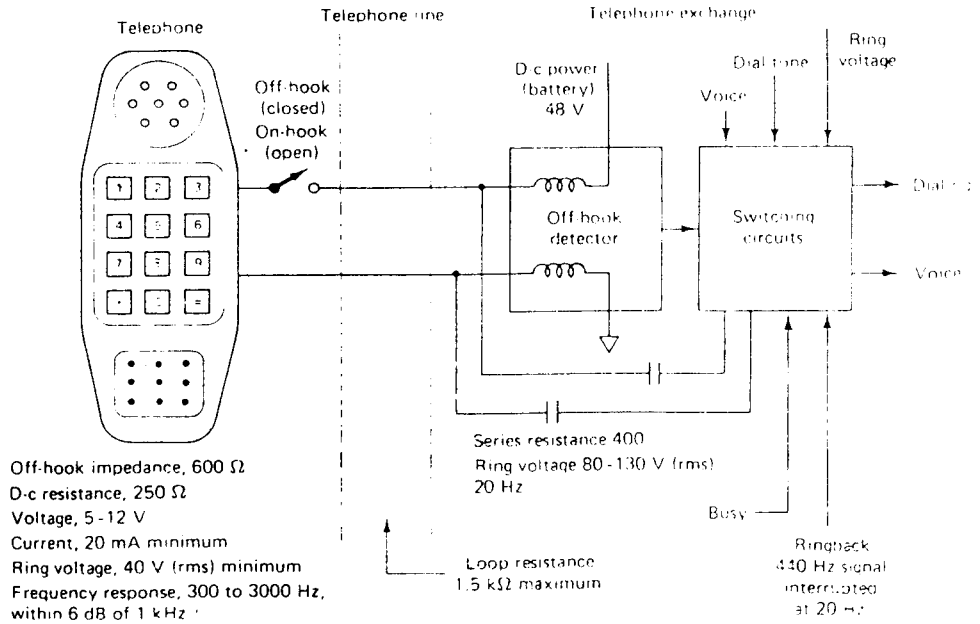


Fig.1 Basic characteristics for both telephones and telephone exchanges.

Batteries are used to provide telephone operators in case of power failure.

When the telephone is on-hook, the telephone appears as an open circuit and no current flows on the line. When the telephone is off-hook, line current flows and powers the telephone.

A standard telephone exchange is requested at least 20ma of line current. The loop resistance of a long telephone may be upto 1500 ohms. Loop resistance refers to the resistance from the exchange to the telephone and from telephone back to the exchange. When the full 1500 ohms value is present, the line current must still be 20 ma. For shorter telephone lines, the available current may be as high as 120 ma. However, most telephones have circuits to automatically shunt excess line current. Although about 48V is available at the exchange, the voltage across an off-hook telephone is 5 to 12V.

The standard polarity of DC operating voltage (battery voltage) is negative to the "ring" and return to the "tip".

"Ring" and "Tip" are telephone terms applied to the concentric ring and tip portions of a telephone Jack and have nothing to do with the ringing of the telephone.

c. VOICE SIGNALS

When voice is present, current variations are super imposed on the DC operating voltage. Typically, a voltage regulator within the telephone provides a constant voltage to the telephone circuits even though the line current is varied by voice signals.

d. THE RINGING VOLTAGE

The exchange applies a 20 Hz sine wave ringing voltage of about 80 - 130 V (rms). Typically the ringing voltage is 100 V (or 280 V peak to peak). Telephones must be capable of ringing properly with a ringing voltage of 40 V (which is the value the ringing voltage may drop to over a long telephone line with 1500 ohms impedence).

The ringing voltage or signal is applied to the

telephone line only when exchange detects a high impedence (when the telephone is on-hook). The ringing is usually 2 to 2.5 secs on and 3.5 to 4 secs off, for a 6-second repetition cycle.

Although the standard frequency for the ringing signal is 20 Hz. Additional frequencies may be used in some party line applications. In those cases, telephone ringers with corresponding resonant frequencies assure that only one telephone rings.

e. THE DIALING SYSTEMS

Dialing is done by means of pulses (for rotary and non-tone dial telephones) or tone pairs (for tone dial telephones)

On rotary dial telephones, the pulses are produced by opening and closing a set of contacts. For push-button pulse-dial telephones, the pulses are produced by turning a switching circuit on and off.

With Touch Tone (" Touch Tone " is a registered trademark of AT&T) and other compatible telephones, the dialing tones are produced by oscillators that generate tone. The tone are mixed in pairs to form each digit. The 3x4 matrix layout of the dialing keypad selects one " row " and one " column " oscillator for each digit. These are commonly known as DTMF (Dual Tone Multi Frequency) frequencies.

DC SIGNALING

Whenever a junction or trunk circuit is of a type suitable to carry direct-current signals, and the resistance is not too high to permit DC signaling currents of adequate strength to be transmitted, a comprehensive range of calling and automatic supervisory signals can be obtained. Dial pulses may also be transmitted unless the length and characteristics of the circuits are such as to cause excessive pulse distortion.

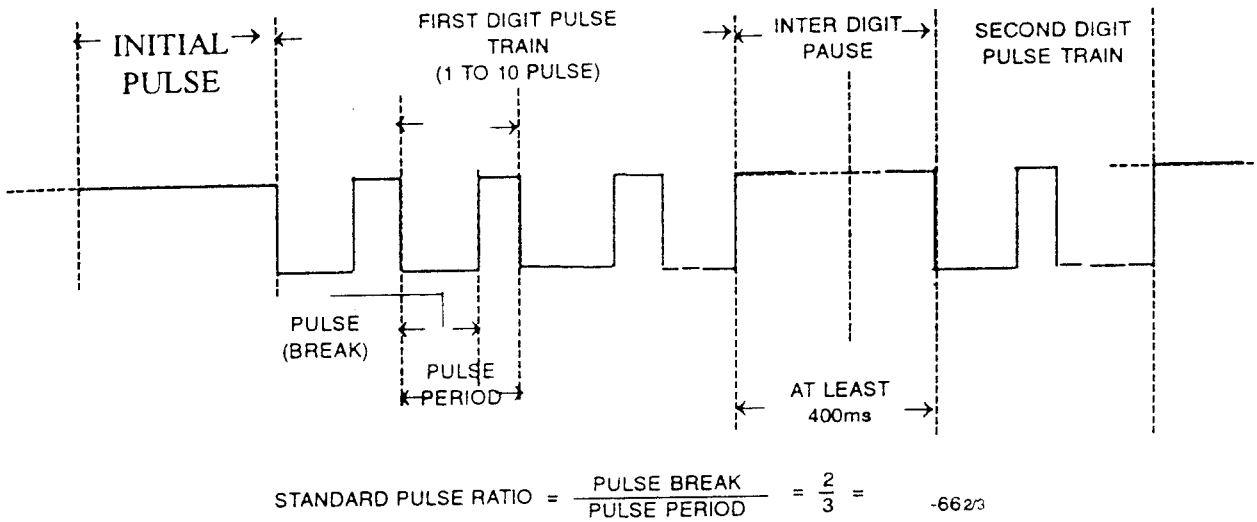


Fig : 2

STANDARD PULSE TRAINS IN AUTOMATIC SWITCHING SYSTEMS

DIALING :

In case of pulse dialing each digit (0 to 9) is represented by different train of pulses and hence two digit will be represented by two trains of impulses. The shortcomings of this method is the time taken was longer for the higher numbers compared to others and hence most of the

systems today encourage the tone dialing. The concept of combination of frequency is made use in tone dialing. Each number dialed is represented as a combination of frequencies depending on the row and column frequencies. This is explained as per the table given below

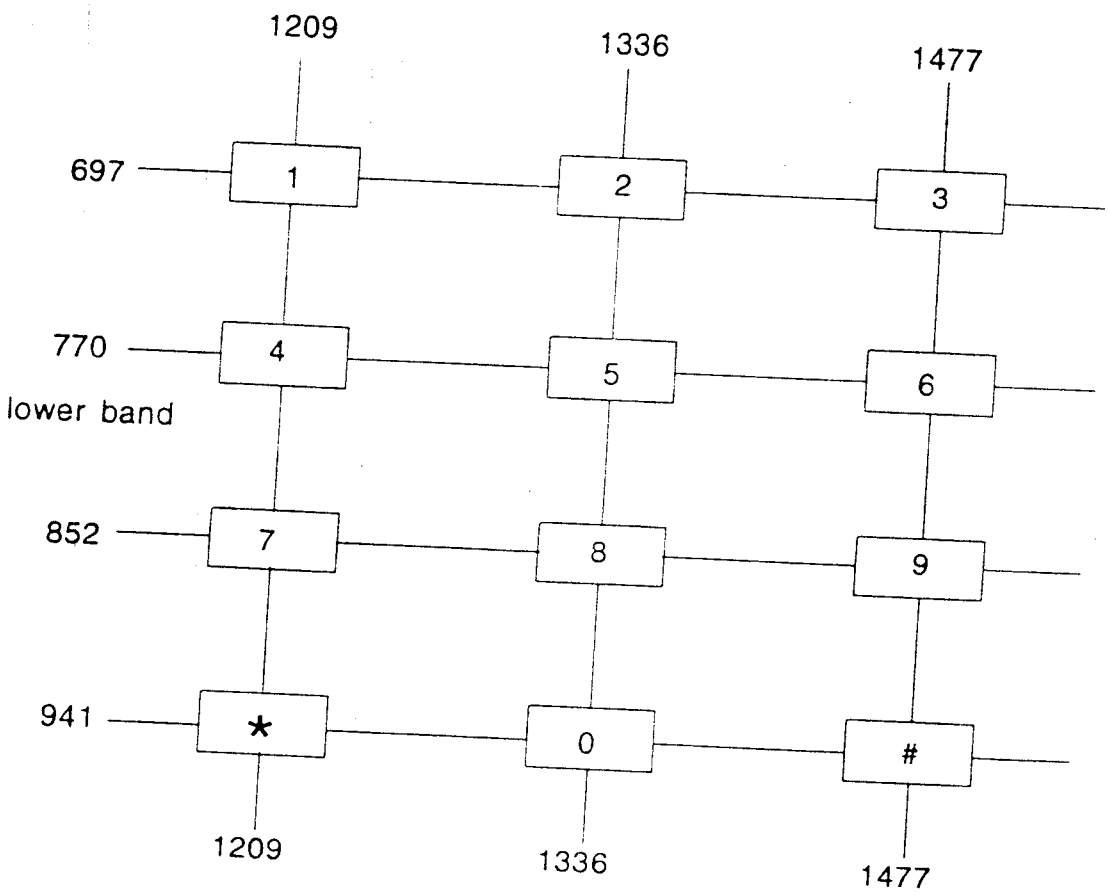


Fig - 3

BASIC ELECTRONIC TELEPHONE CIRCUITS

The ringing signal from the exchange is applied to the electronic ringer circuit through capacitive coupling. The electronic ringer consists of an oscillator and buffer which operates at the rate of about 218 KHz, interrupted at a rate of 20 Hz. This interruption causes the " chirping " sound that is heard when a telephone rings. The signals are applied only to the buffer while the ringing signal is present. So, if the ringing signal is on for 2 seconds and off for 4 seconds, the chirping is heard for 2 seconds (at 4 seconds intervals).

For standard desk telephones (those with a bell rather than an electronic ringer), the ringing signal is applied to an electro mechanical bell through capacitive frequency of 20 Hz.

Capacitive coupling is used with both electronic and non-electronic telephones. In either case the ringer must not offer a DC path for line current when the telephone is on hook.

DC (battery) power, incoming and outgoing audio signals and dialing signals are applied through a diode bridge, an on-hook / off-hook, and a switching circuit. The diode bridge serves as an automatic polarity corrector for electronic circuits in the telephone, providing the proper polarity even if the polarity of the telephone connection becomes reversed (from the normal -48 V).

Note that the dialing IC gets DC power directly from the diode bridge, bypassing the on-hook / off-hook switch. This is necessary with redial and memory telephones because the dialing IC must always have power to store the redial information in the memory.

When the telephone is dialed an oscillator dialing IC generates a certain number of pulses for each digit. These pulses cause the switching circuit to emit the proper pulse train for each digit. The pulse train is fed through the on-hook / off-hook switch and the diode bridge on the telephone line. The dialing pulses are fed through the telephone line to the exchange, where the pulses are decoded to make the proper connection.

While talking, the outgoing audio is fed into an audio amplifier from the microphone. This amplified signal is fed to the primary of the hybrid transformer which super imposes the signal on the DC operating voltage. The voice signal is passed through the switching circuit, on-hook / off-hook switch, and diode bridge out of the telephone line. The signal is then connected to the telephone at the other end of line by the exchange.

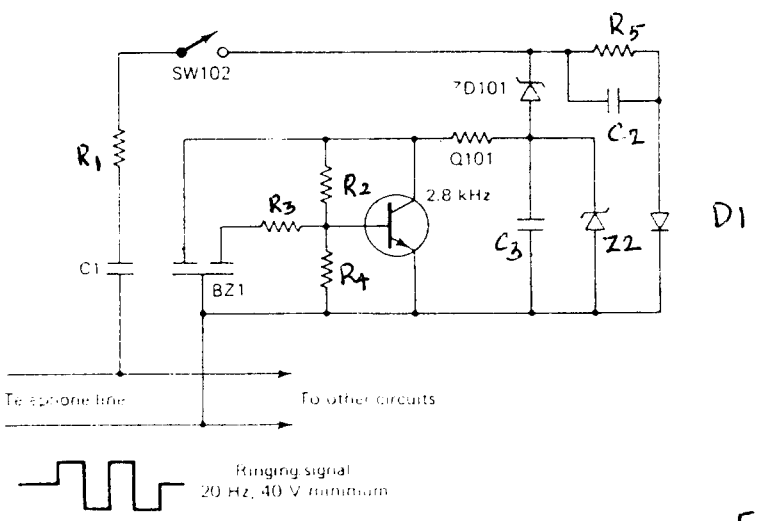
The voice signal is also fed to the secondary of the hybrid transformer which feeds the signal at a low level to the speaker so that you hear you hear your own voice in the ear piece as you speak. This is known as " Side Tone ", without this side tone, the conversation would sound unnatural.

Incoming audio is fed by the exchange through the line and into the telephone. This signal passes through the diode bridge, on-hook / off-hook switch, switching circuit and hybrid transformer to the speaker.

TYPICAL RINGER CIRCUIT FOR AN ELECTRONIC TELEPHONE

The ring buzzer BZ1 and oscillator Q101 are coupled to the telephone line through C1. Capacitive coupling is used to prevent DC voltage from turning Q101 on. A 27V Zener diode ZD101 is also connected between the oscillator and the telephone line to prevent small signals, such as dial tones or audio from triggering Q101. Note that Q101 can be disabled to prevent ringing when power to Q101 is interrupted by opening ringer ON/OFF switch SW102.

The ringing signal (of atleast 40 Vrms at 20 Hz) exceeds the ZD101 Zener voltage turn on point and provides power to Q101, which oscillates at approximately 2.8KHz. Power from the ring signal is essentially a 20 Hz square wave that interrupts the 2.8 KHz. oscillations at a 20 Hz. rate.

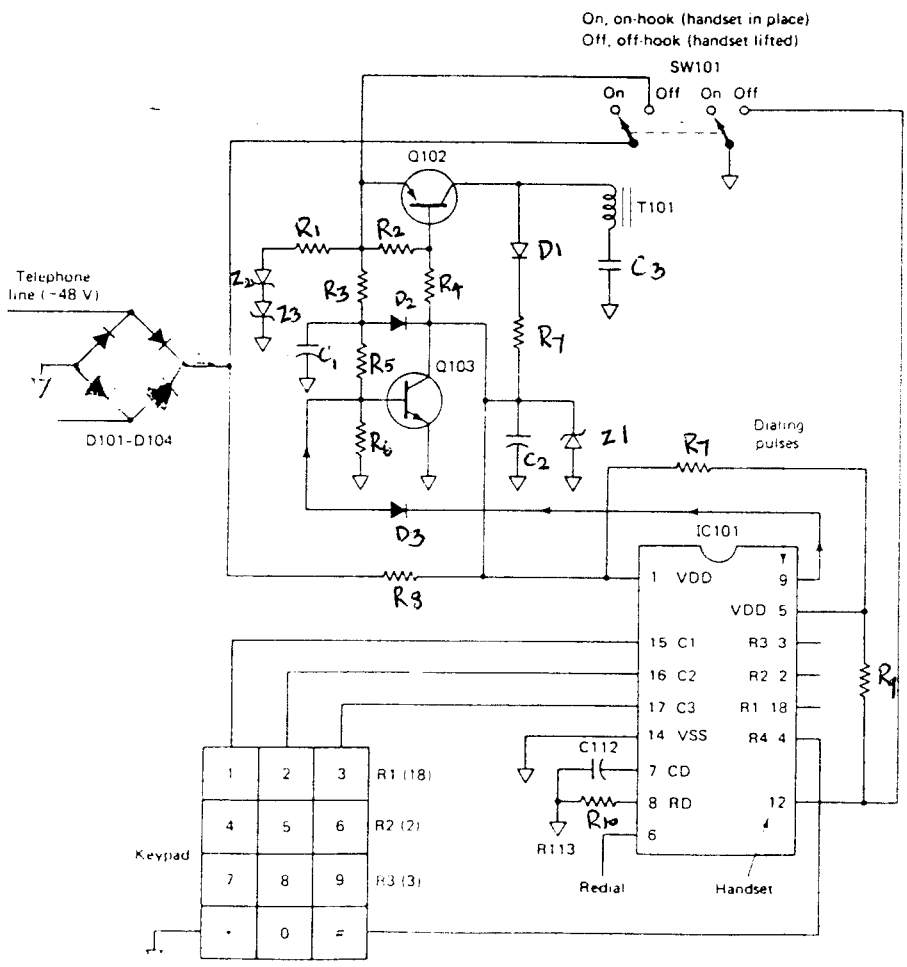


Ringer circuit of an electronic telephone

Fig : 5

TYPICAL DIALING CIRCUIT FOR AN ELECTRONIC TELEPHONE

The power for the dialing circuit is taken from the telephone line (-48 V) and applied through diode bridge D101 - D104 to the keypad, dialer IC 101, and the switching circuit Q102 / Q103. The diode bridge keeps the polarity of the power applied to the dialing circuit constant, even if the polarity of the -48 V provided by exchange is reversed.



Dialing circuit of an electronic telephone

Fig : 6

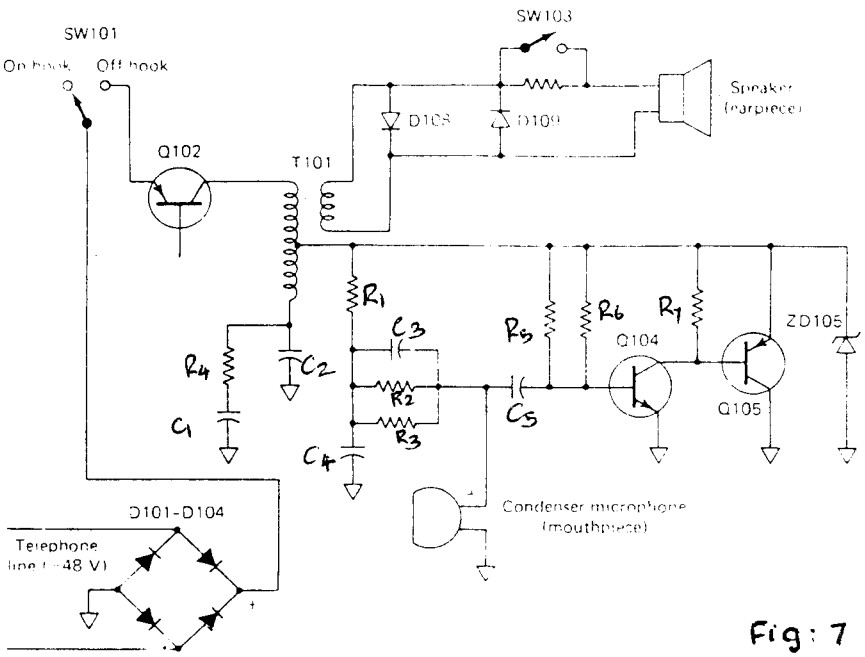
The dialing keypad is connected to IC101, where each digit that has been dialed is read. The figure shows the circuit of a pulse-dial telephone. IC101 releases a corresponding number of pulses for each digit. A storage circuit within IC101 allows the digits to be dialed faster than they are clocked out. C112 and R113 are a timing circuit used to control IC101 so that the dialing pulses are clocked at steady rate.

The dialing pulses from IC101 are applied to Q102 / Q103, which turns on and off. The pulses at the emitter of Q102 are applied to the telephone line and exchange through the hook ON / OFF switch SW101 and diode bridge D101-D104. The collector of Q102 is also connected to hybrid transformer T101. Note that IC101 produces the dialing pulses(at pin 9) only when pin 12 is turned to ground through the other contacts of hook ON/OFF switch SW101, in the OFF hook (handset lifted) condition. Also, when the telephone is hung up (on-hook, handset replaced), the last number dialed is latched into memory within IC101 so that the number can be released when a redial button is pressed. Not all electronic telephones have a redial function.

TYPICAL AUDIO CIRCUIT FOR AN ELECTRONIC TELEPHONE

Power for the audio circuit is taken from the telephone line (-48 V) through diode bridge D101 - D104, SW101, Q102 and the primary of the hybrid transformer T101.

When one speaks into the microphone (on the handset), the signal is amplified by Q104/Q105. The primary of T101 acts as audio load for amplifier circuit Q104/Q105, which varies current through the primary of T101 at the audio line These current variations are applied to the telephone line through Q102, hook on/off switch SW101, and the diode bridge D101-D104. The variations appear at the voice transformer of the telephone exchange and are applied to the telephone at the receiving end as incoming audio. ZD105 keeps the operating voltages for Q104 / Q105 constant, inspite of current variations.



Audio circuit for an electronic telephone

Incoming audio is in the form of current variation on the telephone line. These current variations are fed through diode bridge SW101, Q102 & T101 to audio circuit. The audio signals are coupled through the secondary of T101 to the speaker (in the ear piece of the handset). Diode D108 & D109 protect the speaker from voltage spikes that might be present by clipping off any signal above forward voltage drop of the diodes. Note that volume of the audio to the speaker can be controlled by volume Hi/Low switch SW103.

Note too, that some of the amplified microphone audio from Q104/Q105 is also coupled into the secondary of T101 and is applied to speaker, along with incoming audio.

PROJECT INTRODUCTION...

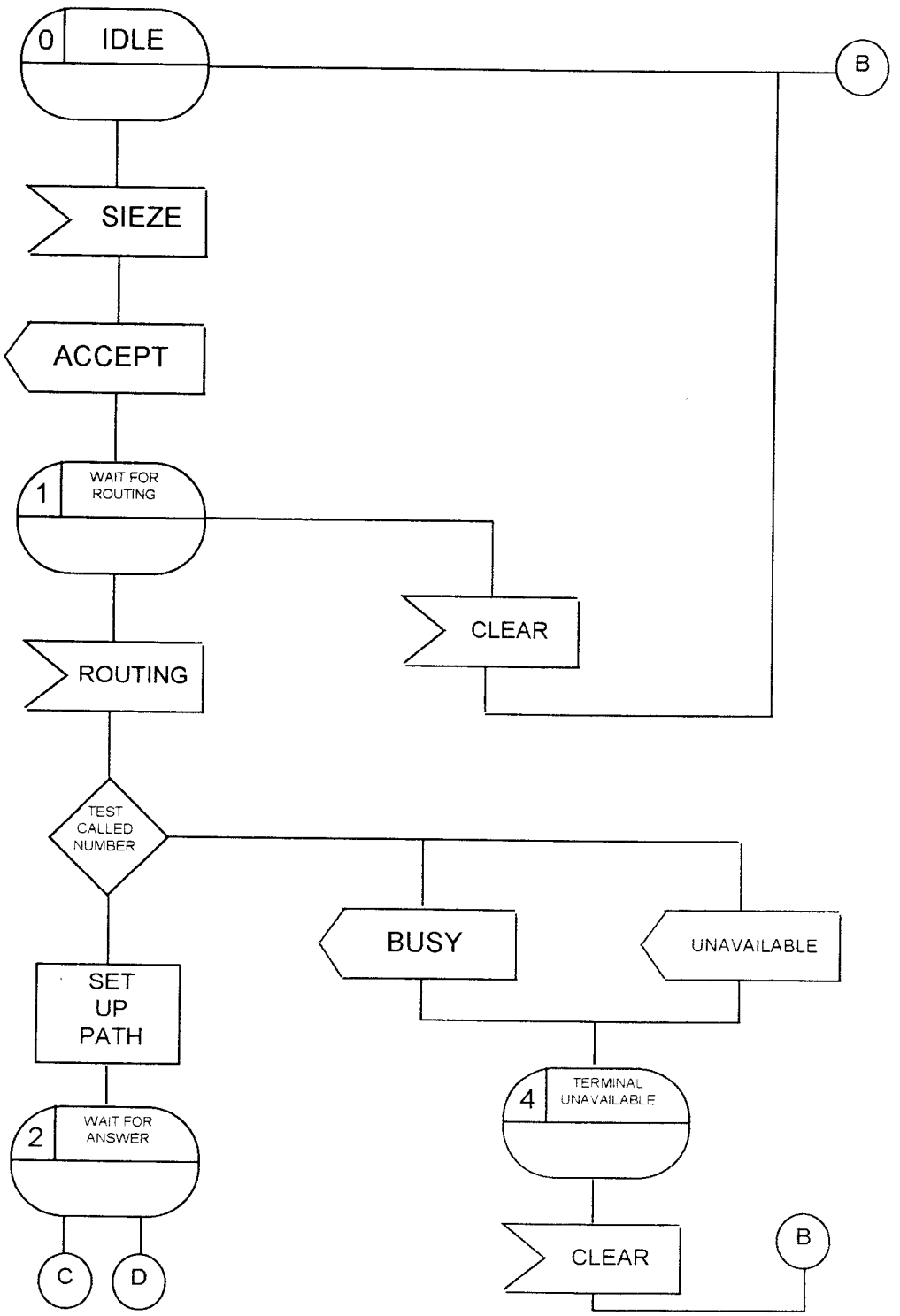
PROJECT INTRODUCTION

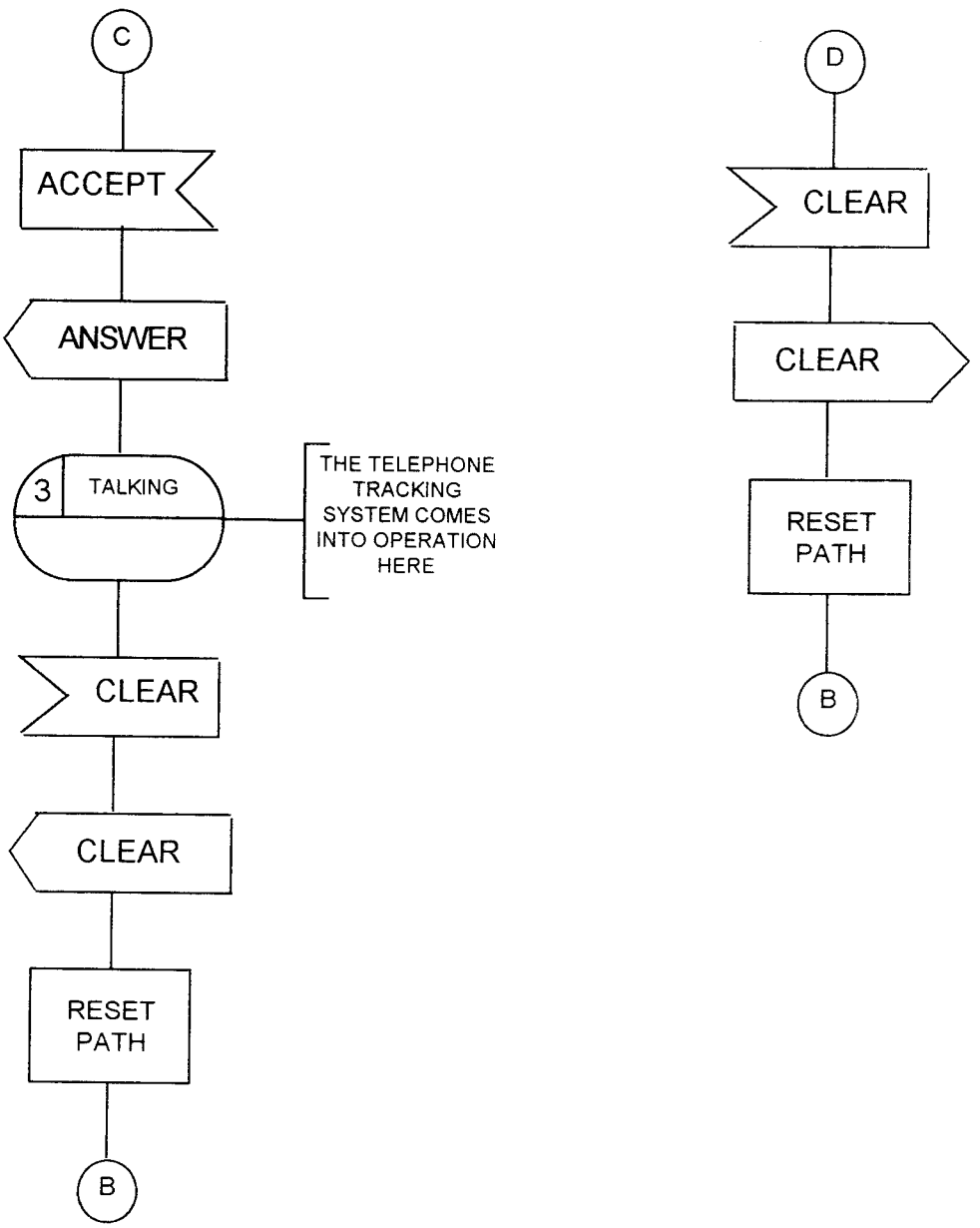
The telephone tracking system provides the user a new facility of viewing the calling party number while answering the telephone. In the present system, a call can be tracked or traced only in the exchange. If the exchange is an Electronic one, the tracing process is comparatively simple since each call is recorded in the magnetic tape. But in a cross bar exchange, tracing of a call is very difficult and consumes a lot of time. In either type of service, a subscriber can trace his calling party only with the help of the exchange.

Our system does not depend on the exchange to trace a call. The incoming call is immediately traced provided the calling party has TTS transmitter and the called party has the TTS - receiver. The incoming calls are traced within 3 seconds after picking up the receiver. The exchange to which the subscriber is connected can be a crossbar (electro mechanical) or an electronic exchange. The only requirement id that the subscriber must have a telephone which is capable of operating in tone dialing (DTMF) mode. The complete operation of the system is described by the state transition diagram and flowcharts. State transition diagrams is the

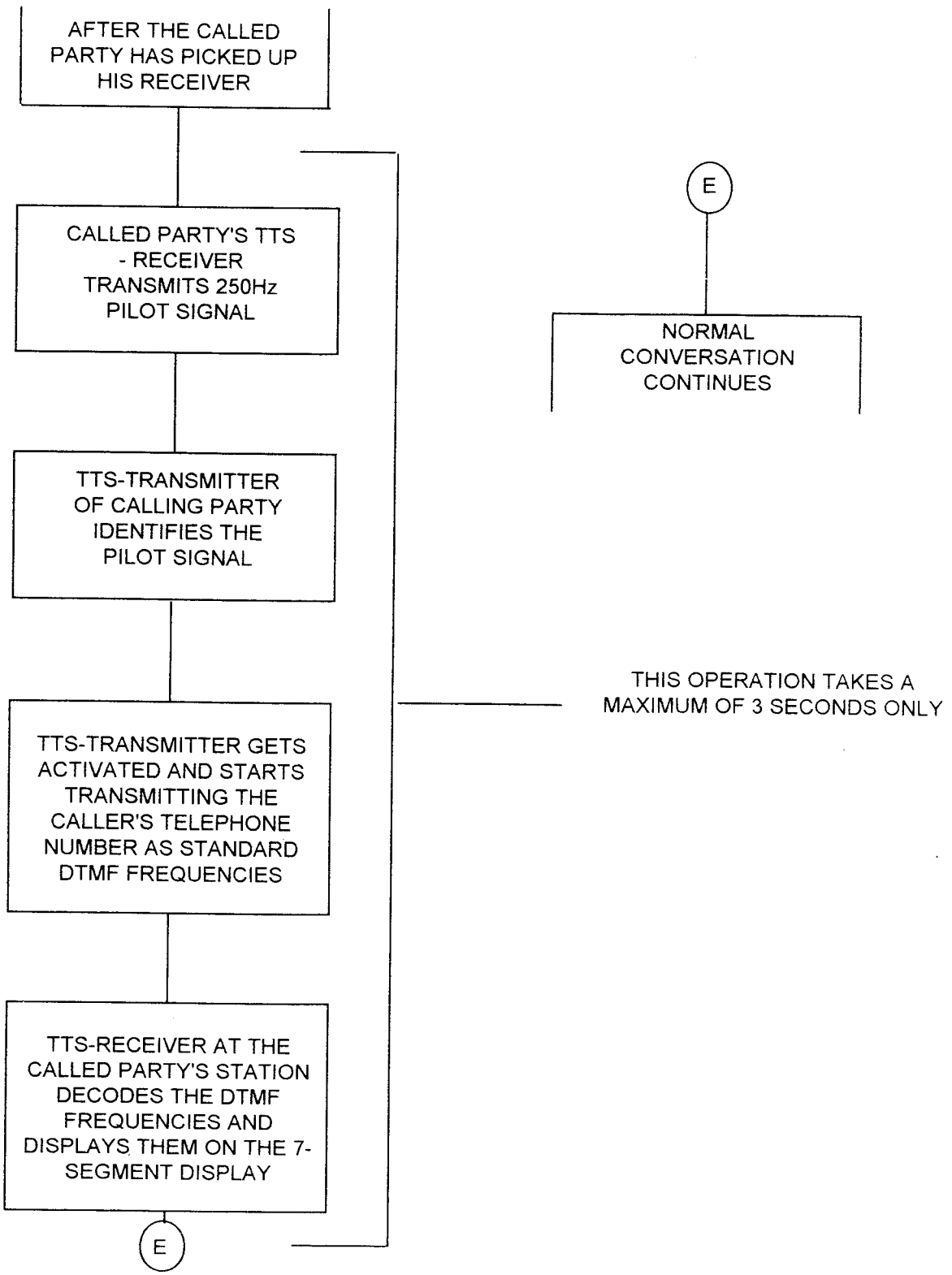
valid sequence of signals or events that take place at the switching centers. The following state transition diagram describes the process of one subscriber making a call to another subscriber taking into account all the possibilities at the called subscribers terminal. The possibilities are, the terminals may be busy or free. If free, the calling subscriber is connected else busy tone is returned. If the connected, then ringing tone is placed and when the called subscriber answers the phone, a direct voice link is established and path is maintained until the calling subscriber resets the path.

THE STATE TRANSITION DIAGRAM




C
ACCEPT
ANSWER
3
TALKING
THE TELEPHONE TRACKING SYSTEM COMES INTO OPERATION HERE
CLEAR
CLEAR
RESET PATH
B
D
CLEAR
CLEAR
RESET PATH
B

THE TELEPHONE TRACKING SYSTEM OPERATION



WORKING PRINCIPLE...

WORKING PRINCIPLE

THE TELEPHONE TRACKING SYSTEM - THE TRANSMITTER

The tone decoder LM567 on detecting the pilot signal, shorts its output transistor to ground and thus a low output voltage is obtained as long as the pilot signal is available at LM567's input pin. This low output voltage is inverted and applied to the SET pin of D-flip flop 4013. The flip flop outputs Q=1. This output devices an astable multivibratoir and an astable output signal is obtained. This astable output is applied as clock signal to the binary counters and the counter starts counting from 0000 H. The counter output lines ABCD are directly connected to the BCD to decimal counter. The decoder decodes the input values and selects a corresponding output line. The selected pin has a logic 1 voltage (+5 V). This is applied as the enable signal for a switch and that switch is closed whenever the corresponding pin is selected. The counter proceeds to count until the count value reaches 1111 H. When the count value reaches 1111 the flip flop is reset and the counting stops.

Since to the IN and OUT pins of the switch a row and a

column is connected. Whenever the switch is closed, the dual tone for the digit corresponding to the row and column is sent on the line ie. pressing of that particular digit is simulated.

The number is transmitted once whenever the pilot signal is detected by the LM567.

The transmitter gets activated only when the pilot signal is sensed. The pilot signal transmitter is present in the receiver. So only a receiver can activate the transmitter to transit the number.

POWER SUPPLY REQUIREMENTS OF TRANSMITTER

The power supply to the tone decoder, flip-flop, counter and CMOS switch in the transmitter is provided by a special circuit which provides a constant voltage of +5 V which is tapped from the telephone line.

In the telephone line on `ON-HOOK' condition, there is a voltage drop of 48 V across the lines. The telephone line is connected to a bridge rectifier. The output of the bridge rectifier is connected to a Zener diode through a power transistor. The Zener diode has a drop of +5.6 V and the

output of the transistor is around +5 V.

When the telephone is in " OFF-HOOK "condition, there is a voltage of 11V across the lines. In this condition also, the output of the transistor is around +5 V, thus powering the transmitter.

Thus for the power supply for the transmitter part of the telephone tracking system, we make use of the voltage available in the telephone itself. The connection of this transmitter does not affect the performance of the telephone in anyway.

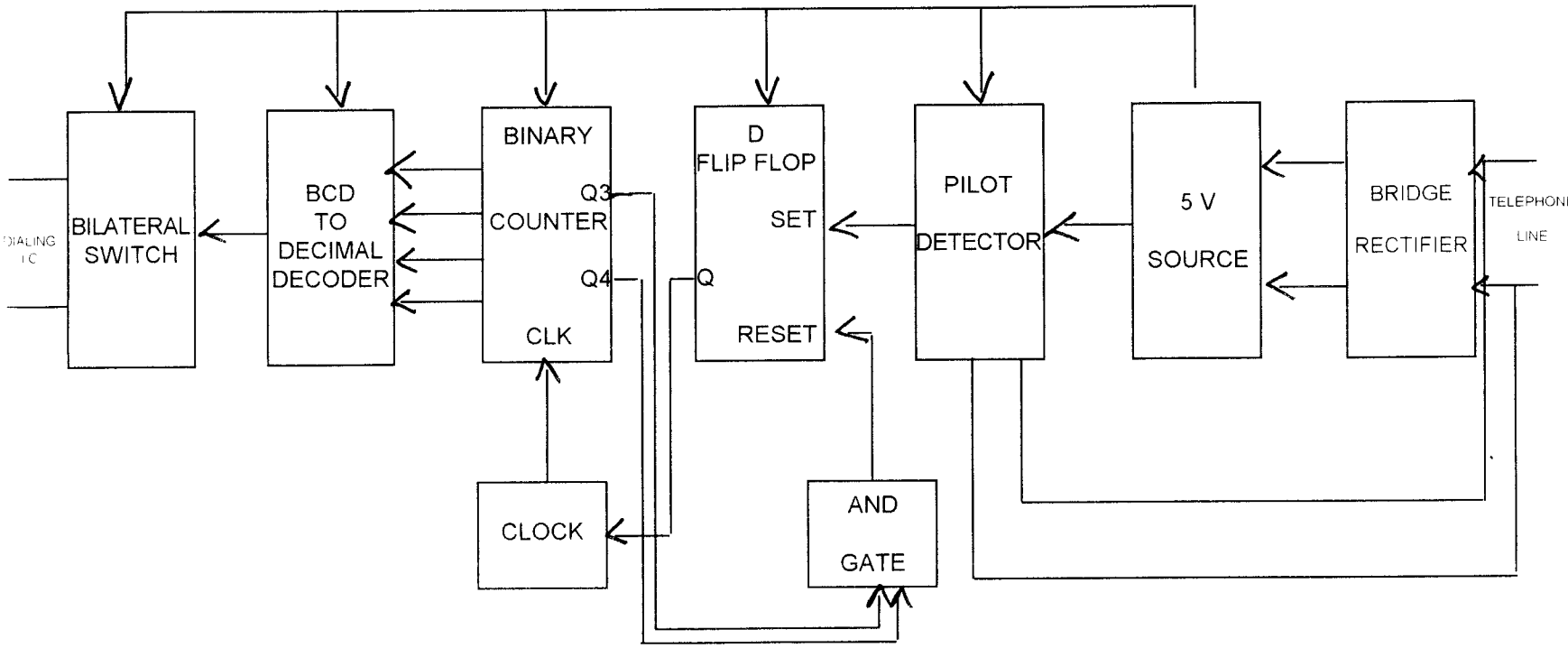
TELEPHONE TRACKING SYSTEM - THE RECIEVER

After the calling party has dialed the telephone number of the person to be called he may get a busy tone or a ringing tone accordingly. In case the calling party is not engaged, he will be intimated by a ringing sound. When the called off-hook's his telephone set as a response to the incoming call, the folling operation takes place if his set is provided with a TTS receiver.

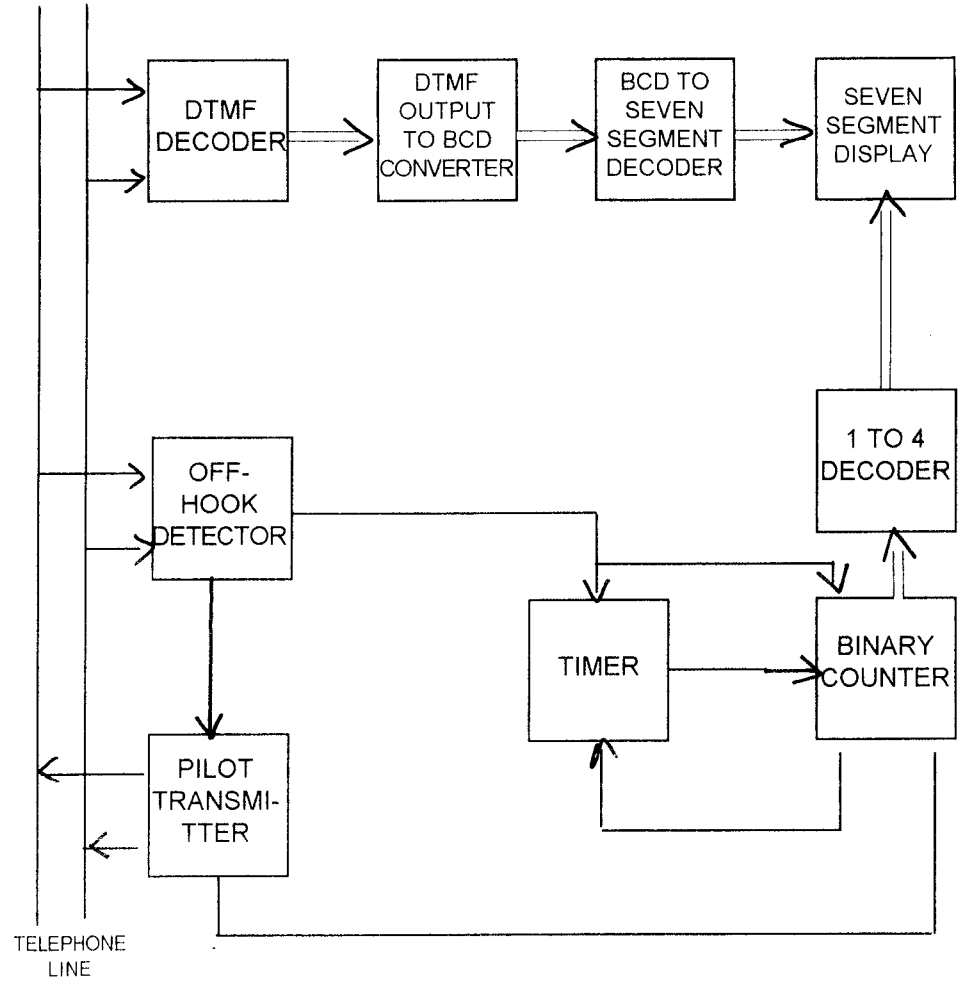
The off-hook condition is detected using LM324. The output of this IC goes high in case of off-hook and goes low in case of on-hook. The output of this IC forms one of the control signals for driving the pilot signal transmitter and clock pulse generator. The output also resets the binary counter to 0000 H. The counter starts counting as its clock input is intiated by LM324. Meanwhile the pilot signal is transmitter through the telephone line and when the counter output is 0100 H, the pilot signal transmission is stopped. The pilot signal transmission is set for a timing of one second. This pilot signal forms an intimation of off-hook state of called party to the calling party. The TTS transmitter on the calling party side senses the signal and starts transmitting the number of the calling party in DTMF mode.

The DTMF decoder MT 8870 decodes the transmitted number. The decoded transmitted number is converted to BCD, and these BCD converted outputs forms the input to 4543 which is a BCD to seven segment decoder/latch. The latches are enabled accordingly using a 4555 which is a 1 to 4 decoder. The two LSB outputs of the counter forms the input to the 1 to 4 decoder.

BASIC BLOCK DIAGRAM OF TTS TRANSMITTER



BASIC BLOCK DIAGRAM OF TTS RECEIVER



HARDWARE DESCRIPTION...

HARDWARE DESCRIPTION

CMOS BILATERAL SWITCH:

The CMOS bilateral switch used here is CD4066B. The RCA-CD4066B is a quad bilateral switch intended for transmission or multiplexing of analog or digital signals. It exhibits a very low on resistance which is relatively constant over the full input signal range.

The CD4066B consists of 4 independent bilateral switches. A single control signal is required per switch. Both the p and n device in a given switch are biased ON or OFF simultaneously by the control signal.

The IC is powered by +5 V on V_{DD} and 0V on V_{SS}. When the voltage on enable line is +5 V, the switch is on and when the voltage is 0 V, the switch is OFF.

The CMOS analog switch is interfaced directly with the pulse/DTMF dialer IC of the telephone. Interfacing is accomplished by making use of the lines from the pulse / DTMF dialer chip which goes to the keypad of the telephone.

All the 4 switches are used. The enable input of each

switch is connected to the output of 4 to 10 decoder. The first switch is used to simulate the pressing of the button '*' which converts the telephone from pulse dialing mode to tone dialing mode. The other 3 switches are used to transmit the 3 digit telephone numbers.

Although only 3 digit dialing is done, the range can be extended upto 9 digits by adding an extra 4066B.

DECODER:

The CMOS decodes used here is CD4028B. The RCA-CD4028B types all BCD to decimal or binary to octal decoders consisting of buffering on all 4 inputs, decoding logic gates and 10 output buffers. A BCD code supplied to the 4 inputs A to D results in a high level at the selected one of 10 decimal decoded outputs.

The IC is powered by +5 V on V_{DD} and 0 V on V_{SS}. It exhibits "positive logic" as decoded output goes high on selection. The 4 bit input from a binary up/down counter.

COUNTER:

The RCA-CD4516B is presettable binary up/down counter. The counter consists of 4 synchronously clocked D-type flip flops connected as counters. These counters can be cleared by a high level on RESET line, and can be preset to any binary number on the jam inputs by a high level on the PRESET ENABLE line.

If the CARRY-IN input is held low, the counter advances up or down on each positive going clock transition. Synchronous cascading is accomplished by connecting all clock inputs in parallel and connecting the CARRY-OUT of less significant stage to the CARRY-IN of a more significant stage.

The chip is powered by +5 V on V_{DD} and 0 V on V_{SS}. The clock to the counter is provided by an astable multivibrator generating a rectangular wave repeating itself at a frequency of 7 Hertz.

The counter is held in count up mode with CARRY IN held low. The preset enable line is grounded when the count value reaches the maximum i.e., 1111 H, the counter is reset and the clock is cut off.

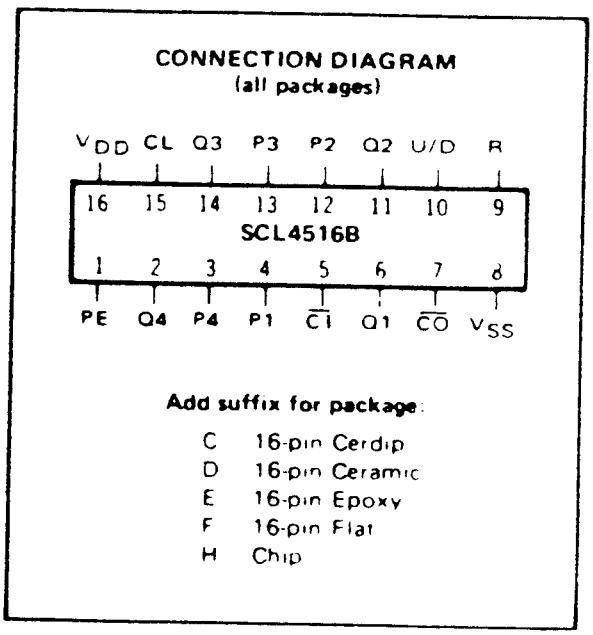


Fig: 8

TRUTH TABLE

CARRY IN	UP/DOWN	PRESET ENABLE	RESET	ACTION
1	X	0	0	No Count
0	1	0	0	Count Up
0	0	0	0	Count Down
X	X	1	0	Preset
X	X	X	1	Reset

X = Don't Care

CLOCK:

A 555 timer used in astable mode will generate a rectangular wave of presettable frequency. This wave is used as a clock for the counter.

The 555 timer can be used with supply voltage in the range of +5 V to +18 V and can drive load upto 200mA. The functional diagram of 555 is shown in the figure. The three 5Kohm internal resistors act as voltage divider, providing a bias voltage of 2/3 V_{CC} to the upper comparator (UC) and 1/3 V_{CC} to lower comparator (LC), where V_{CC} is the supply voltage. Since these 2 voltages fix the necessary comparator threshold voltage, they also aim in determining the timing interval. It is possible to vary the time electronically too, by applying a modulating voltage to the control voltage input terminal. In application where no such modulation is intended, a capacitor (0.01 micro farads) is connected between control voltage terminal and ground to bypass noise or ripple from the supply.

In the standby (stable) state, the output Q of control flip flop is low.

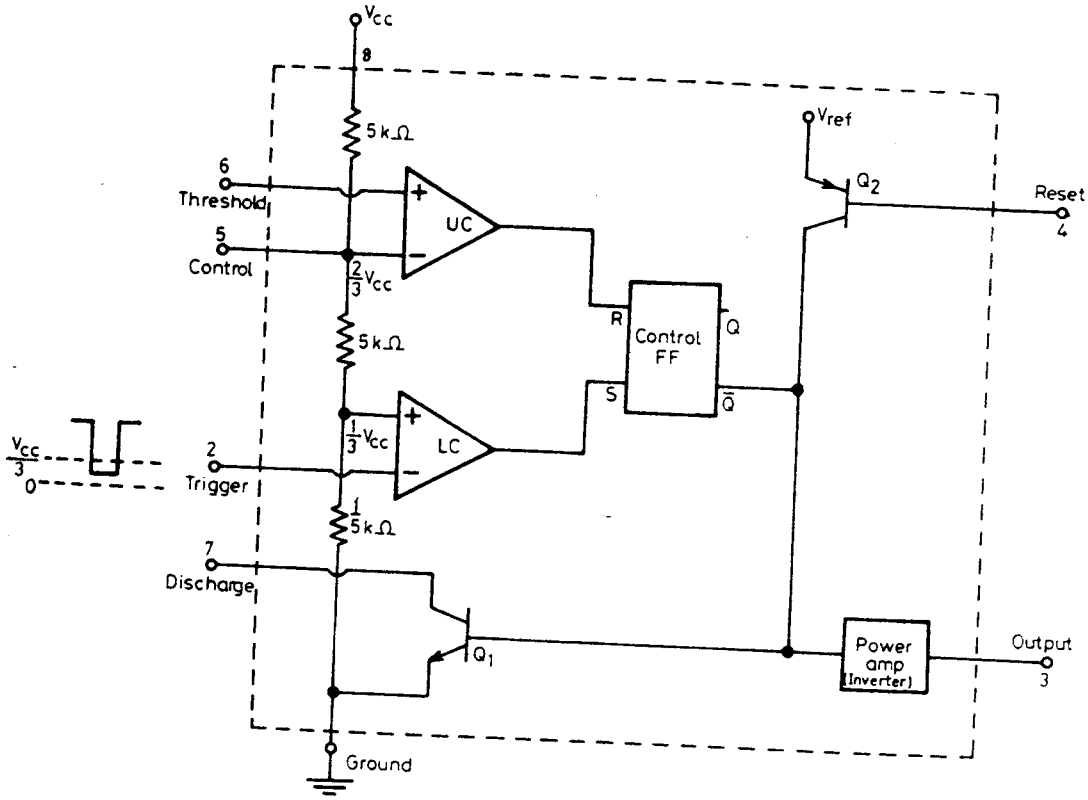


Fig.9 FUNCTIONAL DIAGRAM OF 555 TIMER

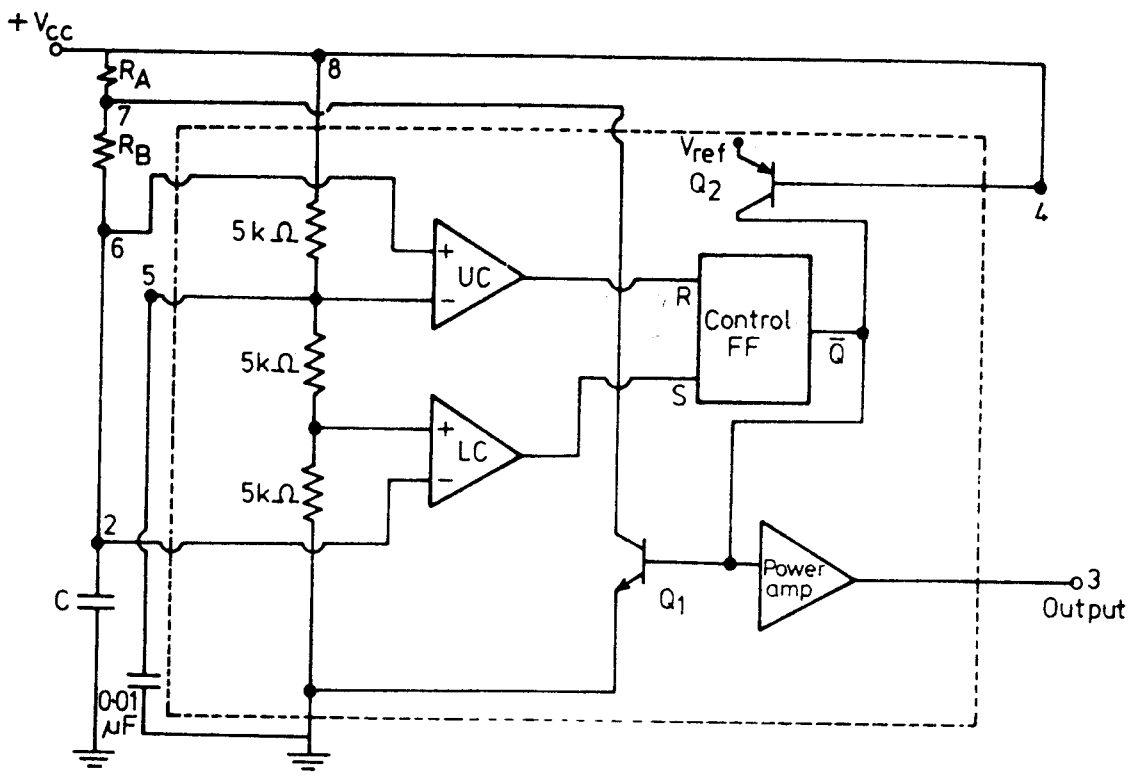
This is because of power amplifier which is basically an inverter. A negative going trigger pulse is applied to PIN 2 and should have its DC level greater than the threshold level of lower comparator (ie Vcc/3). At the negative going edge of the trigger, as the trigger passes through (Vcc/3), the

output of lower comparator goes HIGH and sets the FF (Q=1, Q=0). During the positive excursion, when the threshold voltage at PIN 6 passes through 2/3 V_{CC}, the output of upper comparator goes high and resets FF (Q=0, Q=1).

The reset input (PIN 4) provides a mechanism to reset the FF in a manner which overrides the effects of any instruction coming to FF from the lower comparator. This overriding reset is effective when the reset input is less than about 0.4 V. When the reset is not used, it is returned to Vcc. The transistor Q2 serves as a buffer to isolate the reset input from the FF and transistor Q1. The transistor Q2 is driven by an internal reference voltage Vref obtained from supply voltage Vcc.

ASTABLE OPERATION

The device is connected for astable operation as shown



Functional diagram of astable multivibrator using 555 timer

Fig 10

The timing resistance are R_A & R_B. PIN 7 of discharging transistor Q1 is connected to the function of R_A & R_B. When the power supply Vcc is connected, the external timing capacitor C charges towards Vcc with a time constant (R_A + R_B)*C. During this time, output (PIN 3) is high (equal to Vcc) as reset R=0, set S=1 and this combination makes Q=0 which has unclamped the timing capacitor C.

When the capacitor voltage equals (to be precise is just greater than), (2/3) Vcc the upper comparator triggers the control flip flop so that Q=1. This, inturn makes transistor Q1 on and capacitor C starts discharging towards ground through R_B and transistor Q1 with a time constant R_B*C. Current also flows into transistor Q1 through R_A. Resistors R_A & R_B must be large enough to limit this current and prevent damage to the discharge transistor Q1. The minimum value of R_A is approximately equal to Vcc/0.2 where 0.2A is the maximum current through the ON transistor Q1.

During the discharge of the timing capacitor C, as it reaches (to be precise is just less than) Vcc/3, the lower comparator is triggered and at this stage S=1, R=0, which turns Q=0. Now Q=0 unclamps the external timing capacitor C.

The capacitor C is thus periodically charged and discharged between 2/3 Vcc and 1/3 Vcc respectively. The length of time that the output remains HIGH is the time for the capacitor to charge from 1/3 Vcc to 2/3 Vcc. The design are given below.

$$t_{HIGH} = 0.69\ (R_A + R_B)C$$

$$t_{LOW} = 0.69\ R_B C$$

$$\text{Total time } T = t_{HIGH} + t_{LOW}$$

$$= 0.69\ (R_A + 2R_B)C$$

$$f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)}$$

LATCH

The latch used here is CD 4013, CMOS dual D type flip flop. The C0 4013 has the following features.

a. Set - Reset capability

b. Static flip-flop operation retains state indefinitely with clock level either "high" or "low".

c. Medium speed operation - 10 MHz clock toggle rate at 10V

d. Quiescent current specified at 15 V

e. Maximum input leakage current of 1 μ a at 15 V (full package temperature range)

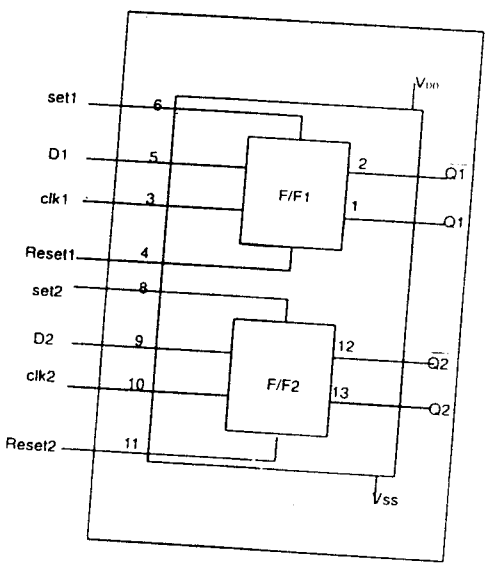
f. 1-V noise margin.

The CD 4013 consists of 2 independent, identical data type flip flops. Each flip flop has independent data set, reset and clock input and Q & Q outputs. The logic level present at the D input is transferred to the Q output during the positive going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line respectively.

Set input to PIN-6 is from the output of LM567 via CD4069. D input is grounded. The clock input at PIN-3 is tied to V_{CC}. The reset input is from the AND gate 4081 and is given to PIN-4. This depends on the count value of the counter. When the bits Q_2 and Q_4 of the counter are 1, the flip flop is reset.

When the pilot is detected, the flip flop is set and the counter is initiated. The Q output of the flip flop is given as input to the astable multivibrator. The output of

astable multivibrator is given as clock input to the counter. The flip flop is reset whenever the bits Q_2 and Q_4 of the counter are 1. This is detected by means of an AND gate CD 4081.



TRUTH TABLE

CLK	D	R	S	Q	$\overline{Q}$
↑	0	0	0	0	1
↑	1	0	0	1	0
↓	X	0	0	Q	$\overline{Q}$
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

CIRCUIT DIAGRAM

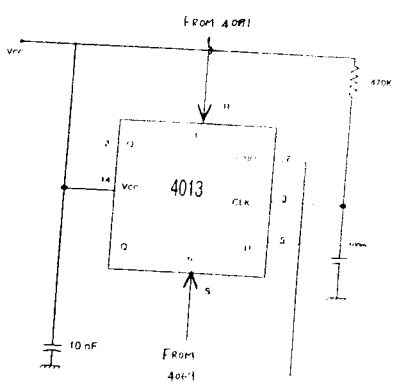
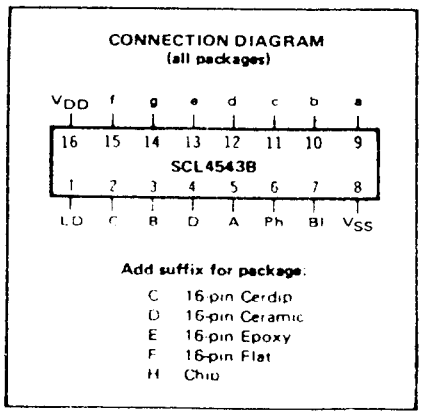


Fig : 11

BCD TO SEVEN SEGMENT LATCH / DECODER / DRIVER

The SCL 4543B BCD to seven segment latch / decoder / driver is designed for use with liquid crystals readouts and is constructed with complementary MOS (CMOS) enhanced mode devices. The circuit provides the function of a four-bit storage latch and a 8421 BCD-to-seven segment decoder and driver. The device has the capability to invert the logic levels of the output combinations. The phase (Ph), blanking (BI), latch disable (LD) inputs are used to the reverse the truth-table phase, blank the display, and store a BCD code respectively. For liquid crystal readouts, a square wave is applied to the Ph input of the circuit and electrically common back plane of the display. The outputs of the circuit are connected directly to the segments of the readout. For other type of readouts, such as light emitting diode (LED), incandescent, gas discharged, and fluroscent readouts, the connection diagrams are given in the data sheets.



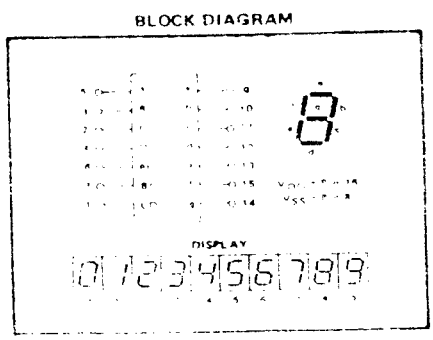
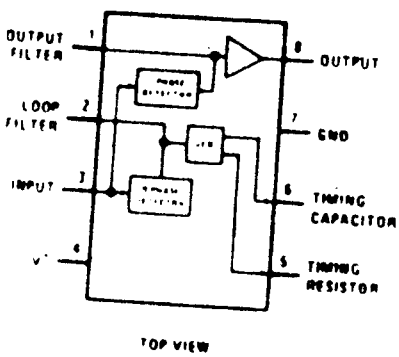


Fig 12

TONE DECODER

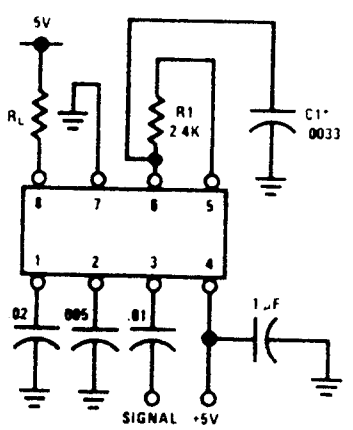
The tone decoder used here is LH567, 567 detects a single frequency at its input terminal. 567 is tunable to a wide range of frequency. The frequency is varied by adjusting the timing resistance and capacitors (Rt, Ct). LM567 is a general purpose tone decoder designed to provide a saturated transistor switch to ground when an input signal is present within the passband. The circuit consists of an I and Q detector driven by a voltage controlled oscillator which determines the center frequency of the decoder. The center frequency is adjustable from 0.01 Hz to 500 KHz.

Dual-In-Line Package



TOP VIEW

AC Test Circuit



f_o = 100 kHz +5V

*Note: Adjust for f_o = 100 kHz

Fig 13

DTMF DECODER

The telephone number of the calling person is dialed in tone mode after he is linked to the called person in a TTS.

On the called side a DTMF receiver is used to receive this tone which is a combination of these two frequencies and convert it to a binary coded decimal. For this purpose the DTMF decoder MT 8870 is used.

The MT 8870 is a complete DTMF receiver designed to detect standard DTMF signals. It includes a differential input amplifier, filter section, decoder section and steering logic circuits. The differential input amplifier allows adjustments of gain and choice of input configuration. The filter section provides a dial tone filter for dial-tone rejection and separates the dual tone signals into low-group and high-group tones. The decoder decodes all 16 DTMF tone pairs into four bit code.

DTMF DECODER

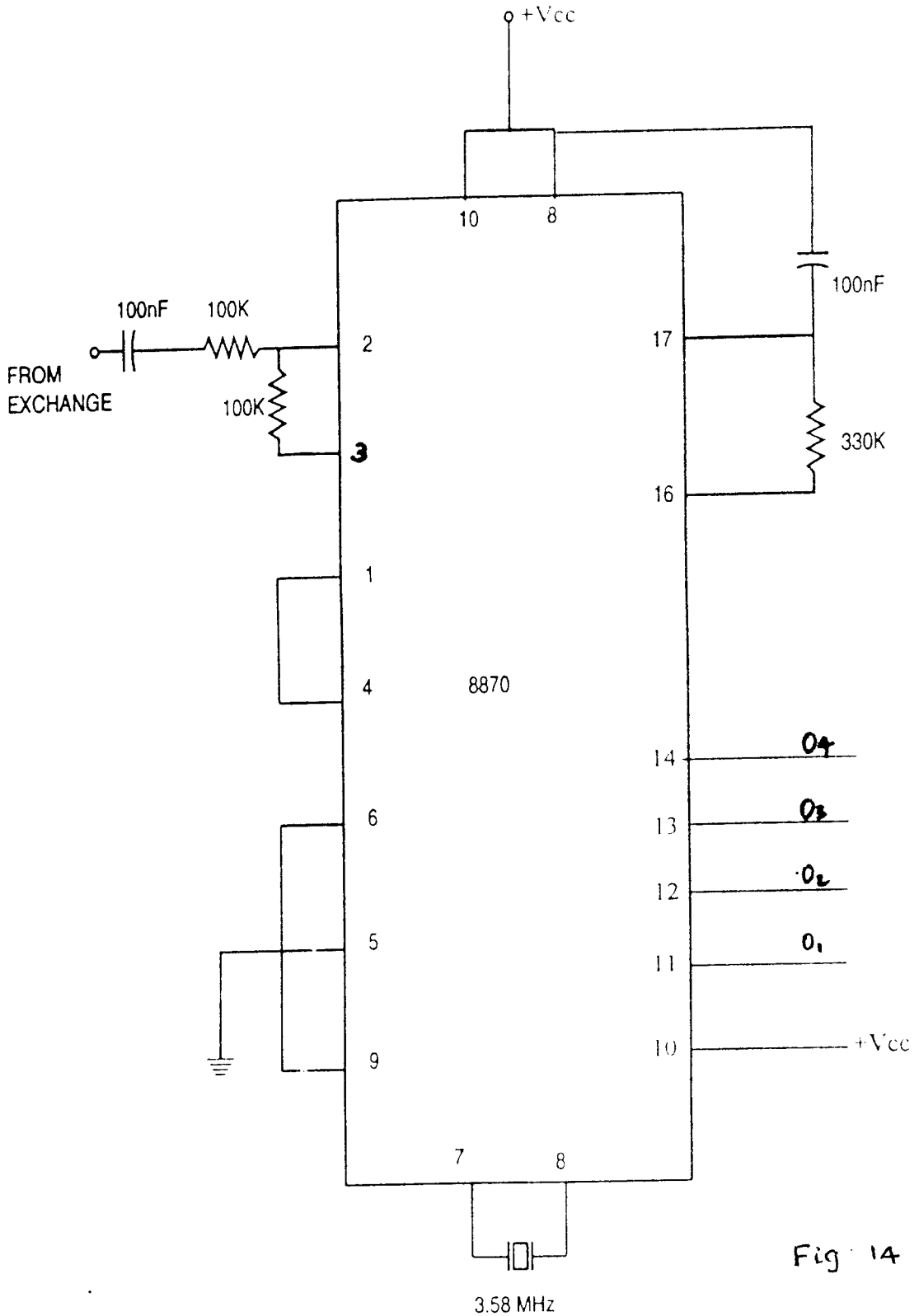


Fig 14

FUNCTIONAL DESCRIPTION

The exchange line is applied to the inverting input through C1, R1 of the differential input operational amplifier and a bias source Vref is used to bias the input at midrail. Adjustment of gain is achieved by connecting a feedback resistor to the op amp output (GS). For a single ended input configuration op amp is connected for unity gain and Vref = $A_{DD}/2$.

The differential amplifier is followed by the filter section. Dial tone at 350Hz and 440 Hz is then rejected by a third order switched capacitor notch filter. The signal is split into individual high and low frequency components by two sixth order switched capacitor bandpass filter. Each component tone is then smoothed by an output filter and squared up by a hard limiting comparator. If the original DTMF input signals are valid tones, then the outputs of the comparators will be two rectangular waves.

The resulting rectangular waves are applied to a decoder where a counting algorithm measures and averages their periods. When the decoder recognizes the presence of a valid tone the Est signal goes high. Est indicates that two

tones of proper frequency have been detected and initiates an RC timing circuit. If both tones are present for a minimum guard time, which is determined by the external RC network, the DTMF signal is decoded and the resulting data is latched in the output register. A logic high on Est causes Vc to reach the threshold of the steering logic. When the voltage on Vc rises above V_{TST} it causes the device to register the detected tone pair and update the output latch. At this point, the GT output is activated and drives Vc to VDD. GT continues to drive high as long as Est remains high. Finally the delayed steering (StD) output is raised and indicates that new data is available. The contents of the output latch are made available on the four-bit output bus by raising the three-state control input (TOE) to a logic high.

The internal clock circuit is completed with the addition of an external 3.579545 MHz crystal.

The counter is still in counting process and helps in latching the number on the corresponding seven segment display. The three digit number of the calling party gets displayed for the counter outputs 0101 H, 0110 H,0111 H respectively. When the counter output is 1000 H, the counting process stops and this ends the receiver operation. The normal conversation then proceeds. The counter is then reset on on-hook condition of the calling party.

The time taken for the reception of the transmitted number is nearly 1 second and the total TTS receiver operation takes place in 2 seconds.

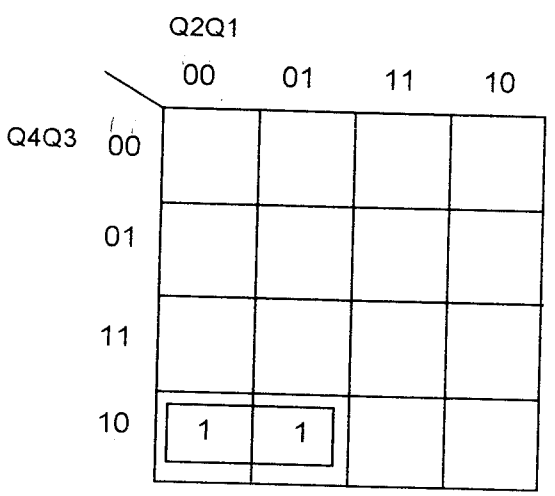
POWER SUPPLY FOR TTS RECEIVER :

The power supply for the TTS receiver is +5 V. It is tapped from 230V ac mains, full wave rectified and fed.

DTMF DECODER OUTPUT TO BCD CONVERSION

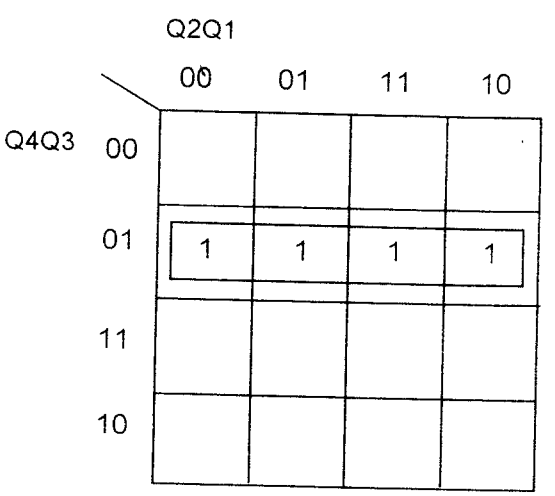
Nos.	DTMF DECODER OUTPUT				REQUIRED BCD OUTPUT			
	Q4	Q3	Q2	Q1	D4	D3	D2	D1
0	1	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	0
3	0	0	1	1	0	0	1	1
4	0	1	0	0	0	1	0	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	0	1	1	0
7	0	1	1	1	0	1	1	1
8	1	0	0	0	1	0	0	0
9	1	0	0	1	1	0	0	1

K-MAP FOR D4



$D4 = \overline{Q2}Q4\overline{Q3}$

K-MAP FOR D3



$D3 = \overline{Q4}Q3$

K-MAP FOR D2

Q4Q3 \ Q2Q1	00	01	11	10
00			1	1
01			1	1
11				
10				

$D2 = \overline{Q4}\ Q2$

K-MAP FOR D1

Q4Q3 \ Q2Q1	00	01	11	10
00		1	1	
01		1	1	
11				
10		1		

$D1 = \overline{Q4}\ Q1 + \overline{Q3}\ \overline{Q2}\ Q1$

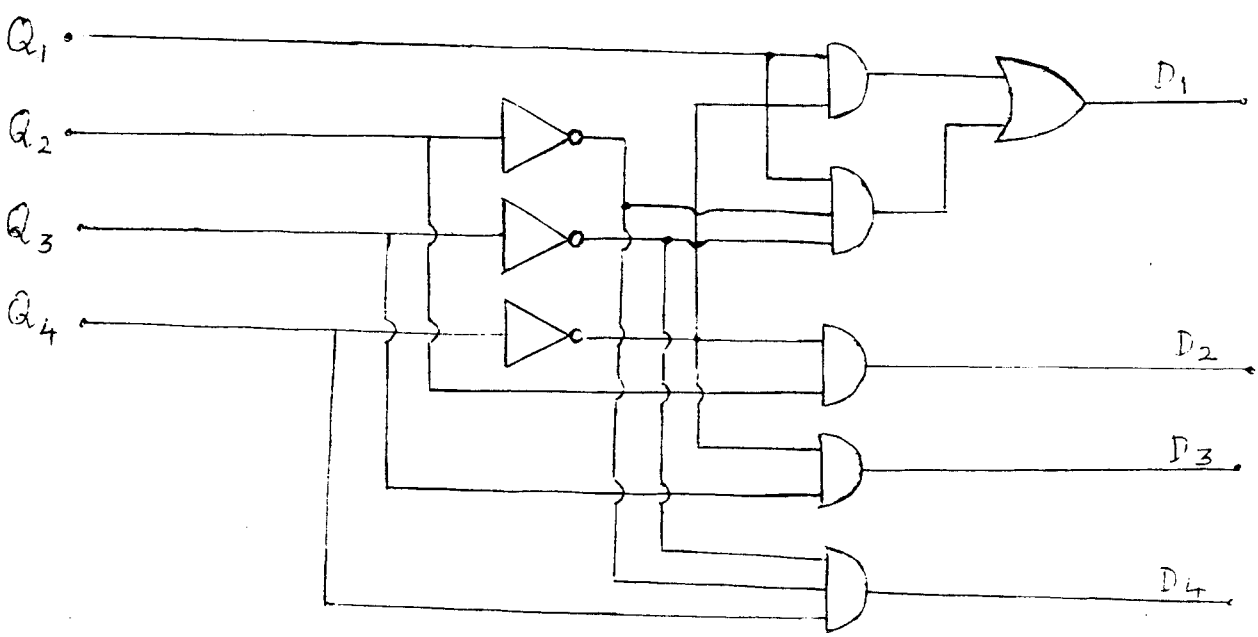


FIG.

OFF - HOOK DETECTION

An off-hook decision circuit is needed in order to detect the ON / OFF hook status of the telephone, since that decides when the telephone should be connected to the exchange.

When the telephone is in on-hook the voltage across the pair of telephone wires is +48 V, and when it goes to off-hook the voltage drops to around 11 V. A comparator is used to sense the changes from 48 V to 11 V and from 11 V to 48 V. To reduce the voltage to the CMOS logic level the resistor divider network is introduced at the input to the negative terminal of LM 324.

BASIC OPERATION OF A COMPARATOR

A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input. It is basically an open loop op-amp with $+V_{sat}$ = Vcc. There are two type of comparators :

1. Non-inverting comparator
2. Inverting comparator.

LM324 PIN CONFIGURATION

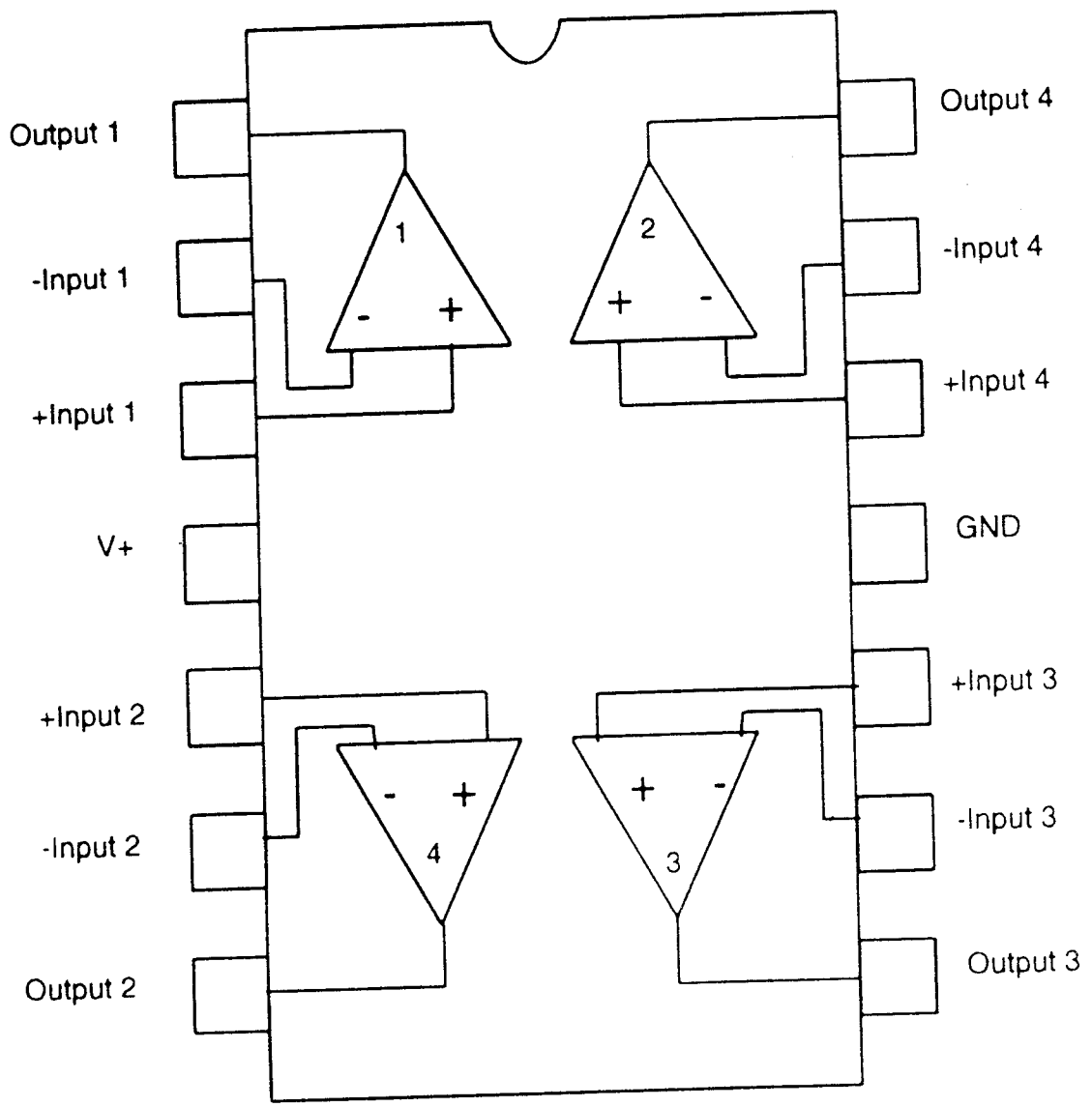


Fig : 14

OFF - HOOK DETECTION

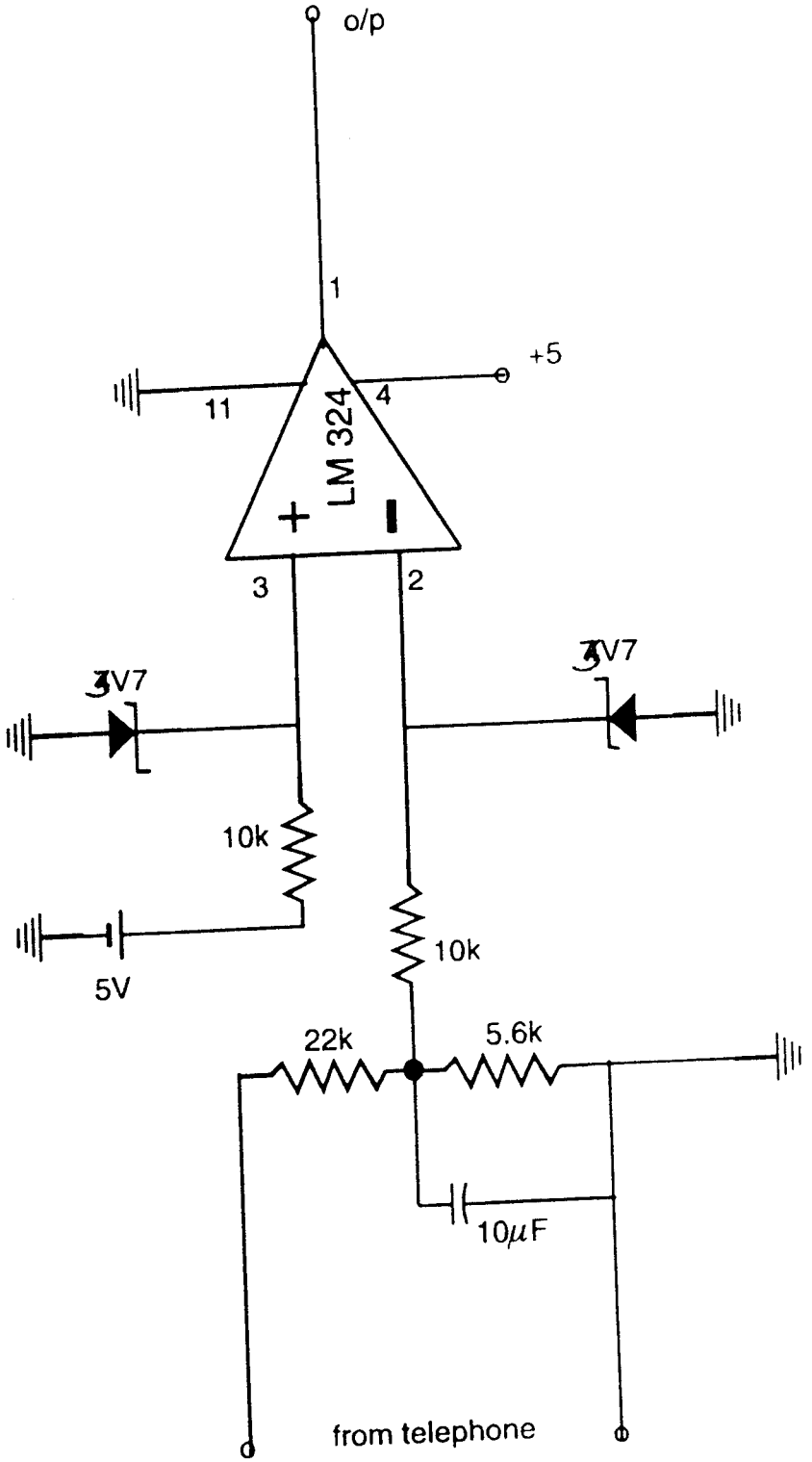


Fig 15

POWER SUPPLY

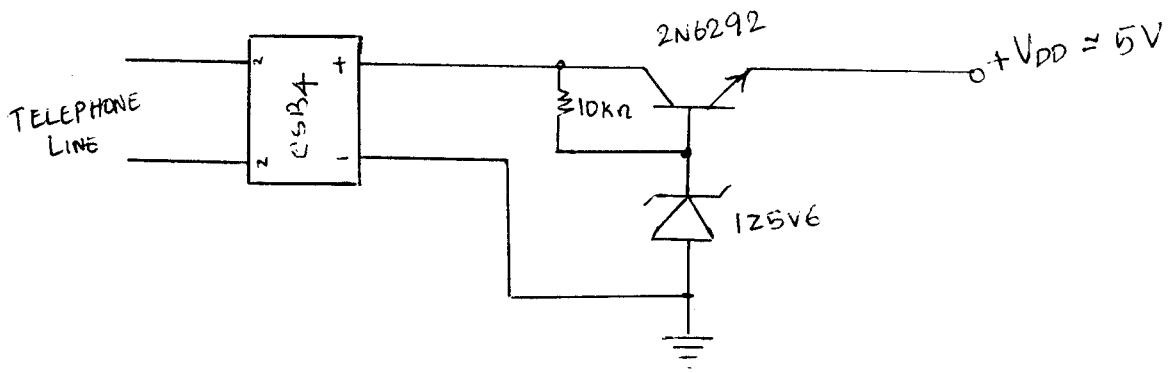


FIG THE POWER SUPPLY.

CSB4 is a monolithic bridge rectifier IC with 4 pins. It is capable of producing a full wave rectified output. The maximum amplitude of the input signal can be upto 400 V.

In this project, the bridge rectifier is connected to 2 wires of the telephone line. As mentioned before the telephone line has a dc of +48 V across it. So the bridge rectifier output is +48 V on on-hook condition.

On off-hook condition the voltage across the lines drops to +11 V. So the bridge rectifier output is +11 V. The

bridge rectifier acts as a full wave rectifier. The connection of this bridge rectifier does not affect the operation of the telephone in any way.

A transmitter of the TTS requires a supply of +5 V to power the integrated circuits. The positive output of the bridge rectifier is connected to the collector pin of the power transistor 2N6292. The base is connected to a 1 Watt Zener diode 1Z5V6. The current limiting to the Zener diode comes through a 10 Kohm resistor which is connected across the collector and base of the power transistor. The output is taken at the emitter pin of the power transistor. The output is roughly +5 V which powers all the integrated circuits in the transmitter.

The output at the emitter pin remains +5 V regardless of whether the telephone is in on-hook / off-hook condition. The power transistor 2N6292 is capable of handling upto 7A of current and a voltage upto 80 V.

CONCLUSION...

CONCLUSION

The project " Telephone Tracking System " has been designed and tested to confirm target specifications.

Details about the integrated circuits, configurations and operations of all the chips used in the hardware implementation has also been explained.

There is also provisions for future developement such as storage of incoming call numbers and dialling the stored number by just pressing a single button which can be provided in the TTS-receiver.

The TTS transmitter can be used in all PCO's and thus any anonymous calls from any PCO can be traced immediately. The transmitter can be installed in houses and if a receiver is also hooked up, the facility of viewing the incoming call number can be availed. This project can be implemented in any EPABX system and in the normal exchange. So this facility can be used in large industries and educational institutions.

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BIBLIOGRAPHY

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4. AN INTRODUCTION TO AUTOMATIC TELEPHONY

   - *Dr. P.N.DAS*

5. TELECOMMUNICATIONS

   - *FRASER*

APPENDIX ...

MITEL

ISO²-CMOS MT8870
Integrated DTMF Receiver

9161-002-031-NA ISSUE 2 January 1985

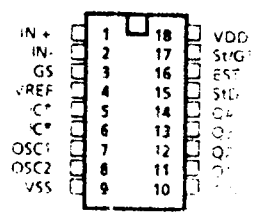
Features

- Complete DTMF receiver
- Low power consumption
- Internal gain setting amplifer
- Adjustable guard time
- Central Office Quality

Applications

- Paging systems
- Repeater systems/mobile radio
- Credit card systems
- Remote Control
- Personal Computers

Pin Connections



*connect to VSS

Ordering Information

MT8870B 18 PIN PLASTIC
MT8870C 18 PIN CERDIP

Description

The MT8870 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions, fabricated in Mitel's double poly ISO²-CMOS technology. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone-pairs into a 4-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched 3-state bus interface

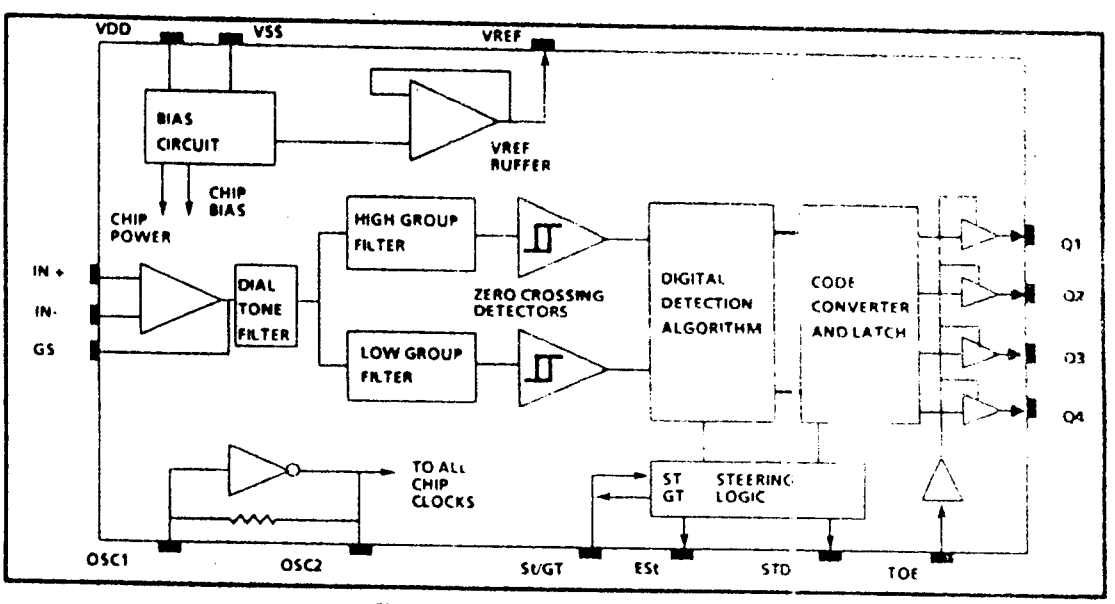


Figure 1. Functional Block Diagram

Operating Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated

Gain Setting Amplifier

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input leakage current	I_{IN}		100		nA	$V_{SS} \le V_{IN} \le V_{DD}$
2	Input resistance	R_{IN}		10		MΩ	
3	Input offset voltage	V_{OS}		25		mV	
4	Power suply rejection	PSRR		60		dB	1 KHz
5	Common mode rejection	CMRR		60		dB	-3.0V ≤ V_{IN} ≤ 3.0V
6	DC open loop voltage gain	A_{VOL}		65		dB	
7	Open loop unity gain bandwidth	f_C		1.5		MHz	
8	Output voltage swing	V_O		4.5		V_{pp}	$R_L \ge 100K\Omega$ to V_{SS}
9	Maximum capacitive load (GS)	C_L		100		pF	
10	Maximum resistive load (GS)	R_L		50		KΩ	
11	Common mode range	V_{CM}		3.0		V_{pp}	No Load

† V_{DD} = 5 V, V_{SS} = 0 V, T_A = 25° C

Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ†	Max	Units	Notes
1	SIGNAL CONDITIONS	Valid input signal levels (each tone of composite signal)		-29			dBm	1,2,3,5,6,9
				27.5			mV_{RMS}	1,2,3,5,6,9
						+1	dBm	1,2,3,5,6,9
						883	mV_{RMS}	1,2,3,5,6,9
2		Positive twist accept			10		dB	2,3,6,9
3		Negative twist accept			10		dB	2,3,6,9
4		Freq. deviation accept		± 1.5% ± 2Hz			Nom.	2,3,5,9
5		Freq. deviation reject		± 3.5%			Nom.	2,3,5,9
6		Third tone tolerance			-16		dB	2,3,4,5,9,10
7		Noise tolerance			-12		dB	2,3,4,5,7,9,10
8		Dial tone tolerance			+22		dB	2,3,4,5,8,9,11

† V_{DD} = 5 V, V_{SS} = 0 , T_A = 25°C and f_C = 3.579545 MHz using test circuit shown in Figure 2

NOTES

1 dBm = decibels above or below a reference power of 1 mW into a 600 ohm load
2 Digit sequence consists of all DTMF tones
3 Tone duration = 40 ms, tone pause = 40 ms
4 Signal condition consists of nominal DTMF frequencies
5 Both tones in composite signal have an equal amplitude
6 Tone pair is deviated by ± 1.5% ± 2Hz
7 Bandwidth limited (3KHz) Gaussian noise
8 The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2 %
9 For an error rate of better than 1 in 10,000
10 Referenced to lowest level frequency component in DTMF signal
11 Referenced to the minimum valid accept level

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	TIMING	Tone present detect time	t_{DP}	5	11	14	ms	see Figure 3
2		Tone absent detect time	t_{DA}	0.5	4	8.5	ms	see Figure 3
3		Tone duration accept	t_{REC}			40	ms	User adjustable
4		Tone duration reject	t_{REC}	20			ms	User adjustable
5		Interdigit pause accept	t_{ID}			40	ms	User adjustable
6		Interdigit pause reject	t_{DO}	20			ms	User adjustable
7	OUTPUTS	Propagation delay (St to Q)	t_{PQ}		8	11	µs	TOE = V_{DD}
8		Propagation delay (St to StD)	t_{PStD}		12		µs	TOE = V_{DD}
9		Output data set up (Q to StD)	t_{QStD}		3.4		µs	TOE = V_{DD}
10		Propagation delay (TOE to Q ENABLE)	t_{PTE}		50		ns	RL = 10KΩ CL = 50 pF
11		Propagation delay (TOE to Q DISABLE)	t_{PTD}		300		ns	RL = 10KΩ CL = 50 pF
26	CLOCK	Crystal /clock frequency	f_C	3.5759	3.5795	3.5831	MHz	
27		Clock input rise time	t_{LHCL}			110	ns	Ext. clock
28		Clock input fall time	t_{HLCL}			110	ns	Ext. clock
29		Clock input duty cycle	DC_{CL}	40	50	60	%	Ext. clock
30		Capacitive load (OSC2)	C_{LO}			30	pF	

†V_{DD} = 5V, V_{SS} = 0V, T_A = 25°C and f_C = 3.579545 MHz, using test circuit in Figure 2

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

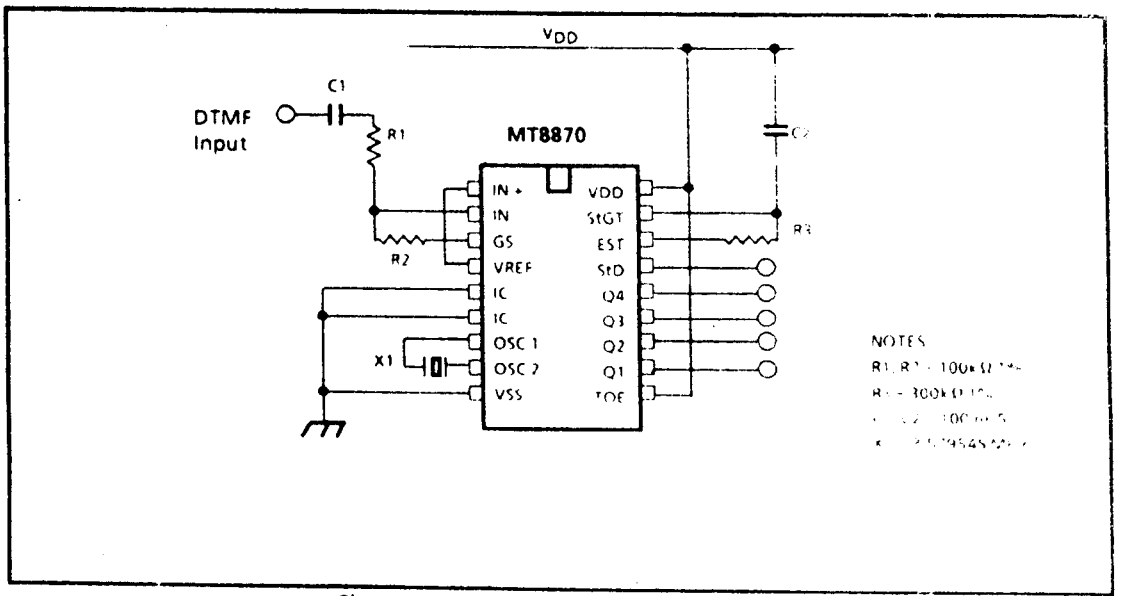
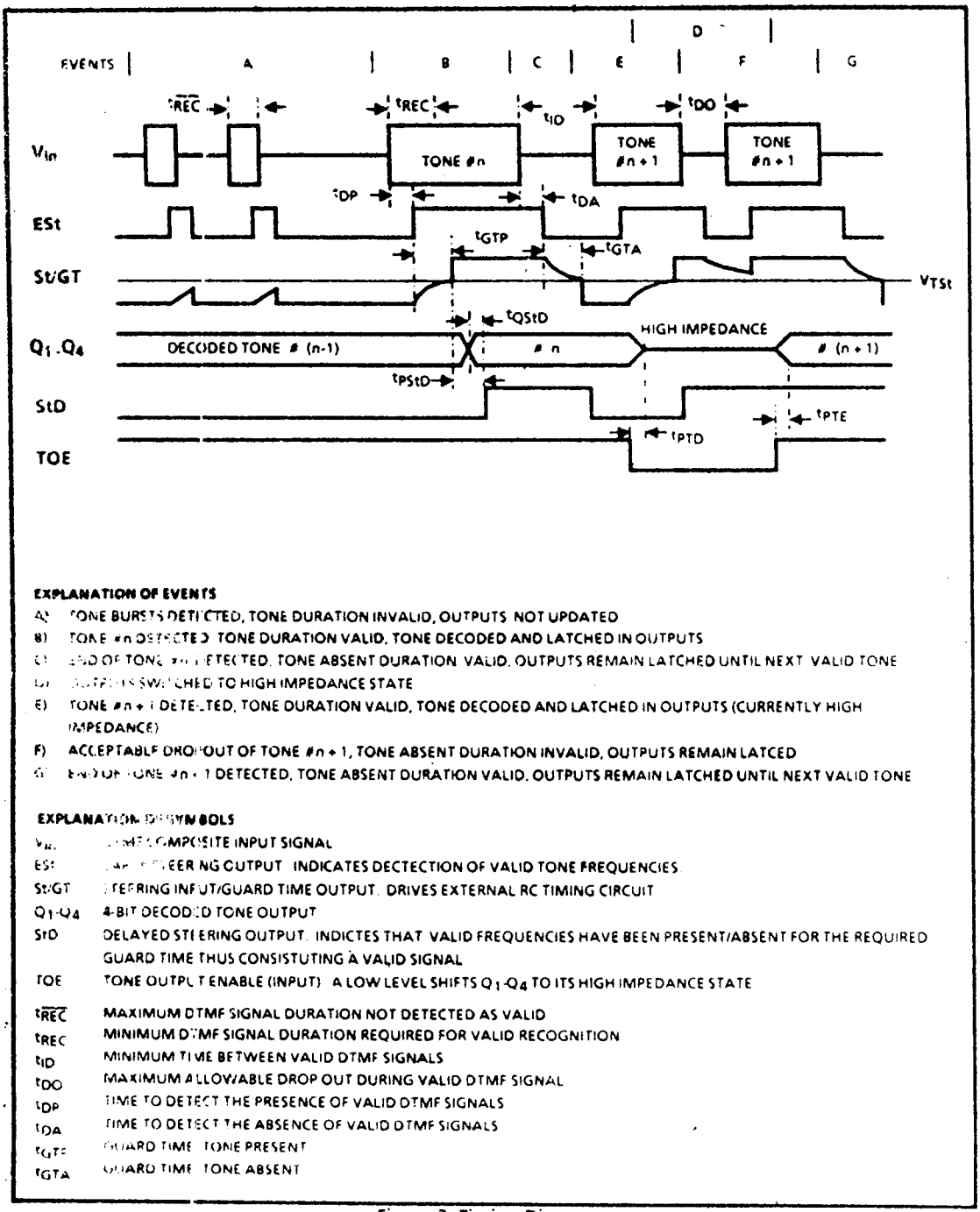


Figure 2. Single Ended Input Configuration

Pin Description

Pin #	Name	Description
1	IN +	Non-inverting op-amp input.
2	IN-	Inverting op-amp input.
3	GS	Gain select. Gives access to output of front end differential amplifier for connection of feedback resistor.
4	V_{REF}	Reference voltage output, nominally $V_{DD}/2$ is used to bias inputs at mid-rail (see Fig.2).
5	IC	Internal connection. Must be tied to V_{SS}.
6	IC	Internal connection. Must be tied to V_{SS}.
7	OSC1	Clock input.
8	OSC2	Clock output. A 3.5795 MHz crystal connected between OSC1 and OSC2 completes the internal oscillator circuit.
9	V_{SS}	Negative power supply input.
10	TOE	3- state output enable (input). Logic high enables the outputs Q1-Q4 [illegible] pull up.
11-14	Q1-Q4	3-state data outputs. When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see Fig. 5).
15	StD	Delayed steering output. Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/Gt falls below V_{TSt}
16	ESt	Early steering output. Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
19	St/GT	Steering input/guard time output (bi-directional). A voltage greater than V_{TS} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
18	V_{DD}	Positive power supply input.



EXPLANATION OF EVENTS

A) TONE BURSTS DETECTED, TONE DURATION INVALID, OUTPUTS NOT UPDATED

B) TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS

C) END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE

D) OUTPUTS SWITCHED TO HIGH IMPEDANCE STATE

E) TONE #n + 1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS (CURRENTLY HIGH IMPEDANCE)

F) ACCEPTABLE DROPOUT OF TONE #n + 1, TONE ABSENT DURATION INVALID, OUTPUTS REMAIN LATCED

G) END OF TONE #n + 1 DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE

EXPLANATION OF SYMBOLS

V_{in}	DTMF COMPOSITE INPUT SIGNAL
ESt	EARLY STEERING OUTPUT. INDICATES DECTECTION OF VALID TONE FREQUENCIES
St/GT	STEERING INPUT/GUARD TIME OUTPUT. DRIVES EXTERNAL RC TIMING CIRCUIT
Q_1-Q_4	4-BIT DECODED TONE OUTPUT
StD	DELAYED STEERING OUTPUT. INDICTES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME THUS CONSISTUTING A VALID SIGNAL
TOE	TONE OUTPUT ENABLE (INPUT). A LOW LEVEL SHIFTS Q_1-Q_4 TO ITS HIGH IMPEDANCE STATE
$t_{\overline{REC}}$	MAXIMUM DTMF SIGNAL DURATION NOT DETECTED AS VALID
t_{REC}	MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION
t_{ID}	MINIMUM TIME BETWEEN VALID DTMF SIGNALS
t_{DO}	MAXIMUM ALLOWABLE DROP OUT DURING VALID DTMF SIGNAL
t_{DP}	TIME TO DETECT THE PRESENCE OF VALID DTMF SIGNALS
t_{DA}	TIME TO DETECT THE ABSENCE OF VALID DTMF SIGNALS
t_{GTP}	GUARD TIME, TONE PRESENT
t_{GTA}	GUARD TIME, TONE ABSENT

Figure 3. Timing Diagram

Functional Description

The MT8870 monolithic DTMF receiver offers small size, low power consumption and high performance. Its architecture consists of a bandsplit filter section, which seperates the high and low group tones, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Filter Section

Seperation of the low-group and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor band pass filters, the band-widths of which correspond to the low and high group frequencies. The filter section also incorporates notches at 350 and 440 Hz for exceptional dial tone rejection (see Fig. 4). Each filter output is followed by a single order switched capacitor filter section which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

Decoder Section

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications) the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state (see "Steering Circuit").

Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes v_c (see Fig. 6) to rise as the capacitor discharges.

Provided signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), v_c reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, latching its corresponing 4-bit code (see Fig. 5) into the output latch. At this point the GT output is activated and drives v_c to VDD. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag (StD) goes high, signalling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three state control input (TOE) to a logic high. The steering circuit works in reverse to

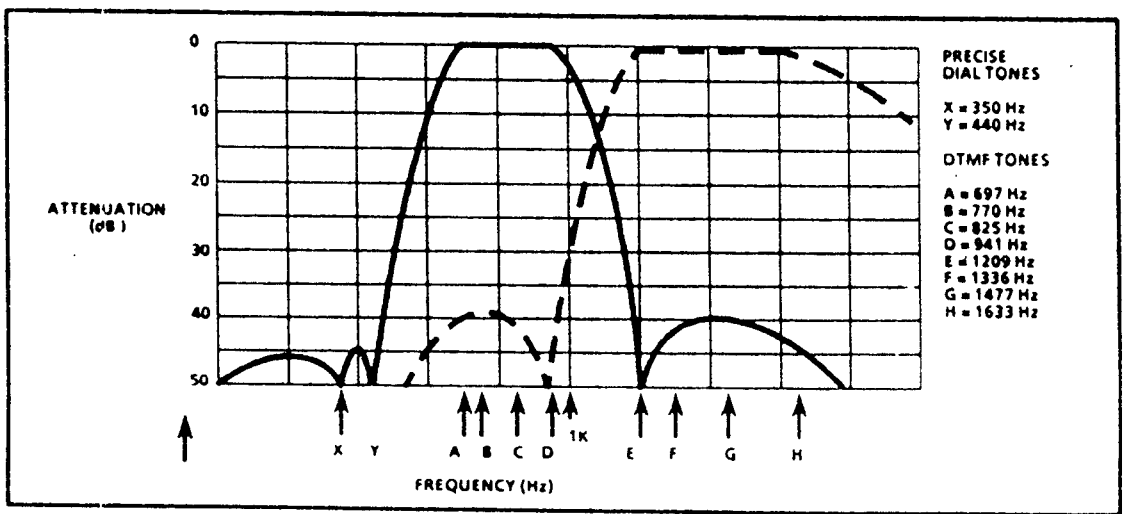


Figure 4. Filter Response

f_{LOW}	f_{HIGH}	NO	TOE	Q_4	Q_3	Q_2	Q_1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1336	0	H	1	0	1	0
941	1209	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
		ANY	L	Z	Z	Z	Z

L = LOGIC LOW, H = LOGIC HIGH, Z = HIGH IMEDANCE

Figure 5. Functional Decode Table

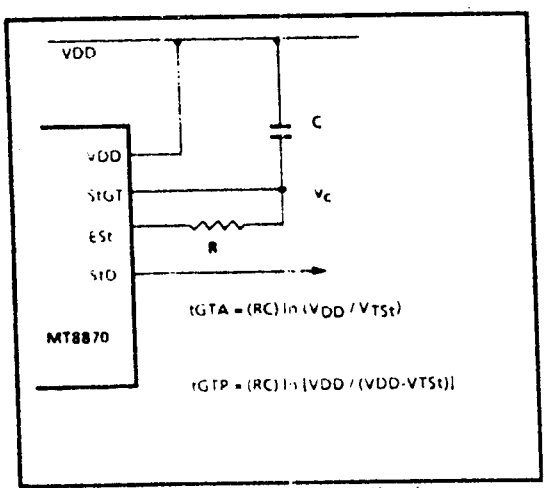


Figure 6. Basic Steering Circuit

validate the interdigit pause between signals. Thus, as well as rejecting signals too short too be considered valid, the receiver will tolerate signal interruptions (drop out) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

In many situations not requiring selection of tone duration and interdigital pause, the simple steering circuit shown in Fig. 6 is applicable. Component values are chosen according to the formula:

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{ID} = t_{DA} + t_{GTA}$$

The value of t_{DP} is a device parameter (see table) and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 μF is recommended for most applications, leaving R to be selected by the designer.

Different steering arrangements may be used to select independantly the guard times for tone present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigital pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity. Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast aquisition time and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figure 7.

Differential Input Configuration

The input arrangement of the MT8870 provides a differential-input operational amplifier as well as a bias source(V_{Ref}) which is used to bias the inputs at mid-rail. Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain. In a single-ended configuration, the input pins are connected as shown in Fig. 2 with the op-amp connected for unity gain and V_{Ref} biasing the input at $\frac{1}{2}V_{DD}$. Fig. 8 shows the differential configuration, which permits the

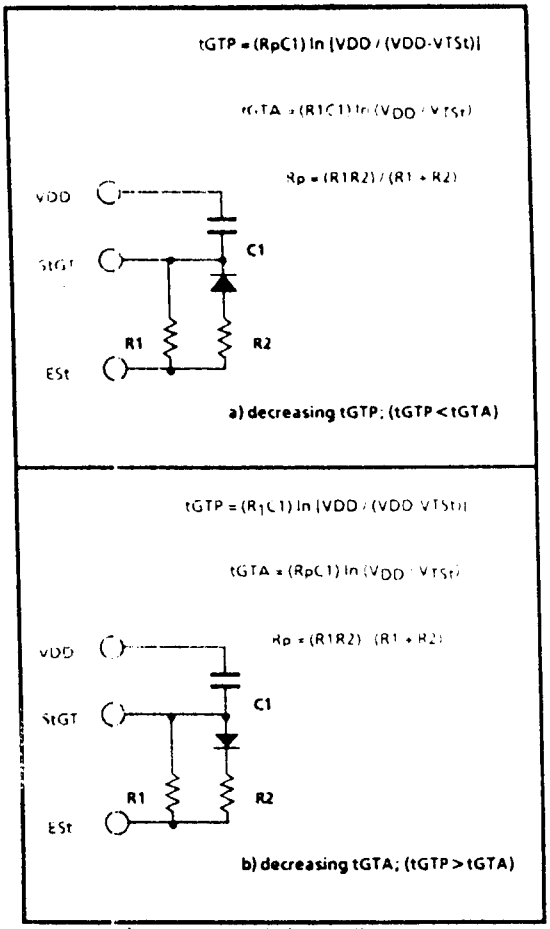


Figure 7. Guard Time Adjustment

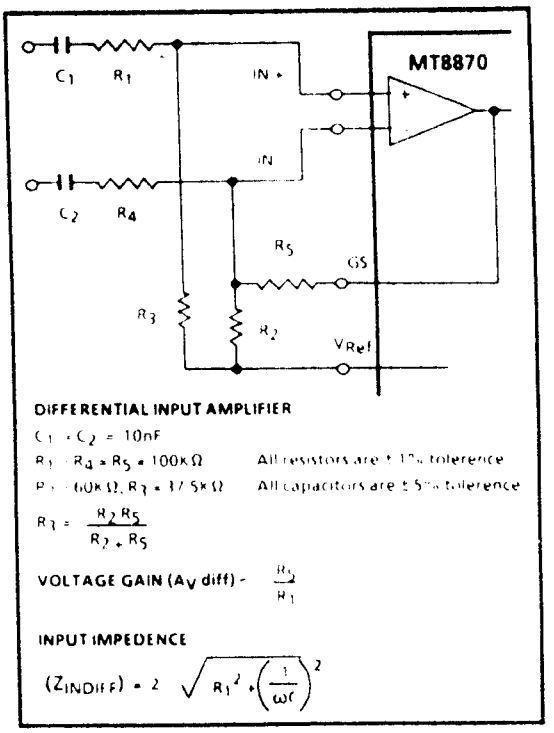


Figure 8. Differential Input Configuration

adjustment of gain with the feedback resistor R_5

Crystal Oscillator

The internal clock circuit is completed with the addition of an external 3.58 MHz crystal and is normally connected as shown in Figure 2 (Single Ended Input Configuration). However, it is possible to configure several MT8870 devices employing only a single oscillator crystal. The oscillator output of the first device in the chain is coupled through a 30 pF capacitor to the oscillator input (OSC1) of the next device. Subsequent devices are connected in a similar fashion. Refer to Fig. 9 for details. The problems associated with unbalanced loading are not a concern with the arrangement shown, ie, precision balancing capacitors are not required.

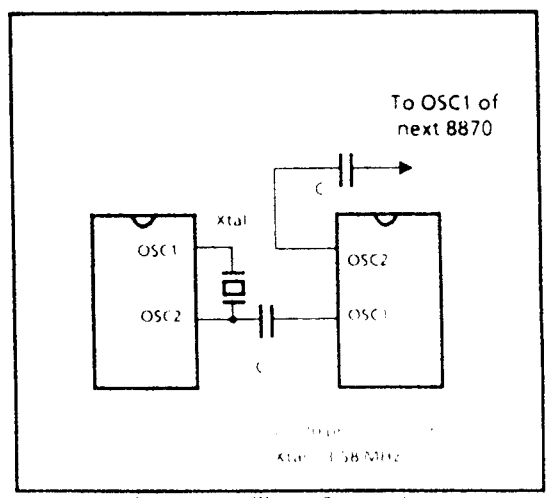


Figure 9. Oscillator Connection

CD4555B, CD4556B Types

CMOS
Dual Binary to 1 of 4 Decoder/Demultiplexers

High-Voltage Types (20-Volt Rating)

CD4555B: Outputs High on Select
CD4556B: Outputs Low on Select

The RCA-CD4555B and CD4556B are dual one-of-four decoders/demultiplexers. Each decoder has two select inputs (A and B), an Enable input ($\overline{E}$), and four mutually exclusive outputs. On the CD4555B the outputs are high on select; on the CD4556B the outputs are low on select.

When the Enable input is high, the outputs of the CD4555B remain low and the outputs of the CD4556B remain high regardless of the state of the select inputs A and B. The CD4555B and CD4556B are similar to types MC14555 and MC14556, respectively.

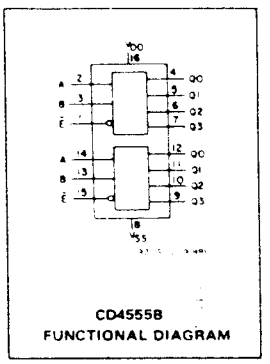
The CD4555B and CD4556B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix)

Features:

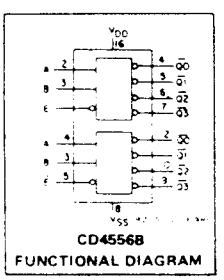
- Expandable with multiple packages
- Standard, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range): 1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Decoding
- Code conversion
- Demultiplexing (using Enable input as a data input)
- Memory chip-enable selection
- Function selection



CD4555B
FUNCTIONAL DIAGRAM



CD4556B
FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS

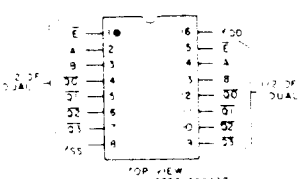
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{DD}	MIN.	MAX.	UNITS
Supply Voltage Range (For T_A = Full Package Temp. Range)	–	3	18	V

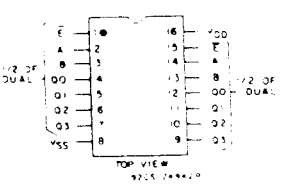
MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	-0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D)	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A)	
PACKAGE TYPES D, F, K, H	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max	+265°C

TERMINAL ASSIGNMENTS



CD45568



CD4555B

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, K, H Packages Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150		0.04	5	μA
	–	0,10	10	10	10	300	300		0.04	10	
	–	0,15	15	20	20	600	600		0.04	20	
	–	0,20	20	100	100	3000	3000		0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1		mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6		
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8		
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1		
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2		
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6		
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8		
Output Voltage Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5		
	–	0,10	10	9.95				9.95	10		
	–	0,15	15	14.95				14.95	15		
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	±10^−5	±0.1	μA

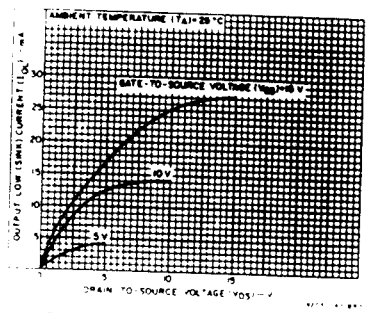


Fig. 1 – Typical output low (sink) current characteristics.

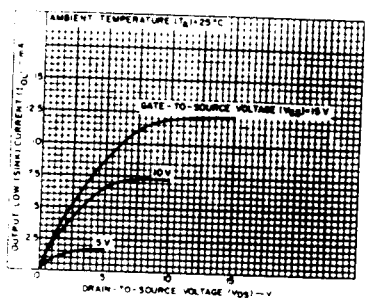


Fig. 2 – Minimum output low (sink) current characteristics.

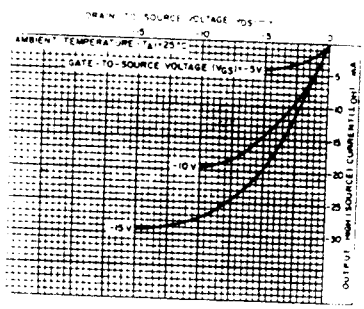


Fig. 3 – Typical output high (source) current characteristics.

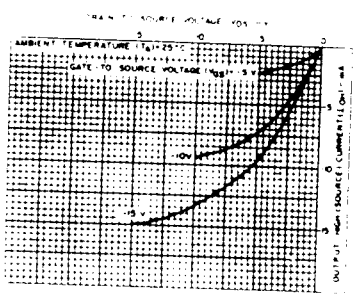


Fig. 4 – Minimum output high (source) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ*

CHARACTERISTIC	TEST CONDITIONS	ALL TYPES LIMITS			UNITS
		V_{DD} Volts	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH} A or B Input to Any Output		5	220	440	ns
		10	95	190	
		15	70	140	
$\overline{E}$ Input to Any Output		5	200	400	ns
		10	85	170	
		15	65	130	
Transition Time t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance C_{IN}	Any Input		5	7.5	pF

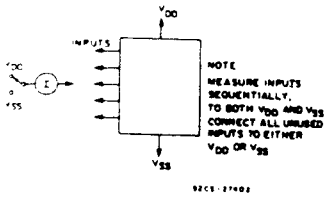


Fig. 14 – Input current test circuit.

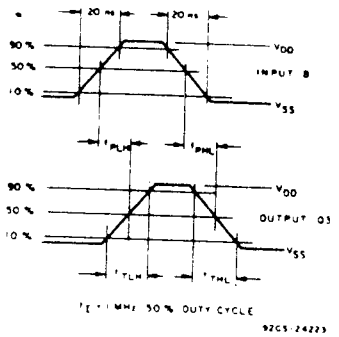


Fig. 15 – CD4555B B input to Q3 output dynamic signal waveforms.

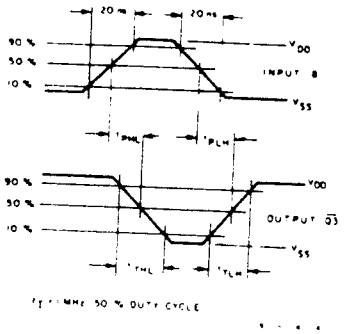


Fig. 16 – CD4556B B input to $\overline{Q3}$ output dynamic signal waveforms.

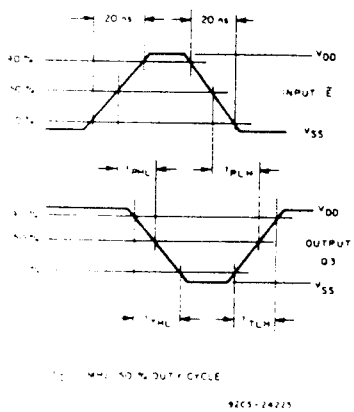


Fig. 17 – CD4555B $\overline{E}$ input to Q3 output dynamic signal waveforms.

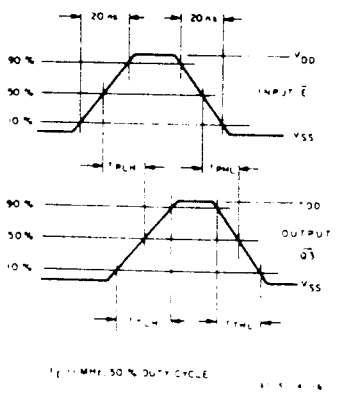
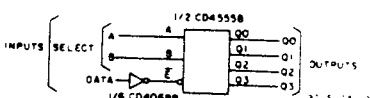


Fig. 18 – CD4556B $\overline{E}$ input to $\overline{Q}_3$ output dynamic signal waveforms.

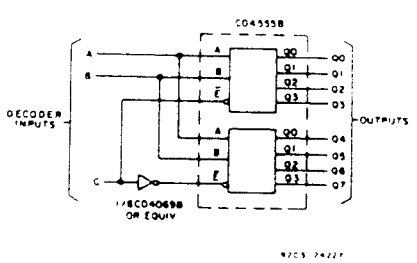
APPLICATIONS



TRUTH TABLE

SELECT INPUTS		OUTPUTS			
B	A	Q0	Q1	Q2	Q3
0	0	DATA	0	0	0
0	1	0	DATA	0	0
1	0	0	0	DATA	0
1	1	0	0	0	DATA

Fig. 19 – 1-of-4 line data demultiplexer using CD4555B.



TRUTH TABLE

INPUTS			Q OUTPUTS							
C	B	A	0	1	2	3	4	5	6	7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Fig. 20 – 1-of-8 decoder using CD4555B.

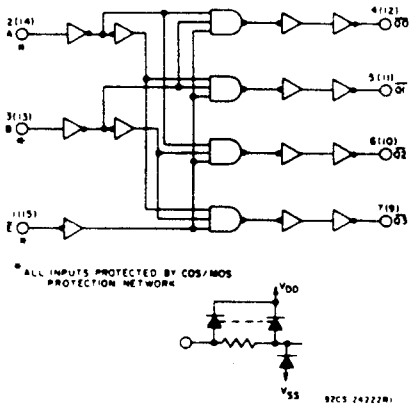


Fig. 5 – CD4556B logic diagram (1 of 2 identical circuits).

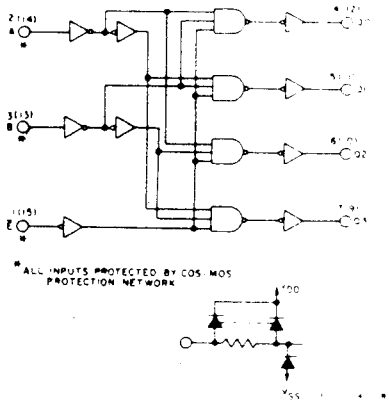


Fig. 6 – CD4555B logic diagram (1 of 2 identical circuits).

TRUTH TABLE

INPUTS ENABLE	SELECT		OUTPUTS CD4555B				OUTPUTS CD4556B			
$\overline{E}$	B	A	Q3	Q2	Q1	Q0	$\overline{Q3}$	$\overline{Q2}$	$\overline{Q1}$	$\overline{Q0}$
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X = DON'T CARE

LOGIC 1 ≡ HIGH
LOGIC 0 ≡ LOW

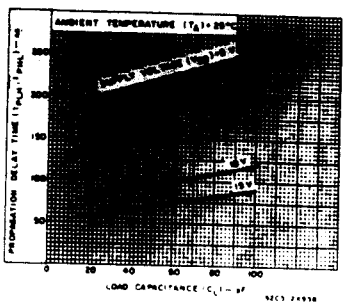


Fig. 7 – Typical propagation delay time vs. load capacitance (A or B input to any output).

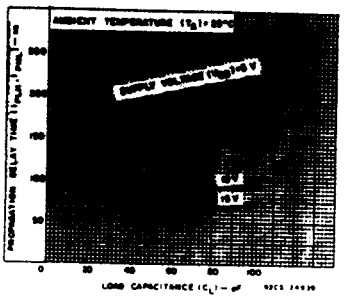


Fig. 8 – Typical propagation delay time vs. load capacitance ($\overline{E}$ input to any output).

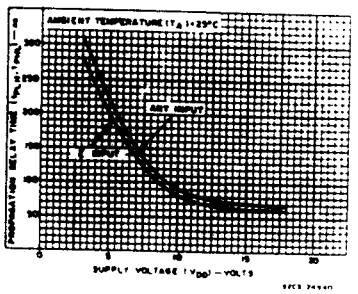


Fig. 9 – Typical propagation delay time vs. supply voltage.

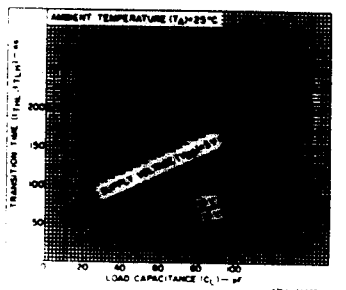


Fig. 10 – Typical transition time vs. load capacitance.

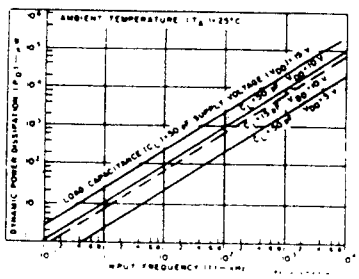


Fig. 11 – Typical dynamic power dissipation vs. frequency.

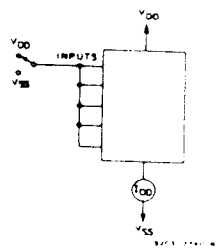


Fig. 12 – Quiescent device current test circuit.

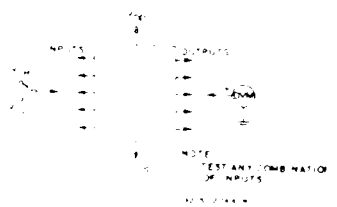
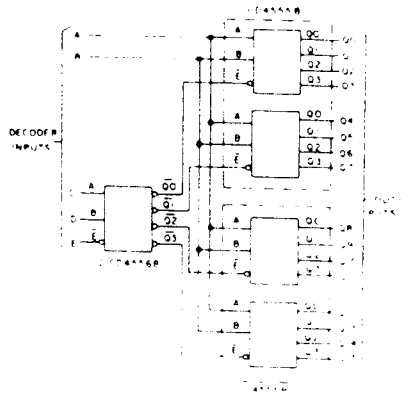


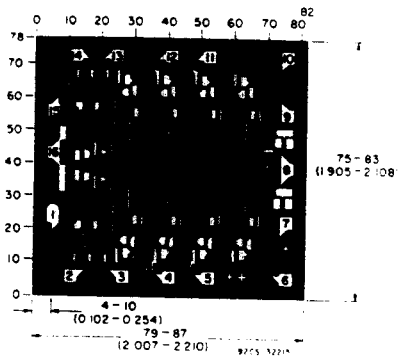
Fig. 13 – [illegible]



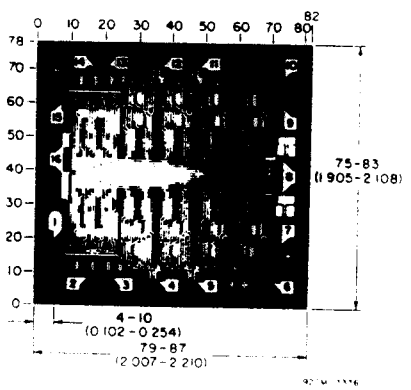
TRUTH TABLE

INPUTS					OUTPUTS													
E	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fig. 21 — 1 of 16 decoder using CD4555B and CD4556B.



DIMENSIONS AND PAD LAYOUT FOR CD4555BH.



DIMENSIONS AND PAD LAYOUT FOR CD4556BH.

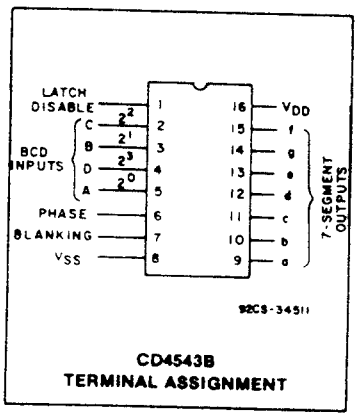
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10⁻³ inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip therefore may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.

CMOS BCD-to-Seven-Segment Latch/Decoder/Driver For Liquid-Crystal Displays

High-Voltage Types (20-Volt Rating)

Features:
- *Display blanking of all illegal input combinations*
- *Latch storage of code*
- *Capability of driving two low power TTL loads, two HTL loads, or one low power Schottky load over the full rated-temperature range*
- *Pin-for-pin replacement for the CD4056B (with pin 7 tied to V_{SS})*
- *Direct LED driving capability*



CD4543B TERMINAL ASSIGNMENT

The RCA-CD4543B is a BCD-to-seven segment latch/decoder/driver designed primarily for liquid-crystal display (LCD) applications. It is also capable of driving light emitting diode (LED), incandescent, gas-discharge, and fluorescent displays. This device is functionally similar to and serves as direct replacement for the CD4056B when pin 7 is connected to V_{SS}. It differs from the CD4056B in that it has a display blanking capability instead of a level-shifting function and requires only one power supply. When the CD4056B is used in the level shifting mode, two power supplies are required. When the CD4543B is used for LCD applications, a square wave must be applied to the PHASE input and the backplane of the LCD device. For LED applications a logic 1 is required at the PHASE input for common-cathode devices; a logic 0 is required for common-anode devices (see truth table).

The CD4543B is supplied in hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

- *100% tested for quiescent current at 20 V*
- *Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C*
- *Noise margin (full package-temperature range)= 1 V at V_{DD}=5 V*
  2 V at V_{DD}=10 V
  2.5 V at V_{DD}=15 V
- *5-V, 10-V, and 15-V parametric ratings*
- *Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"*

Applications:
- *Instrument display driver*
- *Dashboard display driver*
- *Computer/calculator display driver*
- *Timing device driver (clocks, watches, timers)*

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	-0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:	
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max	+265°C

CD4543B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D, F, K, H Packages Values at -40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current Max. I_{DD}	—	0, 5	5	5	5	150	150	—	0.04	5	μA
	—	0,10	10	10	10	300	300	—	0.04	10	
	—	0,15	15	20	20	600	600	—	0.04	20	
	—	0,20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current Min. I_{OL}	0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current Min. I_{OH}	4.6	0, 5	5	-0.46	-0.44	-0.30	-0.26	-0.37	-0.75	—	
	2.5	0, 5	5	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	9.5	0,10	10	-0.98	-0.92	-0.68	-0.55	-0.8	-1.6	—	
	13.5	0,15	15	-3.33	-3.18	-2.2	-1.9	-2.7	-5.4	—	
Output Voltage: Low-Level Max. V_{OL}	—	0, 5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level Min. V_{OH}	—	0, 5	5	4.95				4.95	5	—	
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage Max. V_{IL}	0.5,4.5	—	5	1.5				—	—	1.5	V
	1, 9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage Min. V_{IH}	0.5,4.5	—	5	3.5				3.5	—	—	
	1, 9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current Max. I_{IN}	—	0,18	18	±0.1	±0.1	±1	±1	—	$±10^{-5}$	±0.1	μA

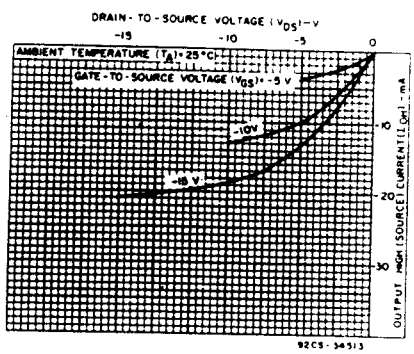


Fig. 2 - Typical output high (source) current characteristics.

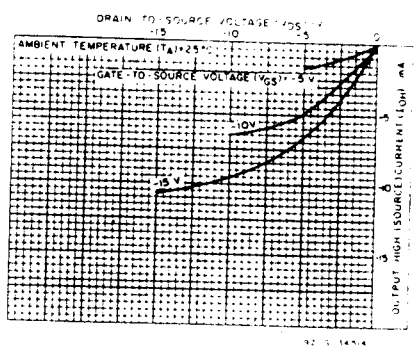


Fig. 3 - Minimum output high (source) current characteristics.

CD4543B Types

TRUTH TABLE FOR CD4543B

INPUT CODE							OUTPUT STATE							DISPLAY CHARACTER
LD	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	
X	1	0	X	X	X	X	0	0	0	0	0	0	0	
1	0	0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	0	0	1	1	1	1	1	1	0	0	1	3
1	0	0	0	1	0	0	0	1	1	0	0	1	1	4
1	0	0	0	1	0	1	1	0	1	1	0	1	1	5
1	0	0	0	1	1	0	1	0	1	1	1	1	1	6
1	0	0	0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	0	0	1	1	1	1	1	0	1	1	9
1	0	0	1	0	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	0	1	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	1	0	0	0	0	0	0	0	Blank
0	0	0	X	X	X	X	••							••
†	†	1	†				Inverse of Output Combinations Above							Display as above

X=Don't care.

†=Above combinations.

*=For liquid-crystal readouts, apply a square wave to Ph.
For common cathode LED readouts, select Ph=0.
For common anode LED readouts, select Ph=1.

**=Depends upon the BCD code previously applied when LD=1.

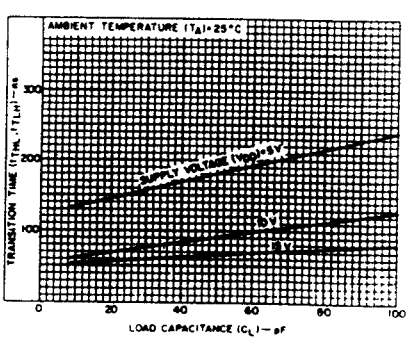


Fig. 7 - Typical transition time as a function of load capacitance.

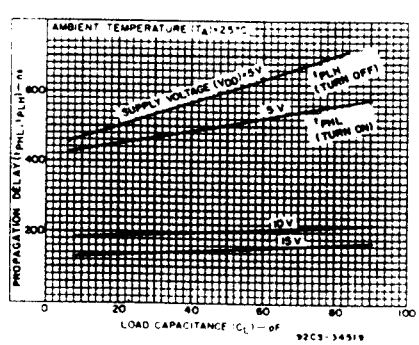


Fig. 8 - Typical propagation delay time as a function of load capacitance.

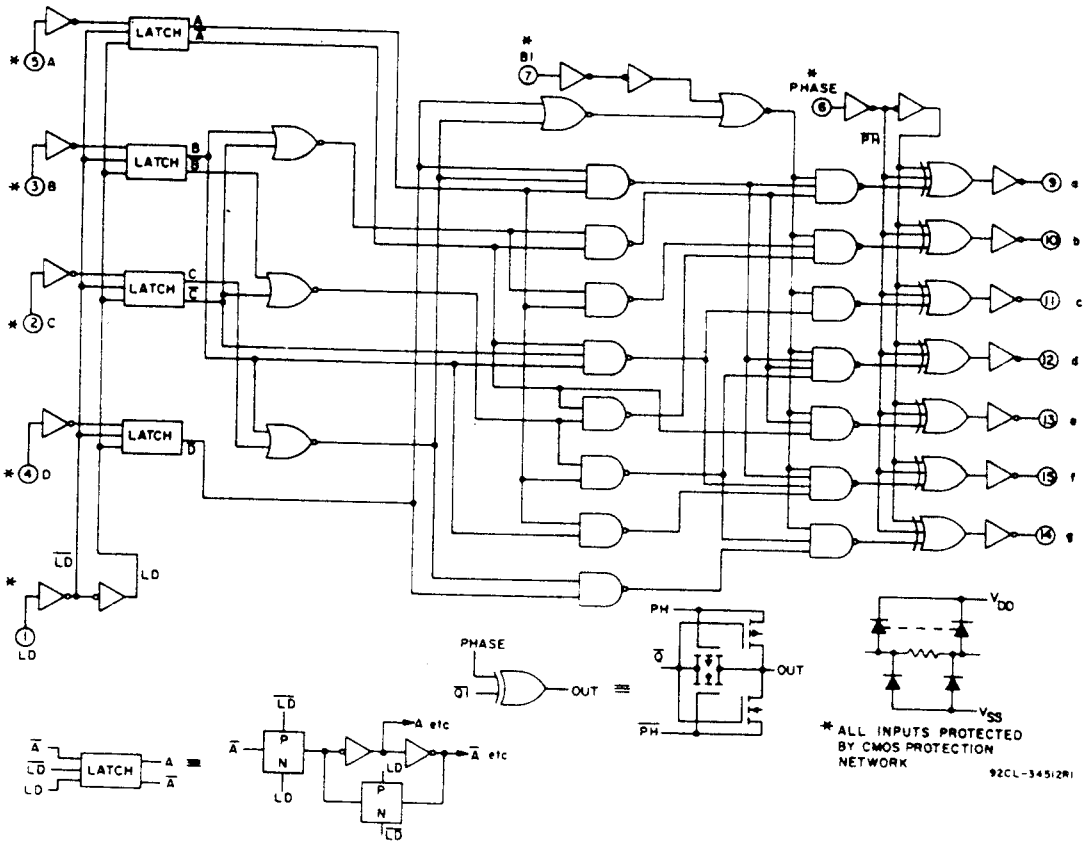


Fig. 1 - BCD-to-seven-segment latch/decoder/driver CD4543B logic circuit diagram.

RECOMMENDED OPERATING CONDITIONS at T_A=25°C, Unless Otherwise Specified
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		V_{DD} (V)	LIMITS MIN.	LIMITS TYP.	UNITS
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		—	3	18	V
Latch Disable Pulse Width	t_{WH}	5	250	125	ns
		10	100	50	
		15	80	40	
Minimum Data Setup Time	t_{SU}	5	60	15	
		10	20	-5	
		15	10	-5	
Minimum Data Hold Time	t_H	5	25	-5	
		10	20	10	
		15	20	10	

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C; C_L=50 pF, Input t_r,t_f=20 ns, R_L=200 kΩ

CHARACTERISTIC		TEST CONDITIONS V_{DD} (V)	LIMITS All Packages MIN.	TYP.	MAX.	UNITS
Propagation Delay Time	t_{PHL}	5	—	600	1200	ns
		10	—	200	400	
		15	—	150	300	
	t_{PLH}	5	—	500	1000	
		10	—	200	400	
		15	—	150	300	
Transition Time	t_{THL}	5	—	180	360	
		10	—	90	180	
		15	—	65	130	
	t_{TLH}	5	—	180	360	
		10	—	90	180	
		15	—	65	130	
Latch Disable Pulse Width	t_{WH}	5	250	125	—	
		10	100	50	—	
		15	80	40	—	
Address Setup Time	t_{SU}	5	60	15	—	
		10	20	-5	—	
		15	10	-5	—	
Address Hold Time	t_H	5	25	-5	—	
		10	20	10	—	
		15	20	10	—	
Input Capacitance	C_{IN}	Any Input	—	5	7.5	pF

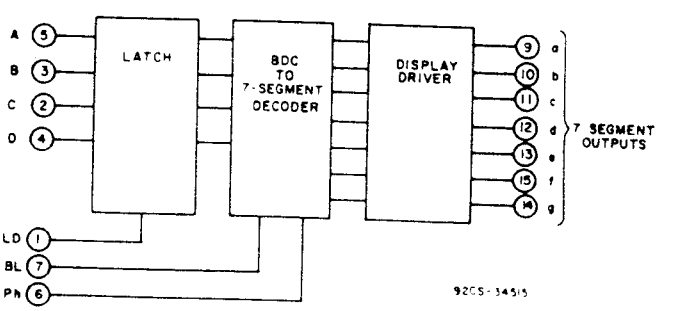


Fig. 4 - BCD-to-seven-segment latch/decoder/driver functional diagram.

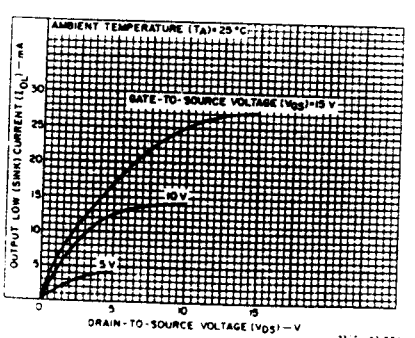


Fig. 5 - Typical output low (sink) current characteristics.

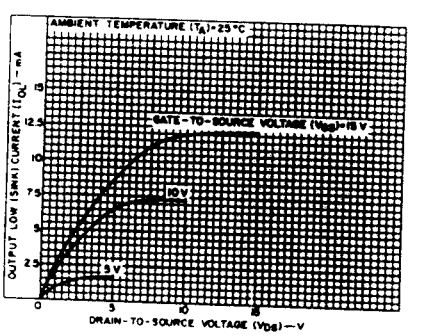


Fig. 6 - Minimum output low (sink) current characteristics.

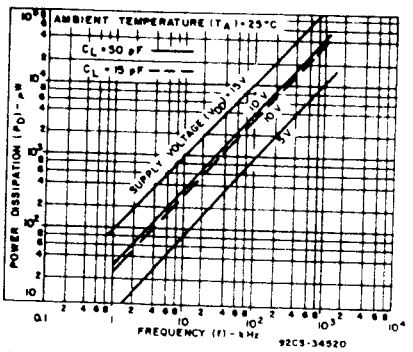


Fig. 9 - Typical dynamic power dissipation as a function of frequency.

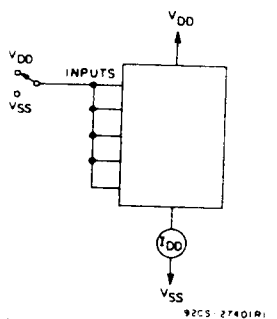


Fig. 10 - Quiescent device current test circuit.

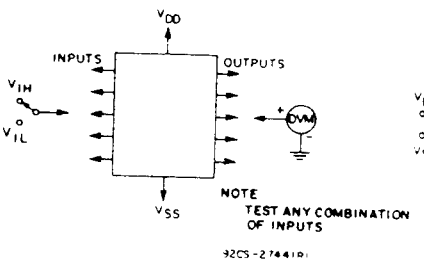


Fig. 11 - Input voltage test circuit.

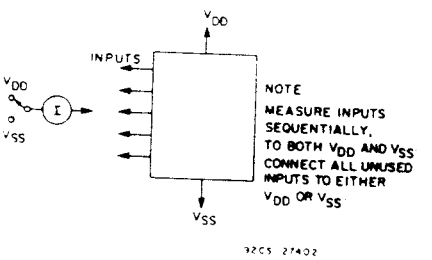
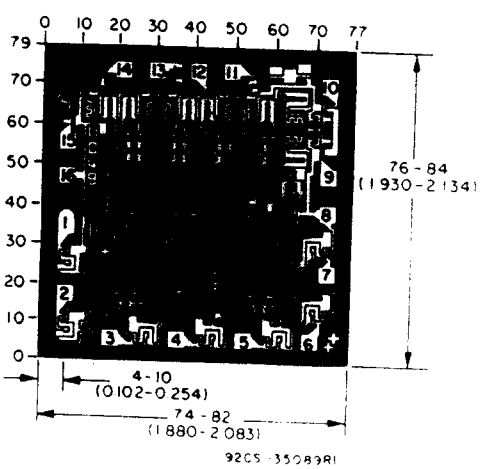


Fig. 12 - Input current test circuit.



Dimensions and pad layout for CD4543BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to +16 mils applicable to the nominal dimensions shown.

National Semiconductor

LM567/LM567C Tone Decoder

General Description

The LM567 and LM567C are general purpose tone decoders designed to provide a saturated transistor switch to ground when an input signal is present within the passband. The circuit consists of an I and Q detector driven by a voltage controlled oscillator which determines the center frequency of the decoder. External components are used to independently set center frequency, bandwidth and output delay.

Features

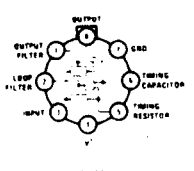
- 20 to 1 frequency range with an external resistor
- Logic compatible output with 100 mA current sinking capability
- Bandwidth adjustable from 0 to 14%
- High rejection of out of band signals and noise
- Immunity to false signals
- Highly stable center frequency
- Center frequency adjustable from 0.01 Hz to 500 kHz

Applications

- Touch tone decoding
- Precision oscillator
- Frequency monitoring and control
- Wide band FSK demodulation
- Ultrasonic controls
- Carrier current remote controls
- Communications paging decoders

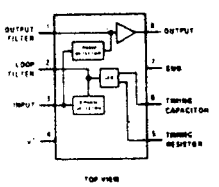
Schematic and Connection Diagrams

Metal Can Package

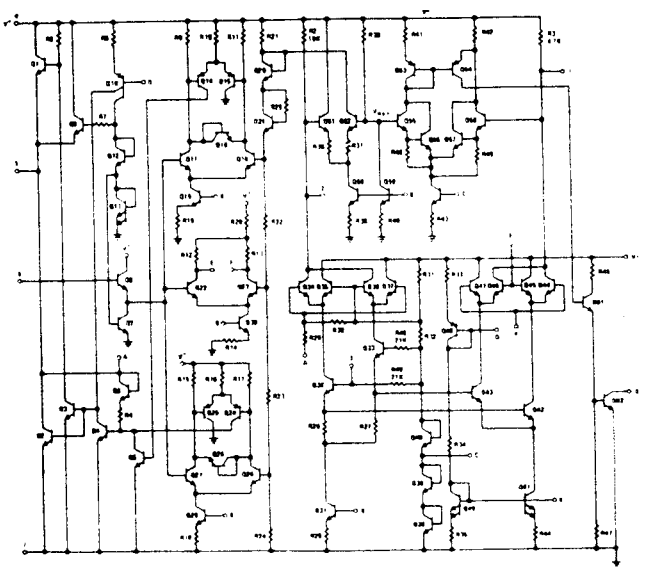


Order Number LM567H or LM567CH
See NS Package H08C

Dual-In-Line Package



Order Number LM567CN
See NS Package N08B



Absolute Maximum Ratings

Supply Voltage Pin	10V
Power Dissipation (Note 1)	300 mW
V_8	15V
V_3	−10V
V_3	V_8 + 0.5V
Storage Temperature Range	−65°C to +150°C

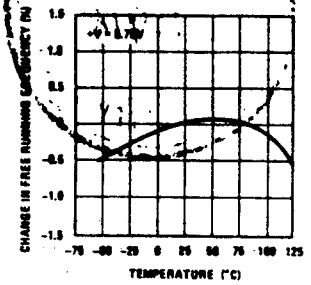
Electrical Characteristics (AC Test Circuit, T_A = 25°C, V_C = 5V)

PARAMETERS	CONDITIONS	LM567			LM567C/LM567CN			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Power Supply Voltage Range		4.75	5.0	9.0	4.75	5.0	9.0	V
Power Supply Current	R_L = 20k							
Quiescent			6	8		7	10	mA
Power Supply Current	R_L = 20k							
Activated			11	13		12	15	mA
Input Resistance		18	20	22	15	20	25	kΩ
Smallest Detectable Input Voltage	I_L = 100 mA, $f_i = f_o$		20	25		20	25	mVrms
Largest No Output Input Voltage	I_C = 100 mA, $f_i = f_o$	10	15		10	15		mVrms
Largest Simultaneous Outband Signal to Inband Signal Ratio			6			6		dB
Minimum Input Signal to Wideband Noise Ratio	B_n = 140 kHz		-6			-6		dB
Largest Detection Bandwidth		12	14	16	10	14	18	% of f_o
Largest Detection Bandwidth Skew			1	2		2	3	% of f_o
Largest Detection Bandwidth Variation with Temperature			±0.1	0.25		±0.1	0.5	%/°C
Largest Detection Bandwidth Variation with Supply Voltage	4.75V – 6.75V		±1	±2		±1	±5	%/V
Highest Center Frequency		100	500		100	500		kHz
Center Frequency Stability	$0 < T_A < 70$		35 ± 60			35 ± 60		ppm/°C
	$-55 < T_A < +125$		35 ± 140			35 ± 140		ppm/°C
Center Frequency Shift with Supply Voltage	4.75V – 6.75V		0.5	1.0		0.4	2.0	%/V
Fastest ON-OFF Cycling Rate			f_o/20			f_o/20		
Output Leakage Current	V_8 = 15V		0.01	25		0.01	25	μA
Output Saturation Voltage	e_i = 25 mV, I_8 = 30 mA		0.2	0.4		0.2	0.4	V
	e_i = 25 mV, I_8 = 100 mA		0.6	1.0		0.6	1.0	
Output Fall Time			30			30		
Output Rise Time			150			150		

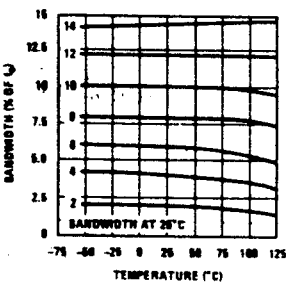
Note 1: The maximum junction temperature of the LM567 is 150°C, while that of the LM567C and LM567CN is For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resist 150°C/W, junction to ambient or 45°C/W, junction to case. For the DIP the device must be derated based on resistance of 187°C/W, junction to ambient.

Typical Performance Characteristics

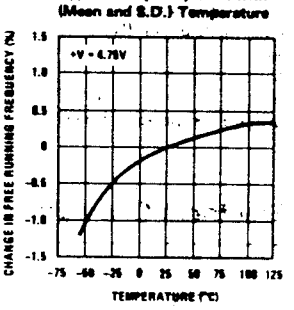
Typical Frequency Drift with Temperature (Mean and S.D.)



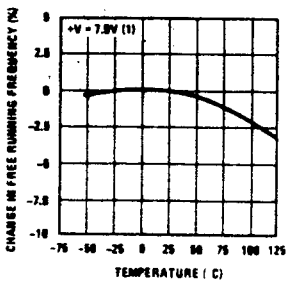
Typical Bandwidth Variation with Temperature



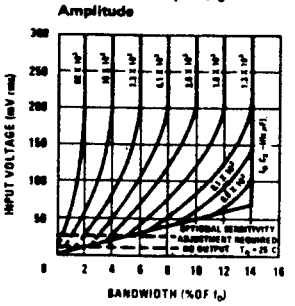
Typical Frequency Drift with (Mean and S.D.) Temperature



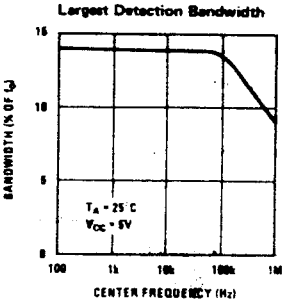
Typical Frequency Drift with Temperature (Mean and S.D.)



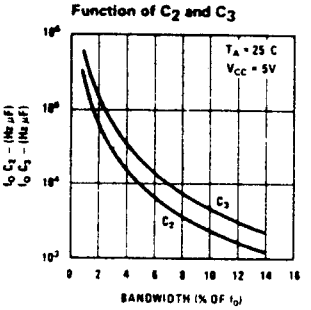
Bandwidth vs Input Signal Amplitude



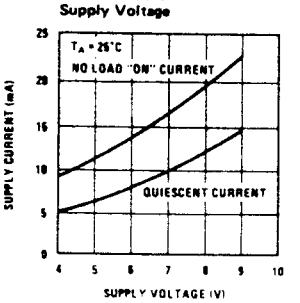
Largest Detection Bandwidth



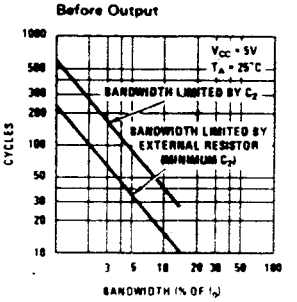
Detection Bandwidth as a Function of C_2 and C_3



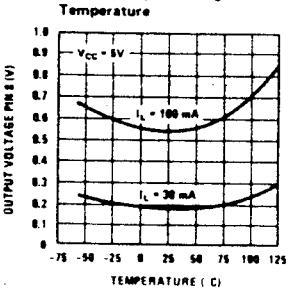
Typical Supply Current vs Supply Voltage



Greatest Number of Cycles Before Output

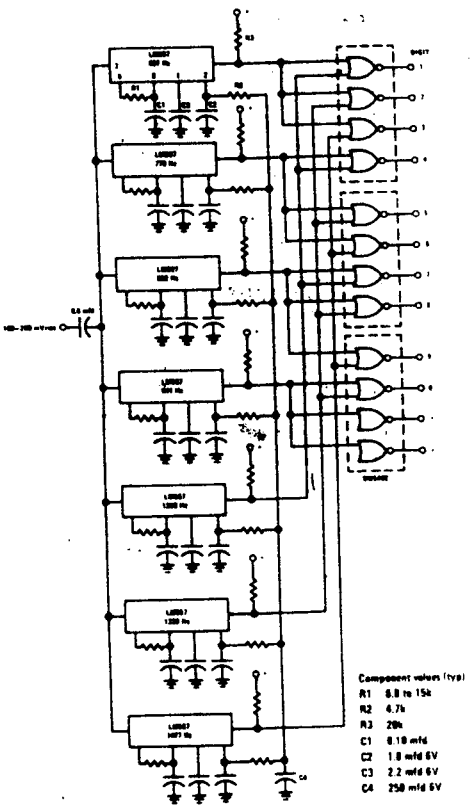


Typical Output Voltage vs Temperature



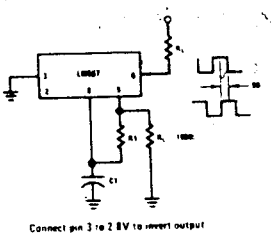
Typical Applications

Touch-Tone Decoder



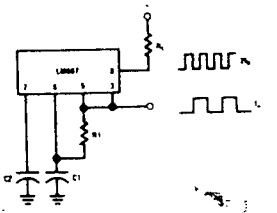
Component values (typ)
R1 6.8 to 15k
R2 4.7k
R3 20k
C1 0.1 mfd
C2 1.8 mfd 6V
C3 2.2 mfd 6V
C4 250 mfd 6V

Oscillator with Quadrature Output

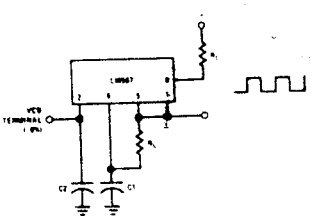


Connect pin 3 to 2.8V to invert output

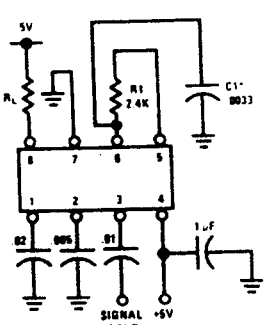
Oscillator with Double Frequency Output



Precision Oscillator Drive 100 mA Loads



AC Test Circuit



f, = 100 kHz +5V
*Note: Adjust for f_o = 100 kHz

Applications Information

The center frequency of the tone decoder is equal to the free running frequency of the VCO. This is given by

$$f_o \cong \frac{1}{1.1R_1C_1}$$

The bandwidth of the filter may be found from the approximation

$$BW = 1070\sqrt{\frac{V_i}{f_o C_2}} \quad \text{in \% of } f_o$$

Where:

V_i = Input voltage (volts rms), $V_i \leq 200$ mV

C_2 = Capacitance at Pin 2 (μF)

CD4066B Types

CMOS Quad Bilateral Switch

For Transmission or Multiplexing of Analog or Digital Signals

High-Voltage Types (20-Volt Rating)

The RCA-CD4066B is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with RCA-CD4016B, but exhibits a much lower on-state resistance. In addition, the on-state resistance is relatively constant over the full input-signal range.

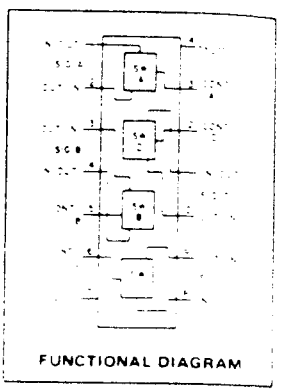
The CD4066B consists of four independent bilateral switches. A single control signal is required per switch. Both the p and the n device in a given switch are biased on or off simultaneously by the control signal. As shown in Fig. 1, the well of the n-channel device on each switch is either tied to the input when the switch is on or to V_{SS} when the switch is off. This configuration eliminates the variation of the switch transistor threshold voltage with input signal, and thus keeps the on-state resistance low over the full operating-signal range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage, and more constant on-state impedance over the input-signal range. For sample-and-hold applications, however, the CD4016B is recommended.

The CD4066B is available in 14-lead ceramic dual-in-line packages (D and F suffixes), 14-lead plastic dual-in-line packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- 15-V digital or ±7.5-V peak-to-peak switching
- 125Ω typical on-state resistance for 15-V operation
- Switch on-state resistance matched to within 5 Ω over 15-V signal-input range
- On-state resistance flat over full peak-to-peak signal range
- High on/off output-voltage ratio: 80 dB typ. @ f_{is} = 10 kHz, R_L = 1 kΩ
- High degree of linearity: <0.5% distortion typ. @ f_{is} = 1 kHz, V_{is} = 5 Vp-p, $V_{DD} - V_{SS} \geq 10$ V, R_L = 10 kΩ
- Extremely low off-state switch leakage resulting in very low offset current and high effective off-state resistance: 10 pA typ. @ $V_{DD} - V_{SS}$ = 10 V, T_A = 25°C
- Extremely high control input impedance (control circuit isolated from signal circuit): 10^{12} Ω typ.
- Low crosstalk between switches: −50 dB typ. @ f_{is} = 8 MHz, R_L = 1 kΩ
- Matched control-input to signal-output capacitance: Reduces output signal transients
- Frequency response, switch on = 40 MHz (typ.)
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of "B" Series CMOS Devices"



FUNCTIONAL DIAGRAM

Applications:

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator
  - Demodulator
  - Commutating switch
- Digital signal switching/Multiplexing
- Transmission-gate logic implementation
- Analog-to-digital & digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT (except for TRANSMISSION GATE which is 25 mA)	±10 mA
POWER DISSIPATION PER PACKAGE (P_D)	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A)	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max	+265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

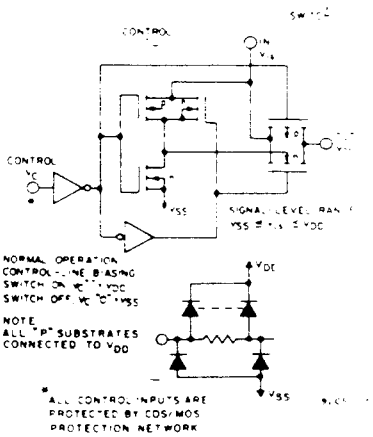


Fig. 1 – Schematic diagram of 1 of 4 identical switches and its associated control circuitry.

ELECTRICAL CHARACTERISTICS (cont'd)

Characteristic	Test Conditions	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D, F, K, H, Packages Values at –40, +25, +85 Apply to E Package						UNITS
			–55	–40	+85	+125	+25 Typ.	+25 Max.	
Control (V_C)									
Control Input Low Voltage, V_{ILC} Max.	I_{is} < 10 μA V_{is} = V_{SS}, V_{OS} = V_{DD} and V_{is} = V_{DD}, V_{OS} = V_{SS}	5	1	1	1	1		1	V
		10	2	2	2	2	–	2	
		15	2	2	2	2	–	2	
Control Input High Voltage, V_{IHC}	See Fig. 6	5	3.5 (Min.)						V
		10	7 (Min.)						
		15	11 (Min.)						
Input Current, I_{IN} Max.	$V_{is} \leq V_{DD}$ $V_{DD} - V_{SS}$ = 18 V $V_{CC} \leq V_{DD} - V_{SS}$	18	±0.1	±0.1	±1	±1	$±10^{-5}$	±0.1	μA
Crosstalk (Control Input to Signal Output)	V_C = 10 V (Sq. Wave) t_r, t_f = 20 ns R_L = 10 kΩ	10	–	–	–	–	50	–	mV
Turn-On and Turn-Off Propagation Delay	V_{IN} = V_{DD} t_r, t_f = 20 ns C_L = 50 pF R_L = 1 kΩ	5	–	–	–	–	35	70	ns
		10	–	–	–	–	20	40	
		15	–	–	–	–	15	30	
Maximum Control Input Repetition Rate	V_{is} = V_{DD}, V_{SS} = GND, R_L = 1 kΩ to gnd, C_L = 50 pF, V_C = 10 V(Square wave centered on 5 V) t_r, t_f = 20 ns, V_{os} = ½ V_{OS} @ 1 kHz	5	–	–	–	–	6	–	MHz
		10	–	–	–	–	9	–	
		15	–	–	–	–	9.5	–	
Input Capacitance, C_{IN}			–	–	–	–	5	7.5	μF

V_{DD} (V)	V_{is} (V)	Switch Input I_{is} (mA) –55°C	–40°C	+25°C	+85°C	+125°C	Switch Output, V_{os} (V) Min.	Max.
5	0	0.64	0.61	0.51	0.42	0.36	–	0.4
5	5	–0.64	–0.61	–0.51	–0.42	–0.36	4.6	–
10	0	1.6	1.5	1.3	1.1	0.9	–	0.5
10	10	–1.6	–1.5	–1.3	–1.1	–0.9	9.5	–
15	0	4.2	4	3.4	2.8	2.4	–	1.5
15	15	–4.2	–4	–3.4	–2.8	–2.4	13.5	–

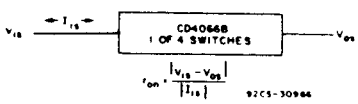


Fig. 6– Determination of r_{on} as a test condition for control input V_{IHC} specification.

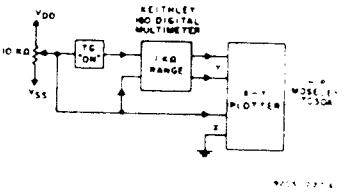


Fig. 7 – Channel on-state resistance measurement circuit.

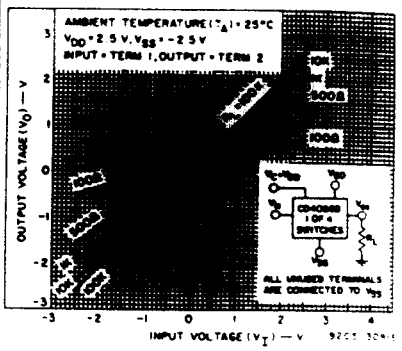


Fig. 8—Typical ON characteristics for 1 of 4 Channels.

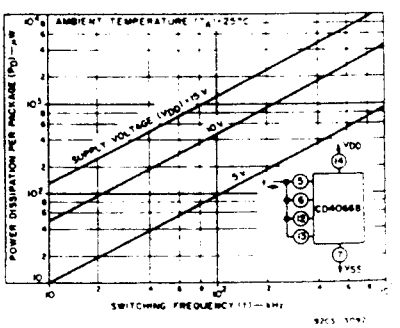


Fig. 9 – Power dissipation per package vs. switching frequency.

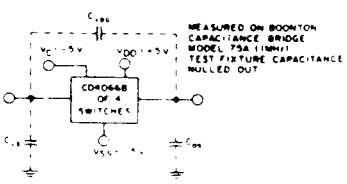


Fig. 10 – Capacitance test circuit.

ELECTRICAL CHARACTERISTICS

Characteristic	Test Conditions	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, K, H Packages Values at −40, +25, +85 Apply to E Package						UNITS
				−55	−40	+85	+125	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD}		0,5	5	0.25	0.25	7.5	7.5	0.01	0.25	μA
		0,10	10	0.5	0.5	15	15	0.01	0.5	
		0,15	15	1	1	30	30	0.01	1	
		0,20	20	5	5	150	150	0.02	5	
Signal Inputs (V_{is}) and Output (V_{os})										
On-State Resistance, r_{on} Max.	$V_C = V_{DD}$, R_L = 10 kΩ returned to $\frac{V_{DD} - V_{SS}}{2}$, $V_{is} = V_{SS}$ to V_{DD}		5	800	850	1200	1300	470	1050	Ω
			10	310	330	500	550	180	400	
			15	200	210	300	320	125	240	
ΔOn-State Resistance Between Any 2 Switches, Δr_{on}	R_L = 10 kΩ, $V_C = V_{DD}$		5	–	–	–	–	15	–	Ω
			10	–	–	–	–	10	–	
			15	–	–	–	–	5	–	
Total Harmonic Distortion, THD	$V_C = V_{DD}$ = 5 V, V_{SS} = −5 V, $V_{is(p-p)}$ = 5 V (Sine wave centered on 0 V) R_L = 10 kΩ, f_{is} = 1 kHz sine wave			–	–	–	–	0.4	–	%
−3dB Cutoff Frequency (Switch on)	$V_C = V_{DD}$ = 5 V, V_{SS} = −5 V, $V_{is(p-p)}$ = 5 V (Sine wave centered on 0 V R_L = 1 kΩ,			–	–	–	–	40	–	MHz
−50dB Feedthrough Frequency (Switch off)	$V_C = V_{SS}$ = −5 V, $V_{is(p-p)}$ = 5 V Sine wave centerd on 0 V R_L = 1 kΩ			–	–	–	–	1	–	MHz
Input/Output Leakage Current (Switch off) I_{is} Max.	V_C = 0 V V_{is} = 18 V, V_{os} = 0 V, V_{is} = 0V; V_{os} = 18 V		18	±0.1	±0.1	±1	±1	$±10^{-5}$	±0.1	μA
−50 dB Crosstalk Frequency	$V_C(A) = V_{DD}$ = +5 V, $V_C(B) = V_{SS}$ = −5 V, $V_{is}(A)$ = 5 V_{p-p}, 50 Ω source R_L = 1 kΩ			–	–	–	–	8	–	MHz
Propagation Delay (Signal Input to Signal Output) t_{pd}	R_L = 200 kΩ $V_C = V_{DD}$, V_{SS} = GND, C_L = 50 pF V_{is} = 10 V (Square wave centered on 5 V t_r, t_f = 20 ns		5	–	–	–	–	20	40	ns
			10	–	–	–	–	10	20	
			15	–	–	–	–	7	15	
Capacitance: Input, C_{is}	V_{DD} = +5 V $V_C = V_{SS}$ = −5 V			–	–	–	–	8	–	pF
Output, C_{os}				–	–	–	–	8	–	
Feedthrough, C_{ios}				–	–	–	–	0.5	–	

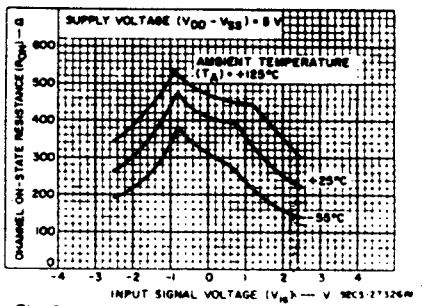


Fig. 2– Typical on-state resistance vs. input signal voltage (all types).

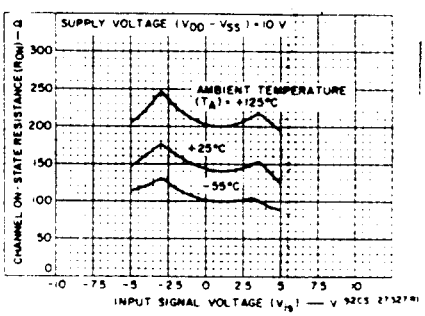


Fig. 3– Typical on-state vs. input signal voltage (all types).

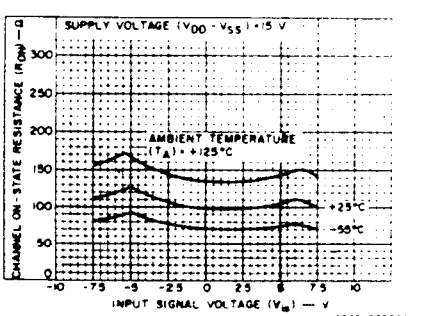


Fig. 4 – Typical on-state resistance vs. input signal voltage (all types).

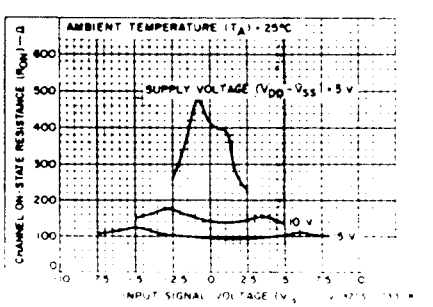


Fig. 5 on state resistance vs. input signal voltage (all types).

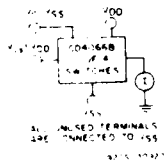


Fig. 11 – Off-switch input or output leakage.

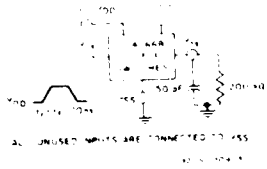


Fig. 12 – Propagation delay time signal input (V_{is}) to signal output (V_{os}).

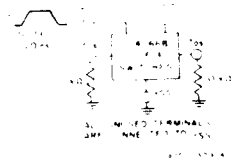


Fig. 13 – Crosstalk-control input to signal output.

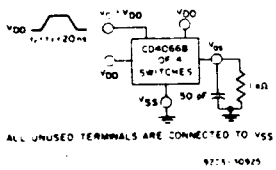


Fig. 14 – Propagation delay t_{PLH}, t_{PHL} control-signal output. Delay is measured at V_{os} level of +10% from ground (turn-on) or on-state output level (turn-off).

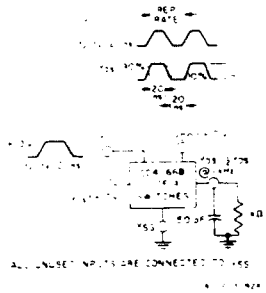


Fig. 15 – Maximum allowable control input repetition rate.

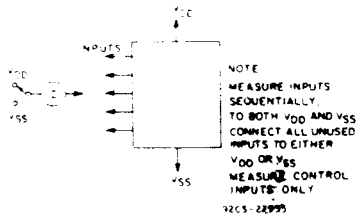


Fig. 16 – Input leakage current test circuit.

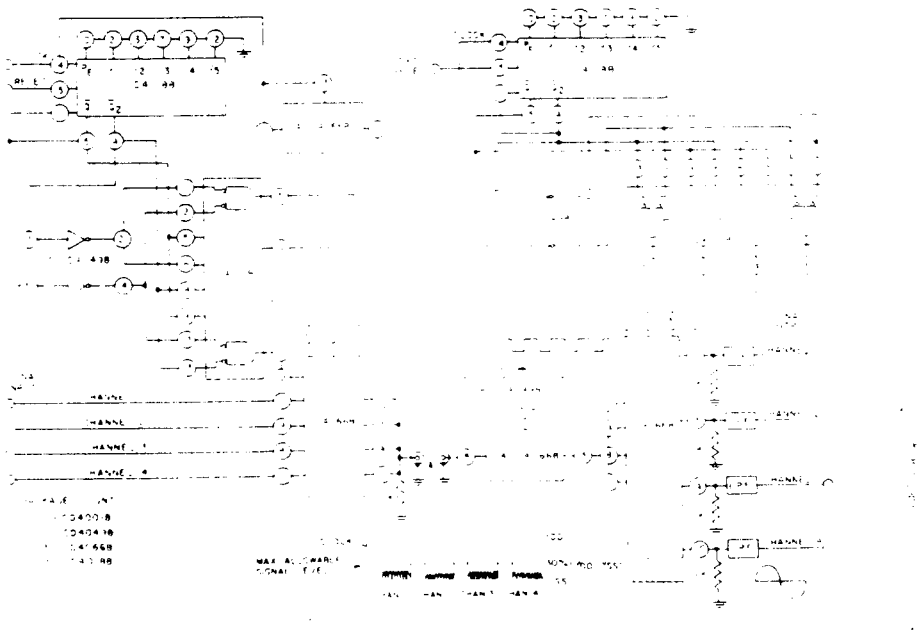


Fig. 17 – 4-channel PAM multiplex system diagram.

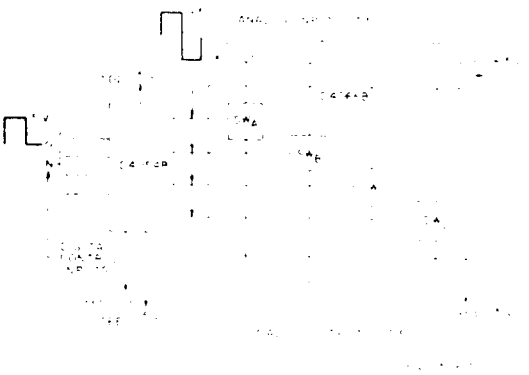
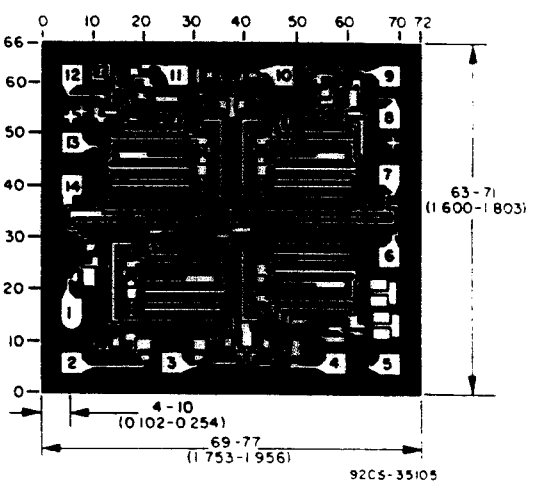


Fig. 18 – Bidirectional signal transmission via a digital control logic



CD4066BH
CHIP PHOTOGRAPH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.

SPECIAL CONSIDERATIONS — CD4066B

1. In applications that employ separate power sources to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the four CD4066B bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or

2. In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1,4,8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 volts (calculated from R_{ON} values shown).

   No V_{DD} current will flow through R_L if the switch current flows into ter-

CD4069UB Types

CMOS Hex Inverter

High-Voltage Types (20-Volt Rating)

The RCA-CD4069UB types consist of six CMOS inverter circuits. These devices are intended for all general-purpose inverter applications where the medium-power TTL-drive and logic-level-conversion capabilities of circuits such as the CD4009 and CD4049 Hex Inverter/Buffers are not required.

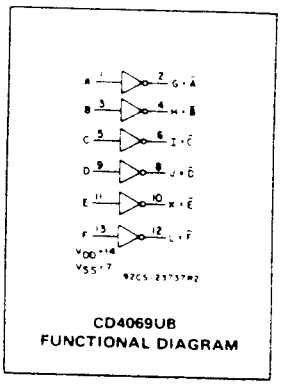
The CD4069UB-Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- Standardized symmetrical output characteristics
- Medium Speed Operation—t_{PHL},t_{PLH}=30 ns (typ.) at 10 V
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Logic inversion
- Pulse shaping
- Oscillators
- High-input-impedance amplifiers



CD4069UB
FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC		CONDITIONS V_{DD} V	ALL TYPES LIMITS Typ.	Max.	UNITS
Propagation Delay Time;	t_{PLH}, t_{PHL}	5	55	110	ns
		10	30	60	
		15	25	50	
Transition Time;	t_{THL}, t_{TLH}	5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance;	C_{IN}	Any Input	10	15	pF

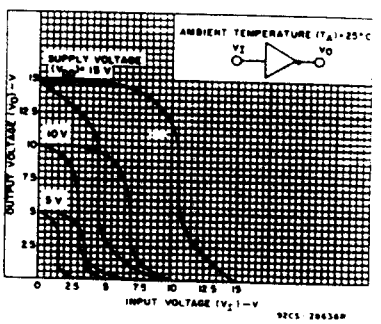


Fig. 1 – Minimum and maximum voltage transfer characteristics.

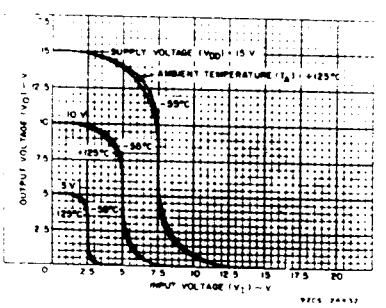


Fig. 2 – Typical voltage transfer characteristics as a function of temperature.

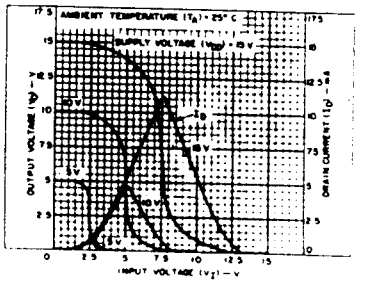


Fig. 3 – Typical current and voltage transfer

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,K,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	5	5	0.05				–	0	0.05	V
	–	10	10	0.05				–	0	0.05	
	–	15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0	5	4.95				4.95	5	–	
	–	0	10	9.95				9.95	10	–	
	–	0	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	4.5	–	5	1				–	–	1	V
	9	–	10	2				–	–	2	
	13.5	–	15	2.5				–	–	2.5	
Input High Voltage, V_{IH} Min.	0.5	–	5	4				4	–	–	
	1	–	10	8				8	–	–	
	1.5	–	15	12.5				12.5	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

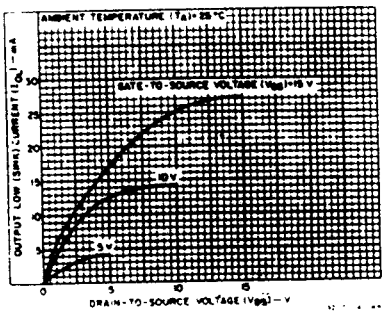


Fig. 4 – Typical output low (sink) current characteristics.

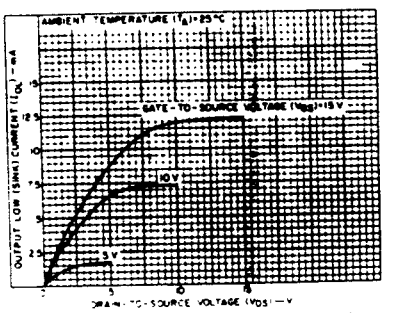


Fig. 5 – Minimum output low (sink) current characteristics.

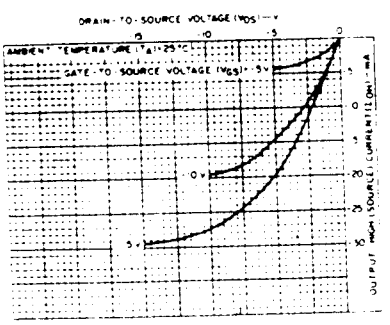


Fig. 8 – Typical output high (source) current characteristics.

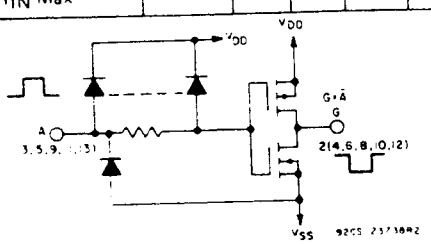


Fig. 6 – Schematic diagram of one of six identical inverters.

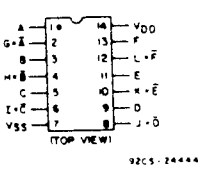


Fig. 7 – CD4069UB terminal assignment.

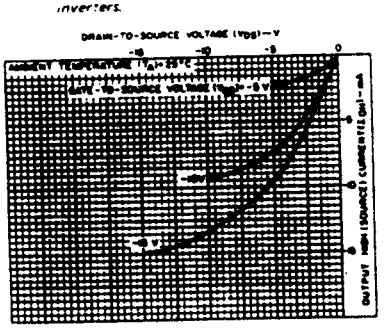


Fig. 9 – Minimum output high (source) current characteristics.

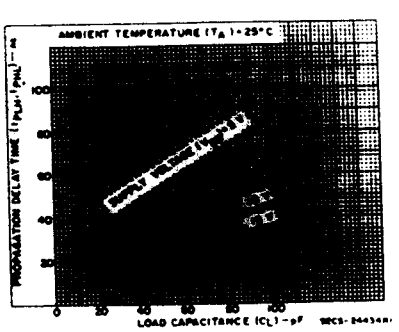


Fig. 10 – Typical propagation delay time vs. load capacitance.

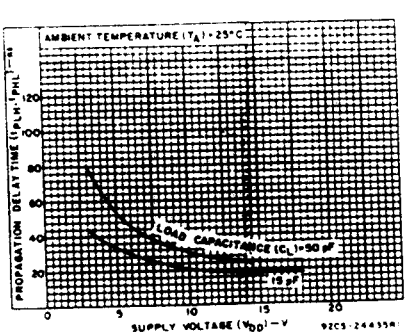


Fig. 11 – Typical propagation delay time vs. supply voltage.

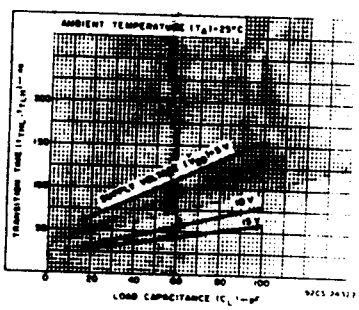


Fig. 12 – Typical transition time vs. load capacitance.

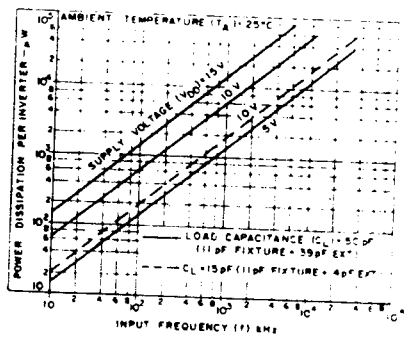


Fig. 13 – Typical dynamic power dissipation vs. frequency.

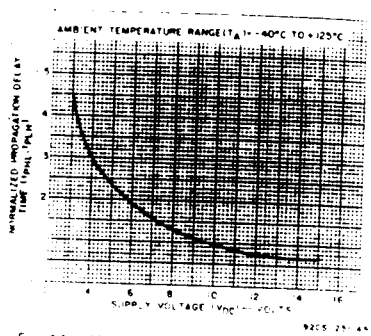


Fig. 14 – Variation of normalized propagation delay time (t_{PHL} and t_{PLH}) with supply voltage.

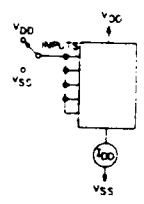


Fig. 15 – Quiescent device current test circuit.

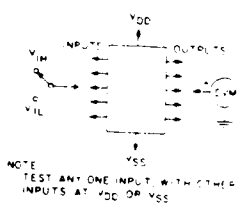


Fig. 16 – Noise immunity test circuit.

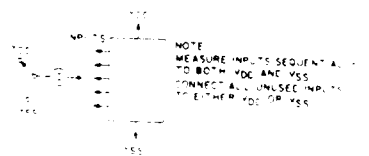


Fig. 17 – Input leakage current test circuit.

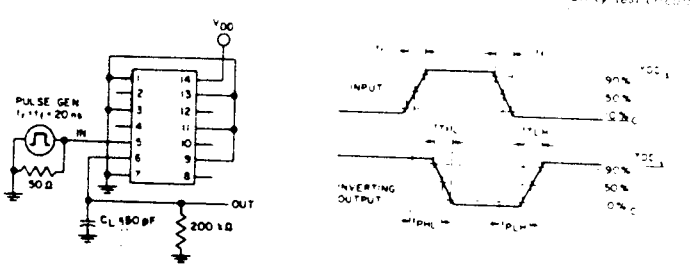


Fig. 18 – Dynamic electrical characteristics test circuit and waveforms.

APPLICATIONS

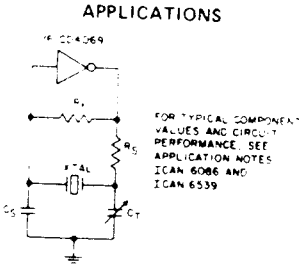


Fig. 19 – Typical crystal oscillator circuit.

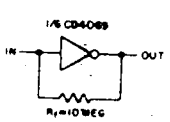


Fig. 20 – High-input impedance amplifier.

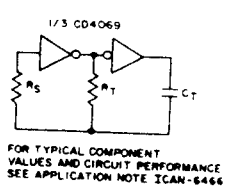


Fig. 21 – Typical RC oscillator circuit.

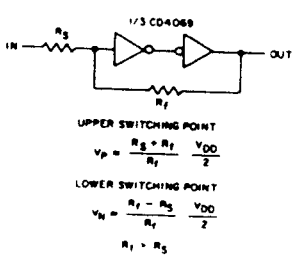
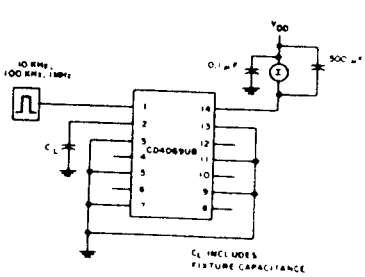
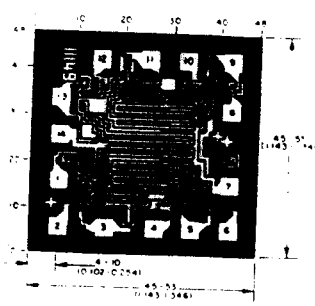


Fig. 22 – Input pulse shaping circuit.





Dimensions and pad layout for CD4069UBH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance

CD4071B, CD4072B, CD4075B Types

CMOS OR Gates

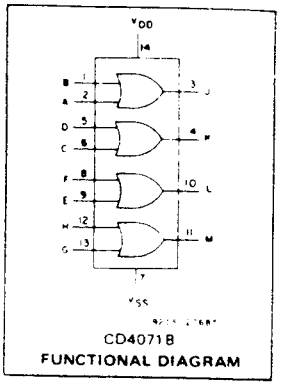
High-Voltage Types (20-Volt Rating)

CD4071B Quad 2-Input OR Gate
CD4072B Dual 4-Input OR Gate
CD4075B Triple 3-Input OR Gate

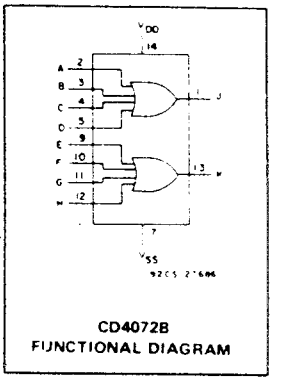
The RCA-CD4071B, CD4072B, and CD4075B OR gates provide the system designer with direct implementation of the positive-logic OR function and supplement the existing family of CMOS gates. The CD4071, CD4072, and CD4075 types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

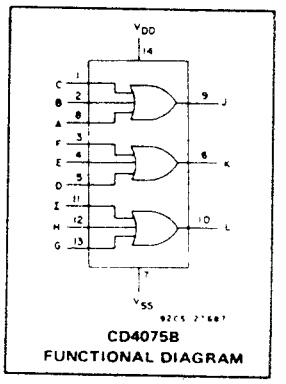
- Medium-Speed Operation-t_{PLH}, t_{PHL} = 60 ns (typ.) at V_{DD} = 10 V
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Standardized, symmetrical output characteristics
- Noise margin (over full package temperature range)
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13 A, "Standard Specifications for Description of 'B' Series CMOS Devices"



CD4071B
FUNCTIONAL DIAGRAM



CD4072B
FUNCTIONAL DIAGRAM



CD4075B
FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D, F, K, H Packages Values at -40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	–	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	–	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5, 13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	4.5	–	5	3.5				3.5	—	—	
	9	–	10	7				7	—	—	
	13.5	–	15	11				11	—	—	
Input Current		0.18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) ..... -0.5 to +20 V
(Voltages referenced to V_{SS} Terminal) ..... -0.5 to V_{DD} +0.5 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... ±10 mA
DC INPUT CURRENT, ANY ONE INPUT ..... 500 mW
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... 500 mW
For T_A = -55 to +100°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... 100 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... -55 to +125°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H ..... -40 to +85°C
PACKAGE TYPE E ..... -65 to +150°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... +265°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. .....

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, and C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		ALL TYPES LIMITS		UNITS
		V_{DD} VOLTS	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5	125	250	ns
		10	60	120	
		15	45	90	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input	—	5	7.5	pF

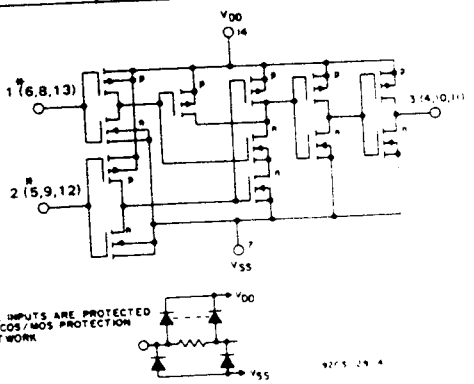


Fig. 3 – Schematic diagram for CD4071B (1 of 4 identical gates).

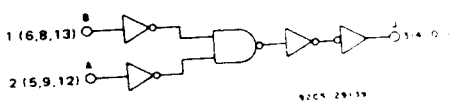


Fig. 5 – Logic diagram for CD4071B (1 of 4 identical gates).

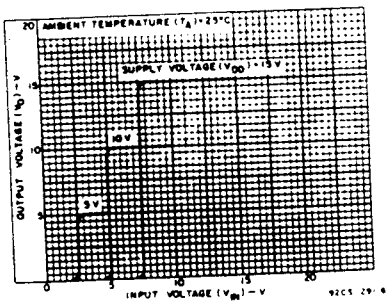


Fig. 1 – Typical voltage transfer characteristics.

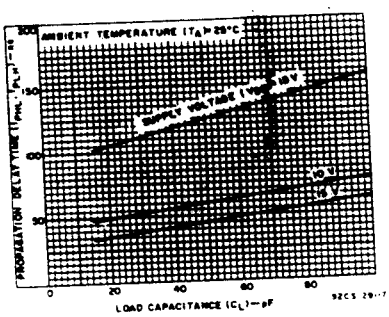


Fig. 2 – Typical propagation delay time as a function of load capacitance.

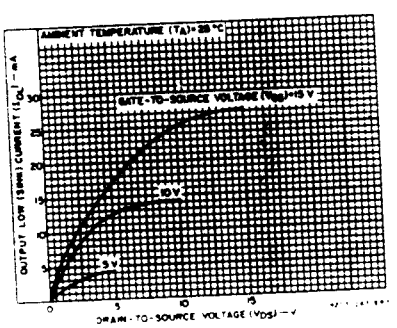


Fig. 4 – Typical output low (sink) current characteristics.

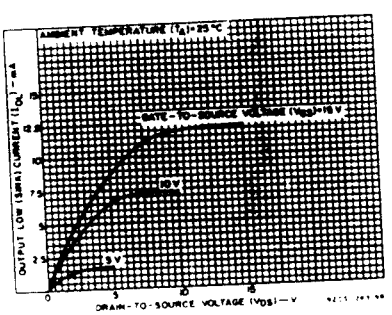
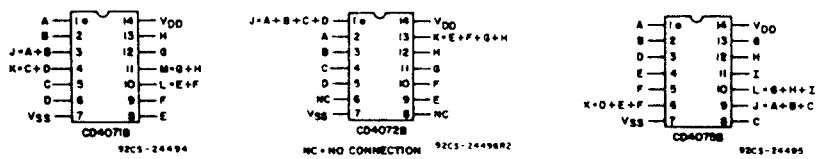


Fig. 6 – Minimum output low (sink) current characteristics.

TERMINAL ASSIGNMENTS (TOP VIEW)



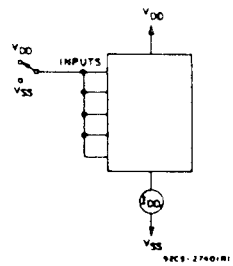


Fig. 15 – Quiescent device current test circuit.

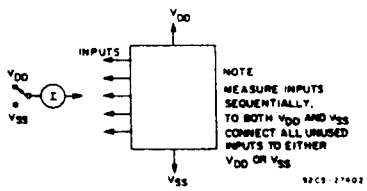


Fig. 16 – Input current test circuit.

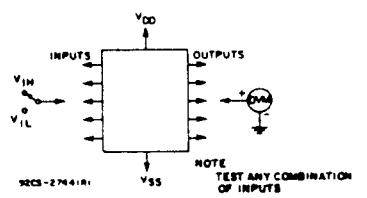
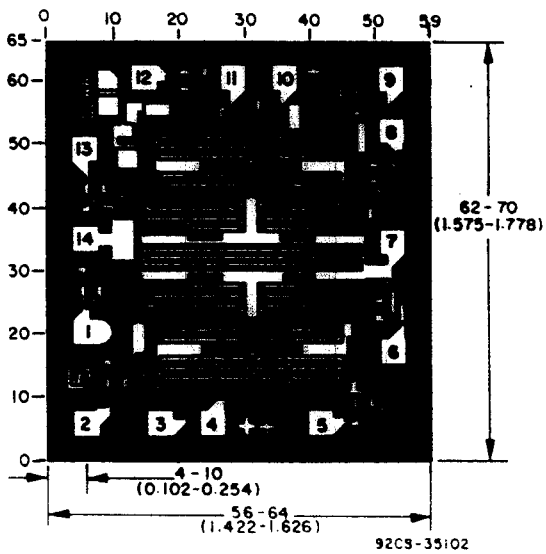


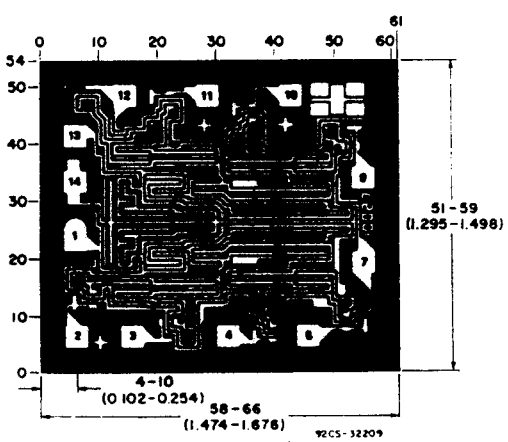
Fig. 17 – Input-voltage test circuit.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

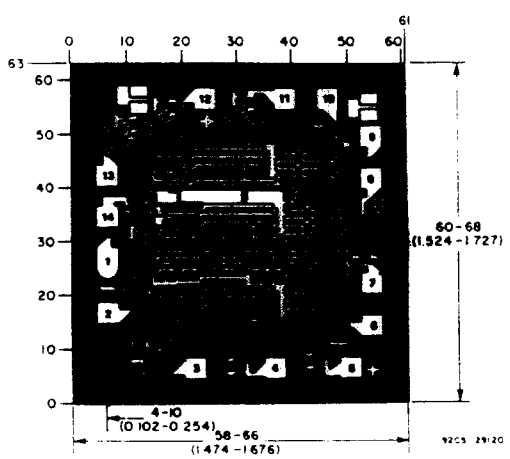
The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.



Dimensions and pad layout for CD4071B.



Dimensions and pad layout for CD4072B.



Dimensions and pad layout for CD4075B.

CD4073B, CD4081B, CD4082B Types

CMOS AND Gates

High-Voltage Types (20-Volt Rating)

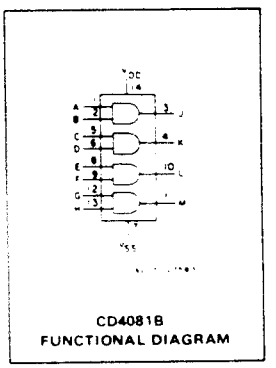
CD4073B Triple 3-Input AND Gate
CD4081B Quad 2-Input AND Gate
CD4082B Dual 4-Input AND Gate

The RCA-CD4073B, CD4081B and CD-4082B AND gates provide the system designer with direct implementation of the AND function and supplement the existing family of CMOS gates.

The CD4073B, CD4081B and CD4082B types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

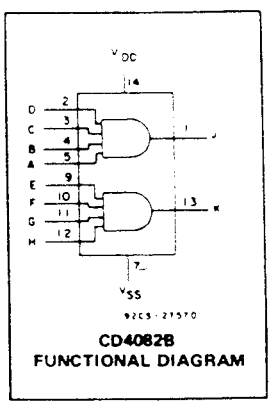
- Medium-Speed Operation – t_{PLH}, t_{PHL} = 60 ns (typ.) at V_{DD} = 10 V
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



CD4081B
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

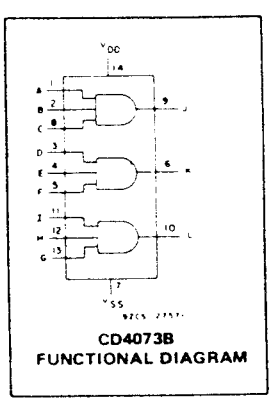


CD4082B
FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V



CD4073B
FUNCTIONAL DIAGRAM

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, Input t_r,t_f=20 ns, and C_L=50 pF, R_L=200 kΩ

CHARACTERISTIC	TEST CONDITIONS		ALL TYPES LIMITS		UNITS
		V_{DD} Volts	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5	125	250	ns
		10	60	120	
		15	45	90	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input	–	5	7.5	pF

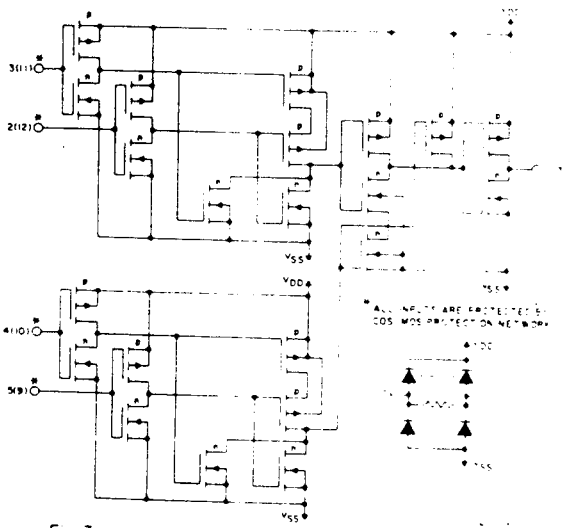


Fig. 7 – Schematic diagram for CD4082B (1 of 2 identical gates).

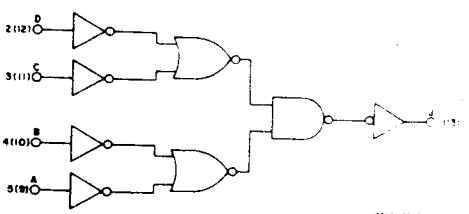


Fig. 9 – Logic diagram for CD4082B (1 of 2 identical gates).

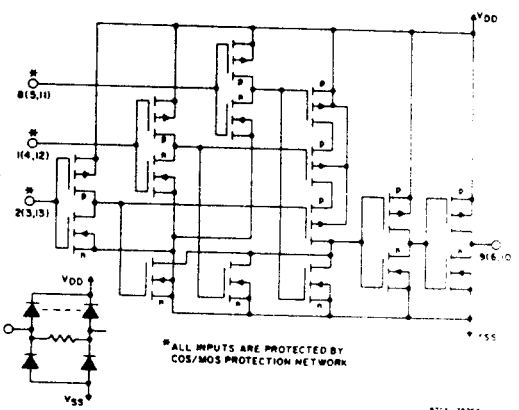


Fig. 11 – Schematic diagram for CD4073B (1 of 3 identical gates).

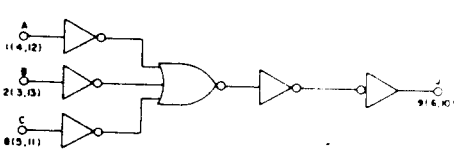


Fig. 13 – Logic diagram for CD4073B (1 of 3 identical gates).

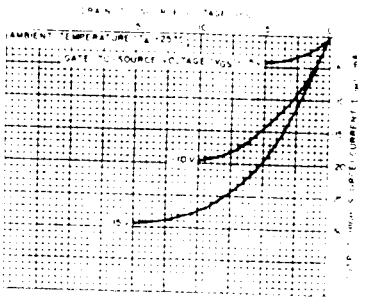


Fig. 8 – Typical output high (source) current characteristics.

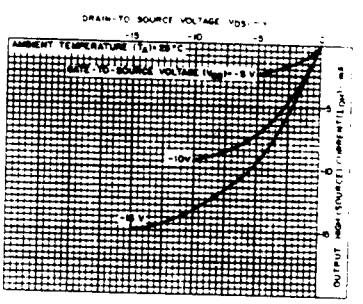


Fig. 10 – Minimum output high (source) current characteristics.

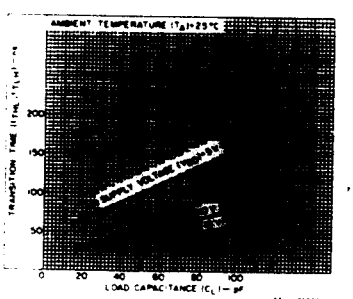


Fig. 12 – Typical transition time as a function of load capacitance.

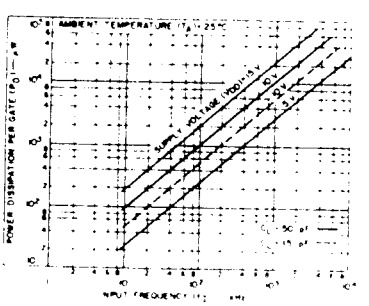


Fig. 14 – Typical dynamic power dissipation per gate as a function of frequency.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D, F, K, H Packages Values at -40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	-	0,5	5	0.25	0.25	7.5	7.5	-	0.01	0.25	µA
	-	0,10	10	0.5	0.5	15	15	-	0.01	0.5	
	-	0,15	15	1	1	30	30	-	0.01	1	
	-	0,20	20	5	5	150	150	-	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage: Low-Level, V_{OL} Max.	-	0,5	5	0.05				-	0	0.05	V
	-	0,10	10	0.05				-	0	0.05	
	-	0,15	15	0.05				-	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	-	0,5	5	4.95				4.95	5	-	
	-	0,10	10	9.95				9.95	10	-	
	-	0,15	15	14.95				14.95	15	-	
Input Low Voltage, V_{IL} Max.	0.5	-	5	1.5				-	-	1.5	V
	1	-	10	3				-	-	3	
	1.5	-	15	4				-	-	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	-	5	3.5				3.5	-	-	
	1,9	-	10	7				7	-	-	
	1.5,13.5	-	15	11				11	-	-	
Input Current I_{IN} Max		0,18	18	±0.1	±0.1	±1	±1	-	$\pm 10^{-5}$	±0.1	µA

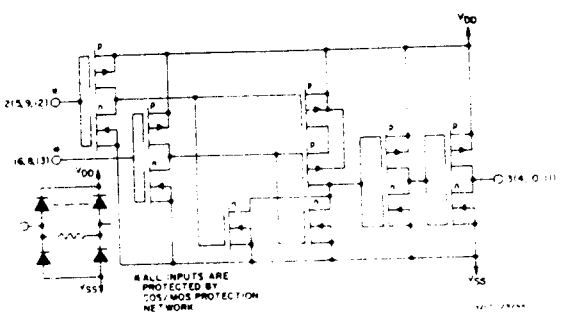


Fig. 1 – Schematic diagram for CD4081B (1 of 4 identical gates).

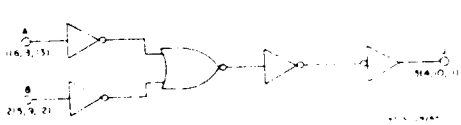


Fig. 2 – Logic diagram for CD4081B (1 of 4 identical gates).

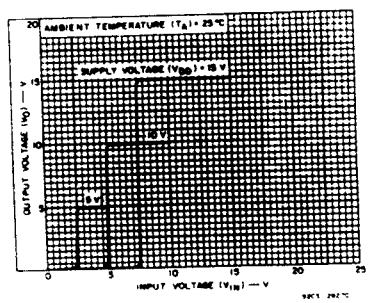


Fig. 3 – Typical voltage transfer characteristics.

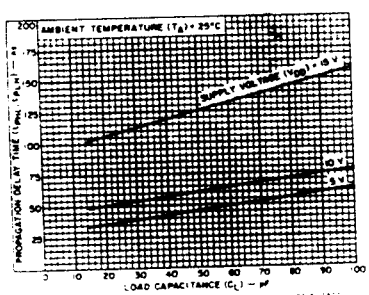


Fig. 4 – Typical propagation delay time as a function of load capacitance.

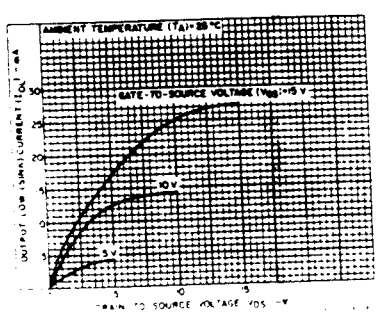


Fig. 5 – Typical output low (sink) current characteristics.

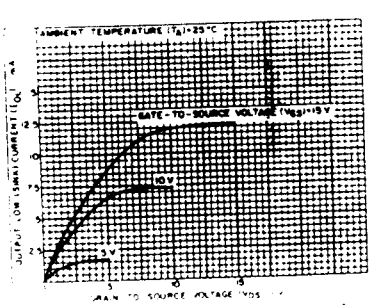


Fig. 6 – Minimum output low (sink) current characteristics.

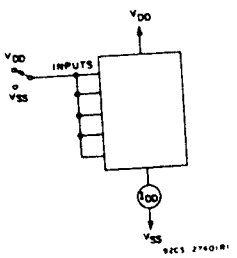


Fig. 15 – Quiescent device current test circuit.

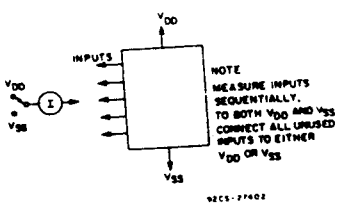


Fig. 16 – Input current test circuit.

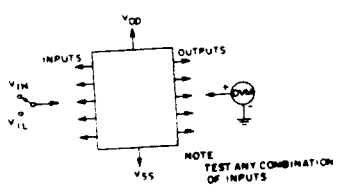
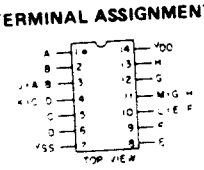
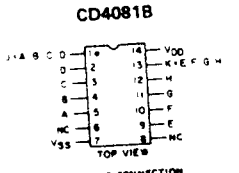


Fig. 17 – Input-voltage test circuit.

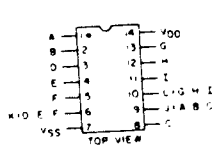
TERMINAL ASSIGNMENTS



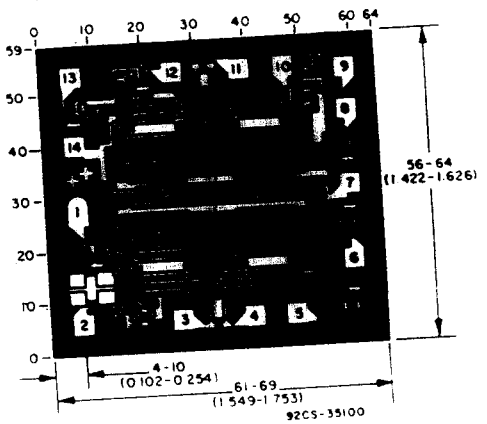
CD4081B



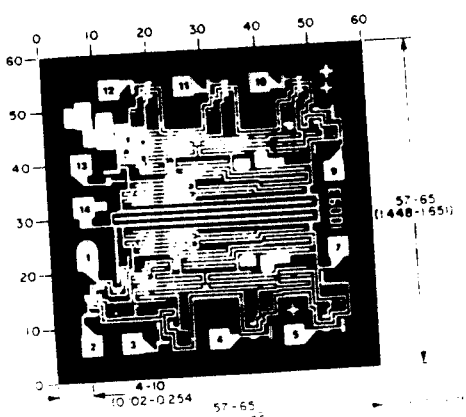
CD4082B



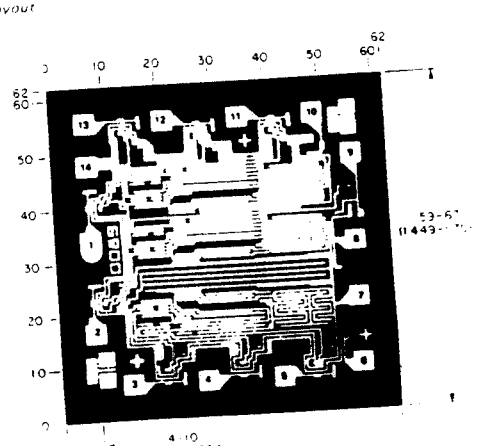
CD4073B



Dimensions and pad layout for CD4081B.



Dimensions and pad layout for CD4082B



Dimensions and pad layout for CD4073B

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of ±3 mils (±0.076 mm) applicable to the nominal dimensions shown.

CMOS Presettable Up/Down Counters

High-Voltage Types (20-Volt Rating)

CD4510B – – – BCD Type

CD4516B – – – Binary Type

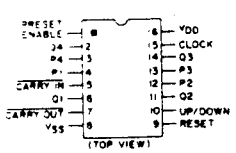
The RCA-CD4510B Presettable BCD Up/Down Counter and the CD4516 Presettable Binary Up/Down Counter consist of four synchronously clocked D-type flip-flops (with a gating structure to provide T-type flip-flop capability) connected as counters. These counters can be cleared by a high level on the RESET line, and can be preset to any binary number present on the jam inputs by a high level on the PRESET ENABLE line. The CD4510B will count out of non-BCD counter states in a maximum of two clock pulses in the up mode, and a maximum of four clock pulses in the down mode.

If the CARRY-IN input is held low, the counter advances up or down on each positive-going clock transition. Synchronous cascading is accomplished by connecting all clock inputs in parallel and connecting the CARRY-OUT of a less significant stage to the CARRY-IN of a more significant stage.

The CD4510B and CD4516B can be cascaded in the ripple mode by connecting the CARRY-OUT to the clock of the next stage. If the UP/DOWN input changes during a terminal count, the CARRY-OUT must be gated with the clock, and the UP/DOWN input must change while the clock is high. This method provides a clean clock signal to the subsequent counting stage. (See Fig. 15).

These devices are similar to types MC14510 and MC14516.

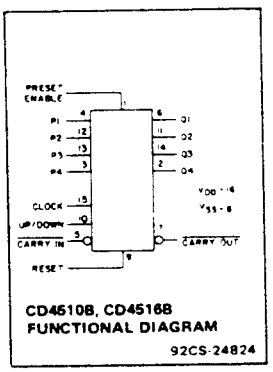
The CD4510B and CD4516B Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4510B, CD4516B
TERMINAL ASSIGNMENT

Features:

- Medium-speed operation – f_{CL} = 8 MHz typ. at 10 V
- Synchronous internal carry propagation
- Reset and Preset capability
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized symmetrical output characteristics
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range): 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



CD4510B, CD4516B
FUNCTIONAL DIAGRAM
92CS-24824

Applications:

- Up/Down difference counting
- Multistage synchronous counting
- Multistage ripple counting
- Synchronous frequency dividers

OPERATING CONDITIONS AT T_A = 25°C, Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD}	Min.	Max.	Units
Supply Voltage Range (At T_A = Full Package-Temperature Range)		3	18	V
Clock Pulse Width, t_W	5	150	–	ns
	10	75	–	
	15	60	–	
Clock Input Frequency, f_{CL}	5	–	2	MHz
	10	–	4	
	15	–	5.5	
Preset Enable or Reset Removal Time*	5	150	–	ns
	10	80	–	
	15	60	–	
Clock Rise and Fall Time, t_rCL, t_fCL*	5	–	15	μs
	10	–	5	
	15	–	5	
Carry-In Setup Time, t_S	5	130	–	ns
	10	60	–	
	15	45	–	
Up-Down Setup Time, t_S	5	360	–	ns
	10	160	–	
	15	110	–	
Preset Enable or Reset Pulse Width, t_W	5	220	–	ns
	10	100	–	
	15	75	–	

*Time required after the falling edge of the reset or preset enable inputs before the rising edge of the clock will trigger the counter (similar to setup time)

*If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW °C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW °C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max ..... 265°C

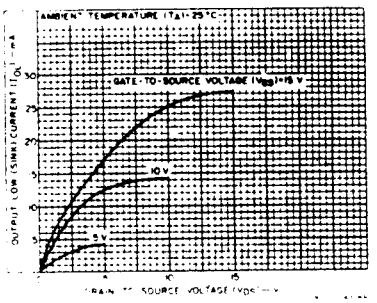


Fig. 1 – Typical output low (sink) current characteristics.

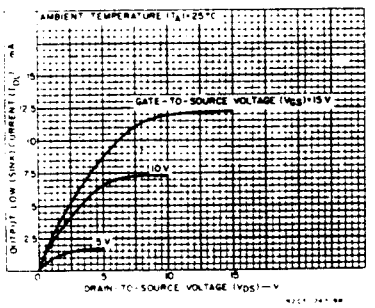


Fig. 2 – Minimum output low (sink) current characteristics.

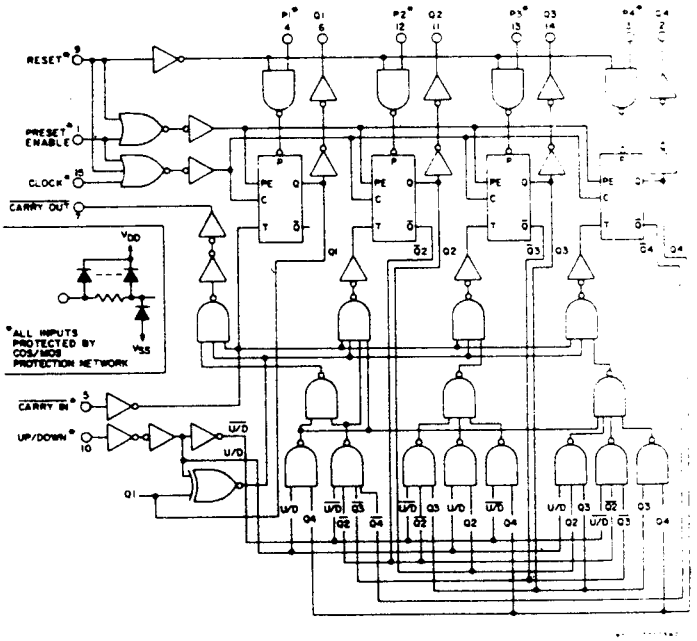


Fig. 3 – Logic Diagram for CD4510B.

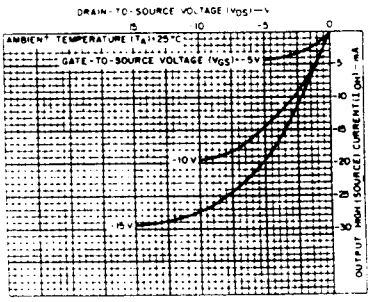


Fig. 4 – Typical output high (source) current characteristics.

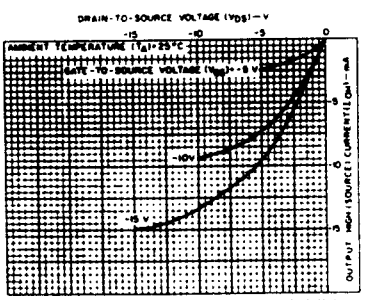


Fig. 5 – Minimum output high (source) current characteristics.

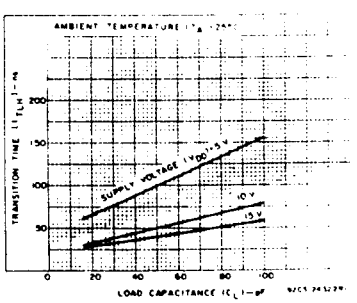


Fig. 6 – Typical transition time vs. load capacitance.

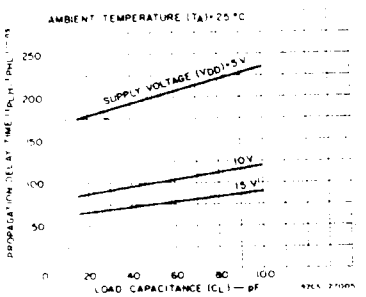


Fig. 7 – Typical propagation delay time vs. load capacitance for clock-to-Q outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 50 pF, Input t_r, t_f = 20 ns, R_L = 200 kΩ

Characteristic	Conditions V_{DD} (V)	Limits All Packages Min.	Typ.	Max.	Units
Propagation Delay Time (t_{PHL}, t_{PLH})					
Clock-to-Q Output (See Fig. 10)	5	–	200	400	ns
	10	–	100	200	
	15	–	75	150	
Preset or Reset-to-Q Output	5	–	210	420	ns
	10	–	105	210	
	15	–	80	160	
Clock-to-Carry Out	5	–	240	480	ns
	10	–	120	240	
	15	–	90	180	
Carry-In-to-Carry Out	5	–	125	250	ns
	10	–	60	120	
	15	–	50	100	
Preset or Reset-to-Carry Out	5	–	320	640	ns
	10	–	160	320	
	15	–	125	250	
Transition Time (t_{THL}, t_{TLH}) (See Fig. 9)	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Max. Clock Input Frequency (f_{CL})	5	2	4	–	MHz
	10	4	8	–	
	15	5.5	11	–	
Input Capacitance (C_{IN})		–	5	7.5	pF
Set-up Time, t_S					ns
Preset Enable to J_n	5	25	12	—	
	10	10	6	—	
	15	10	5	—	
Hold times, t_H					
Clock to Carry-In	5	60	30	—	
	10	30	4	—	
	15	30	1	—	
Clock to Up/Down	5	30	10	—	
	10	30	4	—	
	15	30	5	—	
Preset Enable to J_n	5	70	35	—	
	10	40	20	—	
	15	40	20	—	

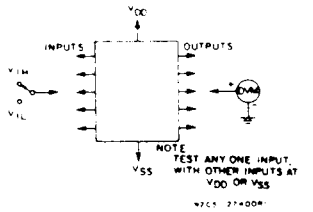
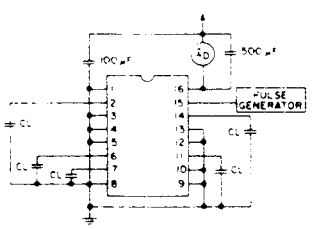


Fig. 13 – Input-voltage test circuit.



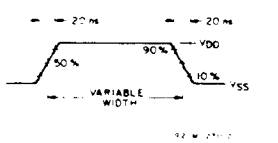
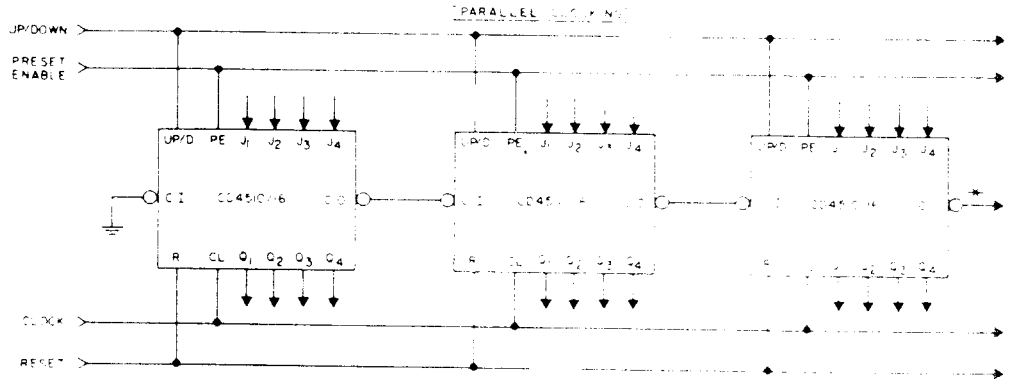
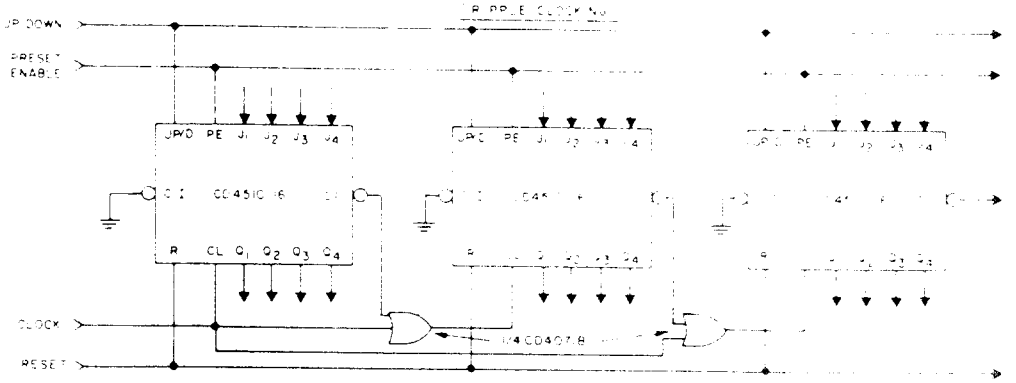


Fig. 14 – Power-dissipation test circuit and input waveform.



* **CARRY OUT** lines at the 2nd, 3rd, etc., stages may have a negative-going glitch pulse resulting from differential delays of different CD4510/16 IC's. These negative-going glitches do not affect proper CD4510/16 operation. However, if the **CARRY OUT** signals are used to trigger other edge-sensitive logic devices, such as FF's or counters, the **CARRY OUT** signals should be gated with the clock signal using a 2-input OR gate such as CD4071B.



RIPPLE CLOCKING MODE
THE UP/DOWN CONTROL CAN BE CHANGED AT ANY COUNT. THE ONLY RESTRICTION ON CHANGING THE UP/DOWN CONTROL IS THAT THE CLOCK INPUT TO THE FIRST COUNTING STAGE MUST BE HIGH

For cascading counters operating in a fixed up-count or down-count mode, the OR gates are not required between stages, and $\overline{CO}$ is connected directly to the CL input of the next stage with $\overline{CI}$ grounded

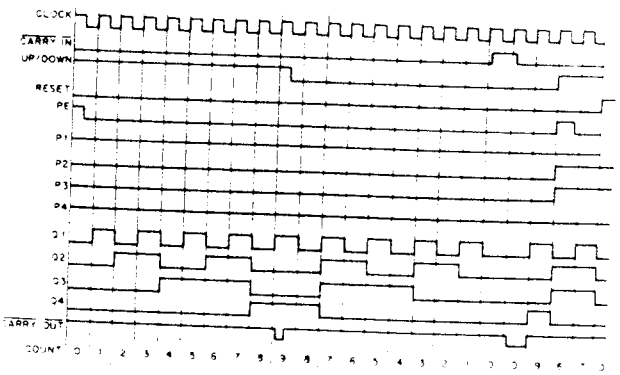
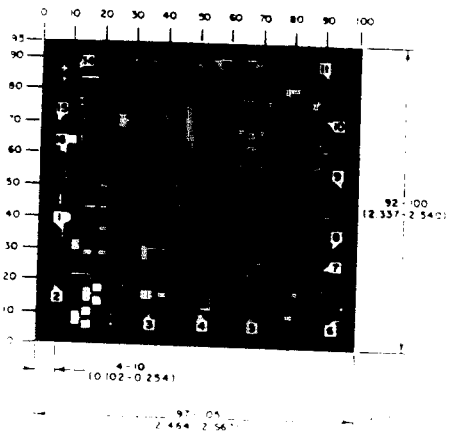


Fig. 15 — Timing Diagram for CD4510B

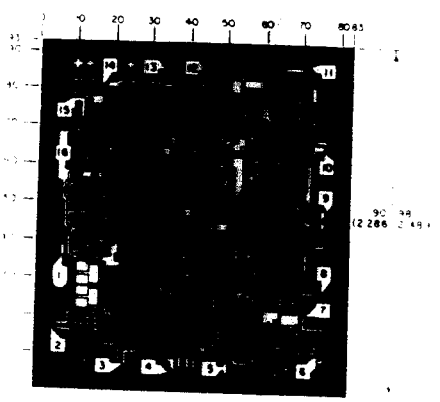
CL	CI	U/D	PE	R	ACTION
X	1	X	0	0	NO COUNT
⎍	0	1	0	0	COUNT UP
⎍	0	0	0	0	COUNT DOWN
X	X	X	1	0	PRESET
X	X	X	X	1	RESET

X = DON'T CARE

TRUTH TABLE



Dimensions and Pad Layout for CD4510BH



Dimensions and Pad Layout for CD4516BH

CD4013B Types

CMOS Dual 'D'-Type Flip-Flop

High-Voltage Types (20-Volt Rating)

The RCA-CD4013B consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and $\overline{Q}$ outputs. These devices can be used for shift register applications, and, by connecting $\overline{Q}$ output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

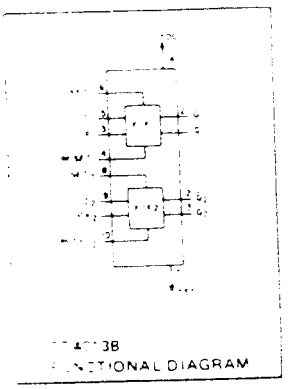
The CD4013B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- Set-Reset capability
- Static flip-flop operation – retains state indefinitely with clock level either "high" or "low"
- Medium-speed operation – 16 MHz (typ.) clock toggle rate at 10V
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range): 1 V at V_{DD}=5 V; 2 V at V_{DD}=10 V; 2.5 V at V_{DD}=15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Registers, counters, control circuits



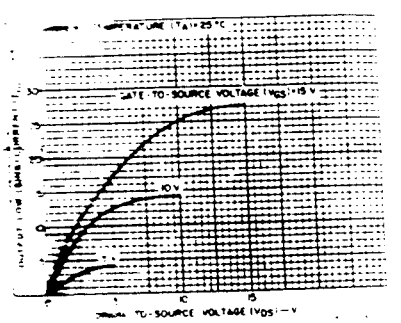


Fig. 1 – Typical output low (sink) current characteristics.

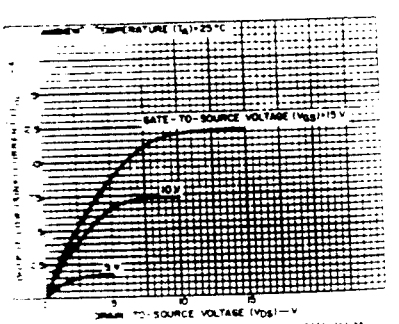


Fig. 2 – Minimum output low (sink) current characteristics.

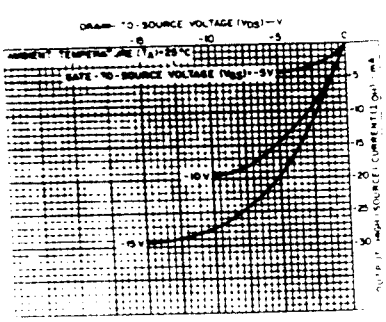


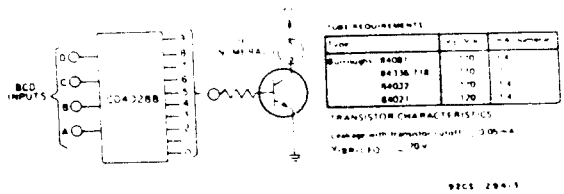
Fig. 3 – Typical output high (source) current characteristics.

RECOMMENDED OPERATING CONDITIONS

At T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	–	3	18	V
Data Setup Time t_S	5	40	–	ns
	10	20	–	
	15	15	–	
Clock Pulse Width t_W	5	140	–	ns
	10	60	–	
	15	40	–	
Clock Input Frequency f_{CL}	5	dc	3.5	MHz
	10		8	
	15		12	
Clock Rise or Fall Time t_rCL,* t_fCL	5	–	70	μs
	10	–	6	
	15	–	2	
Set or Reset Pulse Width t_W	5	180	–	ns
	10	80	–	
	15	50	–	

*If more than one unit is cascaded in a parallel clocked operation, t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.



*(Trademark) Burroughs Corp

Fig. 14 – Neon readout (Nixie Tube) display application.*

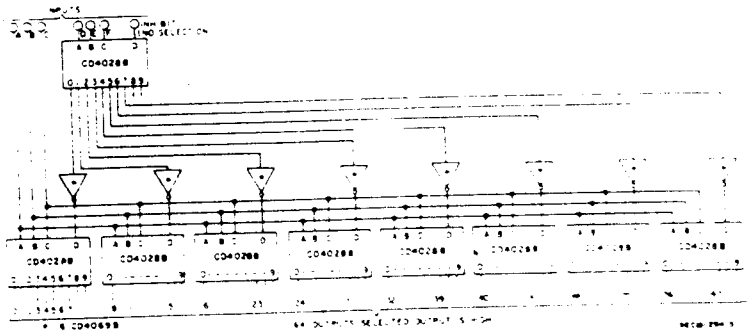
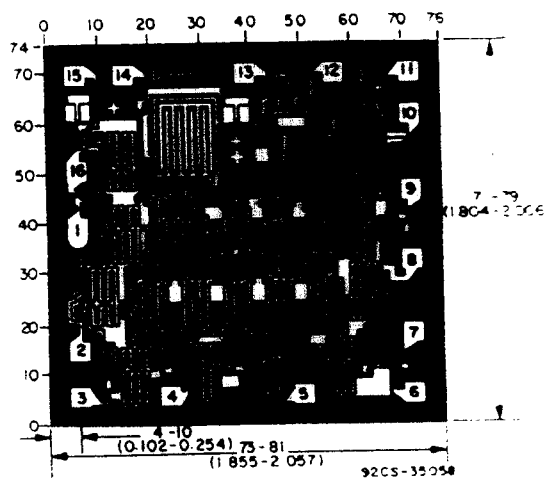


Fig. 15 – 6-bit binary to 1-of-64 address decoder.



CD4028BH
DIMENSIONS AND PAD LAYOUT

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip therefore may differ slightly from the nominal dimensions shown. The user should consider a tolerance of ±3 mils (±0.08 mm) applicable to the nominal dimensions shown.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55,+25,+125 Apply to D,F,K,H Pkgs. Values at −40,+25,+85 Apply to E Pkgs.							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	2.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	9.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
	13.5	0,15	15	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

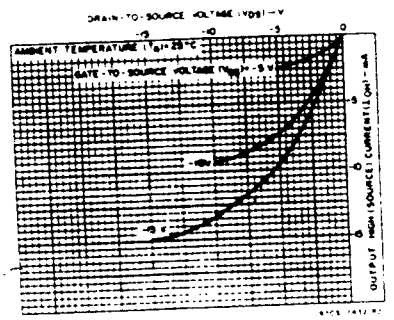


Fig. 4 – Minimum output high (source) current characteristics.

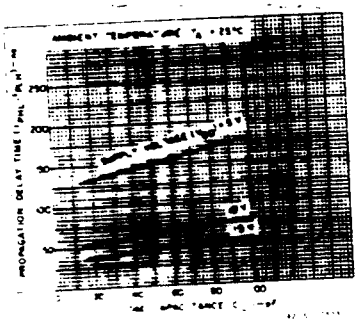
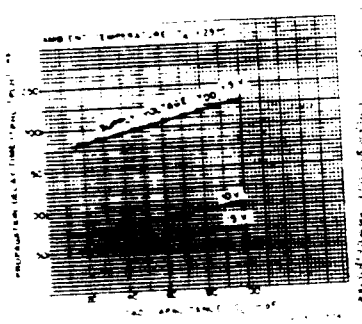


Fig. 5 – Typical propagation delay time vs. load capacitance (CLOCK or SET to Q, CLOCK or RESET to Q).



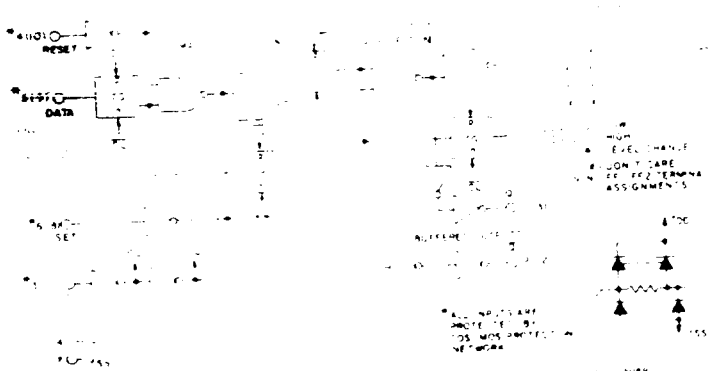


Fig. 7 – Logic diagram and truth table for CD4013B (dual master-slave flip-flop).

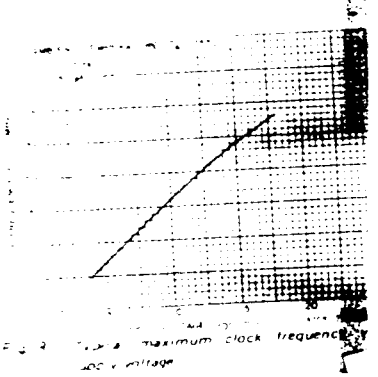


Fig. 8 – Typical maximum clock frequency vs. supply voltage.

CD4013B Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . 0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . 0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A)
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . . +265°C

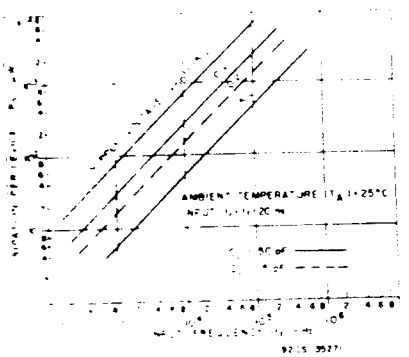


Fig. 9 – Typical power dissipation vs. frequency.

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Propagation Delay Time: Clock to Q or $\overline{Q}$ Outputs t_{PHL}, t_{PLH}	5	–	150	300	ns
	10	–	65	130	
	15	–	45	90	
Set to Q or Reset to $\overline{Q}$ t_{PLH}	5	–	150	300	ns
	10	–	65	130	
	15	–	45	90	
Set to $\overline{Q}$ or Reset to Q t_{PHL}	5	–	200	400	ns
	10	–	85	170	
	15	–	60	120	
Transition Time t_{THL}, t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Maximum Clock Input Frequency Frequency * f_{CL}	5	3.5	7	–	MHz
	10	8	16	–	
	15	12	24	–	
Minimum Clock Pulse Width t_W	5	–	70	140	ns
	10	–	30	60	
	15	–	20	40	
Minimum Set or Reset Pulse Width t_W	5	–	90	180	ns
	10	–	40	80	
	15	–	25	50	
Minimum Data Setup Time t_S	5	–	20	40	ns
	10	–	10	20	
	15	–	7	15	
Clock Input Rise or Fall Time t_{rCL}, t_{fCL}	5	–	–	70	μs
	10	–	–	6	
	15	–	–	2	
Input Capacitance C_{IN}	Any Input	–	5	7.5	pF

*Input t_r, t_f = 5 ns.

TEST CIRCUITS

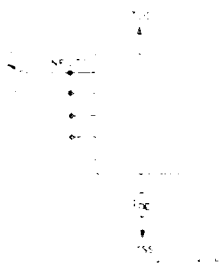


Fig. 10 – Quiescent device current.

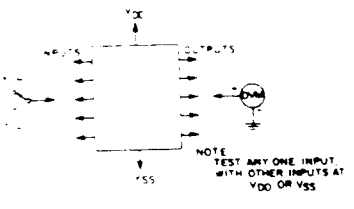


Fig. 11 – Input voltage.

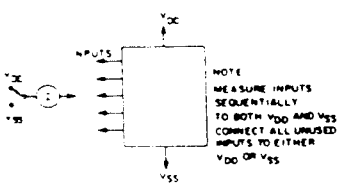
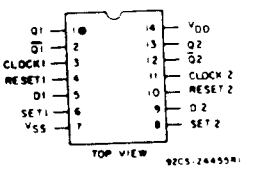


Fig. 12 – Input current.



TERMINAL ASSIGNMENT

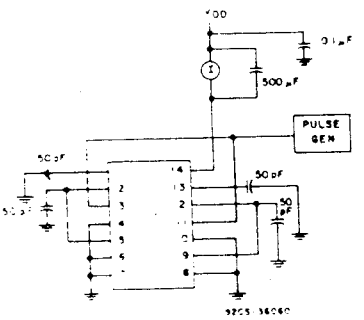
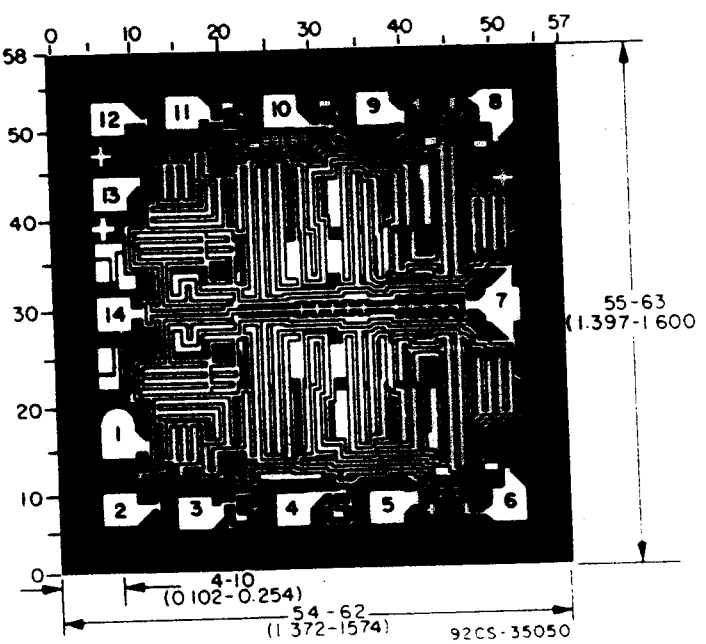


Fig. 13—Dynamic power dissipation test circuit

DIMENSIONS AND PAD LAYOUT FOR CD4013BH



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of ±3 mils to ±16 mils applicable to the nominal dimensions shown.

CD4028B Types

CMOS BCD-to-Decimal Decoder

High-Voltage Types (20-Volt Rating)

The RCA-CD4028B types are BCD-to-decimal or binary-to-octal decoders consisting of buffering on all 4 inputs, decoding logic gates, and 10 output buffers. A BCD code applied to the four inputs, A to D, results in a high level at the selected one of 10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A through C is decoded in octal code at output 0 to 7 if D = "0". High drive capability is provided at all outputs to enhance dc and dynamic performance in high fan-out applications.

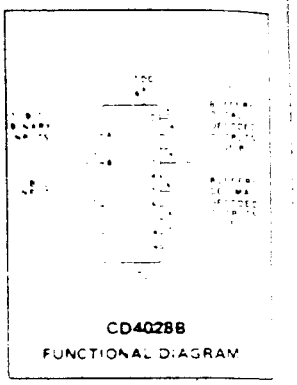
The CD4028B-Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features

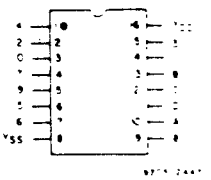
- BCD-to-decimal decoding or binary-to-octal decoding
- High decoded output drive capability
- "Positive logic" inputs and outputs. . . . . decoded outputs go high on selection
- Medium-speed operation. . . . t_{PHL}, t_{PLH} = 80 ns (typ.) @ V_{DD} = 10 V
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range):
  - 1 V at V_{DD} = 5 V
  - 2 V at V_{DD} = 10 V
  - 2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Code conversion
- Indicator-tube decoder
- Address decoding—memory selection control



CD4028B
FUNCTIONAL DIAGRAM



Top View
TERMINAL DIAGRAM

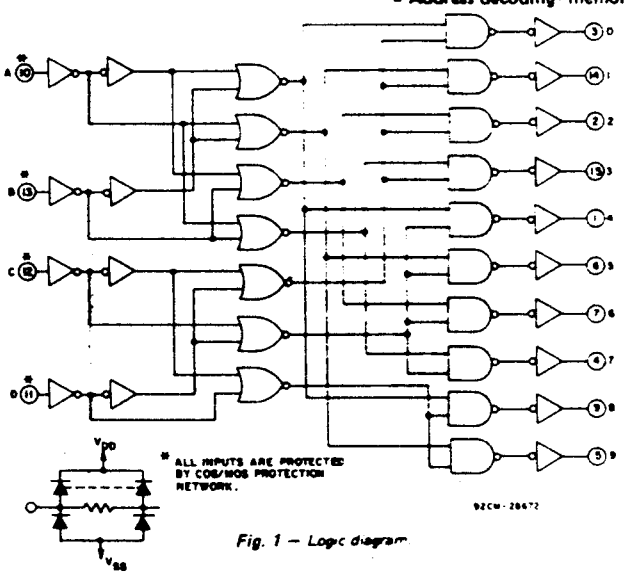


Fig. 1 – Logic diagram

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

TABLE I – TRUTH TABLE

D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

1 = HIGH LEVEL 0 = LOW LEVEL

TABLE II – CODE CONVERSION CHART

INPUTS				INPUT CODES					OUTPUT NUMBER																	
				Hexa-Decimal		Decimal																				
D	C	B	A	4-BIT BINARY	4-BIT GRAY	EXCESS-3	EXCESS-3 GRAY	AIKEN	4,2,2,1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0			0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1			1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	2	3		0	2	2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	3	2	0	3	3		0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	4	7	1	4	4		0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	5	6	2			3	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	6	4	3	1		4	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1	1	1	7	5	4	2			0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	0	8	15	5				0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	9	14	6			5	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	1	0	10	12	7	9		6	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	1	1	11	13	8		5		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	12	8	9	5	6		0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	1	0	1	13	9		6	7	7	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	1	0	14	11		8	8	8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	1	15	10		7	9	9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

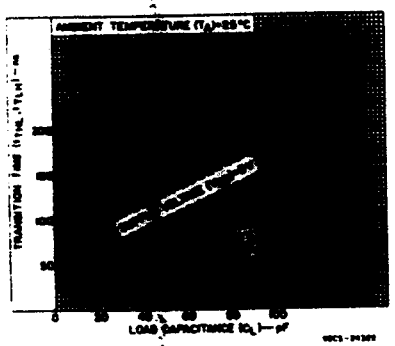


Fig. 8 – Typical transition time as a function of load capacitance.

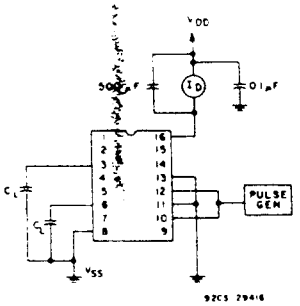


Fig. 10 – Dynamic power dissipation test circuit.

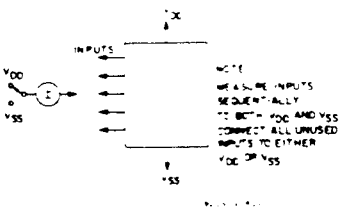


Fig. 9 – Input current test circuit.

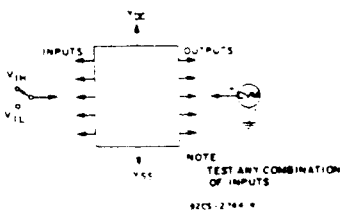


Fig. 11 – Input voltage test circuit.

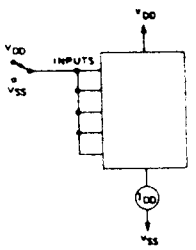


Fig. 12 – Quiescent device current test circuit.

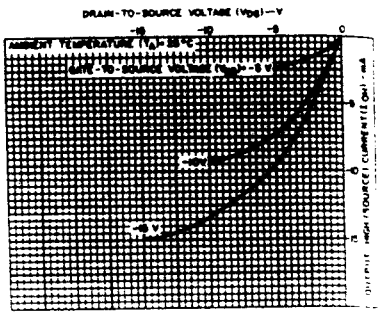


Fig. 6 – Minimum output high (source) current characteristics.

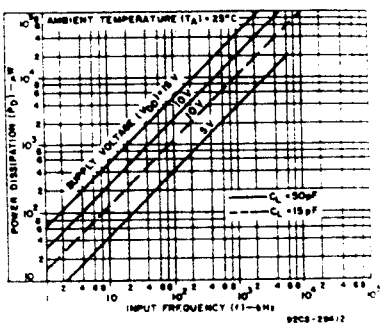


Fig. 7 – Typical dynamic power dissipation as a function of input frequency.

TYPICAL APPLICATIONS

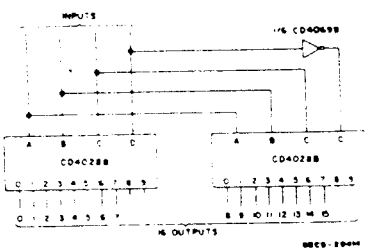


Fig. 13 – Code conversion circuit.

The circuit shown in Fig.13 converts any 4 bit code to a decimal or hexadecimal code. Table 2 shows a number of codes and the decimal or hexadecimal number in these codes which must be applied to the input terminals of the CD4028B to select a particular output. For example: in order to get a high on output No. 8 the input must be either an 8 expressed in 4-Bit Binary code, a 15 expressed in 4-Bit Gray code, or a 5 expressed in Excess-3 code.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, K, H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level V_{OH} Min.	–	0.5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5, 13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5, 13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 50 pF, Input t_r, t_f = 20 ns, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
	V_{DD} (V)	Typ.	Max.	
Propagation Delay Time t_{PHL}, t_{PLH}	5	175	350	ns
	10	80	160	
	15	60	120	
Transition Time t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance, C_{IN}	–	5	7.5	pF

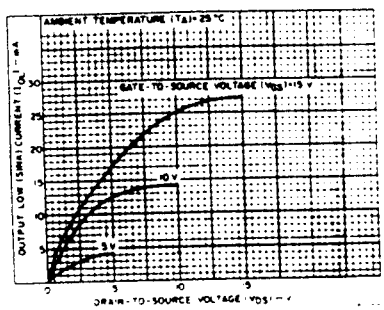


Fig. 2 – Typical output low (sink) current characteristics.

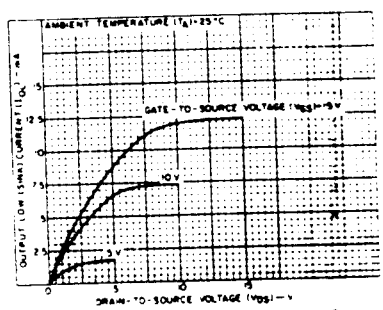


Fig. 3 – Minimum output low (sink) current characteristics.

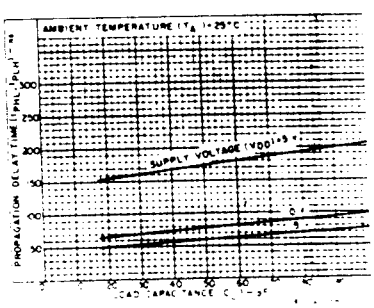


Fig. 4 – Typical propagation delay time as a function of load capacitance.

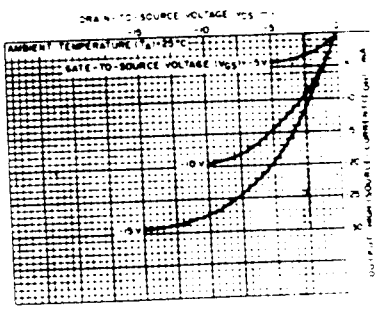


Fig. 5 – Typical output high (source) current characteristics.