MICROCONTROLLER BASED DIGITAL POWER MONITOR

Project Report

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BACHELOR OF ENGINEERING

in **ELECTRONICS AND COMMUNICATION ENGINEERING** of the **BHARATHIAR UNIVERSITY**, Coimbatore.

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Certificate

This is to Certify that the Report entitled

"MICROCONTROLLER BASED DIGITAL POWER METER"

has been submitted by

Ms [illegible]

in partial fulfilment of the requirements for the award of Degree of Bachelor of Engineering in the Electronics and Communication Engineering Branch of the Bharathiar University, Coimbatore - 641 006 during the academic year 1996-'97.

(Guide)

(Head of Department)

Certified that the Candidate was Examined by us in Project Work Viva-Voce Examination held on [illegible] and the University Register Number is 9327EC212, [illegible]

(Internal Examiner)

(External Examiner)

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CHITHRA .K.
DEVI SUGANYA .K.P.

Synopsis

MICROCONTROLLER BASED DIGITAL POWER MONITOR

This project is aimed at developing a digital power monitor employing he Intel 8097BH Microcontroller which is reliable and accurate. The device can measure voltages, currents, powerfactor, frequency, power, voltampere and energy consumed in number of units.

The inputs to the Microcontroller are obtained from voltage and current sensing circuits. Precision rectifier and Signal conditioning circuits are used. Frequency and power factor are obtained by applying pulse waveforms to he High speed I/O unit. Voltages applied to the controller are converted to digital waveforms using the built in A/D converter. Power, Voltampere and number of units are computed using software.

The display used here is 2 rows x 16 columns LCD which is interfaced with the system.

The project has been mainly designed for satisfying the needs of the hree phase users to get accurate results. This objective has been uccessfully achieved by our proposed power monitor.

Contents

INTRODUCTION

neral

There has been rapid changes in technology all over the world. This vancement of science and technology is dependent largely upon a parallel ogress in measurement techniques. One of the quickest ways to access e Science and Technological progress in a nation is to examine the easurement techniques used. As these measurements go hand in hand th revenue and also as it forms an integral part of the nation's financial atus, this meter should be fairly accurate. The power consumed by such eters must also be reduced.

Considering all these requirements and also taking into account the rors and disadvantages of the conventional meters that are in use, the evelopment of a digital power monitor with greater accuracy, reliability and exibility has been attempted in this project.

In any industry monitoring and analysing the power consumption of the achinaries as well as the products are very very essential to improve the roduct quality, life span of the products and reduction in power bills.

Microcontroller based power monitor is a power equipment meant for ne monitoring of various parameters and helps for maximum utilisation of ower at minimum energy cost.

This is a compact and portable equipment which provides built-in onitoring, display and recording facilities. This helps in recording voltage, urrent, frequency and power factor to study fluctuations in the mains supply.

ient Features

1. Voltage Display
2. Current Display
3. Frequency Display
4. Power Factor Display
5. KW Display
6. KVA Display
7. Display of Units of energy Consumed.

ower Monitor

Power Monitor is a device which is used to measure a variety of arameters - voltages, currents, frequency, power factor, power, volt-ampere nd number of units.

The conventional device consists of a panel board with separate meters ntegrated together to measure all these parameters.

Most of these meters incorporate a pointer which moves over a scale to indicate the quantity. Mainly 3 torques are involved.

Deflecting Torque :

The deflecting or operating torque (Td) is produced by utilising any one of the effects like magnetic effect, electrodynamic effect, electromagnetic effect or electrostatic effect. The deflecting torque causes the moving system to move from its `zero' position.

ıtrolling Torque :

The deflection of the moving system would be indefinite if there were controlling or restoring torque. This opposes the deflecting torque and ıter is brought to rest at a position where both are numerically equal. s is obtained by spring or by gravity.

ıping Torque

This acts on the moving system only when it is moving and always poses its motion. If this is not present, pointer will oscillate about its final flected position for some time before coming to rest.

The conventional energy meter has a brake magnet that induces eddy rrents in the disc which revolves continuously. But there are some errors oduced in this case like,

(a) Phase Errors.

(b) Friction compensation and creeping Error.

sadvantages and limitations of conventional meters :

The necessity of the evolution of an alternative for the already existing eter can be clearly understood when following limitations are considered.

1 The meter requires certain minimum amount of power from the signal source for operation. Hence cannot be used for low power measurement.

2. Pointer type indicators can cause human errors in measurements.

3. Presence of moving parts like discs cause friction losses.
4. Power factor variations are not accounted for.
5. Due to magnetic drag and deteriorating nature of magnetic parts, they require calibration once in five years.
6. Needs more space due to presence of mechanical and electrical components which are bulky.
7. Wear and tear causes degradation in accuracy.
8. One main disadvantage is that the meter readings can be altered by illegal means.

crocontroller based power monitor :

The proposed meter is a completely digital instrument and hence has the inherent advantages of a digital circuit. The signal source is not loaded the electronic circuit provides high input impedance which is essential to uce error. The measuring system incorporated has the additional vantage of numerical readout. Hence it reduces human errors in reading d increases reading speed.

The meter employs simple circuit for voltage and current sensing. The nputations for power and the number of units is done using software. quency and power factor are measured directly. This is possible with the o of the 8097 microcontroller which has a built-in A/D converter in it. This eight channels and out of these, six are employed here for the 3 phase rents and voltages.

vantages :

This meter has an edge over all existing meters. It is well suited for

1 Use of electronic components has greatly reduced the amount of power required.

2. Use of 8097 microcontroller has increased the reliability and flexibility.

3. Wide range of operating voltages and currents can be handled by software and hardware adjustments.

4. Accuracy has been greatly improved.

5. Since there are no rotating or moving parts, frictional errors have been completely eliminated.

6. Use of LCD display has reduced the power requirements.

7. Future expansion is easily possible

8. Light weight.

CHOICE OF MICROCONTROLLER

neral

As the heart of the system revolves around the microcontrollers and units computation is done using software, a general understanding of r architecture, instruction sets and comparison with other microcontrollers essential.

A single chip micro-computer, of which microcontrollers are a subset, single integrated circuit that contains the five essential elements of a nputer : input, output, memory, ALU and a control unit. The main difference ong the various models is the type of on-chip program storage, the two tions being no program ROM or some bytes of EPROM.

A major architectural difference among microconotrollers and computers general is the method of accessing I/O ports. The three different proaches are memory mapped I/O, separate I/O and I/O processors. In mory mapped I/O all the I/O is performed as if the I/O devices were mory addresses. In seperate I/O, in addition to a Read/Write control line re is an I/O / memory control line.

Another important feature is that most microcontroller's have versatile ers that can be configured in real time by writing approximate codes to ntrol registers. The timers can be reprogrammed as to the duration that y will measure, type of interrupt, and whether they will reload and continue time the next period automatically. They can also be reconfigured, to act event counters or to count the duration between transitions on the inputs.

Some Microcontroller's make provision for external memory, others ng the possibility of adding external memory. If external memory is ent, it is convenient to erase and reprogram on-chip EPROM program nory.

Thus some of the benefits that arise from having a one chip rocontroller are :

1. Small size and power for the controller portion in an instrument.
2. The opportunity to identify one chip as a kernel for the digital portion of an instrument for test purposes.
3. The definition of an efficient instruction set.

mparison of various microcontrollers

An illustration of a variety of microcontrollers available from INTEL are en below :

Chip	RAM	ROM/EPROM EAROM/EEPROM	CLOCK (Microsec)	I/O Ports	A/D	Timers
el 8021	64	1024 (ROM)	2.5	2 x 8 1 x 4	-	2
el 8022	64	2048 (ROM)	2.5	3 x 8	-	2
el 8035	64	-	2.5	3 x 8	-	2
el 8039	128	-	1.4	3 x 8	-	2
el 8041	64	1024 (ROM)	2.5	3 x 8	-	2
el 8048	64	1024 (ROM)	2.5	3 x 8	-	2
el 8748	64	1024 (EPROM)	2.5	3 x 8	-	2

el 8049	64	2048 (ROM)	1.4	3 x 8	-	2
el 8Y031	128	-	1	4 x 8	-	2
el 8051	128	4096 (ROM)	1	4 x 8	-	2
el 8751	128	4096 (EPROM)	1	4 x 8	-	2
el 8097	232	8192 (EPROM)	0.166	5 x 8	1	2

lection :

It is indeed a great task in selecting a particular controller for our needs m the wide range of microcontroller's available today.

Of all these microcontrollers, a final choice was made on 8097 as this s been designed to be an efficient controller as well as an arithmetic ocessor.

ecifications :

Input :

Nominal Potential Transformer Input : 440 V

Nominal Current Transformer Input : 5 Amps.

Power supply :

Voltage : 440 V + 10%

Frequency : 50 Hz + 6%

Power consumption : 20 watts approximately

equency Measurement :

Resolution : 0.01 Hz

Method : Reciprocal calculation.

Overall Accuracy : Less than 0.5% of full scale.

board

Type : Fully sealed, tactile Keyboard

No : of keys : 2

olay

Type : LCD display - 2 rows, 16 characters in each row.

tus Indicators

Power indicator : Mains on LED.

SYSTEM DESCRIPTION

oduction

The general block diagram of the system is as shown in figure 3.1. It sists of the following blocks :

1. Power supply
2. Transformers
3. Precision Rectifier and Signal Conditioning Circuits
4. Frequency measurement and power factor detection circuits.
5. Controller
6. Keyboard & Display system

stem Description

A general description about the system is given below with ecifications.

wer Supply :

A transformer is used for providing the required voltages to the power pply. Power monitor requires different supply Voltages :

(a) 5V for Microcontroller and associated circuits.

(b) + 5V, - 5V, + 8V, - 8V for signal conditioner.

For providing these voltages, voltage regulators are used. They are three rminal voltage regulators of the series 78xx and 79xx provided with heat nks.

ransformers

The transformers are used for Voltage and Current sensing.

Voltage sensing :-

Potential transformers are used for voltage sensing. They step down three phase voltages to 5V. An output of 5V is produced for 400V rms.

Current sensing :-

Current transformers are used for current sensing. A voltage propotional he current consumed by the load is to be developed in the current sensing cuit. For this we use resistors. This circuit produces an output of 5V peak a maximum load current of 5 Amperes

ecision Rectifier and Signal Conditioning Circuits :

The inputs to these sections come from the transformer outputs. Both e sections use operational amplifiers. The Op - Amp used is LM124, which nternally frequency compensated.

The precision rectifier converts the alternating voltage to a DC voltage. nce the diode is used in feedback path of the OP-Amp the cut-in voltage diode does not pose a problem.

The signal conditioning circuit employs Zero crossing detectors to nvert the outputs of the precision rectifier to a digital form. There are two ch circuits used. One for the voltage O/P and one for the current O/P.

equency measurement and Power factor detection circuits

Frequency measurement is done by using Zero crossing detector. The gnal input is converted into a pulse waveform. The rising edge and trailing dge are noted and difference is found to get the high time. The difference etween the trailing edge and rising edge gives low time. The sum gives the me period. The reciprocal being equal to the frequency.

Power factor is got by finding the difference in position of the rising ges of the current and voltage waveforms. From the principle that one e period corresponds to 360°, the angle corresponding to the difference positions is found. Cosine of the angle gives power factor.

e controller :

The Controller used here is the 8097 with built in RAM, EPROM, timers, d A/D Convertor with eight channels. this forms the heart of the circuit. It 16 bit Intel chip. The built in A/D convertor helps in measuring the voltages d currents by converting the incoming signals to digital form. The High eed input/output units also play an important role in measuring frequency d power factor. The other parameters are computed by using the efficient truction set.

yboard & Display system

A user friendly keyboard with display is provided to interface with the l world.

The display used is the LCD display. It has 2 rows and 16 characters in ch row. The various parameters are displayed using pageup key. Three ase voltage, currents, power factor, KW, KVA, energy consumed and quency are displayed.

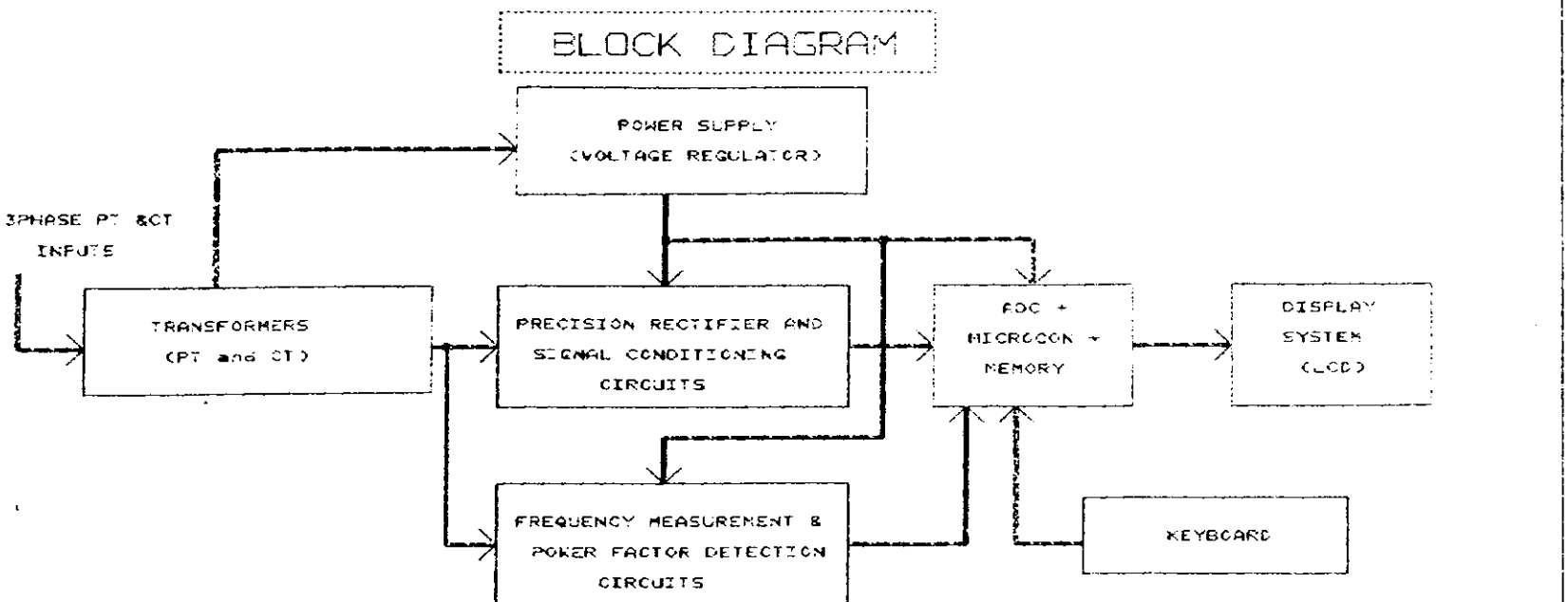

FIG 3.1

Title: MICROCONTROLLER BASED DIGITAL POWER MONITOR		
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MICROCONTROLLER 8097

roduction :

The heart of the system and the software computation revolves around microcontroller.

Some benefits that arise from having a one-chip microcontroller are as ows :

(i) Small size and power for the controller portion of an instrument.

(ii) The opportunity to identify one chip as a kernel for the digital portion of an instrument for test purposes.

(iii) The definition of an efficient instruction set.

lection :

It is indeed a great task in selecting a particular controller for our needs m the wide range of Microcontroller's available today.

Of all these microcontrollers, a final choice was made on 8097 as this s been designed to be an efficient controller as well as an arithmetic ocessor.

The 8097BH can be separted into several sections for the purpose of scribing its operation. There is a 16-bit CPU, a programmable High Speed O unit, an analog to digital converter, a serial port, and a Pulse Width odulated (PWM) output for digital to analog conversion. In addition to these nctional units, there are some sections which support overall operation of e chip such as the clock generator. The CPU and the programmable I/O

U OPERATION

The major components of the CPU on the 8097BH are the Register File
d the RALU. Communication with the outside world is done through either
Special Function Registers (SFRs) or the Memory Controller. The RALU
gister/Arithmetic Logic Unit) does not use an accumulator, it operates
ectly on the 256-byte register space made up of the Register File and the
Rs. Efficient I/O operations are possible by direclty controlling the I/O
ough the SFRs.

U Buses

A "Control Unit" and two busses connect the Register File and RALU.
ure 4.1. shows the CPU with its major bus connections. The two buses
e the "A-Bus" which is 8-bits wide, and the "D-Bus" which is 16-bits wide.
e D-Bus transfers data only between the RALU and the Register File or
ecial Function Registers (SFRs). The A-Bus is used as the address/data
s connecting to the "Memory Controller". Any access of either the internal
M or external memory are done through the Memory Controller.

Within the memory controller is a slave program counter (Slave PC)
ich keeps track of the PC in the CPU. By having most program fetches
m memory referenced to the slave PC, the processor saves time as address
ldom have to be sent to the memory controler. If the address jumps
quence then the slave PC is loaded with a new value and processing
ntinues. Data fetches from memory are also done through the memory
ntroller, but the slave PC is bypassed for this operation.

CPU Register File

The Register File contains 232 bytes of RAM which can be accessed as ytes, words, or double-words. Since each of these locations can be used y the RALU, there are essentially 232 "accumulators". The first word in the egister File is reserved for use as the stack pointer so it cannot be used for ata when stack manipulations are taking place. Address for accessing the egister File and SFRs are temporarily stored in two 8-bit address registers y the CPU hardware.

ALU Control

Instructions to the RALU are taken from the A-Bus and stored emporarily in the instruction register. The Control Unit decodes the structions and generates the correct sequence of signals to have the RALU erform the desired function.

ALU

Most calculations performed by the 8097BH take place in the RALU. he RALU, contains a 17-bit ALU, the Program Status Word (PSW), the rogram Counter (PC), a loop counter, and three temporary registers. All of ie registers are 16-bits or 17-bits (16+Sign extension) wide. Some of the egisters have the ability to perform simple operations to off-load the ALU.

ternal Timing

The 8097BH requires an input clock frequency of between 6.0 MHz nd 12 MHz to function. This frequency can be applied directly to XTALI. ternatively, since XTALI and XTAL2 are inputs and outputs of an inverter, is also possible to use a crystal to generate the clock.

The crystal or external oscillator frequency is divided by 3 to generate he three internal timing phases. Each of the internal phases repeat every 3 scillator periods : 3 oscillator periods are referred to as one "state time", he basic time measurement for 8097BH operations. Most internal operations re synchronized to either with A, B or C, each of which have a 33% duty ycle. Phase A is represented externally by CLKOUT, a signal available on ne 68-pin part. Phases B and C are not available externally. The $\overline{\text{RESET}}$ line an be used to start the 8097BH at an exact time to provide for ynchronization of test equipment and multiple chip systems.

EMORY SPACE

The addressable memory space on the 8097BH consists of 64K bytes, ost of which is available to the user for program or data memory. Locations hich have special purposes are 0000H through 00FFH and 1FFEH through 080H. All other locations can be used for either program or data storage or r memory mapped peripherals. A memory map is shown in Figure 4.2.

egister File

Locations 00H through 0FFH contain the Register File and Special unction Registers, (SFRs). No code can be executed from this internal RAM ection. If an attempt to execute instructions from locations 000H through FFH is made, the instructions will be fetched from external memory. This ection of external memory is reserved for use by Intel development tools. xecution of a nonmaskable interrupt (NMI) will force a call to external cation 0000H, therefore, the NMI and TRAP interrupt are is also reserved r Intel development tools.

The RALU can operate on any of the 256 internal register locations. Locations 00H through 17H are used to access the SFRs. Locations 18H and 19H contain the stack pointer. These are not SFRs, and may be used as standard RAM if stack operations are not being performed. The stack pointer must be initialized by the user program and can point anywhere in the 64K memory space. The stack builds down. There are no restrictions on the use of the remaining 230 locations except that code cannot be executed from them.

Special Function Registers

All of the I/O on the 8097BH is controlled through the SFRs. Many of these registers serve two functions; one if they are read from, the other if they are written to.

There are several restrictions on using special function registers. Neither the source or destination addresses of the Multiply and Divide instructions can be a writable special function register.

These registers may not be used as base or index registers for indirect or indexed instructions.

These registers can only be accessed as bytes unless otherwise specified in Figure 4.3. Note that some of these registers can only be accessed as words, and not as bytes.

Within the SFR space are several registers labeled "RESERVED". These registers are reserved for future expansion and test purposes. Operations should not be performed with these registers as reads from them and writes to them may produce unexpected results. For example, in some versions of the 8097BH writing to location 0CH will set both timers to 0FFXH, This may not be the case in future products, so it should not be

Power Down

The upper 16 RAM locations (0F0H through 0FFH) receive their power from the V_{PD} pin. If it is desired to keep the memory in these locations alive during a power down situation, one need only keep voltage on the V_{PD} pin. The current required to keep the RAM alive is approximately 1 milliamp. To place the 8097BH into a power down mode, the $\overline{\text{RESET}}$ pin is pulled low. To bring the 8097BH out of power down, $\overline{\text{RESET}}$ is held low while V_{CC} is applied.

Reserved Memory Spaces

The locations marked "Reserved" are reserved by Intel for use in testing or future products. They must be filled with the Hex value FFH to insure compatibility with future parts.

Locations 1FFEH and 1FFFH are reserved for Ports 3 and 4 respectively. This is to allow easy reconstruction of these ports if external memory is used in the system. If ports 3 and 4 are not going to be reconstructed, these locations can be treated as any other external memory location. The 9 interrupt vectors are stored in locations 2000H through 2011H.

Locations 2012H through 2017H are reserved for future use. Location 2018H is the Chip Configuration byte. The Jump-To-Self opcodes at locations 201AH and 201BH are provided for EPROM programming. Locations 2020H through 202FH are the security key used with the ROM Lock feature which will be discussed in the next section. All unspecified addresses in locations 2000H through 207FH.

Internal ROM and EPROM

When a ROM part is ordered, or an EPROM part is programmed, the

he interrupt vectors, Chip Configuration Register and Security Key in ocations 2020H through 202FH.

Instruction and data fetches from the internal ROM or EPROM occur nly if the part has a ROM or EPROM, $\overline{EA}$ is tied high, and the address is etween 2000H and 3FFFH. At all other times data is accessed from either ne internal RAM space or external memory and instructions are fetched om external memory. The $\overline{EA}$ pin is latched on $\overline{RESET}$ rising.

lemory Controller

The RALU talks to the memory (except for the locations in the register e and SFR space) through the memory controller which is connected to e RALU by the A-Bus is eight bits wide, the memory controller uses a ave Program Counter to avoid having to always get the instruction location om the RALU. This slave PC is incremented after each fetch. When a jump call occurs, the slave PC must be loaded from the A-Bus before instruction tches can continue.

In addition to holding a slave PC, the memory controller contains a 4 te queue to help speed execution. This queue is transparent to the RALU d to the user unless wait states are forced during external bus cycles. e instruction execution times show the normal execution times with no it states added and the 16-bit bus selected. Reloading the slave PC and ching the first byte of the new instruction stream takes 4 state times.

stem Bus

There are several operating modes on the 8097BH. The standard bus de uses a 16-bit multiplexed address/data bus. Other bus modes include

n 8-bit mode and a mode in which the bus size can dynamically be switched etween 8-bits and 16-bits. In addition, there are several options available n the type of control signals used by the bus.

In the standard mode, external memory is addressed through lines AD_0 rough AD_{15} which form a 16-bit multiplexed (address/data) data bus. These nes share pins with I/O Ports 3 and 4. The falling edge of the Address atch Enable (ALE) line is used to provide a clock to a transparent latch 4LS373) in order to demultiplex the bus. Since the 8097BH's external emory can be addressed as either bytes or words, the decoding is ontrolled with two lines, Bus High Enable ($\overline{BHE}$) and Address/Data Line 0 D_0).

MINGS

Figure 4.4 shows the idealized waveforms related to the following escription of external memory manipulations. When an external memory tch begins, the address latch enable (ALE) line rises, the address is put on D_0-AD_{15} and $\overline{BHE}$ is set to the required state. ALE then falls, the address is ken off the pins, and the $\overline{RD}$ (Read) signal goes low. When $\overline{RD}$ falls, external emory should present its data to the 8097BH.

EAD

The data from the external memory must be on the bus and stable for a nimum of the specified set-up time before the rising edge of $\overline{RD}$. The rising lge of $\overline{RD}$ latches the information into the 8097BH. If the read is for data, e INST pin will be low when the address is valid, if it is for an instruction e INST pin will be high during this time.

/RITE

Writing to external memory requires timings that are similar to those equired when reading from it. The main difference is that the write ($\overline{WR}$) ignal is used instead of the $\overline{RD}$ signal. The timings are the same until the alling edge of the $\overline{WR}$ line. At this poi nt the 8097BH removes the address nd places the data on the bus. When the $\overline{WR}$ line goes high the data should e latched to the external memory.

EADY

A ready line is available on the 8097BH to extend the width of the RD nd WR pules in order to allow access of slow memories or for DMA purposes. the READY line is low by the specified time after ALE falls, the 8097BH ill hold the bus lines to their values at the falling edge of CLKOUT. When ne READY line rises the bus cycle will continue with the next falling edge of LKOUT.

US WIDTH

The 8097BH external bus width can be run-time configured to operate s a standard 16-bit multiplexed address/data bus, or as an 8051 style 16- it address/8-bit data bus.

OFTWARE OVERVIEW

perand Types

- BYTES
- WORDS
- SHORT-INTEGERS
- INTEGERS
- BITS
- DOUBLE-WORDS
- LONG-INTEGERS

PERAND ADDRESSING

. REGISTER-DIRECT REFERENCES

. INDIRECT REFERENCES

. INDIRECT WITH AUTO-INCREMENT REFERENCES

. IMMEDIATE REFERENCES

. SHORT-INDEXED REFERENCES

. LONG-INDEXED REFERENCES

. ZERO REGISTER ADDRESSING

. STACK POINTER REGISTER ADDRESSING

Program Status Word

The program status word (PSW) is a collection of Boolean flags which etain information concerning the state of the user's program.

NTERRUPT FLAGS

The lower eight bits of the PSW are used to individually mask the various sources of interrupt to the 8097BH. A logical `1' in these bit positions enables the servicing of the corresponding interrupt. The mask bits can be accessed as an eight bit byte (INT-MASK-address 8) in the on-board register file. Bit 9 n the PSW is the global interrupt disable. If this bit is cleared then all nterrupts will be locked out except for the Non Maskable Interrupt (NMI). Note that the various interrupts are collected in the INT - PENDING register even if they are locked out.

CONDITION FLAGS

The remaining bits in the PSW are set as side effects of instruction execution and can be tested by the conditional jump instructions.

Z. The Z (Zero) flag is set to indicate that the operation generated a

esult equal to zero. For the add-with-carry (ADDC) and subtract-with-borrow SUBC) operations the Z flag is cleared if the result is non-Zero but is never et. These two instructions are normally used in conjunction with the ADD nd SUB instructions to perform multiple precision arithmetic.

N. The N (Negative) flag is set to indicate that the operation generated negative result. Note that the N flag will be set to the algebraically correct tate even if the calculation overflows.

V. The V (overflow) flag is set to indicate that the operation generated a esult which is outside the range that can be expressed in the destination ata type. For the SHL, SHLB and SHLL instructions, the V flag will be set if ne most significant bit of the operand changes at any time during the shift.

VT. The VT (0 Verflow Trap) flag is set whenever the V flag is set but an only be cleared by an instruction which explicitly operates on it such as he CLRVT or JVT instructions. The operation of the VT flag allows for the esting for a possible overflow condition at the end of a sequence of related rithmetic operations.

C. The C (Carry) flag is set to indicate the state of the arithmetic carry rom the most significant bit of the ALU for an arithmetic operation or the tate of the last bit shifted out of the operand for a shift. Arithmetic Borrow fter a subtract operation is the complement of the C flag.

ST. The ST (STicky bit) flag is set to indicate that during a right shift a has been shifted first into the C flag and then been shifted out. The ST flag s undefined after a multiply operation. The ST flag can be used along with he C flag to control rounding after a right shift.

NTERRUPT STRUCTURE

There are 21 sources of interrupts on the 8097BH. These sources are athered into 8 interrupt types. Each of the eight types of interrupts has its wn interrupt vector. In addition to the 8 standard interrupts, there is a TRAP nstruction which acts as a software generated interrupt.

The programmer must initialize the interrupt vector table with the starting ddress of the appropriate interrupt service routine. Three registers control he operation of the interrupt system : Interrupt Pending, Interrupt Mask nd the PSW which contains a global disable bit.

IMERS

Two 16-bit timers are available for use on the 8097BH. The first is esignated "Timer 1", the Second, "Timer 2". Timer 1 is used to synchronize vents to real time, while Timer 2 can be clocked externally and synchronizes vents to external occurrences.

mer 1

Timer 1 is clocked once every eight state times and can be cleared nly by executing a reset. The only other way to change its value is by writing 000CH but this is a test mode which sets both timers to 0FFFXH and hould not be used in programs.

mer 2

Timer 2 can be incremented by transitions (one count each transition, ing and falling) on either T2CLK or HSI.1. The multiple functionality of the ner is determined by the state of I/O Control Register 0, bit 7 (IOC0.7). To

nsure that all CAM entries are checked each count of Timer 2, the maximum ansition speed is limited to once per eight state times. Timer 2 can be eared by : executing a reset, by setting IOC0.1, by triggering HSO channel EH, or by pulling T2RST or HSI.0 high.

mer Interrupts

Both Timer 1 and Timer 2 can be used to trigger a timer overflow interrupt nd set a flag in the I/O Status Register 1 (IOS1). The interrupts are controlled / IOC1.2 and IOC1.3 respectively. The flags are set in IOS1.5 and IOS1.4,

mer Related Sections

The High Speed I/O unit is coupled to the timers in that the HSI records e value on Timer 1 when transitions occur and the HSO causes transitions occur based on values of either Timer 1 or Timer 2. The baud rate generator n use the T2CLK pin as input to its counter, a complete listing of the nctions of IOS1, IOC0, and IOC1

GH SPEED INPUTS

The High Speed Input Unit (HSI), can be used to record the time at ich an event occurs with respect to Timer1. There are 4 lines (HSI.0 through SI.3) which can be used in the mode and up to a total of 8 events can be corded. HSI.2 and HSI.3 are bidirectional pins which can also be used as O.4 and HSO.5. The I/O Control Registers (IOC0 and IOC1) are used to termine the functions of these pins. A block diagram of the HSI unit is own in Figure 4.5

I Modes

There are 4 possible modes of operation for each of the HSI pins. The

ISI mode register is used to control which pins will look for what type of vents. The 8-bit register is set up as shown if Figure.

ISI FIFO

When an HSI event occurs, a 7 x 20 FIFO stores the 16 bits of Timer 1 and the 4 bits indicating which pins had events. It can take up to 8 state imes for this information to reach the holding register. For this reason, 8 state times must be allowed between consecutive reads of HSI-TIME. When the FIFO is full, oone additional event, for a total of 8 events, can be stored by considering the holding register part of the FIFO. If the FIFO and holding register are full, any additional events will not be recorded.

HSI Interrupts

Interrupts can be generated by the HSI unit in three ways; two FIFO related interrupts and 0 to 1 transitions on the HSI.0 Pin. The HSI.0 pin can generate interrupts even if it is not enabled to the HSI FIFO. Interrupts generated by this pin cause a vector through location 2008H. The FIFO related interrupts are controlled by bit 7 of I/O Control Register 1, (IOC1.7). If the bit is a 0, then an interrupt will be generated every time a value is loaded into the holding register. If it is a 1, an interrupt will only be generated when the FIFO, (independent of the holding register), has six entries in it. Since all interrupts are rising edge triggered, if I0C1.7 = 1, the processor will not be re-interrupted until the FIFO first contains 5 or less records, then contains six or more.

HSI Status

Bits 6 and 7 of the I/O Status register 1 (ISO1) indicate the status of the HSI FIFO. If bit 6 is a 1, the FIFO contains at least six entries. If bit 7 is a 1,

ne FIFO contains at least 1 entry ande the HSI holding register has data vailable to be read. The FIFO may be read after verifying that it contains alid data. Caution must be used when reading or testing bits in IOS1, as nis action clears bits 0-5, including the software and hardware timer overflow ags. It is best to store the byte and then test the stored value.

Reading the HSI is done in two steps. First, the HSI Status register is ead to obtain the current state of the HSI pins and which pins had changed t the recorded time. The format of the HSI-STATUS Register is shown in Figure 4.6. Second, the HSI Time register is read. Reading the Time register nloads one level of the FIFO, so if the Time register is read before the Status register, the event information in the Status register will be lost. The HSI Status register is at location 06H and the HSI Time registers are in ocations 04H and 05H. If the HSI - TIME register is read without the holding egister being loaded, the returned value will be indeterminate. Under the same conditions, the four bits in HSI - STATUS indicating which events have occurred will also be indeterminate. The four HSI - STATUS bits which ndicate the current state of the pins will always return the correct value.

HIGH SPEED OUTPUTS

The High Speed Output unit, (HSO), is used to trigger events at specific imes with minimal CPU overhead. These events include: starting an A to D conversion, resetting Timer 2, setting 4 software flags, and switching 6 output ines (HSO.0 through HSO.5) Up to eight events can be pending at one time and interrupts can be generated whenever any of these events are triggered. HSO.4 and HSO.5 are bidirectional pins which can also be used as HSI.2 and HSI.3 respectively. Bits 4 and 6 of I/O Control Register 1, (IOC1.4, OC1.6), enable HSO.4 and HSO.5 as outputs

NALOG INTERFACE

The 8097BH can easily interface to analog signals using its Analog to igital Converter and its Pulse-Width-Modulated (PWM) output and HSO nit. Analog inputs are accepted by the 8-input, 10-bit A to D converter. he PWM and HSO units provide digital which can be filtered for use as nalog outputs.

nalog Inputs

A to D conversion is performed on one of the 8 inputs at a time using uccessive approximation with a result equal to the ratio of the input voltage vided by the analog supply voltage. If the ratio is 1.00, then the result will e all ones. The A/D converter is available on selected members of the MCS- 6 family.

/D Commands

Analog signals can be sampled by any one of the 8 analog input pins CH0 through ACH7) which are shared with Port 0. ACH7 can also be used an external interrupt if IOC1.1 is set. The A/D Command Register, at cation 02H, selects which channel is to be converted and whether the nversion should start immediately or when the HSO (Channel #0FH) triggers The A/D command register must be written to for each conversion, even he HSO is used as the trigger. A to D commands are formatted as shown Figure 4.6.

The command register is double buffered so it is possible to write a mmand to start a conversion triggered by the HSO while one is still in gress. Care must be taken when this is done since if a new conversion is

tarted while one is cancelled and the new one is started. When conversion s started, the result register is cleared.

/D Results

Results of the analog conversions are read from the A/D Result Register t locations 02H and 03H. Although these addresses are on a word boundary, ney must be read as individual bytes. Information in the A/D Result register s formatted as shown in Figure 4.6. Note that the status bit may not be set ntil 8 state times after the go command, so it is necessary to wait 8 state mes before testing it.

ulse Width Modulation Output (D/A)

Digital to analog conversion can be done with the Pulse Width Modulation output. The 8-bit counter is incremented every state time. When equals 0, the PWM output is set ot a one. When the counter matches the alue in the PWM register, the output is switched low. When the counter verflows, the output is once again switched high.

O PORTS

There are five 8-bit I/O ports on the 8097BH. Some of these ports are put only, some are output only, some are bidirectional and some have lternate functions. In addition to these ports, the HSI/O unit can be used to rovide extra I/O lines if the timer related features of these lines are not eeded.

Input ports connect to the internal bus through an input buffer. Output orts connect through an output buffer to an internal register that hold the ts to be output. Bidirectional ports consist of an internal register, an input uffer, and an output buffe

Port 0 is an input port which is also used as the analog input for the A D converter. Port 1 is a quasi-bidirectional port. Port 2 contains three pes of port lines: quasi-bidirectional, input and output. The input and output nes are shared with other functions in the 8097BH. Ports 3 and 4 are pendrain bidirectional ports which share their pins with the address/data us.

put Ports

Input ports and pins can only be read. There are no output drivers on ese pins. The input leakage of these pins is in the microamp range. The apacitance on these pins is approximately 5 pF and will instantaneously crease by around 5 pF when the pin is being sampled by the A to D nverter.

utput Ports

Output pins include the bus control lines, the HSO lines and some of ort 2. These pins can only be used as outputs as there are no input buffers nnected to them. It is not possible to use immediate logical instructions ch as XOR PORTS, # 00111B to toggle these pins. The output currents on ese ports is higher than that of the quasi-bidirectional ports.

TATUS AND CONTROL REGISTERS

There are two I/O Control registers, IOC0 and IOC1. IOC0 controls Timer and the HSI lines. IOC1 controls some pin functions, interrupt sources d 2 HSO pins.

Whenever input lines are switched between two sources, or enabled, it possible to generate transitions on these lines. This could cause problems

th respect to edge sensitive lines such as the HSI lines, Interrupt line and mer 2 control lines.

O Control Register 0 (IOC0)

IOC0 is located at 0015H. The four HSI lines can be enabled or disabled the HSI unit by setting or clearing bits in IOC0. Timer 2 functionos including ock and reset sources are also determined by IOC0. The control bit cations are show in Figure 4.7.

O Control Register 1 (IOC1)

IOC1 is used to select some pin functions and enable or disable some terrupt sources. Its location is 0016H. Port pin P2.5 can be selected to be e PWM output instead of a standard output. The external interrupt source an be selected to be either EXTINT (same pin as P2.2) or Analog Channel 7 CH7, same pin as PO.7). Timer 1 and Timer 2 overflow interrupts can be dividullay enabled or disabled. The positions of the IOC1 control bits are nown in Figure 4.7.

O Status Register 0 (IOS0)

There are two I/O Status registers, IOS0 and IOS1, IOS0, located at 015H, holds the current status of the HSO lines and CAM. The status bits f IOS0 are shown in Figure 4.7.

O Status Register 1 (IOS1)

IOS1 is located at 016H. It contairs status bits for the timers and the SI/O. The positions of these bits are shown in Figure 4.7.

ESET

eset Signal

As with all processors, the 8097BH must be reset each time the power turned on. This is done by holding the $\overline{\text{RESET}}$ pin low for atleast 2 state mes after the power supply is within tolerance and the oscillator has tabilized.

After the $\overline{\text{RESET}}$ pin is brought high, a ten state reset sequence is xecuted, During this time, the Chip Configuration Byte (CCB) is read from ocation 2018H and written to the 8097BH Chip Configuration Register (CCR). the voltage on the $\overline{\text{EA}}$ pin selects the internal/external execution mode the CB is read from internal ROM/EPROM. If the voltage on the $\overline{\text{EA}}$ pin selects ne external execution only mode the CCB is read from external memory.

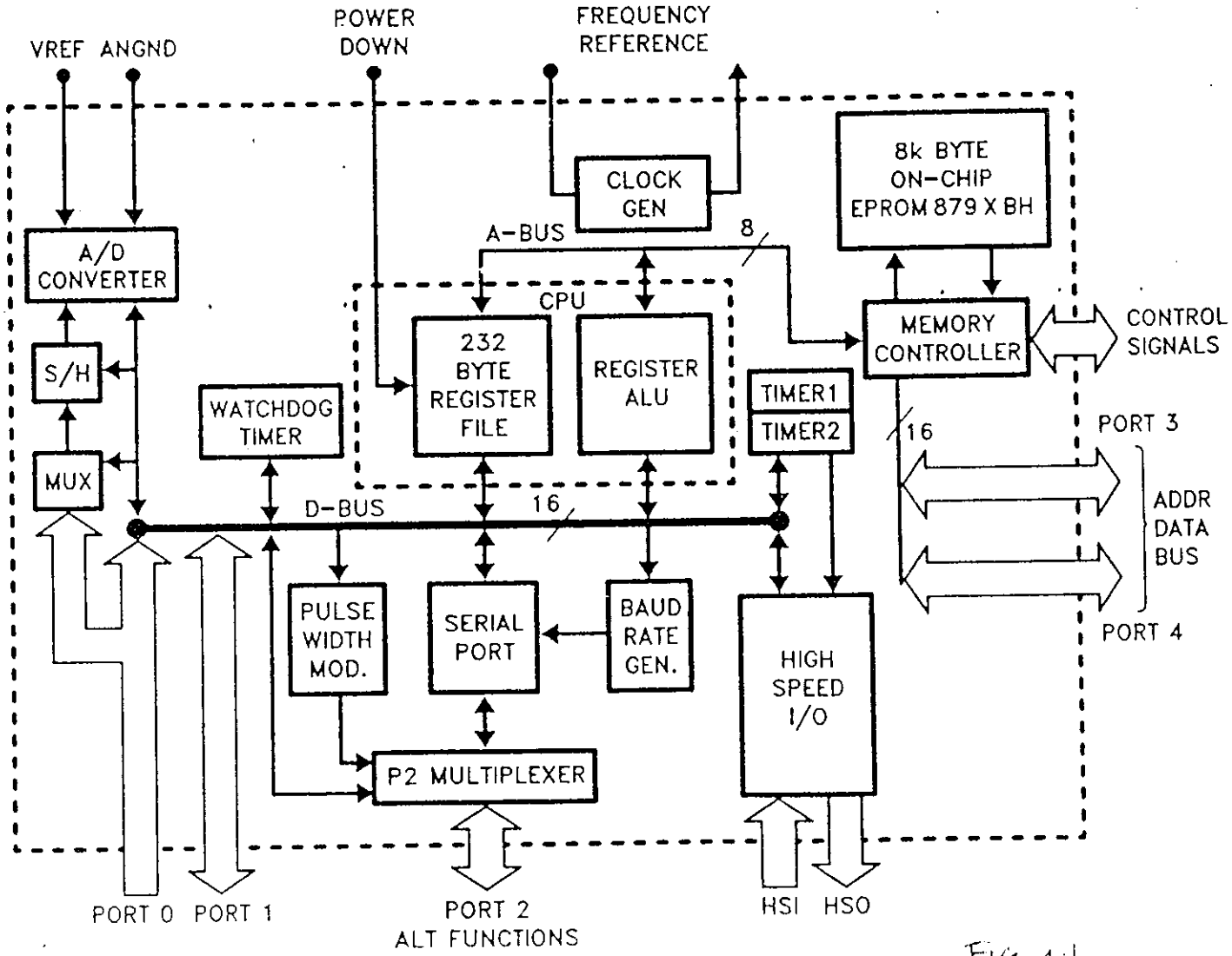
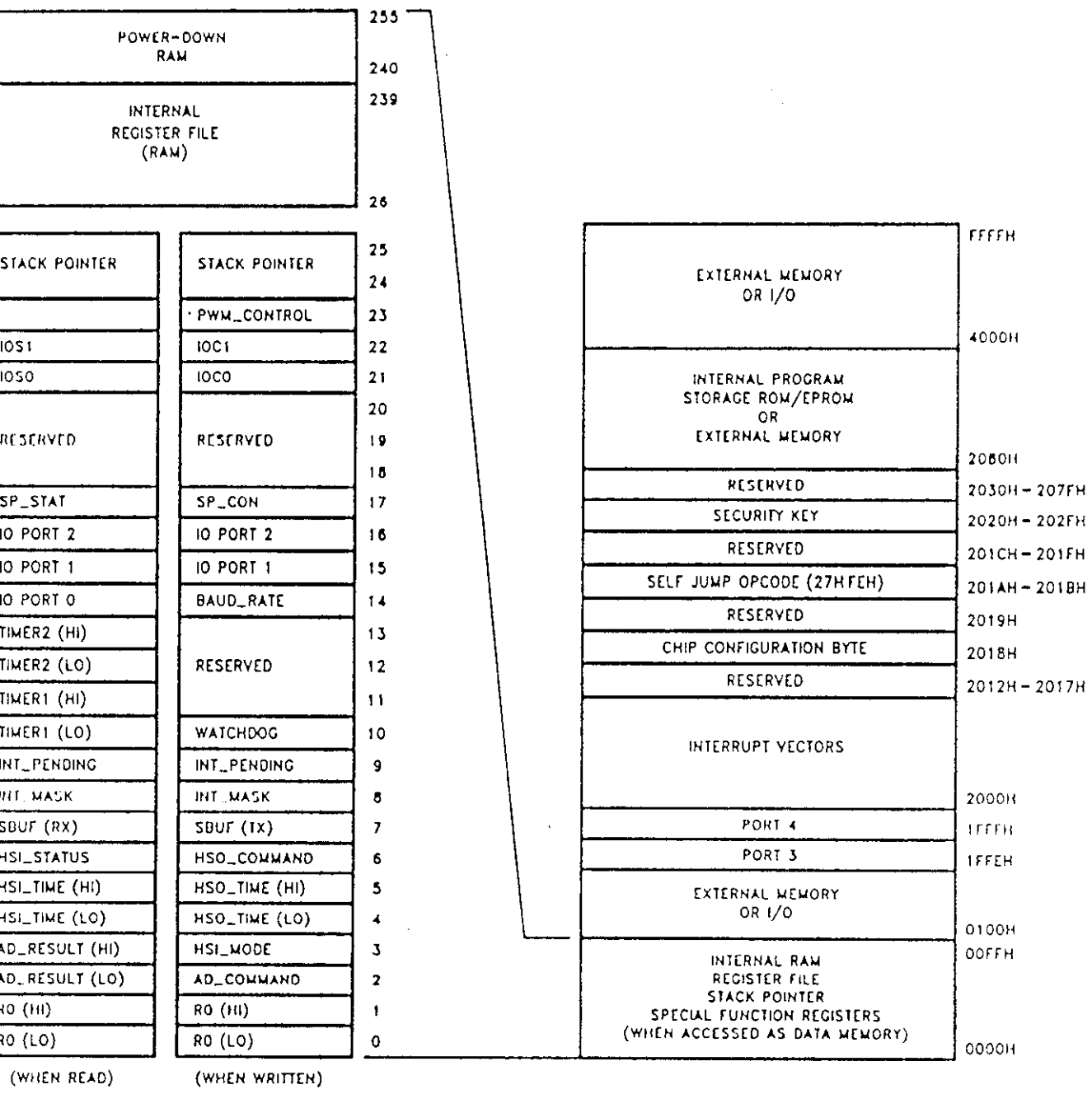


FIG 4-1

270250-1

emory Map



270250-5

Fig. 4.2.

Register	Description	Section
R0	Zero Register — Always reads as a zero, useful for a base when indexing and as a constant for calculations and compares.	3
AD_RESULT	A/D Result Hi/Low — Low and high order Results of the A/D converter (byte read only)	8
AD_COMMAND	A/D Command Register — Controls the A/D	8
HSI_MODE	HSI Mode Register — Sets the mode of the High Speed Input unit.	6
HSI_TIME	HSI Time Hi/Lo — Contains the time at which the High Speed Input unit was triggered. (word read only)	6
HSO_TIME	HSO Time Hi/Lo — Sets the time or count for the High Speed Output to execute the command in the Command Register. (word write only)	7
HSO_COMMAND	HSO Command Register — Determines what will happen at the time loaded into the HSO Time registers.	7
HSI_STATUS	HSI Status Registers — Indicates which HSI pins were detected at the time in the HSI Time registers and the current state of the pins.	6
SBUF (TX)	Transmit buffer for the serial port, holds contents to be outputted.	9
SBUF (RX)	Receive buffer for the serial port, holds the byte just received by the serial port.	9
INT_MASK	Interrupt Mask Register — Enables or disables the individual interrupts.	4
INT_PENDING	Interrupt Pending Register — Indicates that an interrupt signal has occurred on one of the sources and has not been serviced.	4
WATCHDOG	Watchdog Timer Register — Written to periodically to hold off automatic reset every 64K state times.	12
TIMER1	Timer 1 Hi/Lo — Timer 1 high and low bytes. (word read only)	5
TIMER2	Timer 2 Hi/Lo — Timer 2 high and low bytes. (word read only)	5
IOPORT0	Port 0 Register — Levels on pins of port 0.	10
BAUD_RATE	Register which determines the baud rate, this register is loaded sequentially.	9
IOPORT1	Port 1 Register — Used to read or write to Port 1.	10
IOPORT2	Port 2 Register — Used to read or write to Port 2.	10
SP_STAT	Serial Port Status — Indicates the status of the serial port.	9
SP_CON	Serial Port Control — Used to set the mode of the serial port.	9
IOS0	I/O Status Register 0 — Contains information on the HSO status	11
IOS1	I/O Status Register 1 — Contains information on the status of the timers and of the HSI.	11
IOC0	I/O Control Register 0 — Controls alternate functions of HSI pins, Timer 2 reset sources and Timer 2 clock sources.	11
IOC1	I/O Control Register 1 — Controls alternate functions of Port 2 pins, timer interrupts and HSI interrupts.	11
PWM_CONTROL	Pulse Width Modulation Control Register — Sets the duration of the PWM pulse.	8

FIG 4-3.

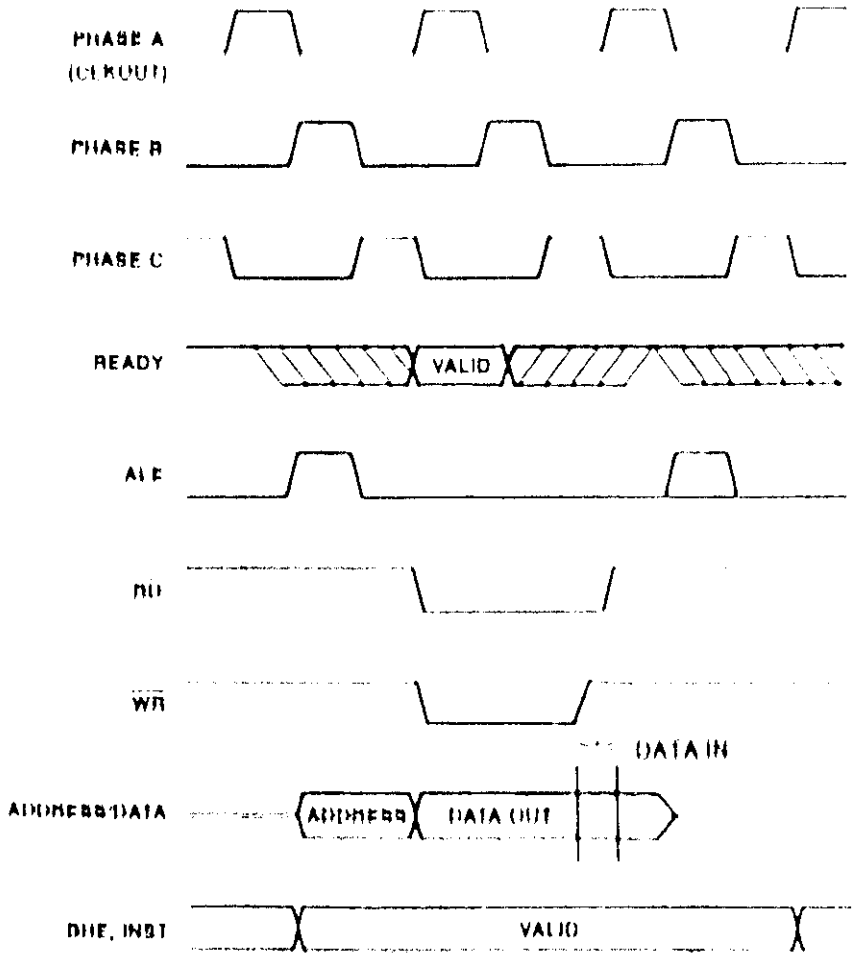
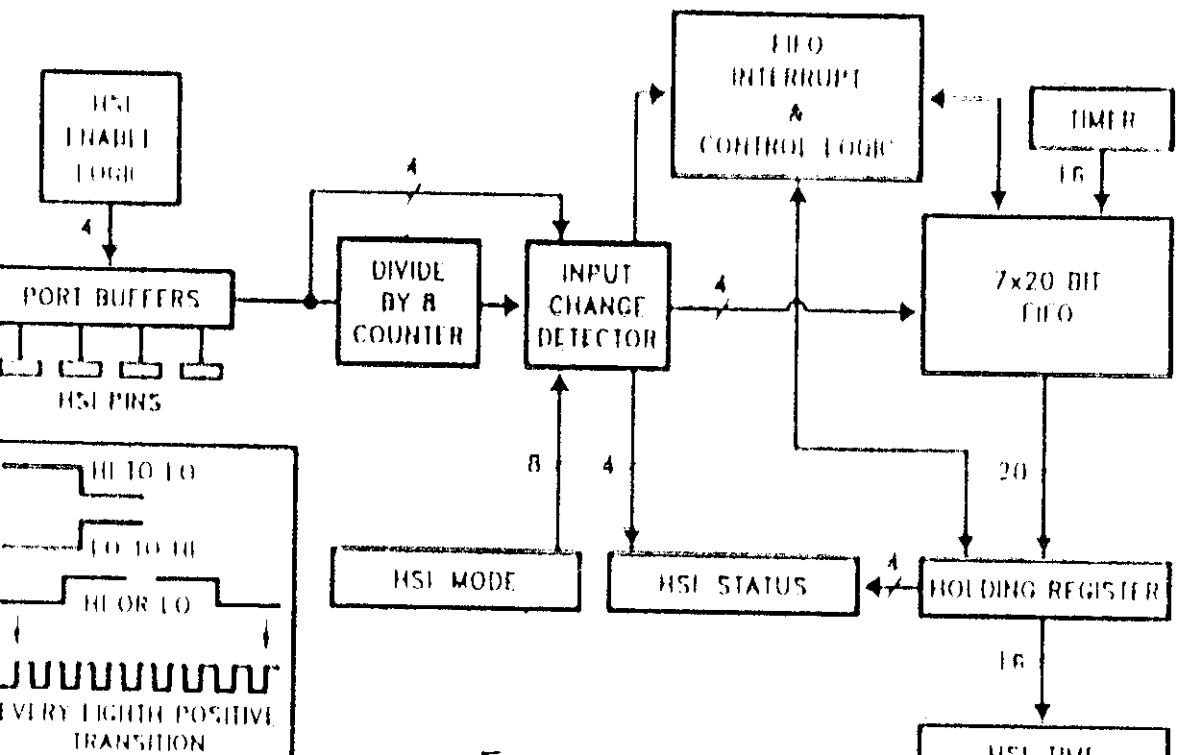
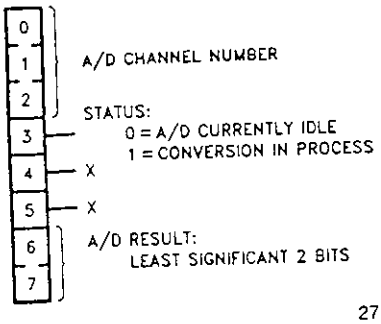

PHASE A
(CLKOUT)
PHASE B
PHASE C
READY
VALID
ALE
RD
WR
DATA IN
ADDRESS/DATA
ADDRESS
DATA OUT
DEN, INST
VALID

FIG. 4-4


HSI ENABLE LOGIC
4
PORT BUFFERS
HSI PINS
4
DIVIDE BY 8 COUNTER
INPUT CHANGE DETECTOR
FIFO INTERRUPT & CONTROL LOGIC
TIMER
16
4
7x20 BIT FIFO
8
4
20
HSI MODE
HSI STATUS
4
HOLDING REGISTER
16
HI TO LO
LO TO HI
HI OR LO
EVERY EIGHTH POSITIVE TRANSITION

A/D Result LO (02H)



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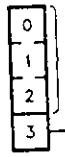
A/D Command (02H)



CHANNEL # SELECTS WHICH OF THE 8 ANALOG INPUT CHANNELS IS TO BE CONVERTED TO DIGITAL FORM.

GO INDICATES WHEN THE CONVERSION IS TO BE INITIATED (GO = 1 MEANS START NOW, GO = 0 MEANS THE CONVERSION IS TO BE INITIATED BY THE HSO UNIT AT A SPECIFIED TIME).

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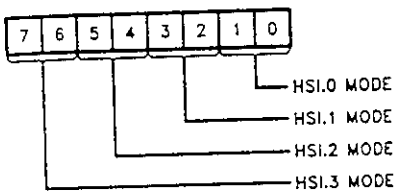
HSI_Mode (03H)

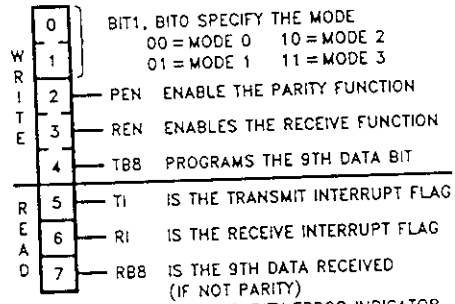


WHERE EACH 2-BIT MODE CONTROL FIELD DEFINES ONE OF 4 POSSIBLE MODES:

00 8 POSITIVE TRANSITIONS
01 EACH POSITIVE TRANSITION
10 EACH NEGATIVE TRANSITION
11 EVERY TRANSITION (POSITIVE AND NEGATIVE)

270250-49

SPCON/SPSTAT (11H)



270250-52

Baud Rate Calculations

Using XTAL1:

$$\text{Mode 0: } \frac{\text{Baud}}{\text{Rate}} = \frac{\text{XTAL1 frequency}}{4*(B+1)};\ B \neq 0$$

$$\text{Others: } \frac{\text{Baud}}{\text{Rate}} = \frac{\text{XTAL1 frequency}}{64*(B+1)}$$

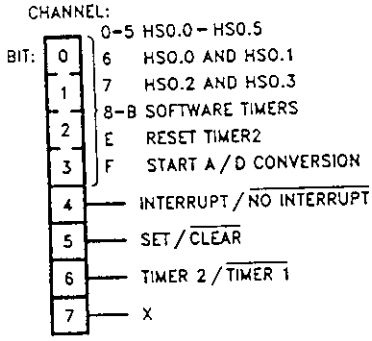
Using T2CLK:

$$\text{Mode 0: } \frac{\text{Baud}}{\text{Rate}} = \frac{\text{T2CLK frequency}}{B};\ B \neq 0$$

$$\text{Others: } \frac{\text{Baud}}{\text{Rate}} = \frac{\text{T2CLK frequency}}{16*B};\ B \neq 0$$

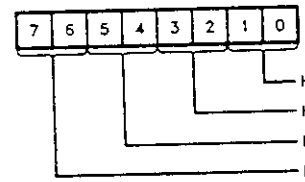
Note that B cannot equal 0, except when using XTAL1 in other than Mode 0.

HSO Command (06H)



270250-50

HSI_Status (06H)



WHERE FOR EACH 2-BIT STATUS FIELD THE LOWER BIT INDICATES WHETHER OR NOT AN EVENT HAS OCCURED ON THIS PIN AND THE UPPER BIT INDICATES THE CURRENT STATUS OF THE PIN.

270250-53

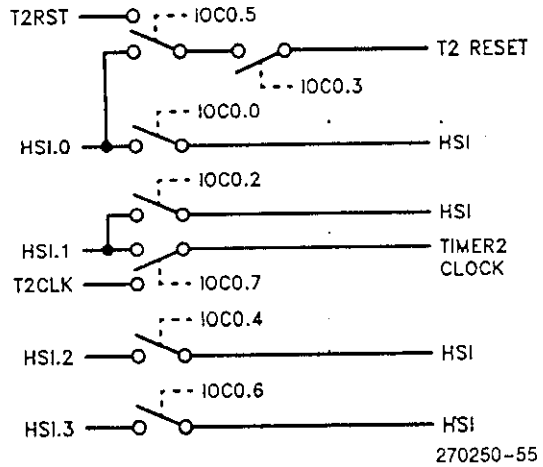
FIG. 4.6.

IOC0 (15H)

0	HSI.0 INPUT ENABLE / $\overline{\text{DISABLE}}$
1	TIMER 2 RESET EACH WRITE
2	HSI.1 INPUT ENABLE / $\overline{\text{DISABLE}}$
3	TIMER 2 EXTERNAL RESET ENABLE / $\overline{\text{DISABLE}}$
4	HSI.2 INPUT ENABLE / $\overline{\text{DISABLE}}$
5	TIMER 2 RESET SOURCE HSI.0 / $\overline{\text{T2RST}}$
6	HSI.3 INPUT ENABLE / $\overline{\text{DISABLE}}$
7	TIMER 2 CLOCK SOURCE HSI.1 / $\overline{\text{T2CLK}}$

270250-54

IOC0 (15H)



270250-55

IOS0 (15H)

0	HSO.0 CURRENT STATE
1	HSO.1 CURRENT STATE
2	HSO.2 CURRENT STATE
3	HSO.3 CURRENT STATE
4	HSO.4 CURRENT STATE
5	HSO.5 CURRENT STATE
6	CAM OR HOLDING REGISTER IS FULL
7	HSO HOLDING REGISTER IS FULL

270250-56

IOC1 (16H)

0	SELECT PWM / $\overline{\text{SELECT P2.5}}$
1	EXTERNAL INTERRUPT ACH7 / $\overline{\text{EXTINT}}$
2	TIMER 1 OVERFLOW INTERRUPT ENABLE / $\overline{\text{DISABLE}}$
3	TIMER 2 OVERFLOW INTERRUPT ENABLE / $\overline{\text{DISABLE}}$
4	HSO.4 OUTPUT ENABLE / $\overline{\text{DISABLE}}$
5	SELECT TXD / $\overline{\text{SELECT P2.0}}$
6	HSO.5 OUTPUT ENABLE / $\overline{\text{DISABLE}}$
7	HSI INTERRUPT FIFO FULL / $\overline{\text{HOLDING REGISTER LOADED}}$

270250-57

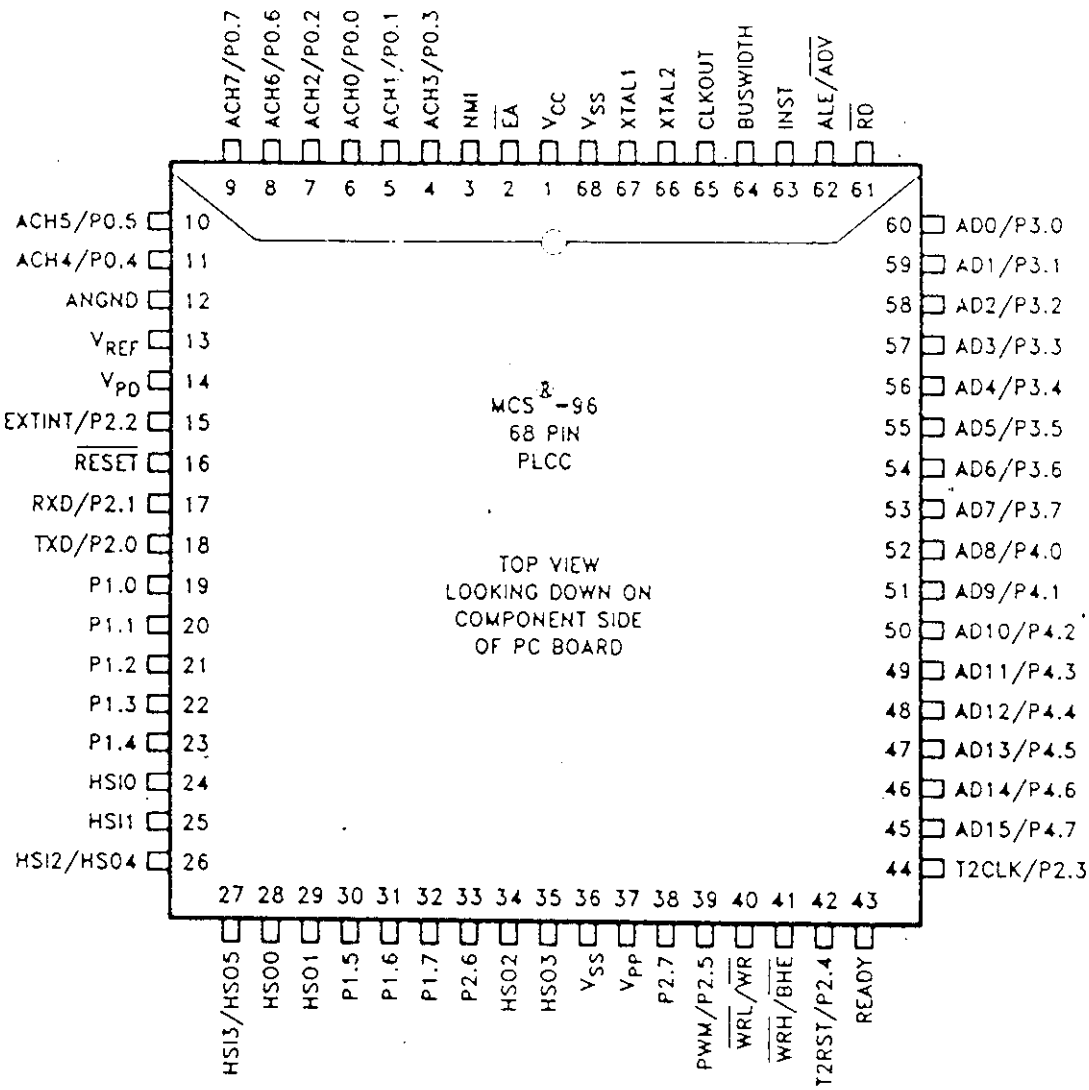
Vector	Vector Location (High Byte)	Vector Location (Low Byte)	Priority
Software	2011H	2010H	Not Applicable
Extint	200FH	200EH	7 (Highest)
Serial Port	200DH	200CH	6
Software Timers	200BH	200AH	5
HSI.0	2009H	2008H	4
High Speed Outputs	2007H	2006H	3
HSI Data Available	2005H	2004H	2
A/D Conversion Complete	2003H	2002H	1
Timer Overflow	2001H	2000H	0 (Lowest)

IOS1 (16H)

0	SOFTWARE TIMER 0 EXPIRED
1	SOFTWARE TIMER 1 EXPIRED
2	SOFTWARE TIMER 2 EXPIRED
3	SOFTWARE TIMER 3 EXPIRED
4	TIMER 2 HAS OVERFLOW
5	TIMER 1 HAS OVERFLOW
6	HSI FIFO IS FULL
7	HSI HOLDING REGISTER DATA AVAILABLE

270250-58

FIG. 4-7


ACH7/P0.7
ACH6/P0.6
ACH2/P0.2
ACH0/P0.0
ACH1/P0.1
ACH3/P0.3
NMI
EA
VCC
VSS
XTAL1
XTAL2
CLKOUT
BUSWIDTH
INST
ALE/ADV
RD
9 8 7 6 5 4 3 2 1 68 67 66 65 64 63 62 61
ACH5/P0.5 10
ACH4/P0.4 11
ANGND 12
VREF 13
VPD 14
EXTINT/P2.2 15
RESET 16
RXD/P2.1 17
TXD/P2.0 18
P1.0 19
P1.1 20
P1.2 21
P1.3 22
P1.4 23
HSI0 24
HSI1 25
HSI2/HSO4 26
60 AD0/P3.0
59 AD1/P3.1
58 AD2/P3.2
57 AD3/P3.3
56 AD4/P3.4
55 AD5/P3.5
54 AD6/P3.6
53 AD7/P3.7
52 AD8/P4.0
51 AD9/P4.1
50 AD10/P4.2
49 AD11/P4.3
48 AD12/P4.4
47 AD13/P4.5
46 AD14/P4.6
45 AD15/P4.7
44 T2CLK/P2.3
MCS®-96
68 PIN
PLCC
TOP VIEW
LOOKING DOWN ON
COMPONENT SIDE
OF PC BOARD
27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43
HSI3/HSO5
HSO0
HSO1
P1.5
P1.6
P1.7
P2.6
HSO2
HSO3
VSS
VPP
P2.7
PWM/P2.5
WRL/WR
WRH/BHE
T2RST/P2.4
READY

270250-43

SUPPORTING IC's

Integrated Circuits play a vital role in the functioning of any system. The integrated circuits used in this systems are :

Three Terminal Positive Regulators

The SG 7800A/7800/140 series of positive regulators offer self contained, fixed-voltage capability with up to 1.5 amps of load current and input voltages up to 50 volts. (SG7800A series only) These units feature a unique on-chip trimming system to set the output voltages to within ±1.5% of nominal on the SG7800A series.

All protective features of thermal shutdown, current limiting and safe area control have been designed into these units and since these regulators require only a small output capacitor for satisfactory performance ease of application is assured.

Although designed as fixed-voltage regulators, the output voltage can be increased through the use of a simple voltage divider. The low quiescent drain current of the device insures good regulation when this method is used.

Product is available in hermetically sealed TO-3, TO-39 and TO-5 power packages as well as the plastic TO-220 package.

Features

- Output voltage set internally to ± 1.5% on SG7800
- Two volt input-output differential
- Excellent line and load regulation
- Foldback current limiting
- Thermal overload protection
- Voltage available --- 5V, 6V, 8V, 12V, 15V, 18V, 20V, 24V

HREE TERMINAL NEGATIVE REGULATORS

ESCRIPTION

The SG 7900A/7900/120/220/320 series of negative regulators offer self-ontained, fixed-voltage capability with up to 1.5 amps of load current. With variety of output voltages and four package options this regulator series is n optimum complement to the SG 7800A/7800/140/240/340 line of three erminal regulators.

These units feature a unique band gap reference which allows the G7900A series to be specified with an output voltage tolerance of ± 1.5%. he SG 7900A versions also offer much improved line regulation haracteristics.

All protective features of thermal shutdown, current limiting, and safe-rea control have been designed into these units and since these regulators equire only a single output capacitor (7900 series) or a capacitor and 5 mA inimum load (SG120 series) for satisfactory performance, ease of pplication is assured.

Although designed as fixed-voltage regulations, the output voltage can e increased through the use of a simple voltage divider. The low quiescent rain current of the device insures good regulation when this method is used, especially for the SG120 series.

EATURES

- Output voltages set internally to ± 1.5% (SG 7900A)
- Output current to 1.5 amp
- Excellent line and load regulation
- Foldback current limiting
- Thermal overload protection

M358 - Low Power Dual Operational Amplifiers

The LM158 series consists of two independent, high gain, intermally equency compensated operational amplifiers which were designed pecifically to operate from a single power supply over a wide range of oltages. Operation from split power supplies is also possible and the low ower supply current drain is independent of the magnitude of the power upply voltage.

Application areas include transducer amplifiers, dc gain blocks and all e conventional op amp circuits which now can be more easily implemented single power supply systems.

nique Characteristics

In the linear mode the input common-mode voltage range includes ground and the output voltage can aslo swing to ground, even though operated from only a single power supply voltage.

The unity gain cross frequency is temperature compensated.

The input bias current is also temperature compensated.

dvantages

Two internally compensated op amps in a single package

Eliminates need for dual supplies

Allows directly sensing near GND and V_{OUT} also goes to GND

Compatible with all forms of logic

Power drain suitable for battery operation

M124 - Low Power Quad Operational Amplifiers

The LM124 series consists of four independent, high gain, internally

pcifically to operate from a single power supply over a wide range of tages Operation from split power supplies is also possible and the low wer supply current drain is independent of the magnitude of the power pply voltage.

Application areas include transducer amplifiers, DC gain blocks and all e conventional op amp circuits which now can be more easily implemented single power supply systems.

nique Characteristics

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage

The unity gain cross frequency is temperature compensated

The input bias current is also temperature compensated

dvantages

- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and Vout also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation.

LM 139 - Low Power Low Offset Voltage Quad Comparators

The LM 139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all our comparators. These were designed specifically to operate from a single

upplies is also possible and the low power supply current drain is ndependent of the magnitude of the power supply voltage. These omparators also have a unique characteristic in that the input common-ode voltage range includes ground, even though operated from a single ower supply voltage.

Application areas include limit comparators, simple analog to digital onverters; pulse, squarawave and time delay generators; wide range VCO; IOS clock timers; multivibrators and high voltage digital logic gates. The M 139 series was designed to directly interface with TTL and CMOS. When perated from both plus and minus power supplies, they will directly interface ith MOS logic.

dvantages

- High precision comparators
- Reduced Vos drift over temperature
- Eliminates need for dual supplies
- Allows sensing near GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

M74HCT138 - 3-to-8 Line Decoder

This decoder utilizes advanced silicon gate CMOS technolegy, and are ell suited to memory address decoding or data routing applications. Both rcuits feature high noise immunity and low power consumption usually ssociated with CMOS circuitry, yet have speeds comparable to low power chottky TTL logic.

The MM74HCT138 have 3 binary

enabled these inputs determine which one of the eight normally high tputs will go low. Two active low and one active high enables (G1, G2A d G2B) are provided to ease the cascading decoders.

The decoders output can drive 10 low power Schottky TTL equivalent ads and are functionally and pin equivalent to 74LS138. All inputs are otected from damage due to static discharge by diodes to Vcc and ground. M74HCT device is intended to interface between TTL and NMOS mponents and standard CMOS devices. These parts are also plug-in placements for LS-TTL devices and can be used to reduce power nsumption in existing designs.

eatures

- TTL input compatible
- Typical propagation delay; 20ns
- Low quiescent current 80 micro amp maximum (74HCT Series)
- Low input current; 1micro amp maximum
- Fanout of 10 LS-TTL loads.

M54HCT373 - TRI-STATE Ocatal D-Type Latch

The MM74HCT373 octal D-type lactches provides the inherent benefits f low power consumption and wide power supply range, but are LS-TTL nput and output characteristic & pin-out compatible. The TRI-STATE output re capable of driving 15 LS-TTL loads. All inputs are protected from damage lue-to static discharge by internal diodes to Vcc and ground.

When the MM74HCT373 LATCH ENABLE input is high, the Q outputs ill follow the D inputs. When the LATCH ENABLE goes low, data at the D nputs will be retained at the outputs until LATCH ENABLE

When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

HM6264 - High Speed Static CMOS RAM

Features

1. Fast Access Time
2. Low Power Standby
3. Low Power Operation
4. Single +5V Supply
5. Completely Static Memory
6. Equal Access And Cycle Time
7. Common Data Input and Output, Three State Output
8. Directly TTL Compatible : All Input and Output
9. Standard 28 Pin Package Configuration
10. Pin out Compatible with 64K EPROM HN482764

27C64 - UV ERASABLE PROMS

27C64 CHMOS EPROM is 64K bit 5V only memory organized as 8192 words of 8 bits. The 27C64 is offered in both a ceramic DIP, Plastic DIP and Plastic Leaded Chip Carrier (PLCC) Packages. A new Quick-Pulse Programming™ Algorithm is employed on Plastic DIP and PLCC devices which may speed up programming by as much as one hundred times. In the absence of Quick-Pulse compatible programming equipment and with Cerdip

AX 232 - Communication Interface

This is a driver / receiver designed for use in RS - 232 communication terfaces. The charge pump circuit converts the single supply to $\pm$ 10V O/P vels. Receiver O/Ps are 3-state TTL/CMOS compatible with I/P levels of oto $\pm$ 30 V. The device has two drivers and two receivers and comes in a 6 pin DIP package.

It has a single + 5V dc supply. The two pins TxD, RxD from the icrocontroller are connected to the 10th and 9th pin of Max 232 espectively. The 7th and 8th pin of Max 232 correspondingly to the TxD, nd RxD are connected to the personal computer.

eatures

. Drivers = 2
. Receivers = 2
. External capacitors = 4 x 1 microfarad
. Pins = 16
. Supply Voltage = 5V dc
. Supply Current Vcc (max) = 10 mA
. I/P voltage range = - 30 to + 30V
. Operating temperature range = 0°C to 70°C

AX 690

This device is designed to protect microprocessors against power ailures by providing a Reset O/P during power UP/DOWN. Battery backup witching for CMOS RAM, CMOS microprocessors or other low power logic included

Features

- ❖ Precision 4.65 V voltage monitor
- ❖ Power OK/Reset time delay of 50ms.
- ❖ Battery back-up power switching
- ❖ Watch dog timer
- ❖ 1 Micro Amp standby current.

Applications :

Computers, controllers, intelligent instruments, automotive systems and critical microprocessor power monitoring.

Technical specifications :

- ✱ Operating Voltage (V_{CC}) = 4.75 to 5.5V

  V_{BAT} = 2 to 4.25 V
- ✱ Supply current = 5 mA (normal), 1 micro amp battery
- ✱ Reset voltage threshold = 4.5 to 4.75 V

DISPLAY AND KEYBOARD SECTION

ntroduction

The display used is the LCD system. It consists of 2 rows, 16 characters n each row. The LCD is the Oriole's Display Module. It is a dot matrix liquid crystal display which displays alphanumerics, Japanese characters and symbols. The built-in controller and driver LSIs provide convenient connectivity between a dot matrix LCD and microprocessors or microcontrollers. All the functions required for dot matrix liquid crystal display drive are internally provided. Internal refresh is provided by the ODM. The CMOS technology makes the device ideal for applications in handheld, portable and other battery powered instruments with low power consumption.

Features

(1) Easy interface with a 4-bit or 8-bit MPU

(2) Built-in Dot Matrix LCD Controller with font 5x7 or 5x10 dots.

(3) Display Data RAM for 80 Characters (80x8 bits)

(4) Character generator ROM, which provides 160 characters with font 5x7 dots and 23 characters with font 5x10 dots.

(5) Bóth display data and character generator RAMs can be read form the MPU.

(6) Internal automatic reset circuit at power ON.

(7) Built-in oscillator circuit.

(8) Wide range of instruction functions:

Clear Display, Cursor Home, Display ON/OF, Cursor Shift, Display Shift.

nterfacing ODM to Microcontroller.

The data bus with MPU is available either for 8 bits 1-operation or 4 bit 2-operation allowing the ODM to be interfaced with the micro controller or microprocessor.

Here the interface data is 4 bits long, hence data is transferred using only 4 bits (DB4 - DB7). Data transfer is completed when 4-bit data is transferred twice. Data of the higher order 4 bits is transferred first, then the lower order 4bits is transferred.

Check the busy flag after 4-bit data has been transferred twice. A 4 bit 2-operation read is used to transfer the busy flag and address counter data.

Chip Select.

The ODM does not have a conventional CS terminal. When ODM is directly connected to the data bus of a micro controller, the enable signal has to be derived from CS or I/O select.

Power Supply Voltage

At the interface of LCD module, there are three power supply terminals V_{DD}, GND and V_0. The LCD is driven by the voltage which is determined by V_{DD}-V_0. Since optimum voltage.of power supply for LCD shifts according to temperature change, Voltage at V_0 terminal needs to be adjusted.

eset

The ODM is automatically initialized when the power is turned on using ne internal reset circuit. The busy flag (BF) holds "H" and does not accept nstructions until initialization ends. The instructions executed in initialization are :

Display Clear
Character Font
No of Lines
Interface Width
Address Counter
Display Shift
Display
Cursor
Blink

Operational Overview

Busy Flag (BF)

When busy flag is high level, it indicates controller is in the internal operation mode and next instruction will not be accepted. The next instruction must be written after the busy flag goes low.

Address Counter (AC)

Address Counter generates the address for the DD RAM, CG RAM and cursor display when an instruction code is written to the controller, after deciding whether it is for DD or CG RAM, address information is transferred

AC. After writing or reading AC is incremented (or decremented) utomatically.

haracter Generator ROM (CG ROM)

This generates 5x10 dot character patterns from the 8-bit character odes. 32 types of 5x10 dot character patterns can be generated.

Character Generator RAM (CG RAM)

The CG RAM is the RAM with which the user can generate character patterns by program. It can store 4 kinds of 5 x 10 dots.

Display Data RAM (DD RAM)

The DD RAM stores display data represented in 8-Bit character codes. ts capacity is 80x8 bits.

Instruction and Display Relationship

For the 4-bit operation using internal reset, the program must set functions prior to the 4-bit operation. When power is turned on 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since nothing is connected to DB_0 - DB_3, function set has to be repeated. However, since subsequent operations are completed in two accesses of 4-bit operation, a rewrite is needed as a function. Thus DB_4 - DB_7 of the function set is written twice, the first write established 4-bit operation and second is the first nibble of the function set instruction.

ESCRIPTION OF INSTRUCTION CODE

ear Display

When this instruction is executed, the LCD display is cleared and eturned to its original status if is was shifted. The cursor goes to the left dge of the display (the left end of the first line if 2-line mode). Space code 20' (hexadecimal) (Character pattern for character code '20' is blank attern) is written into all DD RAM addresses. Sets DD RAM address 0 in ddress counter (AC). Sets I/D = '1' (Increment Mode) of Entry Mode. S of ntry Mode doesn't change.

Return home

The cursor or blink go to the left edge of the display (to the left end of he first line in the 2 line display mode). The display returns to its original status if it was shifted. DD RAM contents do not change. Sets the DD RAM address 0 in address counter.

Entry mode set

I/D : When the I/D is set, the 8-bit character code is written or read to and from the DD RAM, the cursor shifts to the right by 1 character position (I/D='1';increment) or to the left by 1 character position (I/D='0';decrement). The address counter is incremented (I/D='1') or decremented (I/D='0') by 1 at this time. Even after the character pattern code is written or read to and from the CG RAM, the address counter (AC) is incremented (ID='1') or decremented (I/D='0') by 1.

S : Shifts the entire display either to the right or to the left when S is 1;to the eft when I/D=1 and to the right when I/D=0. Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM or when writing into or reading out from the CG RAM when S=0.

Display ON/OFF control

D : The display is ON when D='1' and OFF when D='0'. When off due to D='0', display data remains in the DD RAM. It can be displayed immediately by setting D='1'.

C : The cursor is displayed when C='1' and goes off when C='0'. Even if the cursor disappears, the function of I/D, etc. does not change during display at write. The cursor is displayed using 5 dots in the 8th line when the 5x7 dot character font is selected and 5 dots in the 11th line when the 5x10 dot character font is selected.

B : The character indicated by the cursor blinks when B='1'. The blink is displayed by switching between all black dots and display characters at 409.6 ms interval when fCP or fOSC = 250kHz. The cursor and the blink can be set to display simultaneously. (The blink interval changes according to the reciprocal of fCP or fOSC. 409.6 x 250/270 = 379.2 ms when fCP - 270 kHz.)

Cursor or display shift

Shifts cursor position or display to the right or left without writing or reading display data. This function is used to correct or search for the display. In a 2-line display, the cursor moves to the 2nd line when it passes

the 40th digit of the 1st line. Notice that the 1st and 2nd line displays will shift at the same time. When the displayed data is shifted repeatedly each line only moves horizontally. The 2nd line display does not shift into the 1st line position.

S/C	R/L	
0	0	Shifts the cursor position the left. (AC is decremented by one).
0	1	Shifts the cursor position to the right. (A/C is incremented by one).
1	0	Shifts the cursor position to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

Address counter (AC) contents do not change if the only action performed is shift display.

Function Set

DL : Sets interface data length

When DL='1', the data input/output to and from the MPU is carried out by means of 8bits DB7 to DB0. When DL = '0', the data input/output to and from the MPU is carried out in two steps through the 4 bits DB7 to DB4.

N : Sets number of display lines

The 2-line display mode of the LCD is selected when N='1', while the 1-line display mode is selected when N='0'

F: Sets character font

The 5x7 dots character font is selected when F='0', while the 5x10 dots character font is selected when F='1' and N='0'.

Note : This instruction is to be executed at the start of the program. From this point the function set instruction cannot be executed unless the interface data length is changed i.e. software reset is performed.

N	F	No of display lines	Character font	Duty factor	Remarks
0	0	1	5x7 dots	1/8	
0	1	1	5x10 dots	1/11	
1	*	2	5x7 dots	1.16	cannot display 2 lineswith 5 x 10 dots character font

* No effect

Set CG RAM address

Sets CG RAM address into the Address Counter in binary A5 to A0. In the 5x10 font mode A5 & A4 define the CG RAM block number while A3-A0 define the row within the block. In the 5x7 font mode the CG RAM block is defined by A5-A3 while A2-A0 define the row. Tables 1 and 2 make this clear.

Set DD RAM Address

Sets the DD RAM address into the address counter in binary B6 to B0. Data then written or read from the ODM pertains to the DD RAM. However, when N='0' (1 line display), B6 to B0 is '00' - '4F' (hexa). When

='1' (2-line display), B6 to B0 is '00' - '27' (hexa) for the first line and
0' - '67' (hexa) for the second line.

ead Busy Flag and Address

Reads the busy flag (B/F) that indicates the system is now internally xecuting a previously received instruction. BF = '1' indicates that internal peration is in progress. The next instruction will not be accepted until BF oes '0'. Check the BF status before the next write operation.

At the same time, the value of the address counter expressed in binary C6 to C0 is read. The address counter is used by both Cg and DD RAM ddresses, and its value is determined by the previous instruction.

Write data to CG or DD RAM

Writes binary 8 data DDDDDDDD to the Cg or the DD RAM. Whether the CG or DD RAM is to be written into is determined by the previous specification of CG RAM or DD RAM address setting. After write, the address is automatically incremented or decremented by 1 according to entry mode. The entry mode also determines display shift.

Read data from CG or DD RAM

Reads binary 8 bit data DDDDDDDD from the CG or DD RAM. The previous designation determines whether the CG or DD RAM is to be read. Before entering the read instruction, you must execute either the CG RAM or DD RAM address set instruction. If you don't, the first read data will be invalid.

The 'address set' instruction need not be executed just before the 'read' struction when shifting the cursor by cursor shift instruction (when reading ut DD RAM). The cursor shift instruction operation is the same as that of the D RAM's address set instruction.

After a read, the entry mode automatically increases or decreases the ddress by 1. However, display shift is not executed no matter what the entry node is.

lote : The address counter (AC) is automatically incremented or decremented y 1 after 'write' instructions to either CG RAM or DD RAM. RAM data se- ected by the AC cannot then be read out even if 'read' instruction is ex- ecuted. For correct data read out, execute either the address set instruction only with DD RAM) or 'a shift cursor left' before reading back the data last vritten.

Keyboard Section.

The keyboard section consists of 2 keys.

1) Pageup Key
2) Reset Key

The LCD used is of the 2 row type. After displaying two sets of data, the page up key is pressed to display the next set of data.

Reset key is for complete system resetting.

Both keys are of the Push - Button type.

An ON/OFF switch is provided for the power ON or OFF condition. A Fuse protection is also provided. When the current limit is exceeded, the circuit is cut off from the supply.

Set DD RAM Address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	1	B6	B5	B4	B3	B2	B1	B0

Higher Order Bits — Lower Order Bits

Function set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	1	DL	N	F	*	*

* No effect

Read Busy Flag and Address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	1	BF	C6	C5	C4	C3	C2	C1	C0

Higher Order Bits — Lower Order Bits

Write data to CG or DD RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	D	D	D	D	D	D	D	D

Higher Order Bits — Lower Order Bits

Cursor or display shift

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	1	S/C	R/L	*	*

* No effect

Clear Display

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	0	1

Higher Order Bits — Lower Order Bits

Return home

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	1	*

Higher Order Bits — Lower Order Bits — * No Effect

Entry mode set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

Higher Order Bits — Lower Order Bits

Read data from CG or DD RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	1	D	D	D	D	D	D	D	D

Higher Order Bits — Lower Order Bits

Set CG RAM address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	1	A5	A4	A3	A2	A1	A0

Higher Order Bits — Lower Order Bits

Display ON/OFF control

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	1	D	C	B

Higher Order Bits — Lower Order Bits

WORKING OF THE ENTIRE SYSTEM

The working of the Microcontroller based digital power monitor can be explained by describing the circuits employed in the PCB's used. The main purpose of this system is to monitor and display the 3 phase voltages, 3 phase currents, frequency, power and Energy consumed. For this, the PCB's used are :

(I) Transformer Card
(II) Signal Conditioning Card
(III) Zero Crossing Detector Card and
(IV) Controller Card

The function of the Circuits employed in each card is as follows :

TRANSFORMER CARD

This card is mainly used to convert the 230Vac to 5Vac and 5Amp to 50mA from the mains supply. So step-down transformers are used. For our purpose three potential transformers and four current transformers are used. Appropriate resistors and potentiometers are used to step down the voltages and currents. The current transformer output ie. a current is also converted into a voltage. Then the stepped down 3 phase voltages and 3 phase currents converted into voltages are given as input to the signal conditioning card via a 34 way FRC connector.

GNAL CONDITIONING CARD

For this card the signals from the transformer output act as input. Here e functions like rectifying, filtering, Zero adjustment, Gain adjustment etc., e carried out before sending to the controller section. Here 6 sensing rcuits each for 3 phase voltage & 3 phase current sensing are used. In ach sensing, the first stage which is the rectifier stage consists of half-wave ctifiers. Two half-wave rectifiers are combined to perform the function of a ll wave rectifier. The function of the half-wave rectifier is as follows

An inverting amplifier can be converted into an ideal half-wave rectifier y adding 2 diodes (refer fig 7.1)

When V_i is positive diode D_1 conducts causing V_{0A} to go negative by one iode drop ($\approx$ 0.6V). Hence diode D_2 is reverse biased. The output voltage V_0 s 0, because for all purposes no current flows through D_1 for negative input e. $V_i<0$ diode D_2 conducts and D_1 is off. The negative input V_i forces the utput of Op - Amp positive and Causes D_2 to conduct. The circuit then acts an inverter for $R_1 = R_1$ and output V_0 becomes positive.

Out of the two half-wave rectifiers used, one is non-inverting amplifier and another an inverting amplifier converted into half-wave rectifiers. So in the non-inverting type half-wave rectifier during positive half cycles the diode D_1 is ON and D_2 is OFF and there is an output and during the negative half cycle the output of this half wave rectifier is zero.

The fully rectified output is filtered using lowpass filter in the next stage. The low pass filter circuits is shown in figure 7.2

The low pass filter is a first order low pass filter. A low pass filter can be designed. by implementing the following steps.

(i) Choose a value of high cut-off frequency f_H.

(ii) Select an appropriate value for C_1. Mylar (or) tantalum capacitors are recommended for better performance.

(iii) Calculate the value of R_3 using

$$R_3 = \frac{1}{2\Pi f_H C_1}$$

(iv) Select the value of R_1 and feed back resistor based on desired pass band gain.

The filtered output is fed as input to an inverting amplifier. As the name implies the output from the filter stage is given to the inverting input terminal of the Op-Amp.

The circuit of an inverting amplifier used here is shown in figure 7.3

Here in this inverting amplifier the potentiometer P_1 is used for Zero adjustment of the Op-Amp and potentiometer P_2 is used for gain adjustment. Using P_2 the required output voltage can be obtained.

After these stages the AC input provided at the 5th pin of LM124 is converted into DC voltage output, which is present in pin 14 of the Op-Amp. This O/P DC voltages ie., from the 6 sensing circuits are taken via a 25 way FRC Connector and 4 way relimate connector and these act as input to the controller card.

A circuit for frequency sensing is also available in this card. Here a zero crossing detector is employed. The IC employed is LM358.

POWER SUPPLY UNIT.

The power supply unit is also present in the signal conditioning card. Here we make use of +5v, -5v,+8v and -8v supply. The +8v supply is mainly used as the supply voltage for Op-Amps and + 5v supply is used for all the other IC's. Fixed voltage regulators are mainly employed for power supplies.

The input for the power supply is given from the secondary of the power supply transformer. The secondary AC voltage of 12V - 0 - 12V is given via a 12 way ADD-ON to the input of the power supply. The dual power supply circuit is shown in figure 7.4

Many discrete & IC circuits require bipolar supplies. This can be done easily using two, 3 terminal regulators.

In the circuit diodes D_1 & D_2 are used to protect the regulator against short circuit occurring at its input terminals.

78xx and 79xx corresponds to positive and negative voltage regulator series respectively.

Positive voltage regulators series

The 7800 series consists of 3 terminal positive voltage regulators. These IC's are designed as fixed voltage regulators and with adequate heat sinking can deliver output currents in excess of 1Amp. Although these devices do

ot require external components, such components can be used to obtain djustable voltages and currents. These IC's also have internal thermal verload protection and internal short-circuit current limiting.

Proper operation requires a common ground between input and output voltages and the difference between input and output voltages (Vin - Vo) called dropout voltage, must be typically 2.0v even during the low point on the input ripple voltage.

Negative Voltage Regulators

The 7900 series is fixed output voltage regulators are complements to the 7800 series devices.

Performance parameters of regulators are line regulation, load regulation, temperature stability and ripple rejection.

Line or input regulation

It is defined as the change in output voltage for change in input voltage and it is expressed in millivolts (or) as a % of output voltage V_o.

Load Regulation

It is the change in output voltage for change in load current and is expressed in millivolts (or) as a % of V_0.

emperature stability

It is the change of O/P voltage per unit change in temperature and is expressed in either millivolts/°C (or) parts permillion (PPM)/°C

Ripple Rejection

It is the measure of regulator's ability to reject ripple voltages. It is usually expressed in dB.

The smaller the values of the above parameters, the better the performance of the regulator.

The 7800 regulators can be used as current sources.

Zero Crossing Detector Card.

Zero Crossing Detector is one among the applications of comparator. The circuit is as shown in figure 7.5

It is nothing but a sine to square wave generator.

The zero crossing detector is mainly used for frequency detection and power factor calculation from the time period 'T' of the output waveform of the zero crossing detector. Using software, frequency is calculated as f=1/THz. Power factor is also calculated from the output of the zero crossing detectors and software. Zener diodes are mainly used for protection ie., from avoiding voltages more than 5V to enter the controller section.

ONTROLLER CARD

This card forms the heart of the entire system. The controller used is 097, A sixteen bit microcontroller. It has an inbuilt ADC which performs the unction of digitizing the analog input.

The output of the signal conditioning card is given as input to the controller card via the FRC connector & Reli-mate connector. In the controller card all the manipulations are done using the software ie.. Assembly language programming of 8097 using the input currents, voltages and frequency.

This card consists of RAM, ROM Memories for storing manipulated data. Reset function is incorporated using IC MAX 690 and some passive components. RS232C IC is used for serial interfacing. Latch 74ALS373 is used for separating data from the address. IC 74138 is a 3 to 8 decoder chip present in the controller card which is used as chip select for all the other IC's of the controller card.

In this card the output of the microcontroller is given via a connector to the LCD interface and displayed using a 2 row x 16 characters LCD. The entire system working can be thus understood from the various cards used in the system and their functions.

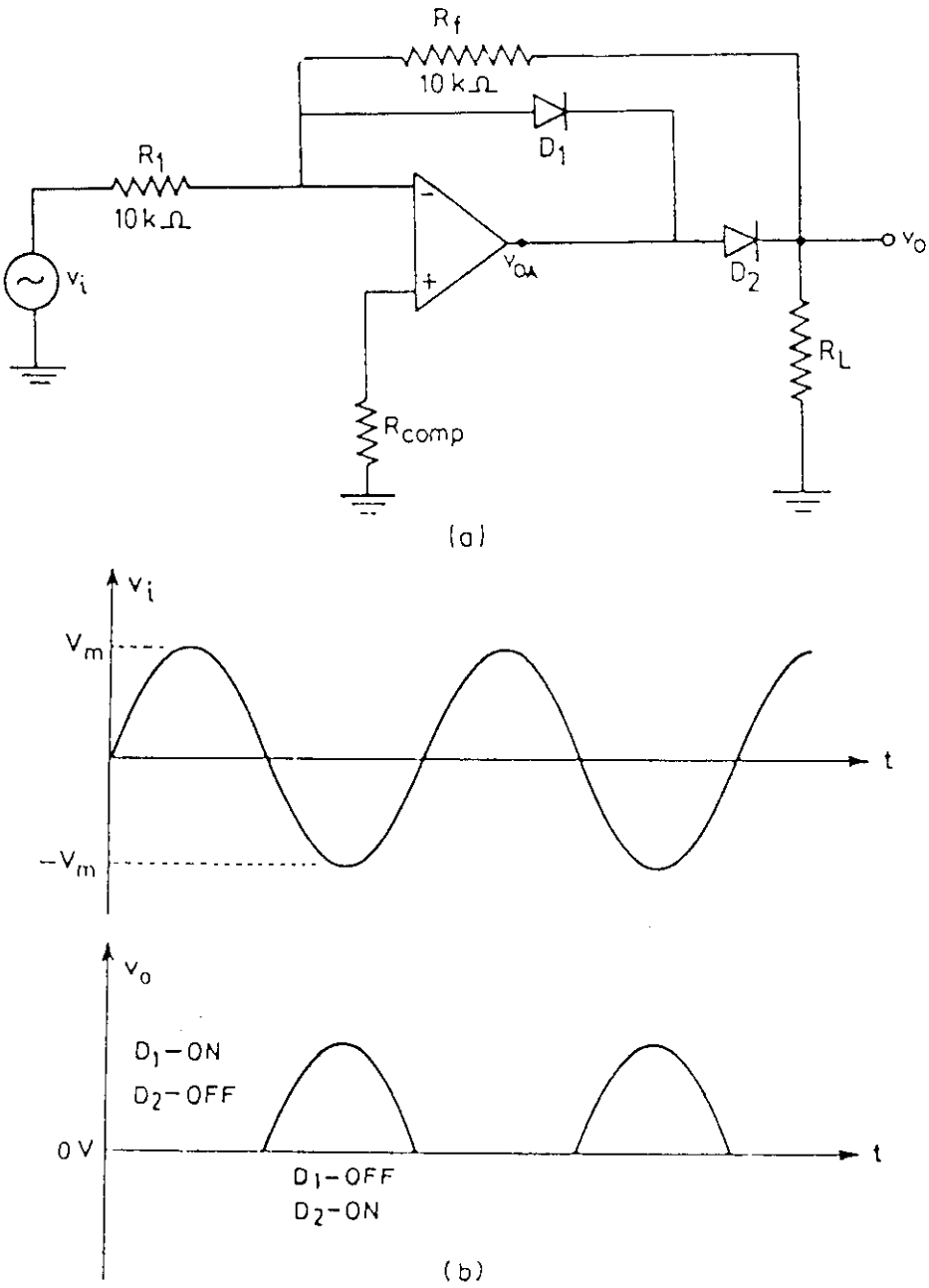

R_f
10 kΩ
D_1
R_1
10 kΩ
v_i
v_{OA}
D_2
v_o
R_L
R_{comp}
(a)
v_i
V_m
$-V_m$
t
v_o
D_1 – ON
D_2 – OFF
0 V
t
D_1 – OFF
D_2 – ON
(b)

FIG: 7.1

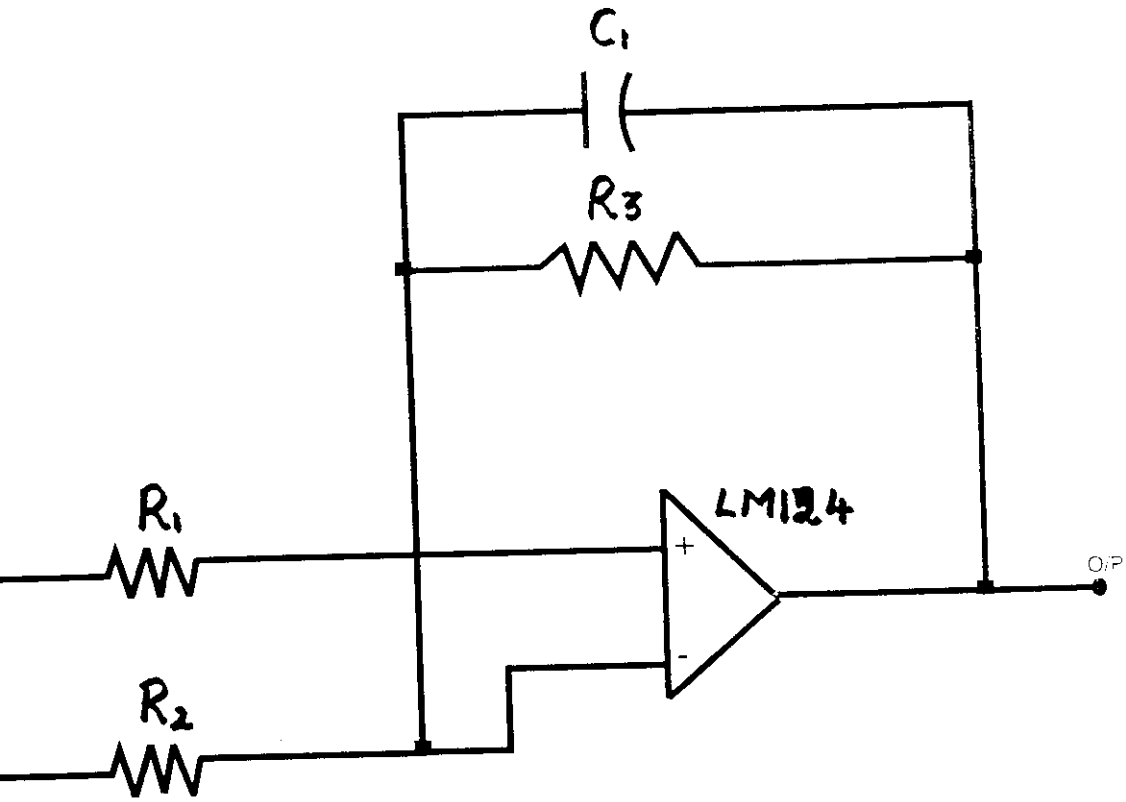
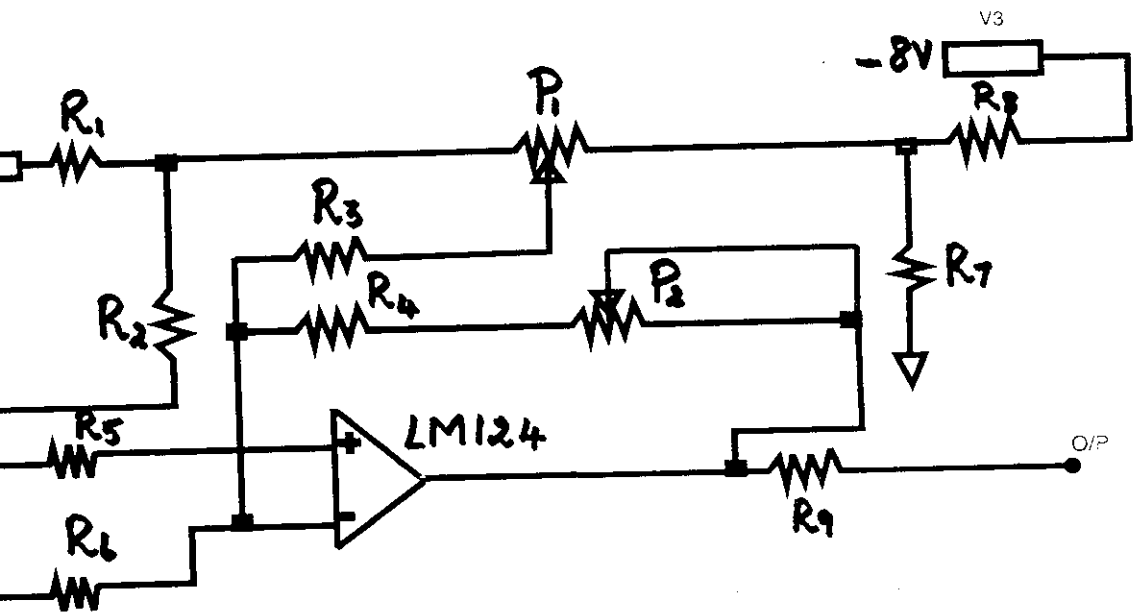
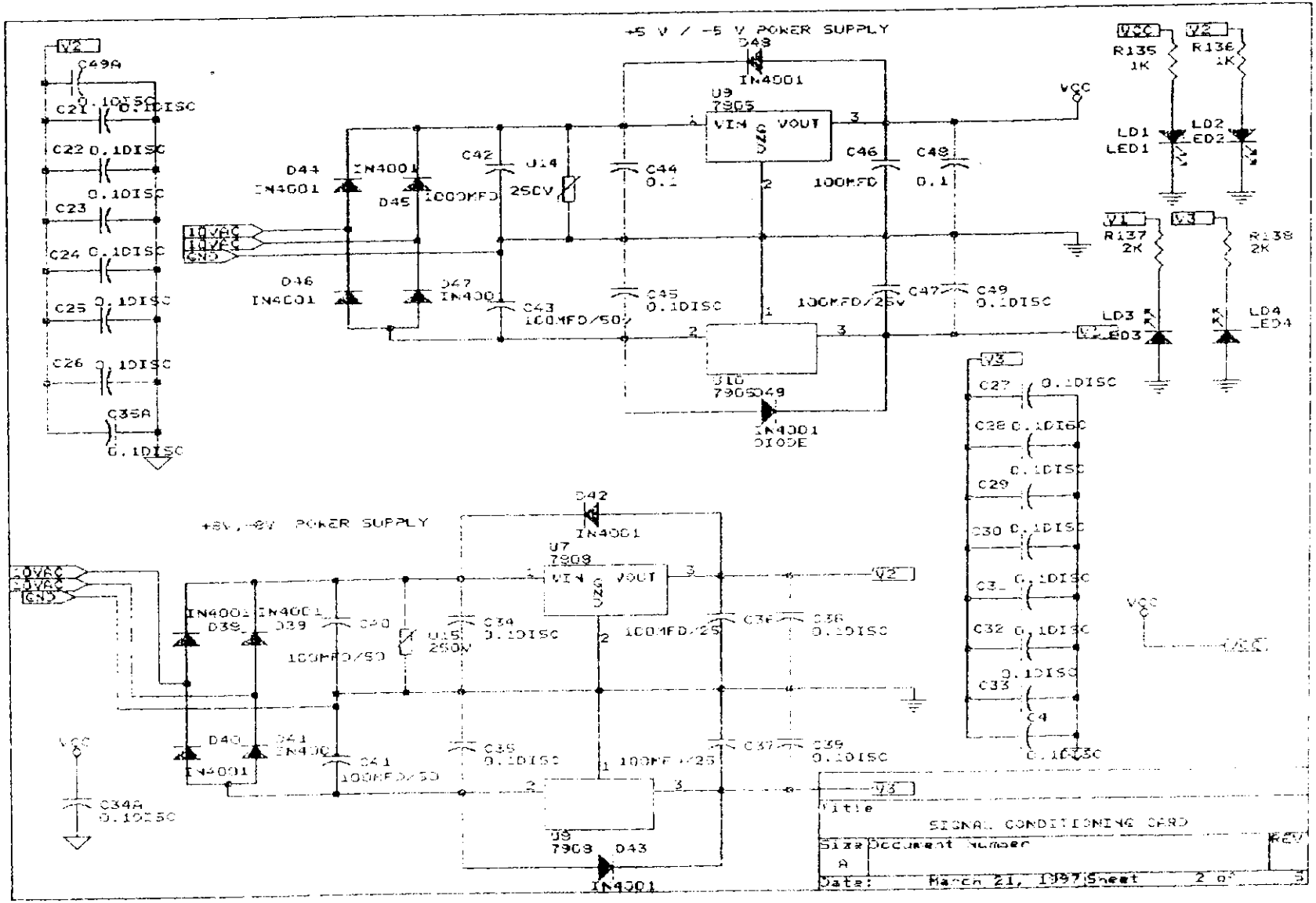


FIG: 7.2




+5 V / -5 V POWER SUPPLY
+8V, -8V POWER SUPPLY
C49A
0.1DISC
C21
C22
C23
C24
C25
C26
C35A
D48
IN4001
U9
7905
VIN
VOUT
VCC
R135
1K
R136
1K
LD1
LED1
LD2
LED2
R137
2K
R138
2K
LD3
LED3
LD4
LED4
D44
D45
D46
D47
C42
U14
100MFD
25CV
C44
0.1
C46
100MFD
C48
0.1
C45
0.1DISC
C43
100MFD/50
100MFD/25V
C47
C49
0.1DISC
U10
7905
D49
IN4001
DIODE
10VAC
GND
C27
C28
C29
C30
C31
C32
C33
C4
D42
U7
7909
D38
D39
C40
100MFD/50
U15
250N
C34
0.1DISC
C36
C38
D40
D41
C41
C35
C37
C39
U8
7908
D43
C34A
0.1DISC
Title
SIGNAL CONDITIONING CARD
Size
A
Document Number
Date:
March 21, 1997
Sheet
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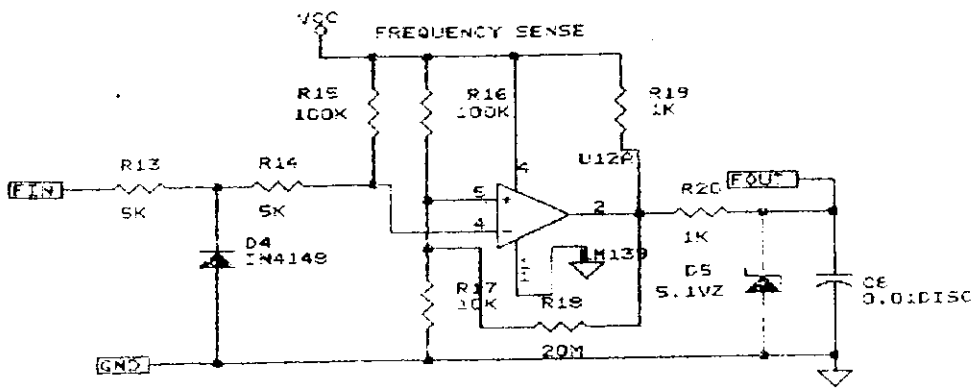
3



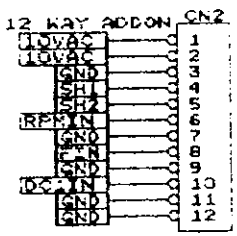
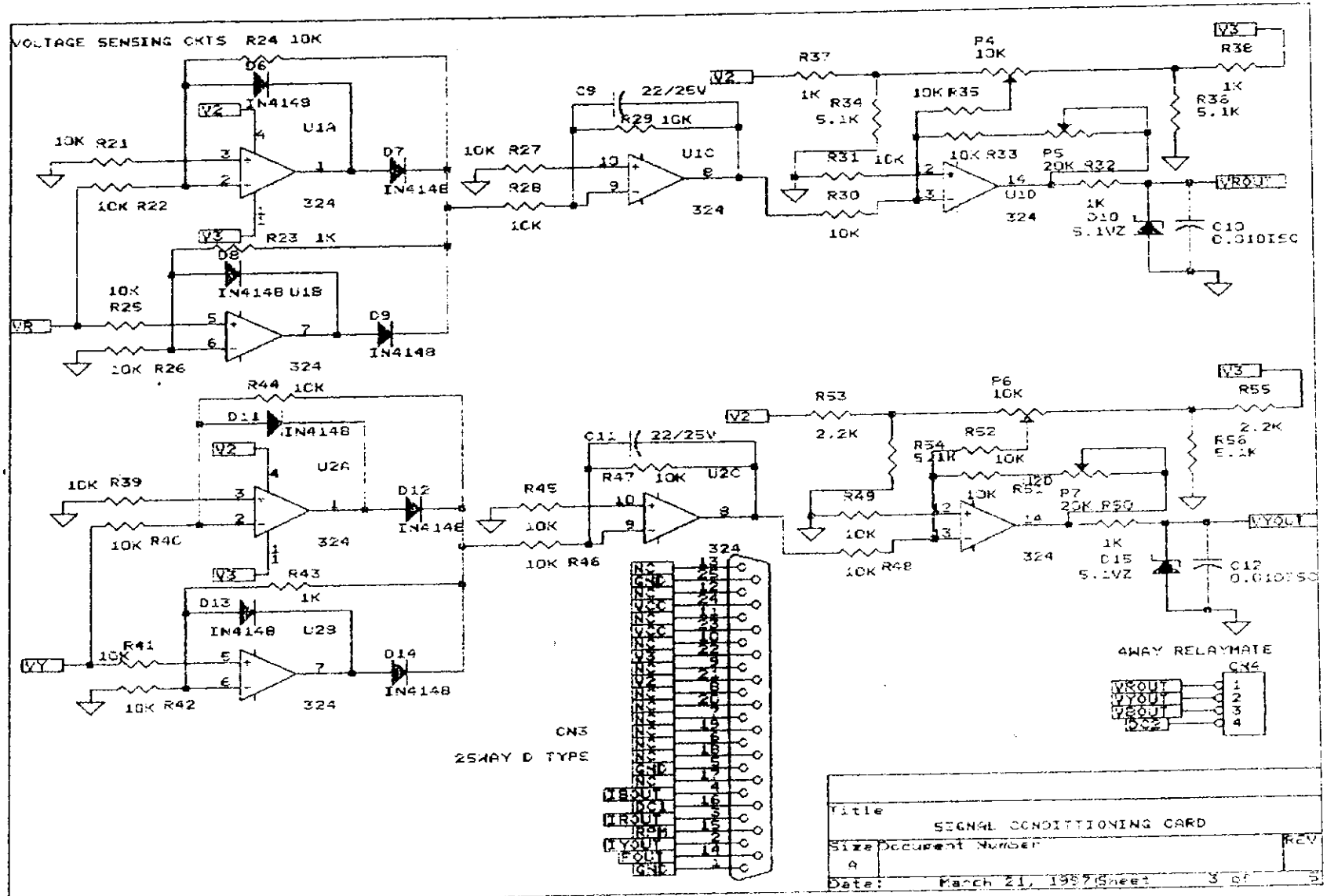
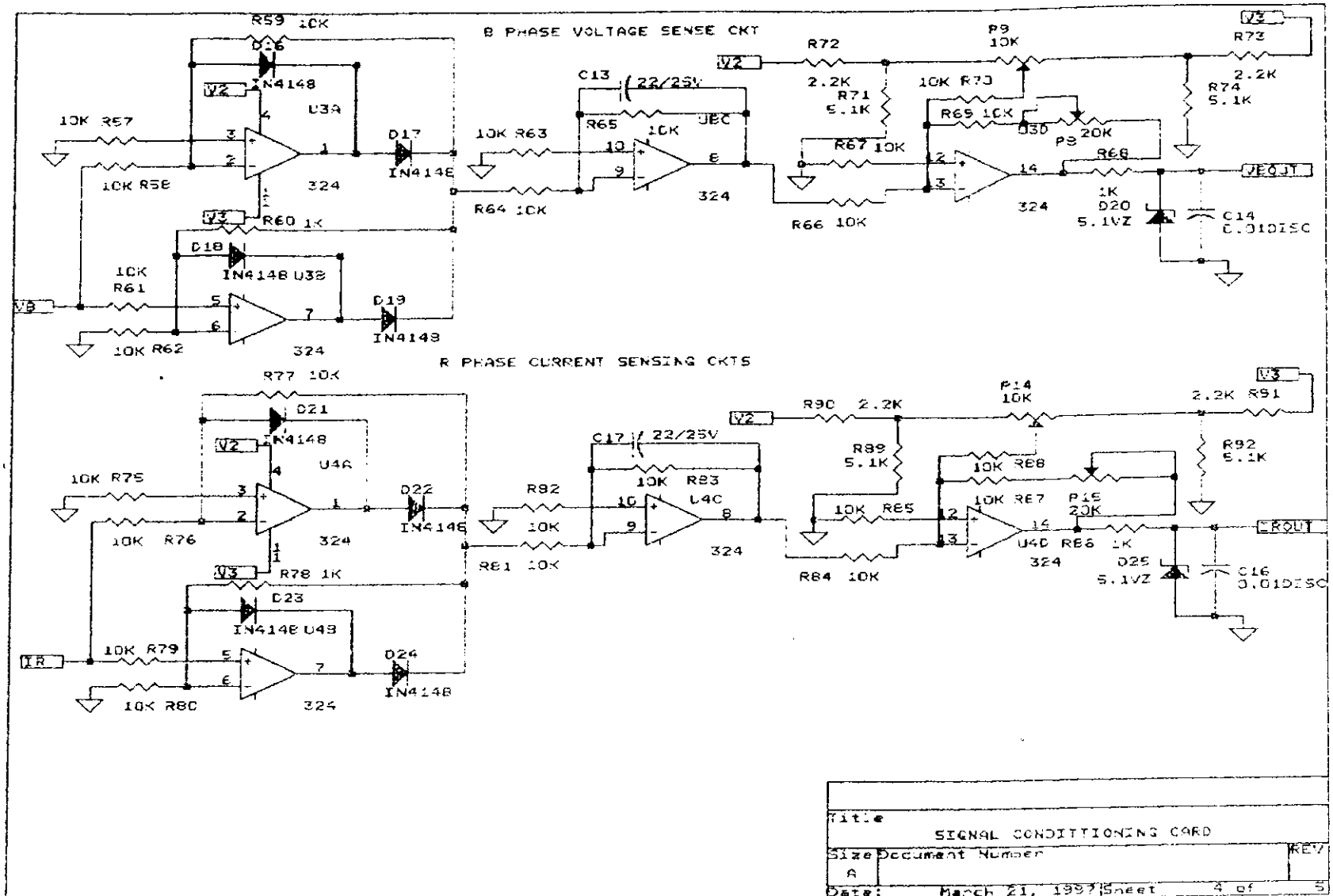
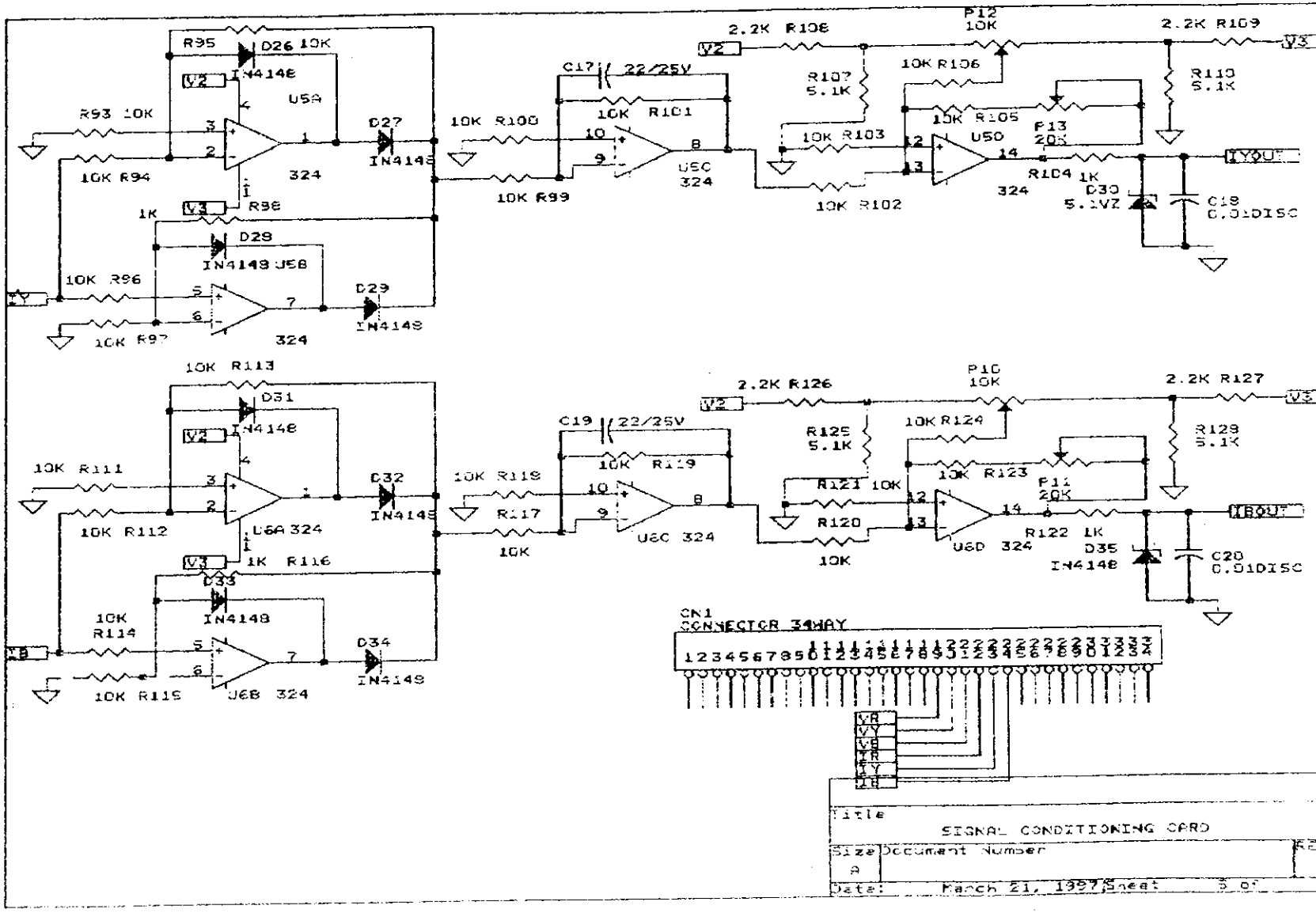


FIG: 7.5

Title: SIGNAL CONDITIONING CARD		
Size: A	Document Number:	REV
Date: March 21, 1997	Sheet 1 of 5	


VOLTAGE SENSING CKTS R24 10K
D6
IN4149
V2
U1A
10K R21
10K R22
D7
IN4148
324
10K R27
R28
10K
C9
22/25V
R29 10K
U1C
324
R37
1K
R34
5.1K
R31 10K
R30
10K
P4
10K
10K R35
10K R33
P5
20K R32
U1D
324
V3
R36
1K
R36
5.1K
VROUT
1K
D10
5.1VZ
C10
0.01DISC
V3
R23 1K
D8
IN4148 U1B
10K
R25
VR
10K R26
324
D9
IN4148
R44 10K
D11
IN4148
V2
U2A
10K R39
10K R40
D12
IN4148
324
V3
R43
1K
D13
IN4148
U2B
R41
10K
VY
10K R42
324
D14
IN4148
R45
10K
10K R46
C11
22/25V
R47 10K
U2C
R53
2.2K
R54
5.1K
R49
10K
P6
10K
R52
10K
R55
2.2K
R56
5.1K
R50
10K R48
P7
20K R50
U2D
324
VYOUT
1K
D15
5.1VZ
C12
0.01DISC
4WAY RELAYMATE
CN4
VROUT
VYOUT
CN5
25WAY D TYPE
324
VBOUT
VROUT
VYOUT
FOUT
GND
Title
SIGNAL CONDITTIONING CARD
Size
A
Document Number
Rev
Date: March 21, 1997 Sheet 3 of 5


B PHASE VOLTAGE SENSE CKT
R PHASE CURRENT SENSING CKTS
R59 10K
D16
IN4148
V2
U3A
10K R57
10K R58
324
D17
IN4148
R60 1K
V3
D18
IN4148 U3B
10K R61
10K R62
V3
324
D19
IN4148
C13 22/25V
R65 10K
U3C
10K R63
R64 10K
324
R72 2.2K
R71 5.1K
R67 10K
R66 10K
P9 10K
10K R70
R69 10K
D30
P8 20K
R68 1K
D20 5.1VZ
C14 0.01DISC
VEOUT
R73 2.2K
R74 5.1K
R77 10K
D21
IN4148
V2
U4A
10K R75
10K R76
324
D22
IN4148
R78 1K
V3
D23
IN4148 U4B
IR
10K R79
10K R80
324
D24
IN4148
C17 22/25V
R82 10K
U4C
R81 10K
324
R90 2.2K
R89 5.1K
R84 10K
P14 10K
10K R88
10K R87
10K R85
P15 20K
U4D R86 1K
324
D25 5.1VZ
C16 0.01DISC
IROUT
2.2K R91
R92 5.1K
Title
SIGNAL CONDITTIONING CARD
Size A
Document Number
REV
Date: March 21, 1997
Sheet 4 of 5


R95
D26 10K
IN4148
V2
U5A
R93 10K
D27
IN4148
10K R94
324
V3
R96
1K
D28
IN4148 U5B
10K R98
D29
IN4148
10K R97
324
10K R113
D31
IN4148
10K R111
D32
IN4148
U6A 324
10K R112
V3
1K R116
D33
IN4148
10K R114
D34
IN4148
10K R115
U6B 324
C17 22/25V
10K R101
10K R100
10K R99
U6C 324
2.2K R106
P12 10K
2.2K R109
10K R106
R107 5.1K
R110 5.1K
10K R105
P13 20K
10K R103
U6D 324
R104 1K
D30 5.1VZ
C18 0.01DISC
10K R102
IYOUT
C19 22/25V
10K R119
10K R118
R117 10K
U6C 324
2.2K R126
P10 10K
2.2K R127
10K R124
R125 5.1K
R128 5.1K
10K R123
P11 20K
R121 10K
R120 10K
U6D 324
R122 1K
D35 IN4148
C20 0.01DISC
IVOUT
CN1
CONNECTOR 34WAY
VR
VY
VB
YR
YY
YB
Title
SIGNAL CONDITIONING CARD
Size A
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Date: March 21, 1997
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SOFTWARE DESCRIPTION

8097BH Microcontroller has a powerful instruction set capable of andling various operations.

ddressing Modes :

The 8097BH instruction set makes use of six addressing modes as lescribed below ;

DIRECT - The operand is specified by an 8-bit address field in the nstruction. The operand must be in the Register File or SFR space (location 0000H through 00FH).

IMMEDIATE - The operand itself follows the opcode in the instruction stream immediate data. The immediate data can be either 8-bits or 16-bits as required by the opcode.

INDIRECT - An 8-bit address field in the instruction gives the word address of a word register in the Register File which contains the 16-bit address of the operand. The operand can be anywhere in memory.

INDIRECT WITH AUTO-INCREMENT - Same as Indirect, except that, after the operand is referenced, the word register that contains the operand's address is incremented by 1 if the operand is a byte, or by 2 if the operand is a word.

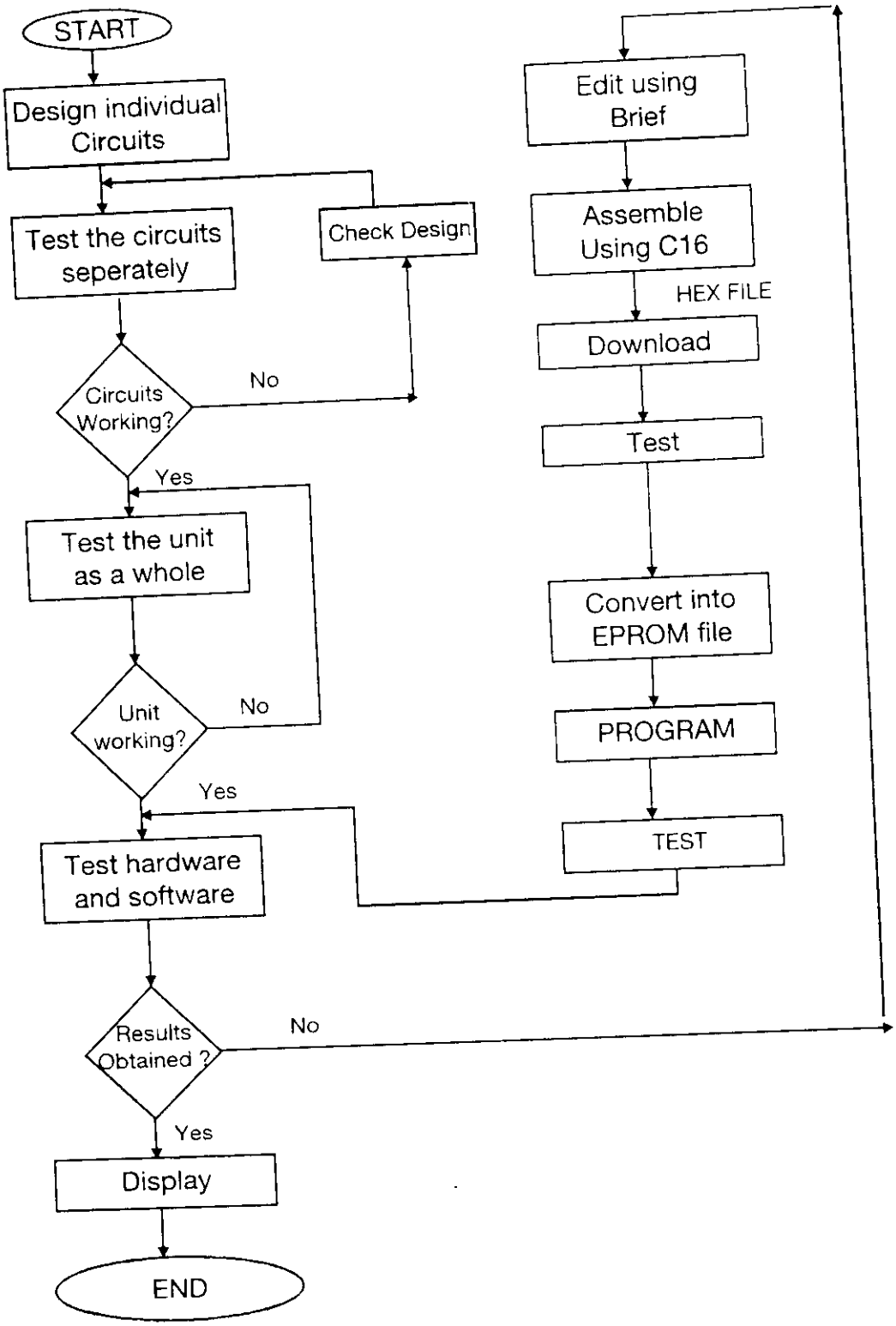
INDEXED (LONG AND SHORT) - The instruction contains an 8-bit address field and either an 8-bit or a 16-bit displacement field. The 8-bit address field gives the word address of a word register in the Register File which contains a 16-bit base address. The 8 or 16-bit displacement field

ontains a signed displacement that will be added to the base address to roduce the address of the operand. The operand can be anywhere in nemory.

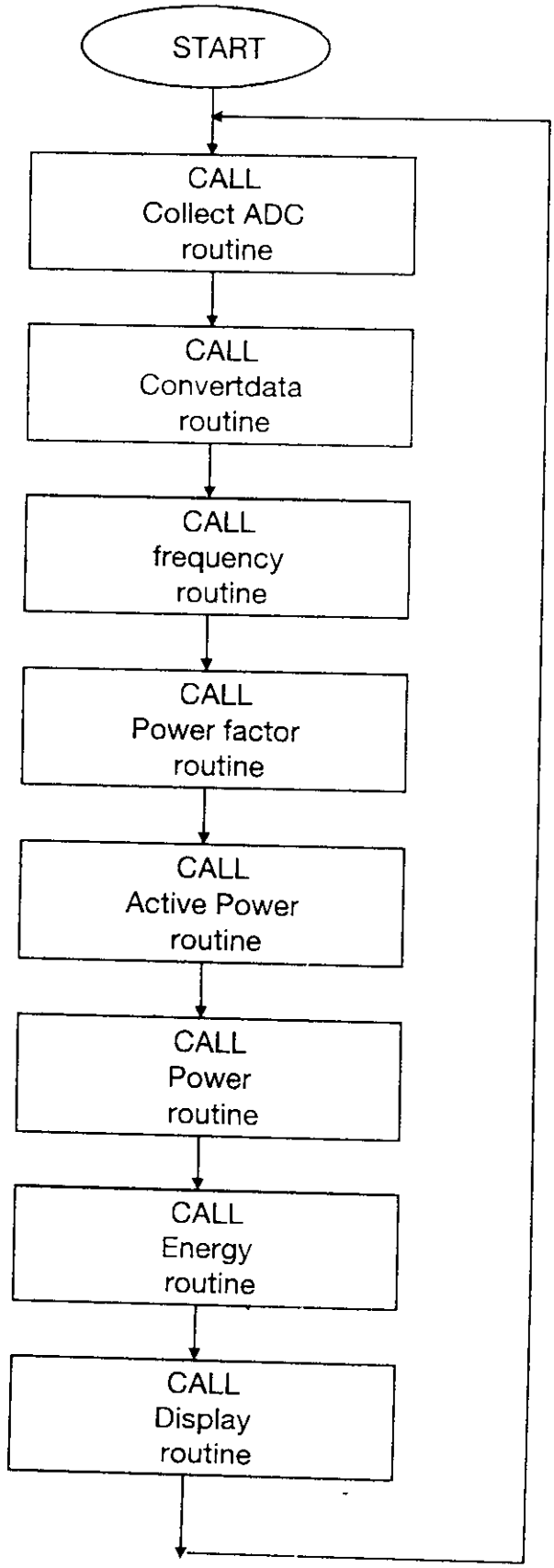
The 8097BH contains a zero register at word address 0000H (and which contains 0000H). This register is available for performing comparisons and or use as a base register in indexed addressing. This effectively provides direct addressing to all 64K of memory.

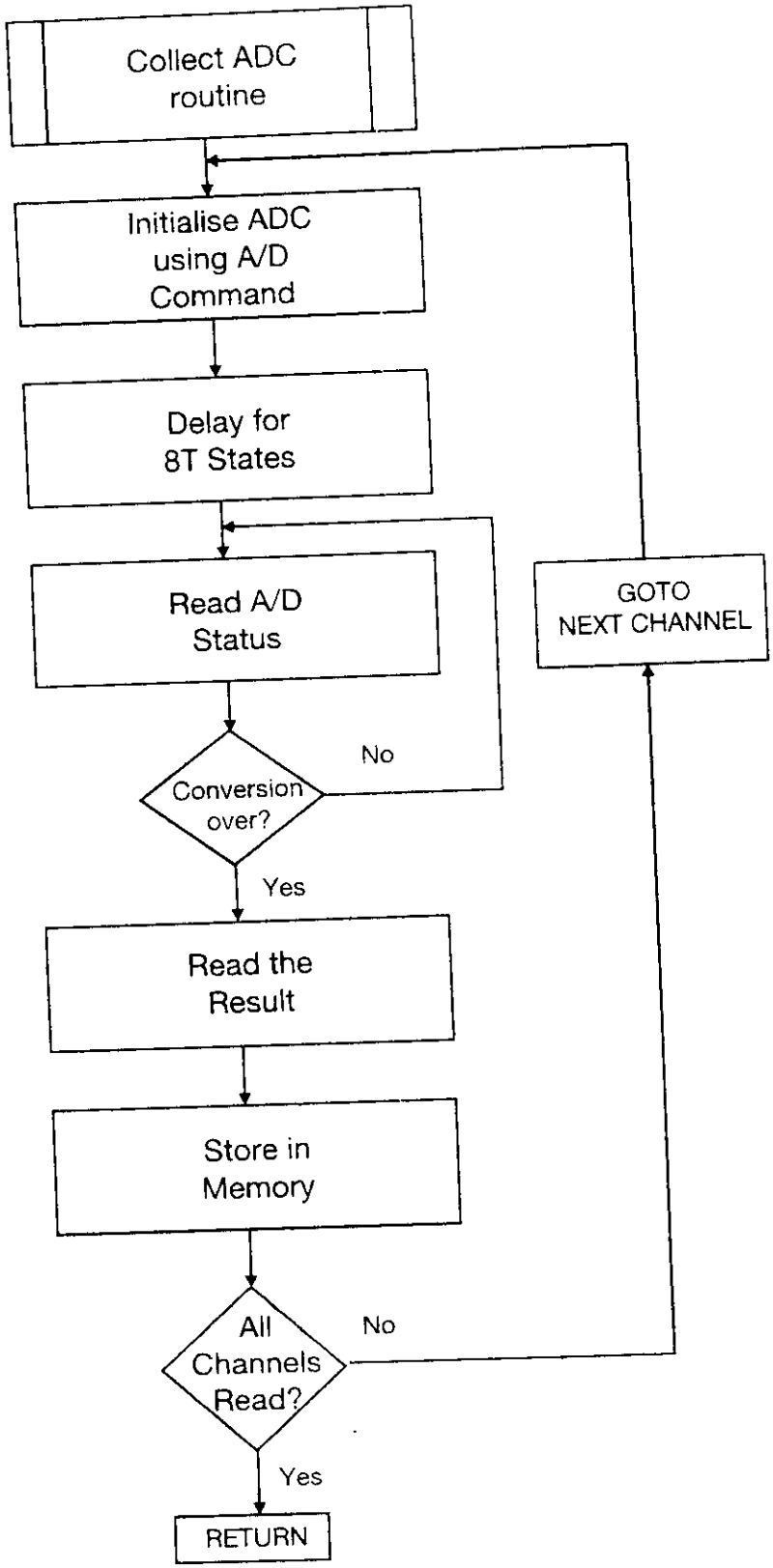
In the 8097BH the Stack Pointer is at word address 0018H in the Register File. If the 8-bit address field contains 18H, the Stack Pointer becomes the base register. This allows direct accessing of variables in the stack.

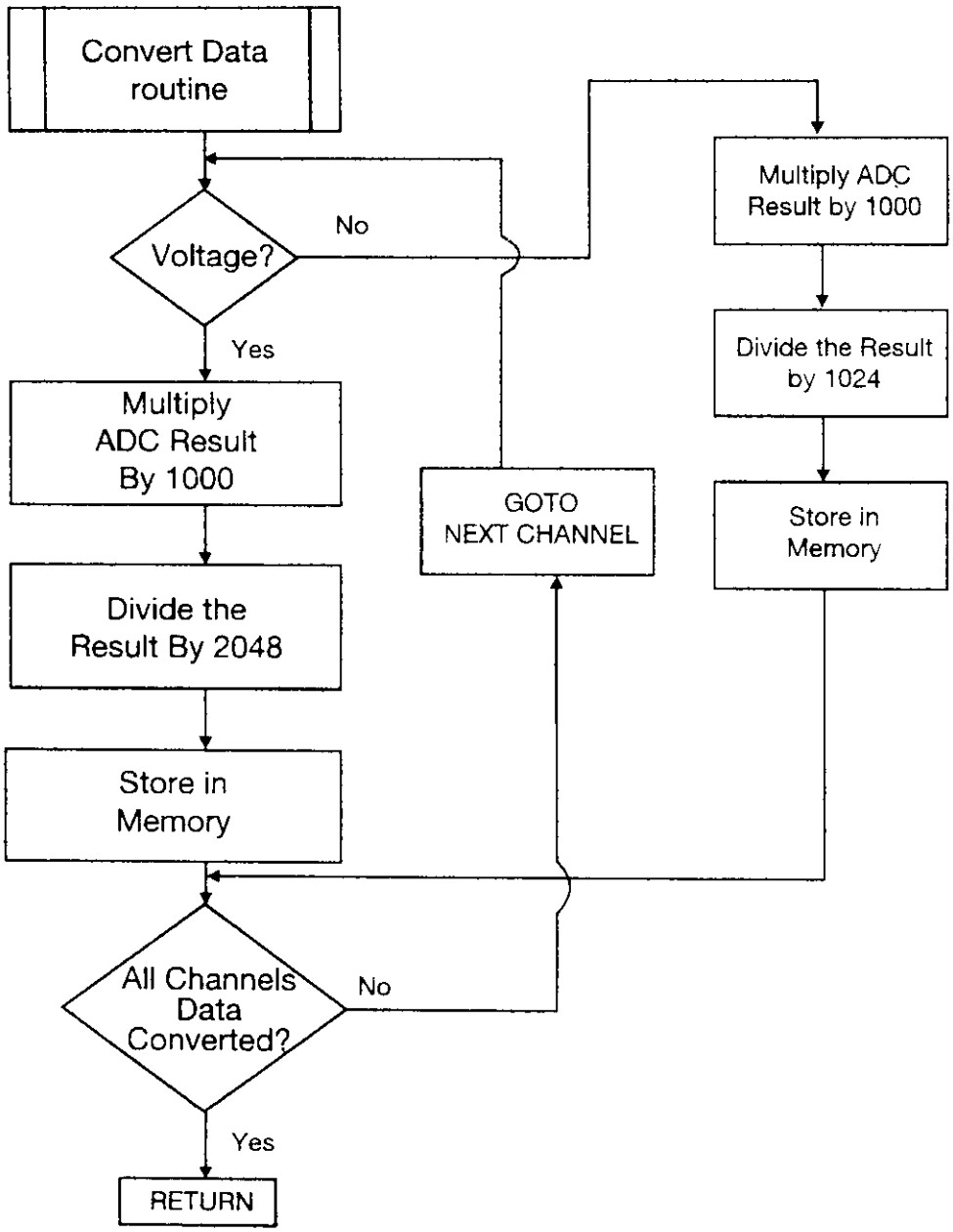
STEM FLOWCHART

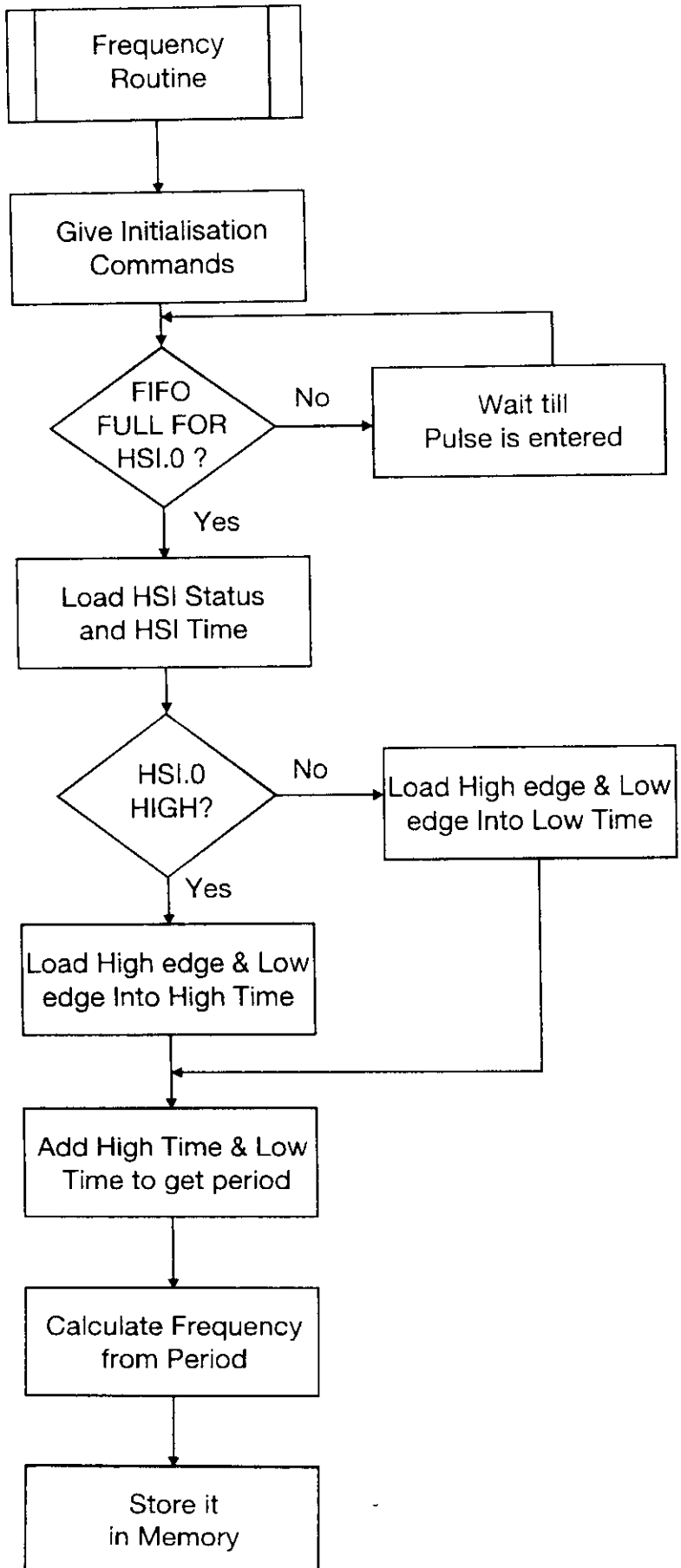


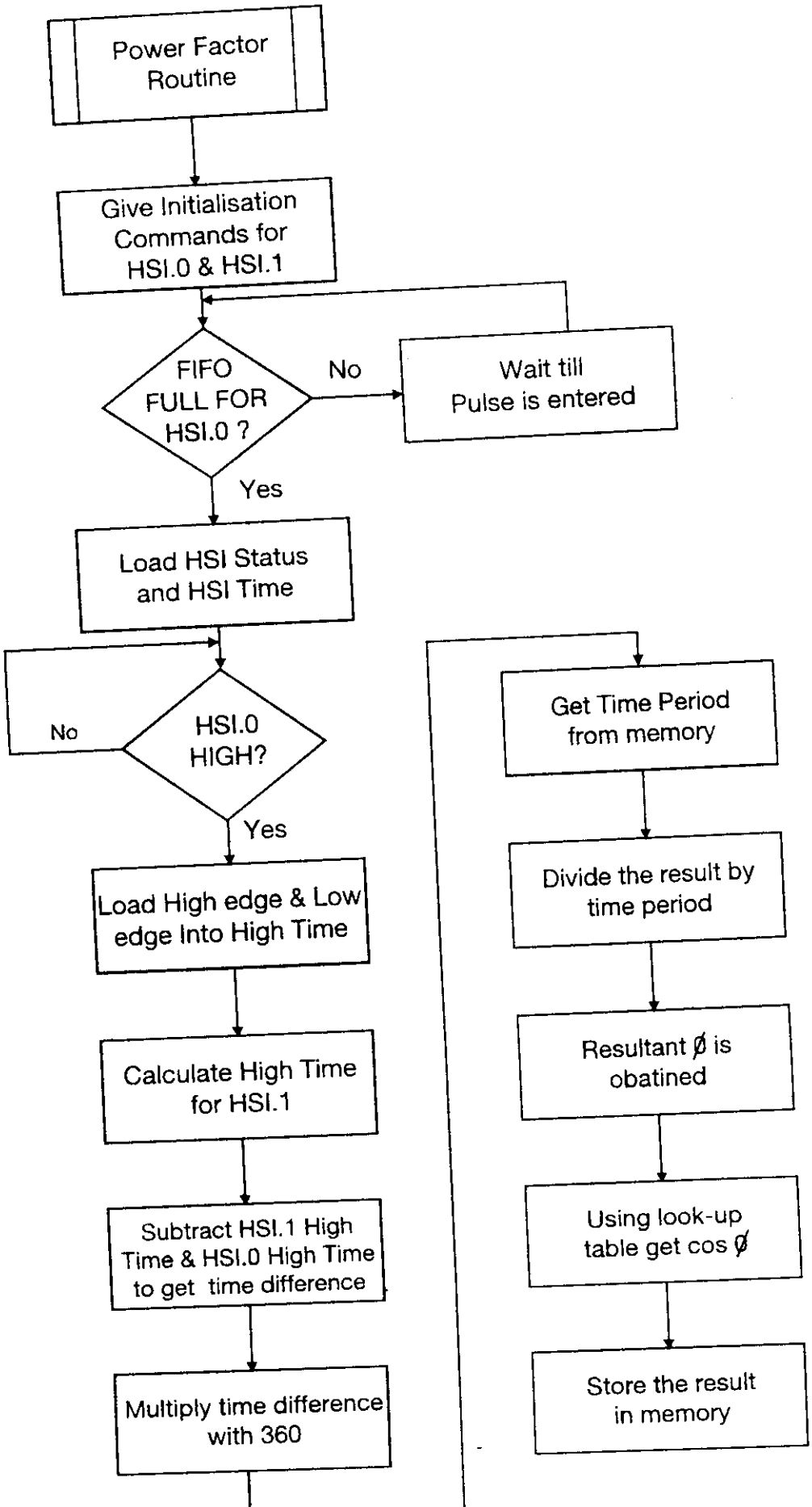
OFTWARE COMPUTATION

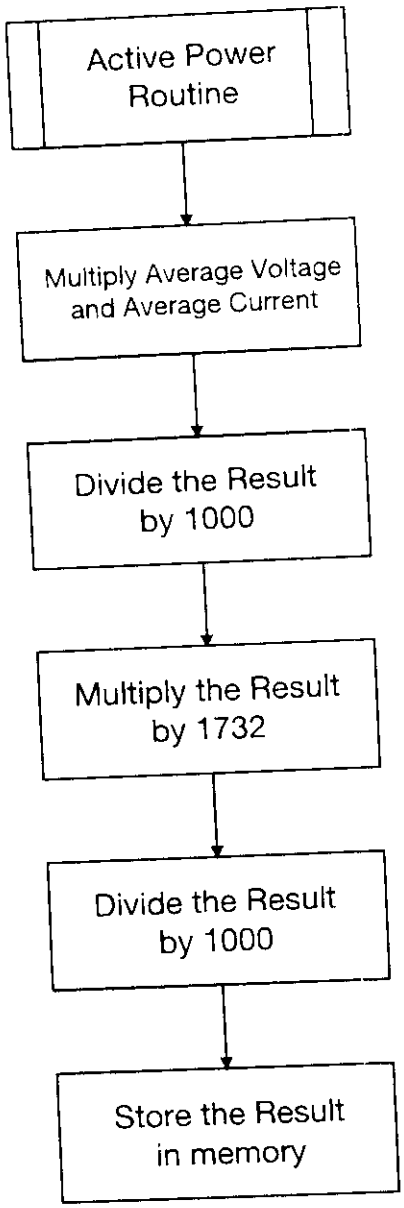


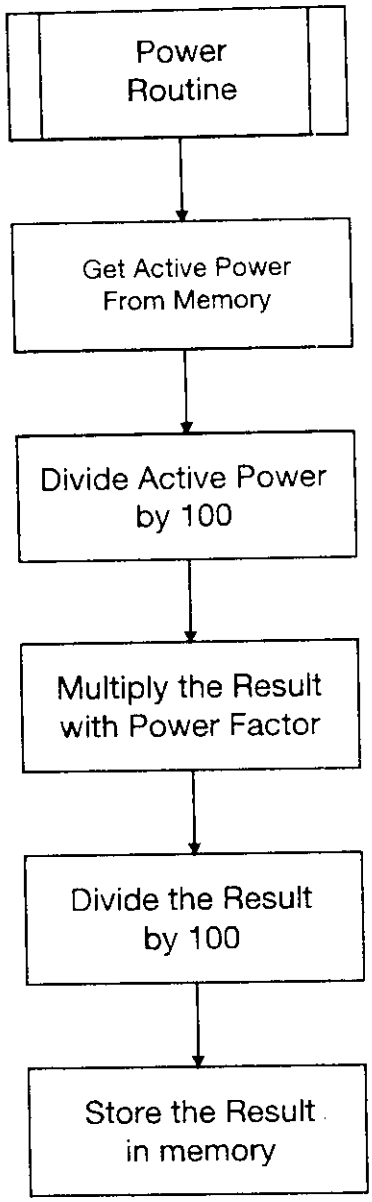

Collect ADC routine
Initialise ADC using A/D Command
Delay for 8T States
Read A/D Status
Conversion over?
No
Yes
Read the Result
Store in Memory
All Channels Read?
No
Yes
RETURN
GOTO NEXT CHANNEL

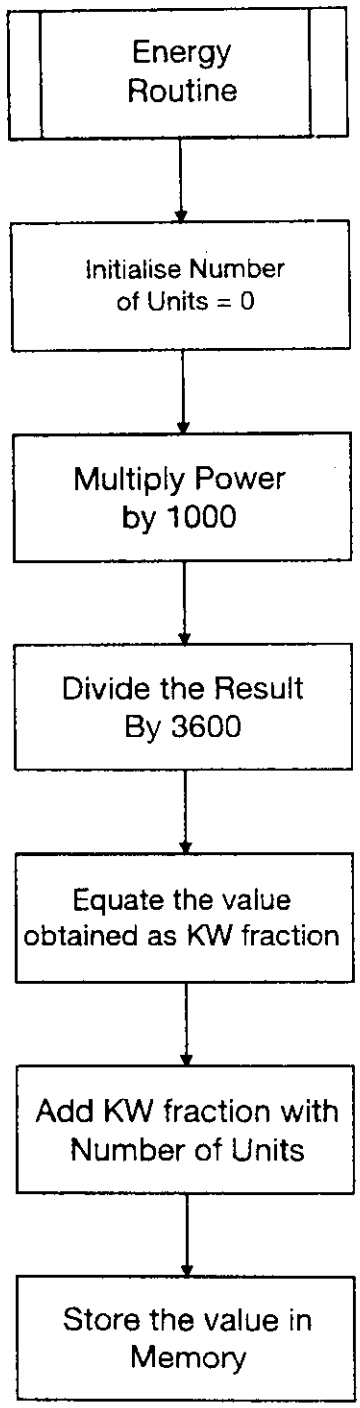

Convert Data routine
Voltage?
No
Yes
Multiply ADC Result By 1000
Divide the Result By 2048
Store in Memory
GOTO NEXT CHANNEL
Multiply ADC Result by 1000
Divide the Result by 1024
Store in Memory
All Channels Data Converted?
No
Yes
RETURN

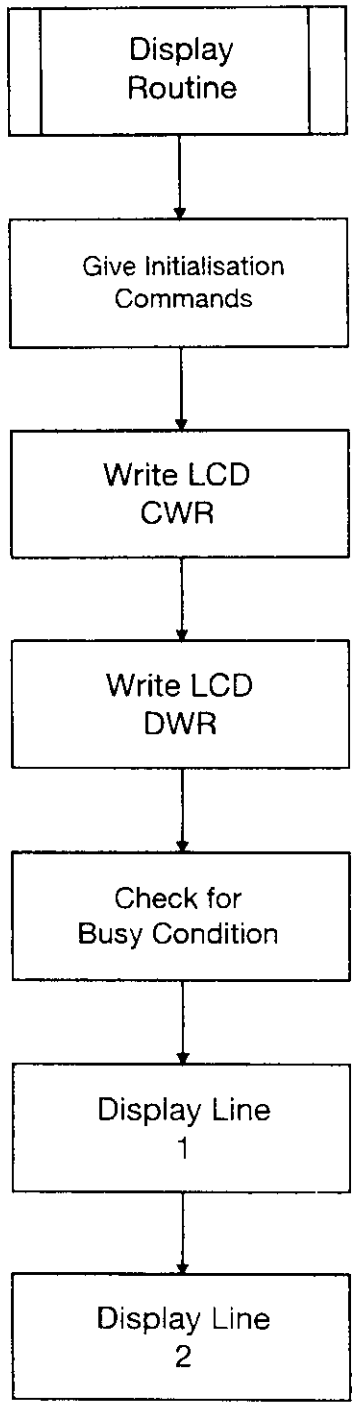

Frequency Routine
Give Initialisation Commands
FIFO FULL FOR HSI.0 ?
No
Wait till Pulse is entered
Yes
Load HSI Status and HSI Time
HSI.0 HIGH?
No
Load High edge & Low edge Into Low Time
Yes
Load High edge & Low edge Into High Time
Add High Time & Low Time to get period
Calculate Frequency from Period
Store it in Memory


Power Factor Routine
Give Initialisation Commands for HSI.0 & HSI.1
FIFO FULL FOR HSI.0 ?
No
Wait till Pulse is entered
Yes
Load HSI Status and HSI Time
No
HSI.0 HIGH?
Yes
Load High edge & Low edge Into High Time
Calculate High Time for HSI.1
Subtract HSI.1 High Time & HSI.0 High Time to get time difference
Multiply time difference with 360
Get Time Period from memory
Divide the result by time period
Resultant ∅ is obatined
Using look-up table get cos ∅
Store the result in memory


Active Power Routine
Multiply Average Voltage and Average Current
Divide the Result by 1000
Multiply the Result by 1732
Divide the Result by 1000
Store the Result in memory


Power Routine
Get Active Power From Memory
Divide Active Power by 100
Multiply the Result with Power Factor
Divide the Result by 100
Store the Result in memory


Energy Routine
Initialise Number of Units = 0
Multiply Power by 1000
Divide the Result By 3600
Equate the value obtained as KW fraction
Add KW fraction with Number of Units
Store the value in Memory


Display Routine
Give Initialisation Commands
Write LCD CWR
Write LCD DWR
Check for Busy Condition
Display Line 1
Display Line 2

```
;                       TITL   " POWER MONITOR "
                        INCL    "C8096T.H"
;
RAM:            EQU     4000H
EPROM:          EQU     2080H
RAMBUFF:        EQU     5600H
BUFF:           EQU     20H
STACK:          EQU     5D00H    ;0FFH
BAUD_HIGH:      EQU     80H
BAUD_LOW:       EQU     13H   ; 26H
EOS:            EQU     04
EOc:            EQU     04
P1:             EQU    PORT1
MAXPAGE:         EQU     02
MAXEDGECNT:      EQU     8
FRQCNT1:         EQU     4B40H      ; 2D00H    ;
FRQCNT2:         EQU      4CH       ; 131H     ;
;
;PORT ALLOCATION
;                                   ORG   BUFF
;
        TEMP:           DFS     04
        XTEMP:          DFS     04
        AX:             DFS     02
        AL:             EQU     AX
        AH:             EQU     AX+1
        BX:             DFS     02
        BL:             EQU     BX
        BH:             EQU     BX+1
        IX:             DFS     02              ; INDEX
        CX:             EQU     IX
        CL:             EQU     CX
        CH:             EQU     CX+1
        I:              DFS     1
        TX:             EQU     I
        D:              EQU     I
        I_1:            EQU     I+1
        PP              DFS
```

```
EL:             EQU         EX
EH:             EQU         EX+1
FX:             DFS         02
FL:             EQU         FX
FH:             EQU         FX+1
GX:             DFS         02
GL:             EQU         GX
GH:             EQU         GX+1
;------------------------------------------- POINTERS -------------------------------
TX_PTR:         DFS         02
QIN_RXR:        DFS         02          ; POINTER FOR Q_ IN RXR
QOUT_RXR:       DFS         02          ;
QIN_TXR:        DFS         02          ; POINTER FOR Q_IN TRANSMITTER
QOUT_TXR:       DFS         02          ;
QIN_ADC:        DFS         02          ; POINTER FOR Q_ IN ADC
;------------------------------------------------------------------------------------
ADCDATA:        DFS         04
NOC:            DFS         02
AD_NUM:         DFS         01
ADNUM:          EQU         AD_NUM
CHANNEL:        DFS         01      ;ADC CHANNEL
CHAN:           DFS         02      ;ADC CHANNEL
TMP:            DFS         02
ADTMP:          DFS         02
HSO_PER:        DFS         02
LAST_LOAD:      DFS         02
COSI:           DFS         02
DEG:            DFS         02
;------------------------------------------------------------------------------------
PROGBUFF:       DFS         01
ADNUM_COPY:     DFS         01
CONCNT:         DFS         01
;------------------------------------------------------------------------------------
QSER_STATUS:    DFS         01
QADC_STATUS:    DFS         01
TXR:            DFS         01                  ;TRANSMITTER REGISTER
RXR:            DFS         01                  ;RECEIVER    [illegible]
[illegible]:    DFS         01
;------------------------------------------------------------------------------------
SPSTAT_COPY:    DFS         01
SPTEMP:         DFS         01
RCV_FLAG:       DFS         01
;------------------------------------------------------------------------------------
OLD_STAT:       DFS         0[illegible]
AMP_TIME:       DFS         01
[illegible]:    DFS         01
[illegible]:    EQU         AMP_[illegible]
[illegible]:    DFS         [illegible]
[illegible]:    DFS         01
;
```

```
SER_FLAG:       EQU     RCV_FLAG
HIGH_TIME:      DFS     02
LOW_TIME:       DFS     02
SUM1:           DFS     04
SUM0:       EQU
PERIOD:         DFS     02
HI_EDGE:        DFS     02
LO_EDGE:        DFS     02
PULSE:          DFS     02
FREQ:           DFS     02
FREQDEC:        DFS     02
VOLT:           DFS     02
AMP:            DFS     02
ANGLE:          DFS     02
PF:             DFS     02
SIN:            DFS     02
PFDEC:          DFS     02
ADC_BUFF:       DFS     02
AVG_VOLT:       DFS     02
AVG_CURR:       DFS     02
KVADEC:             DFS     02
KVARDEC:                    DFS     02
KWDEC:              DFS     02
UNITSDEC:           DFS     02
KVA:            DFS     04
KVAR:           DFS     04
KW:             DFS     04
KW_FRAC:                DFS     04
UNITS:                  DFS     04
VOLT_DEC:               DFS     02
VOLT_UNIT:              DFS     02
VOLT_:                  DFS     02
AMP_DEC:                DFS     02
AMP_UNIT:               DFS     02
```

```
VOLT_R:         DFS     02
VOLT_Y:         DFS     02
VOLT_B:         DFS     02
AMP_R:          DFS     02
AMP_Y:          DFS     02
AMP_B:          DFS     02
AVEVOLT:        DFS     04
AVEAMP:         DFS     04
FRSTE1:         DFS     02
FRSTE2:         DFS     02
INTCNT:         DFS     02
EDGECNT:        DFS     02
EDGECNT1:       DFS     02
;---------------------------------------------------------------
PREVKEY:        DFS     01
STAT:           DFS     01
NOPULSECNT:       DFS       01
UNITCNT:          DFS       02
;---------------------------------------------------------------
                                ORG   RAMBUFF
;---------------------------------------------------------------
Q_RXR:          DFS     08
Q_TXR:          DFS     08
QRXR:           DFS     08
QTXR:           DFS     08
CON_VAR_DIV:    DFS     02
;---------------------------------------------------------------
QADC:           EQU     *
ADCQUE:         DFS     50      ;    DATA STORAGE MAXIMUM
RECORDDATA:     DFS     20
ADTEMP:         DFS     02
RAM:            DFS     02      ;    TEMP REG
RECON:          DFS     01
FAST:           DFS     01
XX:             DFS     02
SETVALUES:      DFS     10
COMM:           DFS     01      ;    TEMP REG
;---------------------------------------------------------------
```

```
;------------------------------------------------------------------------
BEGIN:          EQU       $
;------------------------------------------------------------------------
                                        LD      SP,#STACK
                                        CLRB    SER_FLAG
                                        LDB     PORT1,#[illegible]
;                                       LCALL   CNSC1
                                        LD      TX_PTR,#[illegible]
                                        LDB     SPSTAT_COPY,#[illegible]
                                        ORB     SER_FLAG,#[illegible]
                                        LDB     SBUF,#20H
                                        LCALL   OUTSTRG
                                        ANDB    SER_FLAG,#0FEH
                                        LJMP      ADCEXEC1
CMND:                                   LCALL   [illegible]
```

```
;edREXEC:    EQU     *
;-------------------------------------------------------------------------------
                        LDB     SBUF,#0
                        LCALL   CLRSCREEN
                        LD      TX_PTR,#LCDSTRING   ;
                        LDB     SBUF,#0
                        LCALL   OUTSTRG
                        LDB     PAGE_NO,#0
                        LCALL   initLCD

DISD:                   addb    noc,page_no,page_no
                        extb    noc
                        ld      ix,pagetbl[noc]
                        LD      TX_PTR,ix
                        LCALL   DISP_LINE1
                        LCALL   OUTSTRG
                        LCALL   OUTcrlf
                        addb    noc,page_no,page_no
                        addb    noc,#2
                        extb    noc
                        ld      ix,pagetbl[noc]
                        LD      TX_PTR,ix
                        LCALL   DISP_LINE2
                        LDB     SBUF,#0
                        LCALL   OUTSTRG
                        LCALL   OUTcrlf

CMD:                    LCALL   INSCI
                        CMPB    RXR,#00
                        JE      CMD
                        CMPB    RXR,#03
                        JE      BEGIN1
                        INCB    PAGE_NO
                        CMPB    PAGE_NO,#MAXPAGE
                        JLT     DISD
                        LDB     PAGE_NO,#0
                        SJMP    DISD
begin1:                 jmp     begin
;-------------------------------------------------------------------------------
```

```
tbl:            dwl     page1_1
                dwl     page1_2
                dwl     page2_1
                dwl     page2_2
                dwl     page3_1
                dwl     page3_2
-------------------------------------------------------------------------------
1_1: DFB   "Vryb:400  400  400"
     DFB   EOS
1_2: DFB   "Iryb:100  100  100"
     DFB   EOS
-------------------------------------------------------------------------------
2_1: DFB   "Hz:       kva:      "
     DFB   EOS
2_2: DFB   "pf:.      kw :      "
     DFB   EOS
-------------------------------------------------------------------------------
3_1: DFB   "kvar :              "
     DFB   EOS
3_2: DFB   "units:              "
     DFB   EOS
-------------------------------------------------------------------------------

-------------------------------------------------------------------------------
XEC:    EQU     *
-------------------------------------------------------------------------------
AD A CHANNEL
-------------------------------------------------------------------------------
                        LDB     SBUF,#0
                        LCALL   CLRSCREEN
                        CLRB    AD_NUM
-------------------------------------------------------------------------------
                        LD      TX_PTR,#ADCSTRING   ;
                        LDB     SPSTAT_COPY,#00100000B
                        ORB     SER_FLAG,#01H
                        LCALL   OUTSTRG
                        LCALL   INITBUFF
                        LCALL   INITLCD
                        LCALL   INITINT
-------------------------------------------------------------------------------
                        LCALL   COLLECTADC          ; READS ALL 8 CHANNELS AND LAST
                        LCALL   CONVERT_DATA        ; CONVERTS &SCALES ALL 8 CHANNELS
                        LCALL   CALCDATA            ; CALCULATE KVA, KW AND PF
                        LCALL   CUTFREQ             ; CALCULATE FREQ
                        LCALL   GAUGE               ; CALCULATE GAUGE
                        LCALL   LOADDATA_LCD        ; DISPLAY DATA ON LCD
                        LCALL   LOADDATA_SCI
                        LCALL   KEYSERVE
                        LD      DX,#4000
                        LCALL   DLY
                        JMP     START
```

```
S:                          LDB     PREVKEY,#0
                            INCB    PAGE_NO
                            CMPB    PAGE_NO,#MAXPAGE
                            JLT     OKD
                            LDB     PAGE_NO,#0
D:                          RET
-------------------------------------------------------------------------------

TBUFF:    EQU       *
-------------------------------------------------------------------------------

                          LD  UNITS,#0
                          LD  UNITSDEC,#0
                          LD  KW_FRAC,#0
                          LD  KW_FRAC+2,#0
                          LDB  PAGE_NO,#0
                          LDB  PREVKEY,#0
                          LD   INTCNT,#0
                          LD  EDGECNT,#0
                          LD   EDGECNT1,#0
                          LD   SUM0,#0
                          LD   PULSE,#0
                          LD   SUM0+2,#0
                          LD   FREQ,#0
                          LD   FREQDEC,#0
                          LD   PF,#9999
                          LD   PFDEC,#9999H
                          LD   UNITCNT,#50
                          RET
-------------------------------------------------------------------------------

ITINT:    EQU       *
-------------------------------------------------------------------------------

                          LDB   MSI_MODE,#00000001B
                          LDB   IOC0,#00000001B
                          LDB   IOC1,#00100000B
                          LDB   INT_MASK,#00010000B       ; ONLY HI SPEED O/P INTR,AD
                          LDB   INT_PENDING,#00010000B      ; ONLY HI SPEED O/P INTR
                          LDB   INT_MASK,#00000100B       ; ONLY HI SPEED O/P INTR,AD
                          LDB   INT_PENDING,#00000100B      ; ONLY HI SPEED O/P INTR
                          EI
                          RET
-------------------------------------------------------------------------------

LLSCTADC.     EQU     *
-------------------------------------------------------------------------------

EAD ALL 8 CHANNELS AND STORE IN MEMORY
-------------------------------------------------------------------------------

                            LDB     CHAN,#0C0
                            LDB     CHANNEL,CHAN
                            CALL    AVDAC                   ;GET A/D
                            LDB     NOC,CHAN
                            CMPB    NOC,
                            JGT     NOC,$
                            ADD     A,#0
                            INC     A
                            CMPB    CHAN,#
                            JLT     A,
                            RET
```

```
DATA:   EQU     *
        LD      AVEVOLT,#0              ;INITIALISE AVEVOLT
        LD      AVEAMP,#0               ;INITIALISE AVEAMP

        LD      AX,QADC+14[0]           ;DATA FROM CH4
        MUL     AX,#1000
        DIVU    AX,#2048
        ST      AX,VOLT_R

        LD      AX,QADC+12[0]           ;DATA FROM CH3
        MUL     AX,#1000
        DIVU    AX,#2048
        ST      AX,VOLT_Y

        LD      AX,QADC+10[0]           ;DATA FROM CH2
        MUL     AX,#1000
        DIVU    AX,#2048
        ST      AX,VOLT_B

        LD      AX,QADC[0]              ;DATA FROM CH0
        MUL     AX,#1000
        DIVU    AX,#1024
        ST      AX,AMP_R


        LD      AX,QADC+2[0]            ;DATA FROM CH1
        MUL     AX,#1000
        DIVU    AX,#1024
        ST      AX,AMP_Y

        LD      AX,QADC+4[0]            ;DATA FROM CH4
        MUL     AX,#1000
        DIVU    AX,#1024
        ST      AX,AMP_B

        ADD     AVEVOLT,VOLT_R
        ADD     AVEVOLT,VOLT_Y
        ADD     AVEVOLT,VOLT_B
        EXT     AVEVOLT
        DIVU    AVEVOLT,#03             ;AVERAGE VOLTAGE

        ADD     AVEAMP,AMP_R,AMP_Y
        ADD     AVEAMP,AMP_B
        EXT     AVEAMP
        DIVU    AVEAMP,#03              ;AVERAGE CURRENT

    LD      AX,VOLT_R
    LCALL   BCDCON
    LD      VOLT_RDEC,BX
    LD      AX,VOLT_Y
    LCALL   BCDCON
    LD      VOLT_YDEC,BX
    LD      AX,VOLT_B
    LCALL   BCDCON
    LD      VOLT_BDEC,BX

    LD      AX,AMP_R
    LCALL   BCDCON
    LD      AMP_RDEC,BX
    LD      AX,AMP_Y
```