Microcontroller Based Testing Equipment (Interface Card for Yarn Clearer)

PROJECT REPORT

Submitted by

G. BALAKARUPPAIAH

P.M. MURALIDARAN

R. SATHIA PRIYA

VATSALA V. SHASTRI

Guided by

Mrs. B. DEVI, B.E.,

Sponsored by

PREMIER POLYTRONICS LIMITED, Coimbatore

IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE AWARD OF THE DEGREE OF

BACHELOR OF ENGINEERING IN ELECTRONICS & COMMUNICATION ENGINEERING

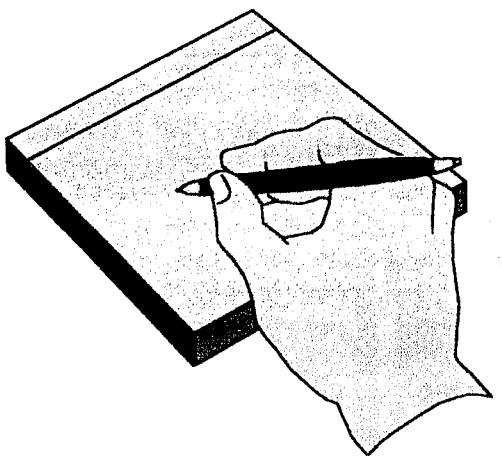
OF BHARATHIAR UNIVERSITY, COIMBATORE.

1997 - 98

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Kumaraguru College of Technology

COIMBATORE - 641 006.



CERTIFICATE

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Kumaraguru College of Technology

COIMBATORE – 641 006

CERTIFICATE

This is to certify that the Project entitled

MICROCONTROLLER BASED TESTING EQUIPMENT
(INTERFACE CARD FOR YARN CLEARER)

has been submitted by

Mr./Miss. . . . . .

In partial fulfilment of the requirements for the award of degree of Bachelor of Engineering in the Electronics & Communication Engineering branch of the Bharathiar University, Coimbatore – 641 046 during the academic year 1997-98.

. . B. D. . . . . .
Guide

. . . . . .
Professor and Head

Certified that the candidate with University Register No. . . . . .
was examined in project work Viva-Voce Examination held on . . . . . .

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Internal Examiner

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External Examiner

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ACKNOWLEDGEMENT

We express our Gratitude's to **Prof.M.Ramasamy, M.E., MISTE.,** Professor and Head of Department of Electronics & Communication Engineering, Kumaraguru College of Technology, Coimbatore for providing the facilities for this project work.

We express our sincere and profound sense of gratitude to **Mrs.B.Devi, B.E.,** Lecturer, Department of Electronics & Communication Engineering, Kumaraguru College of Technology for her invaluable guidance and encouragement to carry out this project work.

We wish to thank **Dr.S.Subramanian, B.E., M.Sc.(Engg), Ph.D.,** Principal, Kumaraguru College of Technology, Coimbatore for providing the facilities for this project work.

We express our thanks to **Mr.K.K.Venkataraman,** Vice-President of Premier Polytronics Ltd., for having accepted to sponsor this project.

We express our deepest gratitude to **Mr.B.Shanmugasundaram,** Assistant Manager (R&D) for helping us from the conceptualization to the realisation of the project.

We would be failing in our duty if we don't express our thanks to **Ms.A.Rajeshwari,** Assistant Engineer (R&D), our guide at Premier Polytronics Ltd., for readily providing us all the facilities and patiently answering all our queries and helping us to carry out this project within the stipulated time.

SYNOPSIS

In Textile Industry, micro-controller based devices used to monitor and control many stable yarn processing machines in order to improve product quality and to increase productivity.

The interface card developed by Premier Polytronics Ltd., is one such device designed around the versatile 80C320 micro-controller.

This project report gives details about a testing equipment designed for the above card.

The IC used in this testing equipment is also the same high speed micro controller 80C320. Assembler ASM-51 and PL/M-51 are used for programming both the interface card and the test system. The interface card is tested for any defects, even before it is installed in the system being used, by interfacing it with the test equipment. The software written, automatically checks for the different faults and displays the necessary details. PL/M-51, compiler makes the system user friendly.

This automatic detection proves to be very effective in increasing the overall efficiency of the mill.

CHAPTER 1

INTRODUCTION

Any winding mill consists of yarn clearer which continuously monitor the different parameters, of the thread especially the thickness.

The three main units of yarn clearer are:

1) Measuring Head
2) Evaluation Unit
3) Control Unit.

As the yarn passes through the measuring head, the analog signal corresponding to the thickness variations is sent to the evaluation unit. The evaluation unit monitors the thread signal and evaluates the different categories of faults. The limiting values for the yarn faults are set in the control unit via a keyboard and the 240 x 128 dot matrix display. The control unit comprises of

The main CPU Card

The interface Card

The power supply Card.

It is the Interface Card for which the TEST EQUIPMENT is developed.

1.1 INTERFACE CARD

To realise an effective testing equipment, a thorough study of Interface card is done before the actual design. The circuit diagram of the card is shown in Fig. The various chips and their functions are listed below:

i) DS 80C320: Dallas high speed Micro controller: This controller forms the heart of the board and is responsible for full duplex serial communication between the various evaluation units and controls unit.

ii) 62256 is a 262, 144 bit low power static Random access memory which serves as auxillary data memory device.

iii) 27512 Erasable programmable Read only memory: EPROM chip act as auxillary program memory in the system.

iv) 74 HCT 245 BUFFER HIGH SPEED CMOS LOGIC: It is a high speed octal 3 – state bidirectional transceiver intended for two way asynchronous communication between data buses.

v) 74 HCT 573 LATCH HIGH SPEED CMOS LOGIC: It is a high speed octal transparent latch which possesses low power consumption as well as ability to drive 15 LSTTL devices.

1.2 FUNCTIONS OF INTERFACE CARD:

The main function of the interface card is to interface display, printer to main CPU cards, also it acts as a slave for CPU card.

1.3 THE TESTING EQUIPMENTS:

1. Power supply test.
2. Display interface test
3. PC interface test.

1.4 HARDWARE CONCEPTS:

The testing system should be capable of automatic detection and display of faults. In order to achieve this, the hardware section of the test system comprises of

1. Controller section
2. Interface section
3. Power Supply section.

A block diagram showing different section is given. The controller section is constituted by the high speed micro controller DS-80 C 320 along with the necessary RAM, EPROM, LATCH and BUFFER circuitry.

A 240 x 128 liquid crystal display forms the interface section. The different connectors used for interfacing the various signals are:

32 pin EURO connector to communicate with the test jig.

20 pin RELIMATE connector which gives access to the display

50 Pin FRC connector.

CHAPTER 2

MICROCONTROLLER DS80C320 DETAILS

2.1 DESCIRPTION OF DS 80 C320:

The DS 80 C320 is a fast 80C31 / 80C31 – compatible microcontroller. Wasted clock and memory cycles have been removed using a redesigned processor core. As a result, every 8051 instruction is executed between 1.5 to 3 times faster than the original for the same crystal speed. Typical application will see a speed improvement of 2.5 times using the same code and same crystal. The DS 80 C320 offers a maximum crystal rate of 33 MHz, resulting in apparent high execution speeds.

The DS 80 C320 is pin compatible with all three packages of standard 80 C32 and offers same timers counters, serial ports and input ports. In short, the DS 80 C320 is extremely familiar to 8051 users but provides speed of a 16 bit – processor.

The DS 80 C320 provides several extras in addition to greater speed. These include a second full hardware serial port, seven additional interrupts, programmable watch dog times, power fail interrupt and reset.

The DS 80 C320 also provides dual data pointers (DPTRs) to speed block data memory moves. It can also adjust the speed of off-chip data memory access to between 2 and 9 machine cycles for flexibility in selecting memory and peripherals.

2.2 FEATURES:

80 C320 compatible

- Pin compatible
- Standard 8051 instruction set
- 4, 8 – bit i/o ports
- 3, 6 – bit timer / counter
- 256 bytes scratchpad RAM
- Multiplexed address / data bus
- Addresses 64 KB ROM and 64 KB RAM
- High Speed Architecture
- clocks / machine cycles (8032 = 12)
- Wasted cycles removed
- Runs DC to 33 MHz clock rates
- Single cycle instruction in 121 ns
- Uses less power for equivalent work
- Dual data pointers
- Optional variable length MOVx to access slow

- RAM / Peripherals.

High integration controller includes

- Power – fail reset
- Programmable Watch dog timer
- Early warning power – fail interrupt
- Two full – duplex hardware serial ports
- 13 total interrupts sources with 6 external.
- Available on 40 pin DIP, 44 – pin PLCC and TOPP.

2.3 PIN DESCRIPTION

DS 80 C320 used in the system is a 40 pin DIP package with Vcc = + 5V. Out of the four ports available 3 ports act as i/p ports and one as output port.

PORT 0 : Pins 32 to 39 (Multiplexed Address / data bus)

PORT 1 : Pins 1 to 8

PORT 2 : Pins 21 to 28 (MSB for external Addressing)

PORT 3 : Pins 10 to 17

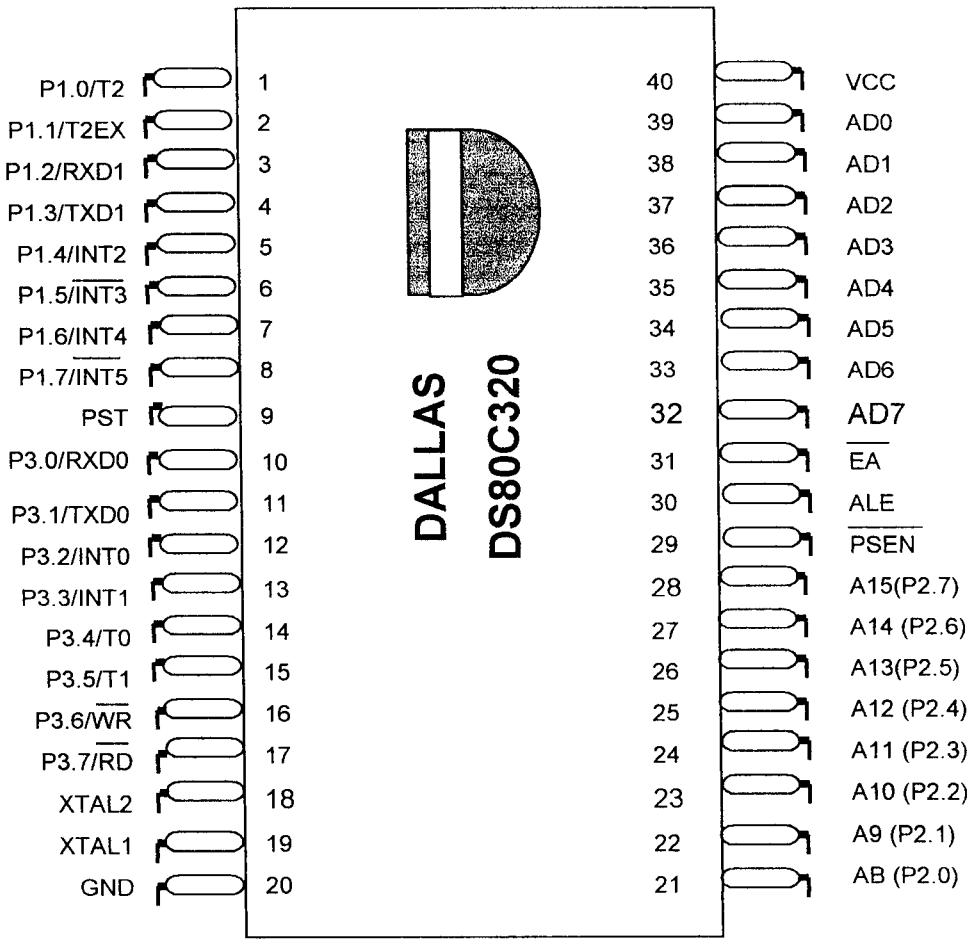


Fig 2.1 40 PIN DIP

All the pins of ports 1 and 3 have alternate functions.

Port pins	Alternate functions
P 3.0	RxD0 Serial port 0 input
P 3.1	TxD0 serial port 0 input
P 3.2.	$\overline{\text{INT0}}$ External interrupt 0
P 3.3	INT1 External interrupt 1
P 3.4	T0 Timer 0 external input
P 3.5	T1 Timer 1 external input
P 3.6	$\overline{\text{WR}}$ External data memory write stroke
P 3.7	RD External data

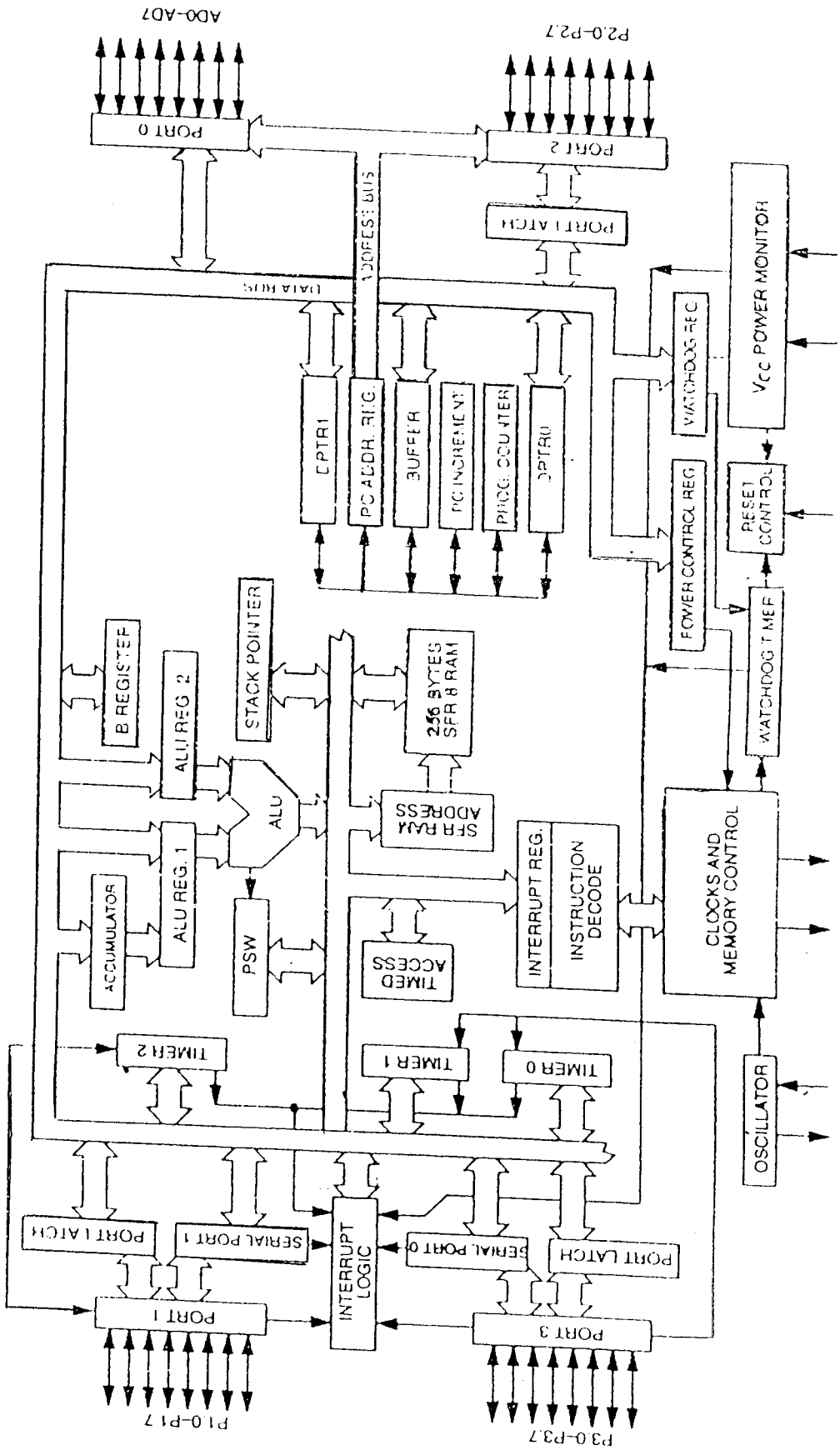
2.4. ARCHITECTURE OF 80 C320:

The section provides a brief description of each architecture feature.

ALU:

The ALU is responsible for math function, comparison and genual decision making in the High Speed micro controller. The ALU is not explicity used by software. It uses two special functions registers as the source and destination. These are the Accumulator and B Register.

DS80C320 BLOCK DIAGRAM Figure 1



Special Function Registers:

All peripherals and operations are not explicit instructions in the high speed micro controller are controlled via SFRS.

Accumulator:

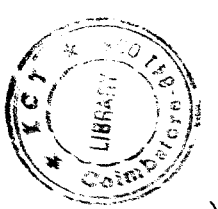
This is the primary register used. It is the source and destination of most math, data movement, decisions and other operations.

B-Register:

This is used as a second 8 bit argument in multiply and divide operations.

Program Status Word:

This holds a selection of bit flags. It includes carry flag. Auxillary carry flag., General purpose flag, Register bank select, overflow flag and parity flag.



Stack Pointer:

This denotes the register location at the top of the stack which is the last used value. The user can place the stack any where in the scratch pad.RAM by setting the stack pointer to that location.

Data Pointer:

Data pointer is used to designate a memory address for the MOVx instruction. When moving data from one memory area to another or from memory to a memory mapped peripheral, a pointer is needed for both source and destination.

I/O Ports:

The standard 80 C320 offers 8 bit i/o ports. 80 C320 chip uses port 0 and port 2 as address and data buses. The other two ports are used for general purpose i/o. Each i/o port is SFR that can be written or read. It has a latch that retains the value which software writes.

Timer / Counters:

Three 16 bit timer / counters are available. Each timer is contained in two SFR location that can be written or read by software.

UARTS:

The two UARTS available are controlled and accessed as SFRs. Each UART has an address that is used to read or write the UART. Each UART is controlled by its own SFR control register.

Scratch Pad RAM:

The 1st 128 bytes of RAM are directly available to software whereas the upper 128 bytes are available through indirect addressing.

Working Register:

The 1st 32 bytes of the RAM area is used as 4 banks of 8 working registers for high speed data movement. In addition to the Accumulator. The working registers are commonly used as a data source or destination. Some can be used as pointer to other RAM locations.

Program Counter:

This is the 16 bit value that designates the next program address to be fetched. On-chip hardware automatically increments the PC value to move to next ROM location.

Interrupts:

There are 13 interrupt sources. Each has an associated interrupt vector, priority and enable. These interrupts can be globally enabled or disabled.

Memory Organisation:

The high speed micro controller uses several distinct memory areas. These are register program memory and data memory. Registers serve to control on-chip peripheral and as RAM. Register are divided into 3 categories.

1. Directly addressed on-chip RAM
2. Indirectly addressed on-chip RAM
3. Special function Registers

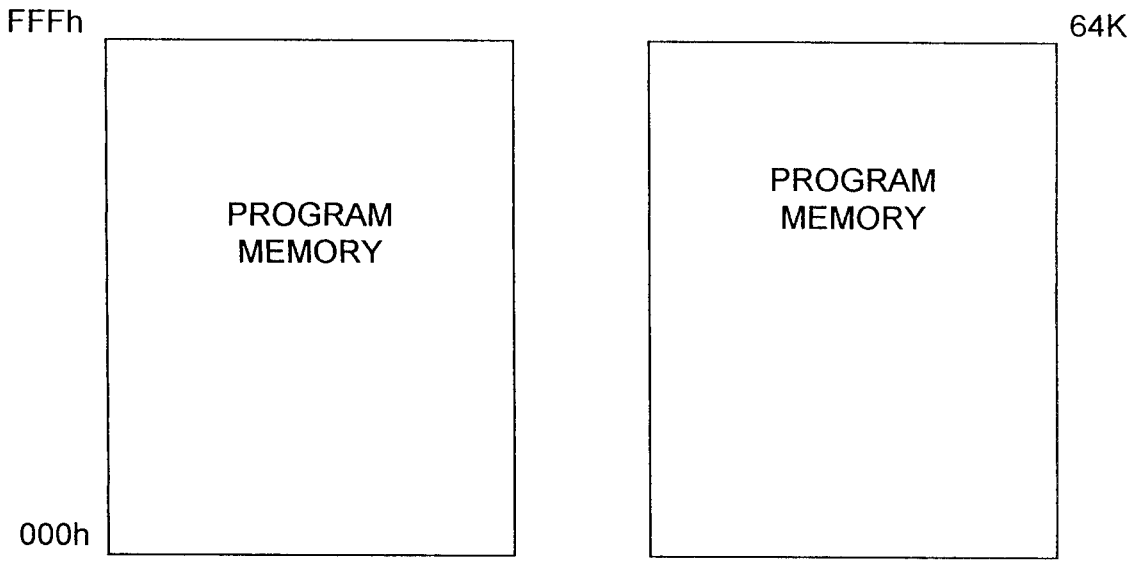
Memory Map:

The high speed micro controller uses a memory addressing scheme that separate program memory (ROM) from data memory (RAM). Each area is 64KB beginning at address 0000h and ending at FFFFh. The program and data segments can overlap since they are accessed in different ways. Program memory is fetched by the micro controller automatically.

Register Map:

The register map is entirely separate from the program memory and data memory areas mentioned above. A separate class of instruction is used to access the registers. There are 256 potential register location values. In practice, the high speed micro controller has 256 bytes of scratch pad RAM and upto 128 special function registers (SFRs). The upper 128 bytes of scratch pad RAM locations can only be accessed indirectly. A direct reference to one of the upper 128 locations is an SFR access. Direct RAM is reached at location 00h to 7Fh. SFRs are accessed directly between 80h and FFh. Memory and register maps are shown in figure 2.3.

MEMORY MAP



REGISTER MAP

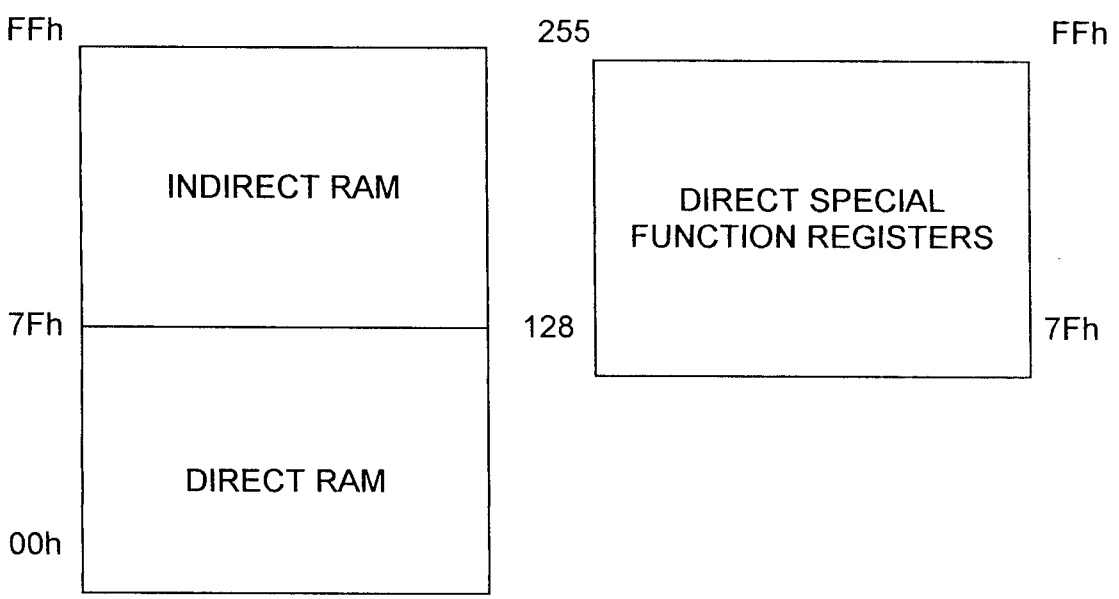


Fig. 2.3

Bit Addressable Location:

`In addition to direct register access some individual bits are also accessible. In scratch pad RAM area, register 20h to 2Fh are bit addressable. A bit access is distinguished from a functional register access by the type of instruction. In the SFR area any location ending in a 0 or 8 is bit addressable.

Programmable Timer / Counter:

This high speed micro controller incorporates three 16 bit programmable timers. In most modes these timers can be used either as counters of external events or timers. When functioning as timers they effectively count oscillator cycle the time base for the timer function in the main oscillator clock is divided by either 4 or 12.

16 Bit Timers:

Timers 0 and 1 are nearly identical. Timer 2 has several additional features such as up/down counting, capture values and an optional output pin that make it unique.

Timer 0 and 1 both have four operating mode.

- 13 bit Timer/Counter
- 16 bit Timer/Counter
- 8 bit Timer/Counter with auto reload
- Two 8 bit Timers

These modes are controlled by the TMOD registers. Each timer can also serve as counter of external pulses (1 to 0 transition) on the corresponding Tn pin. This selection is controlled by the TMOD register.

Timer 0 and 1 are enabled using the TCON register which is also the location of their flags.

Each timer consists of a 16 bit registers in two bytes. These are called TLO, TL1 and TH1. Each timer in broken into low and high bytes. Software can read or write any of these locations at any time.

TIME MODE CONTROL (TMOD):

SFR 89h	Gate	$\overline{C/T}$	M1	M0	Gate	$\overline{C/T}$	M1	M0

GATE (bit 7) Timer/Gate Control : This bits enables or disables the ability of Timer 1 to increment.

$\overline{C/T}$ (bit 6) Timer 1 Counter / Timer Select

M1, M0 : Timer 1 Mode Select

Bits 5-4 : These bits select the operating mode of Timer 1.

M1	M0	MODE
0	0	Mode 0 : 8 bits with 5 bit prescale
0	1	Mode 1 : 16 bits
1	0	Mode 2 : 8 bits in the auto reload
1	1	Mode 3 : Timer 1 is halted but holds its counts.

Gate (bit 3) Timer 0 gate control

$\overline{C/T}$ Timer 0 Counter / Timer select

M1, M0 Timer mode select

M1	M0	MODE
0	0	Mode 0 : 8 bits with 5 bit prescale
0	1	Mode 1 : 16 bits
1	0	Mode 2 : 8 bits in the auto reload
1	1	Mode 3 : Timer 0 is two bit counters.

SERIAL I/O:

High speed micro controller provided two fully independent UARTs (serial ports) for simultaneous communication over two channels. The UARTs can be operated in identical or different modes and communication speed.

Each UART has an associated control register (SCON 0, SCON 1) and each has a transmit / receive register (SBUF 0 nd SBUF 1). The SFR location are

SCON 0	-	98h	SBUF 0	-	99h
SCON 1	-	C0h	SBUF 1	-	C1h

The SBUF location provides access to both transmit and receive registers. Reads are directed to the receive buffer and writes to the transmit buffer automatically.

SERIAL MODE SUMMARY:

Each port provides four operating modes. These offer different communication protocols and baud rates. These modes are summarised briefly as follows:

MODE 0:

Provides synchronous communication with external devices.

Serial I/O occurs on the RXD pin.

Shift clock is provided on the TXD pin.

MODE 1:

Provides standard full duplex asynchronous communication.

A total of 10 bits is transmitted including 1 start bit, 8 data bit and 1 stop bit.

The received stop bit is stored in bit location RB8.

MODE 2:

Asynchronous mode that transmits a total of 11 bits –1 start bit, 8 data bits, a programmable ninth nit and 1 stop bit.

The ninth bit is determined by the value in TB8.

MODE 3:

Transmits 11 bits

Generates baud rates via the timer.

80C32 COMPATIBILITY:

The DS 80 C320 is a CMOS 80C32 compatible micro controller designed for high performance. In most cases the DS 80C320 can drop into an existing 80 C32 design to significantly improve the operation. Every effort has been made to keep the device familiar to 80C32 users, yet it has many new features. In general, software written for existing 80 C32 based systems will work on the DS 80C320. The exception is critical timing since the high speed micro controller performs its instructions much faster than the original. It may be necessary to use memories with faster access times if the same crystal frequency is used.

The DS 80 C320 runs the standard 8051 instruction set and is pin compatible with 80 C32 in any of 3 standard packages. The DS 80 C320 also provides the same timer/counter resources, full-duplex serial port, 256 bytes of scratch pad RAM and i/p ports as the standard 80 C32. Timers will default to a 12 clocks per cycle operation to keep timing compatibility with original 8051 system. However they can be programmed to run at 4 clocks per cycle if required.

2.5. HIGH SPEED OPERATION:

The DS 80 C320 is built around a high speed 80 C32 compatible core. High speed comes not just from increasing the clock frequency, but from a newer, more efficient design.

In this updated core, dummy memory cycles have been eliminated. In a conventional 80 C32, machine cycles are generated by dividing the clock frequency by 12. In DS 80 C320, the same machine cycle is performed in 4 clocks. Thus the fastest instruction, one machine cycle, is executed 3 times faster for the same crystal frequency. A comparison of the timing differences. Some instructions will get between 3 to 1 speed improvement and some between 1.5 to 2.4x improvement. Generally, all instructions are faster than the original 8051.

The numerical average of all opcodes is approximately a 2.5 to 1x speed improvement. Speed sensitive applications should make the most use of instructions that are 3 times faster. When these architecture improvements are combined with 0.8μm CMOS, the result is a single cycle instruction execution in 160ns. The dual data pointer feature also allows the user to eliminate wasted instruction when moving blocks of memory. New hardware are accessed using special function registers that do not overlap with standard registers.

CHAPTER 3

AUXILLARY IC DETAILS

OTHER AUXILLARY IC'S:

1. RAM (62 C 256)
2. Buffer (74HCT245) high speed CMOS logic
3. EPROM (27C512)
4. Latch (74HCT573) high speed CMOS logic

3.1 RAM (62 C 256):

Features : MCM 62256, 28 pin Dip package

- Single 5V supply, 10%
- 32K x 8 organisation
- Fully static design – No clock or timing strober needed
- Low power dissipation – 27.5 MW/MHz
- Output enable and chip enable for more system design flexibility and low power stand by mode.
- Battery backup capability data retention supply voltage 2 to 5.5.v.
- All inputs and outputs are TTL compatible.
- Access time is 85ns.

DESCRIPTION:

The MCM 62256 is a 262, 144 bit low power static random access memory. It is organised as 32,768 words of 8 bits, fabricated using silicon gate CMOS technology static design eliminates the need for external clock and reduces power consumption and gives greater reliability. The operating current is 5mA/MHz. For long cycle timing > 100ns the automatic power down circuitry (APD) will temporarily shut down various power consuming circuits, thereby reducing active power consumption.

3.2. BUFFER (74HCT245) HIGH SPEED CMOS LOGIC:

Features : Octal bus transceiver, 3 state, noninverting

Buffer input

3 state output

Bus line driving capability

DESCRIPTION:

The RCA74HCT245 are high speed octal 3 – state bidirectional transceivers intended for two way asynchronous communication between data buses. They have high drive current outputs which enable high speed operation while driving large bus capacitance. They provide the low power consumption of standard CMOS circuits with speeds and drive capabilities comparable to that of LSTTL circuits.

The 74HCT245 allow data transmission from the A bus to the B bus or from B bus to the A bus. The logic level at the direction input (DIR) determines the direction. The output enable input (OE) when high, puts the i/o ports in the high impedance state.

3.3 EPROM (27C512):

Erasable programmable read only memory is abbreviated as EPROM. It is a port in which software is stored. EPROM is in control with micro controller. The control program is executed by using controller.

Features: 512 K (64 K x 8) CMOS or Erasable PROM

High speed performance

- 120ns access time available

CMOS technology for low power consumption

- 40mA active current
- 100 A stand by current
- OTP (One time programming) available
- Auto insertion compatible plastic packages.
- Auto ID TM aids automated programming

Two programming algorithms allow improved programming times.

- Fast programming
- Rapid pulse programming

Organised 64K x8 JEDEC standard pin out

- 28 pin Dual inline package
- 32 Pin chip carrier.

Available for extended temperature ranges.

- Commercial 0C to 70C
- Industrial 40C to 85C
- Military (B) 55C to 125C

DESCRIPTION

The microchip technology Inc.127C512 is a CMOS 512K bit (ultraviolet light) Erasable (electrically) programmable read only memory. The device is organised into 64 K words by 8 bits (64 k bytes). Accessing individual bytes from an address transition or from power- up (chip enable pin going low) is accomplished in less than 120ns. This very high speed device allows the most sophisticated microprocessor to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in system where reduced power consumption and reliability are required.

MODES:

Operation Modes	CE	OE/VPP	Ag	00-07
Read	V_{IL}	V_{IL}	X	D_{out}
Program	V_{IL}	V_H	X	D_{in}
Program verify	V_{IL}	V_{IL}	X	D_{out}
Program inhibit	V_{IH}	V_H	X	HighZ
Standy by	V_{IH}	X	X	High Z
Output disable	V_{IL}	V_{IH}	X	HighZ
Identity	V_{IL}	V_{IL}	V_H	Identity Code

x – don't care

READ MODE:

Read mode is accessed when

The $\overline{CE}$ pin is low power up (enable) the chip

The OE/V_{PP} pin is low to gate the data to the output pins.

STAND BY MODE:

Standby mode is defined when the $\overline{CE}$ pin is high and a program mode is not identified. When this condition is met, the supply current will drop from 40mA to 100μ A.

ERASE MODE:

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all 1's state as result of being exposed to UV light. To ensure complete erasure, a dose of 15 watt second/Cm^2 is required. This means that the device window must be placed within one inch and directly underneath an UV lamp with a wavelength of 2537 Angstroms, intensity of 12,000 $\mu W/Cm^2$ for 20 minutes.

PROGRAMMING MODE:

Two programming algorithms are available. The fast programming algorithm is the industry standard programming mode that requires both initial programming pulse and over programming pulse. The fast programming algorithm is recommended for windowed product only.

Programming takes place when:

- V_{cc} is brought to the proper voltage.
- OE/V_{PP} is brought to the proper VH level.

Since the erased state is '1' ,the array programming of '0'is required. The address to be programmed is set via pin AO – A15 and data to be programmed is presented to pins D_o –D_7 when data and address are stable, a low going pulse on the $\overline{CE}$ line programs in that location.

VERIFY:

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met,

- Vcc is all at the proper level.
- The $\overline{OE}/V_{PP}$ is low
- The $\overline{CE}$ line is low.

INHIBIT:

When programming multiple devices is parallel with different data, only $\overline{CE}$ needs to be under separate control to each device by pulsing the $\overline{CE}$ line low on a particular device, that devices will be programmed, all the other devices with $\overline{CE}$ held high will not be programmed with the data.

3.4 LATCH (74HCT573) HIGH SPEED CMOS LOGIC:

Features : Octal transparent Latch, 3 state output

- Common latch enable control
- Common 3 state output enable control
- Buffered input

- 3-State outputs
- Bus line driving capacity
- Typical propagation delay = 12ns.

DESCRIPTION:

The RCA 74HCT573/373 are high speed octal transparent latches manufactured with silicon gate CMOS technology. They possess the low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LSTTL devices.

The outputs are transparent to the input when the latch enable $(\overline{LE})$ is high. When the latch enable $(\overline{LE})$ goes low the data is latched. The output enable $(\overline{OE})$ control the 3 state output. When the output enable $(\overline{OE})$ is high the outputs are in high impedance state. The latch operation is independent to the state of the output enable. The 373 and 573 are identical in function and differ only in their pin out arrangement.

CHAPTER 4

DISPLAY CONTROLLER

HD61830B (Dot Matrix Liquid Crystal Graphic Display Controller)

The HD61830B is a dot matrix liquid ctrystal graphic display controller LSI that stores the display data sent from an 8 bit microcomputer in the external RAM to generate dot matrix liquid crystal driving signals.

It is possible to select the graphic mode in which the 1-bit data of the external RAM corresponds to the ON/OFF state of 1 dot on liquid crystal display and the character mode in which characters codes in the external RAM and developing them into the dot patterns with the internal character generator ROM. Both modes can be provided for various applications.

4.1 FEATURES

- Dot matrix liquid crystal graphic display controller
- Display control capacity
- Graphic mode - 512 K dots (216 bytes)
- Character mode-4096 character (212 character)
- Internal character generator ROM – 7360 bits
- 160 types of 5 x 7 dot character fonts
- 32 types of 5 x 11 character fonts
- Total 192 types
- Can be extended to 256 types (4K bytes max.) by external ROM
- Interface to 8 bit MPU
- Display duty (Can be selected by a program)
- Static to 1/128 duty selectable
- Various instruction functions
- Scroll, Cursor ON/OFF/Blink, Character blink, Bit manipulation
- Display method – selectable A or B types
- Operating frequency – 2.4 MHz
- Low power dissipation : Single +5V
- CMOS Process
- 60-pin flat plastic packages

4.2 TERMINAL FUNCTIONS

Name	Function
DBO-7	Data bus – Three state I/O common terminal Data is transferred to MPU through DBO to DB7
CS	Chip selected – Selected state with CS = 0
R/W	Read/Write R/W=1 – MPU + HD61830B R/W = 0 – MPU + HD61830B
E	Enable Data is written at the fall of E Data can be read while E is 1.
CR	External clock input
RES	Reset – RES = 0 results in display OFF, slave mode and Hp=6
MAO~15	External RAM address output In character mode, the line code for external CS is output through MA12 to MA15 ("C" Character 1st line, "F" Character 16th line)
MDO~7	Display data bus – Three state I/O common terminal.
RDO~7	ROM data input – Dot data from external character generator is input

WE	Write enable – write signal for external RAM
CL2	Display data shift clock for LCD drivers
CL1	Display data latch signal for LCD drivers
FLM	Frame signal for display synchronisation
MA	Signal for converting liquid crystal driving signal into AC, A type
MB	Signal for converting liquid crystal driving signal into AC, B type
d1, d2	Display data serial output D1 - For upper half of screen D2 – For lower half of screen
SYNC	Synchronous signal for parallel operation Three state I/O common terminal (with pull-up MDS) Master – Synchronous signal is output Slave – Synchronous signal is input
CE	Chip enable CE = 0 – Chip enable make external RAM in active
OE	Output enable OE=1 – Output enable informs external RAM that HD61830B requires data bus.
NC	Unused terminal. Don't connect any wires to this terminal.

4.3 DISPLAY CONTROL INSTRUCTIONS

Display is controlled by writing data into the instruction register and 13 data registers. The RS signal distinguishes the instruction register from the data registers. 8-bit data is written into the instruction register with RS=1, and the code of data register is specified. After that, the 8-bit data is written in the data register and the specified instruction is executed with RS=0.

During the execution of the instruction, no new instruction can be accepted. Since the busy flag is set during this, read the busy flag and make sure it is 0 before writing the next instruction.

1. Mode control

Code $ "00" (hexadecimal) written into the instruction register specifies the mode control register.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	
Mode control reg.	0	0	0	0	Mode Data					

DB5	DB4	DB3	DB2	DB1	DB0	Cursor/ Blink	CG	Graphic /character display
I/O	I/O	0	0	0	0	Cursor OFF	Internal CG	Character Display (character mode)
		0	1			Cursor ON		
		1	0			Cursor OFF, Character blink		
		1	1			Cursor blink		
		0	0		1	Cursor OFF	External CG	
		0	1			Cursor ON		
		1	0			Cursor OFF, character blink		
		1	1			Cursor blink		
		0	0	1	0			Graphic Mode
Display ON/OFF	Master/ Slave	Blink	Cursor	Graphic/ character mode	Ext./Int./CG			

1 : Display ON 2: Display OFF

1: Master Mode 2: Slave Mode

2. Set Character pitch:

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	1
Character pitch reg.	0	0	(V_p-1) binary				0	(H_p-1)binary		

V_p indicates the number of vertical dots per character. The space between the vertically displayed characters is considered for determination. This value is meaningful only, during character display (in the character mode) and becomes invalid in the graphic mode.

The H_p indicates the number of horizontal dots per character in display, including the space between horizontally displayed characters. In the graphic mode, the H_p indicates the number of bits of 1-byte display data to be displayed. There are three H_p values.

H_p	DB2	DB1	DB0	
6	1	0	1	Horizontal character pitch 6
7	1	1	0	Horizontal character pitch 7
8	1	1	1	Horizontal character pitch 8

3. Set number of characters

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	0
No. of characters reg.	0	0	0	(HN-1) binary						

HN indicates the number of horizontal characters in the character mode or the number of horizontal bytes in the graphic mode. If the total sum of horizontal dots on the screen is taken as n

$n = H_p \times HN$

HN can be set with an even number of 2 to 128 (decimal)

4. Set number of time division (inverse of display duty ratio)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	1	1
No. of time shares reg.	0	0	0	0	$(N_x\text{-}1)$ binary					

N_x indicates the number of time division in multiplex display 1/Nx is a display duty ratio.

A value of 1 to 128 (decimal) can be set to N_x.

5. Set cursor position

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	1	0	0
Cursor position reg.	0	0	0	0	0	0	(C_p-1)binary			

C_p indicates the position in a character where the cursor is displayed in the character mode. For example, in 5 x 7 dot font, the cursor is displayed under a character by specifying C_p = 8 (decimal). The cursor horizontal length is equal to the horizontal character pitch H_p. A value of 1 to 16 (decimal) can be set to C_p. If a smaller value than the number of vertical character pitches V_p is set ($C_p \leq V_p$), and a character is overalapped with the cursor, the cursor has higher priority of display (at cursor display ON). If C_p is greater than V_p, no cursor is displayed. The cursor horizontal length is equal to H_p.

6. Set display start low order address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	
Display start address reg. (low order byte)	0	0	(Start low order address) binary							

7. Set display start high order address:

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	
Display start address reg. (high order byte)	0	0	(Start high order address) binary							

These instructions cause display start addresses to be written in the display start address registers. The display start address indicates a RAM address at which the data displayed at the top left and on the screen is stored. In the graphic mode, the start address is composed of high/low order 16 bits. In the character display, it is composed of the lower 4 bits of high order address (DB3~DB0) and 8 bits of low order address. The upper 4 bits of high order address are ignored.

8. Set cursor address (low order) (RAM write low order address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	1	0
Cursor address counter (low order byte)	0	0	(Cursor low order address) binary							

9. Set cursor address (high order) (RAM write high order address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	1	1
Cursor address counter (high order byte)	0	0	(Cursor high order address) binary							

These instructions cause cursor addresses to be written in the cursor address counters. The cursor address indicates an address for sending or receiving display data and character codes to or from the RAM. Namely, data at address specified by the cursor address are read/written. In the character, mode, the cursor is displayed at the digit specified by the cursor address.

The cursor address consists of the low order address (8 bits) and the high order address (8 bits). Satisfy the following requirements. When setting the cursor address.

1.	When you want to rewrite (set) both the low order address and the high order address.	Set the low order address and then set the high order address
2.	When you want to rewrite only the low order address	Don't fail to set the high order address again after setting the low order address.
3.	When you want to rewrite only the high order address.	Set the high order.

The cursor address counter is a 16 bit up-counter with set and Reset functions. When the bit N changes from 1 to 0, the bit N+1 is added by 1. When setting the low order address, the LSB (bit 1) of the high order address I added by 1 if the MSB (bit 8) of the low order address changes from 1 to 0. Therefore, set both the low order address and the high order as shown in above table.

10. Write display data.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	0	0
RAM	0	0	MSB (pattern data, character code) LSB							

After the code $ "OC" is written into the instruction with RS = 1, 8 bit data with RS = 0 should be written into the data register. This data is transferred to the RAM specified by the cursor address as display data or character code. The cursor address is increased by 1 after this operation.

11. Read display data:

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	0	1
RAM	1	0	MSB (pattern data, character code) LSB							

Data can be read from the RAM with PS = 0 after code $ "OD" into the instruction register. This instruction outputs the contents of data output register on Data Bus (DB0 to DB7) and then transfers RAM data specified by a cursor address to the data output register, also increasing the cursor address by 1. After setting the cursor address, correct data is not output at the first but at the second time. Thus, make one dummy read when reading data after setting the cursor address.

12. Clear bit

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	1	0
Bit clear reg.	0	0	0	0	0	0	0	(NB-1)Binary		

13. Set bit

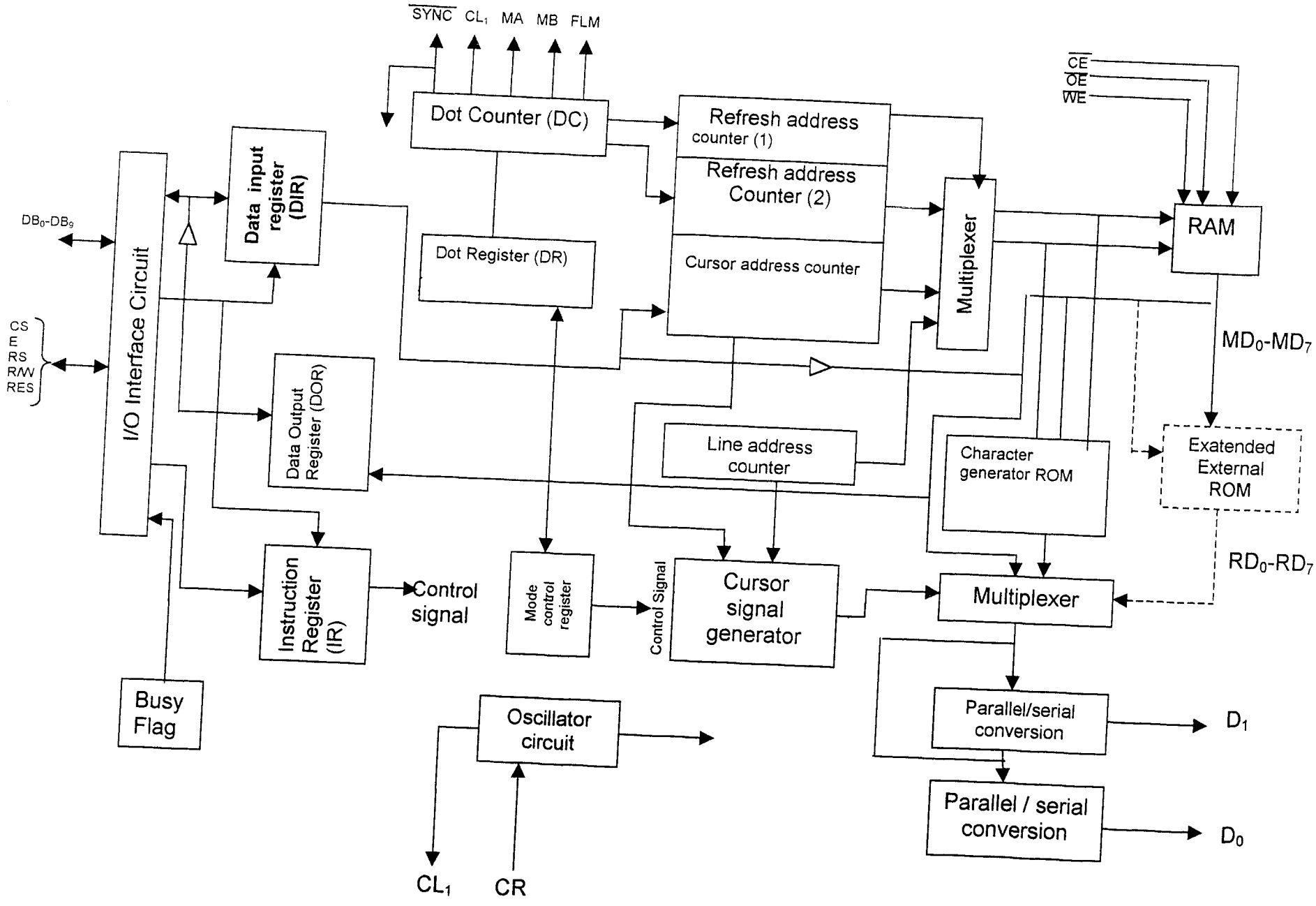
Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	1	1
Bit clear reg.	0	0	0	0	0	0	0	(N_B-1)Binary		

The clear/set bit instruction sets 1 bit in a byte of display data RAM to 0 or 1, respectively. The position of the bit in a byte is specified of NB and RAM address is specified by cursor address. After the execution of the instruction, the cursor address is automatically increased by 1. NB is a value of 1 to 8. NB=1 and NB=8 indicates LSB and MSB, respectively.

14. Read busy flag

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Busy flag	1	1	I/O							

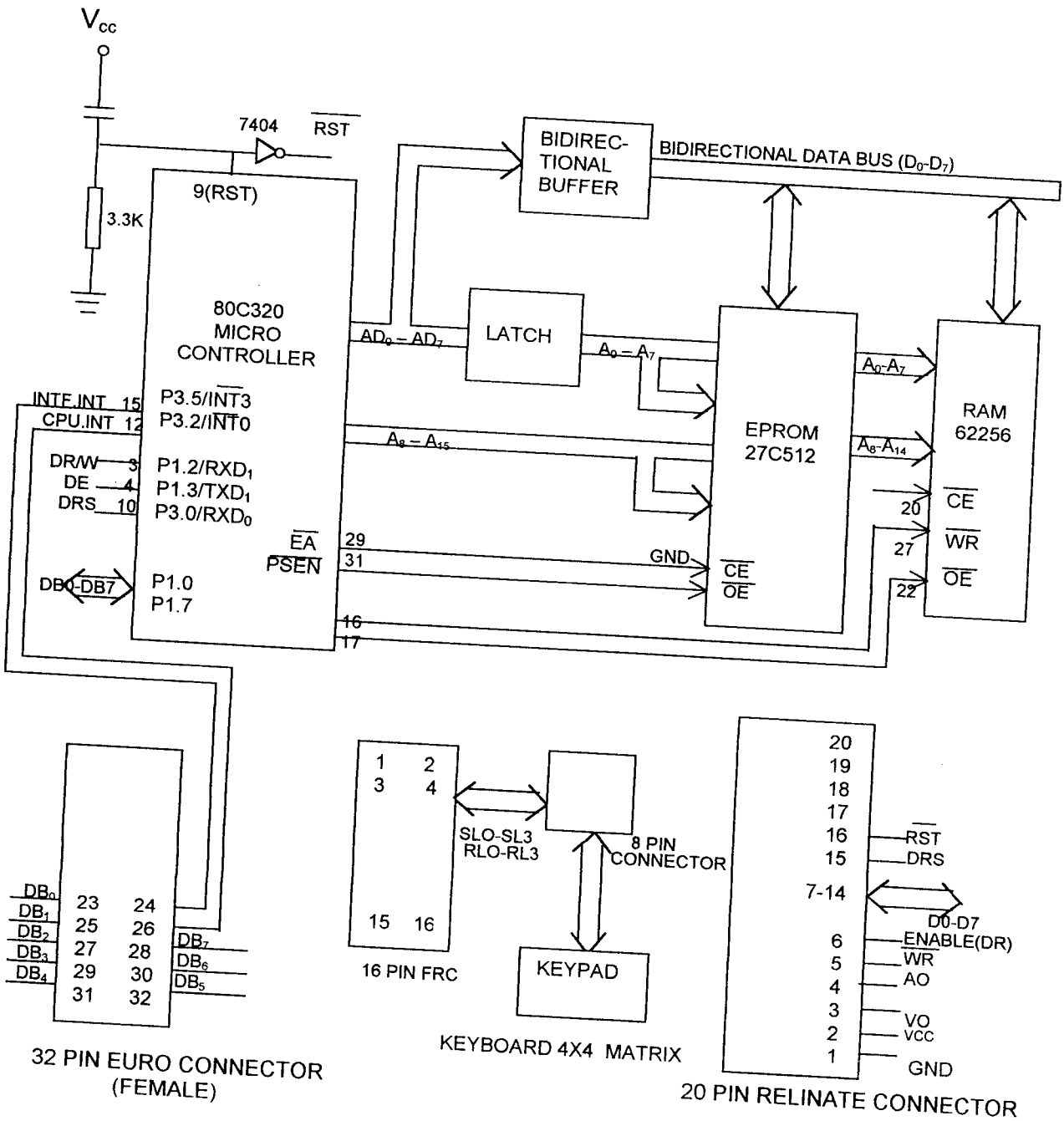
When the read mode is set with RS=1, the busy flag is output to DB7. The busy flag is set to 1 during the execution of any of instruction (1) to (13). After the execution, it is set to 0. The next instruction can be accepted. No instruction can be accepted when busy flag =1. Before executing an instruction or writing data, perform a busy flag check to make sure the busy flag is 0. Thus, no busy flag check is required just after the write operation into the instruction register with RS=1. The busy flag can be read without specifying any instruction register.


SYNC
CL1
MA
MB
FLM
Dot Counter (DC)
Refresh address counter (1)
Refresh address Counter (2)
Cursor address counter
Dot Register (DR)
Multiplexer
CE
OE
WE
RAM
DB0-DB9
Data input register (DIR)
I/O Interface Circuit
CS
E
RS
R/W
RES
Data Output Register (DOR)
Line address counter
Character generator ROM
Exatended External ROM
MD0-MD7
RD0-RD7
Instruction Register (IR)
Control signal
Mode control register
Control Signal
Cursor signal generator
Multiplexer
Busy Flag
Oscillator circuit
Parallel/serial conversion
Parallel / serial conversion
D1
D0
CL1
CR

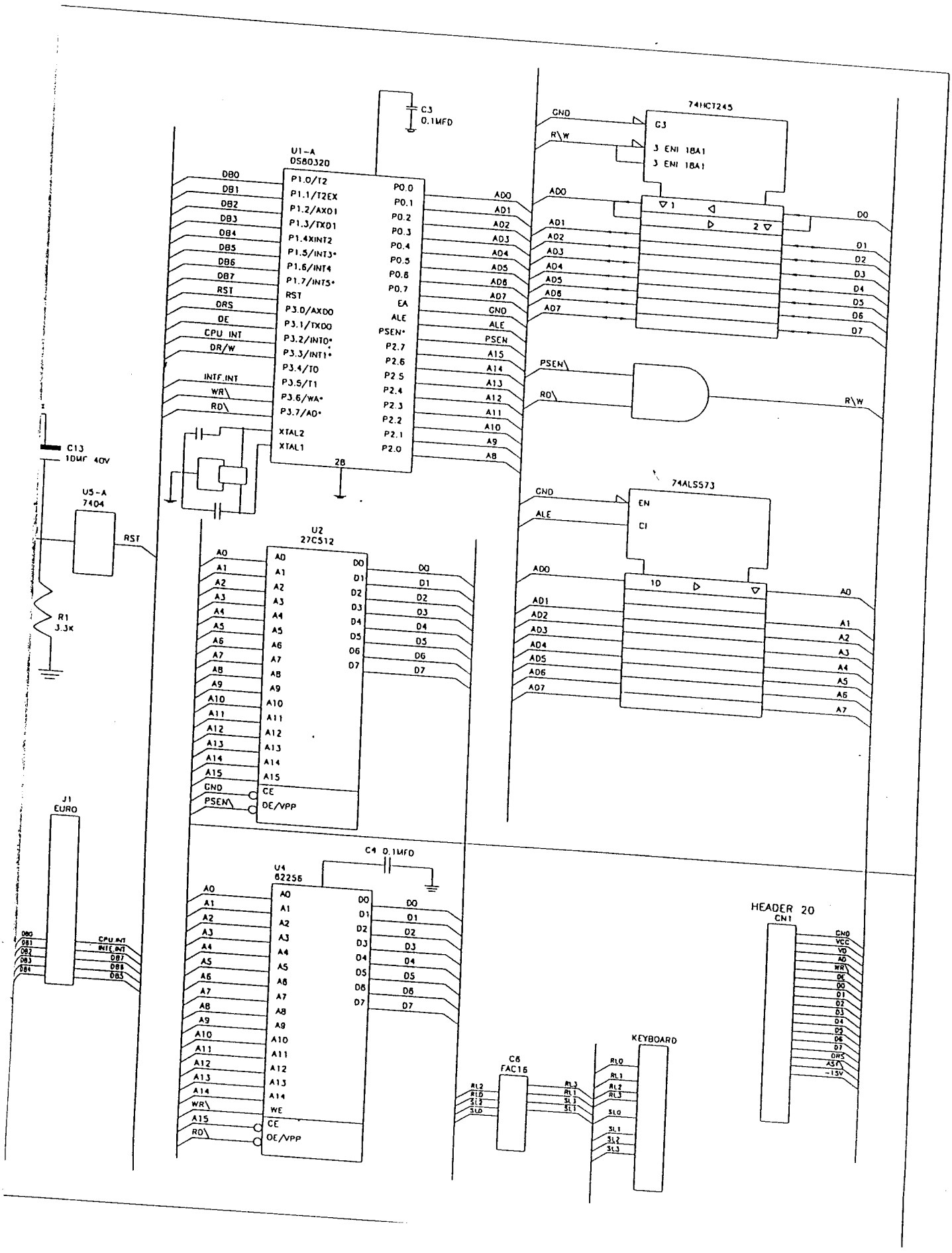
CHAPTER – 5

PCB LAY-OUT

5.1 TEST CIRCUIT BLOCK DIAGRAM



PCB SCHEMATIC OF TESTING EQUIPMENT



5.3 REALISATION OF THE DESIGN:

With the completion of the circuit diagram, the process of realisation of the design started with the selection of suitable software for the design of PCB. This lead to the selection of a software called "CADSTAR".

The 1st step in this is to draw the PCB schematic. The schematic obtained is checked for errors. Errors, if present, are rectified, and we proceed on to the 2nd stage, ie., PCB design itself. The size of the board is selected and the placement of different chips in required position is done. The final stage is "Routing". With the routing completed, the design obtained is given for fabrication.

Once the PCB is obtained, the board is checked for short circuits and track discontinuity. After this phase the soldering procedure starts. The components that are to be soldered are checked for the proper operation and its characteristics are verified. Then the components are soldered on the board. Once soldering is over the next step involved is that of loading the software into the EPROM. This process consists of erasing the previous contents of the EPROM which is done by exposing the chip to UV rays.

Once the erasure procedure is over this is then loaded into a PROM programmes which loads the necessary program into the EPROM. The PCB is set into the cabinet and after connecting the necessary power supply connection and connecting the main CPU and with this system, the cabinet is closed. Thus an explanation of fabrication of hardware is given above.

5.4 INTERFACE CARD TEST EQUIPMENT

Main aim of this test equipment is that is to test

1. address, data bus
2. Interrupts of the microcontroller
3. Ports of the controller 80C320

The testing of the above said hardware is alone using additional firmware. The main function of the card for which the test jig is developed is to interface a CPU with a 240 x 128 dots Graphical display and a 24 column printers. This card before being actually incorporated the unit is tested individually, so that it becomes easy to troubleshoot the problematic area.

The test unit consists of a microcontroller (with the associated circuitry) display, power-supply section and a keyboard.

1. With the help of the keyboard and the display, the port pints of the microcontroller is tested in the following way.
   a) The data that has to be displayed is placed on the port pins.
   b) The chip select for the display is achieved by means of logic gates.
2. The power supply section is the test equipment provides the necessary voltages to the interface card, (being tested) the display and the associated hardware.
3. The test points for various voltages are provided in the test jig; for easy accessibility.
4. The connectors for mounting and testing the interface card is provided.
5. The interrupts of the microcontroller are tested by simulating the interrupt and display the result using a 240 x 128 graphical display.
6. If a problem exist in the address – data bus –(which is very difficult to find out without a test equipment) is troubleshooted and the problem is displayed.

CHAPTER 6

POWER SUPPLY DETAILS

6.1 POWER SUPPLY

The interface card circuit uses three different voltages (+12V, +5V, -15V). The transformer used here gives an AC output of 24V. The bridge rectifier converts AC 24V to DC 24V. Then the DC 24V is given to three regulators.

1. IC 7812 for 12V constant output
2. IC 7805 for 5V constant output
3. IC 7915 for 15V constant output.

Then the outputs are finally filtered by using capacitors. For –15V supply of trimpot is added to the regulator IC 7915.

The filters used here are capacitor filters.

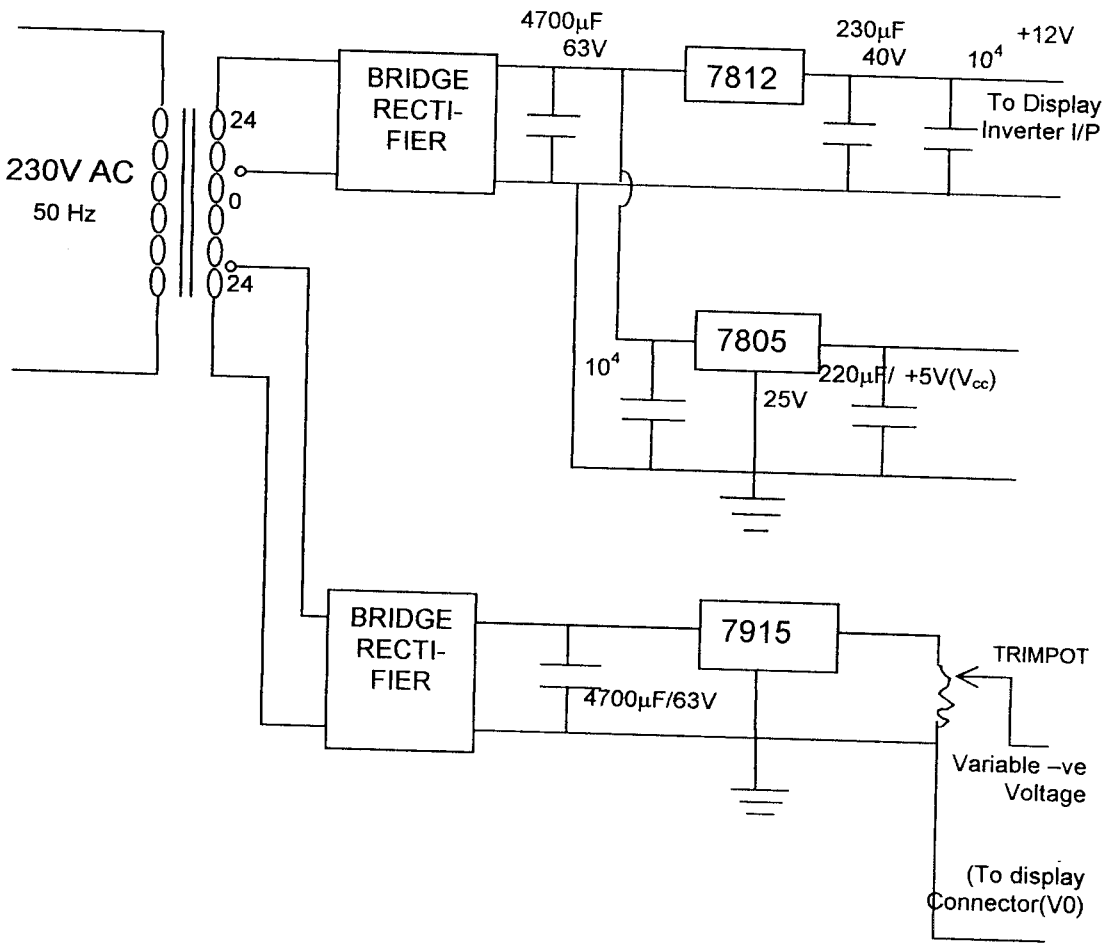
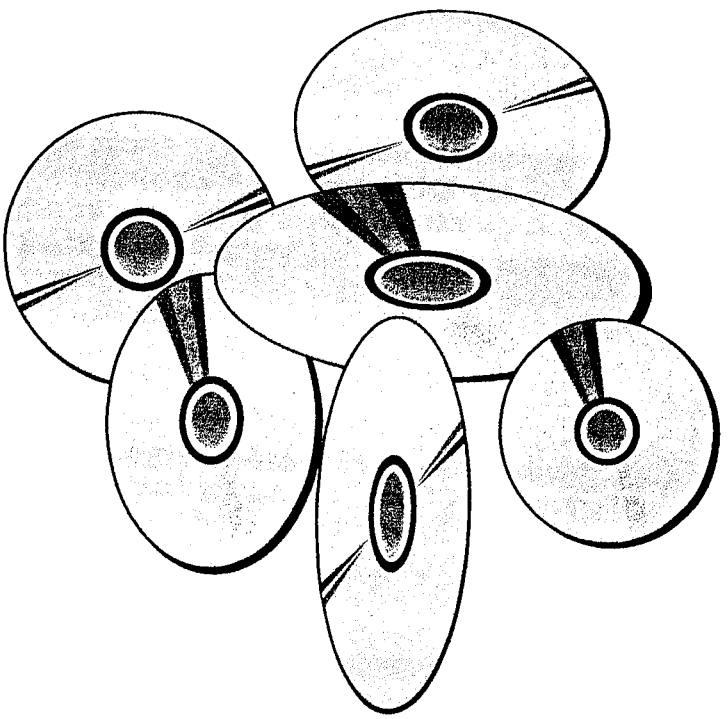


Fig.6.1. Power Supply Section



CHAPTER 7

SOFTWARE

CHAPTER 7

SOFTWARE

```
MAIN2:DO;
$INCLUDE (DEF.DEF)
   DEC CLS(1)BYTE AT (2000H) CONSTANT(' ');
   DEC LINE(2)STRC(TITLE(30)BYTE AT (1000H) CONSTANT('PREMIER –
                                                    M3000 ITRF CARD ')
   DEC INSTREG BYTE AT(0F001H)AUX;
   DEC DATREG BYTE AT(0F000H) AUX;
   DEC I BYTE;
   DEC J WORD;
BUSYCHK:PROCEDURE EXT;
END BUSYCHK;

INIT:PROC;
   INSTREG=00H;
   DATREG=03CH;     /*MODE CONTROL REG */
   CALL BUSYCHK;
   INSTREG=01H;
   DATREG=077H;    /*CHARACTER PITCH SET*/
   CALL BUSYCHK;
   INSTREG=02H;
   DATREG=1DH;     /*NUMBER OF CHARACTERS*/
   CALL BUSYCHK;
   INSTREG=03H;
   DATREG=07FH;    /*NO. OF TIME DIVISIONS,127*/
   CALL BUSYCHK;
   INSTREG=04H;
   DATREG=08H;     /*CURSOR POSITION*/
   CALL BUSYCHK;
   INSTREG=08H;
   DATREG=00H;     /*DISPLAY START ADDR LOW ORDER*/
   CALL BUSYCHK;
   INSTREG=09H;
   DATREG=00H;     /*DISPLAY START ADDR HIGH ORDER*/
   CALL BUSYCHK;
   INSTREG=0AH;
   DATREG=00H;     /*DISPLAY CUR ADDR LOW ORDER*/
   CALL BUSYCHK;
   INSTREG=0BH;
   DATREG=00H;     /*DISPLAY CUR ADDR HIGH ORDER*/
   END INIT;
```

```
        CALL INIT;          /*MAIN*/
         DO J=0 TO 479;

            CALL BUSYCHK;
            INSTREG=0CH;
            DATREG=CLS(0);
         END;
           call busychk;
           instreg=0ah;
           datreg=00h;
           call busychk;
           instreg=0bh;
           datreg=00h;
          DO I=0 TO 29;
            CALL BUSYCHK;
            INSTREG=0CH;
            DATREG=TITLE(I);
          END;
  END MAIN2;



$DEBUG
$XREF
EXTRN CODE(RECD_BYT_PROC)
EXTRN DATA(KY_RCV)

CSEG AT(50H)
IEX0:  PUSH  PSW
               PUSH  ACC
               MOV   KY_RCV,P1
               MOV   A,KY_RCV
               CLR   P3.5
               LCALL RECD_BYT_PROC
       SETB  P3.5
       POP   ACC
       POP   PSW
       RETI

               CSEG AT(0003H)
XINT0:  JMP  IEX0


END
```

```
DEC PORT_CONT  BYTE EXT AUX;
/*DEC PORT_STAT  BYTE EXT AUX; */
DEC VOLT_STAT  BYTE  EXT AUX;
DEC DISP_DATA  BYTE  EXT AUX;
DEC DISP_CONT  BYTE  EXT AUX;
DEC TIME_LSB   BYTE  EXT AUX;
DEC TIME_MSB   BYTE  EXT AUX;
DEC KEY_DAT    BYTE  EXT AUX;
DEC KEY_CONT   BYTE  EXT AUX;
DEC RTC_SLT    BYTE  EXT AUX;


main1:DO;
$ code

  BUSYCHK:PROCEDURE PUBLIC;
  DO;
  DECLARE BUSYCHCK BYTE AT (07000H)AUXILIARY;
  DECLARE INSTREG BYTE AT(0F001H)AUXILIARY;
  BUSYCHCK=INSTREG;
LOOP: IF BUSYCHCK=80H THEN GOTO LOOP;
    ELSE
      RETURN;
      END;
      END BUSYCHK;
END main1;
```

```
$ INCLUDE(REG320.DCL)
$ CODE

DECLARE DEC  LITERALLY 'DECLARE';
DEC    LIT  LITERALLY 'LITERALLY';

DEC    PROC LIT 'PROCEDURE';
DEC    AUX  LIT 'AUXILIARY';
DEC    REGI LIT 'REGISTER';
DEC    CON  LIT 'CONSTANT';
DEC    PUB  LIT 'PUBLIC';
DEC    EXT  LIT 'EXTERNAL';
DEC    STRC LIT 'STRUCTURE';
DEC    WDOG LIT 'T1';
DEC    RET  LIT 'RETURN';
DEC    INTFSTB LIT 'INT1';
DEC    OUT_BUF LIT 'NEW_ARY';
DEC    CU_VER_DIG LIT  '01H';
DEC    CU_VER_DEC LIT  '00H';
DEC    EU_VER_DIG LIT  '01H';
DEC    EU_VER_DEC LIT  '00H';
DEC    ON LIT '1';
DEC    OFF LIT '0';


KYBRD:DO;
$ INCLUDE(DEF.DEF)
$ INCLUDE(PORTS.EXT)
$ INCLUDE(KEY.DEF)
DEC FUN_KEY BYTE AUX;
DEC KEY_LOC BYTE PUB AUX;
DEC RAM_CORRUPT(32)BYTE AUX;

KEY_INIT:PROC PUB;

        KEY_CONT= CLEAR;
        KEY_CONT=KEYMOD;
        KEY_CONT=PRESC;

END KEY_INIT;
```

```
        KEY_SENSE:   PROCEDURE BYTE PUBLIC;
    DECLARE KEY_STAT BYTE AUX;

                                KEY_STAT =  KEY_CONT;
                                KEY_STAT =  KEY_STAT AND 0FH;
                                RETURN (KEY_STAT);

        END KEY_SENSE;

 GETCH:PROC BYTE PUB;
     DEC (STAT_KEY,KEY_VAL,KEY_BAK) BYTE AUX;
     KEY_VAL=0FFH;
      STAT_KEY=KEY_SENSE;
      IF(STAT_KEY<>0) THEN
      DO;
      KEY_CONT= FIFORD;
      KEY_VAL = KEY_DAT;
      KEY_VAL = KEY_VAL OR 10000000B; /* MASKING CONTROL BIT  */

                IF KEY_VAL = 081H THEN
                DO;
                      RAM_CORRUPT(1)=0FFH;
                      /* RESET */
                END;

          KEY_BAK = KEY_VAL AND  01000000B;
          IF KEY_BAK = 0H                          /* CHEKING KEY PRESENCE */
                THEN KEY_LOC = 0;                      /* KEY PRESENT */
                ELSE KEY_LOC = 1;                      /* KEY ABSENT  */

          KEY_VAL = KEY_VAL OR  11000000B;/* MASKING SHIFT KEY */
              /*  KEY_VAL  IS  ASSIGNED  THE  CORRESPONDING  ASCII
VALUES */
          IF KEY_VAL = 0C0H THEN KEY_VAL = 0DH;/* ENTER */
          IF KEY_VAL = 0D3H THEN KEY_VAL = 1BH;/* ESCAPE */
          IF KEY_VAL = 0CBH THEN KEY_VAL = 0BH;/* UP ARROW */
          IF KEY_VAL = 0C3H THEN KEY_VAL = 0AH;/* DN ARROW */
          IF KEY_VAL = 0DBH THEN KEY_VAL = 1CH;/* FUNCTION KEY */
            /*
                DO;
                      KEY_VAL = 1CH;
                      FUN_KEY = 46H;
                END;
                ELSE FUN_KEY = 00H;
            */
         IF KEY_VAL = 0C1H THEN KEY_VAL = 30H;/* NUMBER 0 */
         IF KEY_VAL = 0D8H THEN KEY_VAL = 31H;/* 1 */
```

```
            IF KEY_VAL = 0D9H THEN KEY_VAL = 32H;/* 2 */
            IF KEY_VAL = 0DAH THEN KEY_VAL = 33H;/* 3 */
            IF KEY_VAL = 0D0H THEN KEY_VAL = 34H;/* 4 */
            IF KEY_VAL = 0D1H THEN KEY_VAL = 35H;/* 5 */
            IF KEY_VAL = 0D2H THEN KEY_VAL = 36H;/* 6 */
            IF KEY_VAL = 0C8H THEN KEY_VAL = 37H;/* 7 */
            IF KEY_VAL = 0C9H THEN KEY_VAL = 38H;/* 8 */
            IF KEY_VAL = 0CAH THEN KEY_VAL = 39H;/* 9 */
            IF KEY_VAL = 02CH THEN KEY_VAL = 2EH;/* DECIMAL */
END;
                                    RETURN (KEY_VAL);
        END GETCH;
END;



DEC KEYMOD BYTE CON(01H);
DEC PRESC  BYTE CON(00110100B);  /* 34H */
DEC CLEAR  BYTE CON(0CCH);
DEC FIFORD BYTE CON(40H);


DEC PORT_CONT  BYTE PUB AT(0100H)AUX;
/*DEC PORT_STAT  BYTE PUB PUB AT(0100H)AUX; */
DEC VOLT_STAT  BYTE PUB AT(0101H)AUX;
DEC DISP_DATA  BYTE PUB AT(0102H)AUX;
DEC DISP_CONT  BYTE PUB AT(0103H)AUX;
DEC TIME_LSB   BYTE PUB AT(0104H)AUX;
DEC TIME_MSB   BYTE PUB AT(0105H)AUX;
DEC KEY_DAT    BYTE PUB AT(1000H)AUX;
DEC KEY_CONT   BYTE PUB AT(1001H)AUX;
DEC RTC_SLT    BYTE PUB AT(0101H)AUX;
DEC ALARMBLK   BIT AT(91H) REG;
DEC ALARM2     BIT AT(90H) REG;
```

```
/*  Copyright 1982,1983,1986 Intel Corporation  */

/*  REGISTER DECLARATIONS FOR 8052 */

DECLARE REG  LITERALLY 'REGISTER';

/********* BYTE REGISTERS ********/
DECLARE
  P0   BYTE  AT(80H)  REG,
  P1   BYTE  AT(90H)  REG,
  P2   BYTE  AT(0A0H) REG,
  P3   BYTE  AT(0B0H) REG,
  PSW  BYTE  AT(0D0H) REG,
  ACC  BYTE  AT(0E0H) REG,
  B    BYTE  AT(0F0H) REG,
  SP   BYTE  AT(81H)  REG,
  DPL  BYTE  AT(82H)  REG,
  DPH  BYTE  AT(83H)  REG,
  PCON BYTE  AT(87H)  REG,
  TCON BYTE  AT(88H)  REG,
  TMOD BYTE  AT(89H)  REG,
  TL0  BYTE  AT(8AH)  REG,
  TL1  BYTE  AT(8BH)  REG,
  TH0  BYTE  AT(8CH)  REG,
  TH1  BYTE  AT(8DH)  REG,
  IP   BYTE  AT(0B8H) REG,
  SCON BYTE  AT(98H)  REG,
  SBUF BYTE  AT(99H)  REG,
  PMR  BYTE  AT(0C4H) REG,
  T2CON  BYTE AT(0C8H) REG,
  t2mod byte at(0c9h)reg,
  ckcon byte at(08eh)reg,
  RCAP2L BYTE AT(0CAH) REG,
  RCAP2H BYTE AT(0CBH) REG,
  TL2    BYTE AT(0CCH) REG,
  TH2    BYTE AT(0CDH) REG,

/********** 80320 SFR*************/
  EIE    BYTE AT(0E8H) REG,
/*
  BIT 0 EX2
  BIT 1 EX3
  BIT 2 EX4
  BIT 3 EX5
  BIT 4 EWDI
  ALL OTHER BITS ARE RESERVED.
```

```
 */
   IE    BYTE AT(0A8H) REG,
 /*
   BIT 0 EX0
   BIT 1 ET0
   BIT 2 EX1
   BIT 3 ET1
   BIT 4 ES0
   BIT 5 ET2
   BIT 6 ES1
   BIT 7 EA
 */

   EIP    BYTE AT(0F8H) REG;
 /*
   BIT 0 PX2
   BIT 1 PX3
   BIT 2 PX4
   BIT 3 PX5
   BIT 4 PWDI */

/********* BIT REGISTERS ********/

 /********* PSW  BITS ********/
DECLARE
  CY


def
$ INCLUDE(REG320.DCL)
$ CODE

DECLARE DEC  LITERALLY 'DECLARE';
DEC    LIT  LITERALLY 'LITERALLY';

DEC    PROC LIT 'PROCEDURE';
DEC    AUX  LIT 'AUXILIARY';
DEC    REGI LIT 'REGISTER';
DEC    CON  LIT 'CONSTANT';
DEC    PUB  LIT 'PUBLIC';
DEC    EXT  LIT 'EXTERNAL';
DEC    STRC LIT 'STRUCTURE';
DEC    WDOG LIT 'T1';
DEC    RET  LIT 'RETURN';
DEC    INTFSTB LIT 'INT1';
DEC    OUT_BUF LIT 'NEW_ARY';
IN8155:DO;
```

```
$INCLUDE(DEF.DEF)

DEC CSREG BYTE AT(0100H)AUX;
DEC PA BYTE AT(0101H)AUX;
DEC PB BYTE AT(0102H)AUX;
DEC PC BYTE AT(0103H)AUX;
DEC TLSB BYTE AT(0104H)AUX;
DEC TMSB BYTE AT(0105H)AUX;
DEC WDOG BIT AT(0B5H)REG;
     dec mb1 bit at(097h)REG;
     dec key_cmd byte at(1001h)AUX;
     dec key_rd byte at(1000h)AUX;

     dec key_val byte AT(8000H)AUX; /*BANK1*/
     DEC KEY_ACTL BYTE AT(8001h)AUX;

     DEC CPUINT BIT AT(0B3H)REG;
     DEC INTFINT BIT AT(094H)REG;

     DEC KEY_VAL1 BYTE at(8002h)AUX;

     DEC SF BIT AT(0B2H)REG;

     dec key_pres byte at(8003h) aux;

     DEC I WORD at(8004h)aux;

in_8155:proc;
    csreg=03h;
end in_8155;

KEY_INIT:PROC;
    KEY_CMD=0CCH;
    key_cmd=01h;
    key_cmd=34h;

END KEY_INIT;

key_chk:proc;
    KEY_VAL=KEY_CMD;
    key_val=key_val and 00001111B;
    if key_val<>00h then
        key_pres=1;
        else
         key_pres=0;
end key_chk;
```

```
key_drcv:proc;
      if key_pres=1 then
      do;
         key_cmd=40h;
         key_val1=key_rd;
         WDOG=NOT WDOG;
      end;
end key_drcv;

      CALL TIME(250);
      mb1=0;
      CALL IN_8155;
      CALL KEY_INIT;
      KEY_VAL=00H;
      KEY_VAL1=00H;
           CPUINT =1;
LOOP:  CALL KEY_CHK;
      CALL KEY_DRCV;
      WDOG=NOT WDOG;
           IF(KEY_PRES=1)THEN
                DO;
                PB=KEY_VAL1;
                CPUINT=0;
          CHECK:IF INTFINT=1 THEN GOTO CHECK;
                ELSE
                DO;
                CPUINT=1;
                KEY_PRES=0;
                END;
                END;
     GOTO LOOP;


END IN8155;
```

CHAPTER 8

CONCLUSION

A testing system has been designed for automatic detection of faults in a quality control equipment, ie., Interface card, used in yarn cleaners.

To enable the system to perform the detection function, the required sequence of operations are programmed in EPROM.

PL/M-51 compiler and assembler ASM-51 are used to write the software LCD is used to display the required data in case of defects in the board that is being tested.

Since automatic detection is being tested faults in the Interface board are tracked down easily and quickly. The defects in the board, once detected, can either be rectified or new card incorporated, thus reducing the idle time of the machine which utilises the card. This leads to increased productivity and efficiency of the machine.

Thus the testing equipment developed proves to be an ideal device in winding mills.

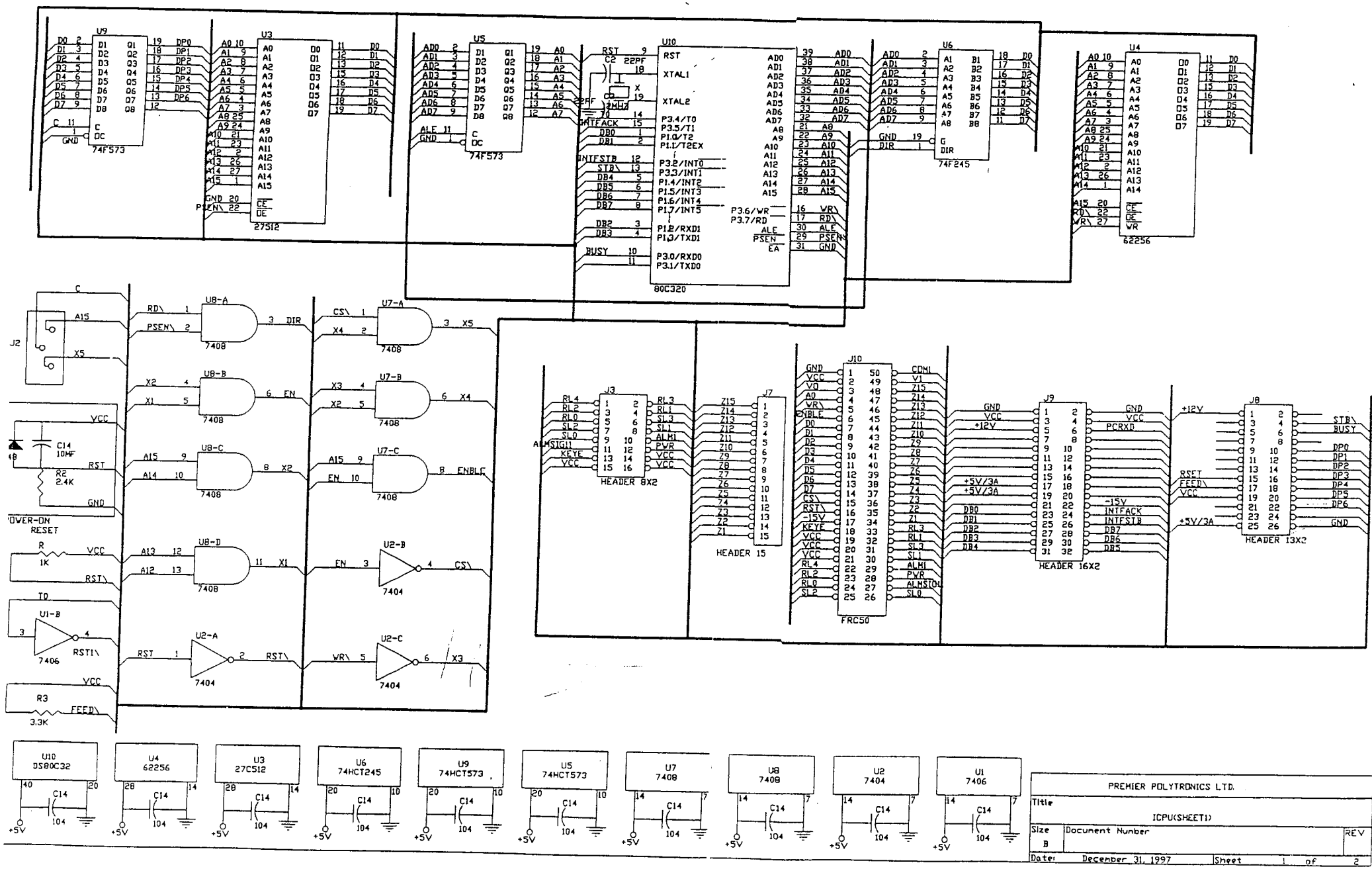
1. Microcontroller 80 C 320 by **DALLAS**

2. Micro Computer Systems by **GIBSON**

3. Power Electronics by **RASHID**

4. Digital Principles and Applications by **MALVINO LEACH**

5. Digital Integrated Electronics by **HERBERT TAUB**
DONALD SCHILLING


U9
74F573
U3
27512
U5
74F573
U10
80C320
U6
74F245
U4
62256
J2
U8-A
U8-B
U8-C
U8-D
U7-A
U7-B
U7-C
U2-B
U2-A
U2-C
U1-B
7408
7404
7406
C14
10MF
R2
2.4K
OVER-ON
RESET
R
1K
R3
3.3K
J3
HEADER 8X2
HEADER 15
J10
FRC50
J9
HEADER 16X2
J8
HEADER 13X2
U10
DS80C32
U4
62256
U3
27C512
U6
74HCT245
U9
74HCT573
U5
74HCT573
U7
7408
U8
7408
U2
7404
U1
7406
+5V
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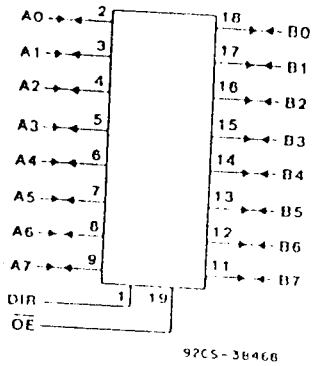
Date: December 31, 1997
Sheet 1 of 2

CD54/74HCT245

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Octal-Bus Transceiver, 3-State, Non-Inverting

Type Features:

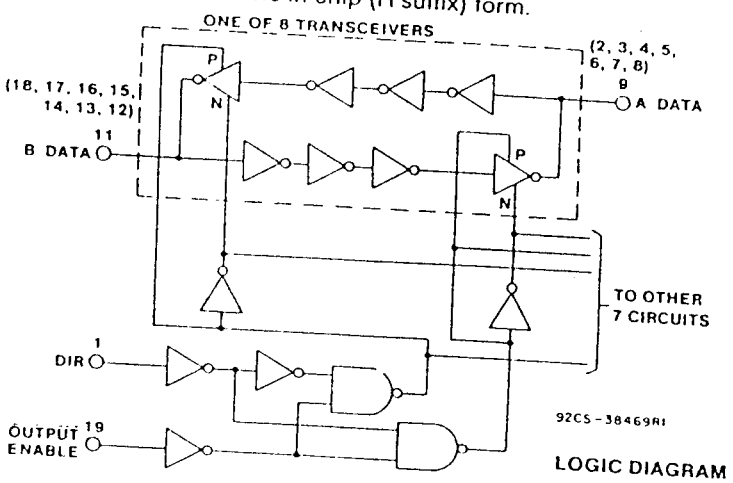
- *Buffered inputs*
- *3-State outputs*
- *Bus line driving capability*
- *Typical propagation delay (A ◄ ► B)*
  9 ns @ V_{CC} = 5V, C_L = 15 pF, T_A = 25° C

The RCA-CD54/74HC245 and CD54/74HCT245 are high-speed octal 3-state bidirectional transceivers intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high-speed operation while driving large bus capacitances. They provide the low power consumption of standard CMOS circuits with speeds and drive capabilities comparable to that of LSTTL circuits.

The CD54/74HC245 and CD54/74HCT245 allow data transmission from the A bus to the B bus or from the B bus to the A bus. The logic level at the direction input (DIR) determines the direction. The output enable input ($\overline{OE}$), when high, puts the I/O ports in the high-impedance state.

The HC/HCT245 is similar in operation to the HC/HCT640 and the HC/HCT643.

The CD54HC245 and CD54HCT245 are supplied in 20-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC245 and CD74HCT245 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line surface mount plastic packages (M suffix). Both devices are also available in chip (H suffix) form.



LOGIC DIAGRAM

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC} @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

TRUTH TABLE		
CONTROL INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B DATA TO A BUS
L	H	A DATA TO B BUS
H	X	ISOLATION

H = high level, L = low level, X = irrelevant

To prevent excess currents in the High-Z (Isolation) modes all I/O terminals should be terminated with 10KΩ to 1MΩ resistors.

MCM60256A
MCM60L256A

Advance Information

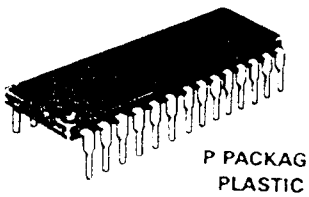
32K × 8 Bit CMOS Static Random Access Memory

The MCM60256A is a 262,144 bit low-power static random access memory organized as 32,768 words of 8 bits, fabricated using silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. The operating current is 5 mA/MHz (typ) and the minimum cycle time is 85 ns. For long cycle times (>100 ns), the automatic power down (APD) circuitry will temporarily shut down various power consuming circuits, thereby reducing the active power consumption.

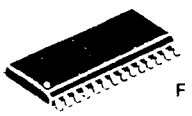
Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. When $\overline{E}$ is a logic high, the part is placed in low power standby mode. The maximum standby current for MCM60L256A is 2 μA (T_A = 25°C). Chip enable also controls the data retention mode. Another control feature, output enable ($\overline{G}$) allows access to the memory contents as fast as 45 ns (MCM60256A-85). Thus the MCM60256A is suitable for use in various microprocessor application systems where high speed, low power, and battery backup are required.

The MCM60256A is offered in a 600 mil, 28 pin plastic dual-in-line package as well as the 330 mil, 28 pin plastic small outline gullwing package.

- Single 5 V Supply, ±10%
- 32K × 8 Organization
- Fully Static — No Clock or Timing Strobes Necessary
- Low Power Dissipation—27.5 mW/MHz (Typical Active)
- Output Enable and Chip Enable Inputs for More System Design Flexibility and Low Power Standby Mode
- Battery Backup Capability (MCM60L256A)
- Data Retention Supply Voltage = 2.0 V to 5.5 V
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: MCM60256A-85 and MCM60L256A-85 = 85 ns (Max)
  MCM60256A-10 and MCM60L256A-10 = 100 ns (Max)
  MCM60256A-12 and MCM60L256A-12 = 120 ns (Max)

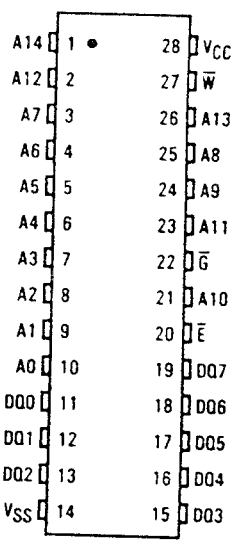


P PACKAGE
PLASTIC
CASE 710

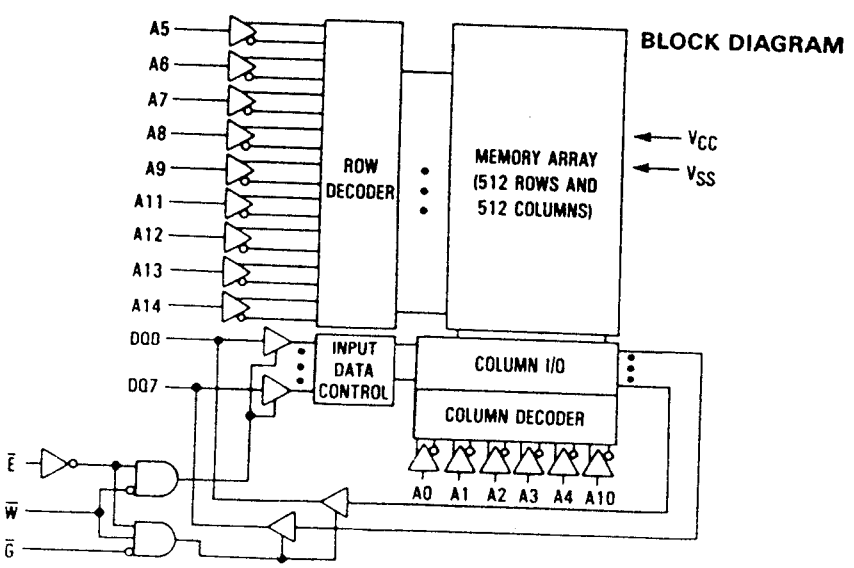


F PACKAGE
SOG
CASE 751H

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A14	Address
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Microchip

27C512

512K (64K x 8) CMOS UV Erasable PROM

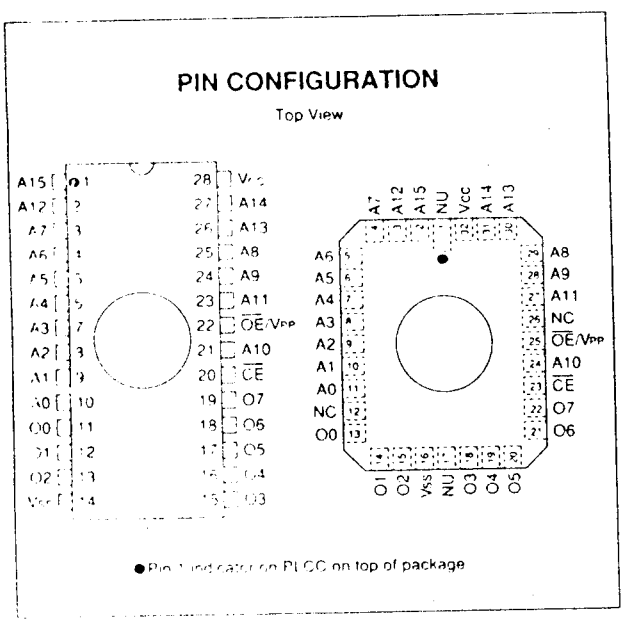
FEATURES

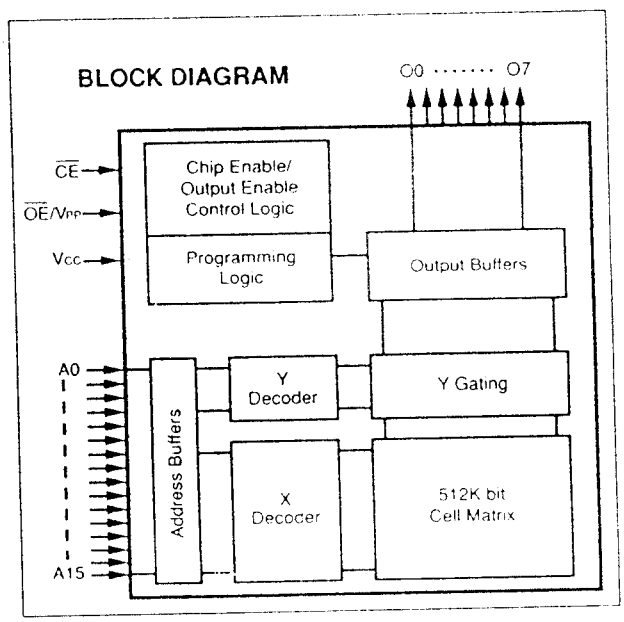
- High speed performance
  - —120ns access time available
- CMOS Technology for low power consumption
  - —40mA Active current
  - —100μA Standby current
- OTP (one-time-programming) available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- Two programming algorithms allow improved programming times
  - —Fast programming
  - —Rapid-pulse programming
- Organized 64K x 8: JEDEC standard pinouts
  - —28-pin Dual-in-line package
  - —32 pin Chip carrier (leadless or plastic)
- Available for extended temperature ranges:
  - —Commercial: 0° C to 70° C
  - —Industrial: -40° C to 85° C
  - —Military** (B): -55° C to 125° C

DESCRIPTION

The Microchip Technology Inc 27C512 is a CMOS 512K bit (ultraviolet light) Erasable (electrically) Programmable Read Only Memory. The device is organized into 64K words by 8 bits (64K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 120ns. This very high speed device allows the most sophisticated microprocessors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are requirements.

A complete family of packages is offered to provide the most flexability in applications. One-time-programming (OTP) is available for low cost (plastic) applications.





**See 27C512 Military Data Sheet DS60014