SATELLITE DISH POSITIONER
USING
REMOTE CONTROL

Project Report

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1997-98

Submitted in partial fulfilment of the requirements
for the award of the degree of
BACHELOR OF ENGINEERING
IN ELECTRONICS AND COMMUNICATION ENGINEERING
of the Bharathiar University, Coimbatore

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PROJECT REPORT 1997-'98

CERTIFICATE

This is to certify that the Project Report entitled

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IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE AWARD ON THE DEGREE OF ***BACHELOR OF ENGINEERING IN ELECTRONICS & COMMUNICATION BRANCH*** **OF THE BHARATHIAR UNIVERSITY**

HEAD OF THE DEPARTMENT **FACULTY GUIDE**

Certified that the candidate was examined by us
in the Project Work and
Viva Voce Examination held on 1.5.98
and the University Register Number was [illegible]TD0[illegible], 215, 219, 223, 52

INTERNAL EXAMINER **EXTERNAL EXAMINER**

ACKNOWLEDGEMENT

Gurur Brahma Gurur Vishnu Gururdevo Maheshwara
Gurur Shakshath Parabrahma Thasmai Sri Guravae Namaha

The essence of success is dedication to one's duty, but there are people who work behind the scene for realisation and betterment of an endeavour undertaken. They do not reap the rewards of success. But surely without them, duty undertaken would be incomplete.

People who have contributed to the successful completion of our project need a special mention in this page.

Our sincere gratitude goes to our principal Dr.Subramaniam, B.E. ,Msc (Engg),. Ph.d, S.M.IEEE for his permanent support rendered through out the project.

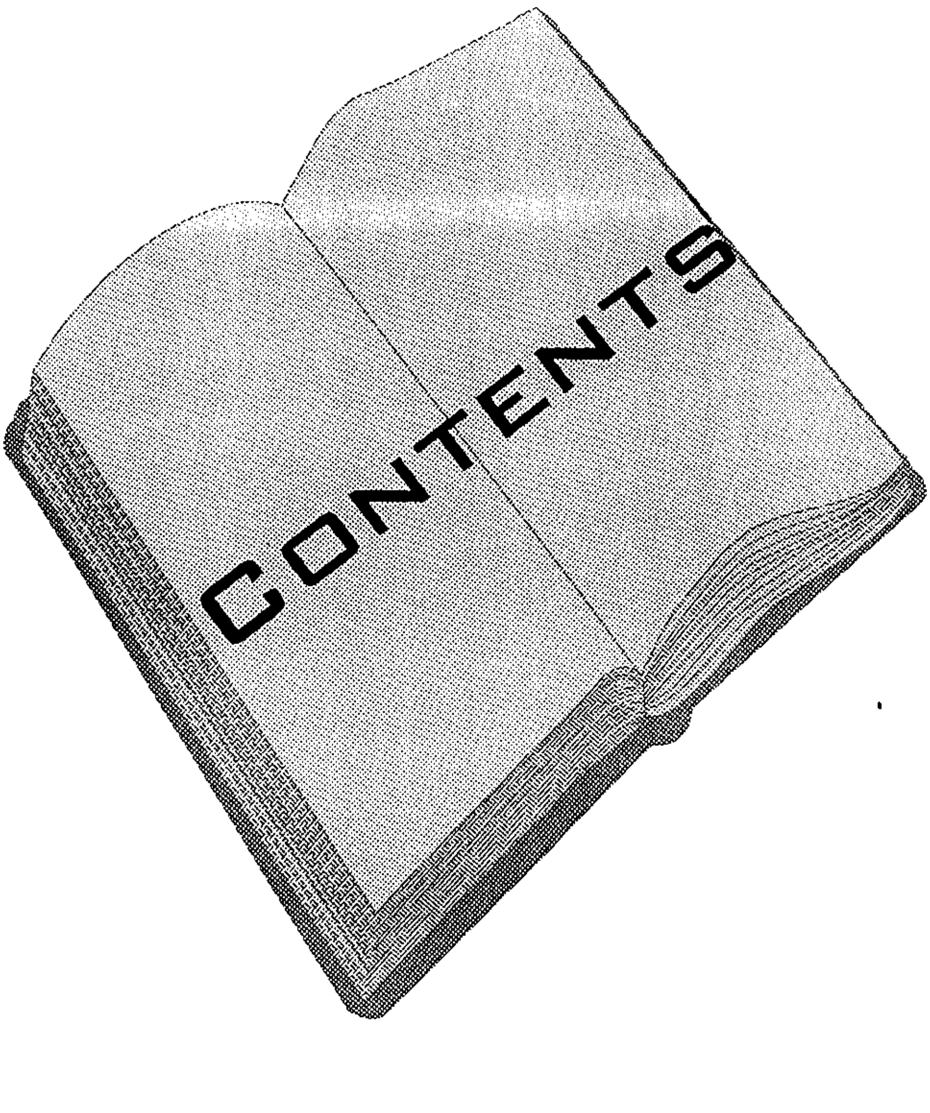
We extend our hearty gratitude to Prof.M.Ramasamy, M.E.,MISTE,MIEEE (USA),M.I.E our head of the department, who is the main source of inspiration for us to under take this project in communication side.

Our sincere thanks to our guide Ms.R.Latha, B.E., lecturer , ECE department for being the pillar of strength and support through out the course of the project.

Our acknowledgement would be incomplete if we don't thank Mr. K.Paramasivam, Managing Director, Comtek Antennas ,who enlightened us on the nuances in the field of satellite communication . His reassuring personality always enlivened us whenever we got stuck up during the progress of our project.

Also our thanks goes to Mr.Guru for the meticulous pains he took in designing our PCB.

Finally our thanks to all our friends and well wishers whose constructive criticism and timely suggestions added a touch of perfection to this endeavour.


CONTENTS

CONTENTS

INTRODUCTION

IC8401 is an Application Specific IC used to control and position a motor to specified locations based on feedback recieved from motor. Here , we utilise it to position a satellite dish.The motor action is simulated on a CRO.

The IC can be used to program any position of the dish and the position is memorised. The programming is done by using command switches present in the front panel. The position number is indicated on the display and buzzer beeps when position is reached. The limiting positions of the dish is set by the limit switch and when the dish reaches the limiting position it is indicated by a 'beep' from the buzzer. 22 positions can be memorised . The dish is operated to the required positions either by utilising the switches on the front panel or by using a remote control. Power fail circuit enables to store the position memorised upon power restoration. The direction of movement can be gauged by two direction indicating LED's and another two LED's are used for indicating power on/off for the motor and the entire system.

RATINGS

**	Supply voltage	5VDC
**	Supply current	<3mA
**	Soldering temperature	300 degree C

FEATURES

** Automatic positioning of motor

** Memorizes 22 motor drive positions.

** Uses square wave feedback

** Indication of movement direction

** Display to indicate motor position

** Remote control capability

** Status unaffected by power failure

** Three key operation and control

SYNOPSIS

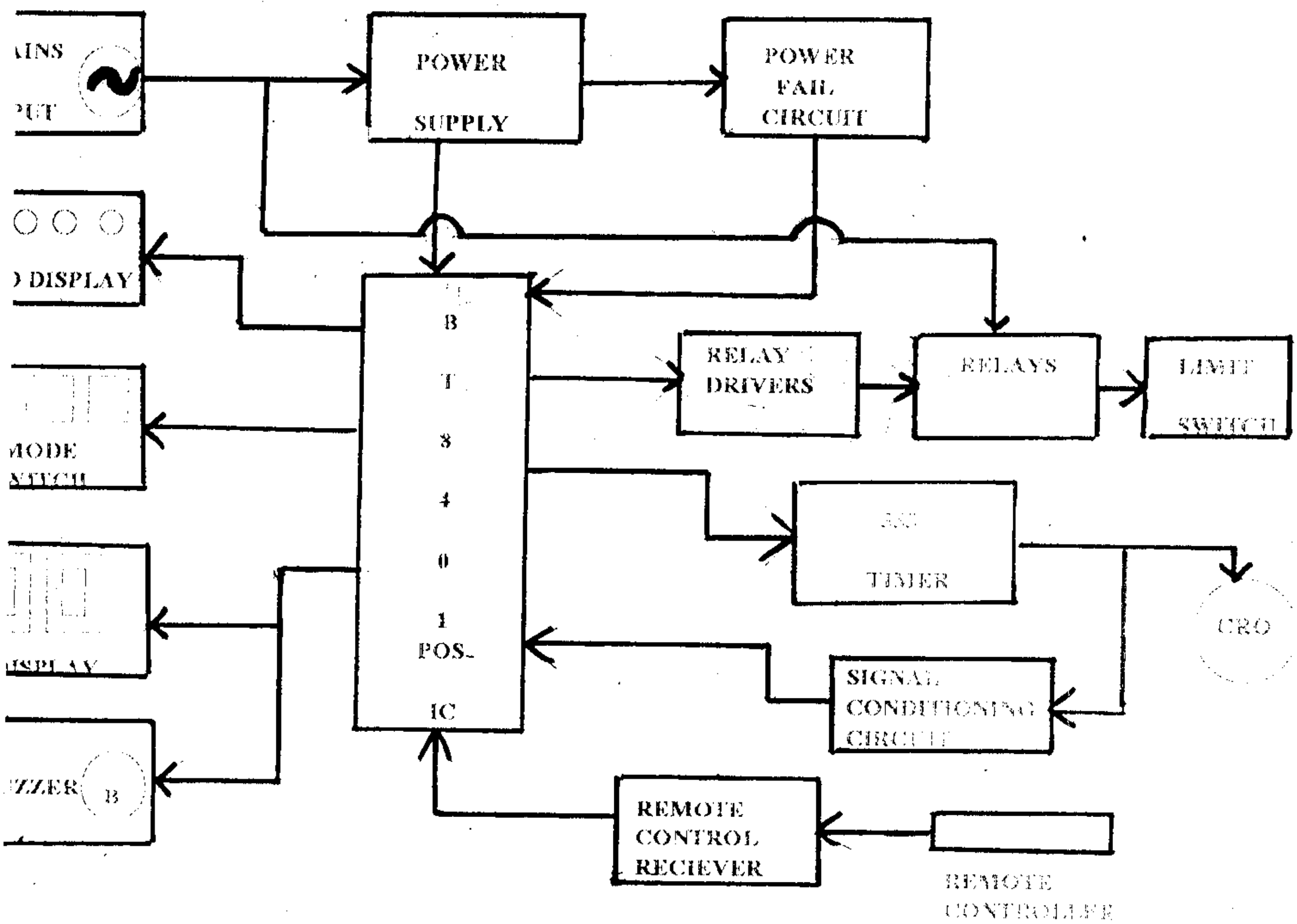
Use of radio relay techniques and radio repeaters has become very prominent in entending the range of a communication setup. Whether it is atelephone channel or a TV programme or even a fascimile signal, all of these fail to reach the users ata considerable distance from the transmitting point. Unless these signals are repeated at requiste intervals , ie the signal are recieved ,processed & retransmitted towards the destination. The concept of entending the range of a communication setup by repeating the signal has been in use for quite sometime now.

Satellite communication has emerged out of the same concept.A satellite is a type of repeater located above the earth.It is beyond doubt that communication by satellites will rule the world of communications in the last decade of the twentieth century & perhaps be the sole agent in the twenty first. Today, scores of communication satellites from various countries are orbitting around the earth & providing a continous mode of communication from one point of the globe to the other . Thus the world has shrunk with the advent of satellite communications. Our project is a small addition to the gargantuan world of satellite communications.

Using IC8401 , a satellite dish can be positioned at a point, where the reception is clear, and its position is automatically memorised using square wave feedback. Dish movement is alsoindicated. Additionally remote control capability is provided , which gives the operator, the ability to position the dish in the required direction from one's room. This represents the cheapest method to

obtain real time positioning of dish.With the status being unaffected by power failure.

BLOCK DIAGRAM



BLOCK DIAGRAM - DESCRIPTION

The motor positioner may be used as a satellite dish positioning controller. As indicated in the block diagram, the controller accepts inputs from the previous, West/Next and mode keys. position feedback from the 555 timer is also received by the controller. The controller operates the on/off and direction changing relays to position the dish. The current position is indicated by a digital display. During dish operation , the LEDs indicate dish movement and direction. In the memorize mode both the direction LEDs are on.

During inching towards a particular position, the appropriate direction LED is lit. The BT8401 may also be used as a controller for similar applications where motor positions need to be memorized.

2.1 FUNCTIONAL DESCRIPTION

The BT8401POS is a single chip solution to positioning of a satellite dish using a motor with a square wave feedback mechanism.

The advantage of using the BT8401 is reliable positioning of the dish even in adverse conditions and with intermittent power failure. Two other Ics are also used to provide the numeric display of the satellite location, as a two digit number. The IC also accepts input from a remote controller for previous and next positions.

The functional block diagram above shows how the satellite dish positioner is controlled by the BT8401 IC. The feedback signal from 555 timer, which is used to simulate the motor action on CRO, is given to the signal input pin of IC8401.

The count value is memorized during programming.

The feedback signal from the 555 is conditioned before being input to theBT8401. The required satellite position is selected by the command switches and the requested position number is indicated by the two digit display.

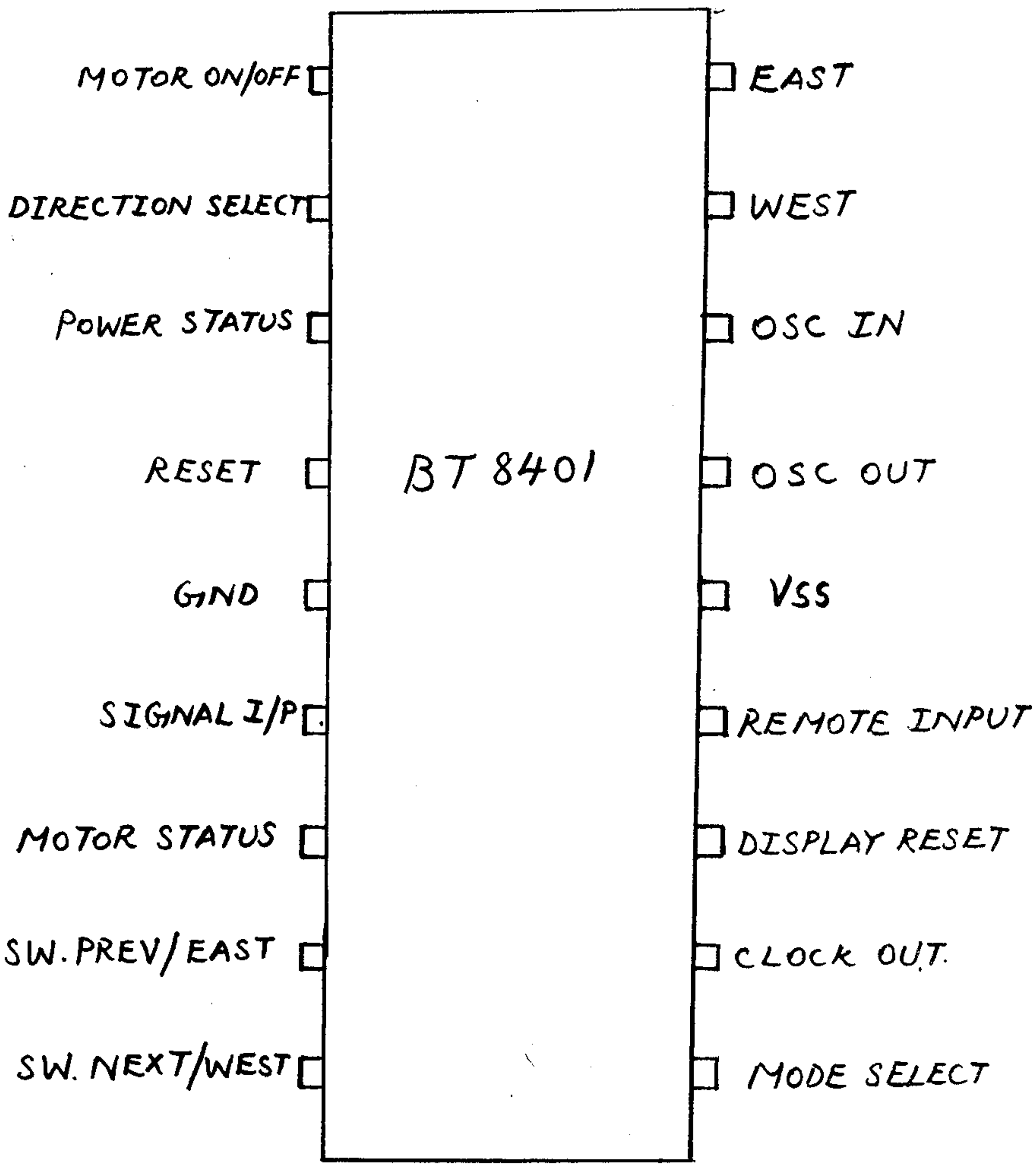
During operation, a satellite number is selected and the motor is energised in either the forward or the reverse direction by the relays.

so as to reach the required position. Three relays are used. The first relay is used for the direction change. The second relay is for motor on/off and the third relay is for the unit on/off.Limit switches are used to sense the home and end positions as well as to provide protection in case of relay failure. The power fail indication circuit provides a signal to the BT8401POS . During operation or positioning , if a power fail is detected, the current position is memorized and the system shuts down. Upon power restoration, the dish is made to go to the home position and then it is moved to the specified location before power fail occured.

The beeper sounds when the dish reaches the home position as well as during programming of the dish positions.

The remote control reciever output is connected to the BT8401 which allows changing the dish position by using a remote control transmitter. Programming functions are not available through the remote controller.The unit can be turned on\off using the remote controller as well as position the dish to the previous or next positions of the satellite. The unit can also be turned on or off using the mode key on the front panel of the unit.

PIN DIAGRAM


MOTOR ON/OFF
DIRECTION SELECT
POWER STATUS
RESET
GND
SIGNAL I/P
MOTOR STATUS
SW. PREV/EAST
SW. NEXT/WEST
BT 8401
EAST
WEST
OSC IN
OSC OUT
VSS
REMOTE INPUT
DISPLAY RESET
CLOCK OUT.
MODE SELECT

2.2 PIN DESCRIPTION OF IC8401

Pin No.	Pin Name	I/O	Description
1	MOTOR	O	Controls the motor on/off relay.
2	DIRECTION	O	Controls the direction change relay.
3	POWER	O	Turns the unit on or off.
4	RESET	I	Resets the system.
5	GROUND		Ground.
6	SIGNAL I/P	I	Recieves output information (feedback).
7	MOTOR	I	Monitors motor on or off condition and limit
8	SWITCH	I	Receives input commands from the operator
9	SWITCH	I	Receives input commands from the operator
10	MODE	I	Receives input commands from the operator
11	CLOCK OUT	O	Clock output for display segments.
12	DISPLAY	O	Resets the display.
13	REMOTE	I	Remote control input.
14	VBB		Power supply voltage input at 5VDC.
15	OSC OUT	O	Oscillator output.
16	OSC IN	I	Oscillator input
17	NEXT/WEST	O	Output to Led for direction indication.
18	PREVIOUS /EAST	O	Output to Led for direction indication.

2.3 OPERATING PROCEDURE FOR SATELLITE DISH POSITIONER

1. Switch ON system either by the MODE key or by using the remote control ON/OFF key.
2. Select the required satellite position by pressing the NEXT or PREVIOUS keys. The selected number appears on the display and the dish moves to the appropriate position. During dish movement , the direction LED is lit. After reaching the required position, all LED'S except the power LED go off.
3. You can fine tune the position by holding the NEXT or PREVIOUS keys for more than 2 seconds.
4. The remote controller may be used to position the PREVIOUS or NEXT position or turn the unit ON or OFF.

2.4 DISH PROGRAMMING PROCEDURE FOR SATELLITE POSITIONER

1. Switch ON the system using the MODE key on the front panel.
2. Press the MODE key. The east and west LEDs will glow to indicate PROGRAMMING mode.
3. Press the MODE key with the EAST key.The satellite dish will move until it reaches the extreme East end and stop after reaching the limit switch. The beeper beeps once to indicate limit reached. When the end limit is reached, the display will read 0.
4. To start memorizing the satellite positions , press and hold the WEST key until the first satellite position is reached. You can fine tune the position by pressing the EAST key or WEST key until the required position is reached. Once the final position is reached press ONLY THE MODE key to memorize this location. The unit will BEEP once to indicate correct position memorization and the display will indicate position 1. Simillarly position the dish to other satellite positions by

pressing the East key or West key to reach the required positions.

The corresponding satellite positions will be displayed as numbers. A total of 22 satellite positions may be memorized. The satellite dish will not move beyond the maximum limit switch position on the west side.

5. To EXIT the programming mode , press the MODE+WEST keys. The satellite dish will move until position 01 is reached and the unit will exit the programming mode.

6. To INSERT a new satellite position, press the MODE key in the last satellite position to enter the programming mode and press the East or West key. Press the MODE key to memorize the new position and repeat STEP 4 . The remote controller cannot be used for programming.

2.5 MANUFACTURING TEST PROCEDURE

1. Solder bridges, open and missing components were checked before proceeding with testing. Shorts between the power supply pins-TP1,TP2 and TP3 were checked.
2. Power is turned on to the unit with the BT8401 IC not inserted.The poweron LED lit up. Power supply is verified at 5VDC between TP1 and TP2 and 12VDC between TP1 and TP3.
3. Power is turned off and plugged in the BT8401. Power is turned on. MODE key is pressed once. The WEST and EAST LEDs lit up.MODE key is pressed again and the LED's go off.
4. Mode key is pressed to enter the programming mode and west key is only pressed . The power relay goes on.
5. While the dish is rotating, press the limit switch located at the end towards which the dish is rotating. The dish stops, thereby connection is checked to be correct.
6. Now the test is completed by going through the programming and operating procedure's.

CIRCUIT DIAGRAM : DESCRIPTION

The input to the IC8401 are mains input, power fail circuit, power supply, remote control unit, signal conditioning circuit,mode switches and the output of IC8401 are two common cathode LED display, buzzer, four LED's.

The main compononts in the diagram consist of IC CD 4033B which is used to provide the seven segment code to two common cathode displays . There are 4 LED 's and 3 push button switches to indicate the direction of moment of dish and on/off condition of motor and entire system.

The dish positioner IC 8401 is used to control and position the dish . It receives a feed back input from the signal conditioning circuit , called the signal i/p , which is a square wave output. A timer IC4541 is used to provide the necessary reset to IC8401 when power goes off. The dish positioner IC can be controlled by remote control also by using the next and previous buttons .

The motor action is simulated on aCRO by a 555 timer .The reset pin of a 555 timer is connected to motor on/off pin of IC8401 .555 timer provides pulses which can be viewed on a CRO ,when ever motor on/off pin is high.

The entire system is powered by +5 v &+12 v .This is providede by a 18-0-18 v transformer.The input to the IC is +5v.

HARDWARE

Hardware section of Dish Positioner consists of four sections. They are

1.DISPLAY SECTION

2.CONTROL SECTION

3.REMOTE CONTROL UNIT

4.POWER SUPPLY

4.1 DISPLAY SECTION

It consists of CD4033 Decade counter and two 7- segment LED common cathode displays, one for LSB & one for MSB. There are 3 push button switches, one to indicate the mode, another to indicate the west direction of dish movement/next position and the last one to indicate east direction of dish/ previous position. It also consists of 4 LED's one to indicate motor on/off, another to show power on/off for the entire system, and the last two to indicate the east and west direction.

IC CD4033B

CD4033B consists of a Johnson (5 stage) decade counter and an output decoder which converts the Johnson code to a 7 segment decoded output for driving one stage in a numerical display. These devices are particularly advantageous in display applications where low power dissipation & low package counter.

Input's to CD4033B are clock, reset and clock inhibit. Output's from CD4033B are carry out and 7- decoded O/P's(a,b,c, d,e,f,g). Signal's specific to the CD4033B are RIPPLE- BLANKING INPUT AND LAMPTEST INPUT and a RIPPLE- BLANKING OUTPUT.

A high RESET signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low.

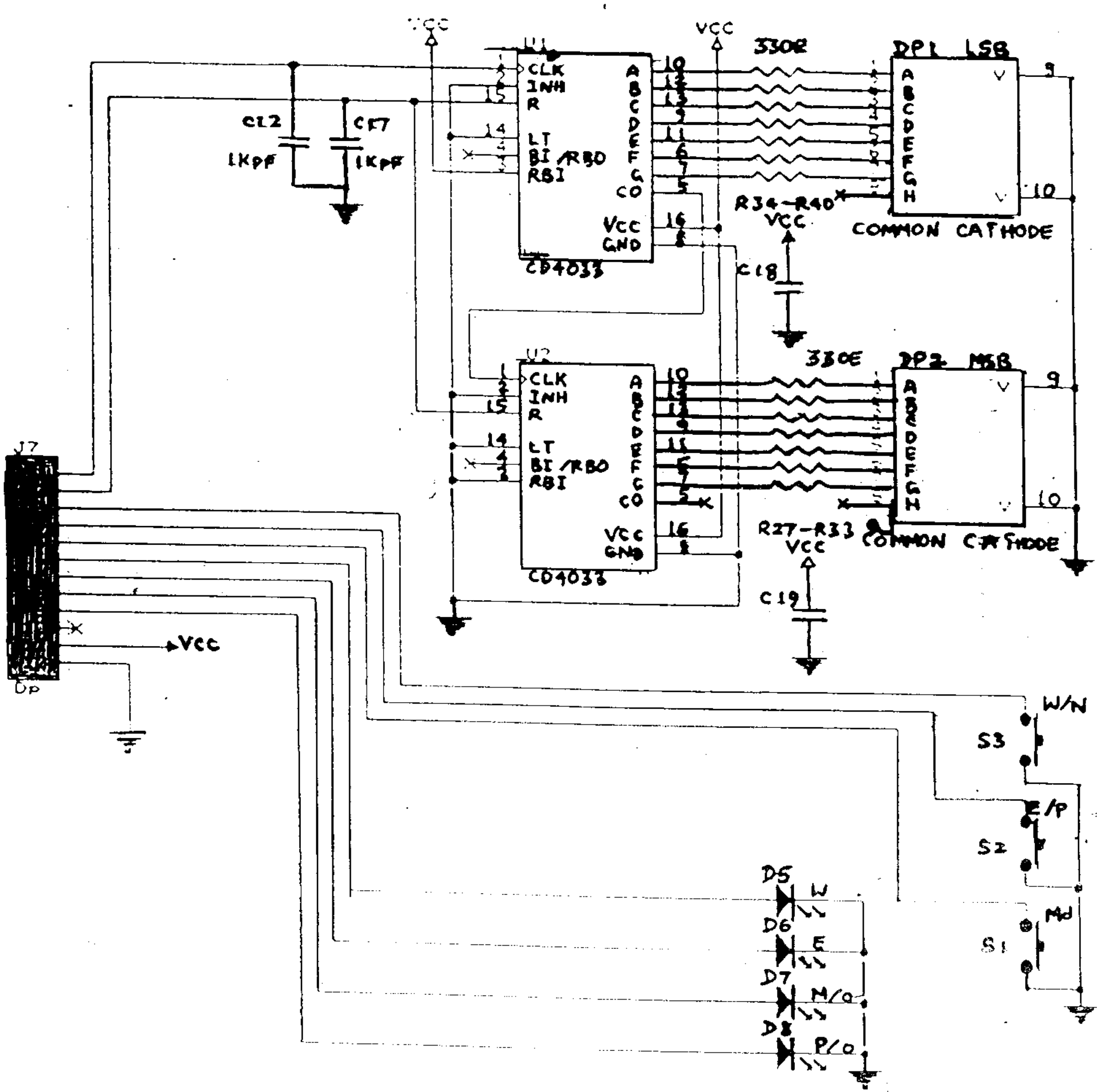
Counter advancement via the clock line is inhibited when the clock INHIBIT signal is high. The CLOCK inhibit signal can be used as a negative edge clock if the clock line is held high.

Anticlock gating is provided on the JOHNSON counter, thus assuring proper counting sequence. The CARRY-OUT (C-out) signal of CD4033B used to drive LSB of display is given to the next CD4033B.The seven decoded output,s (a,b,c,d,e,f,g) illuminate the proper segments in a seven segment display device used for representing the decimal numbers 0 to 9. IC8401 provides the display clock signal to drive the CD4033B. CD4033B can be driven by 0-6 mhz signal.

When the dish reaches the position desired ,display clock is enabled. When the clock inhibit is low, and if the display clock from BT8401IC is positive, then there will be a count advancement. This count advancement is indicated on the 7-segment LED display. A high reset signal clears the decade counter to its 0 count. When power fails, the programmable timer provides a reset to IC8401 which then provides the high display reset output to CD4033B.

This makes the 7-segment display to change to 00. Clock inhibit when high, inhibits any change in the count whenever clock

DISPLAY CIRCUIT



input changes. So here ,it is grounded so that count changes as clock input is high.

Carry out signal completes one cycle every ten clock input cycles, and is used to clock the succeeding decade directly in a multi-decade counting chain. when the first CD4033, recieves the tenth clock pulse, the carry out signal is given as clock to the next CD4033, there by activating the MSB of the display.

The 7-decoded output's provide the 7-segment code to light the corresponding digits on the display.

DISPLAY LED

The led displays used here are common cathode displays . For a common cathode display , a high is applied to a segment to turn it on. When a BCD code is sent to the inputs of the CD4033, it outputs high on the segments required to display the number represented by the BCD code.The function of multiplexing diplays is that segment information is sent out to all of the digits but only one display is turned on at a time.

SWITCHES

The push button switches are used both in the programming and in the operation mode for defining the mode,the direction of dish & to change the position of the dish. These switches are directly connected to IC8401 pins,Mode select ,switch prev/east , switch next/west.

These switches are prevented from tristate operation by using a RC circuit. When the switch is not pressed, the connection is grounded. When switch is pressed ,supply current flows to the switches, thereby operating it.

LED's

The 2 LED's for indicating the direction of dish movement are given directly from the IC8401. They indicate the east and west direction. The power status LED is also given directly. When system is on,power LED glows.

Motor on/off LED glows based on the change over of motor on relay. This is sensed by IC8401 and provides the input to Motor on LED to glow.

4.2 CONTROL SECTION

Control section consists of the main IC 8401 which is used to control and positon the dish based on feedback called signal input.It also consists of a signal conditioning circuit which provides the square wave feed back signal.

There is a programmable timer IC4541 to provide reset pulses to IC8401. A crystal provides the neccessary synchronising pulses of frequency 1.8432 MHZ. The IC8401 can be controlled by remote controller which can be used to get the next and previous position of the dish and It is not used for programming the positions . A buzzer is used to indicate the limiting position of dish and it also rings when a position is memorised.It also consists of relay drivers which is used to limit the output current in order

to drive the relay.The remote is used to control the next and previous positions of the satellite dish.

IC4541B

The RCA-CD4541B programmable timer consists of a 16-stage binary counter , an oscillator that is controlled by external R-C components(2-resistors and a capacitor) an automatic power-on reset circuit , and output control logic. The counter increments on positive edge transitions and can also be reset via the MASTER RESET input.

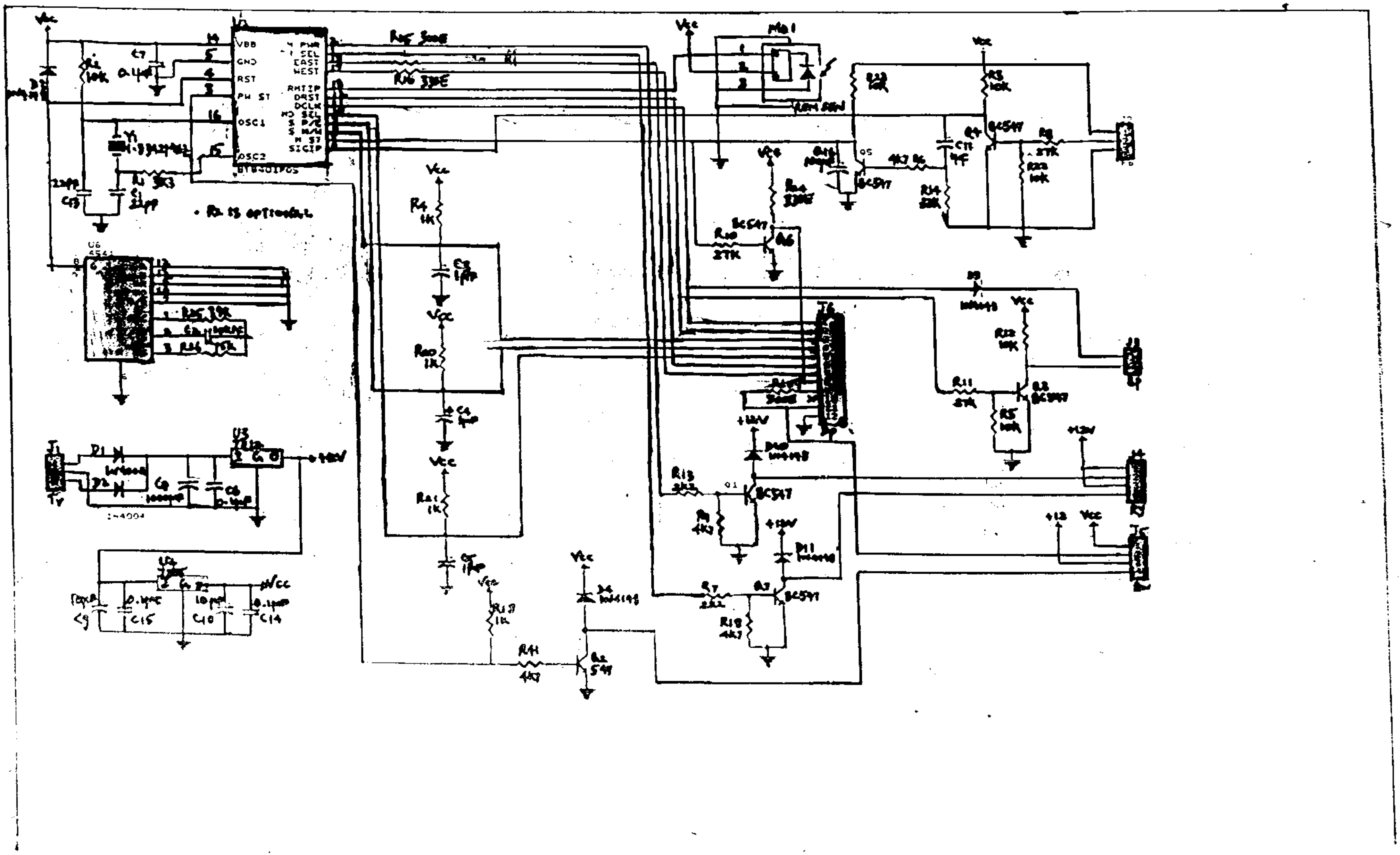
The output from this timer is the Q or Q| output from the 8th counter stage. The desired stage is chosen using time -select inputs A and B (A=0; B=0; No.of.stages(N)=13 ; count (2^N)=8192;). The output is available in either of the two modes selectable via the Mode input pin 10(PIN 5=auto reset

on; PIN 6=master reset off; PIN 9= output initially low after reset (q); PIN 10 = single transition mode.All pins are in logic 0 level i.e grounded.). With the mode input set to logic 0 and after a MASTER RESET is initiated, the output (assuming q output has been selected) changes from a low to a high state after 2^(N-1) counts and remains in that state untill another MASTER RESET pulse is applied or the MODE input is set to a logic 1.

Timing is initialised by setting the AUTO RESET input (pin 5) to logic 0 and turning power on. The AUTO RESET consumes an appreciable amount of power.

The Rc oscillator oscillates with a frequency determined by the R-c network and is calculated using $f=1/(2.3\ R_{tc}C_{tc}) = 7.348$ sec's where f is between 1 khz and 100 khz .

MAIN CIRCUIT



IC8401

When system is on, the power status pin is enabled and power on LED lights up. Oscillator pins are provided with th e synchronising signals from crystal . IC is provided with +5v supply. The initial indication on LED is 00. When either of the switches east/prev or west /next in the remote controller are pressed the dish rotates to the next or previous position. Motor on LED lights up.

When motor power is switched on the direction select pin will be enabled.Depending on the direction, the east or west LED's glow as the dish moves. When mode switch is pressed the mode select pin is enabled indicating the

start ofprogramming or operation mode. Motor status pin is used to light up the motor on/off LED. It also recieves the feedback input from the signal conditioning circuit so that when dish stops rotating the motor on/off LED is switched off.Signal input is the feedback from 555 timer to IC8401. The motor power signal is given to reset pin of 555. When motor power signal is enabled, the 555 timer produces a series of pulses which are then given to the signal input of IC8401 . When motor power is disabled, 555 timer is reset.

Signal conditioning circuit contains a common emitter configuration transistor inverting amplifier. Here , it gets the pulses for the corresponding position from the 555 timer and amplifies, inverting it and sends it to the signal input pin of IC8401 .

Once the dish has reached a particular position , display clock pin which is enabled , is given to the buzzer through a diode . It is used to prevent any negative signals getting in to the buzzer.

RELAY DRIVERS

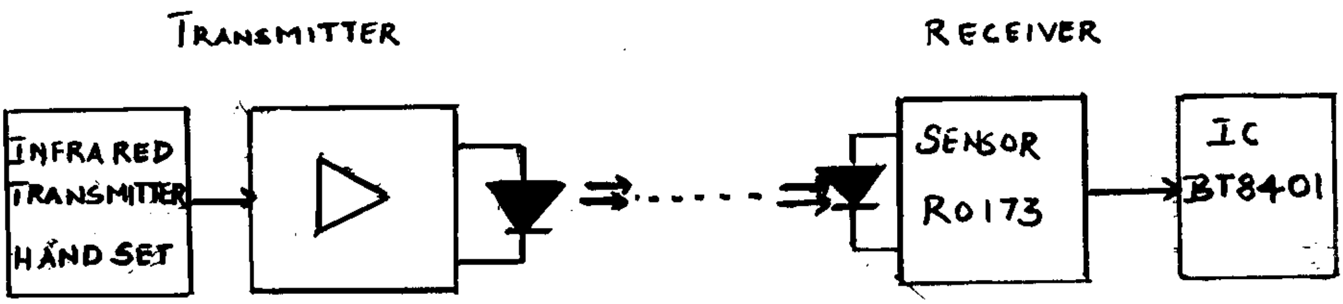
when the amplifier's input terminal goes HIGH , relay drivers turn ON the transistor and picks the relay. This arrangement does provide electrical isolation between logic and output circuits.

3.REMOTE CONTROL UNIT

PRINCIPLE OF OPERATION

Recent trend in remote controlled operation is to use infra red (IR) rays and a special binary (0&1) coding mechanism. The code intensity and the wavelength of the IR wave, helps to select the different functions. Depending on the key pressed, the signal is sent out by the IR source, normally a diode . It generates a code in the parallel format. This is converted to a series format by a shift register.

This signal is received by photosensitive devices such as an avalanche photo diode at the receiver. Here another shift register is used to control the code back



BLOCK DIAGRAM FOR AN INFRARED REMOTE CONTROL SYSTEM

POWER SUPPLY

To provide a stable DC voltage for powering the circuit, we use IC voltage regulator's (7812) and (7805).

A general block diagram of power supply is given below. It consists of transformer, rectifier, filter and regulator. For our circuit we need +12V and +5V. We use a step down transformer of 18-0-18 volt rating. Output of 18 Volt secondary is given to the centre tapped full wave rectifier circuit. Rectifier output consists of pulsating DC. To remove Undesirable AC components it is passed through a filter capacitor is used to reduce inductive effects due to long leads and coils.The other capacitor is used to improve the transient response of the regulator output.

78xx series are three terminal ,positive fixed voltage regulators. There are seven output voltage options available such as 5,12 v etc. In 78xx the last two numbers indicate the output voltage. these regulators are available in two types of packages.

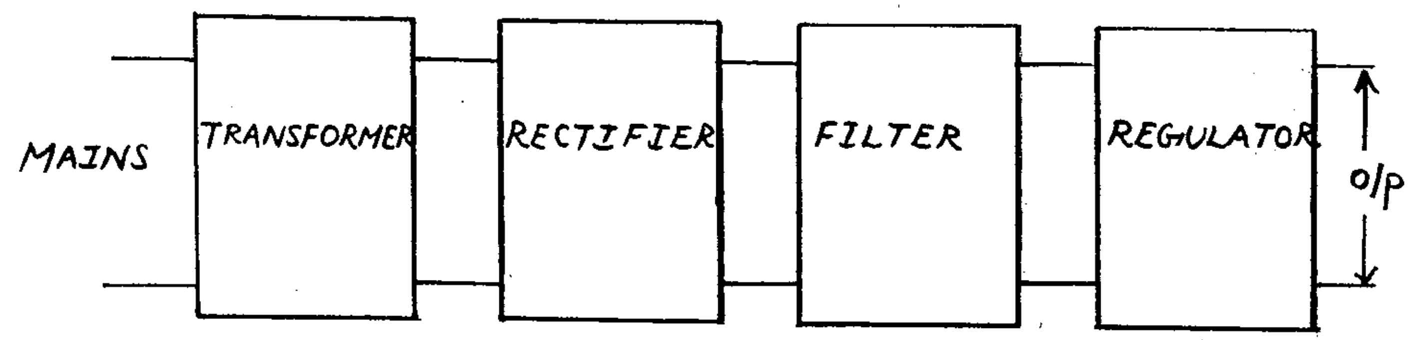
Metal package (TO-3type)

Plastic package (TO-220 type).

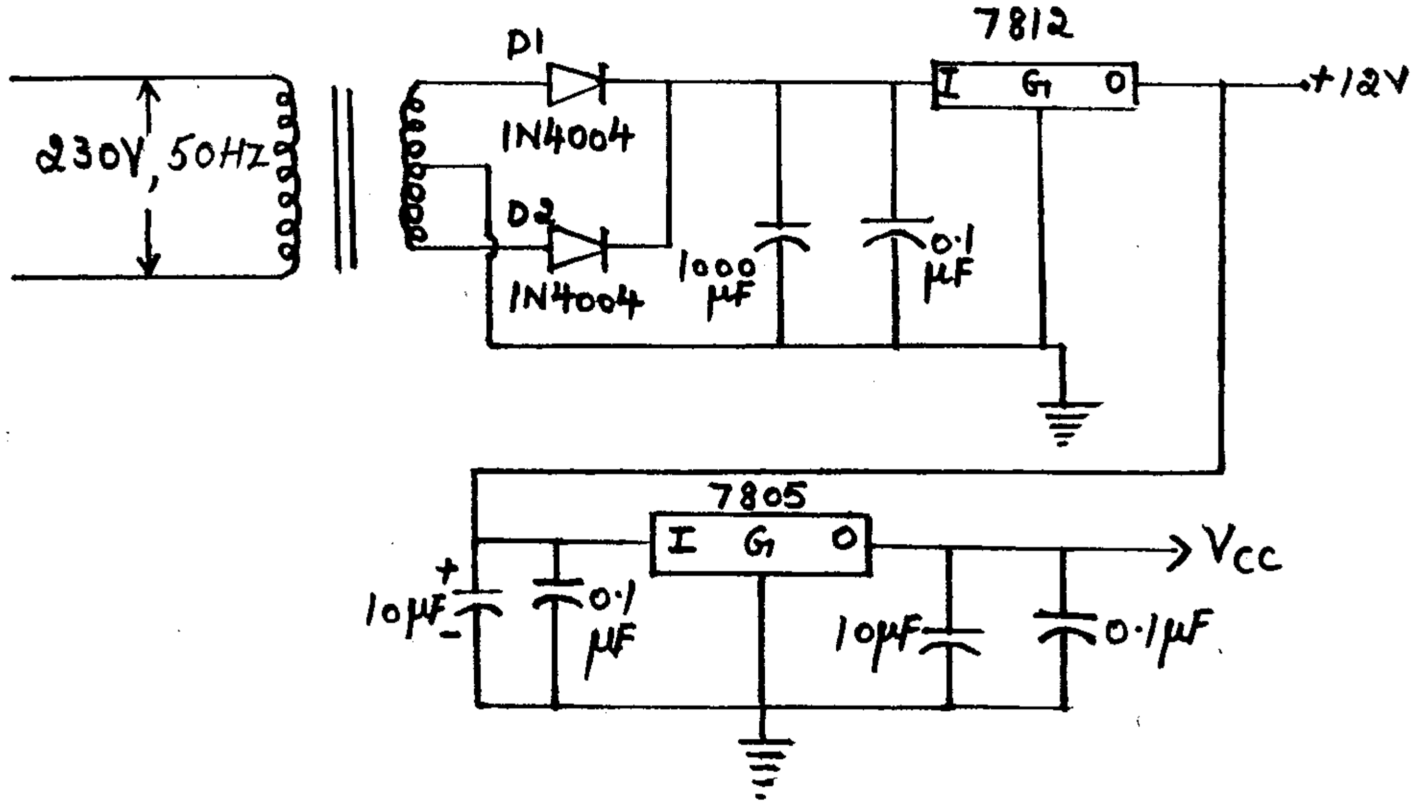
A capacitor is usually connected between input terminal and ground to reduce the inductive effects and an output capacitor to improves the transient response.

To get the output of +5v the output of 7812 IC voltage regulator is given to a capacitor filter and then given to 7805 IC voltage regulator which is used to obtain regulated output of +5v.

BLOCK DIAGRAM



CIRCUIT DIAGRAM



CONCLUSION

The satellite dish positioner is construted and tested. Different positions of the dish, which are required are memorized and dish is positioned at these points.

Its cost effectiveness in positioning, gives enormous scope for usage in many industrial applications requiring accurate positioning of the motor.

The advantage is that the position remains memorised even when power fails.

Another application is X-Y table where 2 motors are used for x& y axis. The XY location may be mentioned for repetitive positions by controlling the XY motors.

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APPENDIX-A

The Pin details and various information about the following IC's , that are used in this project, are given in detail.

1. CD4033

2. CD4541

CD4026B, CD4033B Types

CMOS
Decade Counters/Dividers

High-Voltage Types (20-Volt Rating)
With Decoded 7-Segment Display Outputs and:
Display Enable – CD4026B
Ripple Blanking – CD4033B

The RCA-CD4026B and CD4033B each consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson code to a 7-segment decoded output for driving one stage in a numerical display.

These devices are particularly advantageous in display applications where low power dissipation and/or low package count are important.

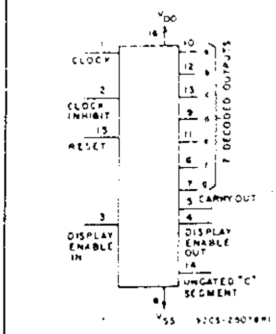
Inputs common to both types are CLOCK, RESET, & CLOCK INHIBIT; common outputs are CARRY OUT and the seven decoded outputs (a, b, c, d, e, f, g). Additional inputs and outputs for the CD4026B include DISPLAY ENABLE input and DISPLAY ENABLE and UNGATED "C-SEGMENT" outputs. Signals peculiar to the CD4033B are RIPPLE-BLANKING INPUT AND LAMP TEST INPUT and a RIPPLE-BLANKING OUTPUT.

A high RESET signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. The CLOCK INHIBIT signal can be used as a negative-edge clock if the clock line is held high. Antilock gating is provided on the JOHNSON counter, thus assuring proper counting sequence. The CARRY-OUT (C_{out}) signal completes one cycle every ten CLOCK INPUT cycles and is used to clock the succeeding decade directly in a multi-decade counting chain.

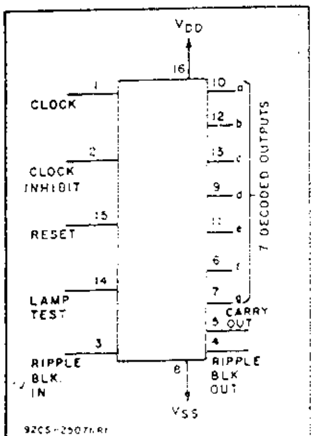
The seven decoded outputs (a, b, c, d, e, f, g) illuminate the proper segments in a seven segment display device used for representing the decimal numbers 0 to 9. The 7-segment outputs go high on selection in the CD4033B; in the CD4026B these outputs go high only when the DISPLAY ENABLE IN is high.

Features:
- **Counter and 7-segment decoding in one package**
- **Easily interfaced with 7-segment display types**
- **Fully static counter operation:** DC to 6 MHz (typ.) **at V_{DD}=10 V**
- **Ideal for low-power displays**
- **Display enable output (CD4026B)**
- **"Ripple blanking" and lamp test (CD4033B)**
- **100% tested for quiescent current at 20 V**
- **Standardized, symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**
- **Schmitt-triggered clock inputs**
- **Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications
- Decade counting 7-segment decimal display
- Frequency division 7-segment decimal displays
- Clocks, watches, timers (e.g. ÷60, ÷ 60, ÷ 12 counter/display)
- Counter/display driver for meter applications



CD4026B FUNCTIONAL DIAGRAM



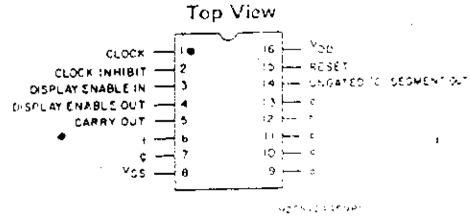
CD4033B FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	-0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

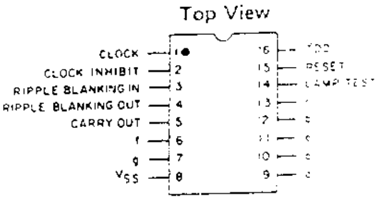
TERMINAL DIAGRAMS

Top View



CD4026B

Top View



CD4033B

MENDED OPERATING CONDITIONS

imum reliability, nominal operating conditions should be selected so that operation is within the following ranges:

CTERISTIC		V_{DD} (V)	LIMITS MIN.	LIMITS MAX.	UNITS
Voltage Range (For T_A = Full Package)erature Range)			3	18	V
ıput Frequency,	f_{CL}	5	–	2.5	MHz
		10	–	5.5	
		15	–	8	
ılse Width,	t_{WCL}	5	220	–	ns
		10	100	–	
		15	80	–	
ise and Fall Time,	t_{rCL}, t_{fCL}	5	–	Unlimited	
		10	–		
		15	–		
ıhibit Set Up Time,	t_{SU}	5	200	–	
		10	50	–	
		15	30	–	
ulse Width,	t_W	5	200	–	
		10	100	–	
		15	50	–	
lemoval Time		5	30	–	
		10	15	–	
		15	10	–	

C ELECTRICAL CHARACTERISTICS

RACTER-IC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D, F, K, H Packages Values at -40, +25, +85 Apply to E Package: –55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
ent Device ent, D Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
ıt Low k) Current)L Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
ıt High urce) rent,)H Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
ıt Voltage: v-Level, OL Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
ut Voltage: ıh-Level, ıH Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
t Low ıltage, /IL Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
t High ıltage, VIH Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
ıt Current ı Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

CD4026B

When the DISPLAY ENABLE IN is low the seven decoded outputs are forced low regardless of the state of the counter. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display-character multiplexing.

The CARRY OUT and UNGATED "C-SEGMENT" signals are not gated by the DISPLAY ENABLE and therefore are available continuously. This feature is a requirement in implementation of certain divider functions such as divide-by-60 and divide-by-12.

CD4033B

The CD4033B has provisions for automatic blanking of the non-significant zeros in a multi-digit decimal number which results in an easily readable display consistent with normal writing practice. For example, the number 0050.0700 in an eight digit display would be displayed as 50.07. Zero suppression on the integer side is obtained by connecting the RBI terminal of the CD4033B associated with the most significant digit in the display to a low-level voltage and connecting the RBO terminal of that stage to the RBI terminal of the CD4033B in the next-lower significant position in the display. This procedure is continued for each succeeding CD4033B on the integer side of the display.

On the fraction side of the display the RBI of the CD4033B associated with the least significant bit is connected to a low-level voltage and the RBO of that CD4033B is connected to the RBI terminal of the CD4033B in the next more-significant-bit position. Again, this procedure is continued for all CD4033B's on the fraction side of the display.

In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the RBI of that stage to a high level voltage (instead of to the RBO of the next more-significant-stage). For example: optional zero → 0.7346. Likewise, the zero in a number such as 763.0 can be displayed by connecting the RBI of the CD4033B associated with it to a high-level voltage.

Ripple blanking of non-significant zeros provides an appreciable savings in display power.

The CD4033B has a LAMP TEST input which, when connected to a high-level voltage, overrides normal decoder operation and enables a check to be made on possible display malfunctions by putting the seven outputs in the high state.

The CD4026B- and CD4033B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

CD4026B, CD4033B Types

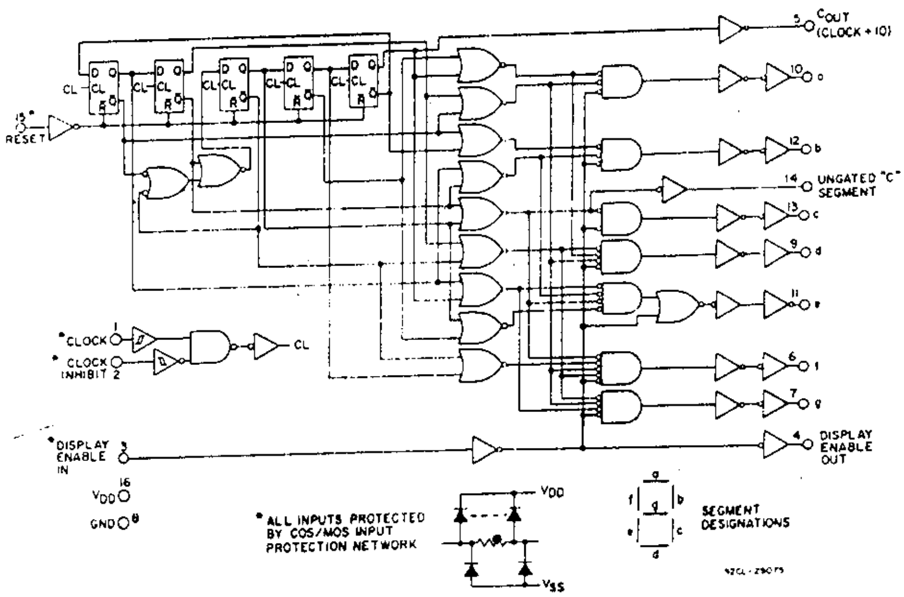


Fig. 1 – CD4026B logic diagram.

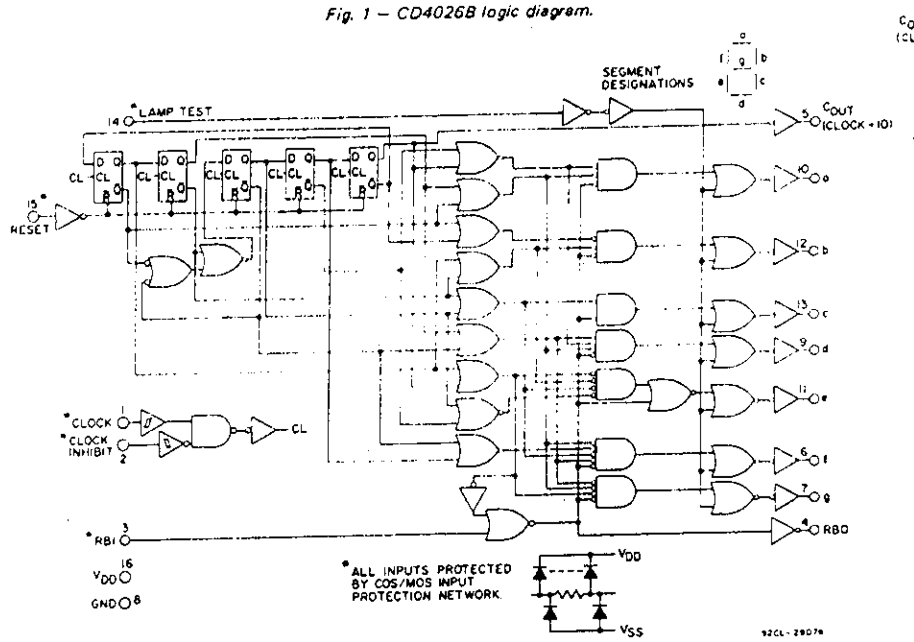


Fig. 2 – CD4033B logic diagram.

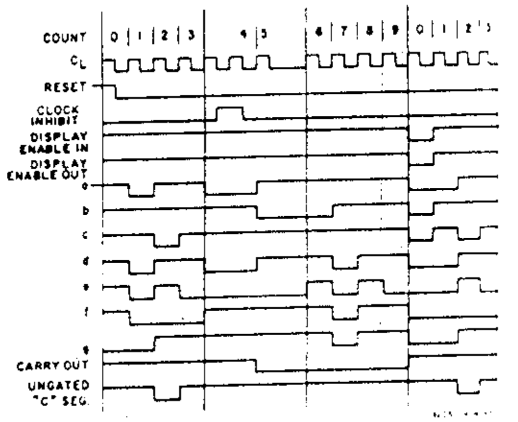


Fig. 3 – CD4026B timing diagram.

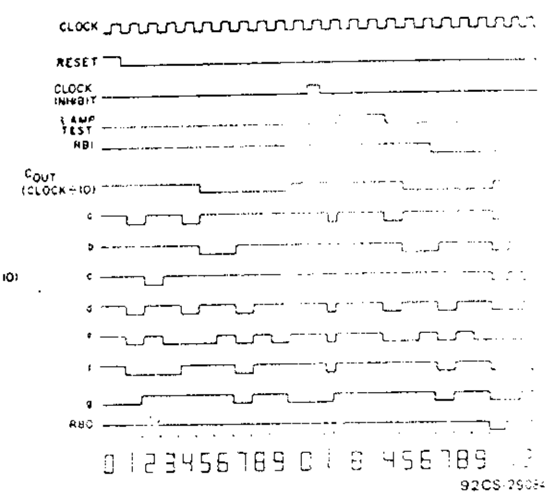


Fig. 4 – CD4033B timing diagram.

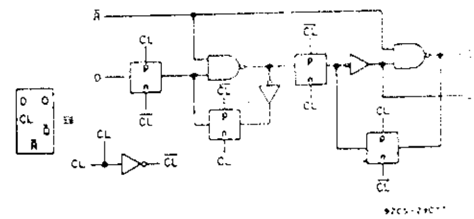


Fig. 5 – Detail of typical flip-flop stage for both types.

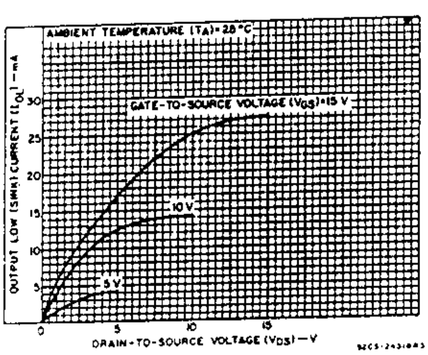


Fig. 6 – Typical n-channel output low (sink) current characteristics.

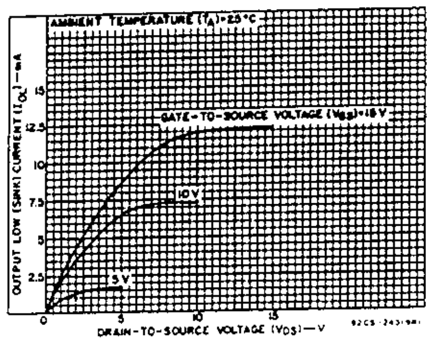


Fig. 7 – Minimum n-channel output low (sink) current characteristics.

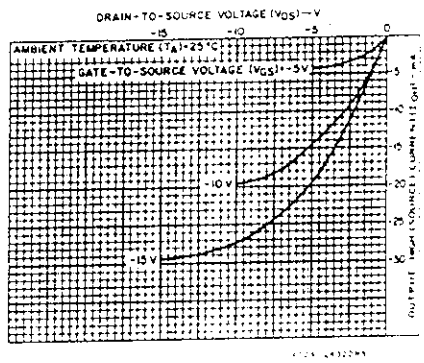


Fig. 8 – Typical p-channel output high (source) current characteristics.

NAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ*

ARACTERISTIC		TEST CONDITIONS	V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
OCKED OPERATION							
›pagation Delay Time; Carry-Out Line	t_{PLH}, t_{PHL}		5	–	250	500	ns
			10	–	100	200	
			15	–	75	150	
Decode Outlines			5	–	350	700	
			10	–	125	250	
			15	–	90	180	
·ansition Time; Carry-Out Line	t_{THL}, t_{TLH}		5	–	100	200	
			10	–	50	100	
			15	–	25	50	
·aximum Clock Input Frequency,	f_{CL}▲		5	2.5	5	–	MHz
			10	5.5	11	–	
			15	8	16	–	
lin. Clock Pulse Width,	t_W		5	–	110	220	ns
			10	–	50	100	
			15	–	40	80	
›lock and Clock Inhibit Rise or Fall Time;	t_{rCL}, t_{fCL}		5	Unlimited			ns
			10				
			15				
Average Input Capacitance, C_{IN}		Any Input		–	5	7	pF
RESET OPERATION							
Propagation Delay Time; To Carry-Out Line,	t_{PLH}		5	–	275	550	ns
			10	–	120	240	
			15	–	80	160	
To Decode Out Lines,	t_{PHL}, t_{PLH}		5	–	300	600	
			10	–	125	250	
			15	–	90	180	
Min. Reset Pulse Width,	t_W		5	–	100	120	
			10	–	50	100	
			15	–	25	50	
Min. Reset Removal Time			5	–	0	30	
			10	–	0	15	
			15	–	0	10	

▲ Measured with respect to carry-out line.

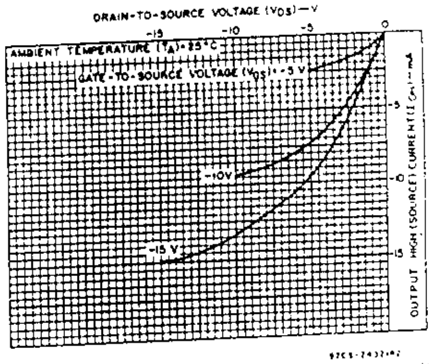


Fig. 9 – Minimum p-channel output high (source) current characteristics.

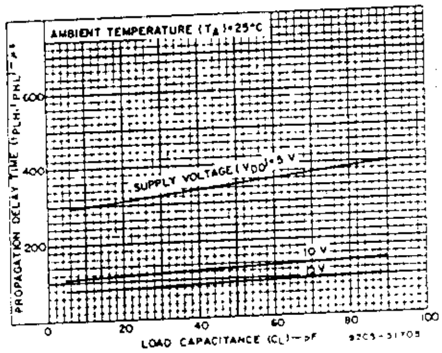


Fig. 10 – Typical propagation delay time as a function of load capacitance for decoded outputs.

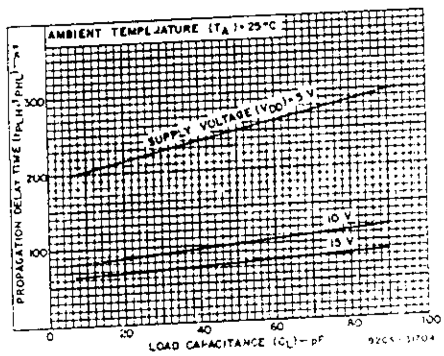


Fig. 11 – Typical propagation delay time as a function of load capacitance for carry-out outputs.

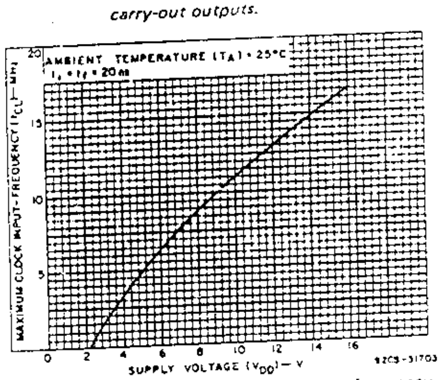


Fig. 12 – Typical maximum clock input-frequency as a function of supply voltage.

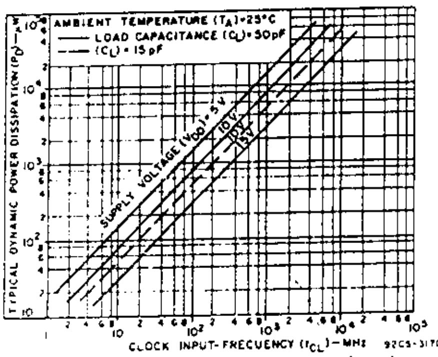


Fig. 13 – Typical power dissipation as a function of clock input frequency.

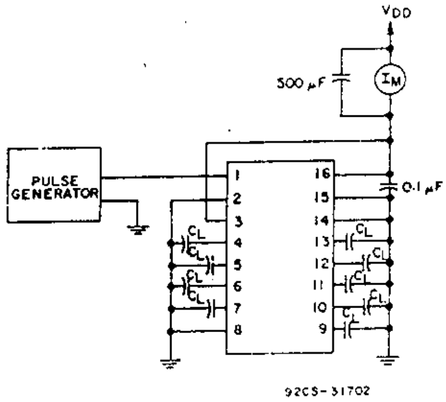


Fig. 14 – Dynamic power dissipation test circuit for CD4033B.

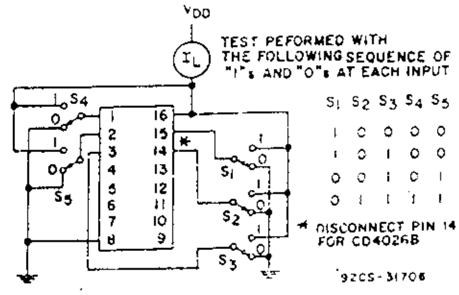


Fig. 15 – Quiescent device current.

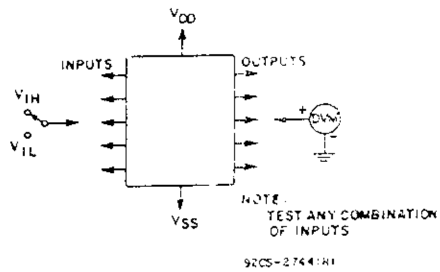
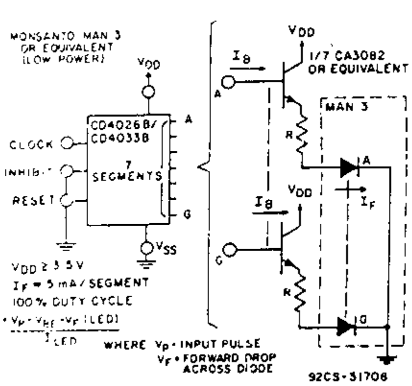
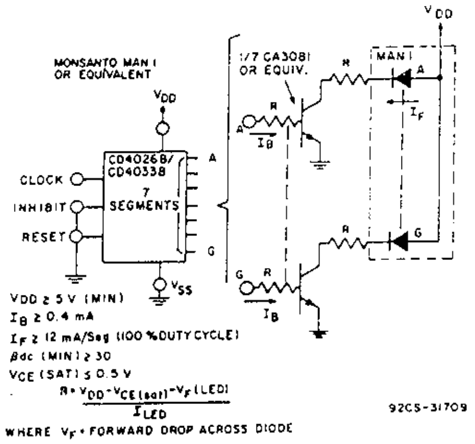


Fig. 16 – Input voltage.

INTERFACING THE CD4026B AND CD4033B WITH COMMERCIALLY AVAILABLE LIGHT EMITTING DIODE DISPLAYS





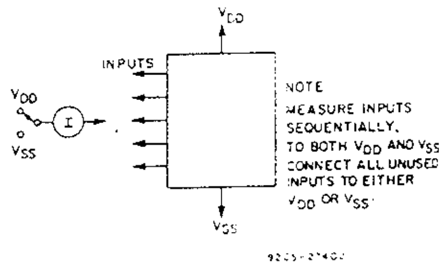
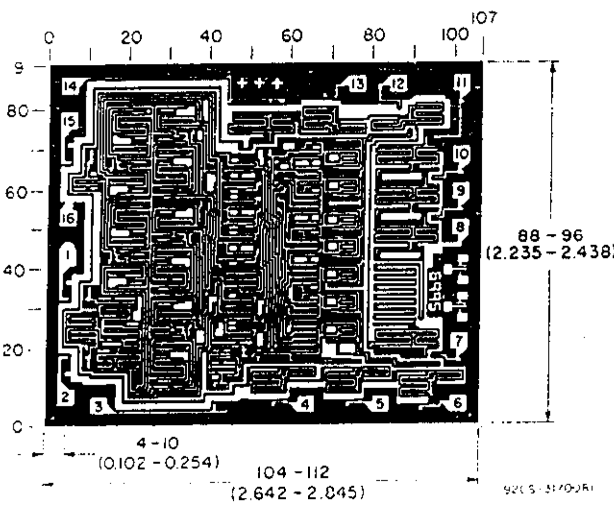
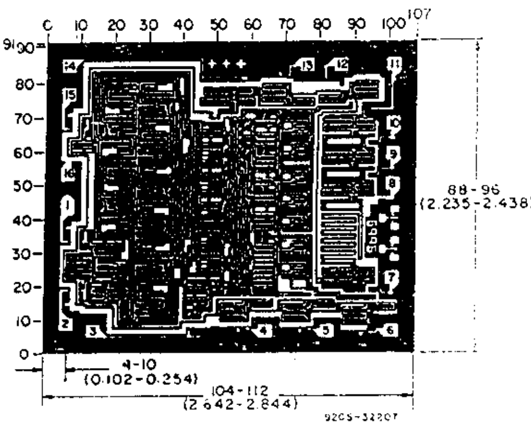


Fig. 17 – Input current.



Dimensions and pad layout for CD4026B.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

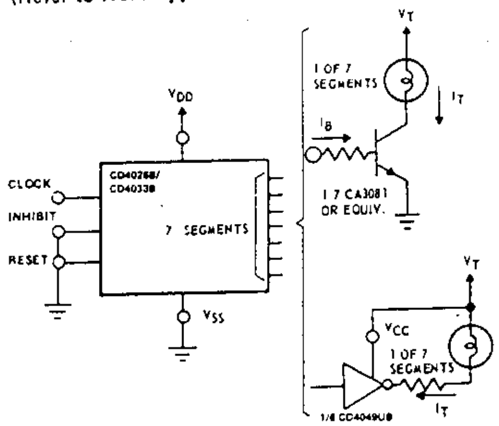


Dimensions and pad layout for CD4033B.

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.

INTERFACING THE CD4026B AND CD4033B WITH COMMERCIALLY AVAILABLE 7-SEGMENT DISPLAY DEVICES*

(Refer to RCA Application Note ICAN-6733 for detailed interfacing information)



INCANDESCENT READOUTS

RCA Numitron DR2000 Series

TUBE REQUIREMENTS

V_T = 3.5-5V

I_T = 24 mA Segment

ASSUMED TRANSISTOR CHARACTERISTICS

β_{dc} (min.) ≥ 25

V_{CE}(sat.) ≤ 0.5 V

V_{DD} = 8 V (min.)

I_B = 1mA (min.)

I_T = 24 mA (min.)

CD4049UB

@ V_{CC} = 10 V (min.)

V_o "0" ≤ 2 V

I_T = 8 mA (min.)

V_T ≈ 3.5 V TO 6 V

CD4049UB

@ V_{CC} = 10 V (min.)

V_o "0" ≤ 0.6 V

I_T = 8 mA (min.)

@ V_{CC} = 6 V (min.)

V_o "0" ≤ 1 V

I_T = 5 mA (min.)

V_T ≈ 1.5 V TO 3.5 V

LOW-POWER INCANDESCENT READOUTS

PINLITES INC-Series O and R

TUBE REQUIREMENTS	V_T(V)	mA/Segment
0-03-15	1.5	8
0-04-30	3	8
0-06-30	3	8
R-R3-20	2	4.3
R-R4-30	3	4.3

ASSUMED TRANSISTOR CHARACTERISTICS

β_{dc} (min.) ≥ 30

V_{CE}(sat.) ≤ 0.5V

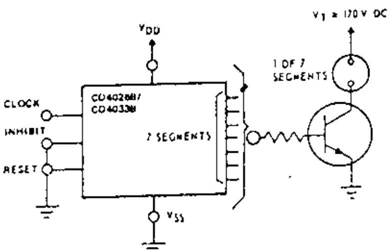
V_{CC} ≥ 3.5 V (min.)

I_B ≥ 0.25 mA (min.)

I_T ≤ 7.5 mA (min.)

92CM-31707

* The interfacing buffers shown, while a necessity with the CD4026A and CD4033A, are not required when using the "B" devices; the "B" outputs (≈ 10 times the "A" outputs) can drive most display devices directly especially at voltages above 10 V.



NEON READOUT (NIXIE TUBE▲)

1. Alco Electronics – MG19
2. Burroughs – B5971, B7971, B8971

TUBE REQUIREMENTS	V_T(Vdc)	mA Segment
Alco MG19	180	0.5
Burroughs B5971	170	3
Burroughs B7971, B8971	170	6

▲ (Trademark) Burroughs Corp.

TRANSISTOR CHARACTERISTICS

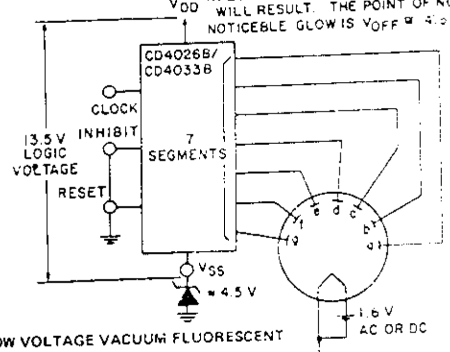
Leakage with transistor cutoff – 0.05 mA

$V_{(BR)CER}$ . . . . . . > V_T

β_{dc} (min.) ≥ 30

92CS-31710

WITH V_{ON} = 18 V MEDIUM BRIGHTNESS IN LOW AMBIENT LIGHT BACKGROUND WILL RESULT. THE POINT OF NO NOTICEBLE GLOW IS V_{OFF} ≈ 4.5 V



LOW VOLTAGE VACUUM FLUORESCENT READOUTS

1. Tung-Sol DIGIVAC S/G ‡ Type DT1704A or DT1705C
2. Nippon Electric (NEC): Type DG12E or LD915

TUBE REQUIREMENTS: 100 to 300 μA/segment at tube voltages of 12 V to 25 V depending on required brightness Filament requirement 45 mA at 1.6 V, ac or dc.

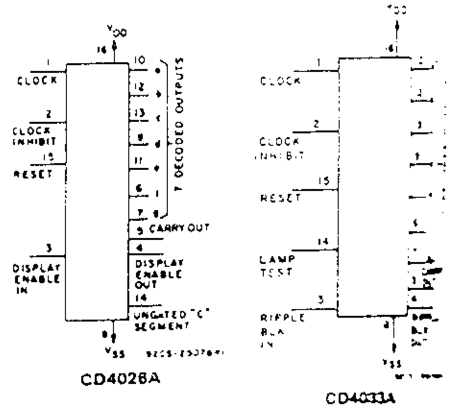
‡ (Trademark) Wagner Electric Co

92CS-31711

CD4026A, CD4033A Types

CMOS Decade Counters/Dividers

With Decoded 7-Segment Display Outputs and:
Display Enable – CD4026A
Ripple Blanking – CD4033A



FUNCTIONAL DIAGRAMS

The RCA–CD4026A and CD4033A each consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson code to a 7-segment decoded output for driving each stage in a numerical display.

These devices are particularly advantageous in display applications where low power dissipation and/or low package count are important.

Inputs common to both types are CLOCK, RESET, & CLOCK INHIBIT; common outputs are CARRY OUT and the seven decoded outputs (a, b, c, d, e, f, g). Additional inputs and outputs for the CD4026A include DISPLAY ENABLE input and DISPLAY ENABLE and UNGATED "C-SEGMENT" outputs. Signals peculiar to the CD4033 are RIPPLE-BLANKING INPUT and LAMP TEST INPUT and a RIPPLE-BLANKING OUTPUT.

A high RESET signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. The CLOCK INHIBIT signal can be used as a negative-edge clock if the clock line is held high. Antilock gating is provided on the Johnson counter, thus assuring proper counting sequence. The CARRY-OUT (C_{out}) signal completes one cycle every ten CLOCK INPUT cycles and is used to clock the succeeding decade directly in a multi-decade counting chain.

The seven decoded outputs (a, b, c, d, e, f, g) illuminate the proper segments in a seven segment display device used for representing the decimal numbers 0 to 9. The 7-segment outputs go high on selection in the CD4033A; in the CD4026A theses outputs go high only when the DISPLAY ENABLE IN is high.

CD4026A

When the DISPLAY ENABLE IN is low the seven decoded outputs are forced low regardless of the state of the counter. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display-character multiplexing.

The CARRY OUT and UNGATED"C-SEGMENT" signals are not gated by the DISPLAY ENABLE and therefore are available continuously. This feature is a requirement in implementation of certain divider functions such as divide-by-60 and divide-by-12.

CD4033A

The CD4033A has provisions for automatic blanking of the non-significant zeros in a multi-digit decimal number which results in an easily readable display consistent with normal writing practice. For example, the number 0050.07000 in an eight digit display would be displayed as 50.07. Zero suppression on the integer side is obtained by connecting the RBI terminal of the CD4033A associated with the most significant digit in the display to a low-level voltage and connecting the RBO terminal of that stage to the RBI terminal of the CD4033A in the next-lower significant position in the display. This procedure is continued for each succeeding CD4033A on the integer side of the display.

On the fraction side of the display the RBI of the CD4033A associated with the least significant bit is connected to a low level voltage and the RBO of that CD4033A is connected to the RBI terminal of the CD4033A in the next more-significant-bit position. Again, this procedure is continued for all CD4033A's on the fraction side of the display.

In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the RBI of that stage to a high level voltage(instead of to the RBO of the next more-significant-stage). For Example: optional zero → 0.7346.

Likewise, the zero in a number such as 763.0 can be displayed by connecting the RBI of the CD4033A associated with it to a high-level voltage.

Ripple blanking of non-significant zeros provides an appreciable savings in display power.

The CD4033A has a LAMP TEST input which, when connected to a high-level voltage, overrides normal decoder operation and enables a check to be made on possible display malfunctions by putting the seven outputs in the high state.

Features:

- Counter and 7-segment decoding in one package
- Easily interfaced with 7-segment display types
- Fully static counter operation: DC to 2.5 MHz (typ.)
- Ideal for low-power displays
- Display Enable Output (CD4026A)
- "Ripple Blanking" and Lamp Test (CD4033A)
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Decade counting/7-segment decimal display
- Frequency division/7-segment decimal displays
- Clock/watches/timers (e.g. ÷ 60, ÷ 60, ÷ 12 counter/display)
- Counter/display driver for meter applications

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg})	−65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
(Voltages referenced to V_{SS} Terminal):	−0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)	
FOR T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max	+265°C

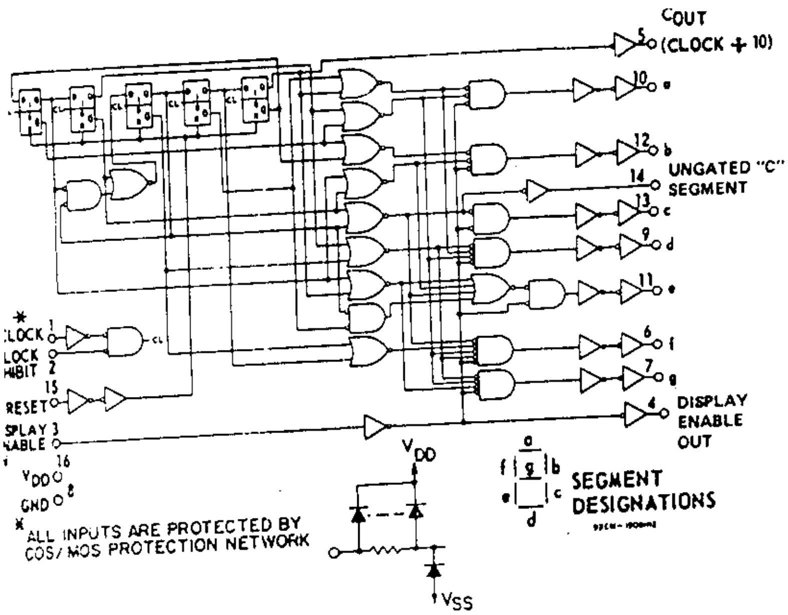


Fig. 1 – CD4026A logic diagram.

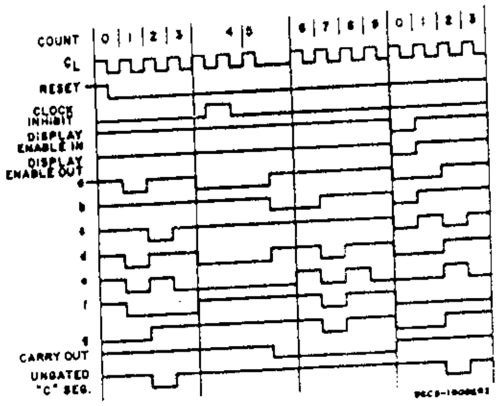


Fig. 2 – CD4026A timing diagram.

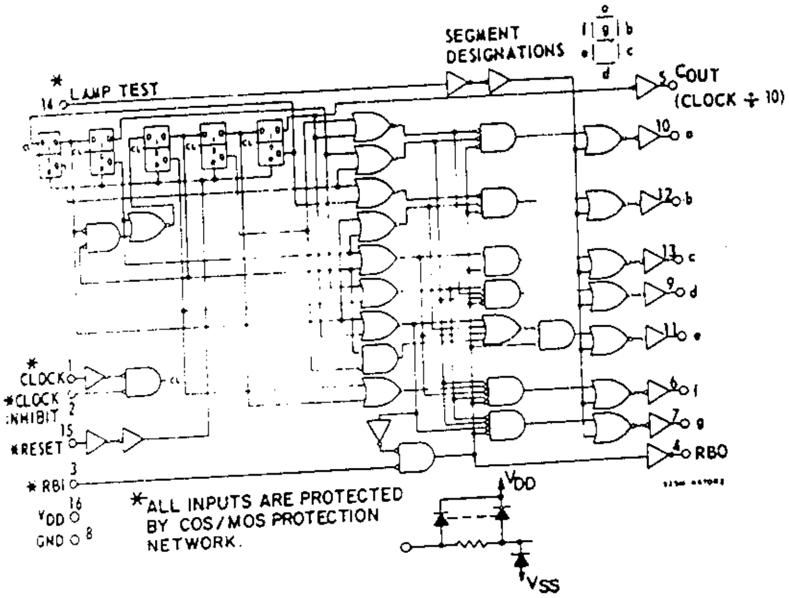


Fig. 3 – CD4033A logic diagram.

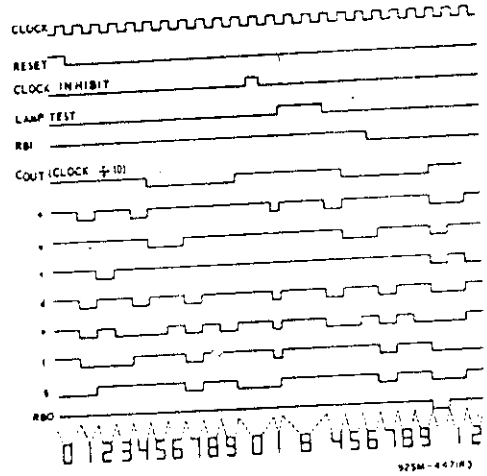


Fig. 4 – CD4033A timing diagram.

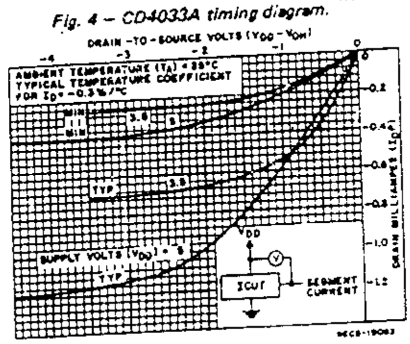


Fig. 5 – Minimum and typical output p-channel decoded drain characteristics @ V_{DD}=3.5 & 5 V.

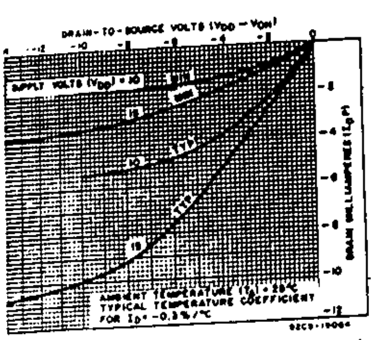


Fig. 6 – Minimum and typical output p-channel decoded drain characteristics @ V_{DD}=10 & 15 V.

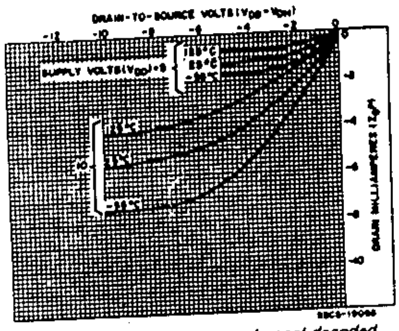


Fig. 7 – Typical output p-channel decoded drain characteristics as a function of temperature.

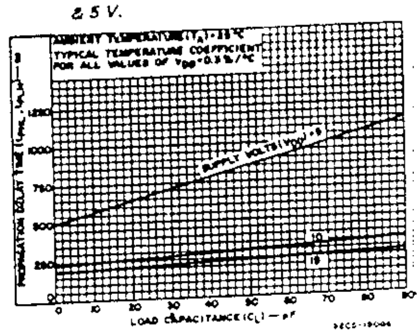


Fig. 8 – Typical propagation delay time vs. C_L for decoded outputs.

CD4026A, CD4033A Types

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS D, F, K, H Packages Min.	D, F, K, H Packages Max.	E Package Min.	E Package Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Clock Inhibit Setup Time, t_S	5 10	500 200	– –	700 300	– –	ns
Clock Pulse Width, t_W	5 10	330 170	– –	500 250	– –	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1.5 3	dc dc	1 2	MHz
Clock Rise or Fall Time, t_rCL, t_fCL	5 10	– –	15 15	– –	15 15	µs
Reset Pulse Width, t_W	5 10	330 165	– –	550 250	– –	ns
Reset Removal Time	5 10	750 225	– –	1000 275	– –	ns

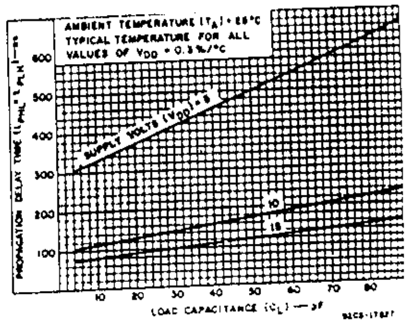


Fig. 9 – Typical propagation delay time vs. C_L for carry outputs.

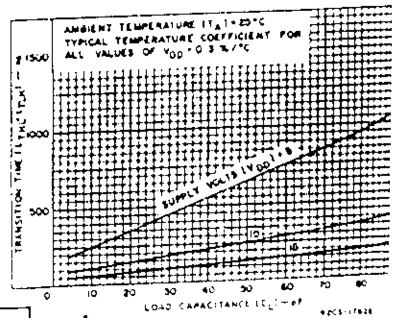


Fig. 10 – Typical transition time vs. C_L for decoded outputs.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions V_O (V)	V_{IN} (V)	V_{DD} (V)	D, F, K, H Packages –55	+25 Typ.	+25 Limit	+125	E Package –40	+25 Typ.	+25 Limit	+85	Units
Quiescent Device Current I_L Max.	–	–	5	5	0.3	5	300	50	0.5	50	700	µA
	–	–	10	10	0.5	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level, V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}		–	5	1.5 Min.; 2.25 Typ.								V
		–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}		–	5	1.5 Min.; 2.25 Typ.								
			10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current n-Channel (Sink), I_DN Min. — Decoded Outputs	0.5	–	5	0.15	0.24	0.12	0.09	0.08	0.24	0.06	0.05	mA
	0.5	–	10	0.32	0.5	0.25	0.18	0.15	0.5	0.12	0.1	
Carry Output	0.5	–	5	0.12	0.4	0.15	0.1	0.095	0.4	0.08	0.06	
	0.5	–	10	0.45	1	0.35	0.25	0.3	1	0.25	0.2	
p-Channel (Source), I_DP Min. — Decoded Outputs	4.5	–	5	-0.21	-0.28	-0.14	-0.1	-0.09	-0.28	-0.07	-0.06	
	9.5	–	10	-0.45	-0.6	-0.3	-0.22	-0.2	-0.6	-0.15	-0.13	
Carry Output	4.5	–	5	-0.12	-0.4	-0.15	-0.1	-0.095	-0.4	-0.08	-0.06	
	9.5	–	10	-0.45	-1	-0.35	-0.25	-0.3	-1	-0.24	-0.2	
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	±10^{-5} Typ., ±1 Max.								µA

...MIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ C$, Input $t_r, t_f = 20$ ns, $C_L = 15$ pF, $R_L = 200$ kΩ

...ARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS D, F, K, H Packages Min.	Typ.	Max.	E Package Min.	Typ.	Max.	UNITS
...CKED OPERATION								
...agation Delay Time; ...t_{PHL} ...ry Out Line	5	–	350	1000	–	350	1300	ns
	10	–	125	250	–	125	300	
...code Out Lines	5	–	600	1700	–	600	2200	ns
	10	–	250	500	–	250	700	
...nsition Time; ...L, t_{TLH} ...rry Out Line	5	–	100	300	–	100	350	ns
	10	–	50	150	–	50	200	
...ecode Out Lines	5	–	300	900	–	300	1200	ns
	10	–	125	350	–	125	450	
...ximum Clock Input ...requency, f_{CL}▲	5	1.5	2.5	–	1	2.5	–	MHz
	10	3	5	–	2	5	–	
...n. Clock Pulse Width, ...W	5	–	200	330	–	200	500	ns
	10	–	100	170	–	100	250	
...ck Rise & Fall Time; ...t_{rCL}, t_{fCL}	5	–	–	15	–	–	15	µs
	10	–	–	15	–	–	15	
...n. Clock Inhibit Set ...Time, t_S	5	–	175	500	–	175	700	ns
	10	–	75	200	–	75	300	
...erage Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF
...ESET OPERATION								
...ropagation Delay Time: ...t_{PLH}, t_{PHL} To Carry Out Line	5	–	350	1000	–	350	1300	ns
	10	–	125	250	–	125	300	
To Decode Out Lines	5	–	550	1400	–	550	1900	ns
	10	–	240	500	–	240	600	
Min. Reset Pulse Width ...W	5	–	200	330	–	200	500	ns
	10	–	100	165	–	100	250	
Min. Reset Removal Time	5	–	300	750	–	300	1000	ns
	10	–	100	225	–	100	275	

▲ Measured with respect to carry out line.

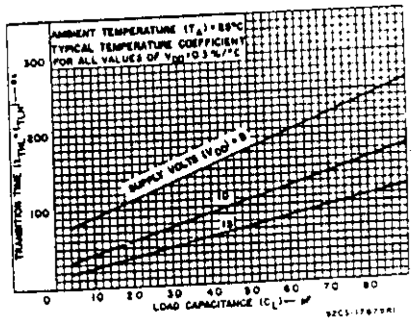


Fig. 11 – Typical transition time vs. C_L for carry output.

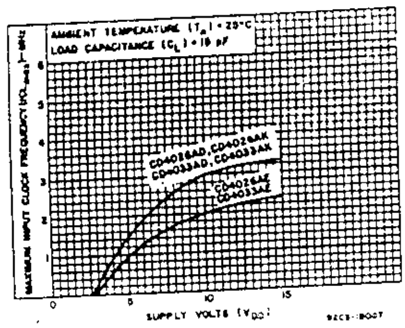


Fig. 12 – Maximum input clock frequency vs. V_{DD}.

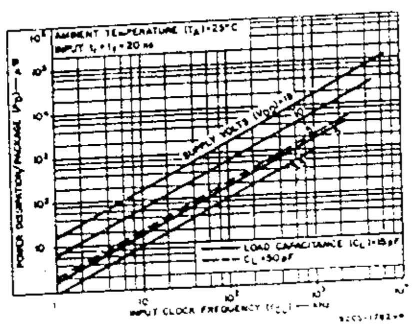


Fig. 13 – Typical dissipation characteristics.

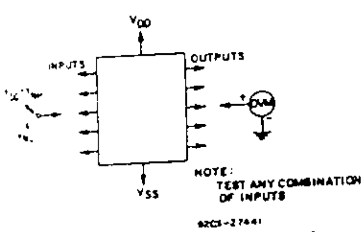


Fig. 14 – Noise immunity test circuit.

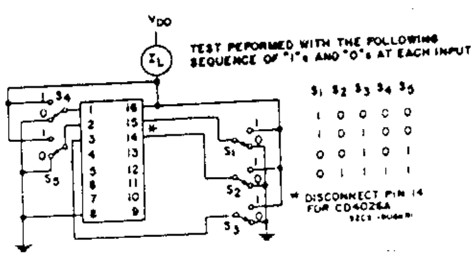


Fig. 15 – Quiescent-device-current test circuit.

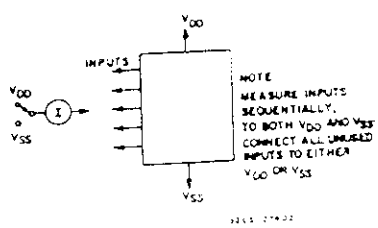


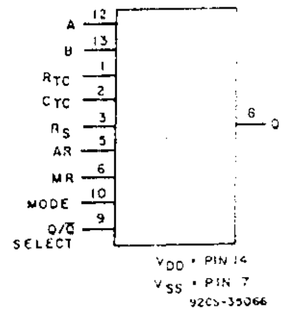
Fig. 16 – Input-leakage-current test circuit.

CMOS Programmable Timer

High-Voltage Types (20-Volt Rating)

Features:

- *Low symmetrical output resistance, typically 100Ω at V_{DD} = 15 V*
- *Built-in low-power RC oscillator*
- *Oscillator frequency range: DC to 100 kHz*
- *External clock (applied to pin 3) can be used instead of oscillator*
- *Operates as 2^N frequency divider or as a single-transition timer*
- *Q/$\overline{Q}$ select provides output logic level flexibility*
- *AUTO or MASTER RESET disables oscillator during reset to reduce power dissipation*
- *Operates with very slow clock rise and fall times*



CD4541B
FUNCTIONAL DIAGRAM

- *Capable of driving six low power TTL loads, three low-power Schottky loads, or six HTL loads over the rated temperature range*
- *Symmetrical output characteristics*
- *100% tested for quiescent current at 20 V*
- *5-V, 10-V, and 15-V parametric ratings*
- *Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"*

The RCA-CD4541B programmable timer consists of a 16-stage binary counter, an oscillator that is controlled by external R-C components (2 resistors and a capacitor), an automatic power-on reset circuit, and output control logic. The counter increments on positive-edge clock transitions and can also be reset via the MASTER RESET input.

The output from this timer is the Q or $\overline{Q}$ output from the 8th, 10th, 13th, or 16th counter stage. The desired stage is chosen using time-select inputs A and B (see frequency select table). The output is available in either of two modes selectable via the MODE input, pin 10 (see truth table). When this MODE input is a logic "1", the output will be a continuous square wave having a frequency equal to the oscillator frequency divided by 2^N. With the MODE input set to logic "0" and after a MASTER RESET is initiated, the output (assuming Q output has been selected) changes from a low to a high state after 2^{N-1} counts and remains in that state until another MASTER RESET pulse is applied or the MODE input is set to a logic "1".

Timing is initialized by setting the AUTO RESET input (pin 5) to logic "0" and turning power on. If pin 5 is set to logic "1", the AUTO RESET circuit is disabled and counting will not start until after a positive MASTER RESET pulse is applied and returns to a low level. The AUTO RESET consumes an appreciable amount of power and should not be used if low-power operation is desired.

The RC oscillator, shown in Fig. 2, oscillates with a frequency determined by the R-C network and is calculated using:

$$f = \frac{1}{2.3\, R_{TC} C_{TC}}$$

where f is between 1 kHz and 100 kHz and $R_S \geq 10$ kΩ and $\approx 2R_{TC}$

The CD4541B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

FREQUENCY SELECTION TABLE

A	B	No. of Stages N	Count 2^N
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

TRUTH TABLE

PIN	STATE 0	STATE 1
5	Auto Reset On	Auto Reset Disable
6	Master Reset Off	Master Reset On
9	Output Initially Low After Reset (Q)	Output Initially High After Reset ($\overline{Q}$)
10	Single Transition Mode	Recycle Mode

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) .... −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS .... −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT .... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60° C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) .... Derate Linearly at 12 mW/° C to 200 mW
For T_A = −55 to +100° C (PACKAGE TYPES D, F) .... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPES D, F) .... Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) .... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H .... −55 to +125° C
PACKAGE TYPE E .... −40 to +85° C
STORAGE TEMPERATURE RANGE (T_{stg}) .... −65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. .... +265° C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS MIN.	LIMITS TYP.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	—	3	18	V

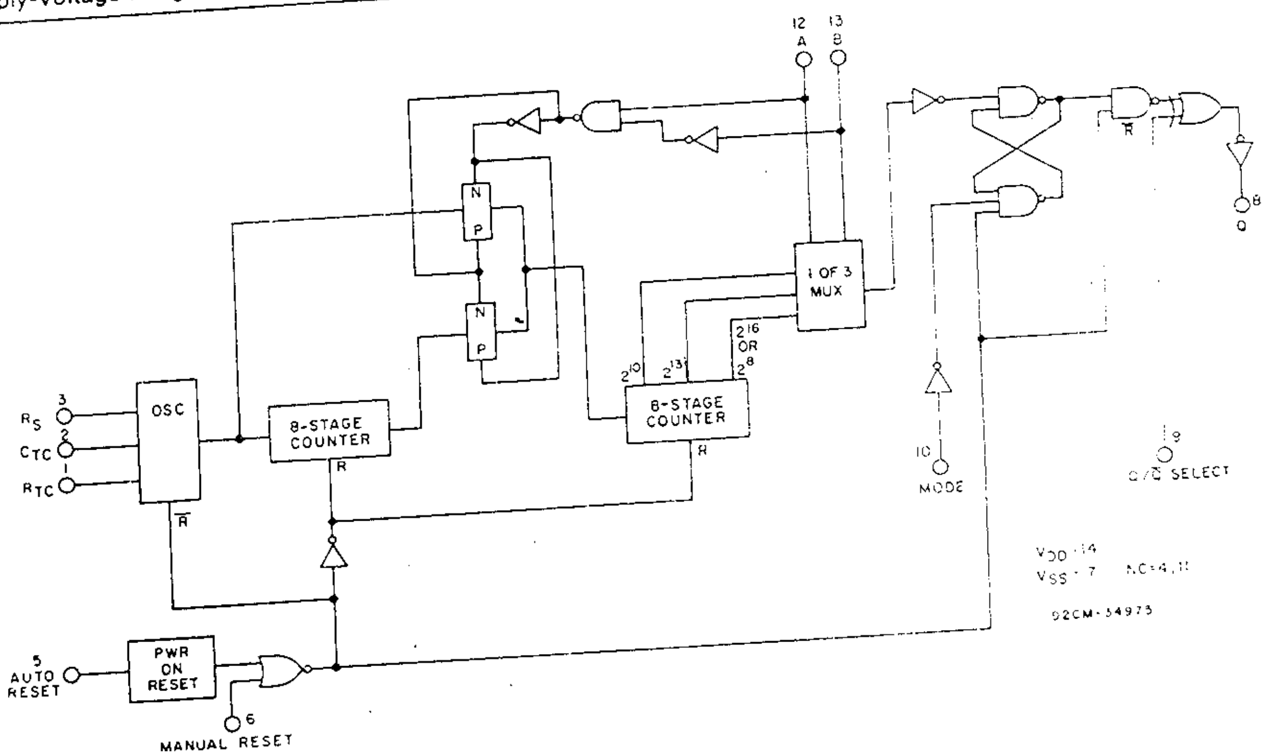
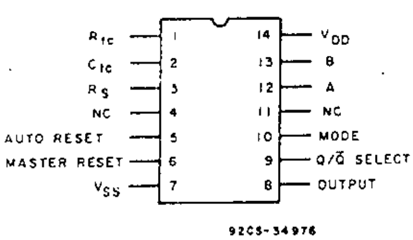


Fig. 1 — CD4541B functional diagram.

CD4541B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D, F, H Packages Values at -40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	+25 MIN.	+25 TYP.	+25 MAX.	
Quiescent Device Current, I_{DD} Max.	—	0,5	5	5	5	150	150	—	0.04	5	µA
	—	0,10	10	10	10	300	300	—	0.04	10	
	—	0,15	15	20	20	600	600	—	0.04	20	
	—	0,20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	1.9	1.85	1.26	1.08	1.55	3.1	—	mA
	0.5	0,10	10	5	4.8	3.3	2.8	4	8	—	
	1.5	0,15	15	12.6	12	8.4	7.2	10	20	—	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−1.9	−1.85	−1.26	−1.08	−1.55	−3.1	—	
	2.5	0,5	5	−6.2	−6	−4.1	−3	−5	−10	—	
	9.5	0,10	10	−5	−4.8	−3.3	−2.8	−4	−8	—	
	13.5	0,15	15	−12.6	−12	−8.4	−7.2	−10	−20	—	
Output Voltage: Low-Level, V_{OL} Max.	—	0,5	5	—	0.05			—	0	0.05	V
	—	0,10	10	—	0.05			—	0	0.05	
	—	0,15	15	—	0.05			—	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	—	0,5	5	—	4.95			4.95	5	—	
	—	0,10	10	—	9.95			9.95	10	—	
	—	0,15	15	—	14.95			14.95	15	—	
Input Low Voltage V_{IL} Max.	0.5, 4.5	—	5	—	1.5			—	—	1.5	V
	1,9	—	10	—	3			—	—	3	
	1.5,13.5	—	15	—	4			—	—	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	—	5	—	3.5			3.5	—	—	
	1,9	—	10	—	7			7	—	—	
	1.5,13.5	—	15	—	11			11	—	—	
Input Current I_{IN} Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	$\pm10^{-5}$	±0.1	µA



TERMINAL ASSIGNMENT

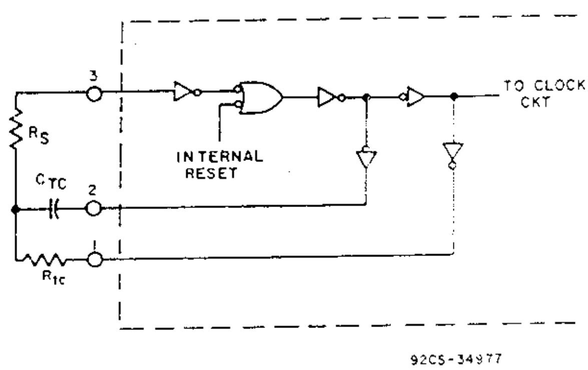
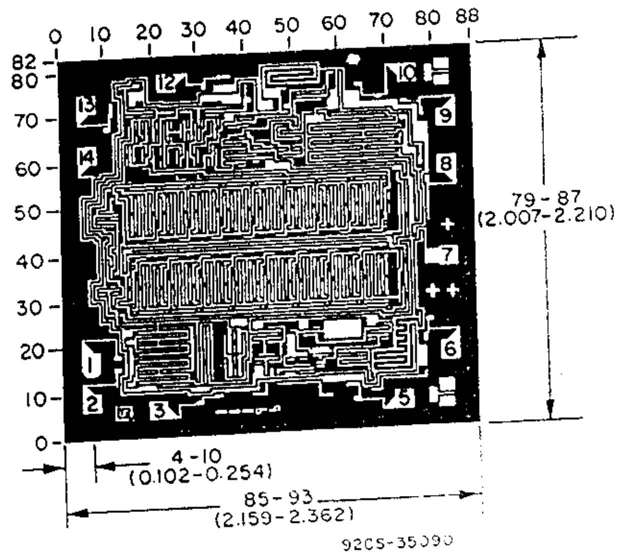


Fig. 2 — RC oscillator circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS, *at $T_A = 25°C$, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ*

CHARACTERISTIC		V_{DD} (V)	LIMITS MIN.	TYP.	MAX.	UNITS
Propagation Delay Times: Clock to Q	(2^8) t_{PHL}, t_{PLH}	5	—	3.5	10.5	μs
		10	—	1.25	3.8	
		15	—	0.9	2.9	
	(2^{16}) t_{PHL}, t_{PLH}	5	—	6	18	μs
		10	—	3.5	10	
		15	—	2.5	7.5	
Transition Time,	t_{THL}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
	t_{TLH}	5	—	180	360	ns
		10	—	90	180	
		15	—	65	130	
MASTER RESET, CLOCK Pulse Width		5	900	300	—	ns
		10	300	100	—	
		15	225	85	—	
Maximum Clock Pulse Input Frequency,	f_{CL}	5	—	1.5	—	MHz
		10	—	4	—	
		15	—	6	—	
Maximum Clock Pulse Input Rise or Fall Time,	t_r, t_f	5,10,15		Unlimited		μs



Dimensions and pad layout for CD4541B

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to +16 mils applicable to the nominal dimensions shown.

DIGITAL TIMER APPLICATION

A positive pulse on MASTER RESET resets the counters and latch. The output goes high and remains high until the number of pulses, selected by A and B, are counted. This circuit is retriggerable and is as accurate as the input frequency. If additional accuracy is desired, an external clock can be used on pin 3. A set-up time equal to the width of the one-shot output is required immediately following initial power up, during which time the output will be high.

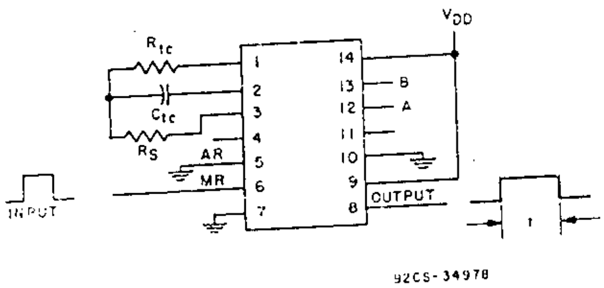


Fig. 3 - Digital timer application circuit.

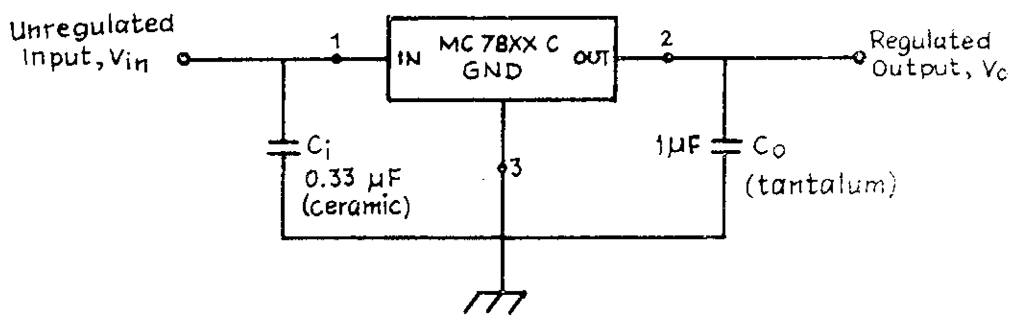
Fixed Voltage Series Regulator

78 XX series are three terminal, positive fixed voltage regulators. There are seven output voltage options available such as 5,6,8,12,15,18 and 24 V. in 78 XX, the last two numbers (XX) indicate the output voltage. Thus 7815 represents a 15 V regulator. There are also available 79 XX series of fixed output, negative voltage regulators which are complements to the 78 XX series devices. There are two extra voltage options of –2 *V* and –5.2 *V* available in 79 XX series. These regulators are available in two types of packages.

Metal package (TO – 3 type)

Plastic package (TO – 220 type)

Figure 6.2 shows the standard representation of monolithic voltage regulator. A capacitor C_i (0.33 μF) is usually connected between input terminal and ground to cancel the inductive effects due to long distribution leads. The output capacitor C_o (1 μF) improves the transient response.



Standard representation of a three terminal positive monolithic regulator

National Semiconductor also produce three terminal voltage regulators in LM series. There are three series available for different operating temperature ranges:

LM	100	series	–55°C	to	+125°C
LM	200	series	–25°C	to	+85°C
LM	300	series	0°C	to	+70°C

The popular series are LM 340 positive regulators and LM 320 negative regulators with output ratings comparable to 78 XX / 79 XX series.

Characteristics

There are four characteristics of three terminal IC regulators which must be mentioned.

Electrical characteristics of 7805 voltage regulator

Absolute Maximum Ratings

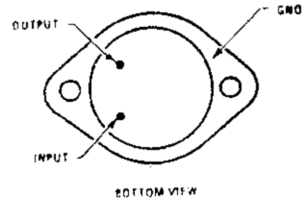
Input Voltage (5 V through 18 V)	35 V
(24 V)	40 V
Internal Power Dissipation	internally limited
Storage Temperature Range	−65°C to + 150°C
Operating Junction Temperature Range	
μA7800	− 55°C to + 150°C
μA7800C	0°C to + 125°C

7805C

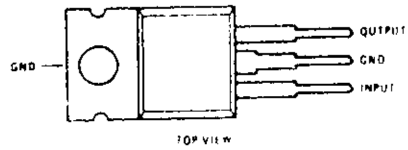
Electrical Characteristics V_{IN} = 10 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

Characteristic		Condition		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		4.8	5.0	5.2	V
Line Regulation		T_J = 25° C	7 V ≤ V_{IN} ≤ V		3	100	mV
			8 V ≤ V_{IN} ≤ 12 V		1	50	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		15	100	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		5	50	mV
Output voltage		7 V ≤ V_{IN} ≤ 20 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		4.75		5.25	V
Quiescent Current		T_J = 25°C			4.2	8.0	mA
Quiescent Current Change	with line	7 V ≤ V_{IN} ≤ 25 V				1.3	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			40		μV
Ripple Rejection		f = 120 Hz, 8 V ≤ V_{IN} ≤ 18 V		62	78		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			17		mΩ
Short-Circuit Current		T_J = 25°C, V_{IN} = 35 V			750		mA
Peak Output Current		T_J = 25°C			2.2		A
Average Temperature Coefficient of output voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 125°C			1.1		mV

Metal Can Package
Aluminum



Plastic Package



1. V_o : The regulated output voltage is fixed at a value as specified by the manufacturer. There are a number of models available for different output voltages, for example, 78 XX series has output voltage at 5, 6, 8 etc.
2. $|V_{in}| \geq |V_o| + 2$ volts : The unregulated input voltage must be atleast 2 V more than the regulated output voltage. For example, if $V_o = 5\ V$, then $V_{in} = 7\ V$.
3. $I_{(o)\ max}$: The load current may vary from 0 to rated maximum output current. The IC is usually provided with a heat sink, otherwise it may not provide the rated maximum output current.
4. Thermal shutdown : The IC has a temperature sensor (built-in) which turns off the IC when it becomes too hot (usually 125°C to 150°C). The output current will drop and remain there until the IC has cooled significantly.

Table 6.1 gives the electrical characteristics of 7805 voltage regulator and the connection diagram of packages available. Some of the important performance parameters listed in the data sheet are explained as follows :

Line / Input Regulation

It is defined as the percentage change in the output voltage for a change in the input voltage. It is usually expressed in millivolts or as a percentage of the output voltage. Typical value of line regulation from the data sheet of 7805 is 3 mV.

Load Regulation

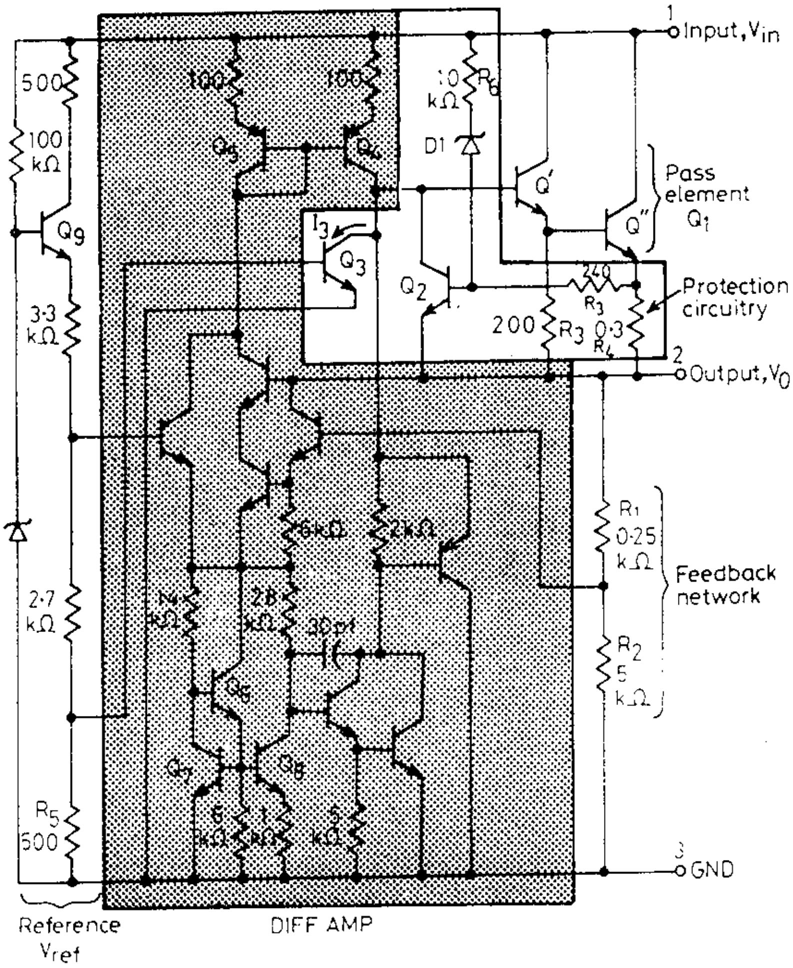
It is defined as the change in output voltage for a change in load current and is also expressed in millivolts or as a percentage of V_o. Typical value of load regulation for 7805 is 15 mV for 5 mA < I_o < 1.5 A.

Ripple Rejection

The IC regulator not only keeps the output voltage constant but also reduces the amount of ripple voltage. It is usually expressed in dB. Typical value for 7805 is 78 dB.

The Schematic diagram of MC 78 XXC* is shown in Fig. 6.3. The circuit consists of a reference voltage V_{ref}. This circuit basically consists of level shifter with zener diode input and the transistor Q_9 used as emitter follower buffer. The circuit enclosed in the shaded region is a difference amplifier consisting of a current mirror (Q_4, Q_5), and an active load (Q_6 Q_7 Q_8). The combination of $R_1 R_2$ forms the feedback network for sampling the output voltage. The sampled voltage is fed

*C stands for commercial use.



Schematic diagram for MC7800C series monolithic regulator

to one of the inputs of the difference amplifier. The Darlington pair Q' and Q'' forms series pass element Q_1 of the circuit shown in Fig. 6.1.

The monolithic regulator has in-built circuitry enclosed in the solid line to provide :

Over-current protection.

Thermal overload protection.

Current is limited by R_3, R_4 and transistor Q_2. If the output voltage goes low due to overload, the excess voltage appears across the pass element (Q' Q''), that is, across the collector emitter of Q''. When this voltage is more than the breakdown voltage of the zener diode D_1, it starts conducting. This provides sufficient base current to transistor Q_2 and drives it ***on***. Now, because of the collector current of Q_2 when fully ***on***, current flowing to the base of Q' is reduced. This in turn reduces the conduction of Q''. Thus the volt-ampere product of the pass element (Q' Q'') is limited.

The thermal overload protection is provided by the resistor R_5 and transistor

Q_3. The voltage drop across resistor R_5 is directly applied to the base-emitter of Q_3. When the temperature goes high, Q_3 conducts more, thereby reducing the base drive of $Q'Q''$ combination. This provides thermal protection.

Current Source

The three terminal fixed voltage regulator can be used as a current source. Figure 6.4 (a) shows the circuit where 7805 has been wired to supply a current of 1 ampere to a 10 Ω, 10 watt load.

$$I_L = I_R + I_Q \tag{6.2}$$

where I_Q is the quiescent current and is about 4.2 mA for 7805. (See Table 6.1)

$$I_L = \frac{V_R}{R} + I_Q \tag{6.3}$$

Since $I_L = 1\,A$, $$\frac{V_R}{R} \simeq 1A\ (I_Q \ll I_L) \tag{6.4}$$

Also $V_R = 5$ V (voltage between terminal 2 and 3)
So the value of R required is

$$R = 5\text{V}/1\text{A} = 5\Omega \tag{6.5}$$

Thus choose $R = 5$ Ω to deliver 1 A current to a load of 10 Ω.

Boosting IC Regulator Output Current

It is possible to boost the output current of a three terminal regulator simply by connecting an external pass transistor in parallel with the regulator as shown in Fig. 6.4 (b).

Let us now see how the circuit works. For low load currents, the voltage drop across R_1 is insufficient (< 0.7 V) to turn on transistor Q_1 and the regulator itself is able to supply the load current. However, as I_L increases, the voltage drop across R_1 increases. When this voltage drop is approximately 0.7 V, the transistor Q_1 turns on. It can be easily seen that if $I_L = 100$ mA, the voltage drop across R_1 is equal to 7Ω × 100 mA = 0.7 V. Thus, if I_L increases more than 100 mA, the transistor Q_1 turns on and supplies the extra current required. Since V_{EB} (ON) remains fairly constant, the excess current comes from Q_1's base after amplification by β. The regulator adjusts I_B so that

$$I_L = I_c + I_o \tag{6.6}$$

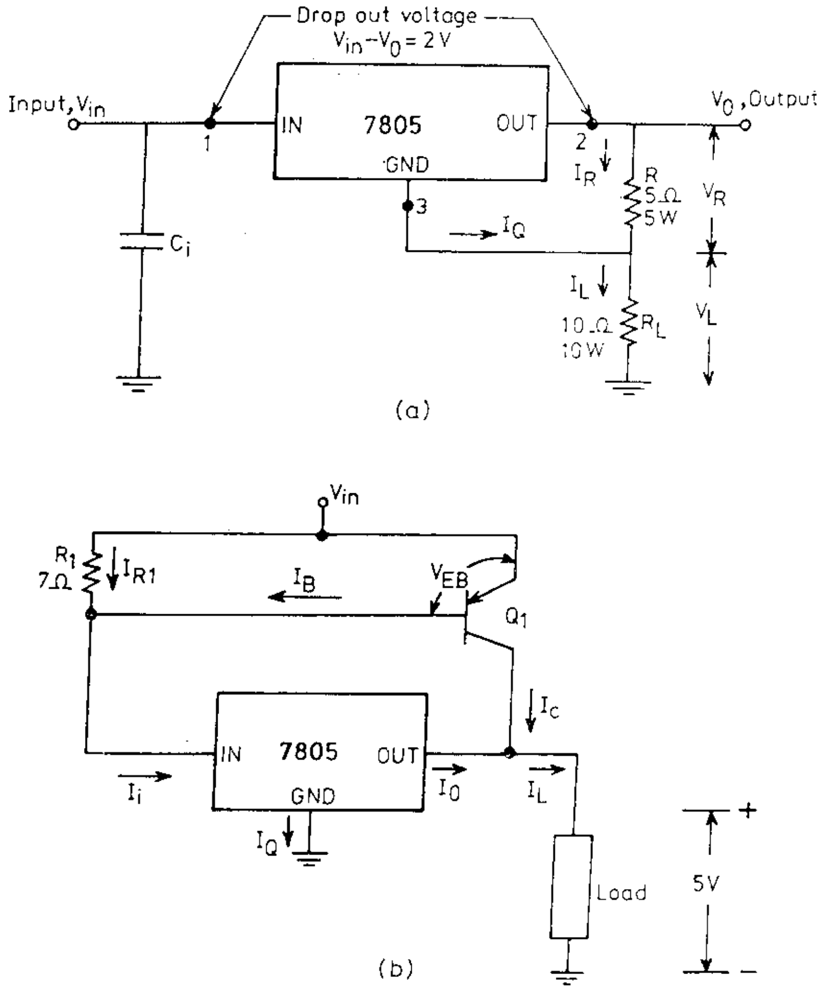


Fig. 6.4. (a) IC 7805 used as a current source (b) Boosting a three terminal regulator

and
$$I_c = \beta I_B \tag{6.7}$$

For the regulator,

$$I_o = I_i - I_Q$$
$$\simeq I_i \text{ (as } I_Q \text{ is small)} \tag{6.8}$$

Also
$$I_B = I_i - I_{R1}$$
$$\simeq I_o - \frac{V_{EB\,(ON)}}{R_1} \tag{6.9}$$

Simplifying we get

$$I_L = (\beta + 1) I_o - \beta \frac{V_{EB\,(ON)}}{R_1} \tag{6.10}$$

The maximum current $I_{o\,(max)}$ for a 7805 regulator is 1 A from the data sheet. Assuming $V_{EB\,(ON)}$ = 1 V and β = 15 we get from Eq. (6.10)

$$I_L = 16 \times 1 - 15 \times (1/7) = 13.8 \text{ A} \tag{6.11}$$

components required

SL.NO	PART DESCRIPTION	VALUE	QTY	REF.DESIGNATOR
1	RESISTOR	220E,1/4W,5%	1	R42
2	RESISTOR	330E,1/4W,5%	18	R15-R17,R24,R27-R40
3	RESISTOR	1K,1/4W,5%	4	R4,R20,R21,R19
4	RESISTOR	2K2,1/4W,5%	2	R7,R13
5	RESISTOR	4K7,1/4W,5%	4	R6,R9,R18,R41
6	RESISTOR	10K,1/4W,5%	8	R2 R3,R5,R12,R22,R23 R43,R44
7	RESISTOR	27K,1/4W,5%	4	R8,R10,R11,R25
8	RESISTOR	33K,1/4W,5%	1	R14
9	RESISTOR	39K,1/4W,5%	1	R25
10	RESISTOR	75K,1/4W,5%	1	R26
11	CAPACITOR	22PF DISC CERAMIC	2	C1,C13
12	CAPACITOR	1KPF DISC CERAMIC	2	C12,C17
13	CAPACITOR	10KPF DISC CERAMIC	1	C2
14	CAPACITOR	0.1UF DISC CERAMIC	6	C6,C7,C14,C15, C18,C19
15	CAPACITOR	0.1UF DISC CERAMIC	2	C20,C21
16	CAPACITOR	1UF DISC CERAMIC	4	C3-C5,C11
17	CAPACITOR	10UF DISC CERAMIC	2	C9,C10
18	CAPACITOR	100UF DISC CERAMIC	1	C16
19	CAPACITOR	1000UF DISC CERAMIC	1	C8
20	CAPACITOR	6UF DISC CERAMIC	2	C22
21	DIODE	1N400	2	D1,D2
22	DIODE	IN4148	5	D3,D9-D11,D4
23	TRANSISTOR	BC 547B	8	Q1-Q8
24	BT8401POS	POSITIONER IC	1	U5
25	CD 4033	COUNTER	2	U1,U2
26	CD4541	PROGRAMMABLE TIMER	1	U6
27	H21A1	SENSOR-OPTOCOUPLER	1	U7
28	7805TO220	REG 5V	1	U4
29	7812TO220	REG 12V	1	U3

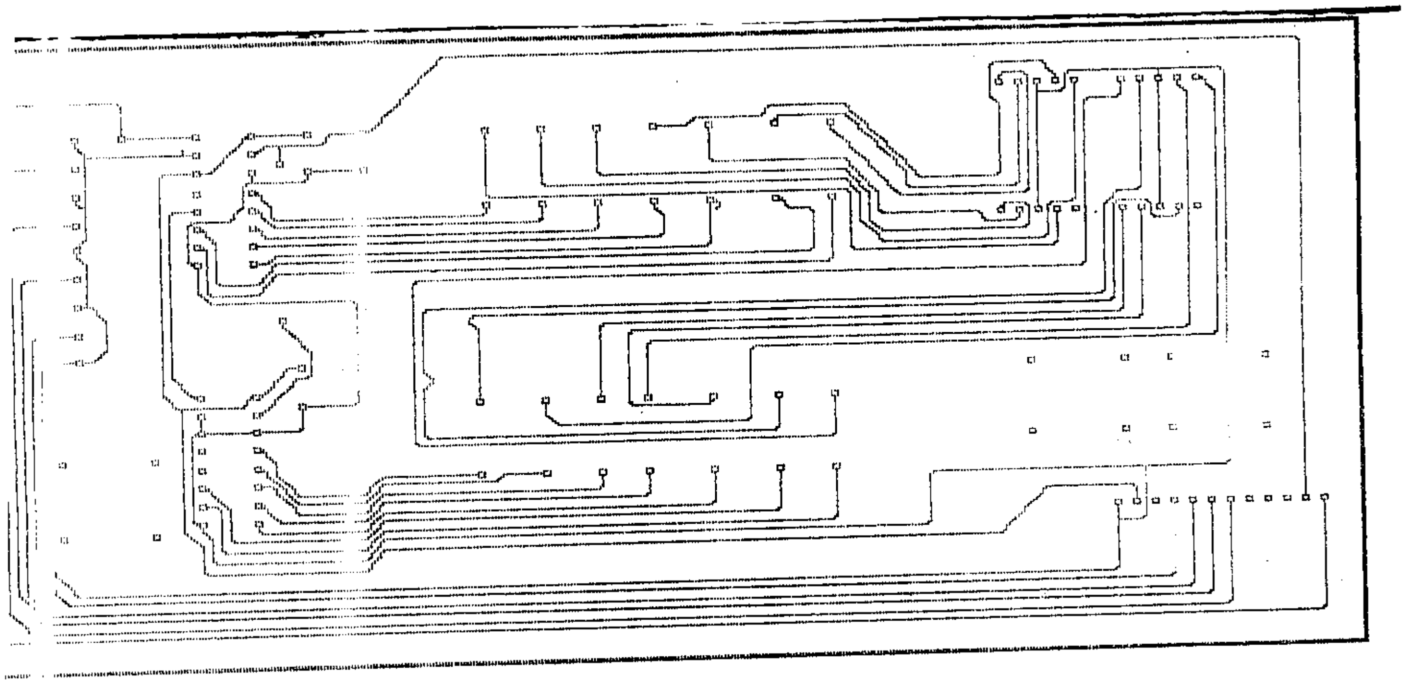
APPENDIX - B

PCB

Two single sided printed circuit boards and one general purpose board are used .

The PCB's consists of display section and control section & GPB consists of 555 timer Smartcopy software is used in designing PCB with std. dimensions for the components.

DISPLAY SECTION - PCB LAYOUT



CONTROL SECTION - PCB LAYOUT