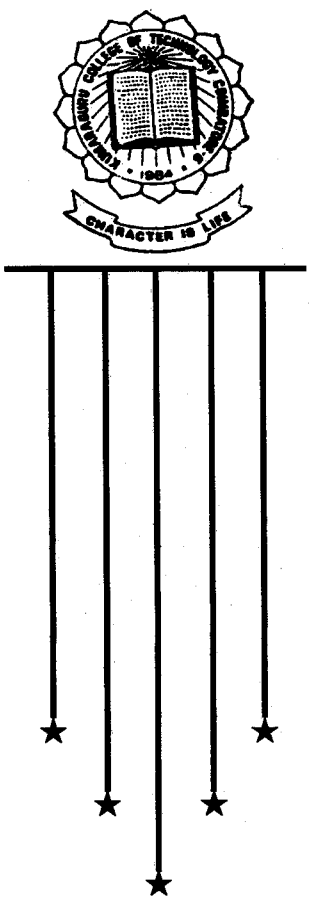
VOICE OPERATED TELEPHONE DIALER

PROJECT REPORT



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IN PARTIAL FULFILMENT OF THE REQUIREMENTS

FOR THE AWARD OF THE DEGREE OF

BACHELOR OF ENGINEERING IN

ELECTRONICS & COMMUNICATION ENGINEERING

OF THE BHARATHIAR UNIVERSITY, COIMBATORE.

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We would also like to thank all the teaching &non teaching staff who have helped us directly or indirectly to complete our project work.

CONTENTS

SYNOPSIS

As the world of technology moves into the new millenium we see the popularization of the various technologies that emerged in the past. The prominent one among them is the use of voice in controlling electronic devices. In the world of communication, telephone is one of the widely used electronic devices. The development of ***VOICE OPERATED TELEPHONE DIALER*** *is an attempt made by us to incorporate speech recognition into telephone instruments. Our objective is to make the instrument dial the number of a person when his or her name is spoken out. This project involves storage of name, recognition of name, storage of number, retrieval of number and dialing of number purely using solid state devices. The* ***VOICE DIRECT IC*** *by Sensory Inc. is being used for speech recognition. The commercialization of such an equipment in the immediate future will definitely be a great success.*

INTRODUCTION

Speech recognition is one of the latest technologies that is gaining popularity in the present digital world. In general speech recognition means the use of human voice in controlling the electronic devices. At present this technology is widely being used in computers as a means of communicating with the device. This is purely based on the software running in the system. Since it is not practical to have a full-fledged PC to control electronic devices, a speech recognition system purely based on solid state devices is a necessity. The development of ***VOICE OPERATED TELEPHONE DIALER*** *is an attempt to incorporate speech recognition into telephones purely using solid state devices.*

The speech recognition IC- VOICE DIRECT is made use of for doing the recognition part of the project. While training, the audio signal being fed into the IC is digitized and is being stored in a memory. A serial EEPROM is interfaced into the processor using I^2C bus architecture. The process of training and recognition is made easy by the use of user-friendly speech prompts.

The process of template generation is done using an advanced neural network engine embedded in the IC. The speaker verification is done by

comparing the stored template with that of the one being generated during the recognition period. The one template which matches with the stored one and having the predefined threshold level is selected. The corresponding LED indicates the recognition of a particular output line.

Since only eight output lines are available the eighth line and the lines one to eight represent the lines above eight. When the twelfth line is recognised the eighth and fourth led glows together. The incorporation of speech recognition into telephone is done by making use of the recognition part of the project. The objective is to dial the number when the person's name is spoken out. The output lines of the recognition part are used to store the number in the memory. The stored numbers are retrieved and fed to dialing section when stored name is recognised.

When a word is recognized the corresponding line(s) go high. This is used to generate the equivalent binary of the line being made high. The binary equivalent is latched and taken as offset address for the memory to store numbers. A four bit counter is used to generate the physical address for the memory. A timer is used to generate pulse for retrieval of numbers from the memory.

*The keypad of the telephone is used to input numbers into the RAM. The # - key is used to indicate record mode and * - key is used to indicate the termination of record mode. The numbers being retrieved during the recognition mode are fed to the dialer circuit. The dialer circuit works with the help of a relay. Here the number being retrieved generates equivalent pulse. These pulses are fed to the relay which cuts the hook switch at an appropriate frequency to dial the number being retrieved.*

The number being dialed is displayed using sixteen seven-segment displays. This ensures that the correct number is being dialed. Once the number is dialed the power supply to the recognition circuit is cut and the telephone works in normal mode. This enhances the power saving capability of the circuit. The incorporation of speech recognition into telephone is primarily aimed at the storage of emergency numbers to be called without touching the keypad. The person whose voice is trained alone is recognized. The speaker dependent recognition ensures security of usage. Interfacing the recognition module with a host processor would increase the number of names being stored.

SPEECH RECOGNITION TECHNIQUES

Phonetically speech sounds are divided into two major groups - vowels and consonants. . An alphabetical or phonetic other than a vowel is considered as a consonant. A general grouping in terms of vowel purity in speech sounds will yield the following:

1. *Vowels (a, e, i, o, u)*
2. *semi vowels (y, w)*
3. *liquids (l, r)*
4. *nasals (m, n)*
5. *retroflex nasal (na)*
6. *fricative (v, o, z)*
7. *fricative breath(f, s, x)*
8. *mutes or stops (b, d, g)*
9. *mute breath(p, t, k)*
10. *plosive(t)*
11. *unvoiced dental plosive(ta)*
12. *voiced dental plosive(dh)*

PHONEMES – ENGLISH LANGUAGE

phoneme			representative sound (bold letters)
decimal code	allophone	duration (ms)	
00		10	pause
01		20	pause
02		50	pause
03		100	pause
04		200	pause
05	OY	290	boy
06	AY	170	five
07	EH	50	left
08	KK3	80	count
09	PP	150	peak
10	JH	100	jump
11	NN1	170	none
12	IH	50	it
13	TT2	100	to
14	RR1	130	right
15	AX	50	trouble
16	MM	180	magnet
17	TT1	80	part
18	DH1	140	they
19	IY	170	see
20	EY	200	stay
21	DD1	90	card
22	UW1	60	computer
23	AO	70	long
24	AA	60	hot
25	YY2	130	yard
26	AE	80	man
27	HH1	90	he
28	BB1	40	trouble
29	TH	130	thin
30	UH	70	push-pull
31	UW2	170	food
32	AW	250	south
33	DD2	250	do
34	GG3	120	jig
35	VV	130	very
36	GG1	80	go
37	SH	120	shift
38	ZH	130	measure
39	RR2	80	bring
40	FF	110	for
41	KK2	140	skip
42	KK1	120	ask
43	ZZ	150	zero
44	NG	200	talking
45	LL	80	look
46	WW	140	wire
47	XR	250	dear
48	WH	150	where
49	YY1	90	yes
50	CH	150	chip
51	ER1	110	counter
52	ER2	210	turn
53	OW	170	slow
54	DH2	180	lathe
55	SS	60	stop
56	NN2	140	no
57	HH2	130	hertz
58	OR	240	store
59	AR	200	arm
60	YR	250	clear
61	GG2	80	glue
62	EL	140	angle
63	BB2	60	bit

DIGITIZATION AND STORAGE

The energy spectral density of human speech shows an extremely innocuous situation. Energy peaks are at a few hundred Hz and about 98% of the energy lie below 3 kHz. It is an accepted fact that only digital processing is capable of yielding satisfactory results in speech recognition. Digitization is specified kind of analog to digital conversion technique. Basically, there are two types of voice digitization techniques - waveform digitization and spectral signal method.

WAVEFORM DIGITIZATION

In waveform digitization, the voice is treated as an analogue signal and coded. PCM (pulse code modulation),DPCM (differential PCM),ADPCM (adaptive PCM) ,DM (delta modulation),ADM (adaptive DM) etc. belong to this class.

SPECTRAL DIGITIZATION

In the spectral method the parameters of speech signal are coded by breaking speech into its basic components and waveform segments. Linear predictive coding (LPC), adaptive predictive coding (APC),etc are based on this approach.

The spectral signal method can separate voices and compress vocal information as low as 1.2 to 9.6 KBPS. The well known spectral signal methods are LPC (LINEAR PREDICTION CODING), DPCM (DIFFERENTIAL PULSE CODE MODULATION), PACOR (PARTIAL AUTO CORRELATION), LSP (LINE SPECTRUM PAIR) and FORMANT.

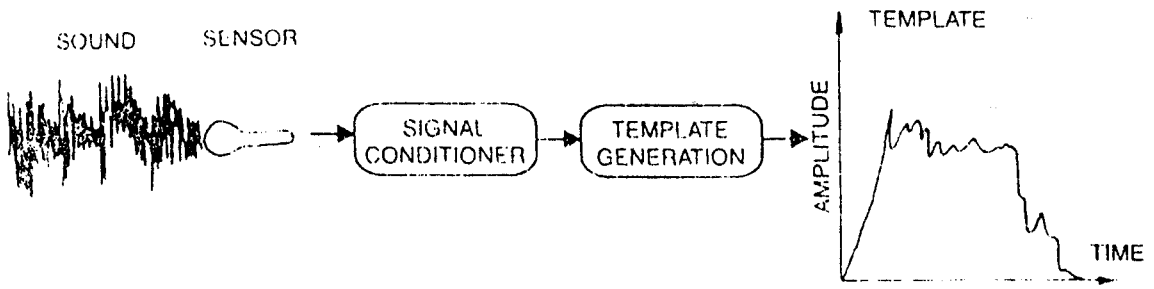
MEMORIZATION

Memorization of voices by digital processing may use either a waveform or a spectral signal to break speech down into coded elements. The original form of the waveform signal system is PCM. A typical PCM at eight bit by eight kilohertz sampling. Thus it needs a data rate of 64 KBPS. The various voice compression techniques are ADM, ADPCM, Adaptive Predictive Coding by Adaptive Bit allocation (APCAB) etc.

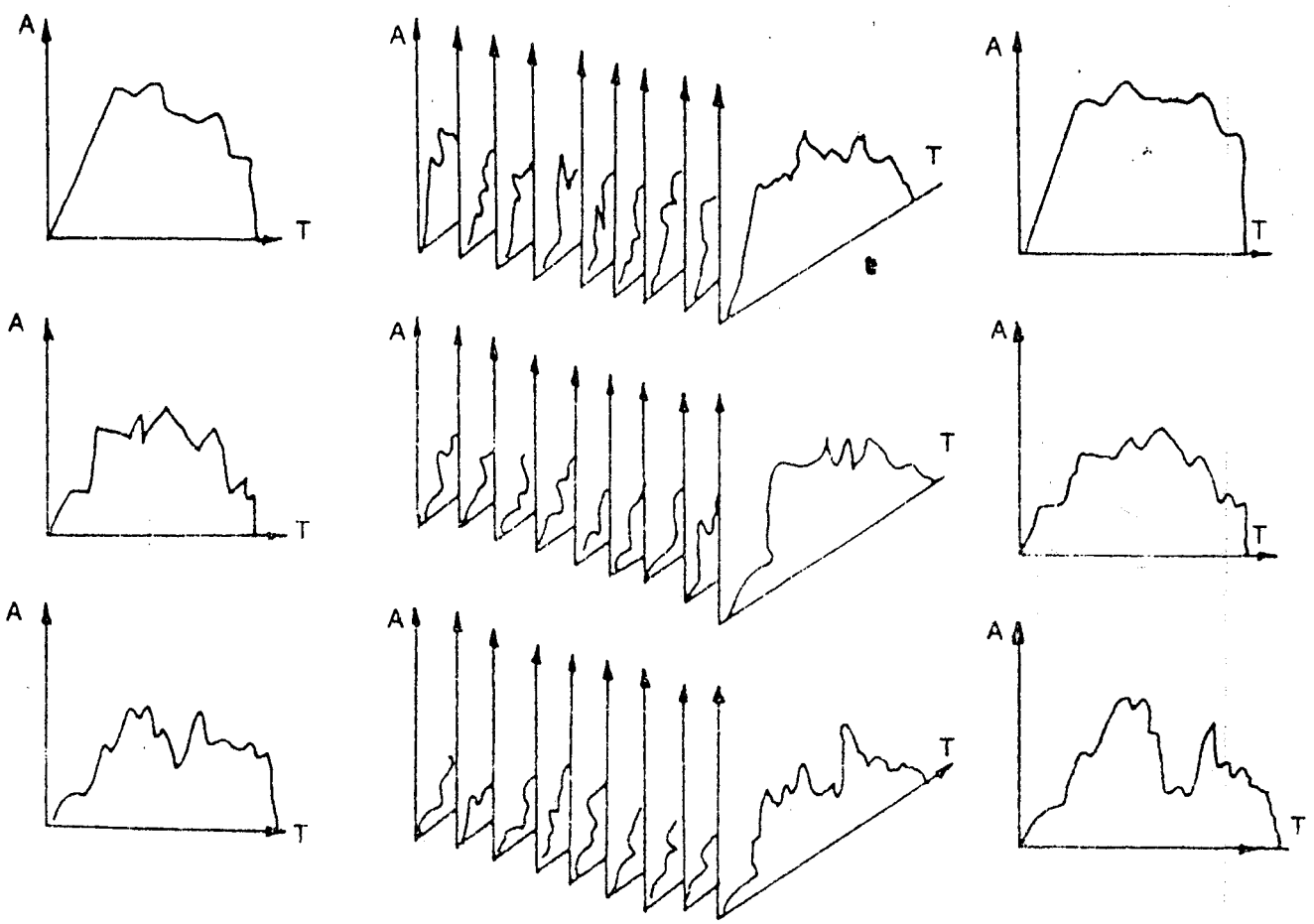
TEMPLATE MATCHING

The bandpass filter divides a speech signal into three frequency bands. These curves show variation in loudness with respect to time in three wide ranges. Collectively these characterize a specific sound figure of given speaker. Each word is processed and maintained in the memory. Such characteristic curves stored in the memory are called templates. These works by

TEMPLATE GENERATION – BLOCK DIAGRAM



TEMPLATE COMPARISON – WAVEFORMS



INPUT TEMPLATE

REF. TEMPLATE

RECOGNISED WORD

matching patterns of processed signals with those stored in memory. If the same speaker whose voice is to be recognised creates templates, these templates will match very closely.

In case a different speaker is the source for the templates, the characteristic curves of the speaker, whose voice is to be recognized, will vary considerably. In such cases, the Comparator assigns a mathematical distance between the sample and the template. This helps the recognition program select the closest word that is being sampled. An announcement of the word match found in the speech synthesis method is usually employed to verify the sample input.

COMPARISON AND RECOGNITITON

Various methods are incorporated for comparison of the characteristic waveforms being generated in real time with the previously stored waveforms. These characteristic waveforms are called templates. The most commonly used methods of template comparison are :

1. *Correlation*
2. *Auto correlation*

CORRELATION

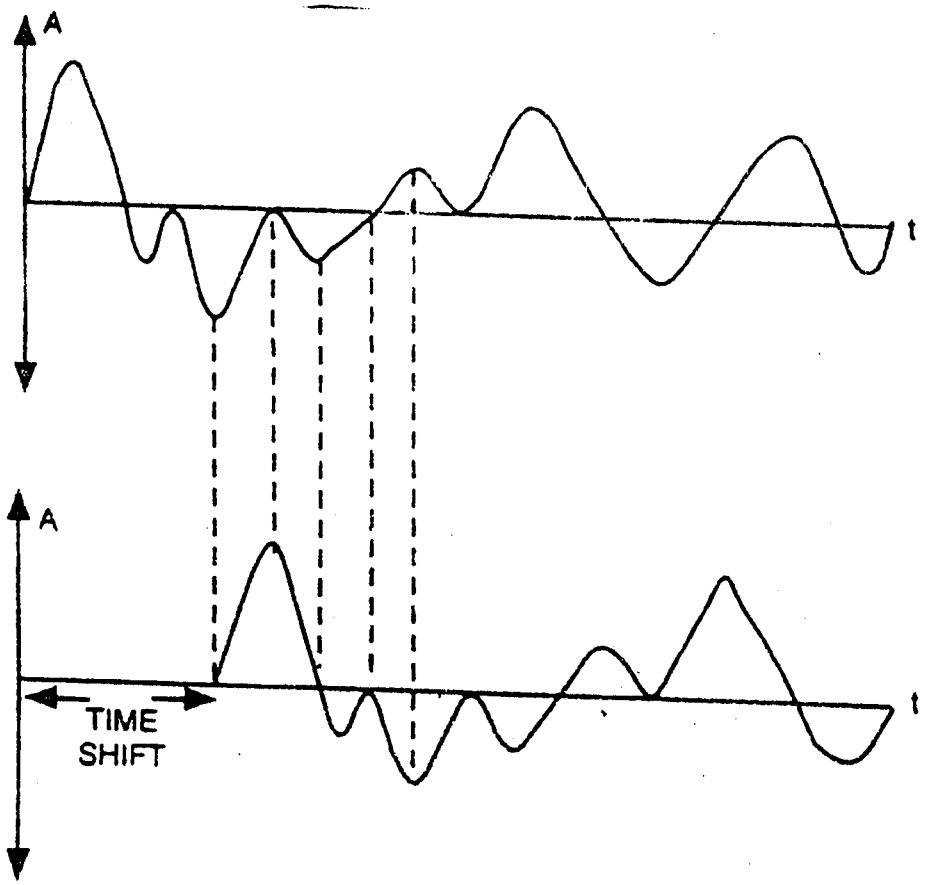
Correlation is measure of the similarity between two waveforms. Waveform correlation is a method of time domain analysis. It is highly useful for detecting periodic signals buried in noise. Correlation is computed by multiplying the waveform ordinate and adding the products over the duration of the waveform.

If the waveforms are identical with respect to time phase and frequency, the correlation between them would be larger. If the waveforms are identical in shape, but different in terms of a time shift between them, the correlation would be smaller. Essentially, correlation is a function of the time shift between two waveforms.

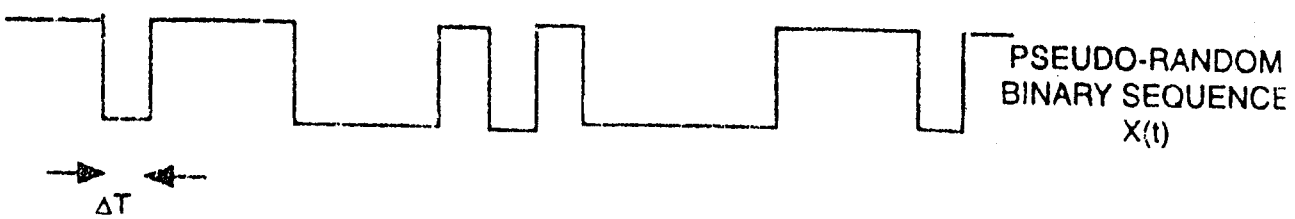
AUTOCORRELATION

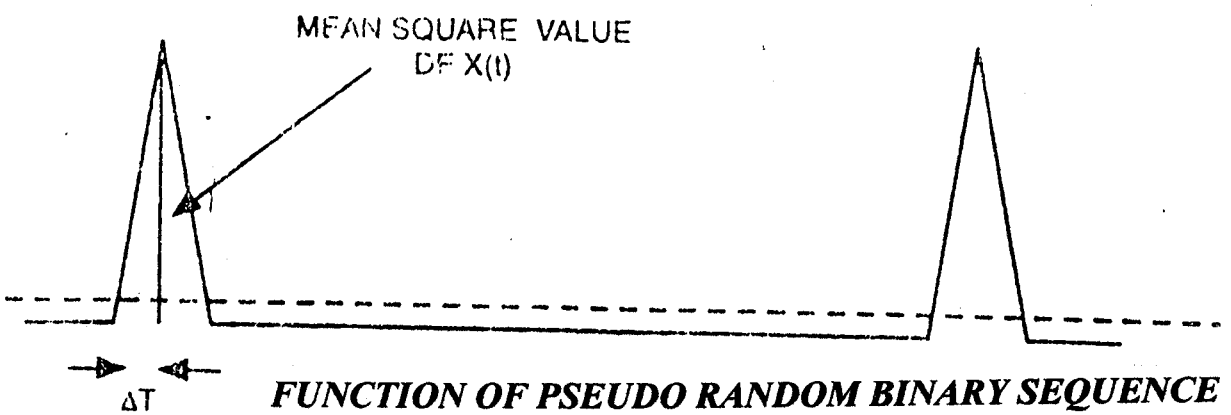
The auto correlation function is also a measure of the similarity between the waveforms and a time shifted version of itself, as a function of time shift. The auto correlation function of any periodic waveform is periodic and has the same period as the waveform itself. For example, the auto correlation of a pseudo-random binary is a series of triangular functions. The more interesting in auto correlation is that, in a random signal (a non-periodic waveform), time shifted with itself (with a time shift value), the similarity recurs. In such a case, the

CORRELATION – FUNCTION OF TIME SHIFT



AUTO CORRELATION –





FUNCTION OF PSEUDO RANDOM BINARY SEQUENCE

auto correlation function is a sharp impulse, which decays from a maximum value to low values of large time shifts.

The width of the auto correlation depends on the mean crossing rate of the random waveform. (The mean zero crossing rate of random signal essentially is its width.).The higher the zero crossing rates, the smaller the time shift required to destroy similarity. In practical terms of speech synthesis, two samples of signals of the same bandwidth may have different waveforms but their auto correlation functions could be identical. In fact, the auto correlation function of any signal does not depend on the actual waveforms, but on their frequency content.

PROCESSOR OVERVIEW

The RSC-164 features a high-performance 8-bit micro controller with on-chip A/D, D/A, RAM and ROM. Various functional units have been integrated qnto the CPU core in order to reduce total system cost and increase system reliability without degrading system performance. The RSC – 164 delivers 4 MIPS of integer performance at 14.32 MHz providing maximum performance at minimum cost.

The CPU core embedded in the RSC-164 is an 8-bit, variable-length-instruction, micro controller. The instruction set is loosely based on Intel's 8051 Ô, and has a variety of addressing mode move instructions. The RSC-164 processor avoids the limitations of dedicated A, B, and DPTR registers by having completely symmetrical source and destinations for all instructions. The 384 bytes of internal RAM are organized as a Register Space.

SPEECH RECOGNITION

The RSC-164 uses a neural network to perform speaker-Independent or speaker-dependent speech recognition. Speaker-dependent recognition requires external memory to store speech recognition

information (e.g., SRAM,Flash Memory). Speaker-independent recognition requires on-chip or off-chip ROM to store the words to be recognized Continuous listening allows the chip to continuously listen for a specific word .

SPEECH AND MUSIC SYNTHESIS

The RSC-164 provides high-quality speech synthesis by using a hybrid of time-domain compression scheme that improves on conventional ADPCM and a customized reuse of sounds. Speech synthesis requires on-chip or off-chip ROM to store audio sounds for synthesis.The RSC-164 provides high-quality, low-cost four- voice music synthesis which allows multiple, simultaneous instruments.

RECORD AND PLAYBACK

The RSC-164 can perform audio record and playback at various compression levels depending on the quantity and quality of playback desired. Data rates of under 14,000 bits per second are achievable while maintaining very high quality reproduction. The RSC-164 also performs silence removal to improve sound quality and reduce memory requirements.

SPEAKER VERIFICATION

The RSC-164 can also perform text-dependent speaker verification. After a speaker trains the chip on a specific word, the chip is able to identify whether that word is spoken by the original speaker, thus providing biometric security.

SOUND PROCESSING

A microphone with an external preamp converts sound into an audio signal that is fed to the RSC-164. The gain of the external preamp may be controlled by the RSC-164 by using two of the I/O lines. The RSC-164 uses an ADC (Analog - to -Digital Converter) to convert incoming analog speech signal into digital data. The output audio signal of the RSC-164 is derived from a DAC (Digital-to-Analog Converter) or PWM (Pulse Width Modulator)

POWER

The typical operating current is 10 mA operating at 14.32 MHz. Lowering clock frequency reduces power consumption, although speech recognition requires a 14.32 MHz clock.

VOICEDIRECT – BLOCK DIAGRAM

ANALOG TO DIGITAL CONVERTER

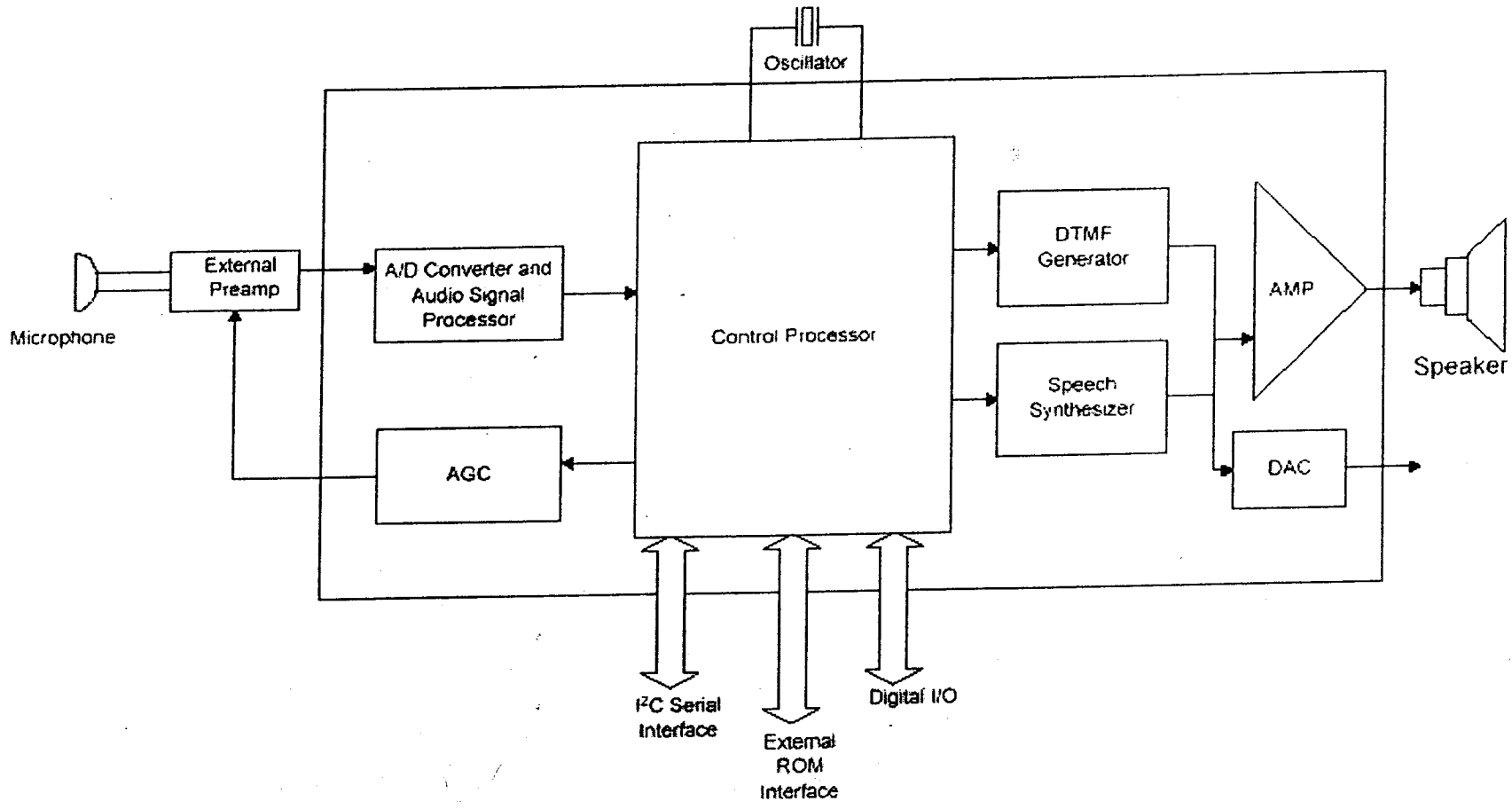
Digitization is specified kind of analog to digital conversion technique. Basically, there are two types of voice digitization techniques - waveform digitization and spectral signal method

In waveform digitization, the voice is treated as an analogue signal and coded. PCM (pulse code modulation),DPCM (differential PCM),ADPCM (adaptive PCM) ,DM (delta modulation),ADM (adaptive DM) etc. belong to this class. In the spectral method the parameters of speech signal are coded by breaking speech into its basic components and waveform segments. Linear predictive coding (LPC), adaptive predictive coding (APC),etc are based on this approach.

AUTOMATIC GAIN CONTROLLER

The VOICEDIRECT IC has an Automatic Gain Controller in built. The recognition ability of the mic is affected if input signal saturates the A/D converter or is too weak. The output of mic are fed to gain 0 and gain 1 of the IC. The AGC is made use of in order to amplify the signal when a weak input is

BLOCK DIAGRAM – VOICE DIRECT



received from the mic or to limit the input voltage when a high input is received. Thus AGC is used for signal conditioning before being fed to the processor.

AUDIO OUTPUT

The audio output section consists of :

1. *DTMF generator*
2. *Speech Synthesizer*
3. *DAC*
4. *Amplifier*
5. *Loud Speaker*

DTMF GENERATOR

The DTMF (Dual Tone Multi Frequency) generator is used to generate two separate tones at different frequencies. It is usually used in the dialing of push button telephones. The multi frequency being generated is being used for frequency shift keying. The frequency-shifted signal is being is made use of in the generation of PWM signal. The pulse width modulated signal is fed to the in built amplifier of the processor.

SPEECH SYNTHESIZER

The speech synthesizer is used to generate the original digital speech from the stored speech prompts. The speech is stored as voice source (periodic) and voiceless (fricative) source. These sources are filtered and fed to the summer. The summed up signal is controlled by various parameters like voicing control and articulation control. This signal is passed through several stages of bandpass filters to remove the noise elements. The filtered signal is amplified and fed to a loudspeaker.

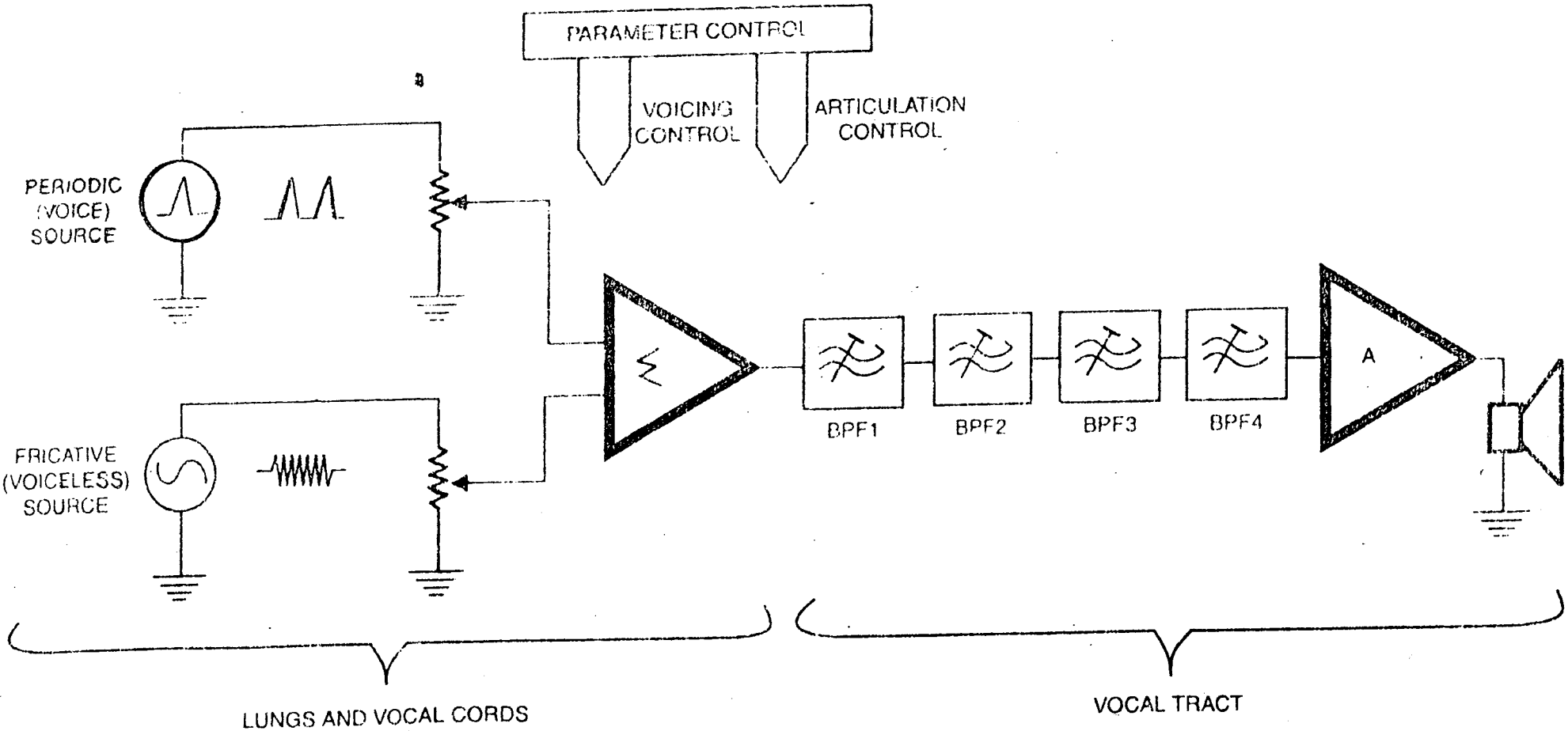
AMPLIFIER

The amplifier is fed with input from the PWM signal being generated. The PWM signal is amplified and sent to the output lines. The PWM output lines can be directly connected to aloud speaker without further amplification.

OSCILLATOR

Two independent oscillators in the RSC-164 provide a High - frequency clock and a 32 kHz time - keeping clock. The oscillator characteristics are as follows:

SPEECH SYNTHESIZER – BLOCK DIAGRAM



- *Oscillator #1: Pins XI1, XO1 14.32 MHz (3.5V-5.0V)*
- *Oscillator #2 Pins XI2 and XO2 32768 Hz (3.5V-5.0V)*

Oscillator #1 works with an external crystal, a ceramic resonator or LC. Use of Oscillator #2 requires a crystal for precision timing.

I^2C SERIAL INTERFACE

. The RSC-164 can connect serially through two I/O lines to a serial EEPROM for applications with low data storage requirements. This method of interfacing with a memory through two lines viz. SDA and SCL is known as I^2C architecture.

EXTERNAL ROM INTERFACE

Separate data and address buses allow use of standard EPROMs, ROMs, SRAMs, and flash memory with little or no additional decoding. The speech prompts can be customized using external speech ROMs. The hardcore index of speech ROM consists of mandatory and optional speech prompts. These can be customized to extended speech ROM or foreign language speech ROM by interfacing with the processor.

FEATURES

- *Recognition accuracy better than 96%(Speaker Independent) and 99% (Speaker Dependent).*
- *Recognizes up to 15 words/phrases (Stand Alone)*
- *Supports phrases up to 3.2 seconds*
- *Minimal memory less than 100 bytes/word external*
- *Integrated Single-Chip Solution*
- *Direct interface to 8K byte external memory for template storage (Serial EEPROM)*
- *English speech prompts*
- *Output PWM circuitry for direct speaker drive*
- *Language localization and custom synthesis options*
- *Two Operating Modes -Standalone & External Host*
- *External Host - controlled by an external processor through a simple 3-wire host interface*
- *Stand Alone - pin-configurable operation with full range of speech capabilities*
- *Synthesis data rates from 5,000-15,000 bits*

per second

- *Speaker-independent speech recognition*
- *Speaker-dependent speech recognition*
- *High quality speech synthesis and sound effects*
- *Four-voice music synthesis*
- *Voice record & playback*
- *4 MIPS 8-bit micro controller*
- *On-chip A/D and D/A converters, digital filtering*
- *32kHz clock for time keeping*
- *Internal 64kbytes ROM; 384 bytes RAM*
- *16 general purpose I/O lines*
- *External memory bus: 16-bit Address, 8-bit Data*
- *On-chip output amplifier for direct speaker drive*
- *Low Power Requirements*
- *3.5 - 5.0V supply*
- *~10mA operating current*

RSC-164 ARCHITECTURE:

The RSC-164 is a highly integrated device that combines:

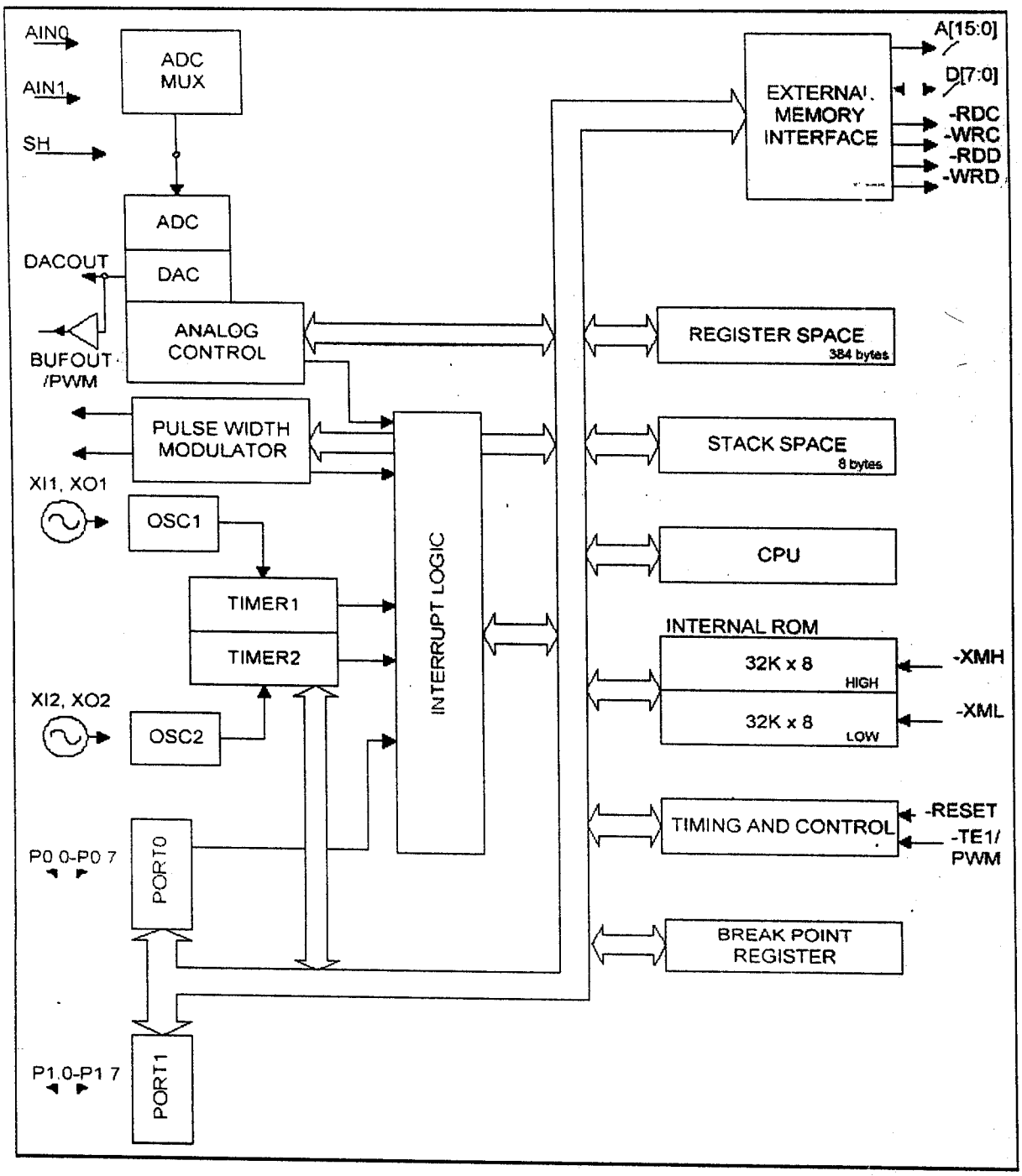
- *8-bit micro controller*
- *On-chip ROM (64 Kbytes) and RAM (384 bytes),*

  and the ability to address off-chip RAM or ROM
- *A/D converter and D/A converter*

The RSC-164 has an external memory interface, with 16-bit addresses and a 8-bit data buses, for accessing external memory. It also has an internal ROM that can be enabled or disabled (partially or fully) by pin inputs (signals -XMH, -XML). Two bi-directional ports provide 16 general-purpose I/O pins to communicate with external devices.

The RSC-164 has a high frequency (14.32 MHz) oscillator and a low frequency (32,768 Hz) oscillator suitable for timekeeping applications. The processor clock can be selected from either source, with a selectable divider value. The device performs speech recognition when running at 14.32 MHz. The RSC-164 also support programmable wait states to allow the use of slower external devices. There are two programmable 8-bit counters / timers, one derived from each oscillator.

ARCHITECTURE – VOICE DIRECT



RSC-164 INSTRUCTION SET

The instruction set for the RSC – 164 has 52 instructions comprising 8 move, 7 rotate, 11 branch, 11 register arithmetic, 9 immediate arithmetic, and 6 miscellaneous instructions. All instructions are 3 bytes or fewer, and no instruction requires more than 8 clock cycles to execute.

GENERAL PURPOSE I/O

The RSC - 164 has 16 general purpose I/O pins (P0.0- P0.7, P1.0-P1.7). Each pin can be programmed as an input with weak pull-up (~200kW equivalent device); input with strong pull- up (~10kW equivalent device) ; input without pull - up, or as an output. This is accomplished by having 32 bits of configuration registers for the I/O pins (Port Control Register A and Port Control Register B for ports 0 and 1).

EXTERNAL MEMORY

Separate data and address buses allow use of standard EPROMs, ROMs, SRAMs, and flash memory with little or no additional decoding . Provision of separate read and write signals for each external memory space further simplifies interfacing. The RSC-164 includes 8 data lines (D[7:0]) and 16 address lines (A[15:0]), along with associated control signals

for interfacing to external memory. The RSC-164 can connect serially through two I/O lines to a serial EEPROM for applications with low data storage requirements.

OSCILLATORS

Two independent oscillators in the RSC-164 provide a High - frequency clock and a 32 kHz time - keeping clock. The oscillator characteristics are as follows:

- *Oscillator #1: Pins XI1, XO1 14.32 MHz (3.5V-5.0V)*
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Oscillator #1 works with an external crystal, a ceramic resonator or LC. Use of Oscillator #2 requires a crystal for precision timing.

CLOCK

The RSC-164 uses a fully static core – the processor can be stopped (by removing the clock source) and restarted without causing a reset or losing contents of internal registers. Static operation is guaranteed from DC to 14.32 MHz. Typically the processor clock runs from a 14.32 MHz crystal with no divisor and one wait state. This creates internal RAM cycles of 70 nsec duration and internal ROM or external cycles of 140 nsec duration.

Gate delays may allow operation with memories having access times as slow as 120 nsec.

TIMERS/COUNTERS

The two independent oscillators of the RSC-164 provide counts to two internal timers. Each of the two timers consists of an 8-bit reload value register and an 8- bit up-counter. The reload register is readable and writeable by the processor.

INTERRUPTS

The RSC -164 allows for five interrupt sources, as selected by software. Each has its own mask bit and request bit in the IMR and IRQ registers respectively. The following events can generate interrupts:

- *Positive edge on Port 0, bit 0*
- *Overflow of Timer 1*
- *Overflow of Timer 2*
- *Completion of PWM sample period*

ANALOG OUTPUT

The RSC - 164 offers two separate options for analog output. The DAC (Digital to Analog Converter) output provides a general

purpose 10-bit analog output that may be used for speech output (with the inclusion of an audio amplifier), or other purposes requiring an analog waveform. For speech applications that require driving a small speaker, the PWM (Pulse-Width Modulator) output can be used instead of the DAC output. The PWM output can directly drive a 32 ohm speaker.

THE VOICE DIRECT IC

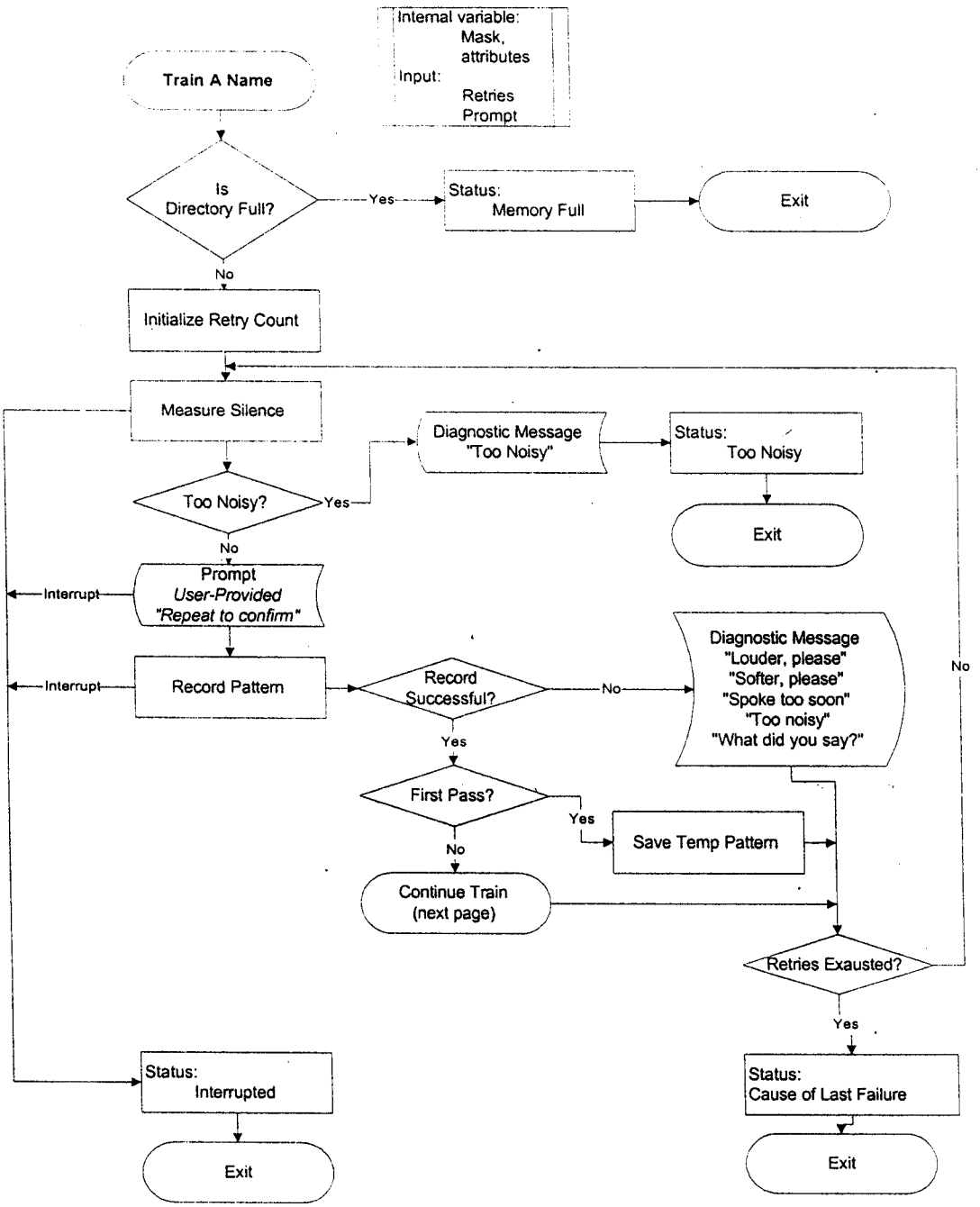
The chip utilizes its neural network recognizer to recognize discrete words or short phrases. The chip performs three basic functions:

- ***Train*** *- Users train the chip to identify a specific word by saying each word twice. After training, the two patterns are averaged and a template is stored.*
- ***Recognize*** *- The user speaks a word and the chip compares the new pattern with the previously trained templates to identify which word was spoken. The chip then outputs the result of its analysis.*
- ***Erase*** *- Users can delete previously trained words from the set of recognition templates. In each of these functions, Voice Direct features integrated speech prompting providing a complete interactive user interface.*

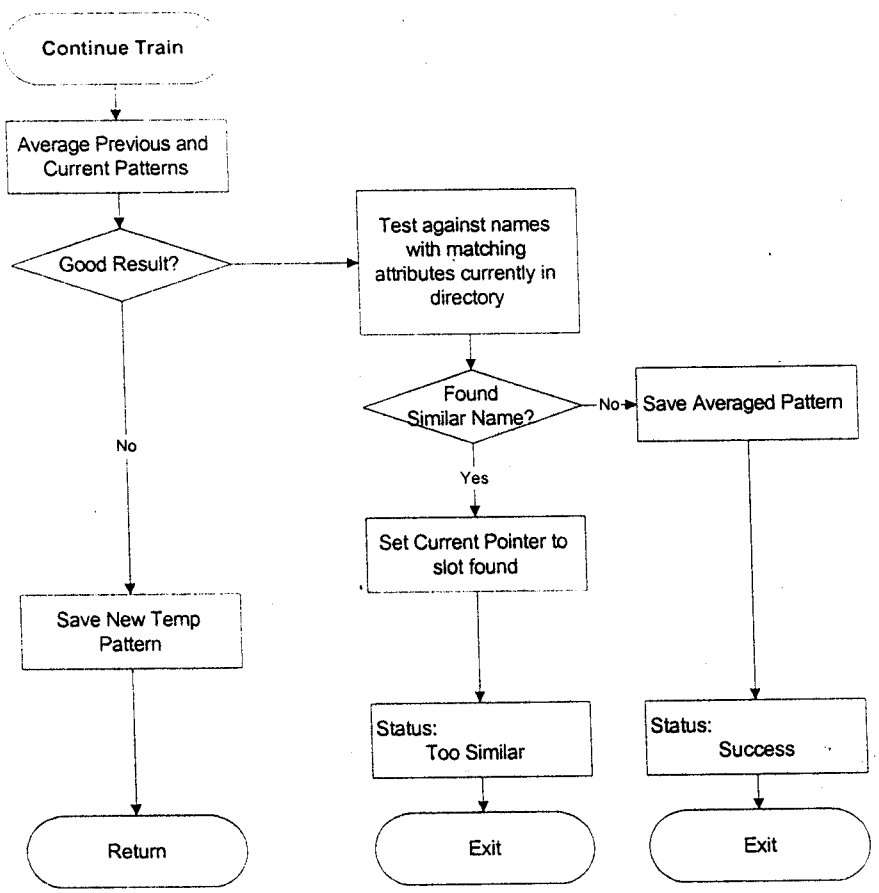
EXTERNAL HOST MODE

Voice Direct's external host operating mode provides a complete speaker dependent recognition system that can easily be controlled by an External Host processor (Host). The Host communicates to Voice Direct using a 3-wire serial bus. This high-level control interface allows the Host to control the flow of operations and to initiate all of its functions including training, recognition, or synthesis. In external host mode, Voice Direct recognizes up to 60 words. To

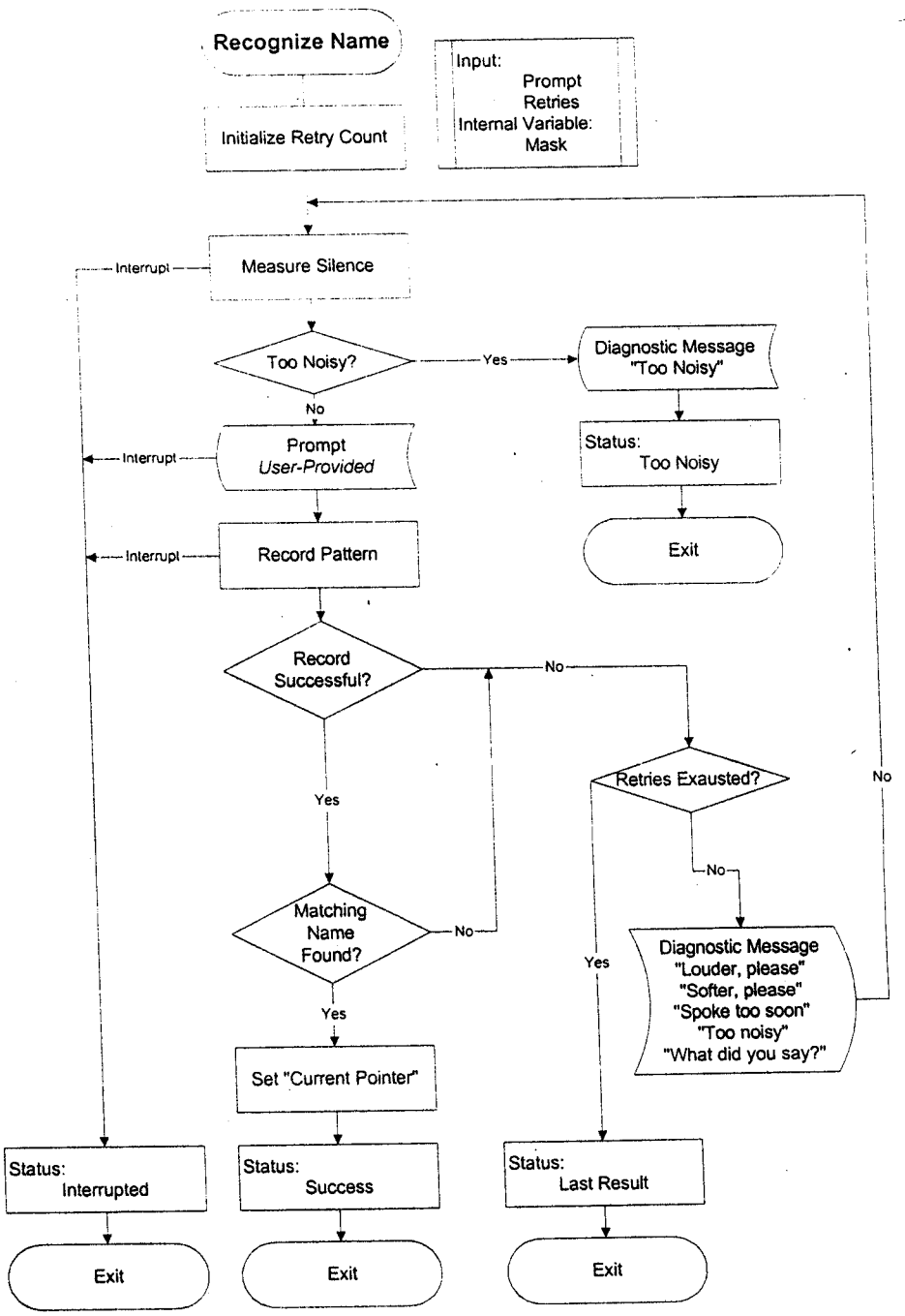
FLOW CHART – TRAINING



FLOW CHART – TRAINING (contd.)



FLOW CHART – RECOGNITION



improve application flexibility these words can be divided into smaller recognition sets, improving accuracy and functionality.

STAND ALONE MODE

Voice Direct's stand alone operating mode is designed to provide a complete recognition system using only the chip, external template storage memory, and a few passive electronic components. All operations, including training, recognition, and erase can be controlled by configuring chip input pins. Output pins provide status information to external devices. In stand-alone mode, Voice Direct can recognize one set of 15 words.

SPEECH PROMPTS

Voice Direct includes a standard English vocabulary of over 100 phrases to guide the user through its functions. This standard word list can be replaced with a customized word list for English or foreign languages via an external ROM chip.

RECOGNITION THRESHOLD

Voice Direct supports multiple acceptance threshold levels during the recognition process. The acceptance level determines how closely the

spoken word must match a pre-trained template in order to pass. The user adjusts the level depending on the complexity of the recognition set. More complex recognition sets should have a higher acceptance level, while simpler sets can use a lower threshold level.

MEMORY INTERFACES

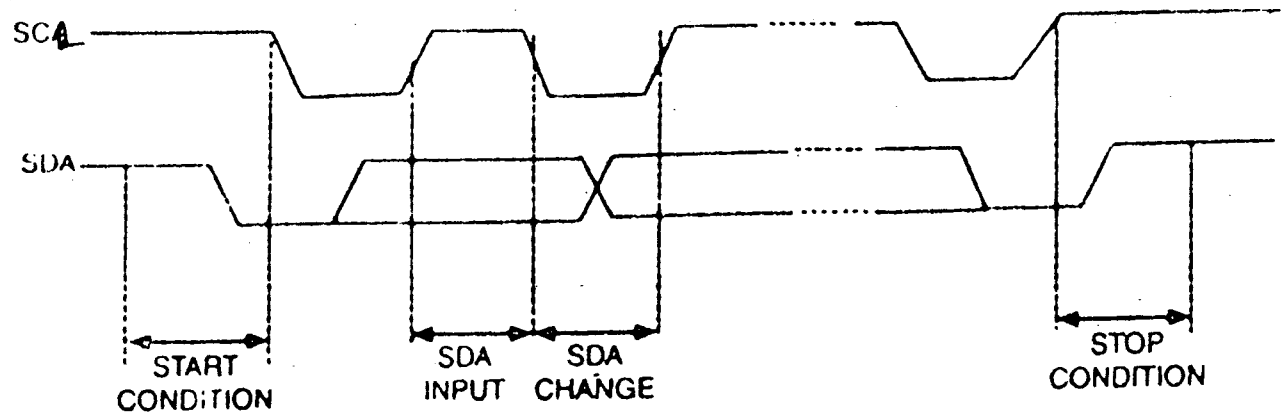
Voice Direct requires 8K bytes of dedicated external Serial EEPROM memory for template storage. Each time a new word is trained, Voice Direct automatically writes the template to the memory device. During recognition, Voice Direct reads the templates from the memory device and compares them with spoken words or phrases. Voice Direct communicates through an I^2C 2-wire serial interface.

NON-VOLATILE MEMORY-24C65

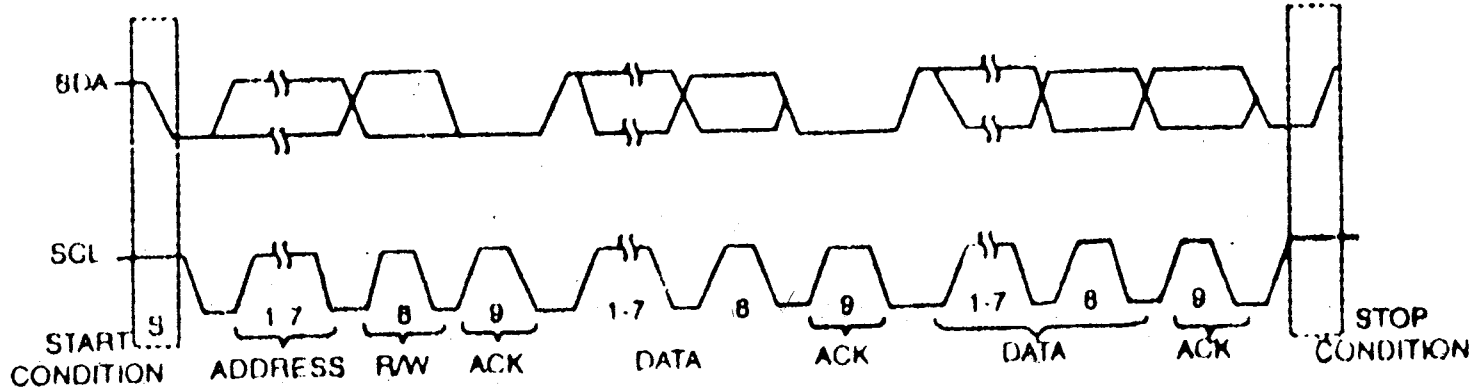
The 2-wire serial CMOS EEPROM 24C65 is used in the circuit for storing the templates generated by the processor. The stored templates remain in memory even after power failure.

The 24C65 is an 8K(1024 x 8) bits non-volatile memory.8K bits are internally organized as 1024 x 8 bits .A total of 512 bits are reserved for each

I^2C BUS TRANSFER DIAGRAM



SAMPLE MESSAGE TRANSFER



word being stored. This allows storage of upto 15 words in the memory when used in standalone mode.

The memory is interfaced with the processor using two control lines SCL (serial clock) and SDA (serial data). This two wire interface is popularly known as I^2C bus interface.

THE I^2C BUS ARCHITECTURE

I^2C stands for Inter-Integrated Circuit. This architecture is mainly used with single-chip micro controller based systems that require external circuits like EEPROM, RAM etc. The key advantage of this is that only two lines can connect multiple devices.

DATA TRANSFER

Four different conditions exists in I^2Cbus transfers. They are:

- *Start*
- *Stop*
- *Bit transfer*
- *Acknowledge*

NORMAL DATA BIT WRITE / READ

During transfer of data from master to slave device , SDA is set to logic 0 or 1 only when SCL is low. After small delay SCL is pulsed high to clock the data. During read operation, SDA is an input line and its logic state is clocked with SCL going high.

START CONDITION

Start is a special condition where SDA changes its state from high to low when SCL is high. Both SCL and SDA are controlled by RSC 164.

STOP CONDITION

Stop is also a special condition where SDA goes from low to high when SCL is high. Both SCA and SDA are controlled by RSC 164.

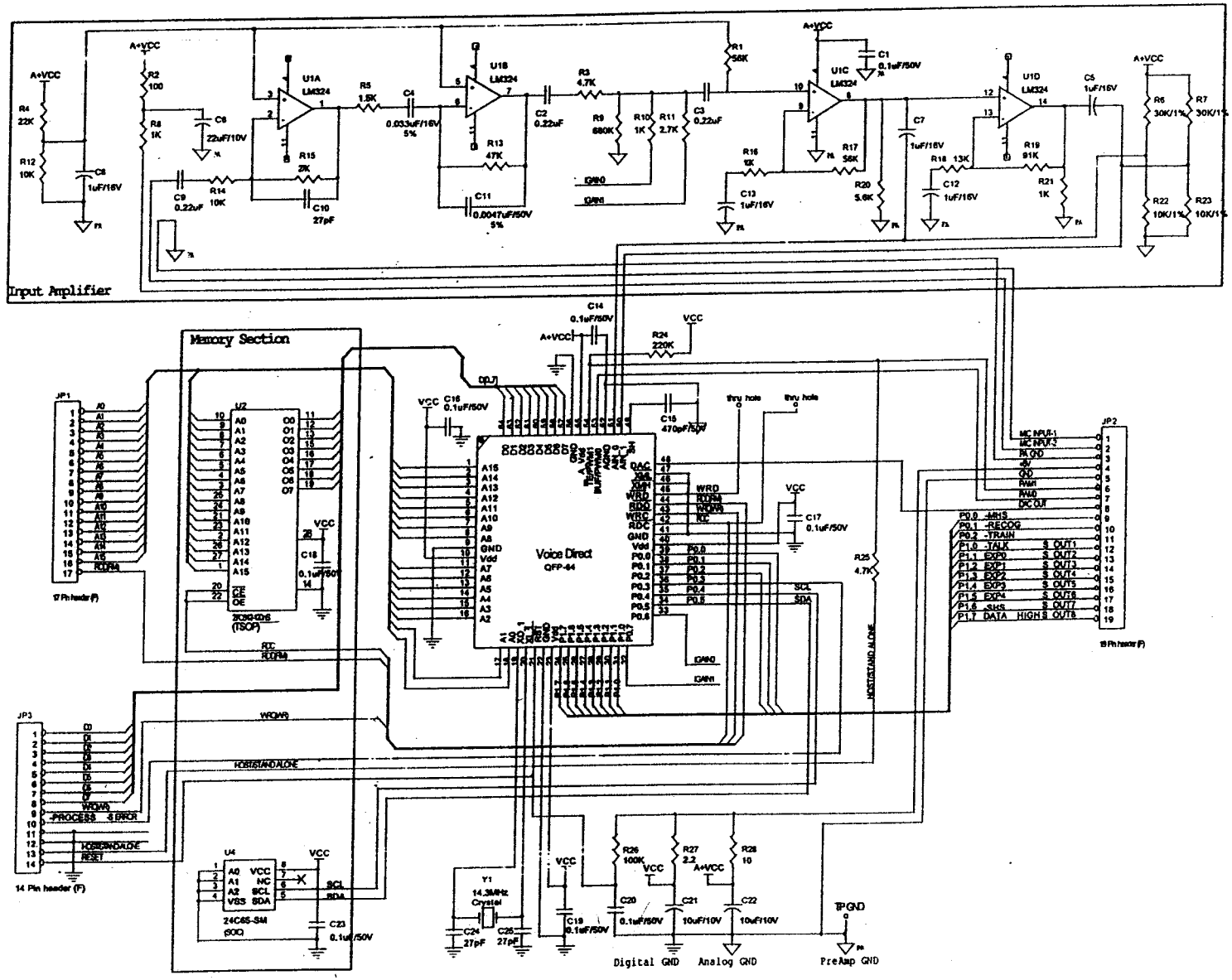
ACKNOWLEDGE

After transmitting 8 data bits from RSC 164 to the memory the direction of SDA line is reversed. One more clock pulse is given by RSC 164.During this period the memory sets SDA low. This indicates the acceptance of data by the memory. When data is read from the memory, after reading 8 bits direction of SDA is reversed. SDA is set low or high and then SCL is pulsed.

MODULE DESCRIPTION

- *A word or phrase shorter than 3.2 seconds and not containing silences longer than 0.5 seconds is fed as input.*
- *The audio signal (spoken word) is externally amplified and filtered and then supplied to the analog inputs of the Voice Direct, which converts the analog waveforms to digital samples.*
- *Voice Direct analyzes the speech signal samples and generates a pattern of information representing significant speech elements.*
- *Voice Direct increases or decreases the gain of the external amplifier as needed to maintain signal quality.*
- *Using a neural network, the pattern is compared with previously stored template patterns; a small number of candidate templates are selected.*
- *The two templates thus created during the training process must closely match (the speech patterns should be similar).*
- *The new candidate word will not be accepted if it is too similar to an existing word*
- *The candidate templates are further processed to determine the one template that provides the best match to the unknown pattern.*

CIRCUIT DIAGRAM – MODULE



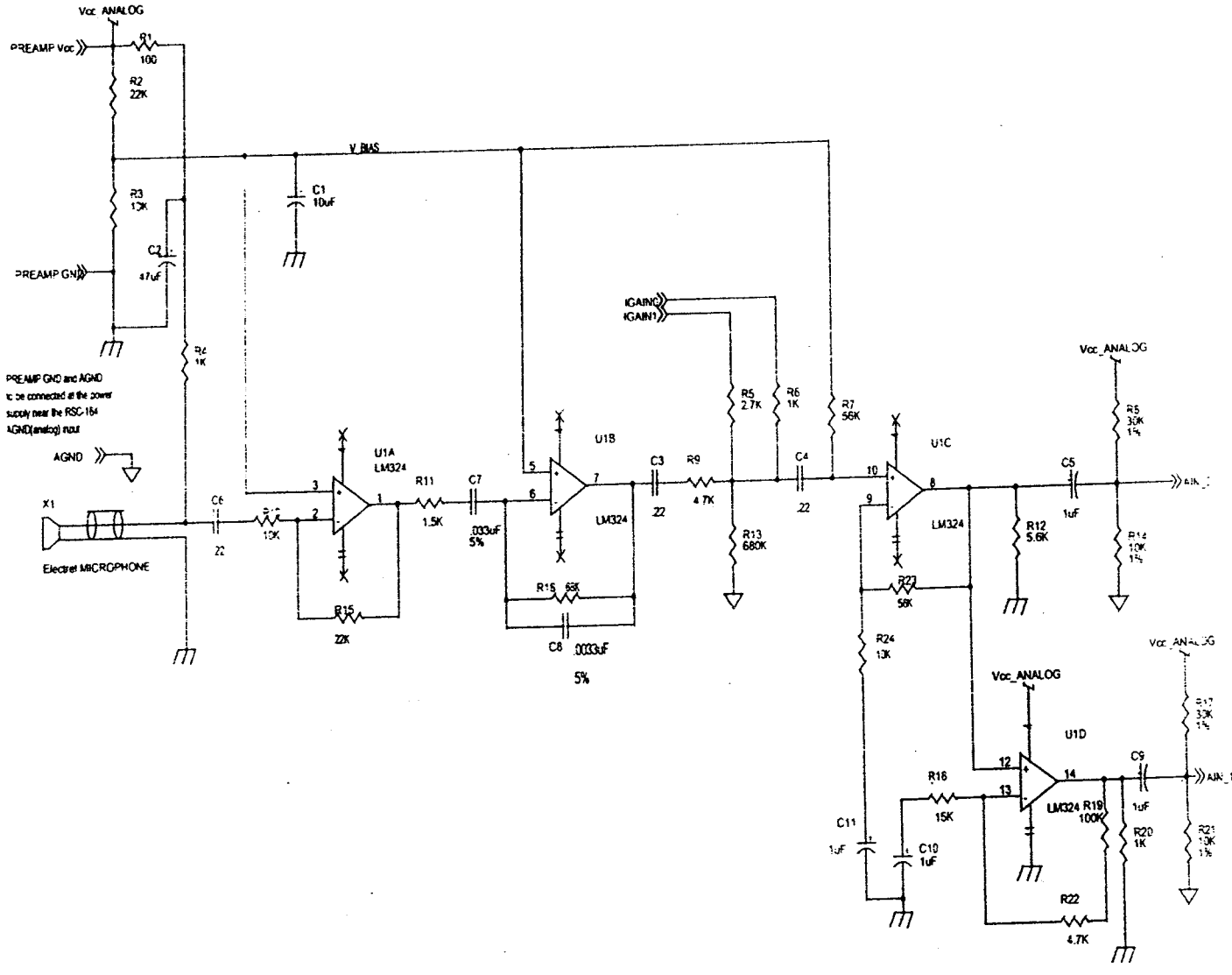
- *If the best match template gives a score above a pre-defined threshold, Voice Direct chooses the word associated with that template.*
- *A third template composed of the average of the first two templates is then created*
- *The third average template is then stored in external memory and used during the recognition process.*
- *When an entry is created, an attribute byte is associated with the voice template. Attribute bytes allow users to distinguish between different groups or kinds of entries.*
- *If no template provides a match above threshold, a special "no match" value is chosen.*

INPUT AUDIO PREAMPLIFIER

The audio preamplifier circuit is shown in Figure. It is a four-stage amplifier with band pass filter and with 2-bit Automatic Gain Control (AGC) circuit. When IGAIN0 and IGAIN0 are set for high-Z, the maximum gain is approximately 53dB at the center frequency of 1.49KHz. This may vary based upon the application's environment. The 3dB cut-off frequencies are 580Hz and 4.2KHz.All power and grounds are analog. Separate analog and digital power and ground supplies for best performance.

- *R4 supplies the power to a standard 2-wire electret microphone. If a self-powered microphone is used, R1, R4 and C2 can be eliminated. Any noise present at R4 will be coupled into the speech signal.*
- *The voltage divider, R2 and R3, is used to provide the DC bias for U1A, U1B, and U1C, and it is set at approximately at 1/3 Vcc.*
- *The first amplifier U1A has a gain of 2.2.*
- *The second amplifier U1B is a band pass with a gain of approximately 7.8 at the center frequency of 1.49KHz.*

INPUT AUDIO PREAMPLIFIER



- *The 2-bit AGC circuit is a programmable voltage divider consisting of C3, R9, R13, R5, R6, and C4.*
- *To prevent DC level shifts with AGC changes, the AGC circuit is AC coupled by C3 and C4, and the AGC circuit has a reference to the analog ground (not to the pre-amp ground).*
- *The IGAIN0 and IGAIN1 AGC control signals may independently be either at ground or at High-Z, giving four different attenuations.*
- *The gain ratios for AGC are "1.0", "0.36", "0.18", and "0.13".*
- *The third amplifier U1C has a gain of 6.6.*
- *The fourth amplifier U1D has a gain of 8.*
- *R12 and R20 provide adequate output bias current to prevent crossover distortion for U1C and U1D respectively.*
- *Both AIN0 and AIN1 outputs are AC coupled and then DC biased such that at full swing the negative peak voltage goes below 0VDC (analog ground) at the inputs of the RSC chip.*

CIRCUIT DESCRIPTION

MIC

An inexpensive omni-directional electret capacitor microphone with a minimum sensitivity of-60 db is being used. Directional microphones have a frequency response that depends on their distance from sound source.

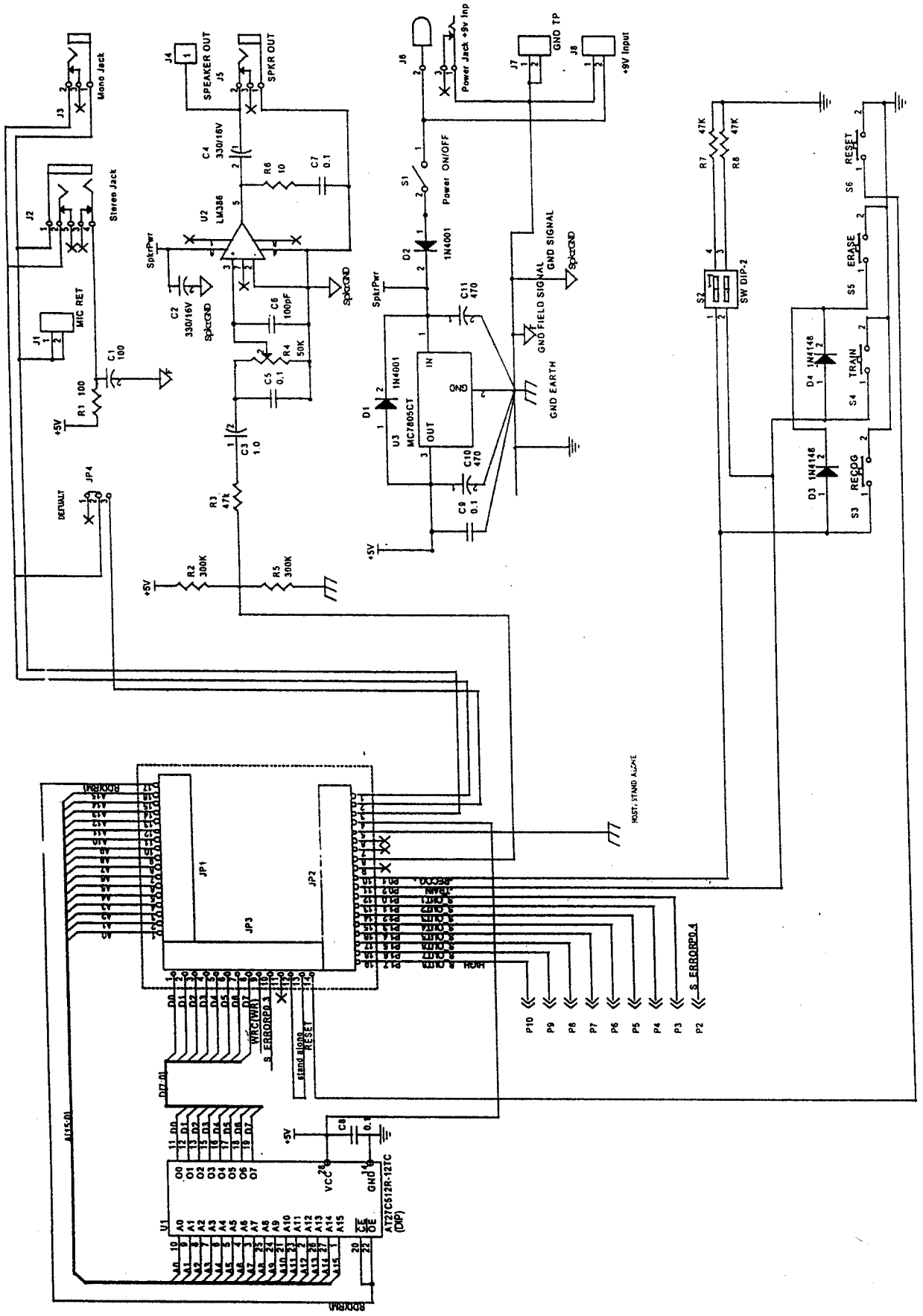
The mic is connected to the voice direct IC through a four stage pre-amplifier section. The pre-amplifier section consists of one input amplifier, bandpass filter AGC circuit, a second stage amplifier and a buffer amplifier of gain 8. The recognition ability of the mic is affected if input signal saturates the A/D converter or is too weak.

The output of mic are fed to gain 0 and gain 1 of the IC. The output of the second stage amplifier is fed to ain0. The output of the buffer amplifier is fed to ain1. Since ain1 accepts only a signal with peak to peak amplitude set to 8 times ain0.

SPEAKER:

The audio outputs are provided from RSC-164 ,using the PWM0,PWM1 and the DAC output VoiceDirect can directly drive a 32 ohm speaker from SP0 and

CIRCUIT DIAGRAM –1



SP1 (Speaker0 and speaker1) .SP0 and SP1 are push pull Pulse width modulation (PWM) outputs with an aliasing frequency well above the audio band , so that the signals can be connected directly to the speaker terminal with no additional filtering. DAC can drive a high impedance (22k Ohm) analogue audio output. This signal is power amplified to drive a speaker as shown in the figure and is low pass filtered with a corner frequency of 20 kHz

The DAC is amplified using LM386 IC which has a 3 pin variable potentiometer. By varying the potentiometer the volume of the speaker is adjusted.

MODES:

Voice direct has two modes of operation:

1. *RECOGNITION*
2. *TRAINING*

TRAINING :

This mode is realized when the training switch is closed for at least 1/10th of a second. A word or phrase being trained should be less than 3.2 seconds long and should not have silence longer than 0.5 secs. Training terminates when no word is spoken in response to a speech prompt. When a word is said the IC generates a time domain template. The characteristic curves are called the template). The IC then prompts for the second template. The first and second

templates are then compared to check whether they are matching. If they match then the IC generates the average pattern and stores the average template in the serial EEPROM.

RECOGNITION :

This mode is initiated when the recognition switch is pressed. The IC generates a speech prompt which is audible through the speakers , the voice direct then waits for the phrase to be recognised to be spoken out. The spoken word is then converted into a template and then compared the template that it stored during the training period. If the comparison is within the threshold limit the word is recognised else the IC prompts WORD NOT RECOGNIZED.

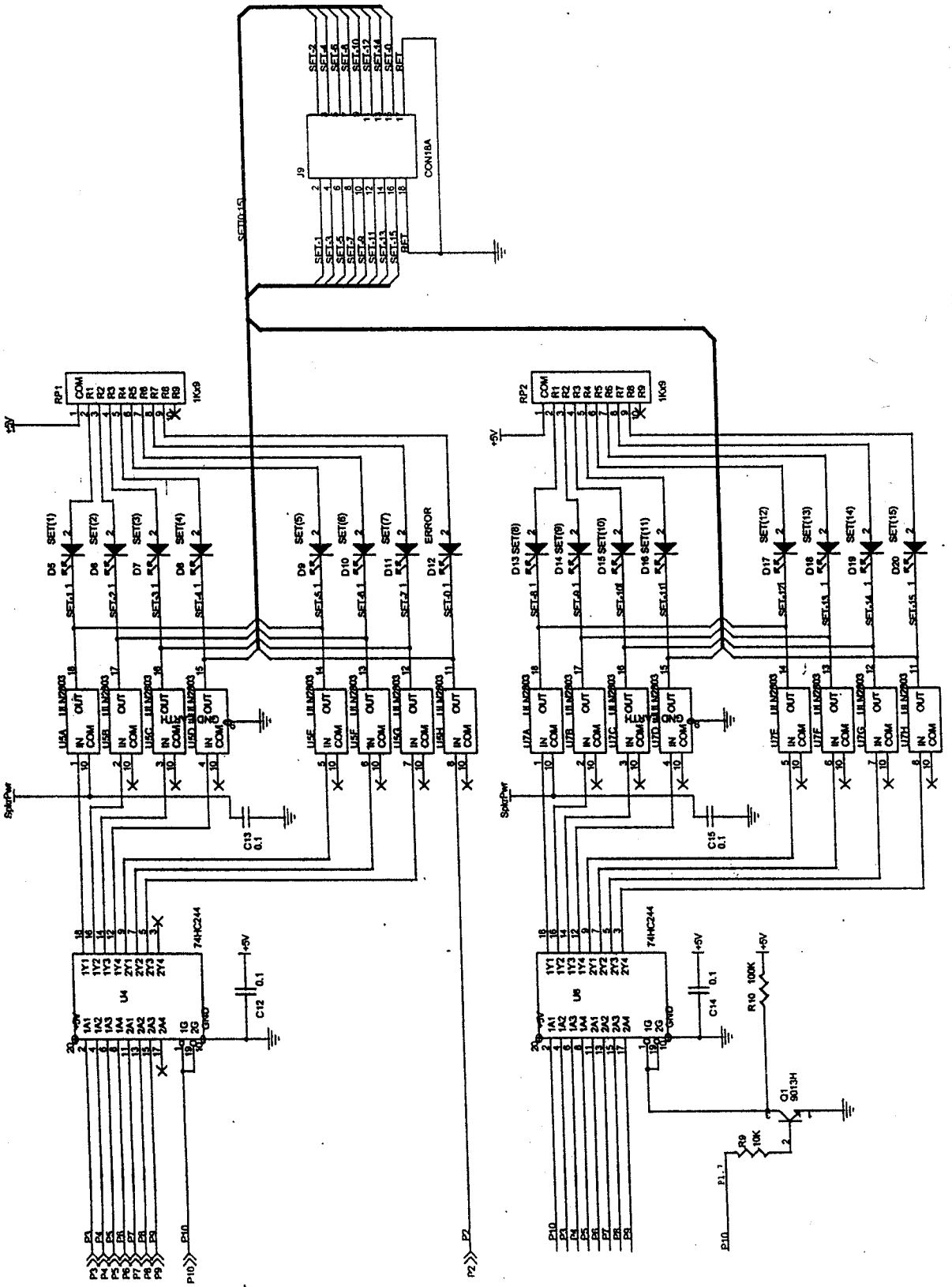
ERASE:

When the recognition and the training switch are pulled to ground for more than a second the words stored in the EEPROM are erased from the memory.

RESET:

When the reset switch is pressed the reset pin of the IC is pulled to ground. The memory interfaced to the processor is also refreshed

CIRCUIT DIAGRAM – 2



THE OUTPUT

The VOICE DIRECT IC has only 8 output pins. The lines above eight and the eighth and the corresponding led arriving from 1 to 8 are made high i.e. when the twelfth word is recognized eighth and fourth lines are made high as shown in the table.

Word 1	Output 1
Word 2	Output 2
Word 3	Output 3
Word 4	Output 4
Word 5	Output 5
Word 6	Output 6
Word 7	Output 7
Word 8	Output 8
Word 9	Output 8 and Output 1
Word 10	Output 8 and Output 2
Word 11	Output 8 and Output 3
Word 12	Output 8 and Output 4
Word 13	Output 8 and Output 5
Word 14	Output 8 and Output 6
Word 15	Output 8 and Output 7

The circuit is provided with an octal buffer IC 74HC244 designed specially to improve both the performance and density of the bus oriented receiver. The output lines from the buffer are fed to the leds through the line driver. IC ULN2803 is used as line drivers for the sixteen output leds. Fifteen of them indicates recognition of words while one indicates an error line.

DIALER CIRCUIT DESCRIPTION

The dialer circuit uses the output lines from the recognition part to store and retrieve numbers. These numbers are used for dialing purpose. The circuit involves four stages of operation:

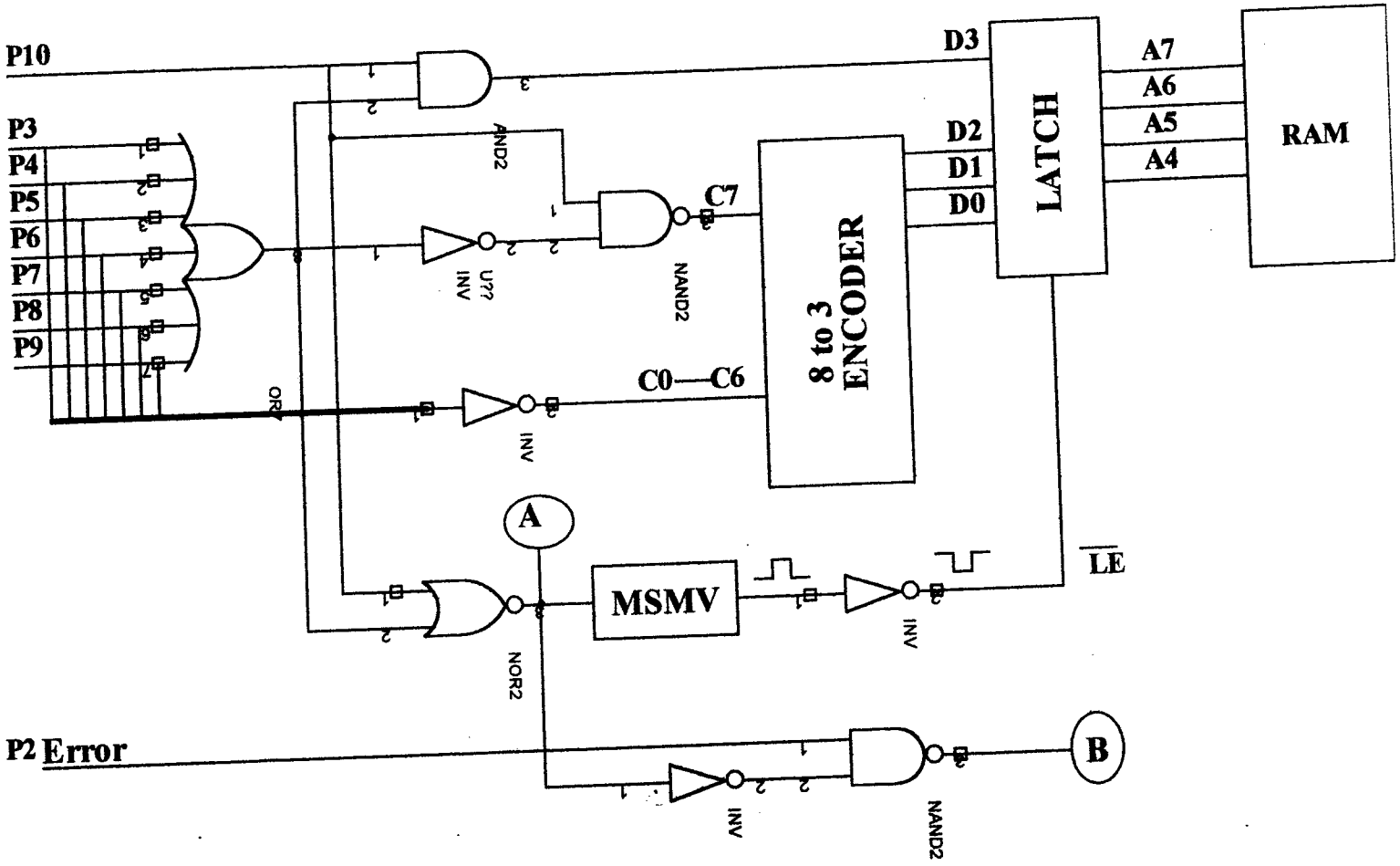
1. *THE OFFSET GENERATION*
2. *THE PHYSICAL ADDRES GENERATION*
3. *STORAGE AND RETREIVAL OF NUMBER*
4. *DIALLING OF NUMBERS*

THE OFFSET ADDRESS GENERATION:

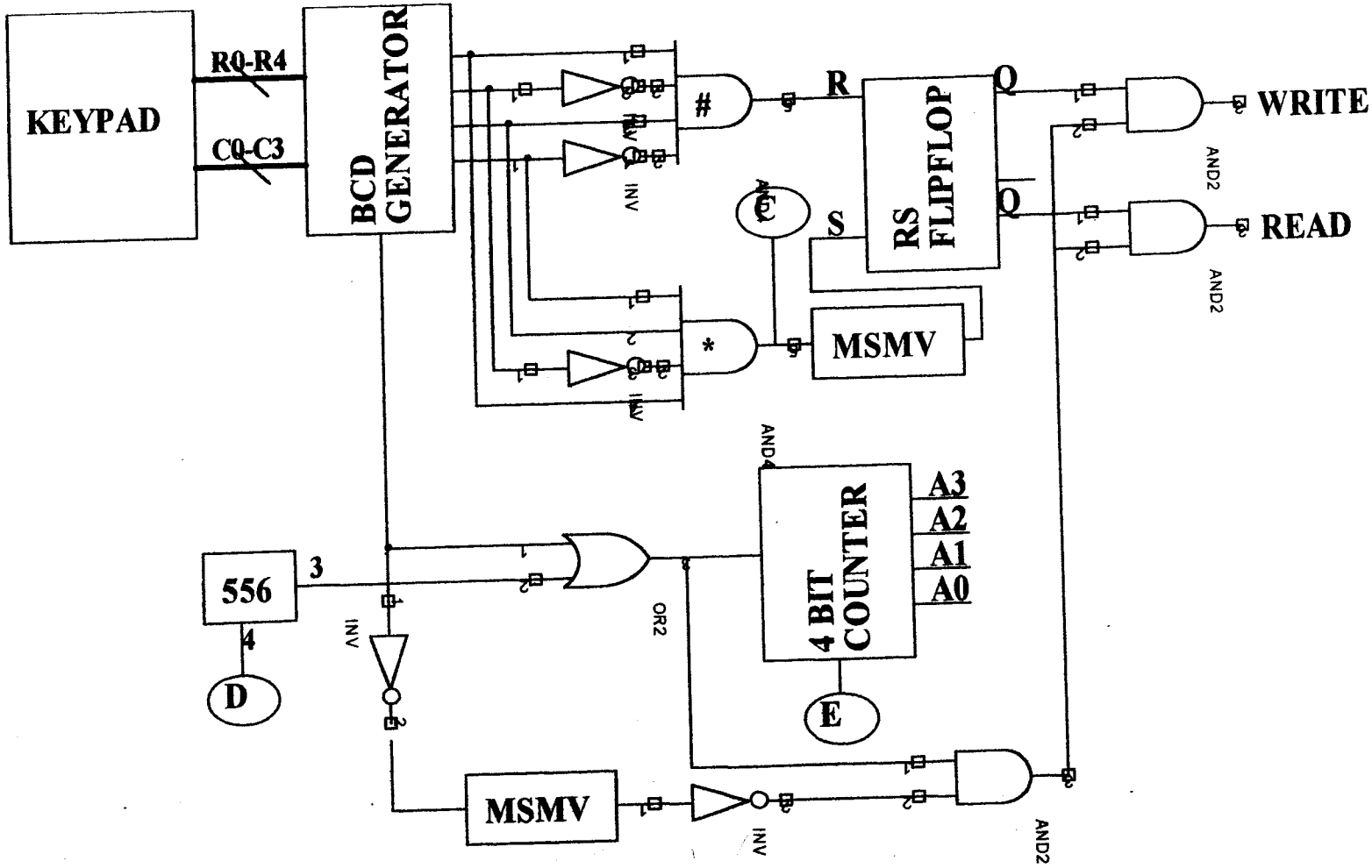
The offset address is generated to the starting address of the number being stored .The output lines of the recognition circuit is being used for this .The address corresponding to the output line that goes high is being generated.

Since the VOICE DIRECT IC has only 8 pins, the lines above eight and the eighth and the corresponding led arriving from 1 to 8 are made high i.e. when the twelfth word is recognised eighth and fourth lines are made high.

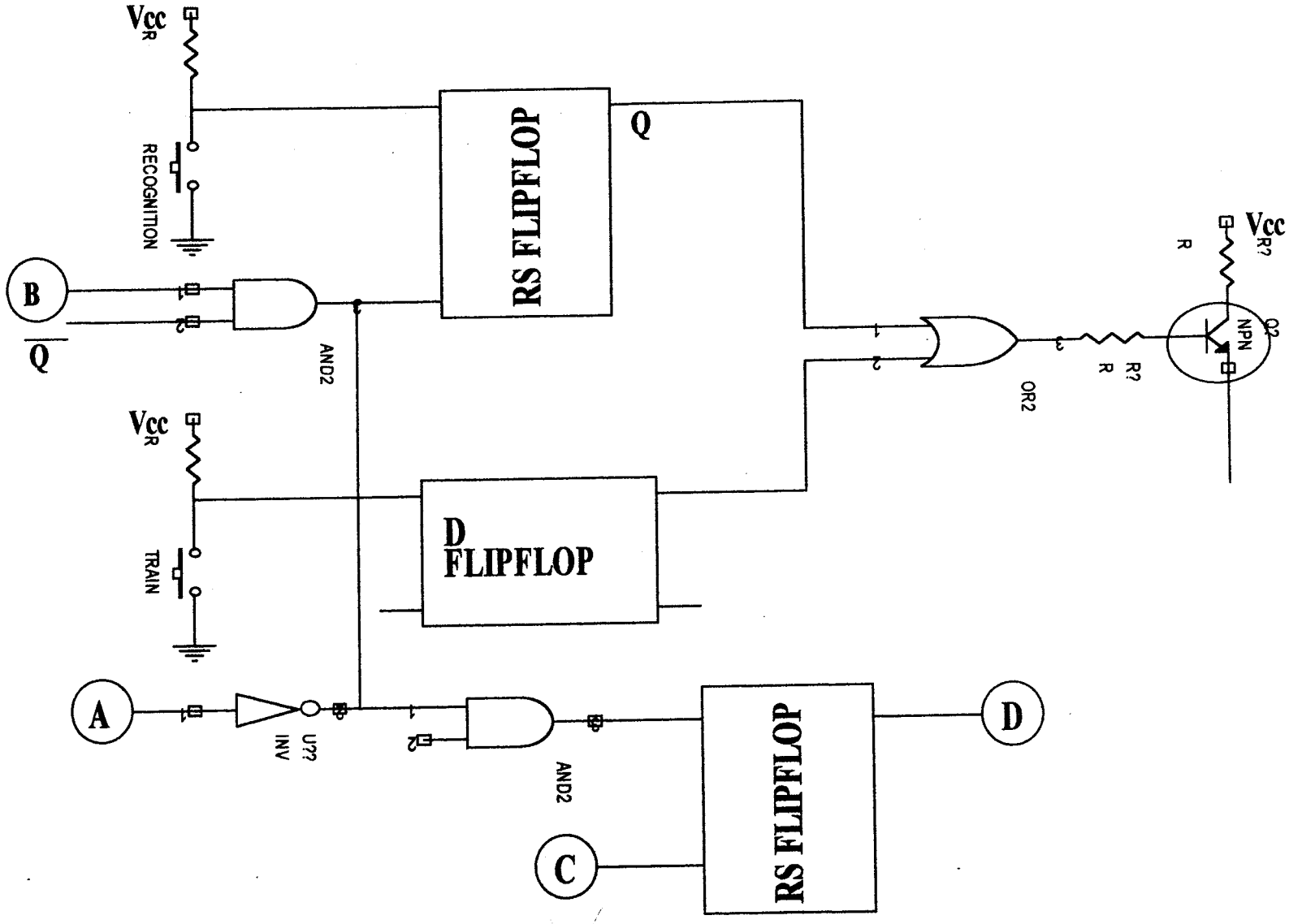
SCHEMATIC – OFFSET ADDRESS GENERATION



SCHEMATIC – PHYSICAL ADDRESS GENERATION



SCHEMATIC – DIALER SECTION



These lines are connected to the arrangement of logic gates as shown in the diagram. The input lines C_o -C_7 are thus generated for the eight to three encoder. The encoder IC74LS148 is used to generate D_0-D_2 as input to the latch IC74LS374 and is fed directly to the RAM. The lower A_4 - A_7 generates the offset address for the RAM.

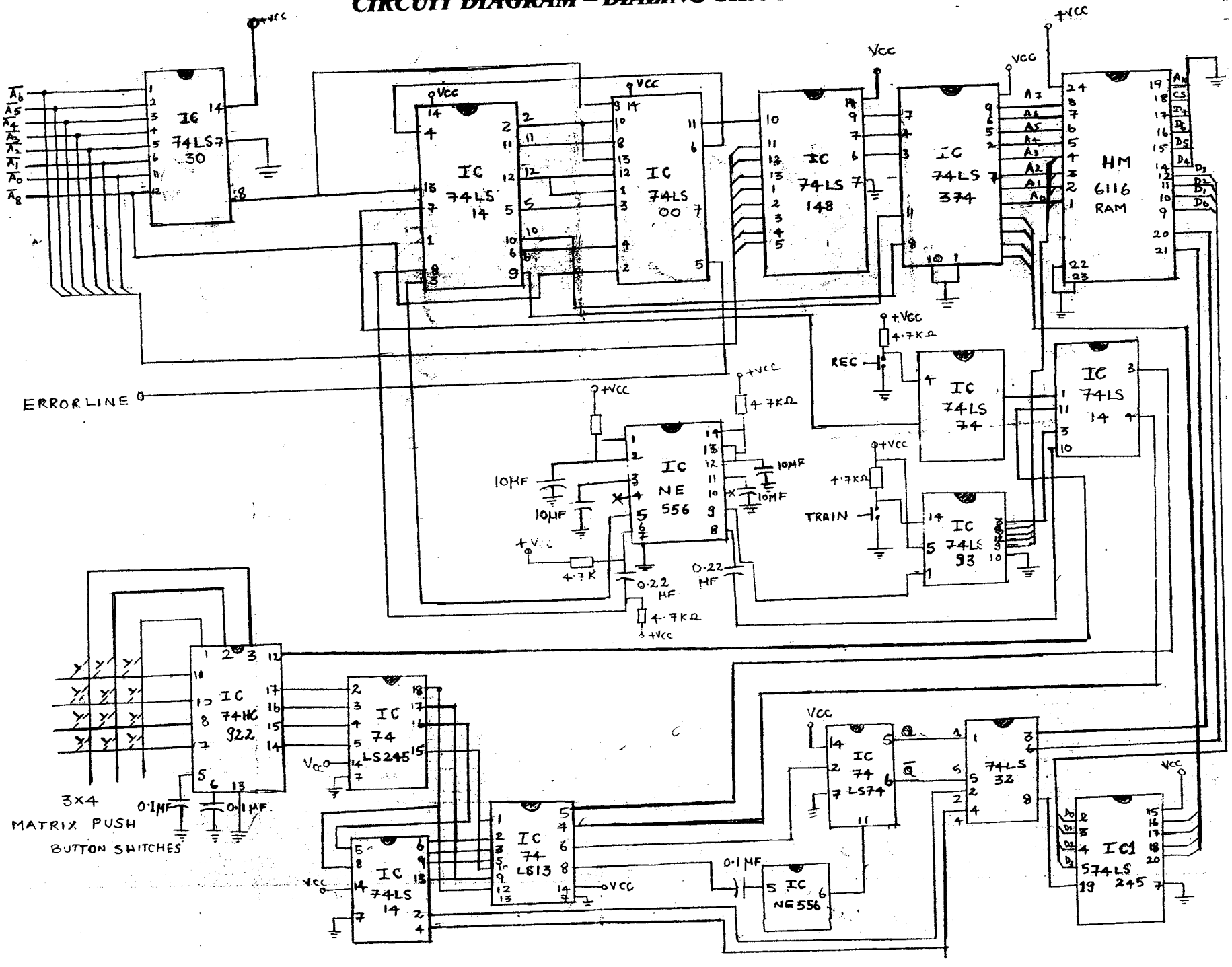
THE PHYSICAL ADDRESS GENERATION:

The physical address is generated for every number to be entered into the RAM. The offset address points to the starting location of the number to be read or written. A four bit synchronous counter 74LS93 is used to generate the physical address every time a number is entered while writing. While reading a 556 timer a clock pulse at 20 ms is fed to the counter for the generation of the physical address. Thus the number location is being generated.

STORAGE AND RETREIVAL OF DATA:

When a number is to be entered the # key in the keypad is pressed. The numbers being entered in the keypad, the BCD is generated using the IC74HC922. The comparator is used to detect the depression of the # key. When # key is detected the RS flip-flop is set and the write enable of the ram is generated. In recognition mode when a stored name is recognised, the offset address is

CIRCUIT DIAGRAM – DIALING CIRCUIT



*generated to locate the number. The IC555 generates pulse for the counter to generate the physical address .the stored number are received one by one and is fed to the dialer circuit. Another comparator is used is used to detect the depression of the * - key. When the * - key is pressed the write mode is terminated and number is read from RAM depending on the word recognized*

DIALING OF NUMBERS

Dialing of numbers is done when the stored numbers are retrieved from the RAM. A four bit binary counter increments the physical address of the RAM for retrieval of data. The clock pulse for the data is provided by the IC 555 timer. The retrieved numbers are fed to a latch trough a transceiver from the RAM. IC 785 acts as the transceiver the number is fed to the comparator for every output enable going high at the latch. The comparator is also fed with input from a counter, which generates synchronous pulses the pulses are output at the comparator until the counter value exceeds data value. Each pulse generated is being fed into a relay. The relay is coupled to the hook switch, which is made to make or break at a frequency of 15ms. This varies voltages between 48V and 10V at a particular frequency of 15ms thus dialing the equivalent number.

APPLICATION

The development of VOICE OPERATED TELEPHONE DIALER is an attempt made by us to incorporate speech recognition into the telephone instrument. The advantage of the system is its wide range of applications. The various applications are:

(i)The equipment can be implemented in the intercom connection the advantage is the ability to call other terminals by knowing only the name of the person and not necessarily the number.

(ii) The equipment can be used to store and dial frequently called numbers without pressing the keypad the stored numbers may include emergency numbers, family numbers etc.

(iii) The equipment can be used to restrict the access of certain numbers only to a particular person this is done by keeping the keypad locked and using the speaker dependent speech recognition capability to dial the stored numbers. Thus the equipment serves security purpose also.

CONCLUSION

An attempt was made to incorporate speech recognition into the telephone instrument. The objective was to dial the number of the person when his/her name is spoken out.

The circuits for recognition number storage, number retrieval and dialing are designed and implemented. The recognition of names, storage and retrieval of numbers and dialing of numbers are done successfully with display.

The advantages of the circuit are its cost effective design, easy implementation and ease of usage. The equipment applies for various applications like intercom connections, emergency number storage and speaker dependent access of numbers for security reasons.

The circuit is found to make errors while training and recognition due to the level of threshold being kept. An easy training threshold level tends to make recognition errors while excellent recognition threshold level makes training tough. The storage retrieval and dialing circuits are found to be pretty big in size, which is to be rectified by, advanced design techniques.

The equipment is thus found to have its own advantages and disadvantages. But the commercialization of such a product in immediate future will definitely be a success.

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Voice Direct IC Specifications

IC Pin Descriptions

Figure 13 - 64-pin MQFP pin assignments

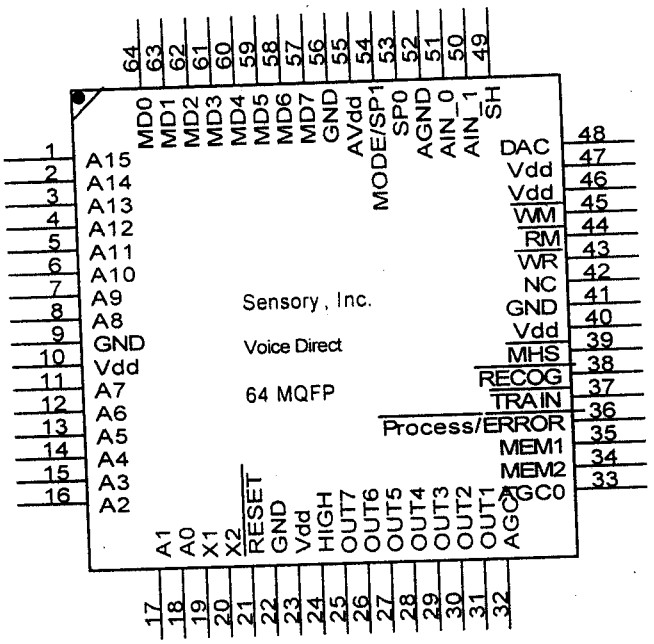


Table 11 - Pin Identification

Name	Pin	Description	I/O
A[15:0]	1-8, 11-18	External ROM Memory Address Bus	O
AGC0	33	AGC control 0. The Voice Direct controls the amplifier gain with this signal.	O
AGC1	32	AGC control 1	O
AGND	52	Analog Ground. For noise reasons, analog and digital grounds should connect together only at the RSC-164.	-
AIN0	51	Analog In, low gain. (range AGND to AVDD/2.)	I
AIN1	50	Analog In, hi gain (8X input amplitude of AIN0, same range)	I
AVDD	55	Analog Supply Voltage. For noise reasons, keep this supply independent of digital circuitry.	-
GND	9, 22, 41, 56	Digital Ground	-
MD[7:0]	57-64	External ROM Memory Data Bus	I/O
SCL	35	Serial Clock for Serial EEPROM.	O

SDA	34	Serial Data for Serial EEPROM.	O
MODE/SP1	54	The MODE pin is connected via a 100K resistor to VDD or GND to select External Host or Stand Alone Mode. This pin is also Speaker Connect1. A 32-Ohm speaker can be connected directly to this pin. (Input for MODE at power up.)	O
MHS	39	Master handshake pin	I
RECOG	38	Trigger recognition pin	I
TRAIN	37	Trigger training pin	I
PROCESS/ ERROR	36	Process pin in external host mode/error pin in stand-alone mode	O
-RESET	21	Reset	I
-RM	44	Read Memory Strobe. Can control -OE pin of External ROM.	O
SH	49	Sample and Hold. Connect a 470 pF capacitor from here to AGND.	I
DAC	48	DAC output	O
SP0	53	Speaker Connect0. A 32-Ohm speaker can be connected directly to this pin.	O
VDD	10,23,36,40, 46, 47	Digital Supply Voltage (core).	-
-WR	43	Write Result. When a recognition sequence is complete the chip will place the result on the memory data bus MD[7:0] and strobe this signal to latch the result into external devices.	O
X1, X2	19,20	Crystal connect. A 14.312 MHz crystal is connected to these pins.	O, I
NC	*42*		

Absolute Maximum Ratings

• Minimum voltage on any pin	V_{ss}-0.6V
• Maximum voltage on any pin	V_{dd}+0.6V
• Operating temperature (T_O)	-20°C to +70°C
• Soldering temperature	260°C for 10 sec
• Maximum voltage	7.5V
• Power dissipation	1W
• Storage Temperature	-65°C to +150°C
• Minimum Operating Voltage	3.5V
• Maximum Operating Voltage	5.0V

WARNING: Stressing Voice Direct beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and may affect device reliability.

DC Characteristics

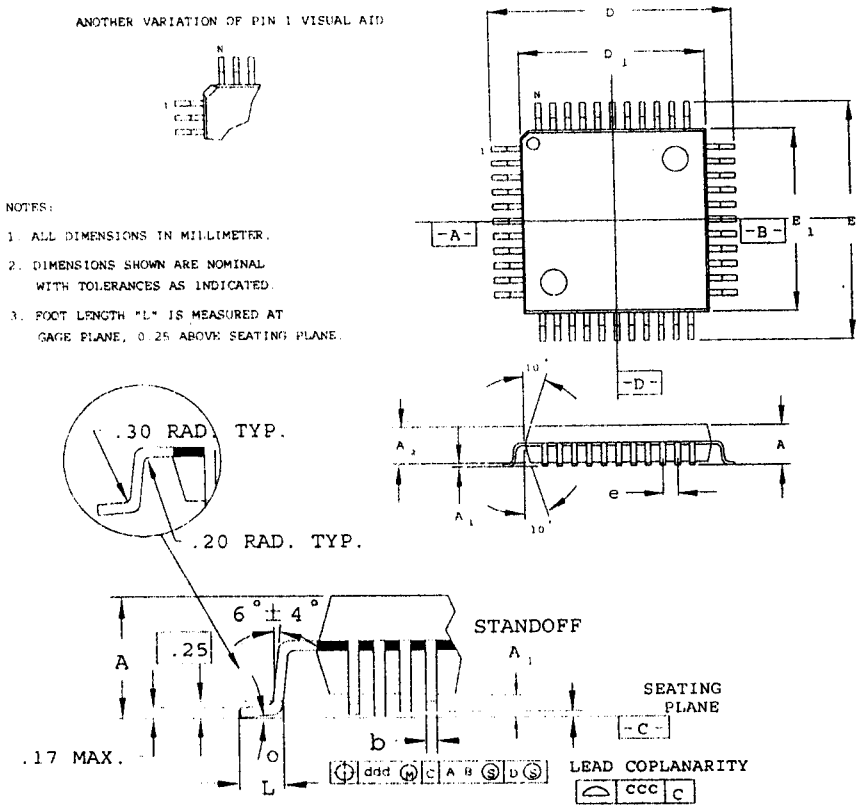
(T_O = -20°C to +70°C, Vdd = 5V)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IL}	**Input Low Voltage** XML, XMH, TE1, I/O pins XI1 RESET	 -0.1 -0.1 -0.1		 0.75 0.2 V_{DD} 0.60	 V V V	
V_{IH}	**Input High Voltage** XML, XMH, TE1, I/O pins XI1 RESET	 2.5 0.7 V_{DD} 3.0		 Vdd+0.3 Vdd+0.3 Vdd+0.3	 V V V	
V_{OL}	**Output Low Voltage** I/O pins			0.5	V	I_{OL}= 2.0 mA
V_{OH}	**Output High Voltage** I/O pins	4.0			V	I_{OH}= -2.0 mA
I_{IL}	**Input Leakage Current** XML, XMH, TE1, I/O pins XI1 RESET AIN0, AIN1, SH		 <1 <1 <1 <1	 5 5 5 5	 uA uA uA uA	 $V_{ss}<V_{pin}<V_{dd}$ $V_{ss}<V_{pin}<V_{dd}$ $V_{ss}<V_{pin}<V_{dd}$ $V_{ss}<V_{pin}<V_{dd}$
C_I	**Input Pin Capacitance**		6		pF	
I_{cc1}	**Supply Current, Operating**		7	20	mA	Hi-Z outputs
I_{cc2}	**Supply Current, Quiescent**		300	600	uA	Hi-Z outputs
R_{PU}	**Internal Pull-up Resistance, I/O pins**		4.5, 200,HiZ		kOhms	Software selected

Analog Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{ILA}	AIN0, AIN1	-0.5		0	V	
V_{IHa}	AIN0, AIN1		Avdd/ 2		V	
C_{SH}	SH- capacitance		470 ±10%	pF	V	I_{OL}= 2.0 mA
V_{DO}	DACOUT Voltage Swing	Agnd		Avdd	V	

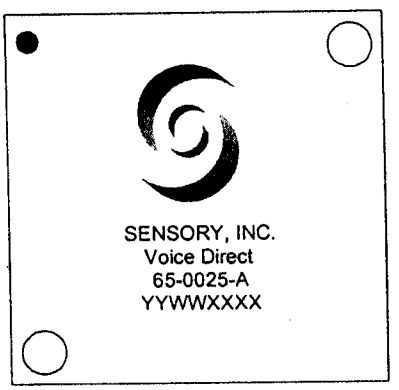
IC Metric Drawings



Package Thickness Dimensions	Tolerance	
A	M	2.35
A_1	M	0.25
A_2	±	2.00
D	±	17.20
D_1	±	14.00
E	±	17.20
E_1	±	14.00
L	±	.88
e	BASIC	.80

b	±.05	.35
θ		0-7°
ddd		.20 NOM
ccc	MAX.	.10

Marking



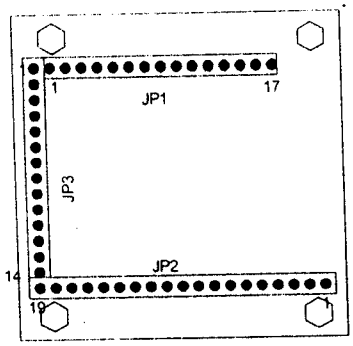
Pin #1 of: .70 mm
Height of Top Mark: Top Left
Height of Character Logo: 4.475mm
"YYWWXXXX": YYWW - Date Code (year and week)
XXXX - Sensory Identifier

IC Packaging Specification

Package: 64L QFP (14x14x2.0)
Tray: Peak Thin Bakeable, Black, Static Dissipative
84 positions.
Max Bake Temperature: 180° C.
DWG #: ND 1414 2.0 0614 8 Rev A.

Bundle (Typical): 5 + 1 (420 parts)

Module Pin Descriptions



Voice Direct™ Module

Table 12 - Pin Identification

Name	Module	Description	I/O
	JP1 - 1-16, JP2 - 1-8, 10, 13	Unused	-
-RDD	JP1 – 17	External Data Read Strobe	O
PREAMP IN	JP2 - 1	Microphone Input Connection	I
MIC BIAS	JP2 - 2	Mic Bias (Electret microphone)	I
AGND	JP2 - 3,5	Analog Ground. For noise reasons, analog and digital grounds should connect together only at the Voice Direct (VDI)	-
+5V	JP2 - 4	5 Volt (+) Power Supply Connection	-
PWM1	JP2 - 6	Pulse Width Modulator Output1 (multiplexed)	O
PWM0	JP2 - 7	Pulse Width Modulator Output0	O
DACOUT	JP2 - 8	Analog Output (unbuffered).	O
MHS	JP2 - 9	Master Handshake. Driven by host.	I
- RECOG	JP2 – 10	Recognition sensitivity selection and activate recognition	
P1.2, P1.3, P1.4,, P1.5	JP2 -14, 15, 16, 17	Reserved Port Pins, No Connections should be made here	-
- TRAIN	JP2 – 11	Training sensitivity selection and activate training	
-TALK/SOUT1	JP2 - 12	Audio talk signal. Active low during speech synthesis	O
EXP 0-4/SOUT 2-6	JP2–13, 14, 15, 16, 17	IO expansion port 0-4 *or* Stand Alone Mode output port 2 -6	
SHS/SOUT7	JP2 – 18	Slave Handshake. Driven by Voice Direct or Stand Alone Mode output port 7.	O
DATA/HIGH/ SOUT8	JP2 – 19	Serial Data between Master and Slave. Bi-directional *or* Stand Alone Mode output high *or* output port 8	I/O
-WRC	JP3 – 9	External Code Write Strobe	O
PROCESS/S_ERROR	JP3 – 10	Active low when VDI processing command *or* Stand Alone Mode error signal	
GND	JP3 - 11,12	Digital Ground, CPU core (pins 1 and 33) and I/O (pins 18and 52)	-
HOST/ STANDALONE	JP3 – 13	VDI mode selection.	
-RESET	JP3 - 14	Reset	I

National Semiconductor

LM386 Low Voltage Audio Power Amplifier

General Description

The LM386 is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 1 and 8 will increase the gain to any value up to 200.

The inputs are ground referenced while the output is automatically biased to one half the supply voltage. The quiescent power drain is only 24 milliwatts when operating from a 6 volt supply, making the LM386 ideal for battery operation.

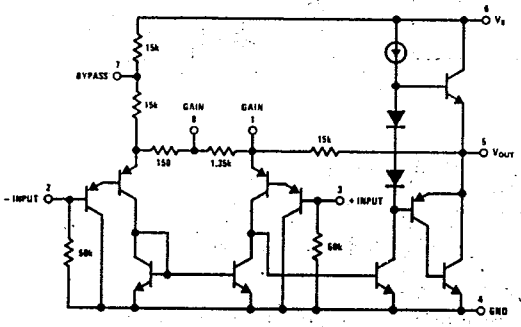
Features

- Battery operation
- Minimum external parts
- Wide supply voltage range 4V–12V or 5V–18V
- Low quiescent current drain 4 mA
- Voltage gains from 20 to 200
- Ground referenced input
- Self-centering output quiescent voltage
- Low distortion
- Eight pin dual-in-line package

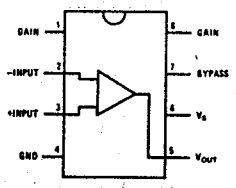
Applications

- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Line drivers
- Ultrasonic drivers
- Small servo drivers
- Power converters

Equivalent Schematic and Connection Diagrams



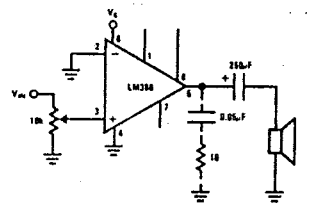
Dual-In-Line Package



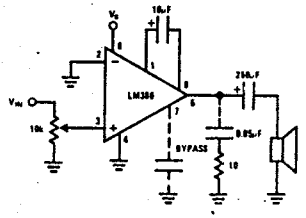
Order Number LM386N-1, LM386N-3 or LM386N-4
See NS Package N08B

Typical Applications

Amplifier with Gain = 20
Minimum Parts



Amplifier with Gain = 200



Absolute Maximum Ratings

Supply Voltage (LM386N)	15V
Supply Voltage (LM386N-4)	22V
Package Dissipation (Note 1) (LM386N-4)	1.25W
Package Dissipation (Note 2) (LM386)	660 mW
Input Voltage	±0.4V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Electrical Characteristics $T_A = 25°C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage (V_S)					
LM386		4		12	V
LM386N-4		5		18	V
Quiescent Current (I_Q)	$V_S = 6V$, $V_{IN} = 0$		4	8	mA
Output Power (P_{OUT})					
LM386N-1	$V_S = 6V$, $R_L = 8\Omega$, THD = 10%	250	325		mW
LM386N-3	$V_S = 9V$, $R_L = 8\Omega$, THD = 10%	500	700		mW
LM386N-4	$V_S = 16V$, $R_L = 32\Omega$, THD = 10%	700	1000		mW
Voltage Gain (A_V)	$V_S = 6V$, f = 1 kHz, 10μF from Pin 1 to 8		26		dB
			46		dB
Bandwidth (BW)	$V_S = 6V$, Pins 1 and 8 Open		300		kHz
Total Harmonic Distortion (THD)	$V_S = 6V$, $R_L = 8\Omega$, $P_{OUT} = 125$ mW, f = 1 kHz, Pins 1 and 8 Open		0.2		%
Power Supply Rejection Ratio (PSRR)	$V_S = 6V$, f = 1 kHz, $C_{BYPASS} = 10\mu F$, Pins 1 and 8 Open, Referred to Output		50		dB
Input Resistance (R_{IN})			50		kΩ
Input Bias Current (I_{BIAS})	$V_S = 6V$, Pins 2 and 3 Open		250		nA

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 100°C/W junction to ambient.

Note 2: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 187°C junction to ambient.

Application Hints

GAIN CONTROL

To make the LM386 a more versatile amplifier, two pins (1 and 8) are provided for gain control. With pins 1 and 8 open the 1.35 kΩ resistor sets the gain at 20 (26 dB). If a capacitor is put from pin 1 to 8, bypassing the 1.35 kΩ resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 1 to ground.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 1 to 5 (paralleling the internal 15kΩ resistor). For 6 dB effective bass boost: $R \cong 15k\Omega$, the lowest value for good stable operation is R = 10 kΩ if pin 8 is open. If pins 1 and 8 are bypassed then R as low as 2 kΩ can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater than 9.

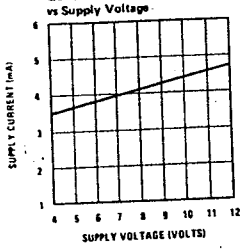
INPUT BIASING

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor. The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM386 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input, 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

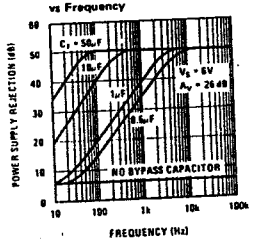
When using the LM386 with higher gains (bypassing the 1.35 kΩ resistor between pins 1 and 8) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1μF capacitor or a short to ground depending on the dc source resistance on the driven input.

Typical Performance Characteristics

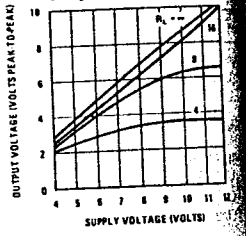
Quiescent Supply Current vs Supply Voltage



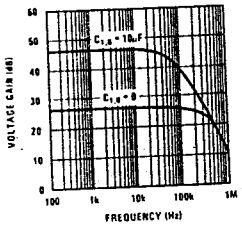
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



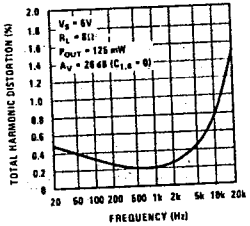
Peak-to-Peak Output Voltage Swing vs Supply Voltage



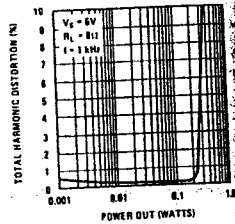
Voltage Gain vs Frequency



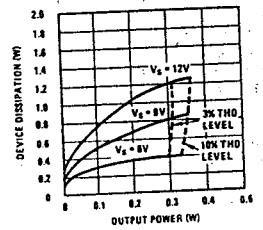
Distortion vs Frequency



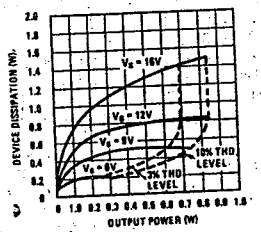
Distortion vs Output Power



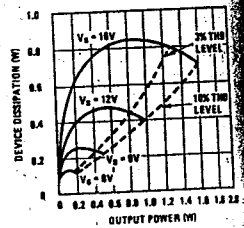
Device Dissipation vs Output Power—4Ω Load



Device Dissipation vs Output Power—8Ω Load

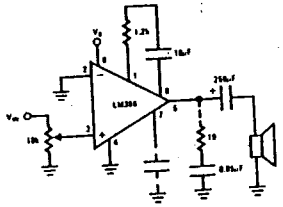


Device Dissipation vs Output Power—16Ω Load

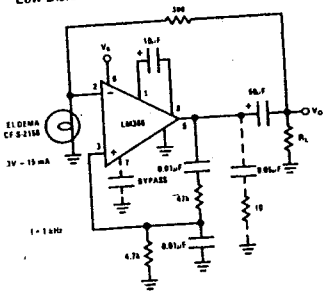


Typical Applications (Continued)

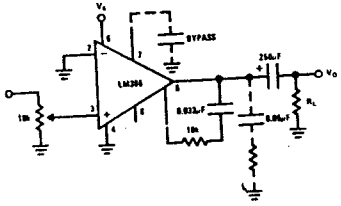
Amplifier with Gain = 50



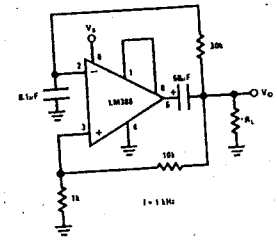
Low Distortion Power Wienbridge Oscillator



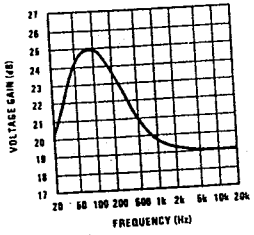
Amplifier with Bass Boost



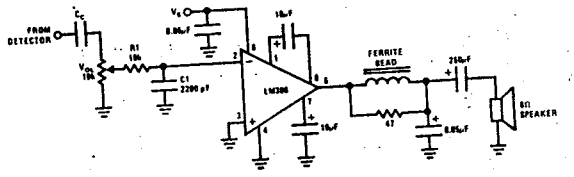
Square Wave Oscillator



Frequency Response with Bass Boost



AM Radio Power Amplifier



Note 1: Twist supply lead and supply ground very tightly.

Note 2: Twist speaker lead and ground very tightly.

Note 3: Ferrite bead is Ferroxcube K5-001-001/3B with 3 turns of wire.

Note 4: R1C1 band limits input signals.

Note 5: All components must be spaced very close to IC.

Applications Information (Continued)

generated. *Figure 12* shows a circuit configuration that will perform this function.

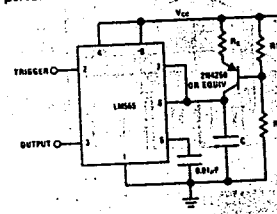


FIGURE 12.

Figure 13 shows waveforms generated by the linear ramp.

The time interval is given by:

$$T = \frac{2/3\, V_{CC}\, R_E\, (R_1 + R_2)\, C}{R_1\, V_{CC} - V_{BE}\, (R_1 + R_2)}$$

$V_{BE} \simeq 0.6V$

FIGURE 13. Linear Ramp

50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14*. The time period for the output high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is $t_2 =$

$$(R_A R_B)/(R_A + R_B)]\ C \ln \left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is $f = \frac{1}{t_1 + t_2}$

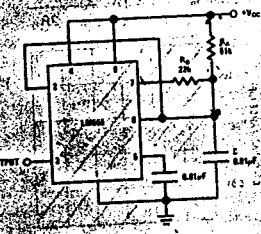


FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1μF in parallel with 1μF electrolytic.

Lower comparator storage time can be as long as 10μs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10μs minimum.

Delay time reset to output is 0.47μs typical. Minimum reset pulse width must be 0.3μs typical.

Pin 7 current switches within 30 ns of the output (pin 3) voltage

National Semiconductor

LM556/LM556C Dual Timer

General Description

The LM556 Dual timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. The 556 is a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other sharing only V_{CC} and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200 mA.

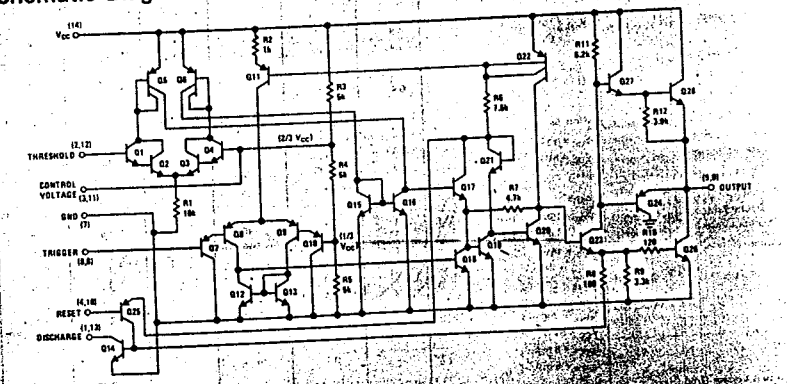
Features

- Direct replacement for SE556/NE556
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Replaces two 555 timers
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

Applications

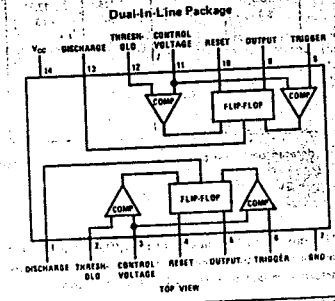
- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



Connection Diagram

Dual-In-Line Package



Order Number LM556CN
See NS Package N14A

Order Number LM556J or LM556CJ
See NS Package J14A

Absolute Maximum Ratings

Supply Voltage	+18V
Power Dissipation (Note 1)	600 mW
Operating Temperature Ranges	
LM556C	0°C to +70°C
LM556	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified)

PARAMETER	CONDITIONS	LM556			LM556C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current (Each Timer Section)	V_{CC} = 5V, R_L = ∞		3	6		3	6	mA
	V_{CC} = 15V, R_L = ∞ (Low State) (Note 2)		10	11		10	14	mA
Timing Error, Monostable								
Initial Accuracy			0.5			0.75		%
Drift With Temperature	R_A, R_B = 1k to 100k, C = 0.1μF, (Note 3)		30			50		ppm/°C
Accuracy Over Temperature			1.5			1.5		%
Drift with Supply			0.05			0.1		%/V
Timing Error, Astable								
Initial Accuracy			1.5			2.25		%
Drift With Temperature			90			150		ppm/°C
Accuracy Over Temperature			2.5			3.0		%
Drift With Supply			0.15			0.30		%/V
Trigger Voltage	V_{CC} = 15V,	4.8	5	5.2	4.5	5	5.5	V
	V_{CC} = 5V	1.45	1.67	1.9	1.25	1.67	2.0	V
Trigger Current			0.1	0.5		0.2	1.0	μA
Reset Voltage	(Note 4)	0.4	0.5	1	0.4	0.5	1	V
Reset Current			0.1	0.4		0.1	0.6	mA
Threshold Current	(Note 5)		0.03	0.1		0.03	0.1	μA
Control Voltage Level And Threshold Voltage	V_{CC} = 15V	9.6	10	10.4	9	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Pin 1, 13 Leakage Output High				100		1	100	nA
Pin 1, 13 Sat	(Note 6)							
Output Low	V_{CC} = 15V, I_L = 15 mA		150	240		180	300	mV
Output Low	V_{CC} = 4.5V, I_L = 4.5 mA		70	100		80	200	mV
Output Voltage Drop (Low)	V_{CC} = 15V							
	I_{SINK} = 10 mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50 mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100 mA		2	2.25		2	2.75	V
	I_{SINK} = 200 mA		2.5			2.5		V
	V_{CC} = 5V							
	I_{SINK} = 8 mA		0.1	0.25		0.25	0.35	V
	I_{SINK} = 5 mA							
Output Voltage Drop (High)	I_{SOURCE} = 200 mA, V_{CC} = 15V		12.5			12.5		V
	I_{SOURCE} = 100 mA, V_{CC} = 15V	13	13.3		12.75	13.3		V
	V_{CC} = 5V	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns
Matching Characteristics	(Note 7)							
Initial Timing Accuracy			0.05	0.2		0.1	2.0	%
Timing Drift With Temperature			±10			±10		ppm/°C
Drift With Supply Voltage			0.1	0.2		0.2	0.6	%/V

Note 1: For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of +150°C/W junction to ambient for both packages.

Note 2: Supply current when output high typically 1 mA less at V_{CC} = 5V.

Note 3: Tested at V_{CC} = 5V and V_{CC} = 15V.

Note 4: As reset voltage lowers, timing is inhibited and then the output goes low.

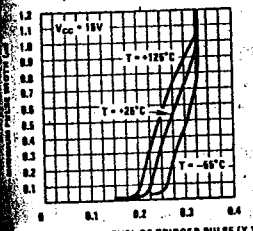
Note 5: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20 MΩ.

Note 6: No protection against excessive pin 1, 13 current is necessary providing the package dissipation rating will not be exceeded.

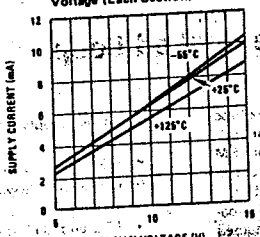
Note 7: Matching characteristics refer to the difference between performance characteristics of each timer section.

Typical Performance Characteristics

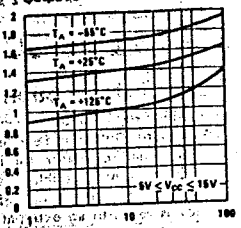
Minimum Pulse Width Required for Triggering



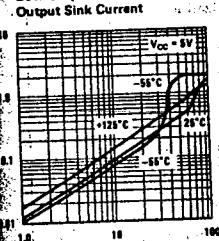
Supply Current vs Supply Voltage (Each Section)



High Output Voltage vs Output Source Current



Low Output Voltage vs Output Sink Current



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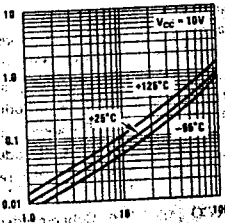
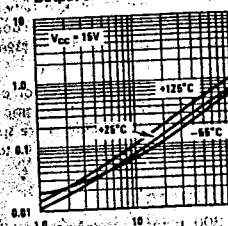
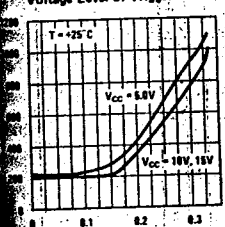


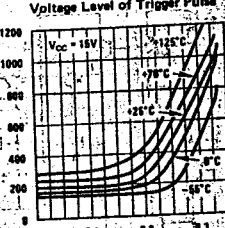
Low Output Voltage vs Output Sink Current



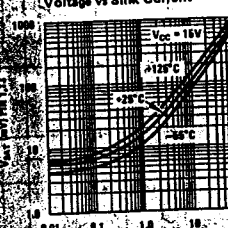
Output Propagation Delay vs Voltage Level of Trigger Pulse



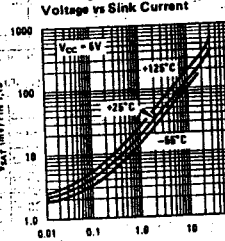
Output Propagation Delay vs Voltage Level of Trigger Pulse



Discharge Transistor (Pin 1,13) Voltage vs Sink Current



Discharge Transistor (Pin 1,13) Voltage vs Sink Current



National Semiconductor

Operational Amplifiers/Buffers

LM124/LM224/LM324, LM124A/LM224A/LM324A, LM2902
Low Power Quad Operational Amplifiers

General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5 V_{DC} power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15 V_{DC} power supplies.

Advantages

- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Internally frequency compensated for unity gain 100 dB
- Large dc voltage gain 1 MHz
- Wide bandwidth (unity gain) (temperature compensated)
- Wide power supply range:
  Single supply 3 V_{DC} to 30 V_{DC}
  or dual supplies ±1.5 V_{DC} to ±15 V_{DC}
- Very low supply current drain (800µA) — essentially independent of supply voltage (1 mW/op amp at +5 V_{DC})
- Low input biasing current 45 nA
  (temperature compensated)
- Low input offset voltage 2 mV
  and offset current 5 nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage 0 V_{DC} to V^+ − 1.5 V_{DC} swing

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Connection Diagram

Dual-In-Line Package

Order Number LM124J, LM124AJ, LM224J, LM224AJ, LM324J, LM324AJ or LM2902J
See NS Package J14A

Schematic Diagram (Each Amplifier)

Absolute Maximum Ratings

	LM124A/LM224A/LM324A	LM2902	LM124/LM224/LM324	LM124A/LM224A/LM324A	LM2902
Supply Voltage, V^+	32 V_{DC} or ±16 V_{DC}	26 V_{DC} or ±13 V_{DC}	Input Current (V_{IN} < −0.3 V_{DC}) (Note 3)	50 mA	50 mA
Differential Input Voltage	32 V_{DC}	26 V_{DC}	Operating Temperature Range		
Power Dissipation (Note 1)			LM324/LM2902	0°C to +70°C	−40°C to +85°C
Molded DIP	570 mW	570 mW	LM224/LM324A	−25°C to +85°C	
Cavity DIP	800 mW		LM224/LM2902	−55°C to +125°C	
Flat Pack	800 mW		LM124/LM124A	−55°C to +150°C	
Output Short-Circuit to GND (One Amplifier) (Note 2)	Continuous	Continuous	Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
$V^+ \leq 15$ V_{DC} and $T_A = 25°C$			Lead Temperature (Soldering, 10 seconds)	300°C	300°C

Electrical Characteristics (V^+ = +5.0 V_{DC}, Note 4)

PARAMETER	CONDITIONS	LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage	$T_A = 25°C$, (Note 5)		1	2		1	3		2	3		2	5		2	7		2	7	mVDC
Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$, $T_A = 25°C$		20	50		40	80		45	100		45	150		45	250		45	250	nADC
Offset Current	$I_{IN}(+) - I_{IN}(-)$, $T_A = 25°C$		2	10		2	15		5	30		13	±30		5	±50		5	±50	nADC
Common-Mode Range	$V^+ = 30$ V_{DC}, $T_A = 25°C$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	VDC
Current	$R_L = \infty$, $V_{CC} = 30V$, (LM2902 $V_{CC} = 26V$)		1.5	3		1.5	3		1.5	3		1.5	3		1.5	3		1.5	3	mADC
	$R_L = \infty$ On All Op Amps		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2	mADC
	Over Full Temperature Range																			
Signal Voltage	$V^+ = 15$ V_{DC} (For Large V_O Swing)	50	100		50	100		25	100		50	100		25	100		25	100		V/mV
	$R_L \geq 2$ kΩ, $T_A = 25°C$																			
Output Voltage Swing	$R_L = 2$ kΩ, $T_A = 25°C$ (LM2902 $R_L \geq 10$ kΩ)	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	VDC
Common-Mode	DC, $T_A = 25°C$	70	85		70	85		65	85		70	85		65	70		50	70		dB
Rejection Ratio																				
Power Supply	DC, $T_A = 25°C$	65	100		65	100		65	100		65	100		65	100		50	100		dP
Rejection Ratio																				
Amplifier-to-Amplifier Coupling (Note 8)	$f = 1$ kHz to 20 kHz, $T_A = 25°C$ (Input Referred)		−120			−120			−120			−120			−120			−120		dB
Output Current	Source	$V_{IN}^+ = 1$ V_{DC}, $V_{IN}^- = 0$ V_{DC}, $V^+ = 15$ V_{DC}, $T_A = 25°C$	20	40		20	40		20	40		20	40		20	40		20	40		mADC
	Sink	$V_{IN}^- = 1$ V_{DC}, $V_{IN}^+ = 0$ V_{DC}, $V^+ = 15$ V_{DC}, $T_A = 25°C$	10	20		10	20		10	20		10	20		10	20		10	20		mADC
		$V_{IN}^- = 1$ V_{DC}, $V_{IN}^+ = 0$ V_{DC}, $T_A = 25°C$, $V_O = 200$ mVDC	12	50		12	50		12	50		12	50		12	50		12	50		µADC
Short Circuit to Ground	$T_A = 25°C$, (Note 2)		40	60		40	60		40	60		40	60		40	60		40	60		mADC

ctrical Characteristics (Continued)

ARAMETER	CONDITIONS	LM124A MIN	LM124A TYP	LM124A MAX	LM224A MIN	LM224A TYP	LM224A MAX	LM324A MIN	LM324A TYP	LM324A MAX	LM124/LM224 MIN	LM124/LM224 TYP	LM124/LM224 MAX	LM324 MIN	LM324 TYP	LM324 MAX	LM2902 MIN	LM2902 TYP	LM2902 MAX	UNITS
				4			4			5			±7			±9			±10	mV_{DC}
it Offset Voltage	(Note 5)		7	20		7	20		7	30		7			7			7		$\mu V/^\circ C$
it Offset Voltage 1	$R_S = 0\Omega$			30			30			75			±100			±150		45	±200	nA_{DC}
ut Offset Current	$I_{IN(+)} - I_{IN(-)}$		10	200		10	200		10	300		10			10			10		$pA_{DC}/^\circ C$
ut Offset Current ft																				
ut Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	100		40	200		40	300		40	500		40	500	nA_{DC}
ut Common-Mode ltage Range (Note 7)	$V^+ = 30\ V_{DC}$	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	V_{DC}
rge Signal Voltage ain	$V^+ = +15\ V_{DC}$ (For Large V_O Swing) $R_L \geq 2\ k\Omega$	25			25			15			25			15			15			V/mV
tput Voltage Swing V_{OH}	$V^+ = +30\ V_{DC}$, $R_L = 2\ k\Omega$	26			26			26			26			26			22			V_{DC}
	$R_L \geq 10\ k\Omega$	27	28		27	28		27	28		27	28		27	28		23	24		V_{DC}
	$V^+ = 5\ V_{DC}$, $R_L \leq 10\ k\Omega$		5	20		5	20		5	20		5	20		5	20		5	100	mV_{DC}
V_{OL}																				
utput Current Source	$V_{IN}^+ = +1\ V_{DC}$, $V_{IN}^- = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
Sink	$V_{IN}^- = +1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	15		10	15		5	8		5	8		5	8		5	8		mA_{DC}
				32			32			32			32			32			26	V_{DC}
ifferential Input oltage	(Note 7)																			

ote 1: For operating at high temperatures, the LM324/LM324A, LM2902 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device ldered in a printed circuit board, operating in a still air ambient. The LM224/LM224A and LM124/LM124A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all ur amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

ote 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply oltage in excess of +15 V_{DC}, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

ote 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby cting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ oltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, gain returns to a value greater than −0.3 V_{DC} (at 25°C).

ote 4: These specifications apply for $V^+ = +5\ V_{DC}$ and −55°C ≤ T_A ≤ +125°C, unless otherwise stated. With the LM224/LM224A, all temperature specifications are limited to −40°C ≤ T_A ≤ +85°C. LM324A temperature specifications are limited to 0°C ≤ T_A ≤ +70°C, and the LM2902 specifications are limited to −40°C ≤ T_A ≤ +85°C.

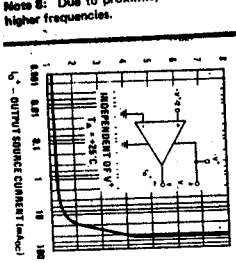
Note 5: $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from 5 V_{DC} to 30 V_{DC}; and over the full input common-mode range (0 V_{DC} to $V^+ - 1.5\ V_{DC}$).

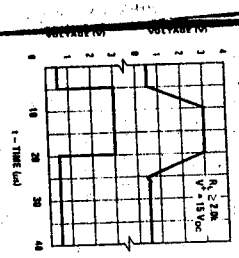
Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

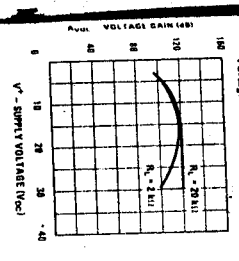
Note 7: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is $V^+ - 1.5V$, but either or both inputs can go to +32 V_{DC} without damage (+26 V_{DC} for LM2902).

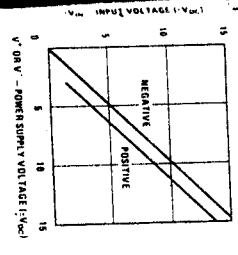
Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.

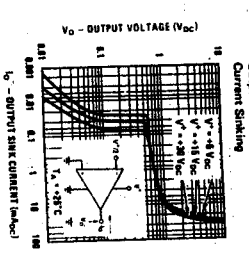
ypical Performance Characteristics

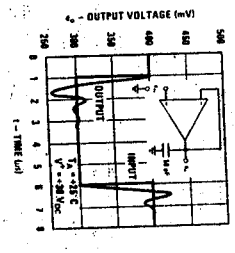


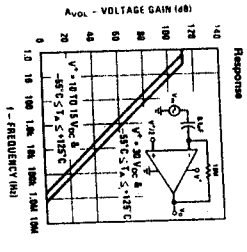


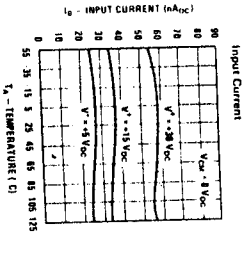


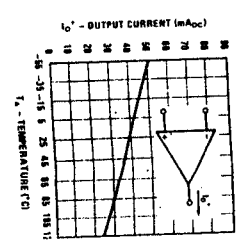


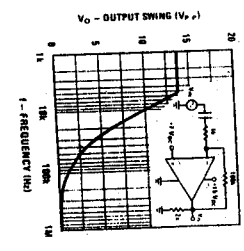


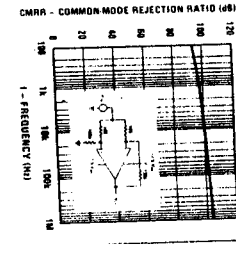


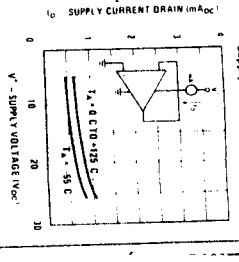












TYPES SN54ALS244A, SN54AS244, SN74ALS244A, SN74AS244
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982–REVISED DECEMBER 1983

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce DC Loading
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

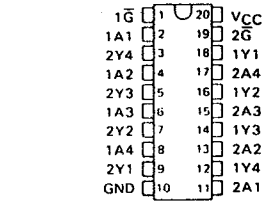
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ALS240A, 'ALS241A, 'AS240, and 'AS241, these devices provide the choice of selected combinations of inverting outputs, symmetrical G (active-low input control) inputs, and complementary G and G inputs.

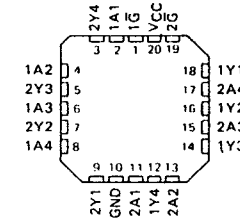
The –1 version of the SN74ALS244A is identical to the standard version except that the recommended maximum I_{OL} is increased to 48 milliamperes. There is no –1 version of the SN54ALS244A.

The SN54ALS244A and SN54AS244 are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS244A and SN74AS244 are characterized for operation from 0°C to 70°C.

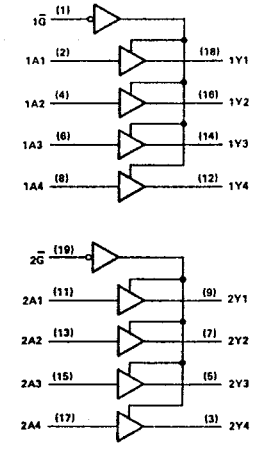
SN54ALS244A, SN54AS244 . . . J PACKAGE
SN74ALS244A, SN74AS244 . . . N PACKAGE
(TOP VIEW)



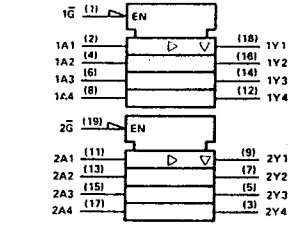
SN54ALS244A, SN54AS244 . . . FH PACKAGE
SN74ALS244A, SN74AS244 . . . FN PACKAGE
(TOP VIEW)



logic diagram (positive logic)



logic symbol



Pin numbers shown are for J and N packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS244A . . . . . −55°C to 125°C
SN74ALS244A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS244A			SN74ALS244A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS244A-1 only.

2 ALS AND AS CIRCUITS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS244A			SN74ALS244A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V (I_{OL} = 48 mA for −1 version)	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	µA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.1			−0.1		mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		9	15		9	15	mA
		Outputs low		15	24		15	24	
		Outputs disabled		17	27		17	27	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS244A		SN74ALS244A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	13	3	10	ns
t_{PHL}			3	13	3	10	
t_{PZH}	$\overline{G}$	Y	7	25	7	20	ns
t_{PZL}			7	25	7	20	
t_{PHZ}	$\overline{G}$	Y	2	12	2	10	ns
t_{PLZ}			3	18	3	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

'90A, 'L90 ... DECADE COUNTERS

'92A, 'L92 ... DIVIDE-BY-TWELVE COUNTERS

'93A, 'L93 ... 4-BIT BINARY COUNTERS

	TYPICAL POWER DISSIPATION
'90A, 'L90	145 mW
'LS90	20 mW
'92A, '93A	45 mW
'LS92, 'LS93	130 mW
'L93	45 mW
	16 mW

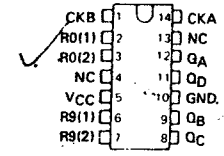
description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A, 'L90, and 'LS90, divide-by-six for the '92A and 'LS92, and divide-by-eight for the '93A, 'L93, and 'LS93.

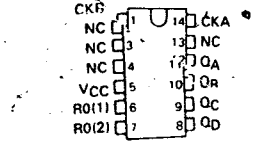
All of these counters have a gated zero reset and the '90A, 'L90, and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the CKB input is connected to the Q_A output. The input count pulses are applied to CKA input and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A, 'L90, or 'LS90 counters by connecting the Q_D output to the CKA input and applying the input count to the CKB input which gives a divide-by-ten square wave at output Q_A.

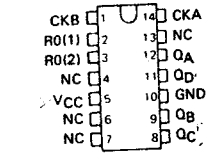
SN5490A, SN54LS90 . . . J OR W PACKAGE
SN54L90 . . . J PACKAGE
SN7490A . . . J OR N PACKAGE
SN74LS90 . . . D, J OR N PACKAGE
(TOP VIEW)



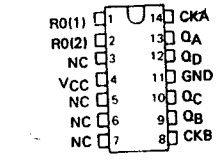
SN54LS92A, SN54LS92 . . . J OR W PACKAGE
SN7492A . . . J OR N PACKAGE
SN74LS92 . . . D, J OR N PACKAGE
(TOP VIEW)



SN5493A, SN54LS93 . . . J OR W PACKAGE
SN7493A . . . J OR N PACKAGE
SN74LS93 . . . D, J OR N PACKAGE
(TOP VIEW)



SN54L93 . . . J PACKAGE
(TOP VIEW)



NC – No internal connection

For new chip carrier design, use 'LS290, 'LS292, and 'LS293.

'90A, 'L90, 'LS90
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'90A, 'L90, 'LS90
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'92A, 'LS92
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

'90A, 'L90, 'LS90
RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

'92A, 'LS92, '93A, 'L93, 'LS93
RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

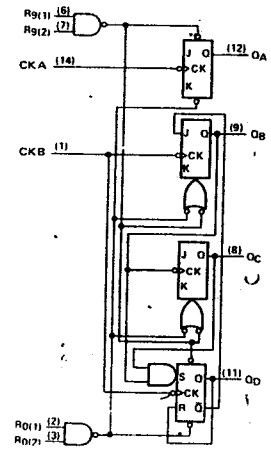
'93A, 'L93, 'LS93
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	
5	L	H	L	
6	L	H		
7	L	H		
8	H	L		
9	H	L		
10	H	L		
11	H	L		
12	H	H		
13	H	H		
14	H	H		
15	H			

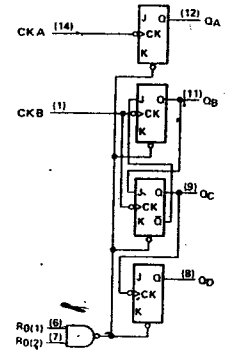
NOTES: A. Output Q_A is connected to input CKB for BCD count.
B. Output Q_D is connected to input CKA for bi-quinary count.
C. Output Q_A is connected to input CKB.
D. H = high level, L = low level, X = irrelevant

logic diagrams

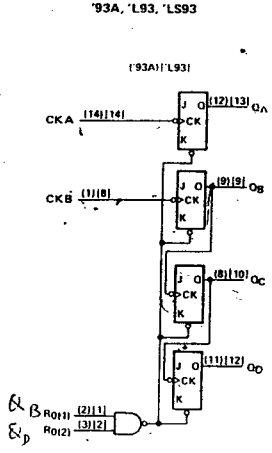
'90A, 'L90, 'LS90



'92A, 'LS92



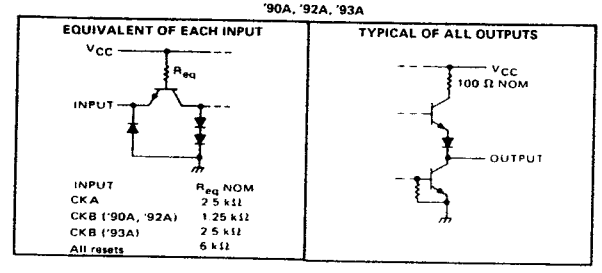
'93A, 'L93, 'LS93



The J and K inputs shown without connection are for reference only and are functionally at a high level.
Pin numbers shown in ( ) are for the 'LS93 and '93A and pin numbers shown in [ ] are for the 54L93.

schematics of inputs and outputs

'90A, '92A, '93A



recommended operating conditions

			SN54LS74A			SN74LS74A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		25	0		25	MHz
t_w	Pulse duration	CLK high	25			25			ns
		$\overline{PRE}$ or $\overline{CLR}$ low	25			25			
t_{su}	Setup time-before CLK↑	High-level data	20			20			ns
		Low-level data	20			20			
t_h	Hold time-data after CLK↑		5			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS74A			SN74LS74A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = −0.4 mA	V_{IH} = 2 V,	V_{IL} = MAX,	2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC} = MIN, I_{OL} = 4 mA	V_{IL} = MAX,	V_{IH} = 2 V,		0.25	0.4		0.25	0.4	V
		V_{CC} = MIN, I_{OL} = 8 mA	V_{IL} = MAX,	V_{IH} = 2 V,					0.35	0.5	
I_I	D or CLK	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
	$\overline{CLR}$ or $\overline{PRE}$						0.2			0.2	
I_{IH}	D or CLK	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
	$\overline{CLR}$ or $\overline{PRE}$						40			40	
I_{IL}	D or CLK	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
	$\overline{CLR}$ or $\overline{PRE}$						−0.8			−0.8	
I_{OS}§		V_{CC} = MAX,	See Note 4		−20		−100	−20		−100	mA
I_{CC}		V_{CC} = MAX,	See Note 2			4	8		4	8	mA

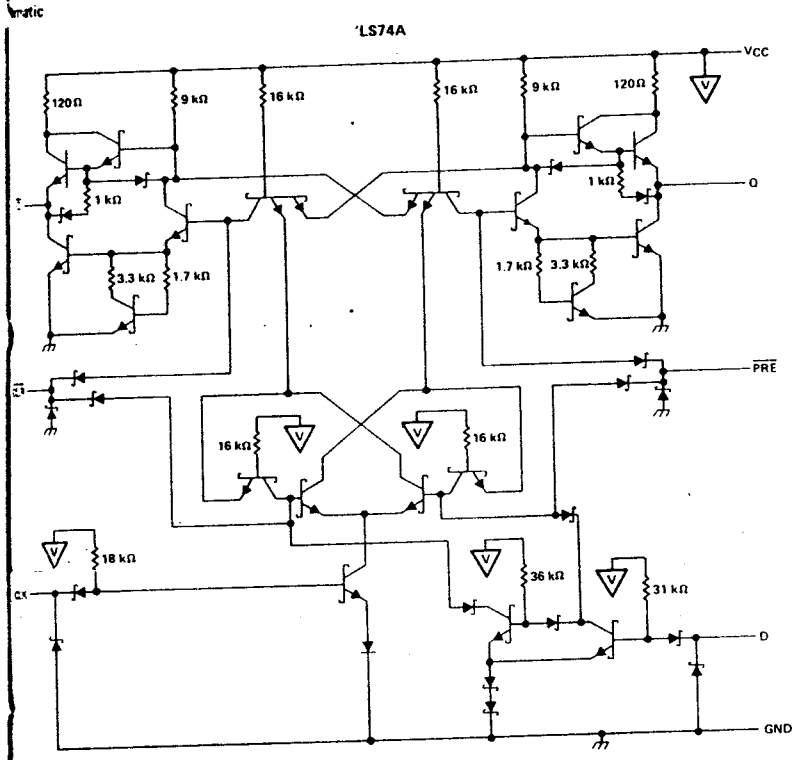
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.
NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 2 kΩ, C_L = 15 pF	25	33		MHz
t_{PLH}	$\overline{CLR}$, $\overline{PRE}$ or CLK	Q or $\overline{Q}$			13	25	ns
t_{PHL}					25	40	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

matic



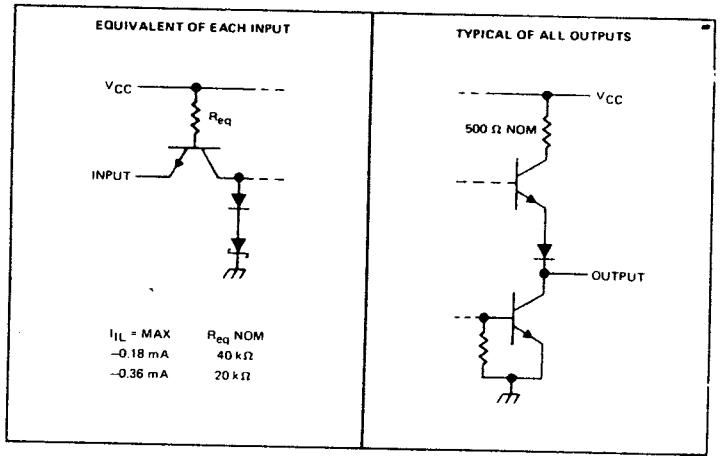
olute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '74, 'H74, 'L74, 'S74 . . . . . 5.5 V
'LS74A . . . . . 7 V
Operating free-air temperature range: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

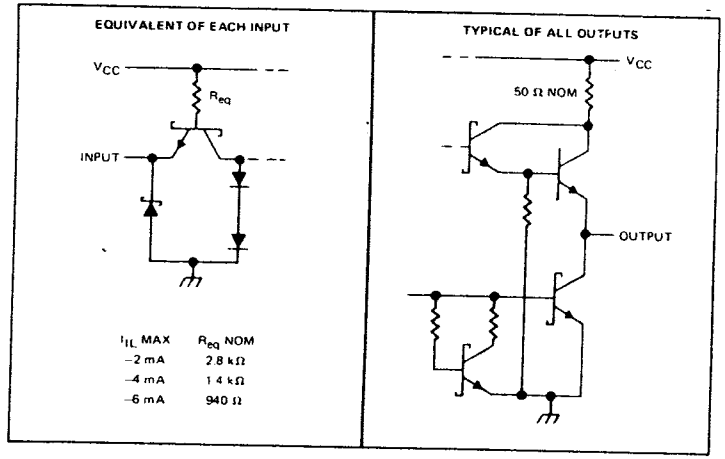
E 1: Voltage values are with respect to network ground terminal.

schematics of inputs and outputs (continued)

'L74



'S74



recommended operating conditions

		SN54S74			SN74S74			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
VCC Supply voltage		4.5	5	5.5	4.75	5	5.25	V
VIH High-level input voltage		2			2			V
VIL Low-level input voltage				0.8			0.8	V
IOH High-level output current				−1			−1	mA
IOL Low-level output current				20			20	mA
tw Pulse duration	CLK high	6			6			ns
	CLK low	7.3			7.3			
	CLR or PRE low	7			7			
tsu Setup time, before CLK ↑	High-level data	3			3			ns
	Low-level data	3			3			
th Input hold time - data after CLK ↑		2			2			ns
TA Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54S74 MIN	SN54S74 TYP‡	SN54S74 MAX	SN74S74 MIN	SN74S74 TYP‡	SN74S74 MAX	UNIT
VIK		VCC = MIN, II = −18 mA			−1.2			−1.2	V
VOH		VCC = MIN, VIH = 2 V, VIL = 0.8 V, IOH = −1 mA	2.5	3.4		2.7	3.4		V
VOL		VCC = MIN, VIH = 2 V, VIL = 0.8 V, IOL = 20 mA			0.5			0.5	V
II		VCC = MAX, VI = 5.5 V			1			1	mA
IIH	D	VCC = MAX, VI = 2.7 V			50			50	mA
	CLR				150			150	
	PRE or CLK				100			100	
IIL	D	VCC = MAX, VI = 0.5 V			−2			−2	mA
	CLR*				−6			−6	
	PRE*				−4			−4	
	CLK				−4			−4	
IOS		VCC = MAX			−100	−40		−100	mA
ICC		VCC = MAX, See Note 2			25			25	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at VCC = 5 V, TA = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.
¶ ICC is tested with preset high and preset is tested with clear high.
NOTE 2: All outputs open, ICC is measured with the Q and Q̄ outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, VCC = 5 V, TA = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
fmax			RL = 280 Ω, CL = 15 pF	75	110		MHz
tPLH	PRE or CLR	Q or Q̄			4	6	ns
tPHL	PRE or CLR (CLK high)	Q̄ or Q			9	13.5	ns
tPLH	PRE or CLR (CLK low)	Q̄ or Q			5	8	ns
tPHL	CLK	Q or Q̄			6	9	ns
					6	9	ns

See General Information Section for load circuits and voltage waveforms

TYPES SN54LS373, SN54LS374, SN54S373, SN54S374, SN74LS373, SN74LS374, SN74S373, SN74S374
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

OCTOBER 1975 – REVISED APRIL 1985

- Choice of 8 Latches or 8 D-Type Flip-Flops In a Single Package
- 3-State Bus-Driving Outputs
- Full Parallel-Access for Loading
- Buffered Control Inputs
- Clock/Enable Input Has Hysteresis to Improve Noise Rejection ('S373 and 'S374)
- P-N-P Inputs Reduce D-C Loading on Data Lines ('S373 and 'S374)

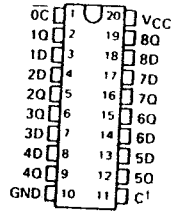
'LS373, 'S373
FUNCTION TABLE

OUTPUT ENABLE	ENABLE LATCH	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

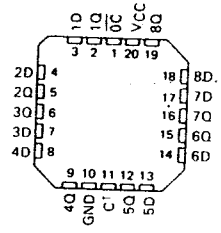
'LS374, 'S374
FUNCTION TABLE

OUTPUT ENABLE	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

SN54LS373, SN54LS374, SN54S373, SN54S374 . . . J PACKAGE
SN74LS373, SN74LS374, SN74S373, SN74S374 . . . DW, J OR N PACKAGE
(TOP VIEW)



SN54LS373, SN54LS374, SN54S373, SN54S374 . . . FK PACKAGE
SN74LS373, SN74LS374, SN74S373, SN74S374 . . . FN PACKAGE
(TOP VIEW)



'C for 'LS373 and 'S373; CLK for 'LS374 and 'S374

description

These 8-bit registers feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'LS373 and 'S373 are transparent D-type latches meaning that while the enable (C) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS' . . . . . −55°C to 125°C
SN74LS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1. Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54LS'			SN74LS'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{OH}	High-level output voltage				5.5			5.5	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Pulse duration	CLK high	15			15			ns
		CLK low	15			15			
t_{su}	Data setup time	'LS373	5↓			5↓			ns
		'LS374	20↑			20↑			
t_h	Data hold time	'LS373	20↓			20↓			ns
		'LS374†	0↑			0↑			
T_A	Operating free-air temperature		−55		125	0		70	°C

† The t_h specification applies only for data frequency below 10 MHz. Designs above 10 MHz should use a minimum of 5 ns.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS' MIN	SN54LS' TYP‡	SN54LS' MAX	SN74LS' MIN	SN74LS' TYP‡	SN74LS' MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = MAX		2.4	3.4		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.7 V				20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.4 V				−20			−20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX, Output control at 4.5 V	'LS373		24	40		24	40	mA
			'LS374		27	40		27	40	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		'LS373 MIN	'LS373 TYP	'LS373 MAX	'LS374 MIN	'LS374 TYP	'LS374 MAX	UNIT
f_{max}			C_L = 45 pF, R_L = 667 Ω, See Notes 2 and 3					35	50		MHz
t_{PLH}	Data	Any Q				12	18				ns
t_{PHL}						12	18				
t_{PLH}	Clock or enable	Any Q				20	30		15	28	ns
t_{PHL}						18	30		19	28	
t_{PZH}	Output Control	Any Q				15	28		20	26	ns
t_{PZL}						25	36		21	28	
t_{PHZ}	Output Control	Any Q	C_L = 5 pF, R_L = 667 Ω, See Note 3	SN54		28	32		28	32	ns
				SN74		15	25		15	28	
t_{PLZ}	Output Control	Any Q				12	20		12	20	ns

NOTES 2. Maximum clock frequency is tested with all outputs loaded.
3. See General Information Section for load circuits and voltage waveforms.

f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{PZH} = output enable time to high level
t_{PZL} = output enable time to low level
t_{PHZ} = output disable time from high level
t_{PLZ} = output disable time from low level

description (continued)

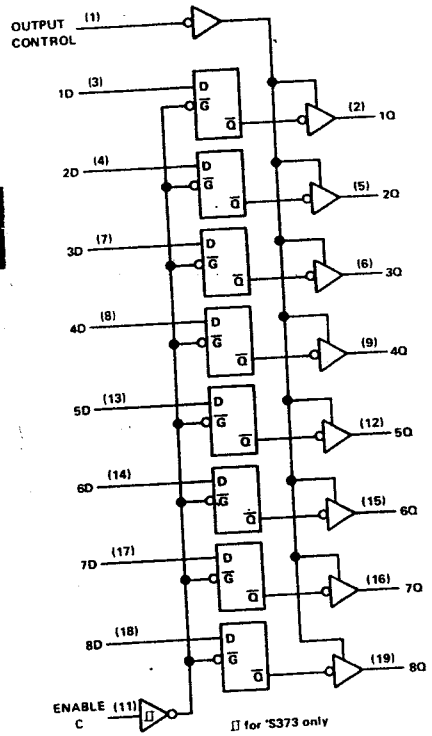
The eight flip-flops of the 'LS374 and 'S374 are edge-triggered D type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were setup at the D inputs.

Schmitt-trigger buffered inputs at the enable/clock lines of the 'S373 and 'S374 devices, simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

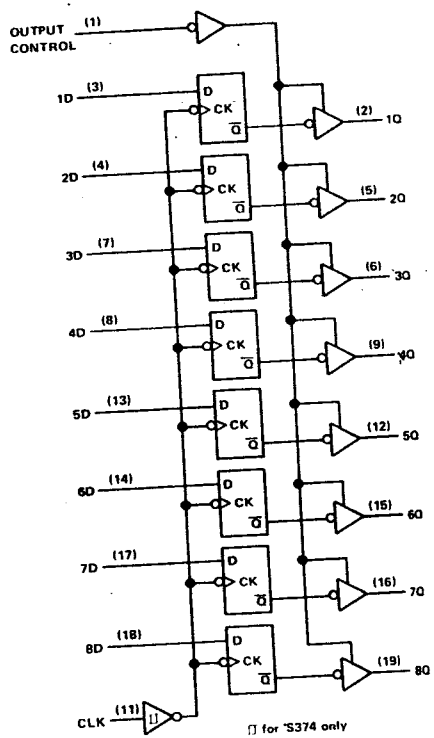
logic diagrams

'LS373, 'S373
TRANSPARENT LATCHES



† for 'S373 only

'LS374, 'S374
POSITIVE-EDGE-TRIGGERED FLIP-FLOPS

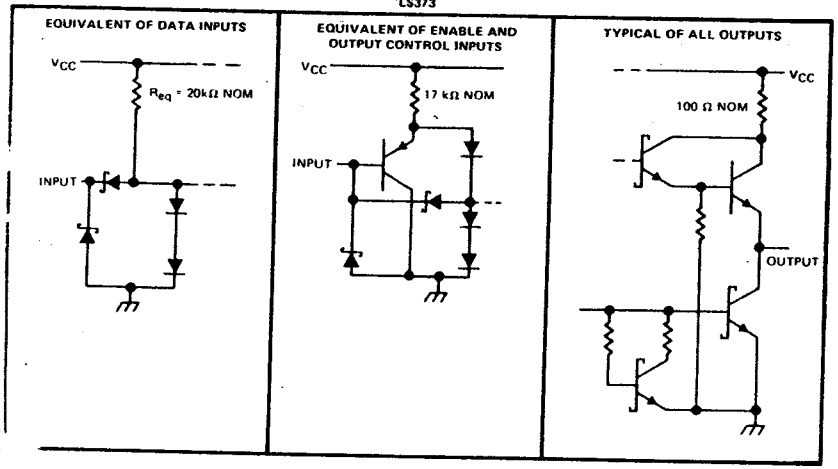


† for 'S374 only

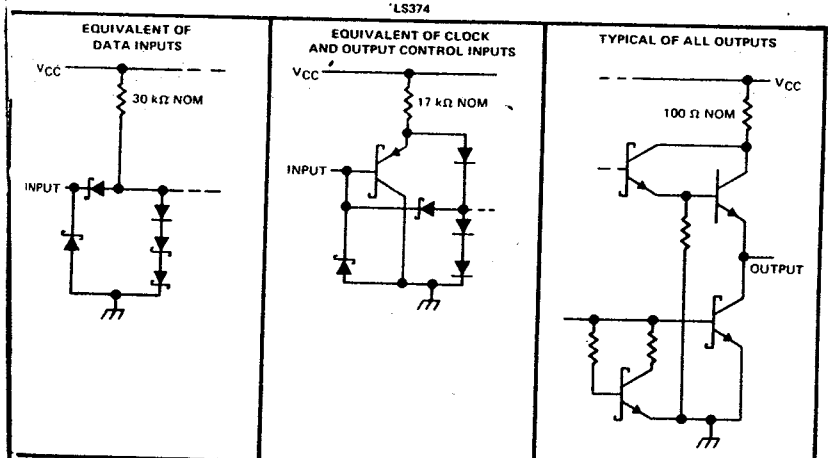
Pin numbers shown on logic notation are for DW, J or N packages.

schematic of inputs and outputs

'LS373



'LS374

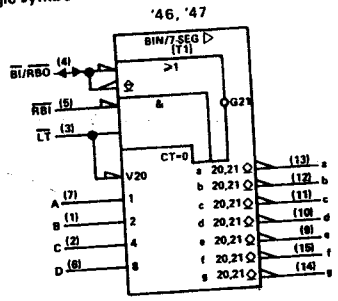


- All Circuit Types Feature Lamp Intensity Modulation Capability

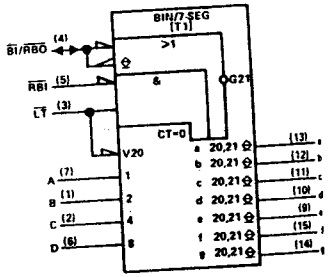
TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION	PACKAGES
	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE		
SN5446A	low	open-collector	40 mA	30 V	320 mW	J, W
SN5447A	low	open-collector	40 mA	15 V	320 mW	J, W
SN5448	high	2-kΩ pull-up	6.4 mA	5.5 V	265 mW	J, W
SN5449	high	open-collector	10 mA	5.5 V	165 mW	W
SN54L46	low	open-collector	20 mA	30 V	160 mW	J
SN54L47	low	open-collector	20 mA	15 V	160 mW	J
SN54LS47	low	open-collector	12 mA	15 V	35 mW	J, W
SN54LS48	high	2-kΩ pull-up	2 mA	5.5 V	125 mW	J, W
SN54LS49	high	open-collector	4 mA	5.5 V	40 mW	J, W
SN7446A	low	open-collector	40 mA	30 V	320 mW	J, N
SN7447A	low	open-collector	40 mA	15 V	320 mW	J, N
SN7448	high	2-kΩ pull-up	6.4 mA	5.5 V	265 mW	J, N
SN74LS47	low	open-collector	24 mA	15 V	35 mW	J, N
SN74LS48	high	2-kΩ pull-up	6 mA	5.5 V	125 mW	J, N
SN74LS49	high	open-collector	8 mA	5.5 V	40 mW	J, N

logic symbols

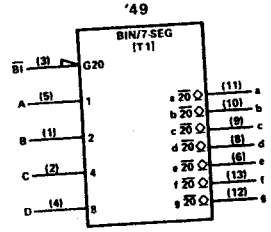
'46, '47



'48



'49



Pin numbers shown on logic notation are for D, J or N packages.

TEXAS INSTRUMENTS
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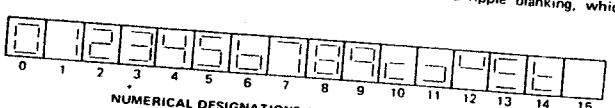
description

The '46A, 'L46, '47A, 'L47, and 'LS47 feature active-low outputs designed for driving common-anode VLEDs or incandescent indicators directly, and the '48, '49, 'LS48, 'LS49 feature active-high outputs for driving lamp buffers or common-cathode VLEDs. All of the circuits except '49 and 'LS49 have full ripple-blanking input/output controls and a lamp test input. The '49 and 'LS49 circuits incorporate a direct blanking input. Segment identification and resultant displays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

The '46A, '47A, '48, 'L46, 'L47, 'LS47, and 'LS48 circuits incorporate automatic leading and/or trailing-edge zero-blanking control ($\overline{RBI}$ and $\overline{RBO}$). Lamp test ($\overline{LT}$) of these types may be performed at any time when the $\overline{BI}/\overline{RBO}$ node is at a high level. All types (including the '49 and 'LS49) contain an overriding blanking input ($\overline{BI}$) which can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL logic outputs.

The SN54246/SN74246 through '249 and the SN54LS247/SN74LS247 through 'LS249 compose the 5 and 3 with tails and have been designed to offer the designer a choice between two indicator fonts. The SN54249/SN74249 and SN54LS249/SN74LS249 are 16-pin versions of the 14-pin SN5449 and 'LS49. Included in the '249 circuit and 'LS249 circuits are the full functional capability for lamp test and ripple blanking, which is not available in the '49 or 'LS49 circuit.

SEGMENT IDENTIFICATION



NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

'46A, '47A, 'L46, 'L47, 'LS47 FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						$\overline{BI}/\overline{RBO}$†	OUTPUTS							NOTE
	$\overline{LT}$	$\overline{RBI}$	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	1
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

†H = high level, L = low level, X = irrelevant

1. The blanking input ($\overline{BI}$) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple blanking input ($\overline{RBI}$) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input ($\overline{BI}$), all segment outputs are off regardless of the level of any other input.
3. When ripple-blanking input ($\overline{RBI}$) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple blanking output ($\overline{RBO}$) goes to a low level (response condition).
4. When the blanking input/ripple blanking output ($\overline{BI}/\overline{RBO}$) is open or held high and a low is applied to the lamp test input, all segment outputs are on.

‡Wire-AND logic serving as blanking input ($\overline{BI}$) and/or ripple blanking output ($\overline{RBO}$).

TEXAS INSTRUMENTS
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MARCH 1974, REVISED DECEMBER 1983

'46A, '47A, 'L46, 'L47, 'LS47 feature

- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

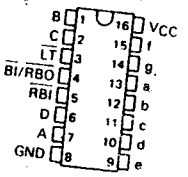
'48, 'LS48 feature

- Internal Pull-Ups Eliminate Need for External Resistors
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

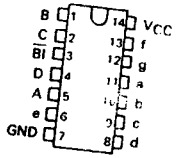
'49, 'LS49 feature

- Open-Collector Outputs
- Blanking Input

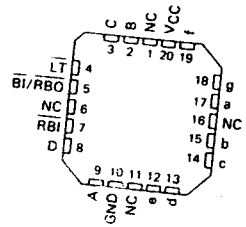
SN54L46, SN54L47 . . . J PACKAGE
SN5446A, SN5447A, SN54LS47, SN5448, SN54LS48 . . . J OR W PACKAGE
SN7446A, SN7447A, SN7448 . . . J OR N PACKAGE
SN74LS47, SN74LS48 . . . D, J OR N PACKAGE
(TOP VIEW)



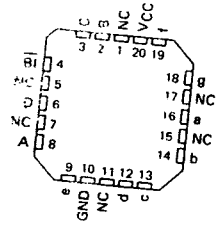
SN5449 . . . W PACKAGE
SN54LS49 . . . J OR W PACKAGE
SN74LS49 . . . D, J OR N PACKAGE
(TOP VIEW)



SN54LS47, SN54LS48 . . . FK PACKAGE
SN74LS47, SN74LS48 . . . FN PACKAGE
(TOP VIEW)



SN54LS49 . . . FK PACKAGE
SN74LS49 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

TEXAS INSTRUMENTS
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TYPES SN5432, SN54LS32, SN54S32, SN7432, SN74LS32, SN74S32
QUADRUPLE 2-INPUT POSITIVE-OR GATES

REVISED DECEMBER 1983

Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs

Dependable Texas Instruments Quality and Reliability

iption

These devices contain four independent 2-input OR gates.

The SN5432, SN54LS32 and SN54S32 are characterized for operation over the full military range of -55°C to 125°C. The SN7432, SN74LS32 and SN74S32 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

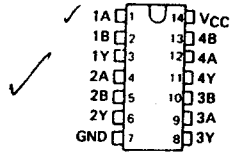
INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logram (each gate)

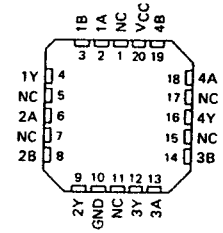
logic

$Y = A + B$ or $Y = \overline{\overline{A} \cdot \overline{B}}$

SN5432, SN54LS32, SN54S32 . . . J OR W PACKAGE
SN7432 . . . J OR N PACKAGE
SN74LS32, SN74S32 . . . D, J or N PACKAGE
(TOP VIEW)



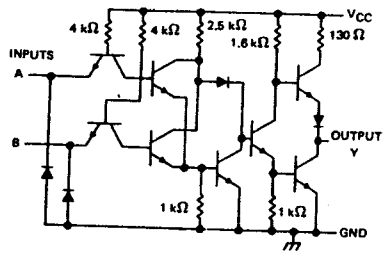
SN54LS32, SN54S32 . . . FK PACKAGE
SN74LS32, SN74S32 . . . FN PACKAGE
(TOP VIEW)



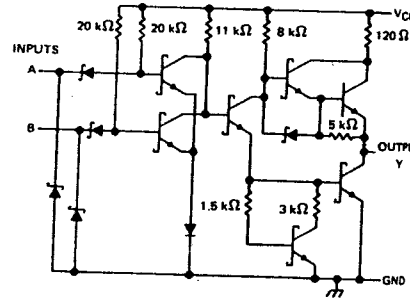
NC - No internal connection

schematics (each gate)

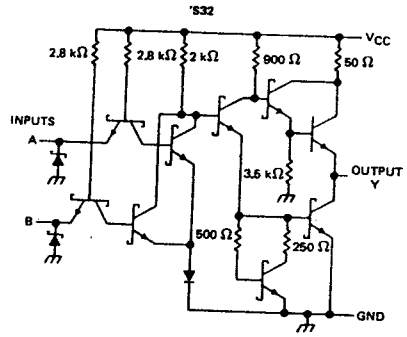
'32



'LS32



'S32



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '32, 'S32 . . . . . 7 V
'LS32 . . . . . 5.5 V
Operating free-air temperature: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5432			SN7432			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			−0.8			−0.8	mA
I_{OL} Low-level output current			16			16	mA
T_A Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN5432			SN7432			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IH} = 2 V,	I_{OH} = −0.8 mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN, V_{IL} = 0.8 V,	I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.4 V				40			40	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6	mA
I_{OS}§	V_{CC} = MAX		−20		−55	−18		−55	mA
I_{CCH}	V_{CC} = MAX, See Note 2			15	22		15	22	mA
I_{CCL}	V_{CC} = MAX, V_I = 0 V			23	38		23	38	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 400 Ω, C_L = 15 pF		10	15	ns
t_{PHL}					14	22	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54S03, SN74S03
QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	SN54S03			SN74S03			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
V_{OH} High-level output voltage			5.5			5.5	V
I_{OL} Low-level output current			20			20	mA
T_A Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = MIN, I_I = −18 mA			−1.2	V
I_{OH}	V_{CC} = MIN, V_{IL} = 0.8 V, V_{OH} = 5.5 V			0.25	mA
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 20 mA			0.5	V
I_I	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V			50	μA
I_{IL}	V_{CC} = MAX, V_I = 0.5 V			−2	mA
I_{CCH}	V_{CC} = MAX, V_I = 0 V		6	13.2	mA
I_{CCL}	V_{CC} = MAX, V_I = 4.5 V		20	36	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 280 Ω, C_L = 15 pF	2	5	7.5	ns
t_{PHL}				2	4.5	7	ns
t_{PLH}			R_L = 280 Ω, C_L = 50 pF		7.5		ns
t_{PHL}					7		ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN5404, SN54H04, SN54L04, SN54LS04, SN54S04
SN7404, SN74H04, SN74LS04, SN74S04
HEX INVERTERS

REVISED DECEMBER 1983

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain six independent inverters.

The SN5404, SN54H04, SN54L04, SN54LS04 and SN54S04 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7404, SN74H04, SN74LS04 and SN74S04 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each inverter)

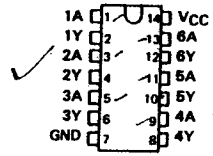
INPUTS A	OUTPUT Y
H	L
L	H

logic diagram (each inverter)

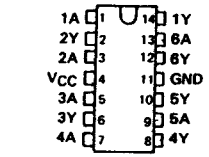
positive logic

$Y = \overline{A}$

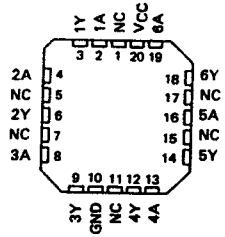
SN5404, SN54H04, SN54L04 . . . J PACKAGE
SN54LS04, SN54S04 . . . J OR W PACKAGE
SN7404, SN74H04 . . . J OR N PACKAGE
SN74LS04, SN74S04 . . . D, J OR N PACKAGE
(TOP VIEW)



SN5404, SN54H04 . . . W PACKAGE
(TOP VIEW)



SN54LS04, SN54S04 . . . FK PACKAGE
SN74LS04, SN74S04 . . . FN PACKAGE
(TOP VIEW)

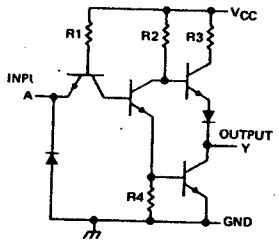


NC – No internal connection

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

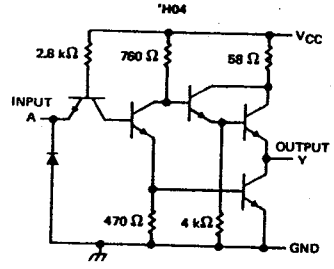
schematics (each gate)

'04,'L04

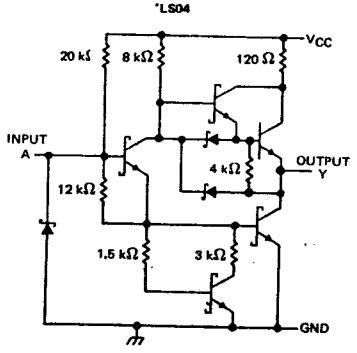


CIRCUIT	R1	R2	R3	R4
'04	4 kΩ	1.6 kΩ	130 Ω	1 kΩ
'L04	40 kΩ	20 kΩ	500 Ω	12 kΩ

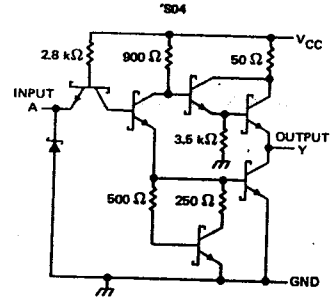
'H04



'LS04



'S04



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1): '04, 'H04, 'LS04, 'S04 ..... 7 V
'L04 ..... 8 V
Input voltage: '04, 'H04, 'L04, 'S04 ..... 5.5 V
'LS04 ..... 7 V
Operating free-air temperature range: SN54' ..... −55°C to 125°C
SN74' ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5404			SN7404			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			−0.4			−0.4	mA
I_{OL} Low-level output current			16			16	mA
T_A Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5404			SN7404			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −0.4 mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}§	V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CCH}	V_{CC} = MAX, V_I = 0 V		6	12		6	12	mA
I_{CCL}	V_{CC} = MAX, V_I = 4.5 V		18	33		18	33	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	R_L = 400 Ω, C_L = 15 pF		12	22	ns
t_{PHL}					8	15	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3 TTL DEVICES

TYPES SN5400, SN54H00, SN54L00, SN54LS00, SN54S00, SN7400, SN74H00, SN74LS00, SN74S00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

REVISED DECEMBER 1983

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

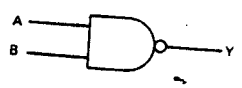
These devices contain four independent 2-input NAND gates.

The SN5400, SN54H00, SN54L00, and SN54LS00, and SN54S00 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7400, SN74H00, SN74LS00, and SN74S00 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

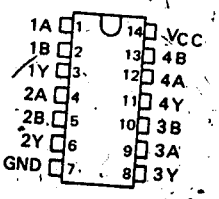
logic diagram (each gate)



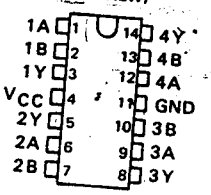
positive logic

$$Y = \overline{A \cdot B} \text{ or } Y = \overline{A} + \overline{B}$$

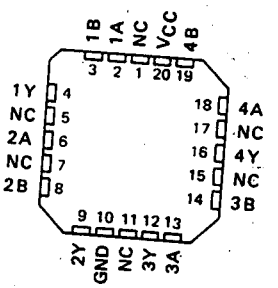
SN5400, SN54H00, SN54L00 . . . J PACKAGE
SN54LS00, SN54S00 . . . J OR W PACKAGE
SN7400, SN74H00 . . . J OR N PACKAGE
SN74LS00, SN74S00 . . . D, J OR N PACKAGE
(TOP VIEW)



SN5400, SN54H00 . . . W PACKAGE
(TOP VIEW)



SN54LS00, SN54S00 . . . FK PACKAGE
SN74LS00, SN74S00 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

ecommended operating conditions

		SN54LS00			SN74LS00			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †				SN54LS00			SN74LS00			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA					−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	V_{IL} = MAX,	I_{OH} = −0.4 mA		2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 4 mA			0.25	0.4		0.25	0.4	V
	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 8 mA						0.35	0.5	
I_I	V_{CC} = MAX,	V_I = 7 V					0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V					20			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V					−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX				−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V				0.8	1.6		0.8	1.6	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V				2.4	4.4		2.4	4.4	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 2 kΩ, C_L = 15 pF		9	15	ns
t_{PHL}					10	15	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.