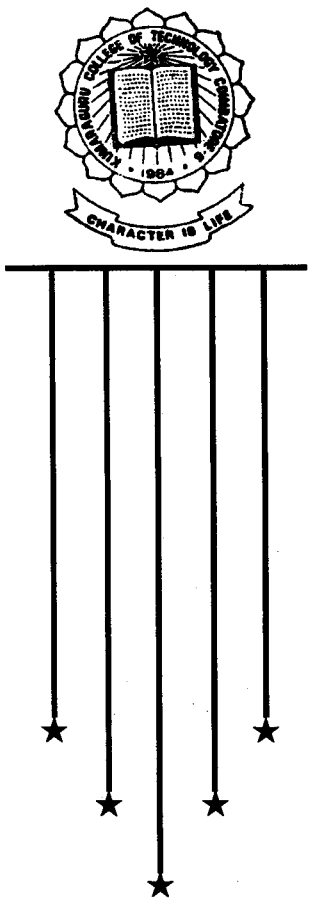
MICROPROCESSOR CONTROLLED BIOTELEMETRY BASED ELECTROCARDIOGRAM

PROJECT REPORT



1999 -2000

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IN PARTIAL FULFILMENT OF THE REQUIREMENTS

FOR THE AWARD OF THE DEGREE OF

BACHELOR OF ENGINEERING IN

ELECTRONICS & COMMUNICATION ENGINEERING

OF THE BHARATHIAR UNIVERSITY, COIMBATORE.

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ACKNOWLEDGEMENT

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First and foremost, we thank our Principal ***Dr. K.K. Padmanabhan, B.Sc. (Engg), M.Tech., Ph.D.*** *for providing us with excellent laboratory facilities for doing the project work.*

It is a great pleasure to thank our head of the department ***Prof. M. Ramasamy, M.E., M.I.S.T.E., M.I.E.E.E., M.I.E., C (Engg), M.B.M.E.S.I.*** *for being the chief motivation behind our project work and for having provided us with laudable advice and material at the time of need.*

We express our gratitude to our guide ***Asst. Prof. K. Ramprakash, M.E.,*** *for having provided us with constructive ideas and efficiently guiding us in the design and implementation of our project work.*

We are immensely grateful to all the staff members of Electronics and Communication Engineering Department, who helped us directly or indirectly to complete our project work.

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INTRODUCTION

INTRODUCTION

"Quality is no Accident" *- With the emerging applications in this modern age of highly improved medical sciences providing quality medical service has taken on a new importance. We bring into focus the biotelemetry system, which is one of the areas of modern medical sciences. Biotelemetry has made possible studies of active subjects under the conditions that so far prohibited measurements. It is therefore an indispensable technique in situations where the patient cannot reach the hospital in time.*

Telemetric surveillance is convenient during transportation, within the hospital area and for continuous monitoring of patients sent to other wards or clinics for checkup or therapy.

The electrical signal from the heart characteristically precede the normal mechanical function and monitoring of these signals has great clinical significance. It provides valuable information about a wide range of cardiac disorders such as the presence of an inactive part (infarction) or an enlargement (cardiac hypertrophy) of the heart muscle. Electro cardiographs are used in catheterisation laboratory, coronary care units and for routine cardiac diagnostic applications in cardiology. Hence there is a need for the biotelemetric system for measurement of physiological parameters. Here the priority is more for ECG as it detects a wide range of cardiac disorders.

AN OVERVIEW . . .

ECG WAVEFORM ANALYSIS

Before we proceed, let us have some knowledge about electrocardiogram waveform. The electrocardiogram is a graphic recording or display of the time – variant voltages produced by the myocardium during the cardiac cycle.

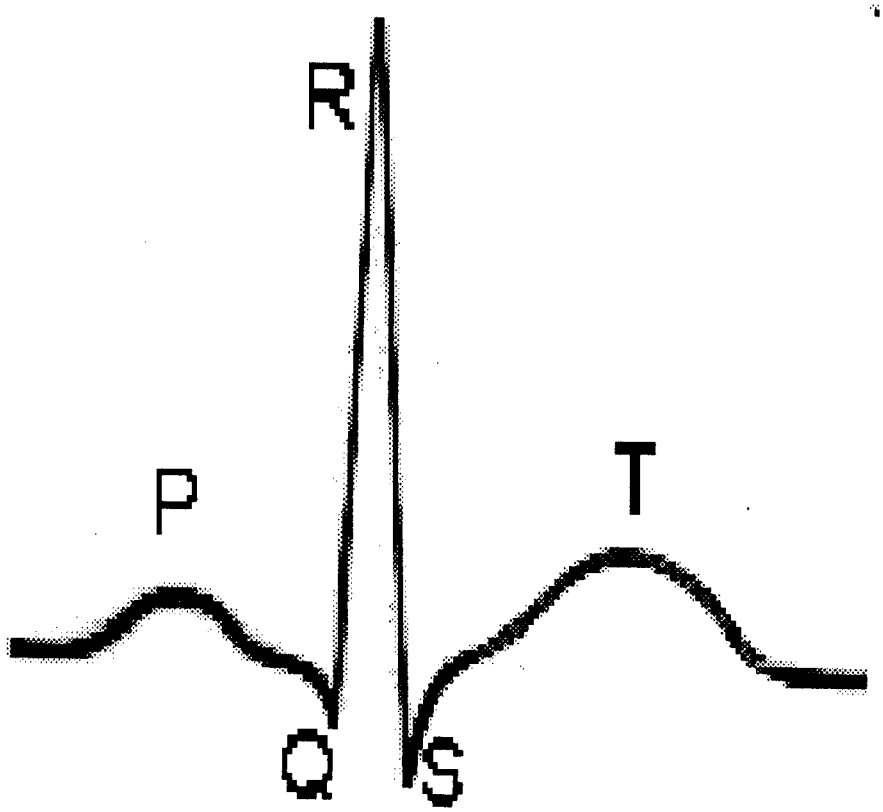


Figure shows the typical ECG wave

It consists of P wave, QRS complex and T wave. They reflect the rhythmic electrical depolarization and repolarisation of the myocardium

associated with the contractions of atria and ventricles. The electrocardiogram is used clinically in diagnosing various diseases and conditions associated with the heart. It also serves as a timing reference for other measurements.

Alphabetic designations have been given to each of the prominent features of the ECG. These can be identified with events related to the action potential propagation pattern. The P wave represents depolarization of the atrial musculature. The QRS complex is the combined result of the repolarisation of the atria and the depolarisation of the ventricles, which occur almost simultaneously. The T wave is the wave of ventricular repolarisation, whereas the U wave, if present, is generally believed to be the result of after – potentials in the ventricular muscle. The P – Q interval represents the time during which the excitation wave is delayed in the fibers near the AV node.

The shape and polarity of each of these features vary with location of the measuring electrodes with respect to the heart, and a cardiologist normally bases his diagnosis on the readings taken from several electrode locations. A cardiologist would first look at the heart rate. The normal value lies in the range of 60 – 100 beats per minute. A slower rate than this is called bradycardia (slow heart) and a higher rate, tachycardia (fast heart). He would then see if the cycles are evenly

spaced. If not, an arrhythmia may be indicated. If the P – R interval is greater than 0.2 second, it can suggest blockage of AV node. If one or more of the basic features of the ECG should be missing, a heart block of some sort may be indicated.

In healthy individuals, the ECG remains reasonably constant, even though the heart rate changes with the demands of the body. It should be noted that the position of the heart within the thoracic region of the body, as well as the position of the body itself, influences the electrical activity of the heart.

Under pathological conditions, several changes may occur in the ECG. These include

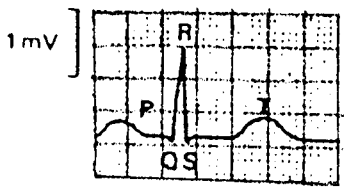
- *altered paths of excitations in heart*
- *changed origin of waves (ectopic beats)*
- *altered relationships (sequences) of features*
- *changed magnitudes of one or more features*
- *differing durations of waves or intervals*

If the PR interval is more than 0.22 sec., the AV Block (First degree heart attack) occurs. When the QRS complex duration is more than 0.1 second, the bundle block (severe heart attack) occurs.

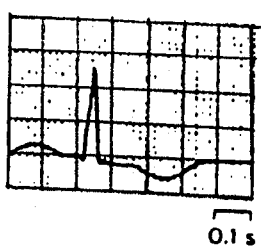
The origin, amplitude and duration of the different waves in the electrocardiogram are given in the table.

PHYSIOLOGICAL NATURE OF ECG WAVEFORM:

	Origin	Amplitude (mV)	Duration (SECS)
P Wave	Artrial depolarisation or contraction	0.25	0.12 to 0.22 (P-R interval)
R wave (QRS complex)	Repolarisation of the artria and the deplorisation of the ventricles	1.60	0.07 to 0.1
T wave	Ventricular Repolarisation (Relaxation of myocardium)	0.1 to 0.5	0.05 to 0.15 (S-T interval)
S-T interval	Ventricular contraction		
U wave	Slow Repolarisation of the intraventricular (Purkinje fibers) system	< 0.1	0.2 (T-U interval)

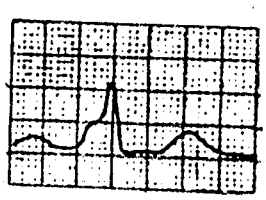


→ Normal ECG curve



→ Here ST segment is depressed and negative T wave is persent.

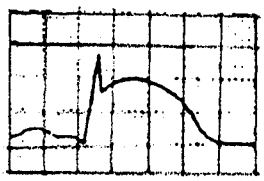
Result: Coronary insufficiency.



→ Here QRS complex is widened i.e. QRS interval is greater than 0.1 second.

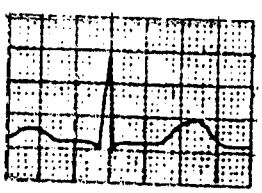
Result: Bundle block

ANALYSIS OF ECG WAVEFORMS



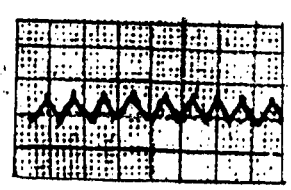
→ Here ST segment is elevated.

Result: Myocardial infarction.



→ Here PQ segment has prolonged conduction time i.e. greater than 0.22 second

Result: First degree AV block



→ Here there is a train of pulses instead of PQRST waves.

Result: Ventricular fibrillation which may lead to death if it is not properly corrected by defibrillator.

ANALYSIS OF ECG WAVEFORM

ECG LEAD CONFIGURATION

Usually surface electrodes are used with jelly as electrolyte between skin and electrodes. The potentials generated in the heart are conducted to the body surface. The potential distribution changes in a regular and complex manner during each cardiac cycle. Therefore to record electrocardiogram, we must choose standardized electrode systems.

1. *Bipolar limb leads (or) standard leads*
2. *Augmented unipolar limb leads*
3. *Chest leads (or) precordial leads*
4. *Frank lead system (or) corrected orthogonal leads*

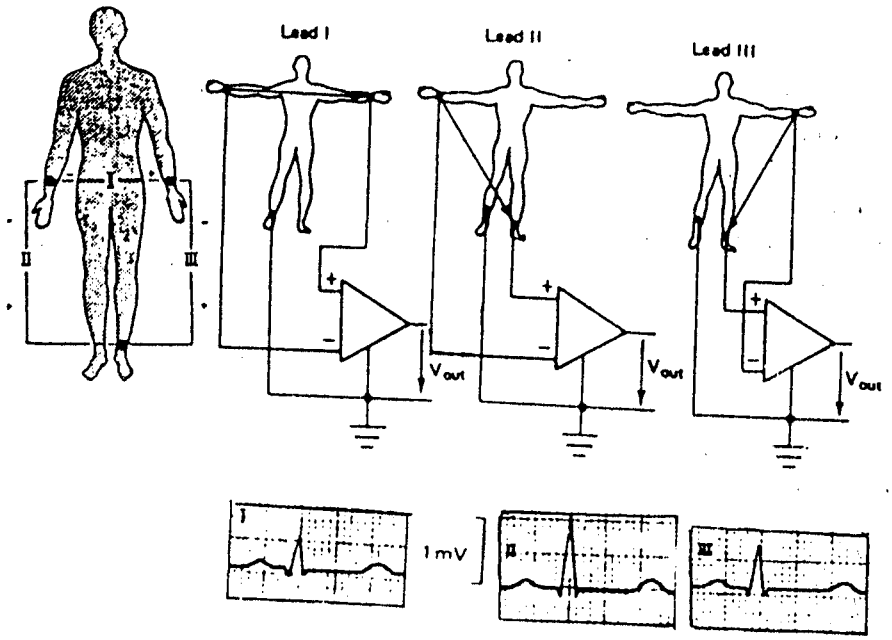
Among these four systems, the first three are widely used.

Bipolar Limb Leads – Standard Leads I, II and III:

In standard leads, the potentials are tapped from four locations of our body. They are

1. *Right arm.*
2. *Left arm.*
3. *Right leg.*
4. *Left leg.*

Usually the right leg electrode acts as ground reference electrode.



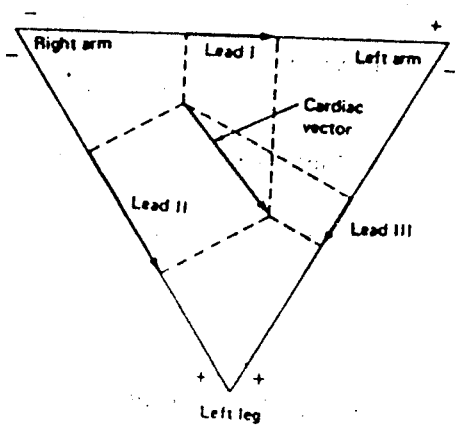


Figure shows the standard limb leads positions and it's corresponding wave patterns and the Einthoven triangle.

Lead 1 position – gives voltage V1, the voltage drop from the Left arm (LA) to the right arm (RA).

Lead 2 position gives voltage V2, the voltage drop from the Left leg (LL) to the Right arm (RA).

Lead 3 position – gives voltage V3, the voltage drop from the Left leg (LL) to the Left arm (LA).

The closed path RA to LA to LL and back to RA is called the Einthoven triangle. According to Einthoven, in the frontal plane of the body, the cardiac electric field vector is a two dimensional one. The ECG measured from any one of the three limb leads is a time variant single dimensional component of that vector. Along the sides of this triangle, the three projections of ECG vector are measured as shown in the figure. Further, the vector sum of the projections on all the three sides is equal to zero. Thus following Kirchoff's law, the R wave amplitude of lead II is equal to the sum of the R wave amplitude of leads III and I. For example, the R wave nominal voltage from different leads is given in the next page.

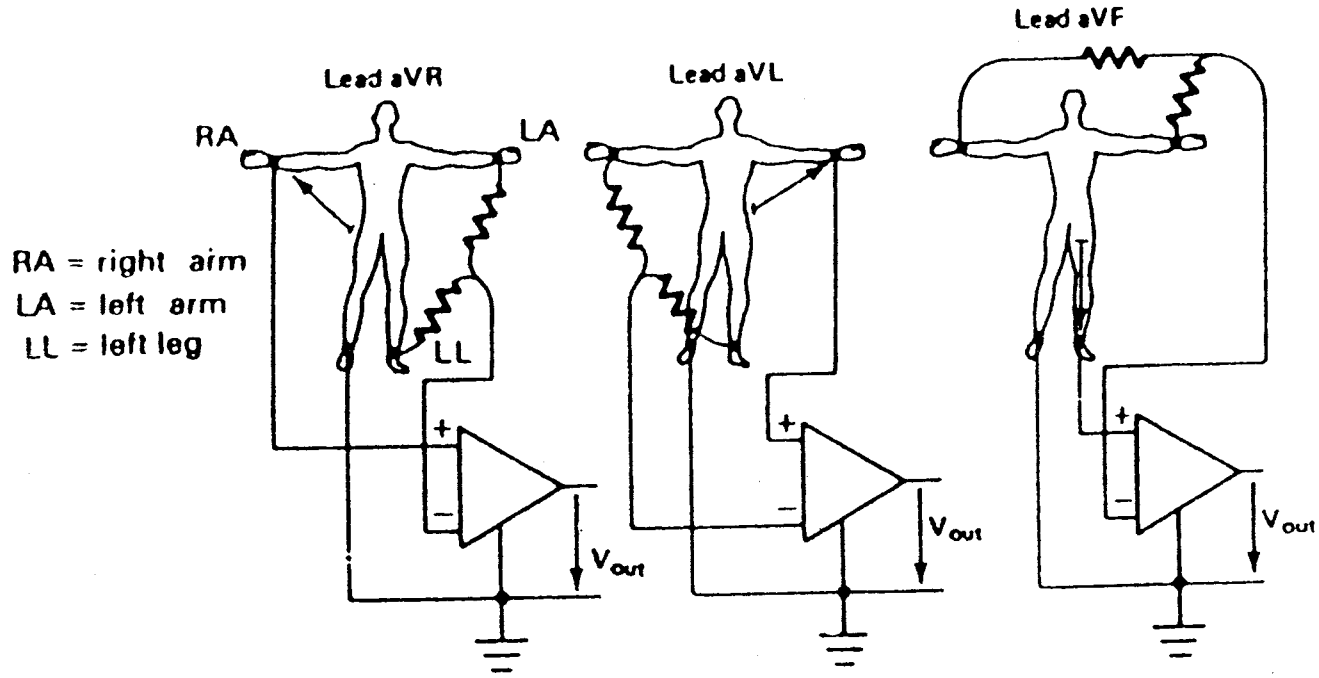
Lead I V1 (mV)	Lead II V2 (mV)	Lead III V3 (mV)
0.53	0.71	0.38
0.07 – 1.13	0.18 – 1.68	0.03 – 1.13

The voltage given in brackets indicate the range of the measured voltage. Thus V2 = V1 + V3.

AUGMENTED UNIPOLAR LIMB LEADS:

In the augmented unipolar limb leads system, which is introduced by Wilson, the electrocardiogram is recorded between a single exploratory electrode and the central terminal that has a potential corresponding to the center of the body. Thus two equal and large resistors are connected to a pair of limb electrodes and the center of this resistive network acts as the exploratory electrode. By means of augmented ECG lead connections, a small increase in the ECG voltage can be realized. The augmented lead connections are augmented voltage Right arm (aVR), augmented voltage Left arm (aVL) and augmented voltage Foot (aVF) as shown in the figure.

Even though the resistors in these limb leads have large value, their values are smaller when we compare with the input resistance of the



AUGMENTED LIMB LEAD SYSTEM

preamplifier. By Kirchoff's law, the augmented voltages can be written as in terms of standard lead voltages.

$$aVR = - V1 - V3/2$$

$$aVR = V1 - V2/2$$

$$aVR = V2 - V1/2$$

UNIPOLAR CHEST LEADS:

In the case of unipolar chest leads, the exploratory electrode is obtained from one of the chest electrodes. The chest electrodes are placed on the six different points on the chest close to the heart as shown in the figure. By connecting three equal large resistances to the left arm, right arm and the left leg, a reference electrode or central terminal is obtained. This lead system is known as Wilson system. Thus the electrocardiograms are recorded from these 12 lead selections such that 3 standard bipolar leads, 3 augmented unipolar leads and chest leads.

The ECG potentials are measured with colour coded leads according to the convention:

White – Right arm

Black – Left arm

Green – Right leg

Red – Left leg

Brown – Chest

This is internationally adopted for easy reference.

FRANK LEAD SYSTEM:

The corrected orthogonal leads system (or) Frank lead system is used in vector cardiography. Here one can get informations from above said 12 leads. Further using this lead system, the heart's dipole field is resolved into three mutually perpendicular components and hence the state of the pulse is studied three dimensionally.

BIOTELEMETRY SYSTEM

Biotelemetry is the measurement of biological parameters over a distance. The means of transmitting data from the point of generation to the point of reception can take many forms. Perhaps the simplest application of the principle of Biotelemetry is the stethoscope, whereby heartbeats are amplified acoustically and transmitted through a hollow tube system to be picked up by the ear of the physician for interpretation. The following types of data were obtained by biotelemetry:

1. *Temperature by rectal or oral thermistor.*
2. *Respiration by impedance pneumograph.*
3. *Electrocardiograms by surface electrodes.*
4. *Indirect blood pressure by contact microphone and cuff.*

As the field progressed, it became apparent that literally any quantity that could be measured was adaptable to biotelemetry. Just as with hardwire systems, measurements can be applied to two categories:

1. *Bioelectrical variables, such as ECG, EMG, and EEG.*
2. *Physiological variables that require transducers, such as blood pressure, gastrointestinal pressure, blood flow, and temperature.*

With the first category, a signal is obtained directly in electrical form whereas the second category requires a type of excitation, since the physiological parameters are measured as variations of resistance, inductance or capacitance.

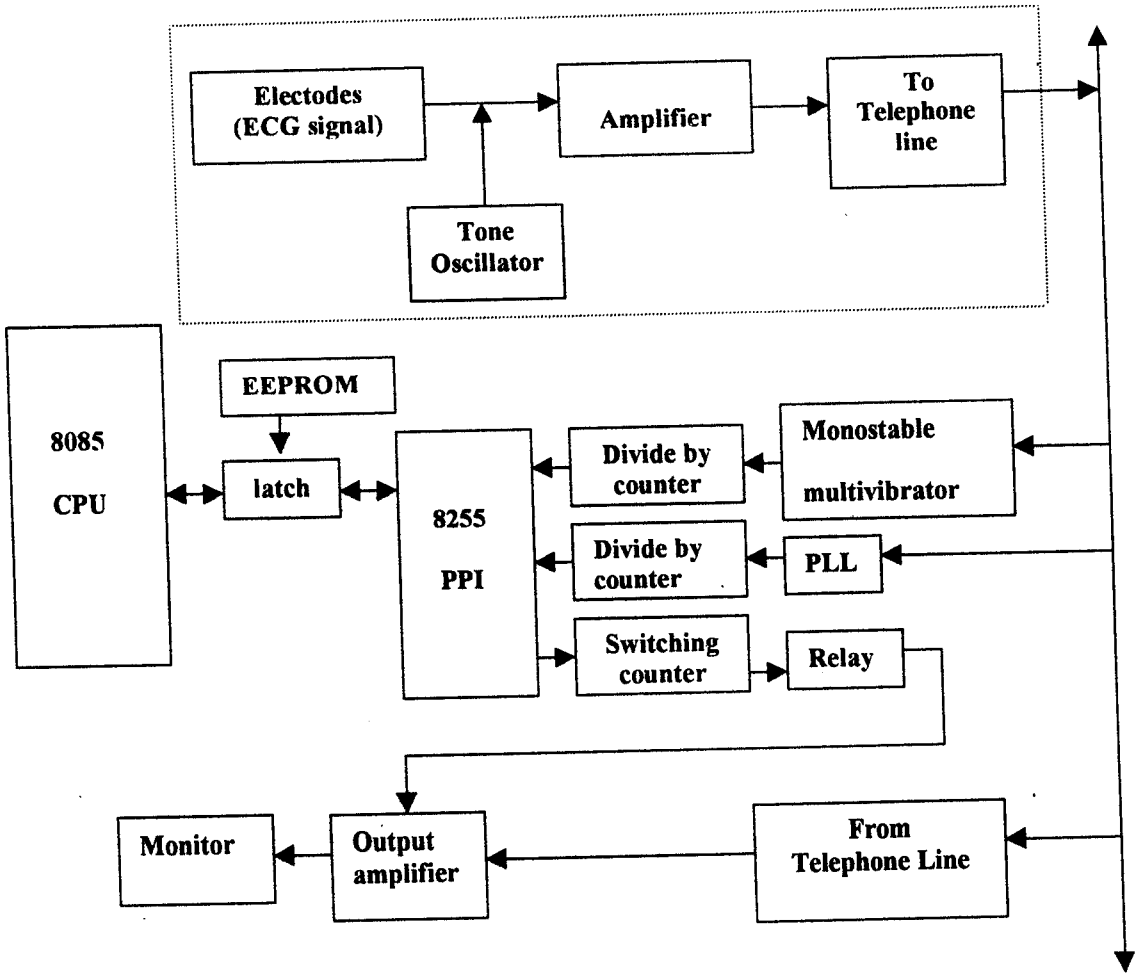
In a typical system, the appropriate analog signal (Voltage, Current, etc.) is converted into a form or code capable of being transmitted. After being transmitted, the signal is decoded at the receiving end and converted back into its original form. Currently, the most widespread form of biotelemetry for bioelectric potentials is in the transmission of the electrocardiogram.

One example of ECG telemetry is the transmission of electrocardiograms from an ambulance or the site of an emergency to a hospital, where a cardiologist can immediately interpret the ECG and arrange for any special treatment that may be necessary upon the arrival of the patient at the hospital.

The use of telemetry for ECG signals is not confined to emergency applications. It is used for exercise electrocardiograms in the hospitals so that the patient can run up and down steps, unencumbered by wires. Also, there have been cases in which individuals with heart conditions wear ECG telemetry units at home and on the job and relay ECG data periodically to the hospital for checking.

PROJECT INTRODUCTION

Transmitter section



The Block Diagram

CIRCUIT OPERATION

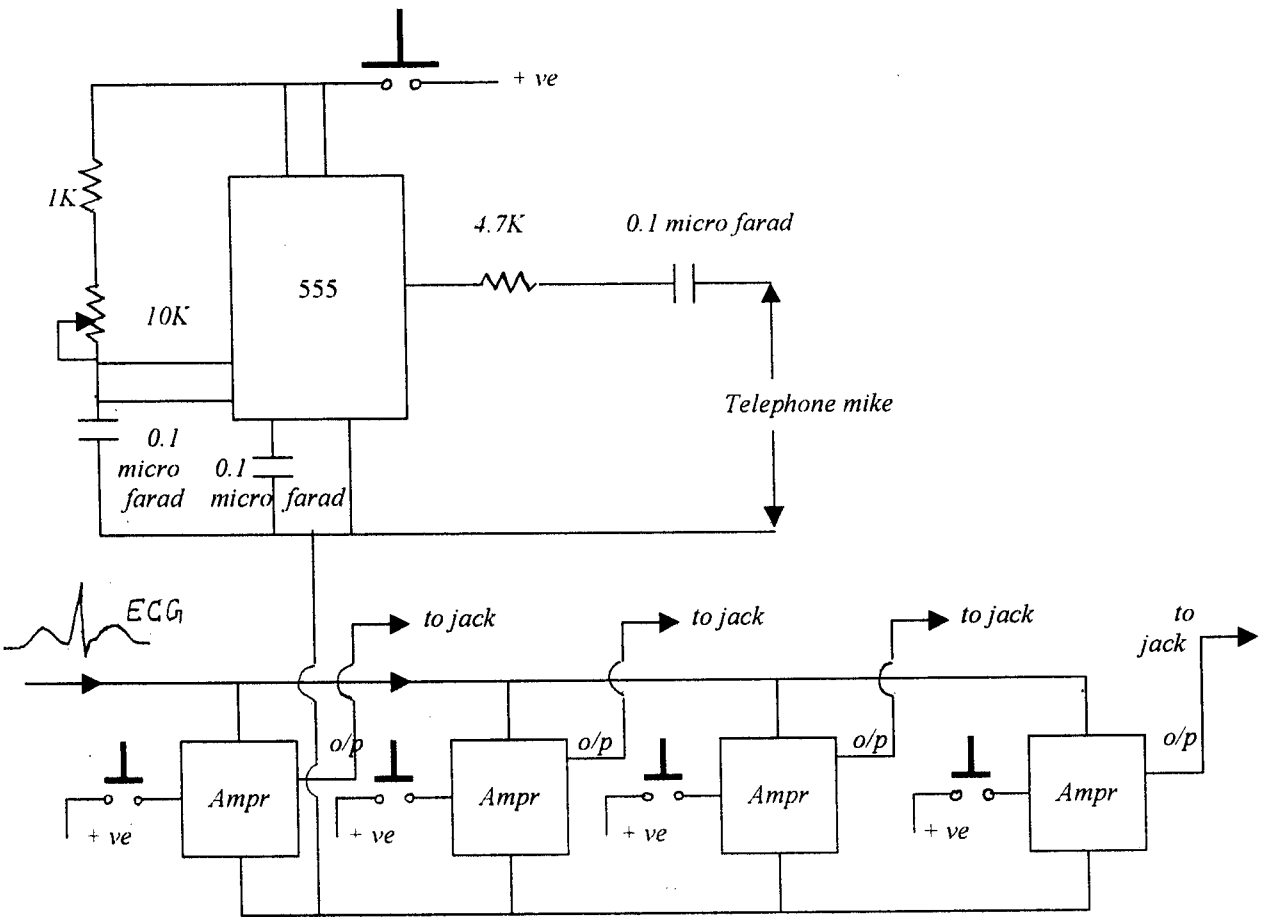
CIRCUIT OPERATION

By placing the electrodes in the correct part of the body, the ECG signals that are to be transmitted are received. These signals are amplified in two stages in order to increase the strength of the signal. The amplified signal is then transmitted to the receiving end through the telephone line. Before the signal gets transmitted a tone signal is generated by the timer oscillator to indicate the transmission of the electrocardiogram signal from the transmitter section. The amplified signal is connected to the mike point in the telephone that is used to transmit the signals through the telephone line. The signals from the various parts are mixed and amplified by 741 series operational amplifier.

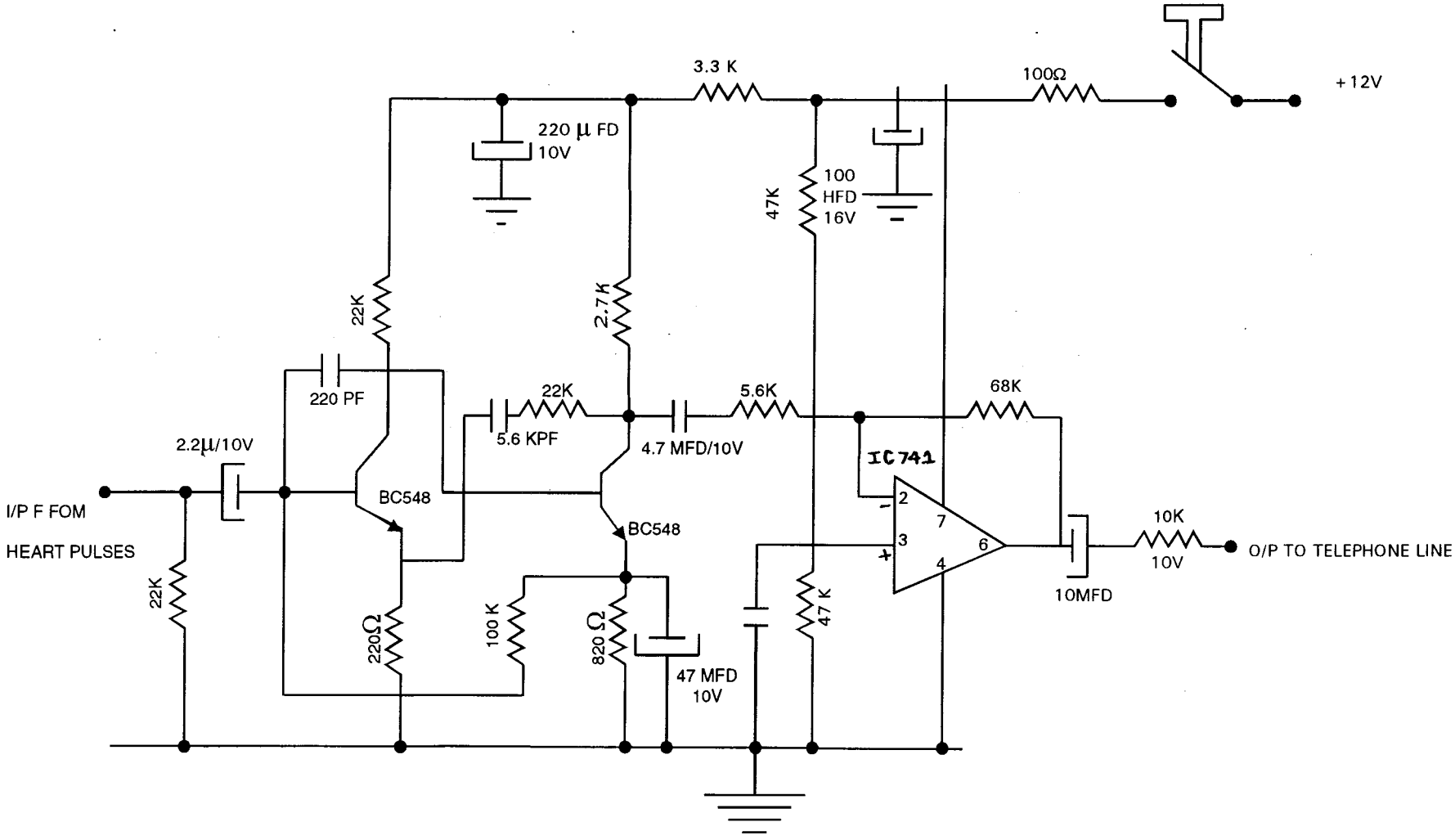
RING DETECTION:

In the receiver side, we have the microprocessor, ring detector, tone detector and a monitor. The ring detection section in the receiver detects the ringing and hence receives the amplified signal through the telephone line by lifting the telephone unit. In the ring detector section by using 4017 IC as a monostable multivibrator, we have already set that,

Transmitter Circuit



AMPLIFIER SECTION



after receiving 3 pulses, ring detector sends the ring detection pulse. At ringing time AC signal is received. The bridge rectifier with IN4007 and the capacitance setup converts this AC signal to DC signal. This DC signal is amplified by the transistor BC547.When it receives 4 rings it enables the port A. By using Port A of 8255 peripheral interface device as input, this pulse is compared with the pulse that is already stored in EPROM. If it matches, a signal is triggered in the Port B of 8255. At this time, the hook switch is released by switching on the hook switch-relay.

TONE DETECTION:

In the tone detection section, the phase locked loop IC567 is used as a tone decoder. The action of the PLL is to lock the output frequency and phase to the frequency and phase of input signal. Similar to ring detector section, after receiving the preset number of pulses, we receive the tone detector pulse at the output of 567 IC. By using Port C, this tone detector pulse is compared with the tone detection pulse that is stored in the memory. If this matches, then the output Port B is activated and the triggering signal switches on the amplifier ON – relay. The power supply of +12V is regulated by a regulator 7805 IC to +5V, which is the supply voltage for the microprocessor unit. The two

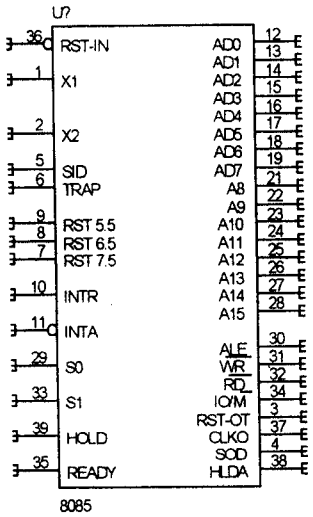
relays, hook switch relay and amplifier ON-relay remain in on condition for 3 minutes. The microprocessor switches OFF the relays after this delay time of 3 minutes by resetting the entire unit.

If Port B is activated, then the switch is closed and the data terminals of PPI (8255) are enabled. The data followed by ring and tone signals are amplified by the 741 series op – amp. The output terminal can be connected to either a plotter or a CRO. By using parallel connection, we can use both.

THE FUNCTION OF 8085:

The microprocessor unit in the receiver section features a 8085 processor that controls the relays. It operates on 8-bit data and uses 16-bit address. Since it uses16-bit address it can directly address 2 power 16=65,536=64K memory locations. The 8085 is designed using NMOS transistor in 40 pin DIP (Dual In-line Package). It requires a single power supply of +5 volts. The 8085 generates a clock signal internally and divide by two for internal operations. The NMOS 8085 is available in two versions 8085A and 8085A-2 with maximum internal clock frequency of 3.03MHz and 5MHz respectively.

The pin configuration of the microprocessor used in the receiver circuit is shown below:



The lower order address byte and data lines AD0 to AD7 are multiplexed. At the beginning of a machine cycle the address is given out on AD0 to AD7 and it is latched on into the external latch by using ALE. Then the line lines AD0 to AD7are multiplexed. At the beginning of a machine cycle the address is latched into external latch by using ALE. Then the lines AD0 to AD7 are used to carry data. The pins A8 to A15 are unidirectional and contain the high byte address. The $\overline{RD}$ signal is asserted low by the 8085 during a memory or I/O READ operation. Similarly, the $\overline{WR}$ pin signal is asserted low during its internal operations.

The ready input can be used by the slower external devices for obtaining extra time in order to communicate with the 8085.The READY is made low to provide wait state clock periods in the machine cycles.

The $\overline{HOLD}$ and $\overline{HLDA}$ signals are used for the Direct Memory Access (DMA) type of data transfer. The DMA controller places a HIGH on HOLD pin in order to take control of the system bus. The $\overline{HOLD}$ function is acknowledged by the 8085 by placing a HIGH output on the $\overline{HLDA}$ pin.

The 8085 has the clock generation circuit on the chip but an external quartz crystal or LC circuit or RC circuit should be connected at the pins X1 and X2 is divided by two internally for internal clock. The frequency of output clock signal is same as that of internal clock. The $\overline{RESET}$ $\overline{IN}$ signal, when pulsed LOW, causes the 8085 to execute the first instruction at the 0000H location. In addition, the 8085 resets instruction register, interrupt mask bits and other registers. The $\overline{RESET}$ $\overline{IN}$ must be held LOW for at least three clock periods.

The program instructions are stored in memory, which is an external device. To execute a program in 8085, the starting address of the program should be loaded in program counter. The 8085 output the content of program counter in the address bus and assert read control signal low. Also, the program counter is incremented.

The address and the read control signal enable the memory to output the content of memory location on the data bus. Now the content of data bus is the opcode of an instruction. The read control

signal is made high by timing and control unit after a specified time. At the rising edge of read control signals, the opcode is latched into the microprocessor internal bus and placed in the instruction register. The instruction-decoding unit decodes the instructions and provides information to timing and control unit to take further actions.

FUNCTION OF THE 8255 PPI:

The 8255 has three ports A, B and C. the ports A and B are 8 – bit parallel ports. Port A can be programmed to work in any one of the three operating modes as input or output port. They are:

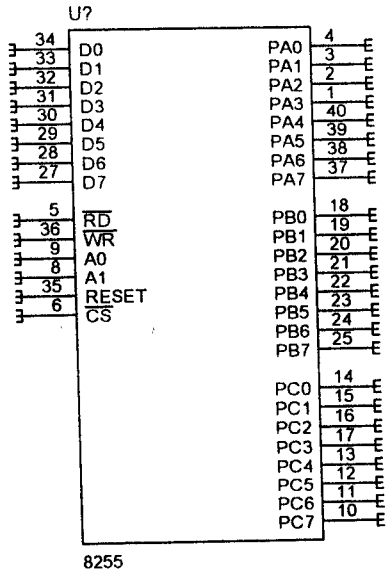
Mode 0 – simple I/O port

Mode 1 – handshake I/O port

Mode 3 – bi-directional I/O port

The port B can be programmed to work either in mode – 0 or mode – 1 as input or output port. The port C pins (8 – pins) have different assignments depending on the mode of port A and B. The Port A and Port C act as input ports and Port B acting as the output port releases the hook switch and activates the amplifier.

The pin configuration of the programmable peripheral interface used in conjunction the processor is shown in the next page.



If ports A and B are programmed in mode – 1 or mode – 2, then some of the pins of port C are used for handshake signals and the remaining pins can be used as input/output lines or individually set/reset for control applications.

I/O MODES of 8255:

Mode – 0: *in this mode all the three ports can be programmed either as input or output port. In mode – 0, the outputs are latched and the inputs are not latched. The ports do not have handshake or interrupt capability. The ports in mode – 0 can be used to interface DIPswitches. Hexa – keypad, LED's and 7 – segment LED's to the processor.*

Mode – 1: *in this mode, only ports A and B can be programmed either as input or output port. In mode – 1, handshake signals are exchanged between the processor and peripherals prior to data transfer. The port C pins are used for handshake signals. Input and output data are latched. Interrupt driven data transfer scheme is possible.*

Mode – 2: *in this mode, the port will be a bi-directional port. Only port A can be programmed to work in mode – 2. Five pins of port C are used for handshake signals. This mode is used primarily in applications such as data transfer between two computers or floppy disk controller interface.*

The ports are grouped as group A and group B. the group A has Port A, Port C upper and its control circuit. The group B comprises of Port B, Port C lower and its control circuit.

The Read/Write control logic requires six control signals. These signals are given below.

$\overline{RD}$ *(Read): This control signal enables the read operation. When this signal is LOW, the microprocessor reads data from a selected I/O port of the 8255A.*

$\overline{WR}$ *(Write): This control signal enables the write operation. When this goes LOW, the microprocessor writes into a selected I/O port or the control register.*

$\overline{RESET}$: *This is an active high signal. It clears the control register and set all ports in the input mode.*

$\overline{CS}$, *A0,A1: These are device select signals. The* $\overline{CS}$ *is connected to the decoder in the system. A0 and A1 are generally connected to A0 and A1 of the processor.*

The 8255 can be either memory mapped in the system or it can be I/O mapped in the system. When $\overline{CS}$ *is LOW the 8255 is selected. The A0 and A1 select any one of the four internal devices.*

The 8255 ports are programmed by writing a control word in the control register. For setting I/O functions and mode of operation the I/O mode control word is sent to the control register.

FUNCTION OF THE EPROM:

The EPROM in the receiver section for storing the ring detection and the tone detection pulses and it acts as a memory for the microprocessor.

This memory stores a bit by charging the floating gate of a FET. Information is stored by using an EPROM programmer, which applies high voltages to charge the gate. Exposing the chip to ultra violet light can erase all the information and the chip can be reprogrammed.

We have used an Intel 2732 EPROM which is a 32, 76 8 – bit ultraviolet erasable and electrically programmable read only memory (EPROM). It operates from a single 5-volt power supply, has a standby mode, and features an output enable control. The total programming time for all bits is three and a half minutes. The above mentioned features have made designing with the 2732 in microcomputer systems faster, easier, and more economical.

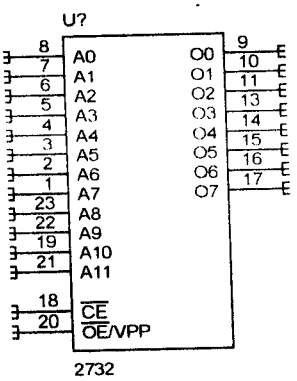
An important 2732 feature is the separate output control, output enable ($\overline{OE}$) from the chip enables control ($\overline{CE}$). The $\overline{CE}$ control eliminates bus contention in multiple bus microprocessor systems. It also has a standby mode, which reduces the power dissipation without increasing access time. The maximum active current is 150mA. While the maximum standby current is only 30mA, an 80% savings. The standby mode is achieved by applying a TTL high signal to the $\overline{CE}$ input.

Thirteen address lines (A0 - A12) are required to access the 2 (8kb) location within the device. D0 – D7 are the data output lines and are connected to the data bus.

MODE SELECTION:

PINS MODE	$\overline{CE}$ (18)	$\overline{OE}/V$ (20)	Vcc (24)	OUTPUTS (9-11-13-17)
Read	VIL	VIL	+5	DOUT
Standby	VIH	Don't Care	+5	High Z
Program	VIL	Vpp	+5	DIN
Program verify	VIL	VIL	+5	DOUT
Program inhibit	VIL	Vpp	+5	High z p73

The pin diagrams and functional block diagram are given in figure.



Vpp is used for programming (writing into and burning) the 2732 by providing a high voltage (usually 12.5V or 21V). PGM is also used for programming. Its functions as a $\overline{WR}$ signal and is held low for the time that is required for programming (write into) a selected location (accessed by the status of the A0 – A12 lines). In addition to these lines, the 2732 has two enable lines, the $\overline{CE}$ (chip enable) and the $\overline{OE}$ (output enable). When the $\overline{CE}$ is made low, it is used to force the 2732 out of the standby mode. $\overline{OE}$ is used in conjunction with $\overline{CE}$ for two-line control to avoid bus contention.

OPERATIONAL MODES:

The 2732 has eight modes of operation. The modes are selected on the basis of the signals present on the pins. The first three modes (read,

output disable and standby) manifest, depending on the status of the $\overline{CE}$, $\overline{OE}$ and PGM when the 2732 is not being programmed.

The various modes are described here:

READ:

In this mode, the Vpp pin is held at Vcc level (+5V) and PGM is held high. The $\overline{CE}$ pin is made low in order to select the device and $\overline{OE}$ is made low in order to gate the data from the output pins (D0 – D7). The contents of the memory location specified by A0 – A12 can then be read out into the system data bus.

STANDBY:

When the $\overline{CE}$ pin is held high, the device is deselected and enters the standby mode in which the current consumption is reduced from an active value of approximately 100mA to 40mA. The outputs are (D0 – D7) are tristated regardless of the $\overline{CE}$ status.

OUTPUT DISABLE:

The outputs are disabled and tristated when the $\overline{CE}$ is low and $\overline{DE}$ is high.

PROGRAM (STANDARD PROGRAMMING):

In this mode, data can be written into a desired location by selectively programming zeros. Prior to programming, the data at a location is FFH. If the data at that location is to be changed, the Vpp pin

is given upto the programming level voltage; with $\overline{CE}$ and PGM enabled, and the desired data is placed on the D0 – D7 pins of the device.

VERIFY:

After a location is programmed, a verify operation to be performed to ensure that the location has been programmed correctly. The Vpp pin is made high (22V or 12.5V for 2732 and 2732A respectively), the $\overline{CE}$ and $\overline{DE}$ made low, while PGM is high. The data on D0 – D7 pins can then be compared with the data that was placed on the pins during programming.

PROGRAM INHIBIT:

With the Vpp pin held high 22V for 2732 a high $\overline{CE}$ inhibits programming regardless of the status of the PGM input. This is of particular advantage when multiple 2732s are programmed with different data for the same addresses.

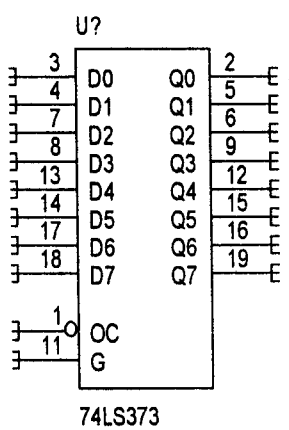
FUNCTION OF THE LATCH:

The latch is a basic component of any circuit. We have used a latch in the receiver section of the circuit. The latch has been used in demutiplexing the address lines in the microprocessor. Latch is a basic element of memory, which is nothing but a flip-flop. To write or store a bit in the latch, we need an input data bit (Din) and an enable signal

($\overline{EN}$). In this latch, the stored bit always available on the output line (Dout). The latch we have used is a 74LS373 latch.

A latch is used commonly to interface output devices. When the microprocessor unit sends an output, data are available on the data bus for only a few microseconds, and therefore, a latch is used to hold data for display.

Typical examples of the latches are the 74LS373 and the 8282. Both are functionally similar; however, they are pin compatible. These octal latches are suitable to latch 8 – bit data. The latch we have used is 74LS373 latch the pin diagram of which is shown below:



The devices include eight-D latches with tristate buffers. It requires two input signals, enables (G) and output control (OC). The enable is an active high signal connected to the clock input of the flip – flop.

When this signal goes low, data are latched from the data bus. The output control signal is active low, and it enables the tristate buffers to output data to the display devices.

TRUTH TABLE OF 74 LS 373

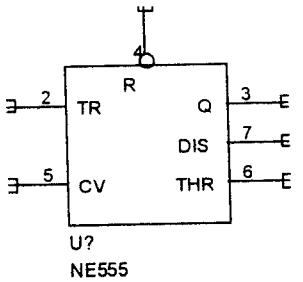
FUNCTION TABLE:

OUTPUT CONTROL	*ENABLE G*	*D*	*OUTPUT*
L	*H*	*H*	*H*
L	*H*	*L*	*L*
L	*L*	*X*	*Q0*
H	*X*	*X*	*Z*

FUNCTION OF 555 TIMER:

The 555 timer is used both in the transmitter and the receiver section. In the transmitter section it functions as a tone oscillator and it functions in the monostable mode in the receiver section. It is highly a stable integrated circuit capable of functioning as an accurate time – delay generator and as a free running multivibrator. In the transmitter

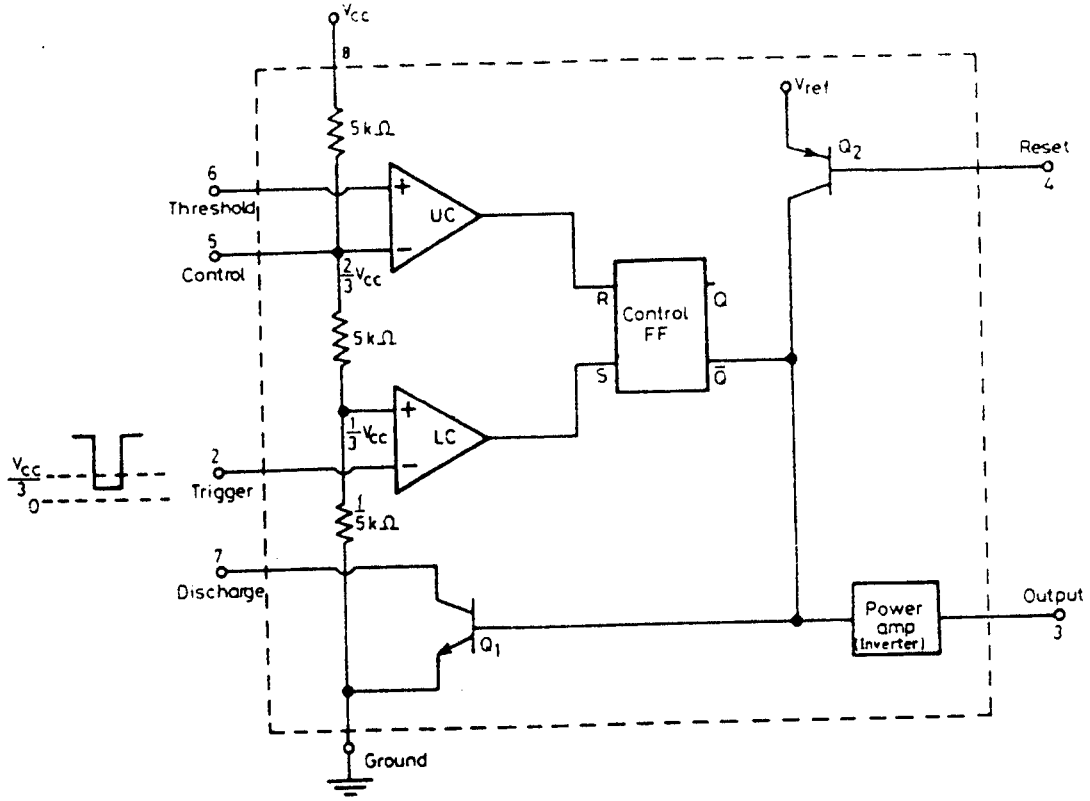
section, it is used as a tone oscillator and in the receiver section, it operates in monostable mode.



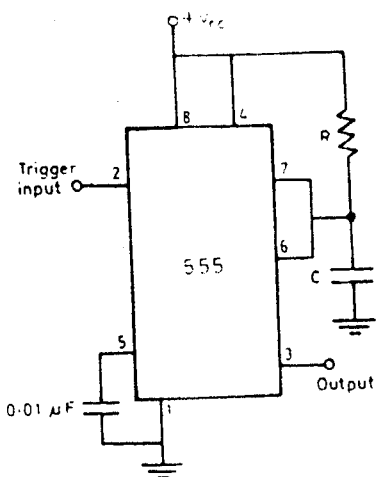
Pin connections for the IC are shown in the figure.

The functional diagram, which is shown in the next page, is explained below. The three 5k ohm resistors act as voltage divider, providing bias voltage of (2/3) Vcc to the Upper Comparator (UC) and (1/3) Vcc to the Lower Comparator (LC), where Vcc is the supply voltage. Since these two voltages fix the necessary comparator threshold voltage, they also aid in determining the timing interval.

It is possible to vary time electronically too, by applying a modulation voltage to the control voltage input terminal (Pin 5). In applications where no such modulation is intended, it is recommended by manufacturers that a capacitor (0.01 micro farad) be connected between control voltage terminal (Pin 5) and ground to by – pass noise or ripple from supply. In the standby (stable) state, the output Q of the control flip–flop (FF) is HIGH. This makes the output LOW because of power amplifier



FUNCTIONAL DIAGRAM OF 555 TIMER



555 TIMER IN MONOSTABLE MODE

that is basically an inverter. A negative going trigger pulse is applied to Pin 2 and should have its DC level greater than the threshold level of the power comparator (Vcc/3). At the negative going edge of the trigger, as the trigger passes through (Vcc/3), the output of the lower comparator goes HIGH and sets the FF (Q=1,Q =0). During the positive excursion, when the threshold voltage at Pin 6 passes through (2/3) Vcc, the output of the upper comparator goes HIGH and resets the FF (Q = 0).

The reset input (Pin 4) provides a mechanism to reset the FF in a manner that overrides the effect of any instruction coming to FF from lower comparator. This overriding reset is effective when the reset input is less than about 0.4 V. When this reset is not used, it is returned to Vcc. The transistor Q2 serves as a buffer to isolate the reset input from the FF and transistor Q1. The transistor Q2 is driven by an internal reference voltage Vref obtained from supply voltage Vcc.

MONOSTABLE OPERATION:

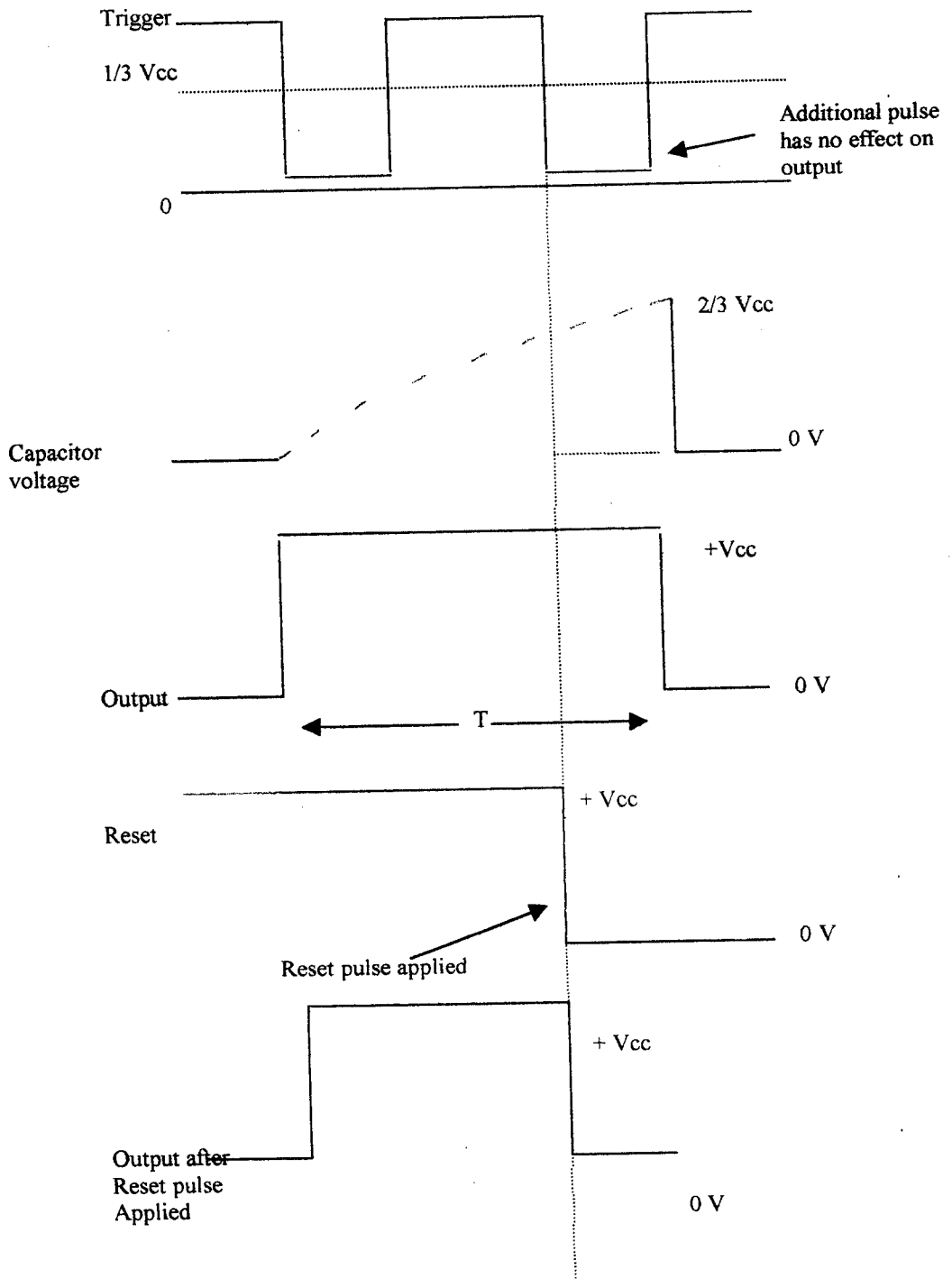
In the standby state, F holds transistor Q1 on, thus clamping the external timing capacitor C to ground. The output remains at ground potential (LOW). As the trigger passes through Vcc/3, the FF is set. This makes the transistor Q1 off and the short circuit across the timing

capacitor C is released. As Q is LOW, output goes HIGH (= Vcc). The timing cycle now begins. Since C is unclamped, voltage across it rises exponentially through R toward Vcc with a time constant RC. After a time period T the capacitor voltage is just greater than (2/3) Vcc and the upper comparator resets the FF, R=1,S=0. This makes Q = 1, transistor Q1 goes on, thereby discharging the capacitor C rapidly to ground potential. The output returns to the standby state or ground potential.

$$T = 1.1RC \text{ seconds}$$

The timing interval is independent of the supply voltage. Once triggered, the output remains in the HIGH state until time T elapses, which depends only upon R and C. Any additional trigger pulse coming during this time will not change the output state. However, if a negative going reset pulse is applied to the reset terminal (Pin 4) during the timing cycle, transistor Q2 goes off, Q1 becomes on and the external timing capacitor C is immediately discharged. The output will now be as in figure in the previous page.

It may be seen that the output of Q2 is connected directly to the input of Q1 so as to turn Q1 immediately and thereby avoid the propagation delay through FF. Now, even if the reset is released, the output will still remain LOW until a negative going trigger is again



TIMING PULSES OF THE IC555 TIMER

applied at Pin 2. The figure in the previous page shows a graph of the various combinations of R and C necessary to produce a given time delay.

FUNCTION OF RELAYS:

Relays are used in our circuit basically to control the hook switch and to switch on the amplifier. The relays are activated if signals are received from the output port of the PPI. They are basically electromagnetic devices, by which operation of one or more circuits are controlled by the operation of some mechanical contact and with their help, they control the operation of their circuits. They are required to produce impulses at rather high speed and are also used to receive signals at high speed at the receiving side. They are generally provided with one moving contact known as tongue.

There are mainly four types of contacts as given below:

**Make contacts: in this the contacts that are normally broken are made when the relay is operated*

**Break contacts: these are the normally made contacts that are broken by the operation of the relay.*

*Change over contacts: in this the movable contacts while changing over its positions by the operation of the relay breaks with one contacts and makes with the others.

*Make – Before – Break contacts: in this type when the relay is operated, one normally broken is first made and then only a second normally contact is first made and then only a second normally contact is broken.

When a current is passed through the coil of the relay, a magnetic flux is produced through the core. It's path is completed through the yoke, the armature and it moves against the force exerted by the different spring contacts and when it moves, the pin also moves up thereby moving all the spring contacts fixed to the pin and so the various contacts are operated.

The electromagnetic relay is basically a switch (or a combination of switches) operated by a current flowing through a coil. Essentially, it consists of four parts – an electromagnet comprising of a coil and a magnetic circuit, a movable armature, a set of contacts, and a frame to mount all these components. The relay used in our circuit is the clapper type relay. Although this relay has many variations, all have one feature in common – a hinged armature that is attracted to a core when the core is magnetized by a current in the coil wound around the core. It contains

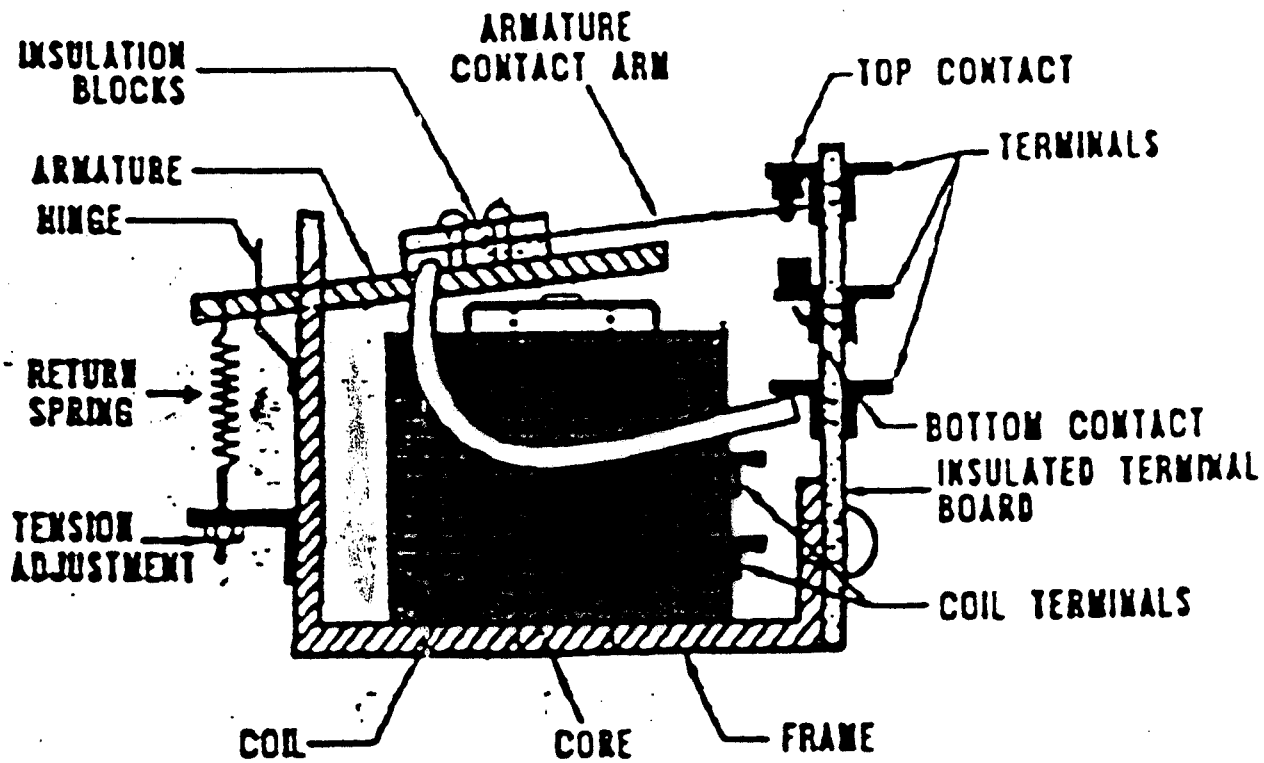


FIGURE OF ELECTROMAGNETIC RELAY

a core surrounded by a coil of wire. The core is mounted on a metal frame. The movable part is called armature. When a voltage is applied to the coil terminals, the current flowing through the coil produces a magnetic field in the core. In other words, the core acts as an electromagnet and attracts the metal armature. When the armature is attracted to the core, the magnetic path is from the core through the armature, through the frame, and back to the core. On removing the voltage, the spring attached to the armature returns the spring to its original position. In this position, there is a small air – gap in the magnetic path. Hence, more power is needed to keep it held in the attracted position.

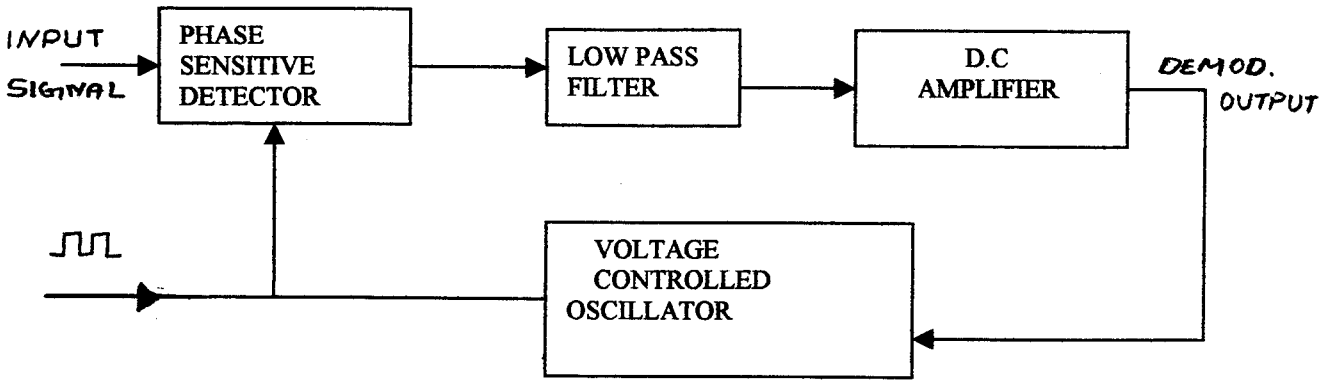
The relay contacts and the terminals are mounted on an insulating board. When no current flows through the relay coil, the contact arm, or pole as it is called, mounted on the armature, touches the top contact. When the coil is energized by the flow of current, the armature along with the contact arm, touches the bottom contact. The relay is actually a Single Pole Double Throw (SPDT) switch.

When an electric current is flowing through a relay coil, it is said to be energized and when the current flow stops, it is said to be de–energized. The commercially available clapper type relays have a set of parallel contacts that are all pulled On being energized, whether a relay makes contact(s) or breaks them depends on the design of the contact arrangements.

FUNCTION OF THE PHASE LOCKED LOOP:

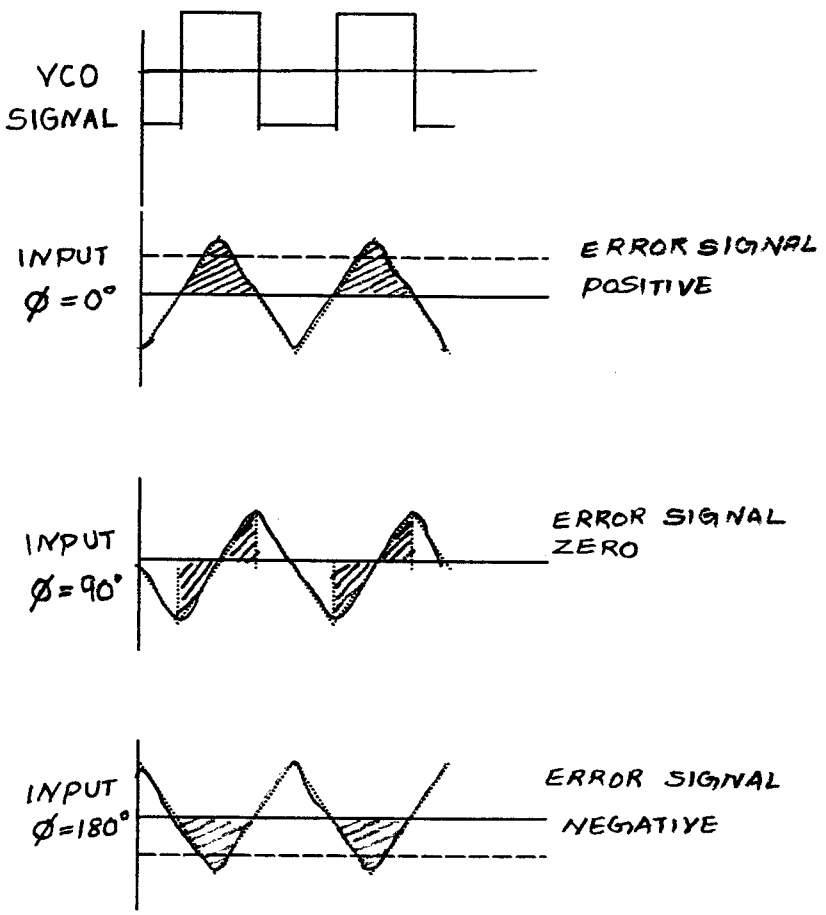
The receiver section in the circuit features a PLL IC 567 to lock the output frequency and phase to the frequency and phase of an input signal. In our circuit it acts as a tone decoder. PLL synchronizes the signal that is developed by an oscillator with an input signal in frequency as well as phase.

If the generated signal is matched with the reference signal, the phase difference between these two signals (error signal) is zero. The VCO is a free running multivibrator whose center frequency is determined by an external timing capacitor and an external resistor. Its center frequency can also be shifted to either side by application of a dc control voltage to appropriate terminal of the IC. The frequency deviation is directly proportional to the dc control voltage and hence it is called a 'voltage controlled oscillator' or in short as VCO. The VCO output is presented to a phase sensitive detector, where its phase is compared with that of the incoming signal. The detector produces a dc output whose magnitude is directly proportional to the phase difference. This is called the error signal and is first passed through a low-pass filter to remove the components of the VCO and input signal frequency and then amplified by a dc amplifier, called the 'error amplifier'.



BLOCK DIAGRAM OF PLL

WAVEFORMS



SOFTWARE

SOFTWARE DESCRIPTION

Port initialization of 8255 PPI is done by writing the appropriate control word in control register. Then port A is read for input from the ring detector. It is compared immediate with 01 and if it is not zero then hook switch relay is activated by giving the output to port B. The port C is then read for input from tone detector. This is compared immediate with 01,if it is zero means hook switch relay and amplifier power ON is activated by giving the output to port B and some delay is given for receiving the ECG signal.

After delay the hook switch and amplifier power is switched off. Then the program jumps to the start again and the whole procedure repeats again when the tone oscillator generates the pulse for signaling transmission of ECG signal.

PROGRAM ASSEMBLY FORM

PROGRAM TITLE : EPROM PROGRAMME

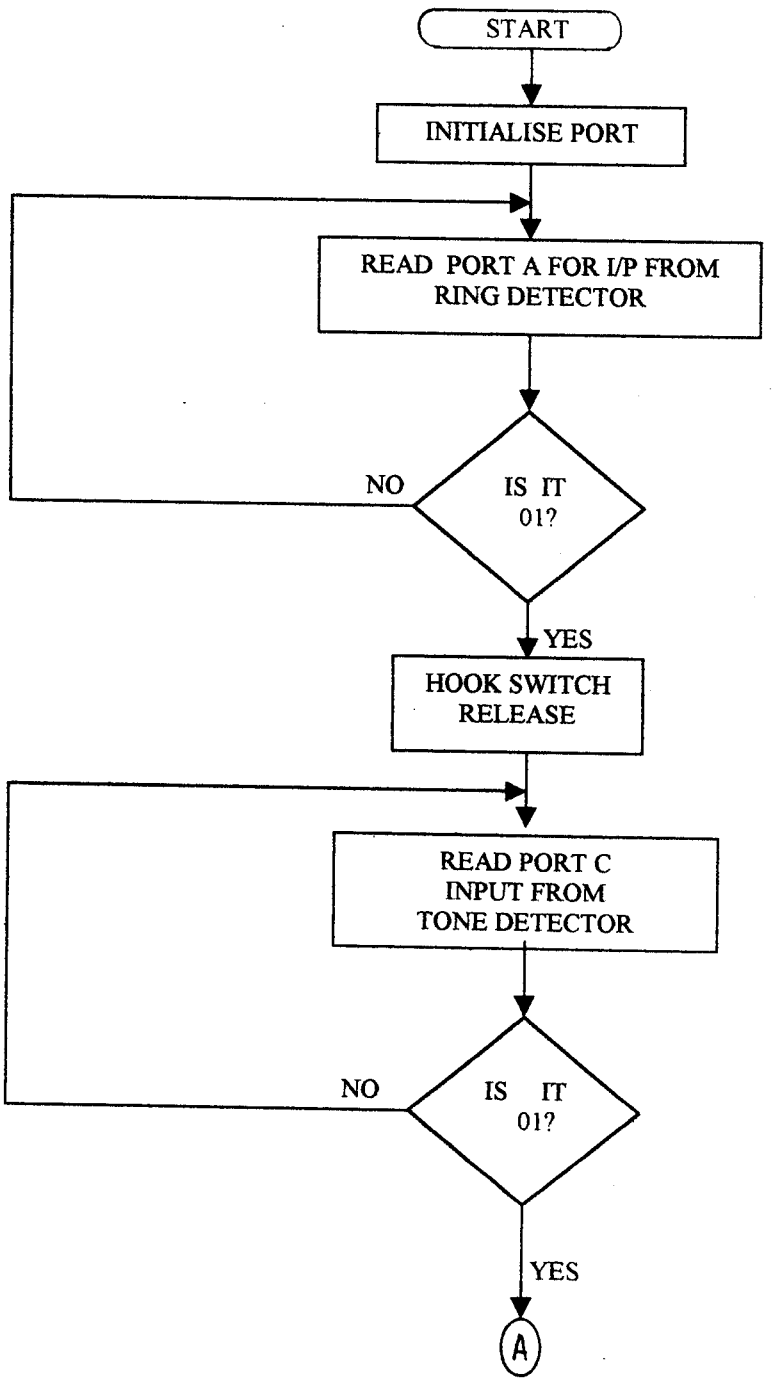
HEXADECIMAL		MNEMONIC INSTRUCTION			COMMENTS
ADDRESS	INSTR.	LABLE	OPCODE	OPERAND	
8000	3E	START:	MVI A	99	CONTROL WORD
8001	99				
8002	D3		OUT 03	03	CONTROL REGISI
8003	03				
8004	DB	L1:	IN	00	RING DETECTION
8005	00				
8006	FE		CPI	01	INPUT FROM POR
8007	01				IS COMPARED WI
8008	C2		JNZ	L1	01, IF ZERO JUC
8009	04				TO LOOP 1.
800A	80				
800B	3E		MVI A	01	IF NOT ZERO
800C	01				ACTIVATE THE
800D	D3		OUT	01	HOOK SWITCH REL
800E	01				
800F	DB	L2:	IN	02	TONE DETECTIO
8010	02				
8011	FE		CPI	01	PORTC INPUT IS
8012	01				COMPARED WITH
8013	C2		JNZ	L2	IF ZERO JUMP T
8014	0F				LOOP 2.
8015	80				
8016	3E		MVI A	03	IF NOT ZERO
8017	03				THE AMPLIFIER
8018	D3		OUT	01	POWER ON IS
8019	01				ACTIVATED
801A	11		LXI D	B4,00	
801B	B4				
801C	00				
801D	01	L4:	LXI B	FF FF	
801E	FF				
801F	FF				

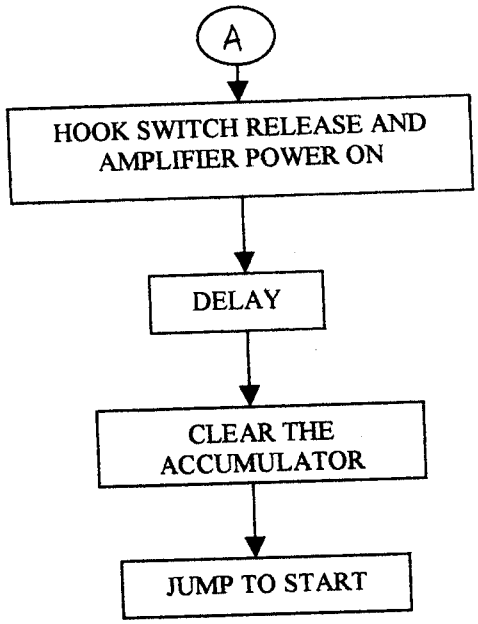
PROGRAM ASSEMBLY FORM

PROGRAM TITLE : EPROM PROGRAM

HEXADECIMAL		MNEMONIC INSTRUCTION			COMMENTS
ADDRESS	INSTR.	LABLE	OPCODE	OPERAND	
8020	0B	L3:	DCX	B	DELAY FOR
8021	79		MOV A	C	RECEIVING THE
8022	B0		ORA	B	ECM SIGNAL
8023	C2		JNZ	L3	
8024	20				
8025	80				
8026	1B		DCX	D	
8027	7B		MOV A	E	
8028	B2		ORA	D	
8029	C2		JNZ	L4	
802A	1D				
802B	80				
802C	3E		MVI A	00	
802D	00				
802E	D3		OUT	01	
802F	01				
8030	C3		JMP	START	PROGRAM JUMP
8031	00				TO START AGA
8032	80				

FLOW CHART


START
INITIALISE PORT
READ PORT A FOR I/P FROM RING DETECTOR
NO
IS IT 01?
YES
HOOK SWITCH RELEASE
READ PORT C INPUT FROM TONE DETECTOR
NO
IS IT 01?
YES
A


A
HOOK SWITCH RELEASE AND AMPLIFIER POWER ON
DELAY
CLEAR THE ACCUMULATOR
JUMP TO START

CONCLUSION

FUTURE ENHANCEMENTS...

BIBLIOGRAPHY

APPENDIX

intel

8085A/8085A-2
SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSORS

- Single +5V Power Supply
- 100% Software Compatible with 8080A
- 1.3 μs Instruction Cycle (8085A); 0.8 μs (8085A-2)
- On-Chip Clock Generator (with External Crystal, LC or RC Network)
- On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control
- Four Vectored Interrupt Inputs (One is non-Maskable) Plus an 8080A-compatible Interrupt
- Serial In/Serial Out Port
- Decimal, Binary and Double Precision Arithmetic
- Direct Addressing Capability to 64k Bytes of Memory

The Intel® 8085A is a complete 8 bit parallel Central Processing Unit (CPU). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's [8085A (CPU), 8156 (RAM/IO) and 8355/8755A (ROM/PROM/IO)] while maintaining total system expandability. The 8085A-2 is a faster version of the 8085A.

The 8085A incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A, thereby offering a high level of system integration.

The 8085A uses a multiplexed data bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of 8155/8156/8355/8755A memory products allow a direct interface with the 8085A.

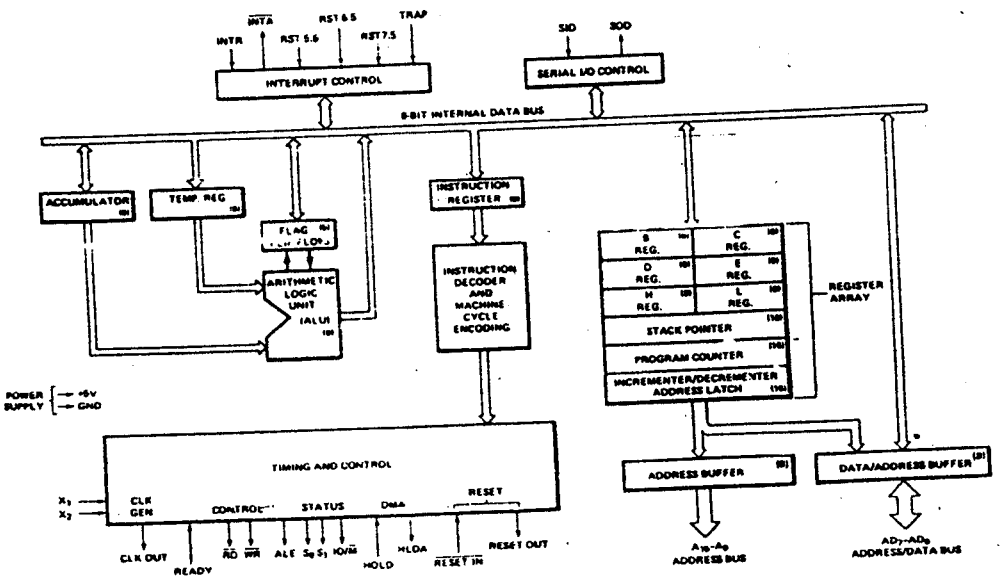


Figure 1. 8085A CPU Functional Block Diagram

BASIC SYSTEM TIMING

The 8085A has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Figure 9 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines ($IO/\overline{M}$, S_1, S_0) and the three control signals ($\overline{RD}$, $\overline{WR}$, and $\overline{INTA}$). (See Table 2.) The status lines can be used as advanced controls (for device selection, for example), since they become active at the T_1 state, at the outset of each machine cycle. Control lines $\overline{RD}$ and $\overline{WR}$ become active later, at the time when the transfer of data is to take place, so are used as command lines.

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless WAIT or HOLD states are forced by the receipt of $\overline{READY}$ or HOLD inputs). Any T state must be one of ten possible states, shown in Table 3.

TABLE 2. 8085A MACHINE CYCLE CHART

MACHINE CYCLE		STATUS			CONTROL		
		$IO/\overline{M}$	S1	S0	$\overline{RD}$	$\overline{WR}$	INTA
OPCODE FETCH	(OF)	0	1	1	0	1	1
MEMORY READ	(MR)	0	1	0	0	1	1
MEMORY WRITE	(MW)	0	0	1	1	0	1
I/O READ	(IOR)	1	1	0	0	1	1
I/O WRITE	(IOW)	1	0	1	1	0	1
ACKNOWLEDGE OF INTR	(INA)	1	1	1	1	1	0
BUS IDLE	(BI): DAD	0	1	0	1	1	1
	ACK. OF RST,TRAP	1	1	1	1	1	1
	HALT	TS	0	0	TS	TS	1

TABLE 3. 8085A MACHINE STATE CHART

Machine State	Status & Buses				Control		
	$S1,S0$	$IO/\overline{M}$	A_8–A_{15}	AD_0–AD_7	$\overline{RD},\overline{WR}$	INTA	ALE
T_1	X	X	X	X	1	1	1*
T_2	X	X	X	X	X	X	0
T_{WAIT}	X	X	X	X	X	X	0
T_3	X	X	X	X	X	X	0
T_4	1	0†	X	TS	1	1	0
T_5	1	0†	X	TS	1	1	0
T_6	1	0†	X	TS	1	1	0
T_{RESET}	X	TS	TS	TS	TS	1	0
T_{HALT}	0	TS	TS	TS	TS	1	0
T_{HOLD}	X	TS	TS	TS	TS	1	0

0 = Logic "0"
1 = Logic "1"
TS = High Impedance
X = Unspecified

* ALE not generated during 2nd and 3rd machine cycles of DAD instruction.
† IO/M = 1 during T_4–T_6 of INA machine cycle.

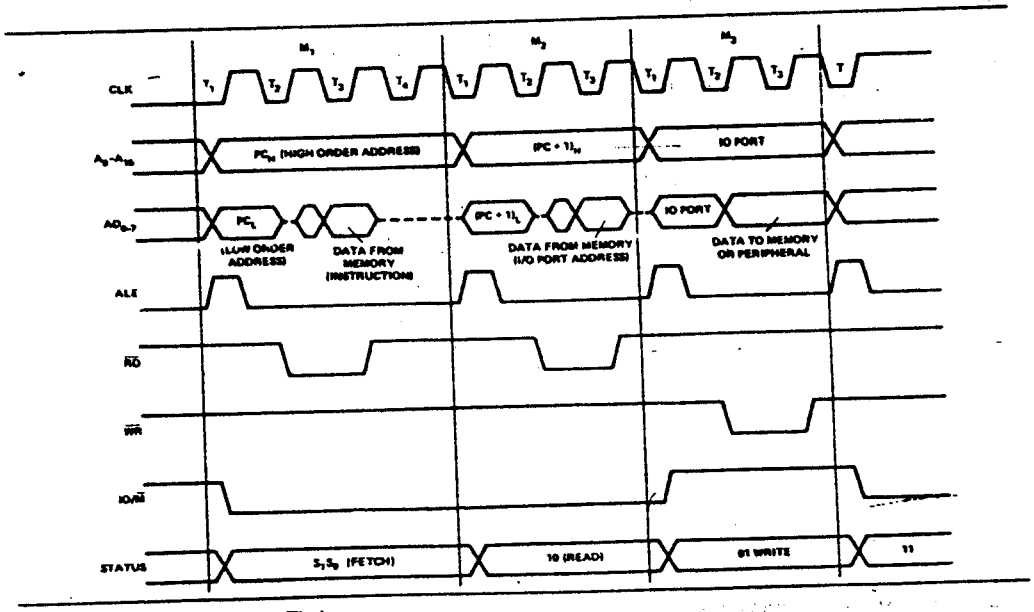


Figure 9. 8085A Basic System Timing

TABLE 4. ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin With Respect to Ground	−0.5V to +7V
Power Dissipation	1.5 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 5. D.C. CHARACTERISTICS

(T_A = 0°C to 70°C; V_{CC} = 5V ±5%; V_{SS} = 0V; unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400μA
I_{CC}	Power Supply Current		170	mA	
I_{IL}	Input Leakage		±10	μA	$V_{in} = V_{CC}$
I_{LO}	Output Leakage		±10	μA	$0.45V \leq V_{out} \leq V_{CC}$
V_{ILR}	Input Low Level, RESET	-0.5	+0.8	V	
V_{IHR}	Input High Level, RESET	2.4	V_{CC}+0.5	V	
V_{HY}	Hysteresis, RESET	0.25		V	

TABLE 6. A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$; $V_{CC} = 5V \pm 5\%$; $V_{SS} = 0V$

Symbol	Parameter	8085A[2]		8085A-2[2] (Preliminary)		Units
		Min.	Max.	Min.	Max.	
t_{CYC}	CLK Cycle Period	320	2000	200	2000	ns
t_1	CLK Low Time (Standard CLK Loading)	80		40		ns
t_2	CLK High Time (Standard CLK Loading)	120		70		ns
t_r, t_f	CLK Rise and Fall Time		30		30	ns
t_{XKR}	X_1 Rising to CLK Rising	30	120	30	100	ns
t_{XKF}	X_1 Rising to CLK Falling	30	150	30	110	ns
t_{AC}	A_{8-15} Valid to Leading Edge of Control[1]	270		115		ns
t_{ACL}	A_{0-7} Valid to Leading Edge of Control	240		115		ns
t_{AD}	A_{0-15} Valid to Valid Data In		575		350	ns
t_{AFR}	Address Float After Leading Edge of $\overline{READ}$ ($\overline{INTA}$)		0		0	ns
t_{AL}	A_{8-15} Valid Before Trailing Edge of ALE[1]	115		50		ns
t_{ALL}	A_{0-7} Valid Before Trailing Edge of ALE	90		50		ns
t_{ARY}	READY Valid from Address Valid		220		100	ns
t_{CA}	Address (A_{8-15}) Valid After Control	120		60		ns
t_{CC}	Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$)	400		230		ns
t_{CL}	Trailing Edge of Control to Leading Edge of ALE	50		25		ns
t_{DW}	Data Valid to Trailing Edge of $\overline{WRITE}$	420		230		ns
t_{HABE}	HLDA to Bus Enable		210		150	ns
t_{HABF}	Bus Float After HLDA		210		150	ns
t_{HACK}	HLDA Valid to Trailing Edge of CLK	110		40		ns
t_{HDH}	HOLD Hold Time	0		0		ns
t_{HDS}	HOLD Setup Time to Trailing Edge of CLK	170		120		ns
t_{INH}	INTR Hold Time	0		0		ns
t_{INS}	INTR, RST, and TRAP Setup Time to Falling Edge of CLK	160		150		ns
t_{LA}	Address Hold Time After ALE	100		50		ns
t_{LC}	Trailing Edge of ALE to Leading Edge of Control	130		60		ns
t_{LCK}	ALE Low During CLK High	100		50		ns
t_{LDR}	ALE to Valid Data During Read		460		270	ns
t_{LDW}	ALE to Valid Data During Write		200		120	ns
t_{LL}	ALE Width	140		80		ns
t_{LRY}	ALE to READY Stable		110		30	ns

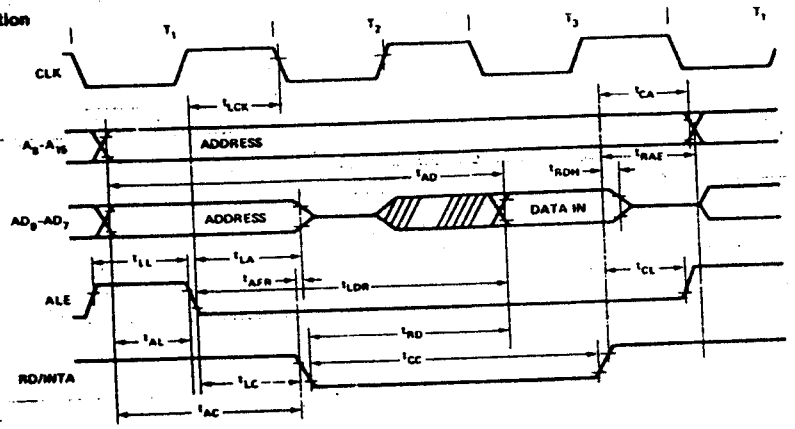
Table 6. A.C. Characteristics (Cont.)

Symbol	Parameter	8085A[2]		8085A-2[2] (Preliminary)		Units
		Min.	Max.	Min.	Max.	
t_{RAE}	Trailing Edge of $\overline{READ}$ to Re-Enabling of Address	150		90		ns
t_{RD}	$\overline{READ}$ (or $\overline{INTA}$) to Valid Data	400	300	220	150	ns
t_{RV}	Control Trailing Edge to Leading Edge of Next Control	0		0		ns
t_{RDH}	Data Hold Time After $\overline{READ}$ $\overline{INTA}$[7]	0		0		ns
t_{RYH}	READY Hold Time	110		100		ns
t_{RYS}	READY Setup Time to Leading Edge of CLK	100		60		ns
t_{WD}	Data Valid After Trailing Edge of $\overline{WRITE}$		40		20	ns
t_{WDL}	LEADING Edge of WRITE to Data Valid					ns

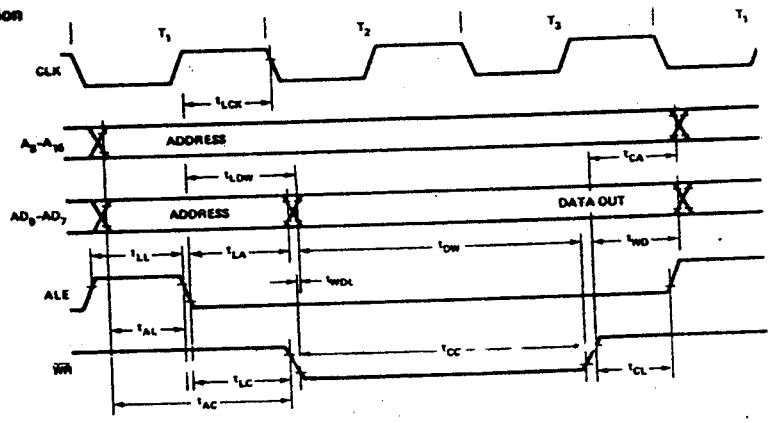
Notes:
1. A_8-A_{15} address Specs apply to IO/$\overline{M}$, S_0, and S_1 except A_8-A_{15} are undefined during T_4-T_6 of OF cycle whereas IO/$\overline{M}$, S_0, and S_1 are stable.
2. Test conditions: t_{CYC} = 320 ns (8085A)/200 ns (8085A-2); C_L = 150 pF.
3. For all output timing where C_L = 150 pF use the following correction factors:
   25 pF ≤ C_L < 150 pF: −0.10 ns/pF
   150 pF < C_L ≤ 300 pF: +0.30 ns/pF
4. Output timings are measured with purely capacitive load.
5. All timings are measured at output votage V_L = 0.8V, V_H = 2.0V, and 1.5V with 20 ns rise and fall time on inputs.
6. To calculate timing specifications at other values of t_{CYC} use Table 7.
7. Data hold time is guaranteed under all loading conditions

Input Waveform for A.C. Tests:

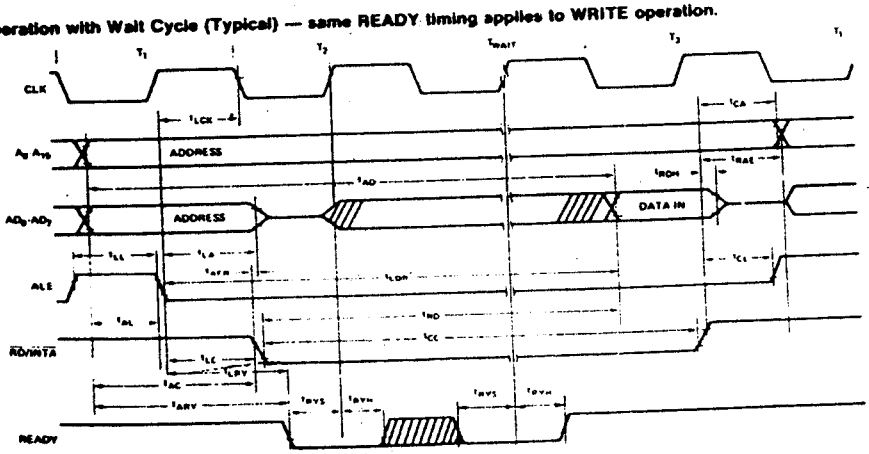
Read Operation



Write Operation



Read operation with Wait Cycle (Typical) — same READY timing applies to WRITE operation.



NOTE 1: READY MUST REMAIN STABLE DURING SETUP AND HOLD TIMES.

Figure 11. 8085A Bus Timing, With and Without Wait

Hold Operation

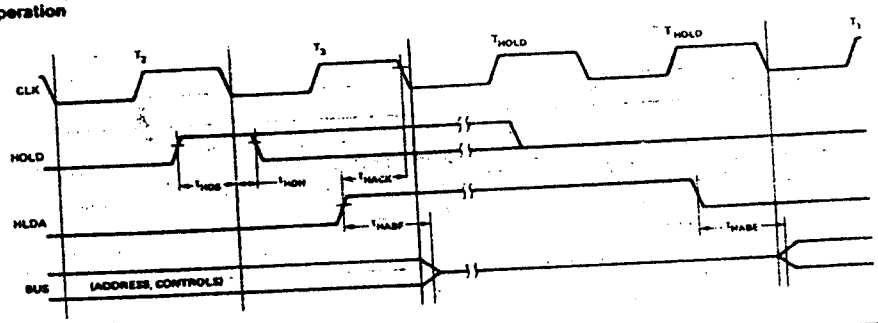


Figure 12. 8085A Hold Timing.

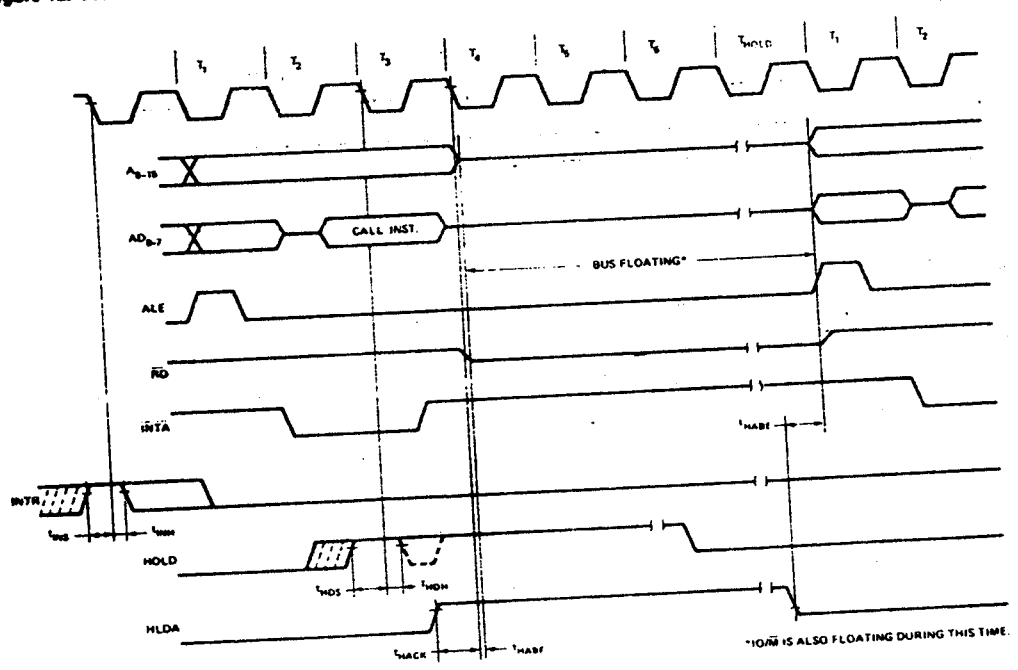


Figure 13. 8085A Interrupt and Hold Timing

8085A INSTRUCTION SET SUMMARY BY FUNCTIONAL GROUPING

Table 6-1

Mnemonic	Description	Instruction Code (1) D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Page
MOVE, LOAD, AND STORE										
MOV r1,r2	Move register to register	0	1	D	D	D	S	S	S	5-4
MOV M,r	Move register to memory	0	1	1	1	0	S	S	S	5-4
MOV r,M	Move memory to register	0	1	D	D	D	1	1	0	5-4
MVI r	Move immediate register	0	0	D	D	D	1	1	0	5-4
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	5-4
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	5-5
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	5-5
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	5-5
STAX B	Store A indirect	0	0	0	0	0	0	1	0	5-6
STAX D	Store A indirect	0	0	0	1	0	0	1	0	5-6
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	5-5
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	5-5
STA	Store A direct	0	0	1	1	0	0	1	0	5-5
LDA	Load A direct	0	0	1	1	1	0	1	0	5-5
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	5-5
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	5-5
XCHG	Exchange D & E, H & L Registers	1	1	1	0	1	0	1	1	5-6
STACK OPS										
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	5-15
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	5-15
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	5-15
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	5-15
POP B	Pop register Pair B & C off stack	1	1	0	0	0	0	0	1	5-15
POP D	Pop register Pair D & E off stack	1	1	0	1	0	0	0	1	5-15
POP H	Pop register Pair H & L off stack	1	1	1	0	0	0	0	1	5-15
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	5-15
XTHL	Exchange top of stack, H & L	1	1	1	0	0	0	1	1	5-16
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	5-16
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	5-5
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	5-9
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	5-9
JUMP										
JMP	Jump unconditional	1	1	0	0	0	0	1	1	5-13
JC	Jump on carry	1	1	0	1	1	0	1	0	5-13
JNC	Jump on no carry	1	1	0	1	0	0	1	0	5-13
JZ	Jump on zero	1	1	0	0	1	0	1	0	5-13
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	5-13
JP	Jump on positive	1	1	1	1	0	0	1	0	5-13
JM	Jump on minus	1	1	1	1	1	0	1	0	5-13
JPE	Jump on parity even	1	1	1	0	1	0	1	0	5-13
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	5-13
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	5-15
CALL										
CALL	Call unconditional	1	1	0	0	1	1	0	1	5-13
CC	Call on carry	1	1	0	1	1	1	0	0	5-14
CNC	Call on no carry	1	1	0	1	0	1	0	0	5-14
CZ	Call on zero	1	1	0	0	1	1	0	0	5-14
CNZ	Call on no zero	1	1	0	0	0	1	0	0	5-14
CP	Call on positive	1	1	1	1	0	1	0	0	5-14
CM	Call on minus	1	1	1	1	1	1	0	0	5-14
CPE	Call on parity even	1	1	1	0	1	1	0	0	5-14
CPO	Call on parity odd	1	1	1	0	0	1	0	0	5-14
RETURN										
RET	Return	1	1	0	0	1	0	0	1	5-14
RC	Return on carry	1	1	0	1	1	0	0	0	5-14
RNC	Return on no carry	1	1	0	1	0	0	0	0	5-14
RZ	Return on zero	1	1	0	0	1	0	0	0	5-14
RNZ	Return on no zero	1	1	0	0	0	0	0	0	5-14
RP	Return on positive	1	1	1	1	0	0	0	0	5-14
RM	Return on minus	1	1	1	1	1	0	0	0	5-14
RPE	Return on parity even	1	1	1	0	1	0	0	0	5-14
RPO	Return on parity odd	1	1	1	0	0	0	0	0	5-14
RESTART										
RST	Restart	1	1	A	A	A	1	1	1	5-14
INPUT/OUTPUT										
IN	Input	1	1	0	1	1	0	1	1	5-16
OUT	Output	1	1	0	1	0	0	1	1	5-16
INCREMENT AND DECREMENT										
INR r	Increment register	0	0	D	D	D	1	0	0	5-8
DCR r	Decrement register	0	0	D	D	D	1	0	1	5-8
INR M	Increment memory	0	0	1	1	0	1	0	0	5-8
DCR M	Decrement memory	0	0	1	1	0	1	0	1	5-8
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	5-9
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	5-9
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	5-9
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	5-9
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	5-9
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	5-9
ADD										
ADD r	Add register to A	1	0	0	0	0	S	S	S	5-6
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	5-6
ADD M	Add memory to A	1	0	0	0	0	1	1	0	5-6
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	5-7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	5-6
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	5-7
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	5-9
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	5-9
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	5-9
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	5-9
SUBTRACT										
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	5-7
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	5-7
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	5-7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	5-8
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	5-7

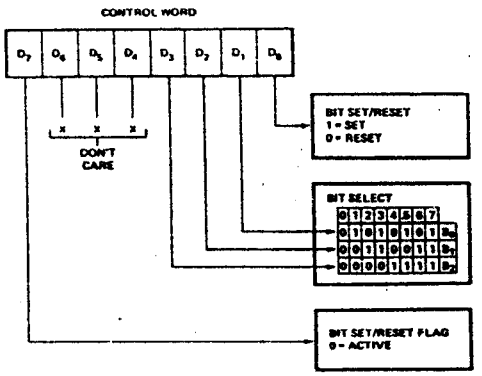


Figure 5. Bit Set/Reset Format

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 8255A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET) — INTE is SET — Interrupt enable
(BIT-RESET) — INTE is RESET — Interrupt disable

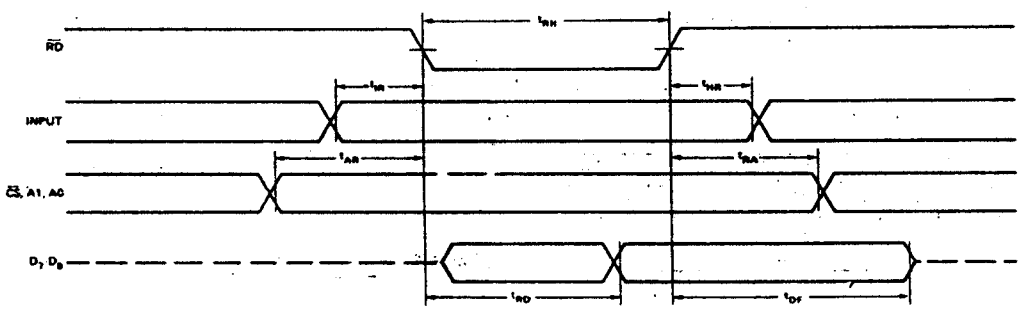
Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

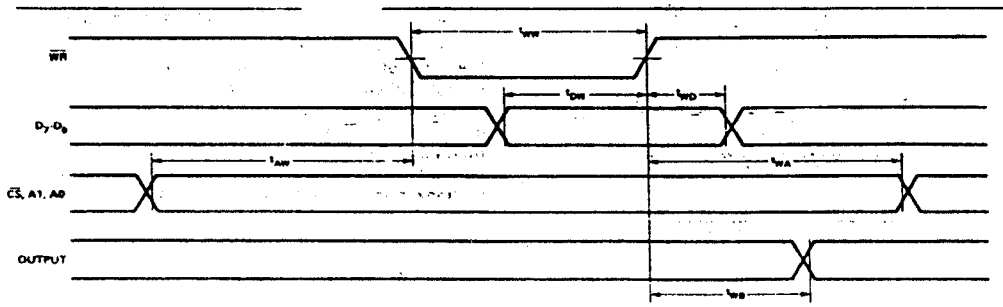
MODE 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.



MODE 0 (Basic Input)



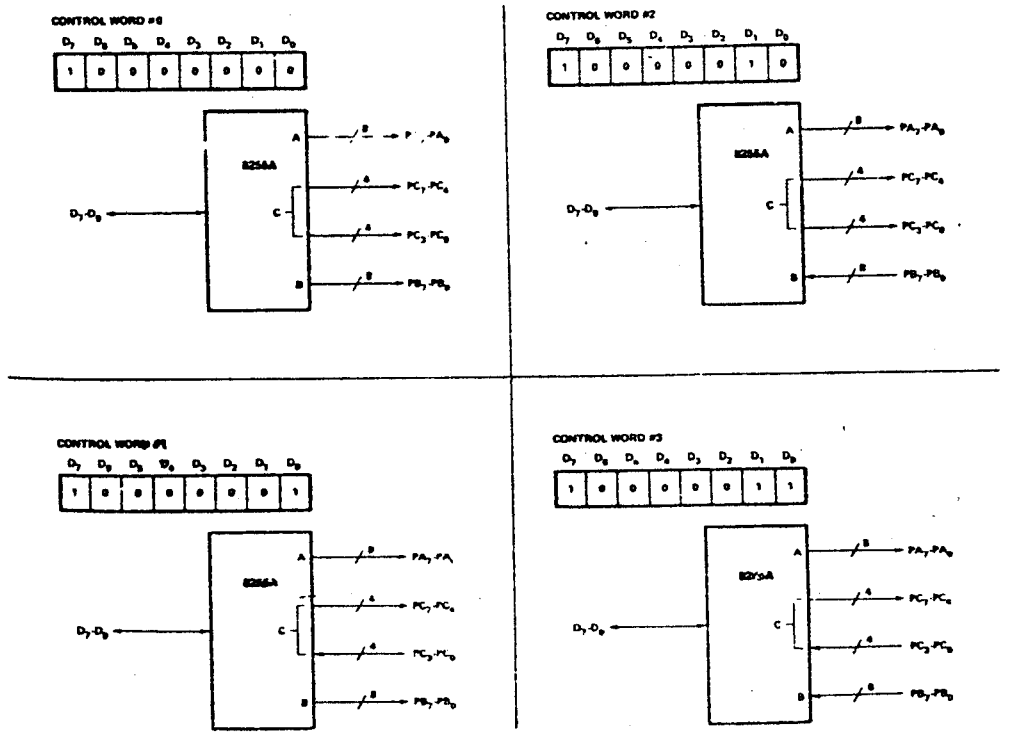
MODE 0 (Basic Output)

00744A

MODE 0 Port Definition

A		B		GROUP A			GROUP B	
D_4	D_3	D_1	D_0	PORT A	PORT C (UPPER)	#	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

MODE 0 Configurations



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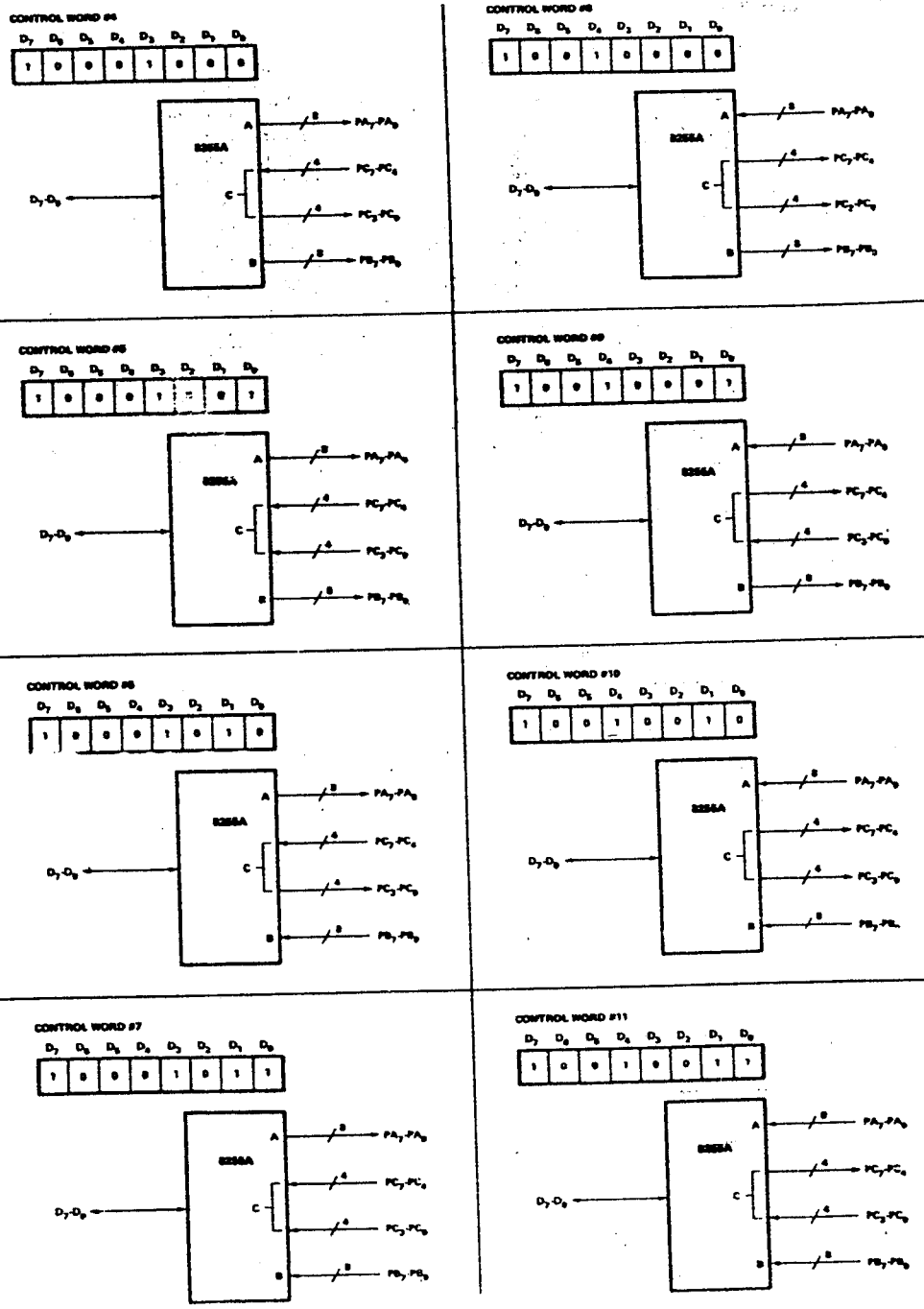
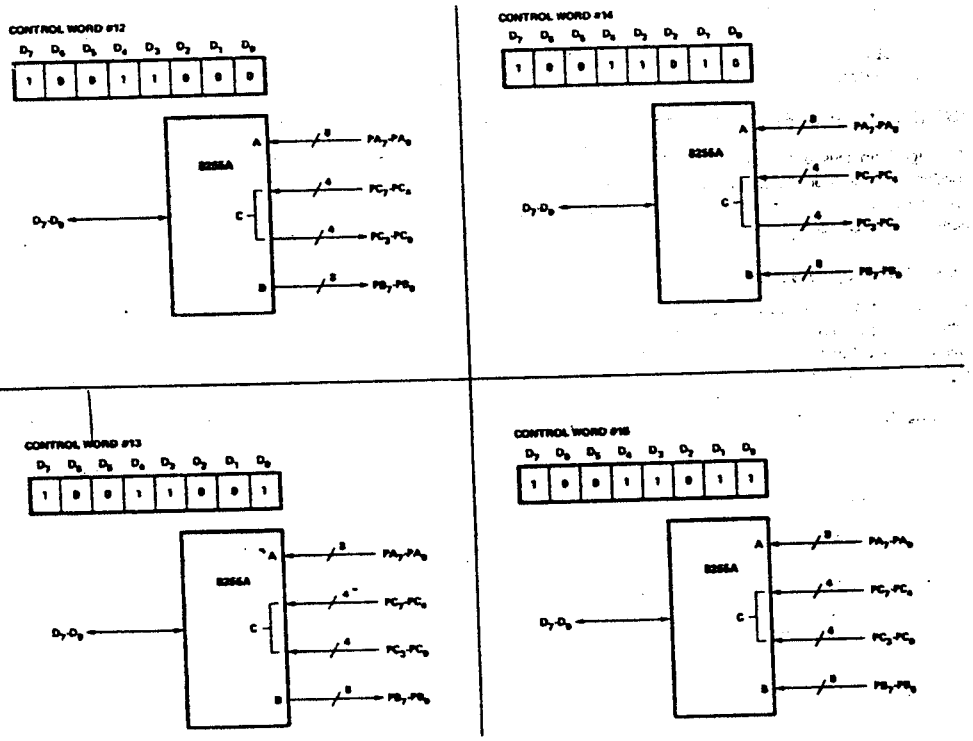

CONTROL WORD #4
CONTROL WORD #8
CONTROL WORD #5
CONTROL WORD #9
CONTROL WORD #6
CONTROL WORD #10
CONTROL WORD #7
CONTROL WORD #11
8255A
A
B
C

00744A



Operating Modes

MODE 1 (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, port A and Port B use the lines on port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

intel

PRELIMINA
Notice: This is not a final specification
parametric limits are subject to change

2732
32K (4K x 8) UV ERASABLE PROM

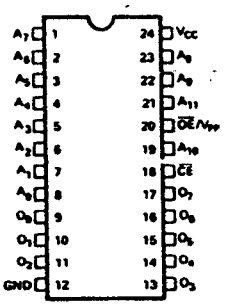
- **Fast Access Time:**
  - **— 450 ns Max. 2732**
  - **— 550 ns Max. 2732-6**
- **Single +5V ± 5% Power Supply**
- **Output Enable for MCS-85™ and MCS-86™ Compatibility**
- **Low Power Dissipation:**
  150mA Max. Active Current
  30mA Max. Standby Current
- **Pin Compatible to Intel® 2716 EPROM**
- **Completely Static**
- **Simple Programming Requirements**
  - **— Single Location Programming**
  - **— Programs with One 50ms Pulse**
- **Three-State Output for Direct Bus Interface**

The Intel® 2732 is a 32,768-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2732 operates from a single 5-volt power supply, has a standby mode, and features an output enable control. The total programming time for all bits is three and a half minutes. All these features make designing with the 2732 in microcomputer systems faster, easier, and more economical.

An important 2732 feature is the separate output control, Output Enable ($\overline{OE}$), from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems. Intel's Application Note AP-30 describes the microprocessor system implementation of the $\overline{OE}$ and $\overline{CE}$ controls on Intel's 2716 and 2732 EPROMs. AP-30 is available from Intel's Literature Department.

The 2732 has a standby mode which reduces the power dissipation without increasing access time. The maximum active current is 150mA, while the maximum standby current is only 30mA, an 80% savings. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input.

PIN CONFIGURATION



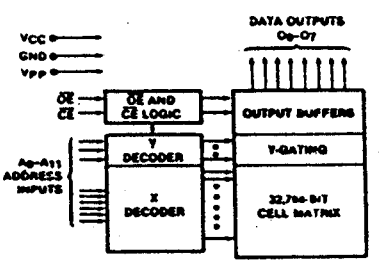
MODE SELECTION

MODE \ PINS	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	OUTPUTS (9-11,13-17)
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

PIN NAMES

A_0-A_{11}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS

BLOCK DIAGRAM



PROGRAMMING

The programming specifications are described in the Data Catalog PROMIROM Programming Instructions.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-10°C to +80°C
Storage Temperature	-65°C to +125°C
All Input or Output Voltages with Respect to Ground	+6V to -0.3V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ± 5%

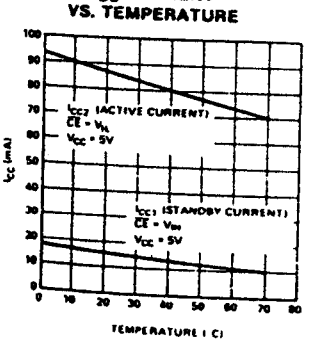
READ OPERATION

Symbol	Parameter	Limits Min.	Typ. [1]	Max.	Unit	Conditions
I_{LI1}	Input Load Current (except $\overline{OE}/V_{PP}$)			10	µA	V_{IN} = 5.25V
I_{LI2}	$\overline{OE}/V_{PP}$ Input Load Current			10	µA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = 5.25V
I_{CC1}	V_{CC} Current (Standby)		15	30	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}
I_{CC2}	V_{CC} Current (Active)		85	150	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
V_{IL}	Input Low Voltage	-0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400µA

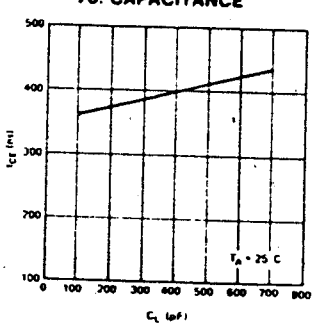
Note: 1. Typical values are for T_A = 25°C and nominal supply voltages.

TYPICAL CHARACTERISTICS

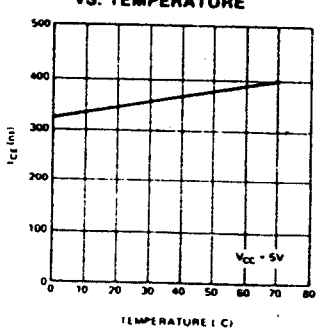
I_{CC} CURRENT VS. TEMPERATURE



$\overline{CE}$ TO OUTPUT DELAY (t_{CE}) VS. CAPACITANCE



$\overline{CE}$ TO OUTPUT DELAY (t_{CE}) VS. TEMPERATURE



A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ± 5%

Symbol	Parameter	2732 Limits		2732-6 Limits		Unit	Test Conditions
		Min.	Max.	Min.	Max.		
t_{ACC}	Address to Output Delay		450		550	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		450		550	ns	$\overline{OE} = V_{IL}$
t_{OE}	Output Enable to Output Delay		120		120	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Float	0	100	0	100	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

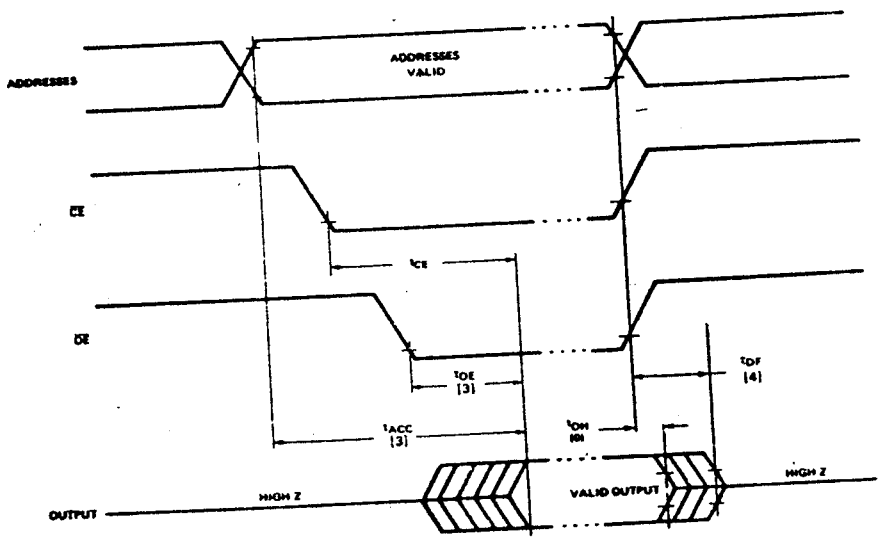
CAPACITANCE [1] T_A = 25°C, f = 1MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN1}	Input Capacitance Except $\overline{OE}/V_{PP}$	4	6	pF	V_{IN} = 0V
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance		20	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance		12	pF	V_{OUT} = 0V

A.C. TEST CONDITIONS

Output Load: 1 TTL gate and C_L = 100pF
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. WAVEFORMS [2]



NOTES:
1. THIS PARAMETER IS ONLY SAMPLED AND IS NOT 100% TESTED.
2. ALL TIMES SHOWN IN PARENTHESES ARE MINIMUM TIMES AND ARE NSEC UNLESS OTHERWISE SPECIFIED.
3. $\overline{OE}$ MAY BE DELAYED UP TO $t_{ACC} - t_{OE}$ AFTER THE FALLING EDGE OF $\overline{CE}$ WITHOUT IMPACT ON t_{ACC}.
4. t_{DF} IS SPECIFIED FROM $\overline{OE}$ OR $\overline{CE}$, WHICHEVER OCCURS FIRST.

ERASURE CHARACTERISTICS

The erasure characteristics of the 2732 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 2732 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 2732 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 2732 window to prevent unintentional erasure.

The recommended erasure procedure (see Data Catalog page 4-83) for the 2732 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The 2732 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

DEVICE OPERATION

The five modes of operation of the 2732 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL level to 25V.

TABLE 1. Mode Selection

PINS / MODE	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	OUTPUTS (9-11,13-17)
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

Read Mode

The 2732 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs 120ns (t_{OE}) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The 2732 has a standby mode which reduces the active power current by 80%, from 150mA to 30mA. The 2732 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state independent of the $\overline{OE}$ input.

Output OR-Tieing

Because EPROMs are usually used in larger memory arrays, Intel has provided a 2 line control function that accommodates this use of multiple memory connections. The two line control function allows for:

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

Programming

Initially, and after each erasure, all bits of the 2732 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2732 is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 25V. It is required that a 0.1μF capacitor be placed across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50msec, active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time — either individually, sequentially, or at random. The program pulse has a maximum width of 55msec. The 2732 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of multiple 2732s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2732s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled 2732s.

Program Inhibit

Programming of multiple 2732s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel 2732s may be common. A TTL level program pulse applied to a 2732's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 25V will program that 2732. A high level $\overline{CE}$ input inhibits the other 2732s from being programmed.

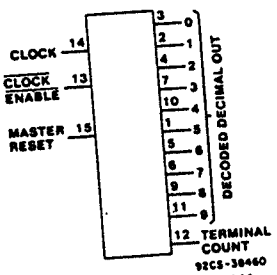
Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified tov after the falling edge of $\overline{CE}$.

File Number 1639

CD54/74HC4017
CD54/74HCT4017

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM
CD54/74HC4017, CD54/74HCT4017

Decade Counter/Divider with 10 Decoded Outputs

Type Features:
- *Fully static operation*
- *Buffered inputs*
- *Common reset*
- *Positive edge clocking*
- *Typical f_{MAX} = 50 MHz @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25° C*

The RCA-CD54/74HC4017 and CD54/74HCT4017 are high speed silicon gate CMOS 5-stage Johnson counters with 10 decoded outputs. Each of the decoded outputs is normally low and sequentially goes high on the low to high transition of the CLOCK (CP) input. Each output stays high for one clock period of the 10 clock period cycle. The CARRY (TC) output transitions low to high after OUTPUT 10 goes low, and can be used in conjunction with the CLOCK ENABLE ($\overline{CE}$) to cascade several stages. The CLOCK ENABLE input disables counting when in the high state. A RESET (MR) input is also provided which when taken high sets all the decoded outputs, except "0", low.

The device can drive up to 10 low power Schottky equivalent loads. The CD54/74HCT4017 is an enhanced version of equivalent CMOS types.

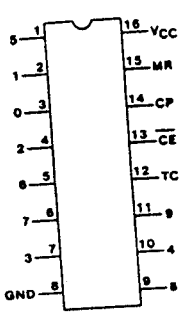
The CD54HC4017 and CD54HCT4017 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC4017 and CD74HCT4017 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

TRUTH TABLE

CP	$\overline{CE}$	MR	Output State*
L	X	L	No Change
X	H	L	No Change
X	X	H	"O"=H, "1"-"9"=L
↘	L	L	Increments Counter
↗	X	L	No Change
X	↗	L	No Change
H	↘	L	Increments Counter

H = High Level
L = Low Level
↘ = High-to-Low Transition
↗ = Low-to-High Transition
X=Don't Care
*If n<5 TC=H, Otherwise=L

Family Features:
- *Fanout (Over Temperature Range):*
  Standard Outputs — 10 LSTTL Loads
  Bus Driver Outputs — 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} @ V_{CC} = 5V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC4017
CD54/74HCT4017

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}): -0.5 to +7 V
(Voltages referenced to ground) ± 20 mA
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V) ± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V) ± 25 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} + 0.5$ V) ± 50 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC})
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to −60°C (PACKAGE TYPE E) 500 mW
For T_A = +60 to −85°C (PACKAGE TYPE E) Derate Linearly at 8 mW/°C to 300 mW
For T_A = −55 to +100°C (PACKAGE TYPE F, H) 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) Derate Linearly at 8 mW/°C to 300 mW
For T_A = −40 to +70°C (PACKAGE TYPE M) 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H −55 to +125°C
PACKAGE TYPE E, M −40 to +85°C
STORAGE TEMPERATURE (T_{stg}) −65 to −150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only +300°C

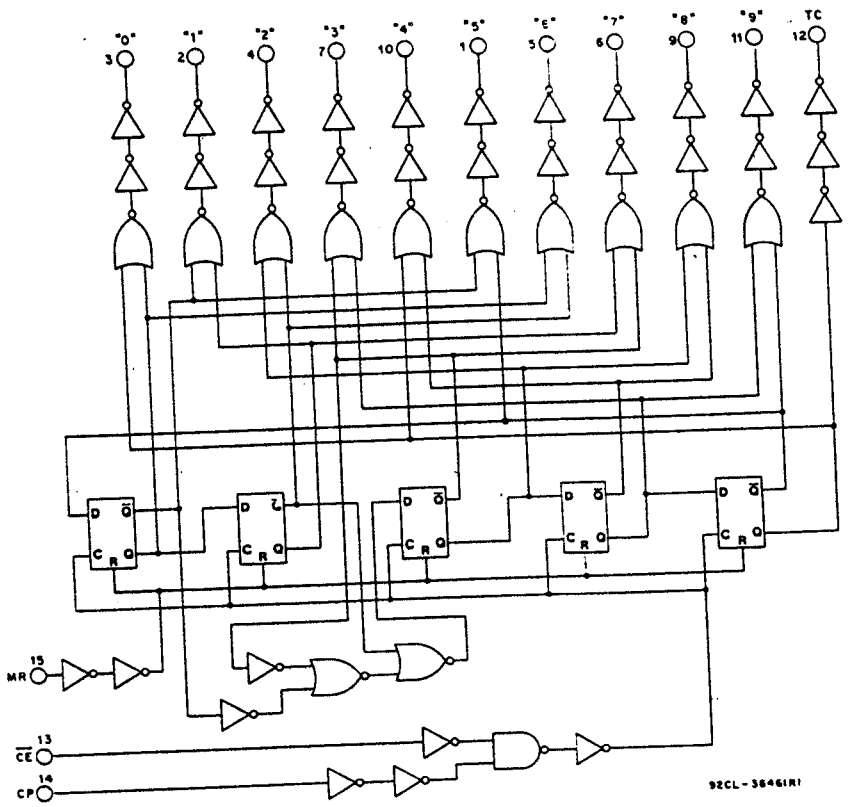


Fig. 1 — Logic diagram for the CD54/74HC/HCT 4017

CD54/74HC4017
CD54/74HCT4017

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	TEST CONDITION V_{CC} V	LIMITS 25°C HC Min.	HC Max.	HCT Min.	HCT Max.	-40°C to +85°C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55°C to +125°C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
CP Pulse Width t_w	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
	4.5	16	—	16	—	20	—	20	—	24	—	24	—	
	6	14	—	—	—	17	—	—	—	20	—	—	—	
MR Pulse Width t_w	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
	4.5	16	—	16	—	20	—	20	—	24	—	24	—	
	6	14	—	—	—	17	—	—	—	20	—	—	—	
Max. Clock Freq. f_{CL} (max.)	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
	4.5	30	—	25	—	35	—	20	—	20	—	17	—	
	6	35	—	—	—	49	—	—	—	23	—	—	—	
$\overline{CE}$ to CP Setup Time t_{su}	2	75	—	—	—	95	—	—	—	110	—	—	—	ns
	4.5	15	—	15	—	19	—	19	—	22	—	22	—	
	6	13	—	—	—	16	—	—	—	19	—	—	—	
$\overline{CE}$ to CP Hold Time t_H	2	0	—	—	—	0	—	—	—	0	—	—	—	ns
	4.5	0	—	0	—	0	—	0	—	0	—	0	—	
	6	0	—	—	—	0	—	—	—	0	—	—	—	
MR Removal Time t_{REM}	2	5	—	—	—	5	—	—	—	5	—	—	—	ns
	4.5	5	—	5	—	5	—	5	—	5	—	5	—	
	6	5	—	—	—	5	—	—	—	5	—	—	—	

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C HC Min.	HC Max.	HCT Min.	HCT Max.	-40°C to +85°C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55°C to +125°C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Propagation Delay CP to any Dec. Out	t_{PLH} t_{PHL}	2	—	230	—	—	—	290	—	—	—	345	—	—	ns
		4.5	—	46	—	46	—	58	—	58	—	69	—	69	
		6	—	39	—	—	—	49	—	—	—	59	—	—	
CP to TC	t_{PLH} t_{PHL}	2	—	230	—	—	—	290	—	—	—	345	—	—	ns
		4.5	—	46	—	46	—	58	—	58	—	69	—	69	
		6	—	39	—	—	—	49	—	—	—	59	—	—	
$\overline{CE}$ to any Dec. Out	t_{PLH} t_{PHL}	2	—	250	—	—	—	315	—	—	—	375	—	—	ns
		4.5	—	50	—	50	—	63	—	63	—	75	—	75	
		6	—	43	—	—	—	54	—	—	—	64	—	—	
$\overline{CE}$ to TC	t_{PLH} t_{PHL}	2	—	250	—	—	—	315	—	—	—	375	—	—	ns
		4.5	—	50	—	50	—	63	—	63	—	75	—	75	
		6	—	43	—	—	—	54	—	—	—	64	—	—	
MR to any Dec. Out	t_{PLH} t_{PHL}	2	—	230	—	—	—	290	—	—	—	345	—	—	ns
		4.5	—	46	—	46	—	58	—	58	—	69	—	69	
		6	—	39	—	—	—	49	—	—	—	59	—	—	
MR to TC	t_{PLH} t_{PHL}	2	—	230	—	—	—	290	—	—	—	345	—	—	ns
		4.5	—	46	—	46	—	58	—	58	—	69	—	69	
		6	—	39	—	—	—	49	—	—	—	59	—	—	
Transition Time TC, Dec. Out	t_{THL} t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_{IN}		—	10	—	10	—	10	—	10	—	10	—	10	pF

CD54/74HC4017
CD54/74HCT4017

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2V	0	1000	ns
at 4.5 V	0	500	ns
at 6V	0	400	ns

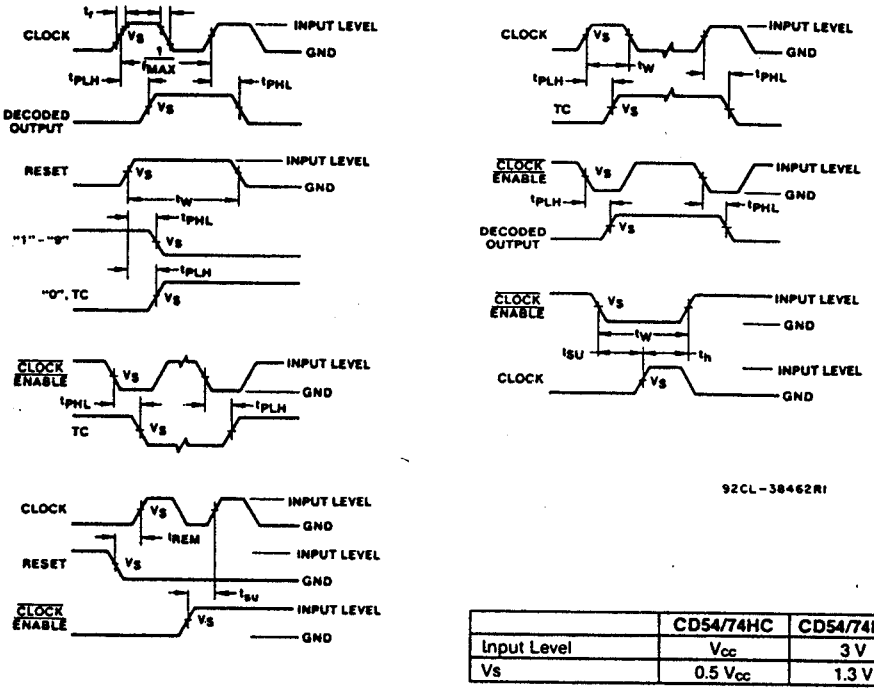
*Unless otherwise specified, all voltages are referenced to Ground.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	C_L (pF)	Typical Values		UNITS
			HC	HCT	
Propagation Delay CP to Out	t_{PLH} t_{PHL}	15	19	19	ns
CP to TC	t_{PLH} t_{PHL}	15	19	19	ns
$\overline{CE}$ to Out	t_{PLH} t_{PHL}	15	21	21	ns
$\overline{CE}$ to TC	t_{PLH} t_{PHL}	15	21	21	ns
MR to Out	t_{PLH} t_{PHL}	15	19	19	ns
MR to TC	t_{PLH} t_{PHL}	15	19	19	ns
Max. CP Frequency	f_{MAX}	15	60	50	MHz
Power Dissipation Capacitance*	C_{PD}	—	39	39	pF

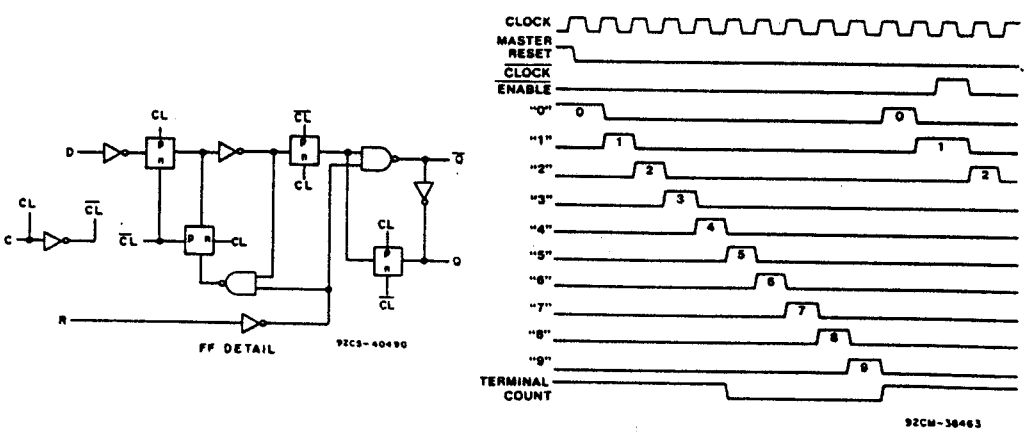
*C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o$ where f_i = input frequency.
f_o = output frequency.
C_L = output load capacitance.
V_{CC} = supply voltage.

CD54/74HC4017
CD54/74HCT4017



	CD54/74HC	CD54/74HCT
Input Level	V_{CC}	3 V
Vs	0.5 V_{CC}	1.3 V

Transition times and propagation delay times.



Timing diagram for the CD54/74HC/HCT4017

National Semiconductor

Industrial Blocks

LM555/LM555C Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

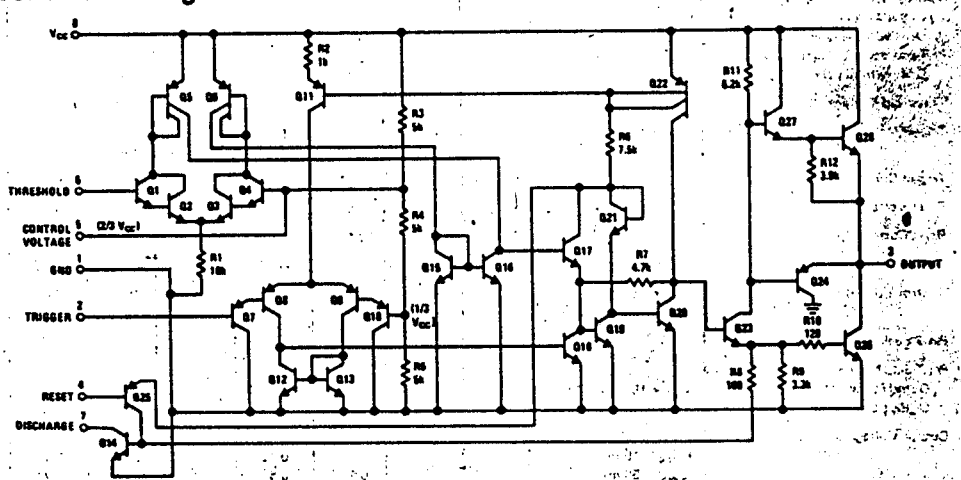
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

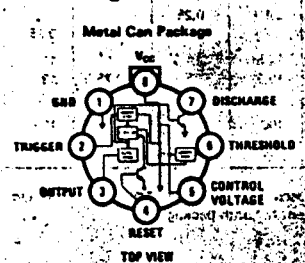
Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

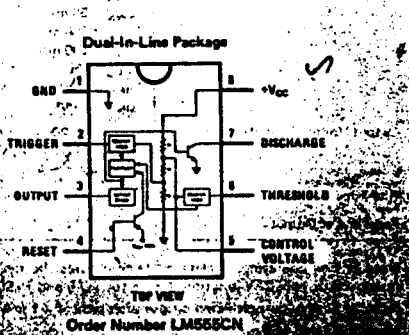
Schematic Diagram



Connection Diagrams



Order Number LM555H, LM555CH



Order Number LM555CN
See NS Package N08B

Order Number LM555J or LM555CJ
See NS Package J08A

Absolute Maximum Ratings

Supply Voltage	+18V
Power Dissipation (Note 1)	600 mW
Operating Temperature Ranges	
LM555C	0°C to +70°C
LM555	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LM555			LM555C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	6		3	6	mA
	V_{CC} = 15V, R_L = ∞ (Low State) (Note 2)		10	12		10	15	mA
Timing Error, Monostable								
Initial Accuracy			0.5			1		%
Drift with Temperature	R_A, R_B = 1k to 100 k, C = 0.1μF, (Note 3)		30			50		ppm/°C
Accuracy over Temperature			1.5			1.5		%
Drift with Supply			0.05			0.1		%/V
Timing Error, Astable								
Initial Accuracy			1.5			2.25		%
Drift with Temperature			90			150		ppm/°C
Accuracy over Temperature			2.5			3.0		%
Drift with Supply			0.15			0.30		%/V
Threshold Voltage			0.667			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2		5		V
	V_{CC} = 5V	1.45	1.67	1.9		1.67		V
Trigger Current			0.01	0.5		0.5	0.9	μA
Reset Voltage		0.4	0.5	1	0.4	0.5	1	V
Reset Current			0.1	0.4		0.1	0.4	mA
Threshold Current	(Note 4)		0.1	0.25		0.1	0.25	μA
Control Voltage Level	V_{CC} = 15V	9.6	10	10.4	9	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Pin 7 Leakage Output High			1	100		1	100	nA
Pin 7 Sat (Note 5)								
Output Low	V_{CC} = 15V, I_7 = 15 mA		150			180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5 mA		70	100		80	200	mV
Output Voltage Drop (Low)	V_{CC} = 15V							
	I_{SINK} = 10 mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50 mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100 mA		2	2.2		2	2.5	V
	I_{SINK} = 200 mA		2.5			2.5		V
	V_{CC} = 5V							
	I_{SINK} = 8 mA		0.1	0.25				V
	I_{SINK} = 5 mA					0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200 mA, V_{CC} = 15V		12.5			12.5		V
	I_{SOURCE} = 100 mA, V_{CC} = 15V	13	13.3		12.75	13.3		V
	V_{CC} = 5V	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns

Note 1: For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of +45°C/W junction to case for TO-5 and +150°C/W junction to ambient for both packages.

Note 2: Supply current when output high typically 1 mA less at V_{CC} = 5V.

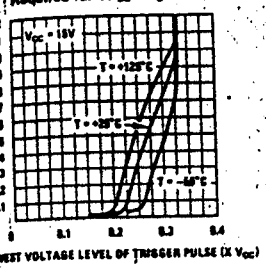
Note 3: Tested at V_{CC} = 5V and V_{CC} = 15V.

Note 4: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20 MΩ.

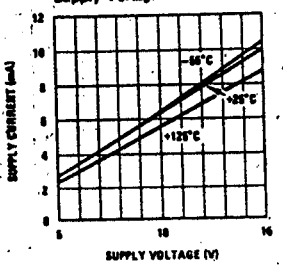
Note 5: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Typical Performance Characteristics

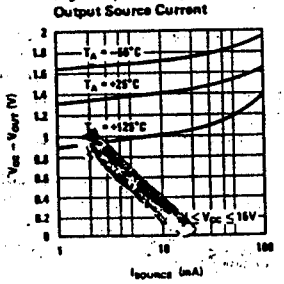
Minimum Pulse Width Required for Triggering



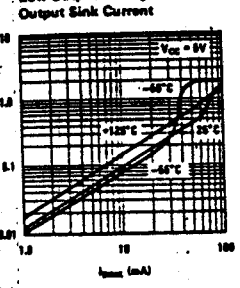
Supply Current vs Supply Voltage



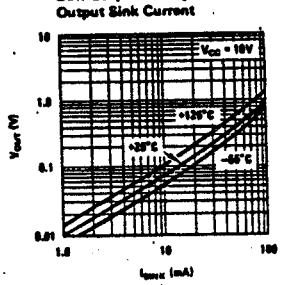
High Output Voltage vs Output Source Current



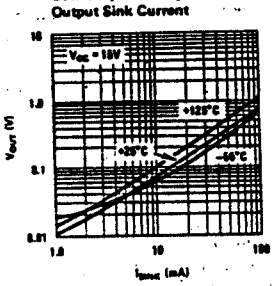
Low Output Voltage vs Output Sink Current



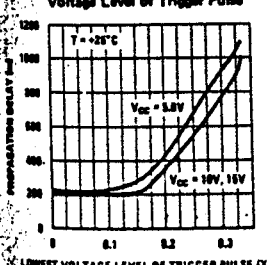
Low Output Voltage vs Output Sink Current



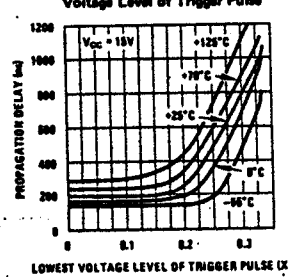
Low Output Voltage vs Output Sink Current



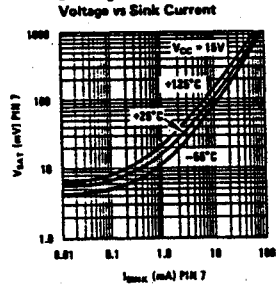
Output Propagation Delay vs Voltage Level of Trigger Pulse



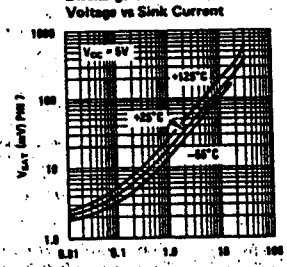
Output Propagation Delay vs Voltage Level of Trigger Pulse



Discharge Transistor (Pin 7) Voltage vs Sink Current



Discharge Transistor (Pin 7) Voltage vs Sink Current



or, R_A, in the monostable circu
ant current source, a linear ramp

Applications Information

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (*Figure 1*). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

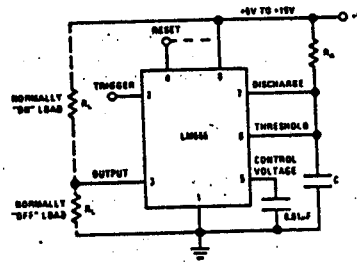


FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of $t = 1.1\ R_A C$, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.

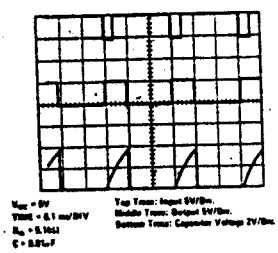


FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

NOTE: For operation as an astable, the trigger should be driven ce of +45°C/W junction timing cycle.

Supply current when output h

AS in 3: Tested at V_{CC} = 5V and V_{CC}

Note 4: This will determine the maximum in *Figure 4* (pins 2

Note 5: No protection against excessive self and free run as a

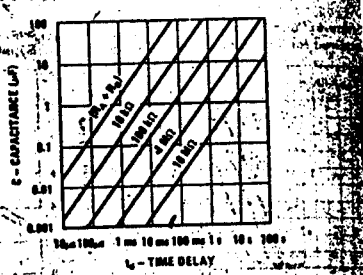


FIGURE 3. Time Delay

multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

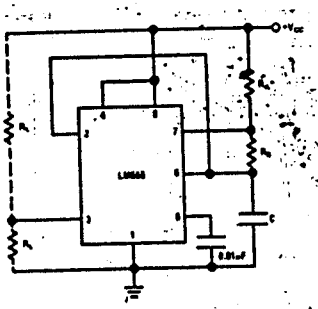


FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 5 shows the waveforms generated in this mode of operation.

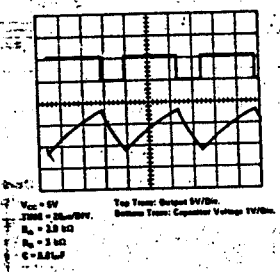


FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$$

National Semiconductor

LM567/LM567C Tone Decoder

General Description

The LM567 and LM567C are general purpose tone decoders designed to provide a saturated transistor switch to ground when an input signal is present within the passband. The circuit consists of an I and Q detector driven by a voltage controlled oscillator which determines the center frequency of the decoder. External components are used to independently set center frequency, bandwidth and output delay.

Features

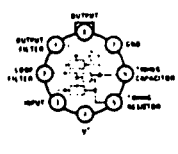
- 20 to 1 frequency range with an external resistor
- Logic compatible output with 100 mA current sinking capability
- Bandwidth adjustable from 0 to 14%
- High rejection of out of band signals and noise
- Immunity to false signals
- Highly stable center frequency
- Center frequency adjustable from 0.01 Hz to 500 kHz

Applications

- Touch tone decoding
- Precision oscillator
- Frequency monitoring and control
- Wide band FSK demodulation
- Ultrasonic controls
- Carrier current remote controls
- Communications paging decoders

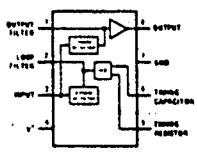
Schematic and Connection Diagrams

Metal Can Package

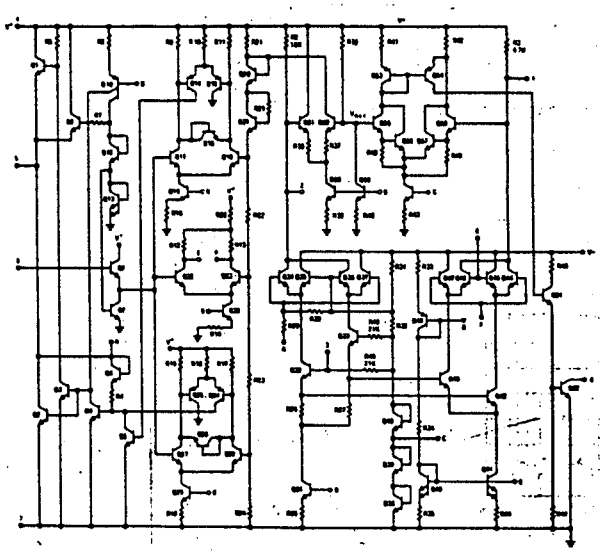


Order Number LM567H or LM567CH
See NS Package H08C

Dual-In-Line Package



Order Number LM567CN
See NS Package N08B



Absolute Maximum Ratings

Supply Voltage Pin	10V
Power Dissipation (Note 1)	300 mW
V_8	15V
V_3	−10V
V_3	V_8 + 0.5V
Storage Temperature Range	−65°C to +150°C

Electrical Characteristics (AC Test Circuit, T_A = 25°C, V_C = 5V)

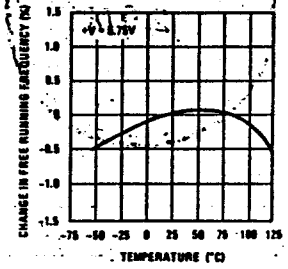
PARAMETERS	CONDITIONS	LM567			LM567C/LM567CN			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Power Supply Voltage Range		4.75	5.0	9.0	4.75	5.0	9.0	V
Power Supply Current	R_L = 20k							
Quiescent			6	8		7	10	mA
Power Supply Current	R_L = 20k							
Activated			11	13		12	15	mA
Input Resistance		18	20	22	15	20	25	kΩ
Smallest Detectable Input Voltage	I_L = 100 mA, $f_i = f_o$		20	25		20	25	mVrms
Largest No Output Input Voltage	I_C = 100 mA, $f_i = f_o$	10	15		10	15		mVrms
Largest Simultaneous Outband Signal to Inband Signal Ratio			6			6		dB
Minimum Input Signal to Wideband Noise Ratio	B_n = 140 kHz		−6			−6		dB
Largest Detection Bandwidth		12	14	16	10	14	18	% of f_o
Largest Detection Bandwidth Skew			1	2		2	3	% of f_o
Largest Detection Bandwidth Variation with Temperature			±0.1	0.25		±0.1	0.5	%/°C
Largest Detection Bandwidth Variation with Supply Voltage	4.75V – 6.75V		±1	±2		±1	±5	%V
Highest Center Frequency		100	500		100	500		kHz
Center Frequency Stability	$0 < T_A < 70$		35 ± 60			35 ± 60		ppm/°C
	$-55 < T_A < +125$		35 ± 140			35 ± 140		ppm/°C
Center Frequency Shift with Supply Voltage	4.75V – 6.75V		0.5	1.0		0.4	2.0	%/V
Fastest ON-OFF Cycling Rate			$f_o/20$			$f_o/20$		
Output Leakage Current	V_8 = 15V		0.01	25		0.01	25	μA
Output Saturation Voltage	e_i = 25 mV, I_8 = 30 mA		0.2	0.4		0.2	0.4	V
	e_i = 25 mV, I_8 = 100 mA		0.6	1.0		0.6	1.0	V
Output Fall Time			30			30		ns
Output Rise Time			150			150		ns

Note 1: The maximum junction temperature of the LM567 is 150°C, while that of the LM567C and LM567CN is For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resist 150°C/W, junction to ambient or 45°C/W, junction to case. For the DIP the device must be derated based on a resistance of 187°C/W, junction to ambient.

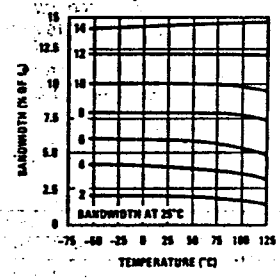
mA
Ω
24 mA

Typical Performance Characteristics

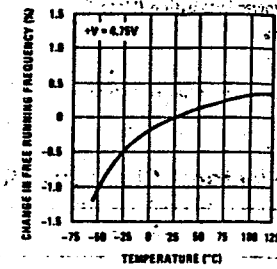
Typical Frequency Drift with Temperature (Mean and S.D.)



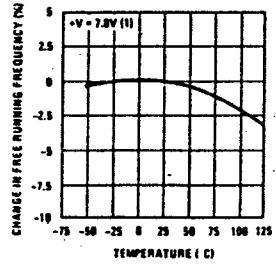
Typical Bandwidth Variation with Temperature



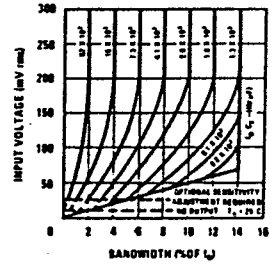
Typical Frequency Drift with (Mean and S.D.) Temperature



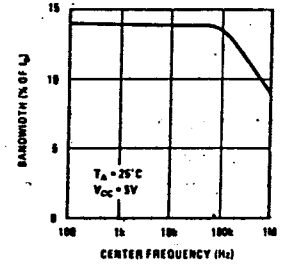
Typical Frequency Drift with Temperature (Mean and S.D.)



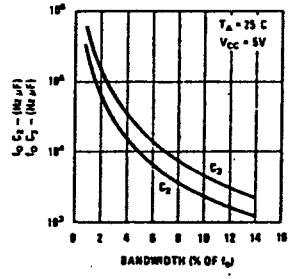
Bandwidth vs Input Signal Amplitude



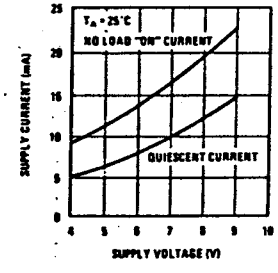
Largest Detection Bandwidth



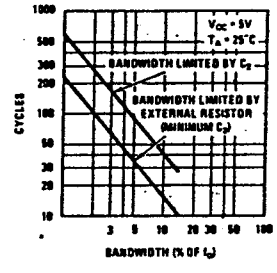
Detection Bandwidth as a Function of C_2 and C_3



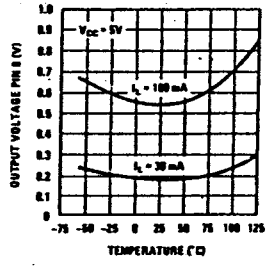
Typical Supply Current vs Supply Voltage



Greatest Number of Cycles Before Output



Typical Output Voltage vs Temperature



Typ Type Type Tipo	Hersteller Manufacturers Fabricants Costruttori	M/Pol. M/Pol. M/Pol. M/Pol.	Bild Fig. Fig. Fig.	Kurzbeschreibung Short description Description succ. Descrizione somm.	Vergleichstypen (Bild) Comparison types (fig.) Types d'eqivalence (fig.) Tipi correspondenti (fig.)	Anmerkungen Notes Notes Note
BC 527 (-6...-25)	FCH	Si-PNP	21e	NF-Tr/E, 60V, 1A, 0,625W	BC 534 (21e), BC 488 (21e) BC 638 (21)	kompl.: BC 537
BC 528 (-6...-25)	FCH	Si-PNP	21e	NF-Tr/E, 80V, 1A, 0,625W	BC 534 (21e), BC 490 (21e) BC 640 (21)	kompl.: BC 538
BC 529	FCH	Si-PNP	21e	Uni, 50V, 0,2A, 0,625W >100MHz, B=60-300	BC 557 (21e)	
BC 530	FCH	Si-PNP	21e	Vid, 130V, 0,1A, 0,625W >50MHz, B=40-180	BF 398 (21e), 2N3930-31 (4e) BF 423 (21)	kompl.: BC 532
BC 531	FCH	Si-PNP	21e	Vid, 160V, 0,1A, 0,625W >50MHz, B=60-240	BF 398 (21e), 2N3930-31 (4e) BF 423 (21)	kompl.: BC 533
BC 532	FCH	Si-NPN	21e	Vid, 160V, 0,1A, 0,625W >50MHz, B=60-250	BF 297 (21e), 2N5550 (21e) BF 422 (21)	kompl.: BC 530
BC 533	FCH	Si-NPN	21e	Vid, 180V, 0,1A, 0,625W >50MHz, B=40-250	BF 298 (21e), 2N5551 (21e) BF 422 (21)	kompl.: BC 531
BC 534	FCH	Si-PNP	21e	NF-Tr/E, 80V, 0,5A, 0,625W	BC 490 (21e), BC 528 (21e) BC 640 (21)	kompl.: BC 535
BC 535	FCH	Si-NPN	21e	NF-Tr/E, 80V, 0,5A, 0,625W	BC 489 (21e), BC 538 (21e) BC 639 (21)	kompl.: BC 534
BC 537 (-6...-25)	FCH	Si-NPN	21e	NF-Tr/E, 60V, 1A, 0,625W	BC 535 (21e), BC 487 (21e) BC 637 (21)	kompl.: BC 527
BC 538 (-6...-25)	FCH	Si-NPN	21e	NF-Tr/E, 80V, 1A, 0,625W	BC 535 (21e), BC 489 (21e) BC 639 (21)	kompl.: BC 528
BC 546 (VI,A,B)	AEG, ITT, MUL, PHI, SIE, VAL	Si-NPN	21e	Uni, 80V, 0,2A, 0,5W 300MHz, B=75-500	BC 174 (21e), BC 190 (4e), BC 447 (21e)	kompl.: BC 556
BC 547 (VI,A,B,C)	AEG, ITT, MUL, PHI, SIE, VAC	Si-NPN	21e	Uni, 50V, 0,2A, 0,5W 300MHz, B=75-900	BC 107 (4e), BC 171 (21e), BC 182 (21e), BC 207 (4), BC 237 (21e), BC 382 (21e), BC 582 (21e)	kompl.: BC 557
BC 548 (VI,A,B,C)	AEG, ITT, MUL, PHI, SIE, VAL	Si-NPN	21e	Uni, 30V, 0,2A, 0,5W 300MHz, B=75-900	BC 108 (4e), BC 172 (21e), BC 183 (21e), BC 208 (4), BC 238 (21e), BC 383 (21e), BC 583 (21e)	kompl.: BC 558
BC 549 (B,C)	AEG, ITT, MUL, PHI, SIE, VAL	Si-NPN	21e	Uni-rs, 30V, 0,2A, 0,5W 300MHz, B=240-900	BC 109 (4e), BC 173 (21e), BC 184 (21e), BC 209 (4), BC 239 (21e), BC 384 (21e), BC 584 (21e)	kompl.: BC 559
BC 550 (B,C)	AEG, ITT, MUL, PHI, SIE, VAL	Si-NPN	21e	Uni-rs, 50V, 0,2A, 0,5W 300MHz, B=240-900	BC 184 (21e), BC 384 (21e), BC 414 (21e)	kompl.: BC 560
BC 556 (VI,A,B)	AEG, ITT, MUL, PHI, SIE, VAL	Si-PNP	21e	Uni, 80V, 0,2A, 0,5W 150MHz, B=75-500	BC 256 (21e), BC 266 (4e), BC 448 (21e)	kompl.: BC 546
BC 557 (VI,A,B)	AEG, ITT, MUL, PHI, SIE, VAL	Si-PNP	21e	Uni, 50V, 0,2A, 0,5W 150MHz, B=75-500	BC 177 (4e), BC 204 (4), BC 212 (21e), BC 251 (21e), BC 307 (21e), BC 512 (21e)	kompl.: BC 547
BC 558 (VI,A,B,C)	AEG, ITT, MUL, PHI, SIE, VAL	Si-PNP	21e	Uni, 30V, 0,2A, 0,5W 150MHz, B=75-900	BC 178 (4e), BC 205 (4), BC 213 (21e), BC 252 (21e), BC 308 (21e), BC 513 (21e)	kompl.: BC 548

TYPES SN5400, SN54H00, SN54L00, SN54LS00, SN54S00, SN7400, SN74H00, SN74LS00, SN74S00
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

REVISED DECEMBER 1983

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

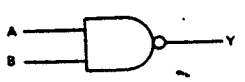
These devices contain four independent 2-input NAND gates.

The SN5400, SN54H00, SN54L00, and SN54LS00, and SN54S00 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7400, SN74H00, SN74LS00, and SN74S00 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

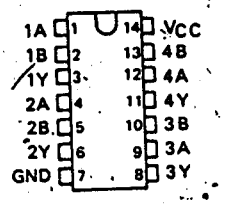
logic diagram (each gate)



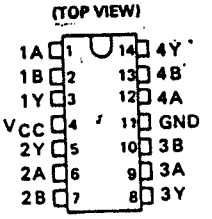
positive logic

$$Y = \overline{A \cdot B} \text{ or } Y = \overline{A} + \overline{B}$$

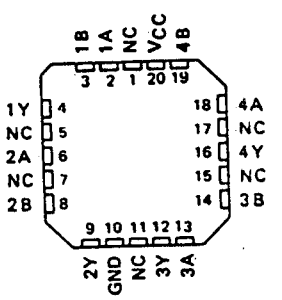
SN5400, SN54H00, SN54L00 . . . J PACKAGE
SN54LS00, SN54S00 . . . J OR W PACKAGE
SN7400, SN74H00 . . . J OR N PACKAGE
SN74LS00, SN74S00 . . . D, J OR N PACKAGE
(TOP VIEW)



SN5400, SN54H00 . . . W PACKAGE
(TOP VIEW)



SN54LS00, SN54S00 . . . FK PACKAGE
SN74LS00, SN74S00 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

recommended operating conditions

	SN5400			SN7400			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			−0.4			−0.4	mA
I_{OL} Low-level output current			16			16	mA
T_A Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5400			SN7400			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −0.4 mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}§	V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CCH}	V_{CC} = MAX, V_I = 0 V		4	8		4	8	mA
I_{CCL}	V_{CC} = MAX, V_I = 4.5 V		12	22		12	22	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

... :ching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 400 Ω, C_L = 15 pF		11	22	ns
t_{PHL}					7	15	ns

'E 2: See General Information Section for load circuits and voltage waveforms.

ES

t_{PHL}	A or B	Y	R_L = 280 Ω,	C_L = 25 pF	6.2 10 ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.