MICROCONTROLLER BASED INTERFACE UNIT WITH SOFTWARE SECURITY

PROJECT REPORT

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1999 -2000

Department of Electronics & Communication Engineering

Kumaraguru College of Technology

Coimbatore - 641 006

CERTIFICATE

Kumaraguru College of Technology

Coimbatore – 641 006

Department of Electronics and Communication Engineering

Certificate

This is to certify that this project entitled

MICROCONTROLLER BASED INTERFACE UNIT WITH SOFTWARE SECURITY

Has been submitted by

Mr/Ms...

In partial fulfillment of the requirements for the award of Degree of Bachelor of Engineering in the Electronics and Communication Engineering Branch of the Bharathiar University, Coimbatore - 641 046 during the academic year 1999-2000.

.... (Guide)

.... (Head of Department)

Certified that the Candidate was Examined by us in the Project Work.

Viva - Voce Examination held on ....

University Register Number ....

.... (Internal Examiner)

.... (External Examiner)

DEDICATED
TO OUR
BELOVED PARENTS

ACKNOWLEDGEMENT

ACKNOWLEDGEMENT

We profusely thank **Prof. M. Ramasamy, M.E., MIEEE (USA) MIE., MISTE C.Eng (I) MBMESI.,** Professor and Head of the department of Electronics and Communication Engineering for his invaluable advise and gentle reminders, that really motivated us through many a tough encounter, only to help us reach our goal.

We are highly indebted and grateful to our guide **Ms. R. Latha, B.E., MISTE.,** lecturer department of Electronics and Communication Engineering for her constant support and guidance offered to us during the course of this project work.

We express our sincere and profound sense of gratitude to our principal **Dr. K. K. Padmanabhan, B.Sc (Engg)., M. Tech., Ph.D.,** and the management for the facilities provided in the college to accomplish this project.

Though words are not enough, it is all that we have got, to express our deepest gratitude to **Mr. V. Hariharakrishnan,** Senior Engineer (R&D), our guide at Premier Polytronics Limited, Coimbatore, for being

SYNOPSIS

SYNOPSIS

"COMMUNICATION HAS VIRTUALLY SHRUNK THE WORLD". To emphasize this thought, a project of designing and developing an interface unit between a personal computer and machines had been undertaken. This interface unit is a new product being developed by Premier Polytronics Ltd., Coimbatore.

The interface unit allows the controlling PC to access the data station connected to each machine, in which the various parameters of the machine are being collected. These parameters can be used for effective monitoring of machines and also for improving the overall performance.

This unit also provides security to the software being distributed along with the hardware. This security is facilitated by programming the microcontroller with a code. Each interface unit is associated with a software, both having a common code.

The salient features that differentiate this from the conventional interface units are the distance of access and the number of machines being interfaced. This unit can be used to interface a wide range of machines by suitably designing the data station.

a beacon to us from the conceptualization to the realization of the project. We also thank him and all the other staff of the company for readily providing us with all the facilities, patiently answering all our queries and helping us to carry out this project meticulously within the stipulated time.

We would be failing in our duty if we don't express our indebtedness to all our teachers in the department of Electronics and Communication Engineering for their suggestions and constant encouragement. We would also like to thank the non – teaching and our friends for their timely help, big and small alike, that culminated as good, in the end.

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INTRODUCTION

1.INTRODUCTION

Computerization is the buzzword that is being pronounced in the world today. Almost all the institutions have come to a state that without computerization they would be left behind. Computers cannot be directly connected to machines, they have to be interfaced through some specifically designed units. Here comes the necessity of interfacing unit to do the above job.

1.1 AIM OF OUR PROJECT:

This project deals with the design and construction of an interfacing unit that is used to connect spinning machines in textile industry to PC's that monitor the various parameters of the machine. In general it can also be used to interface other machines with suitable changes in design. This unit also provides security to the software used to control the machines. With this interface unit a maximum of 256 machines can be interfaced over a distance of about two kilometers.

1.2 PROJECT OVERVIEW:

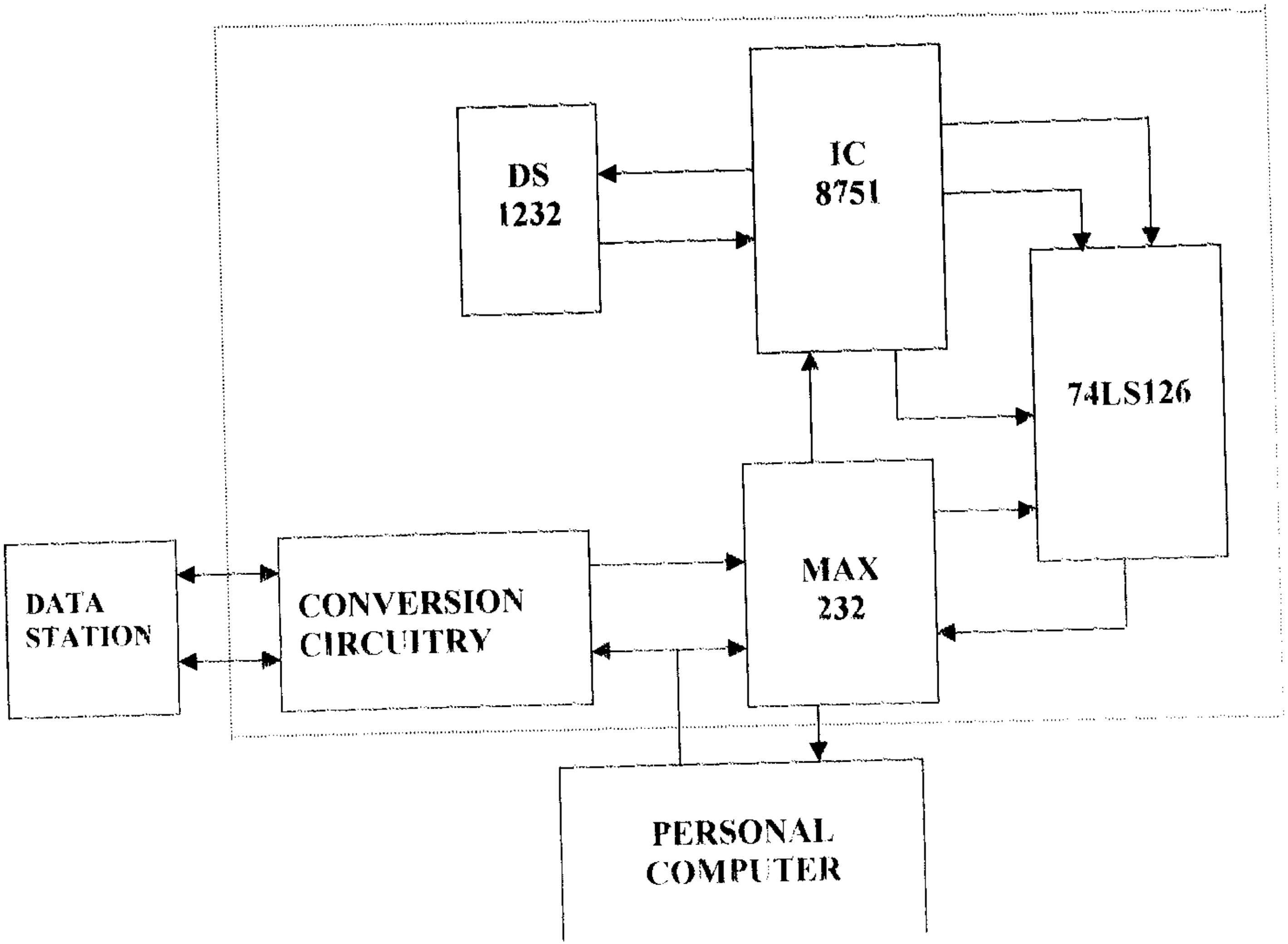
In our project, we have used IC 87C51 microcontroller which forms the heart of this interface unit. The microcontroller is programmed with a code, enabling us to provide software security. The design consists of transmission and reception part circuits.

The information from the PC is sent to the data station through the transmission circuit. The PC is also linked to the microcontroller through MAX 232 IC which converts the input RS232 signal into corresponding TTL signal at its output. This connection is used for the transmission of the code incorporated in the software to reach the microcontroller for comparison.

The reception part is used for the data transfer from a particular data station to the PC. The data from the data station is passed onto a comparator, whose output is a RS232 signal. This signal is converted into a TTL signal and is fed to the gate of 74LS126.

The code sent from the PC is compared with the one that is set in the microcontroller. If found okay, the gate in 74LS126 is enabled. This allows the PC to access the data station. On the other hand if the code is not satisfied, the gate is disabled and the PC is not allowed to access the data station.

INTERNAL BLOCK DIAGRAM :



The microcontroller 87C51 is programmed using assembler ASM51 software. The transmission and reception of data, enabling and disabling of gates is indicated to the user by corresponding LED illumination. Thus our purpose of interfacing and providing software security is achieved.

IC 87C51

2. IC 87C51

CHMOS SINGLE CHIP 8-BIT MICROCONTROLLER:

2.1 FEATURES:

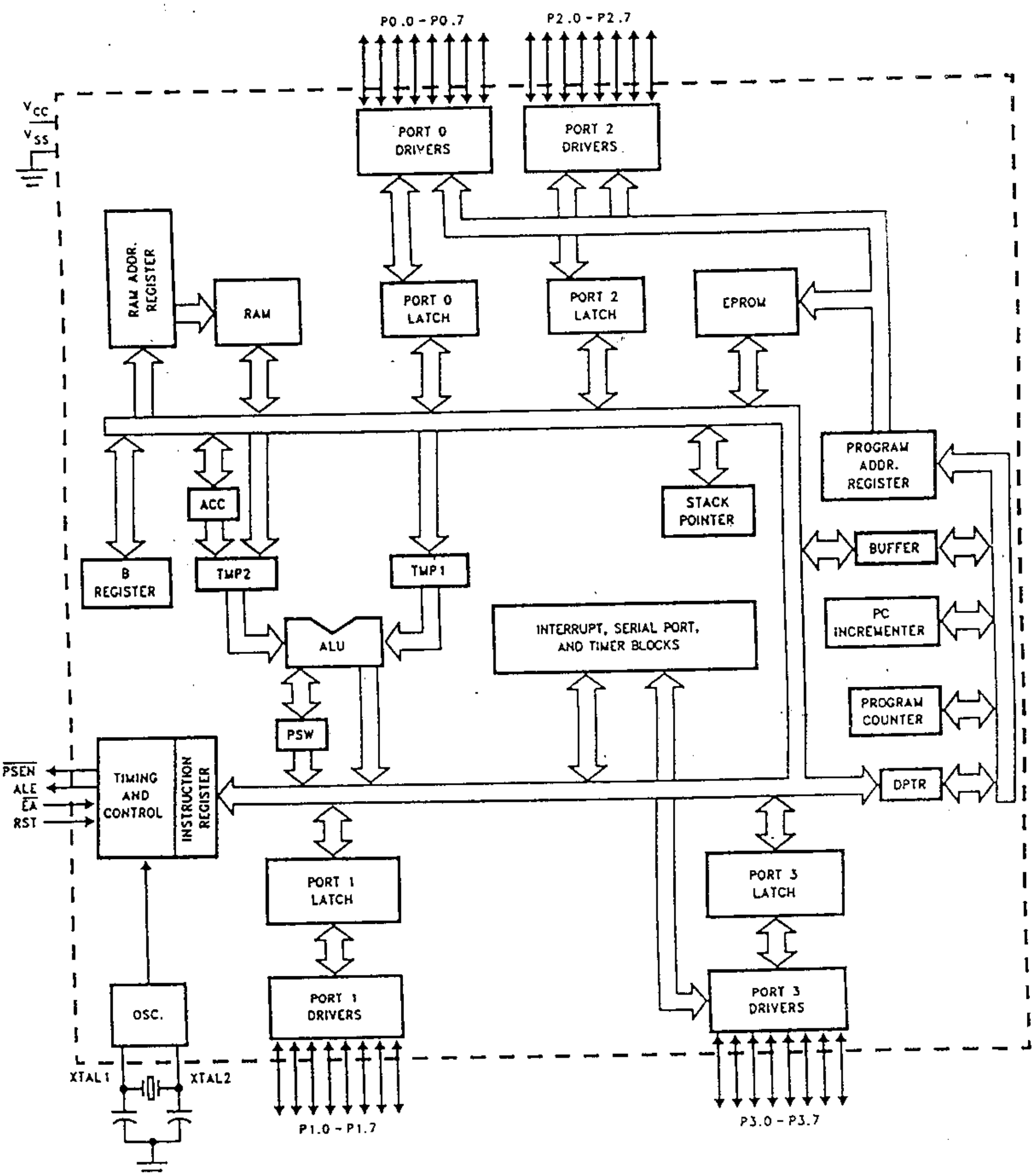
- High performance CHMOS EPROM.
- 24 MHz operation.
- Boolean processor.
- 128-byte data RAM.
- 32 programmable input output lines.
- Two 16 – bit timer/counter.
- Upwardly compatible with existing 8048 software.
- Five interrupt sources.
- Direct byte and Bit addressability.
- Four register banks.
- Programmable serial port.
- Binary or decimal arithmetic.
- TTL and CMOS compatible logic levels.
- 64 K external program memory source.
- Power control modes
    - Idle
    - Power Down

2.2 ARCHITECTURE:

The 87C51 combines a central processing unit, two kinds of memory (Data RAM and Program ROM or EPROM), input/output ports, and the mode, status and the data registers and random logic needed for a variety of peripheral functions. These elements communicate through an 8 – bit data bus, which runs through out the chip. This bus is buffered to the outside world through an I/O port when memory or I/O expansion is desired.

The primary elements of the central processing unit are 8 – bit arithmetic/logic unit with associated registers A, B, PSW and SP, and the 16 – bit Program counter and the Data pointer registers. An important and unique feature of this architecture is that the ALU can also manipulate one – bit as well as 8 – bit data types. Individual bits may be set, cleared, or complemented, moved, tested, and used in logic computations. The accumulator can be the source and the destinations for the logical operations and a number of special data movement instructions including table look - ups and external RAM expansions.

ARCHITECTURE:



A special 8 – bit register (B) serves in the execution of the multiply and the divide instructions. This register is used in conjunction with the accumulator as the second input operand and to return 8 – bits of the result. The stack pointer (SP) is an 8 – bit pointer register, which indicates the address of the last byte pushed onto the stack. The stack pointer is automatically incremented or decremented on all push or pop instructions and all subroutine calls and returns.

The 87C51 have 32 I/O pins configured as four 8 – bit parallel ports (P0, P1, P2 and P3). All 4 ports are bi-directional and each consists of a latch, an output driver and an input buffer. The output drivers of ports 0 and 2 and the input buffers of port 0 are used in accesses to external memory. Port 0 outputs the low byte of the external memory address, time multiplexed with the byte being written or read. Port 2 outputs the high byte of the external memory address when the address is 16 – bits wide. All the port 3 pins are multi functional.

TIMERS/COUNTERS:

The 87C51 have two 16 – bit timer/counter registers: Timer 0 and Timer 1. Both can be configured to operate either as timers or event counters. In the timer function, the register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency. In the counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. The timer/counter function is selected using the mode register TMOD and controlled with the register TCON.

MEMORY ORGANIZATION:

All 80C51 devices have separate address space for program and data memory. The logical separation of program and data memory allows the data memory to be accessed by 8 – bit addresses, which can be quickly stored and manipulated by 8 – bit CPU. A 16 – bit data memory address can also be generated through the DPTR register.

PROGRAM MEMORY:

Program memory (ROM, EPROM) can only be read, not written to. There can be up to 64K bytes of program memory. In the 80C51, the lowest 4K bytes of program are on chip. In ROM less versions, all program memory is external. The read strobe for external program memory is the $\overline{PSEN}$ (Program Store Enable).

DATA MEMORY:

Data memory (RAM) occupies a separate address space form program memory up to 64K bytes of external RAM can be addressed in the external data memory space. The CPU generates read and write signals, $\overline{RD}$ and $\overline{WR}$ as needed during external data memory accesses.

SERIAL PORT INTERFACE:

The serial port is full duplex , meaning it transmit and receive simultaneously. It is also receive – buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the register. The serial port receive and transmit registers are both accessed at a special function register SBUF. Writing to SBUF loads the transmit register and reading SBUF accesses a physically separate received register.

The serial port can operate in 4 modes, which are controlled by the register SCON. The serial port modes are as follows:

Mode 0:

Serial data enters and exits through RXD. TXD outputs the shift clock. 8 – bits are transmitted/received (LSB first). The baud rate is fixed at 1/12th the oscillator frequency.

Mode 1:

Ten bits are transmitted or received: a start bit (0), 8 data bits (LSB first) and a stop bit (1). On receive, the stop bit goes into RB8 in special function register SCON. The baud rate is variable.

Mode 2:

11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9th data bit and a stop bit (1). On transmit, the 9th data bit (TB8 in SCON) can be assigned a value of 0 or 1. On receive, the 9th data bit goes into RB8 in SCON, while the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 the oscillator frequency.

Mode 3:

11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9th data bit and a stop bit (1). The baud rate in mode 3 is variable.

2.3 PIN DESCRIPTION:

Vcc: Supply voltage during normal, idle and power down operations.

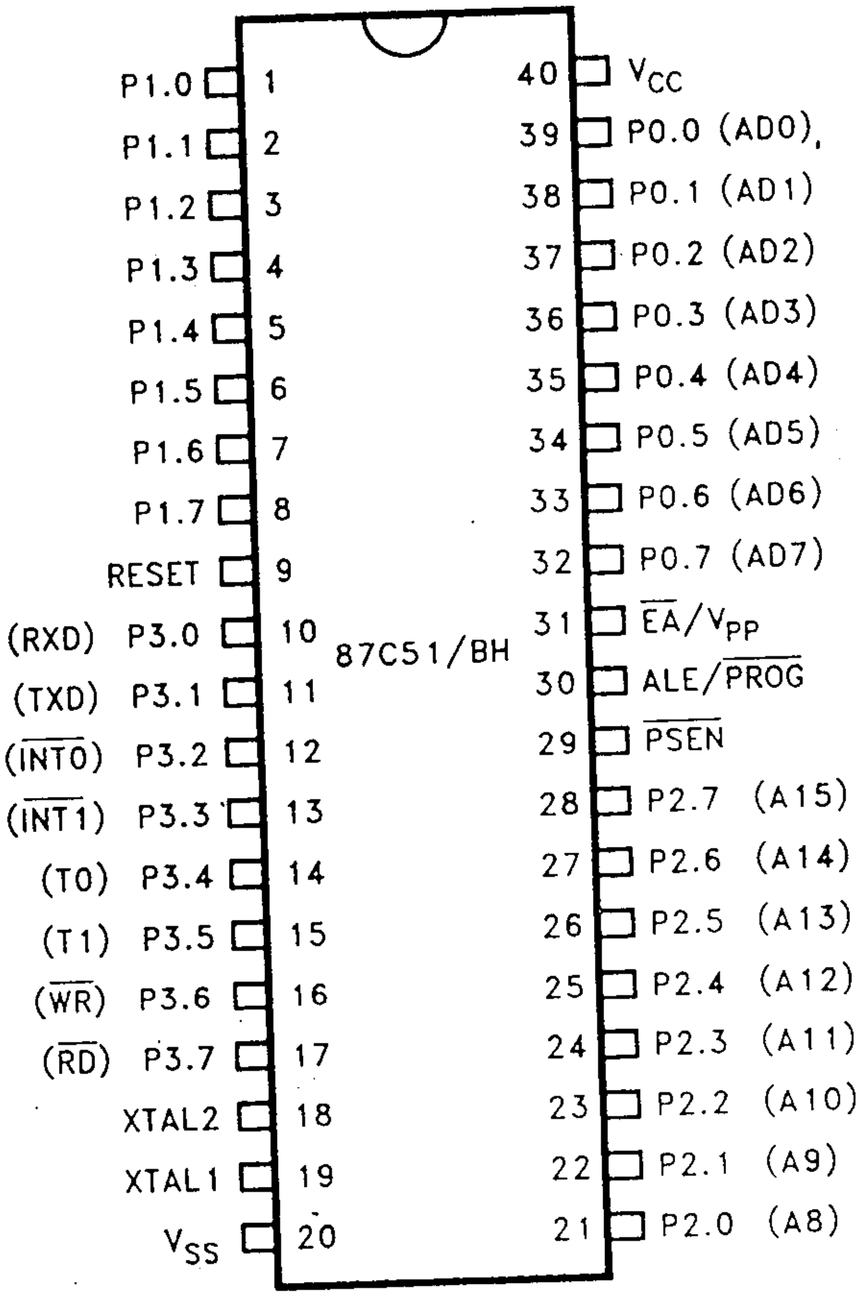
Vss: Circuit ground.

Port 0: Port 0 is an 8 – bit open drain bi-directional input output port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float and in that state can be used as high impedance inputs.

Port 1: Port 1 is a 8 – bit bi-directional input output port with internal pull ups. The port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pull ups and in that state can be used as inputs. As inputs, port 1 pins that are extremely pulled low will source current (I_{IL}, on the data sheet) because of the internal pull ups.

Port 2: Port 2 is a 8 – bit bi-directional input output port with internal pull ups. Port 2 pins have 1's have written to them are pulled high by the internal pull ups and in that state can be used as inputs. As inputs, port 2 pins that are pulled low will source current (I_{IL}, on the data sheet) because of the internal pull ups.

PIN DIAGRAM:


87C51/BH
P1.0 1
P1.1 2
P1.2 3
P1.3 4
P1.4 5
P1.5 6
P1.6 7
P1.7 8
RESET 9
(RXD) P3.0 10
(TXD) P3.1 11
($\overline{INT0}$) P3.2 12
($\overline{INT1}$) P3.3 13
(T0) P3.4 14
(T1) P3.5 15
($\overline{WR}$) P3.6 16
($\overline{RD}$) P3.7 17
XTAL2 18
XTAL1 19
V_{SS} 20
40 V_{CC}
39 P0.0 (AD0)
38 P0.1 (AD1)
37 P0.2 (AD2)
36 P0.3 (AD3)
35 P0.4 (AD4)
34 P0.5 (AD5)
33 P0.6 (AD6)
32 P0.7 (AD7)
31 $\overline{EA}/V_{PP}$
30 ALE/$\overline{PROG}$
29 $\overline{PSEN}$
28 P2.7 (A15)
27 P2.6 (A14)
26 P2.5 (A13)
25 P2.4 (A12)
24 P2.3 (A11)
23 P2.2 (A10)
22 P2.1 (A9)
21 P2.0 (A8)

Port 3: Port 3 is a 8 – bit bi-directional input output port with internal pull ups. The port 3 output buffer can drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pull ups and in that state can be used as inputs. As inputs, port 3 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pull ups.

Port 3 also serves the function of various special features of the MCS – 51 family as listed below:

PIN	NAME	ALTERNATE FUNCTION
P 3.0	RXD	Serial input line
P 3.1	TXD	Serial output line
P 3.2	$\overline{INT0}$	External interrupt 0
P 3.3	$\overline{INT1}$	External interrupt 1
P 3.4	T0	Timer 0 external input
P 3.5	T1	Timer 1 external input
P 3.6	$\overline{WR}$	External data memory write strobe
P 3.7	$\overline{RD}$	External data memory read strobe

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a minimum V_{IH1} voltage is applied whether the oscillator is running or not. An internal pull down resistor permits a power – on – reset with only a capacitor connected to Vcc.

ALE/$\overline{\textbf{PROG}}$: Address latch enable output signal for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{\text{PROG}}$) during EPROM programming for the 87C51.

$\overline{\textbf{PSEN}}$: Program store enable is the read strobe to external program memory. When the 87C51 is executing from the internal program memory, $\overline{\text{PSEN}}$ is inactive (high). When the device is executing code from external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory.

$\overline{\textbf{EA}}$/Vpp: External access enable. $\overline{\text{EA}}$ must be strapped to Vss in order to enable the 87C51 to fetch code from the external program memory locations starting at 0000H upto FFFFH. $\overline{\text{EA}}$ must be strapped to Vcc for internal program execution. This pins also receives the programming supply voltage (Vpp) during EPROM programming.

XTAL 1: Input to the inverting oscillator amplifier.

XTAL 2: Output from the inverting oscillator amplifier.

2.4 INTERRUPT STRUCTURE:

The 87C51 have 5 interrupt sources : 2 external interrupts, 2 timer interrupts and the serial port interrupt. Each interrupt source can be individually enable or disabled by setting or clearing a bit in the SFR named IE(Interrupt Enable). This register also has a global disable bit, which can be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one of two priority levels by setting or clearing a bit in the SFR named IP(Interrupt Priority). A low – priority interrupt can be interrupted by a high – priority, but not by another low – priority interrupt. A high - priority can't be interrupted by any other interrupt source. If two interrupt requests of different priority levels are received simultaneously, the request of the higher priority is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

2.5 SPECIAL FUNCTION REGISTERS:

PSW: PROGRAM STATUS WORD. BIT ADDRESSABLE

CY	AC	F0	RS1	RS0	OV	-	P

CY	PSW.7	Carry flag.
AC	PSW.6	Auxiliary carry flag.
F0	PSW.5	Flag 0 available to the user for general purpose.
RS1	PSW.4	Register bank selector bit 1 (See Note).
RS0	PSW.3	Register bank selector bit 0 (See Note).
OV	PSW.2	Overflow flag.
-	PSW.1	Usable as a general-purpose flag.
P	PSW.0	Parity flag.

NOTE: The value presented by RS0 and RS1 selects corresponding register bank.

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00H-07H
0	1	1	08H-0FH
1	0	2	10H-17H
1	1	3	18H-1FH

PCON : POWER CONTROL REGISTER. NOT BIT ADDRESSABLE

SMOD	-	-	-	GF1	GFO	PD	IDL

SMOD	Double baud rate bit.
-	Not implemented.
GF1, GF0	General purpose flag bits.
PD	Power down bit.
IDL	Idle mode bit.

❖ If 1's are written to both PD and IDL, PD takes precedence.

IE: INTERRUPT ENABLE REGISTER.BIT ADDRESSABLE

EA	-	-	ES	ET1	EX1	ET0	EXO

EA	IE.7	Disable all interrupts.
-	IE.6	Not implemented.
-	IE.5	Not implemented.
ES	IE.4	Enable or disable the serial port interrupt.
ET1	IE.3	Enable or disable the Timer 1 overflow interrupt
EX1	IE.2	Enable or disable External interrupt 1.
ET0	IE.1	Enable or disable Timer 0 overflow interrupt.
EX0	IE.0	Enable or disable External interrupt 0.

IP: INTERRUPT PRIORITY REGISTER.BIT ADDRESSABLE

-	-	-	PS	PT1	PX1	PT0	PXO

-	IP.7	Not implemented .
-	IP.6	Not implemented .
-	IP.5	Not implemented .
PS	IP.4	Defines the serial port interrupt priority level.
PT1	IP.3	Defines the Timer 1 interrupt priority level.
PX1	IP.2	Defines External interrupt 1 priority level.
PT0	IP.1	Defines the Timer 0interrupt priority level.
PX0	IP.0	Defines the External interrupt 0 priority level.

PRIORITY WITHIN LEVEL:

From high to low, interrupt sources are listed below:

1. IE0
2. TF0
3. IE1
4. TF1
5. R1 or T1

TCON:TIMER/COUNTER CONTROL REGISTER.BIT ADDRESSABLE.

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

TF1	TCON.7	Timer 1 overflow flag.
TR1	TCON.6	Timer 1 run control bit.
TF0	TCON.5	Timer 0 overflow flag.
TR0	TCON.4	Timer 0 run control bit.
IE1	TCON.3	External interrupt 1 edge flag.
IT1	TCON.2	Interrupt 1 type control bit.
IE0	TCON.1	External interrupt 0 edge flag.
IT0	TCON.0	Interrupt 0 type control bit.

TMOD:TIMER/COUNTER MODE CONTROL REGISTER. NOT BIT ADDRESSABLE

GATE	$C/\overline{T}$	M1	M0	GATE	$C/\overline{T}$	M1	M0

GATE When TRx (in TCON) is set and GATE = 1, TIMER/COUNTERx will run only while INTx pin is high(hardware control). When GATE =0 , TIMER/COUNTERx will run only while TRx = 1 (software control).

TB8	SCON.3	The 9^{th} bit that will be transmitted in modes 2 and 3.Set/Cleared by software.
RB8	SCON.2	In modes 2 and 3, is the 9^{th} data bit that was received. In mode 1, if SM2 = 0. RB8 is the stop bit that was received.
T1	SCON.1	Transmit interrupt flag.
R1	SCON.0	Received interrupt flag.

NOTE : MODE SELECTION

SM0	SM1	MODE	DESCRIPTION	BAUD RATE
0	0	0	Shift Register	Fosc /12
0	1	1	8 – bit UART	Variable
1	0	2	9 – bit UART	Fosc /64 or Fosc /32
1	1	3	9 – bit UART	Variable

SERIAL PORT SETUP :

MODE	SCON	SM2 VARIATION
0	10H	Single processor Environment (SM2 = 0)
1	50H	
2	90H	
3	D0H	
0	NA	Multi Processor Environment (SM2 = 1)
1	70H	
2	B0H	
3	F0H	

2.6 POWER CONTROL MODES OF OPERATION:

IDLE MODE:

In idle mode, the CPU puts itself to sleep while all the on – chip peripherals remain active. The mode is invoked by software. The content of the on – chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset. To eliminate the possibility of an unexpected write to a port pin when idle is terminated by reset, the instruction following the one that invokes the idle should not be one that writes to a port pin or to external memory.

POWER DOWN MODE:

To save even more power, a power mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked power down is the last instruction executed. The on – chip RAM and the special function registers retain their values until the power down mode is transmitted.

On the 87C51, a hardware reset or an external interrupt can cause an exit from power down. Reset redefines all the SFR's but does not change the on – chip RAM. An external interrupt allows both the SFR's and on – chip RAM to retain their values.

To properly terminate power down, the reset or external interrupt should not be executed before Vcc is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

The status of the external pins during idle and power down operations are as listed below:

MODE	PROGRAM MEMORY	ALE	$\overline{PSEN}$	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power down	External	0	0	Float	Data	Data	Data

ONCE MODE:

The ONCE (on – circuit emulation) mode facilitates 87C51 without the 87C51 having to be removed from the circuit. The ONCE mode is invoked by:

- Pull ALE low while the device is in reset and $\overline{\text{PSEN}}$ is high.
- Hold ALE low as RST is deactivated.

While the device is in ONCE mode, the port 0 pins float and the other port pins and ALE and $\overline{\text{PSEN}}$ are weakly pulled high. The oscillator circuit remains active. While the 87C51is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

ADDRESSING MODES:

DIRECT ADDRESSING:

In direct addressing the operand is specified by an 8 – bit address field in the instruction. Only internal data RAM and SFR's can be directly addressed.

INDIRECT ADDRESSING:

In indirect addressing the instruction specifies a register, which contains the address of the operand. Both internal and external RAM can be indirectly addressed. The address register for 8 – bit addresses can be

R0 and R1 of the selected bank, or the stack pointer. The address register for 16 – bit addresses can only be the 16 – bit "data pointer" register, DPTR.

REGISTER ADDRESSING:

The register banks, containing registers R0 through R7, can be accessed by certain instructions which carry a 3 – bit register specification within the op code of the instruction. When the instruction is executed, one of the 8 registers in the selected bank is accessed.

IMMEDIATE ADDRESSING:

When a source operand is a constant rather than a variable then the constant can be incorporated into the instruction. The value used is fixed at the time of ROM manufacture or EPROM programming and cannot be altered during program execution.

2.7 PROGRAMMING THE 87C51:

The set up for programming the microcontroller is as shown in the Figure below. Note that the part is running with a 4 – 6 MHz oscillator. The clock must be running because the device is executing internal address and program data transfers during the programming.

To program the 87C51, the address of the EPROM location to be programmed is applied to ports 1 and 2 as shown in the Figure. The code byte to be programmed into this location is applied to port 0. RST, $\overline{\text{PSEN}}$, and the pins of the ports 2 and 3 specified in the table. The ALE/$\overline{\text{PROG}}$ is then pulsed low 25 times to program the addressed locations.

ENCRYPTION TABLE.

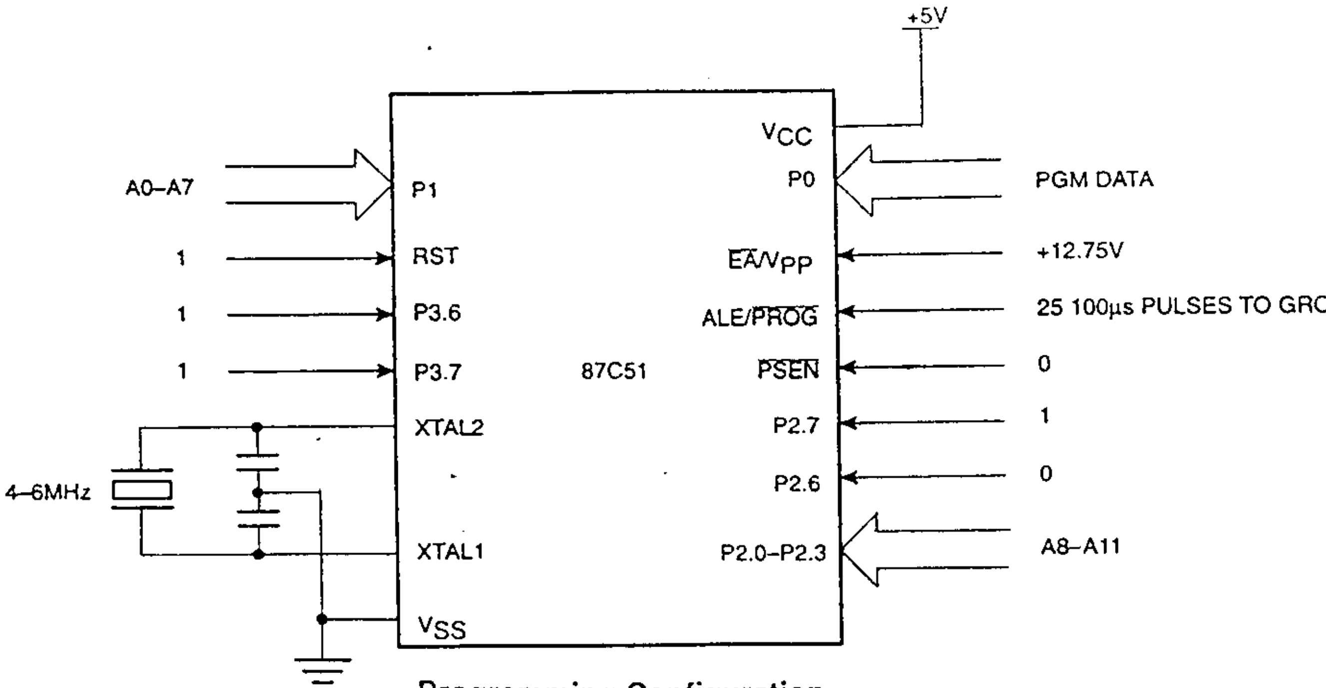
The encryption table is a feature of 87C51, and its derivatives that protects the code from being easily read by anyone other than the programmer. The encryption table is 16 to 64 bytes of code, depending on the microcontroller, that are exclusive NORed with the program code data as it is read out. The first byte is XNORed with the first location read, the second with the second read etc.. through the 16th byte read. The

17th byte is XNORed with the first byte of the encryption table, the 18th with the second etc.. and on in 16 byte groups.

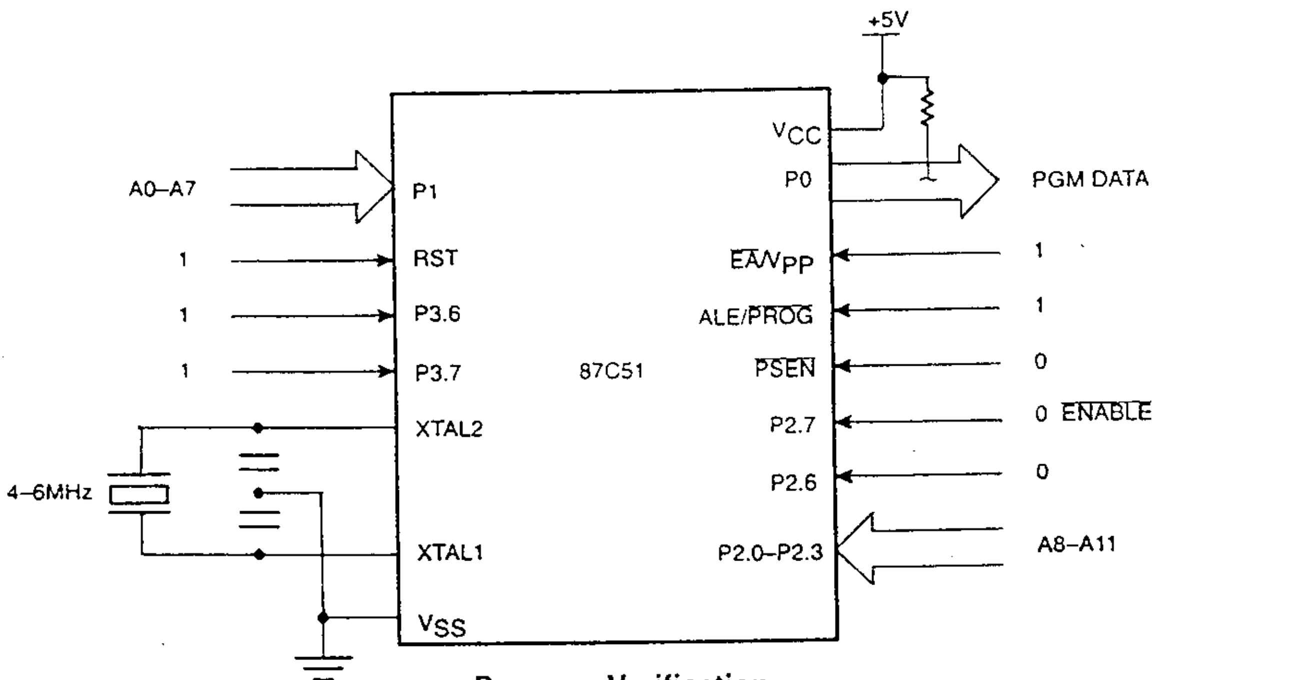
After the encryption table has been programmed, the user has to know its contents in order to correctly decode the program code data. The encryption table itself cannot be read out. The encryption table is programmed in the same manner as the program memory, but using the "Pgm Encryption Table" levels specified in the table below. After the encryption table is programmed, verification cycles will produce only encrypted information.

SECURITY BIT

There are two security bits on the 87C51 that, when set, prevent the program data memory from being read out or programmed further. To program the security bits, repeat the programming sequence using the "Pgm Security Bit" levels specified in given table. After the security bit is programmed, further programming of the code memory or the encryption table is disabled. The other security bit can of course still be programmed. With only security bit one programmed, the memory can still be read out for program verification. After the second security bit is programmed, it is no longer possible to read out (verify) the program memory.



Programming Configuration



Program Verification

PROGRAM VERIFICATION

If security bit 2 has not been programmed the on chip program memory can be read out for program verification. To verify the contents of the program memory, the address of the location to be read is applied to the ports 1 and 2 as shown in the figure below. The other pins are held at the "Verify Code Data" levels indicated in the above table. The contents of the addressed locations will appear on the port 0. For this operation external pull ups are required on port 0 as shown in the figure below. Note that if the encryption table has been programmed the data presented at port 0 will be the exclusive NOR of the program byte with a byte from the encryption table.

SIGNATURE BYTES

The 87C51 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an IC87C51. The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to logic low.

ERASURE CHARACTERISTICS:

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to this light sources over an extended time (about one week in sunlight, or three years in room level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultra violet light (at 2537 Angstroms) to an integrated dose of at least $15W\text{-}Sec/Cm^2$. Exposing the EPROM to an ultra violent lamp of 12000 Micro W/Cm^2 rating for 30 Minutes, at a distance of about 1 inch should be sufficient. Erasure leaves the array in an all 1's state.

DS 1232

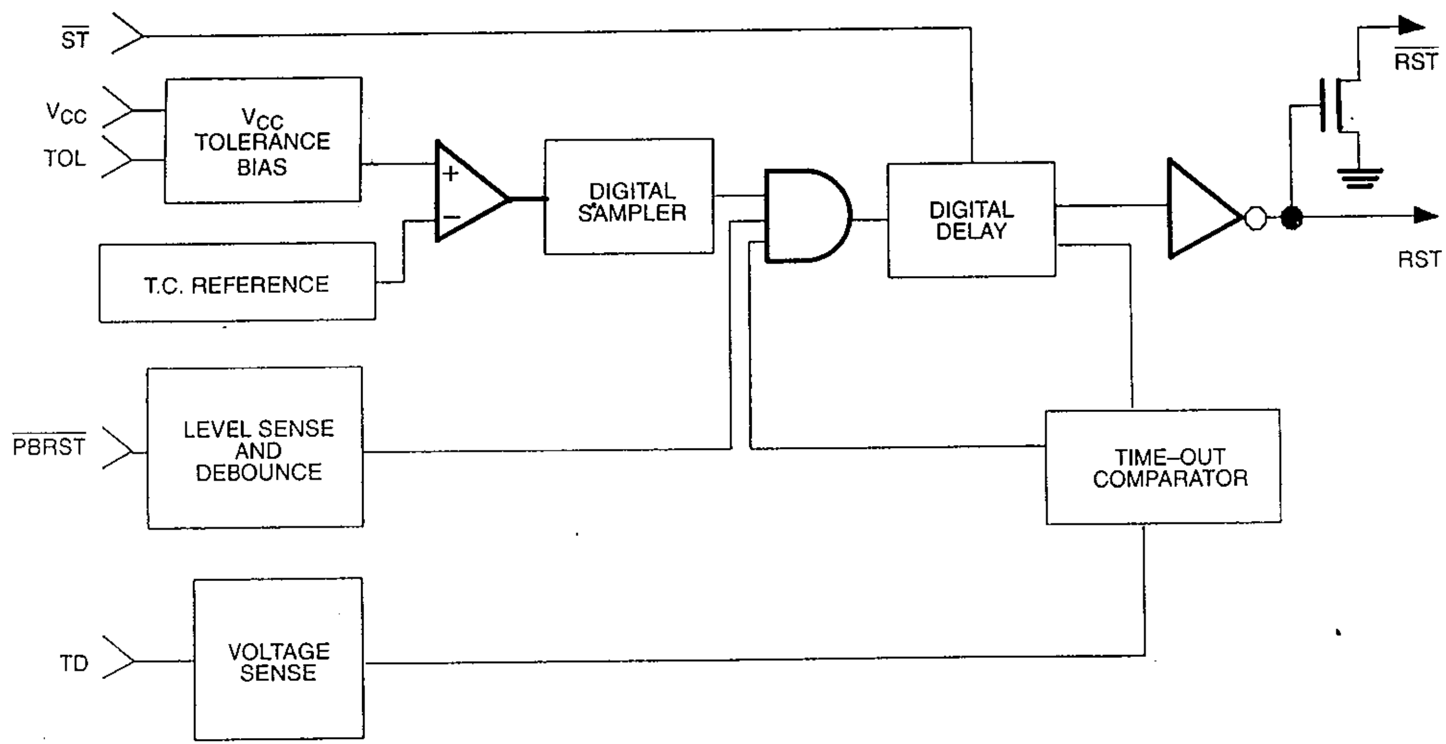
3. DS – 1232

MICRO MONITOR CHIP

3.1 GENERAL DESCRIPTION:

The DS – 1232 chip monitors three vital conditions for the microprocessor: power supply, software execution and external override. First a precision temperature compensated reference and comparator circuit monitors the status of Vcc. When an out of tolerance condition occurs, an internal power fail signal is generated which forces reset to the active state. When Vcc returns to an intolerance condition, the reset signals are kept in the active state for a minimum of 250 milliseconds to allow the power supply and the processor to stabilize. The second function of the DS – 1232 is push button reset control. The DS – 1232 debounces the push button input and guarantees an active reset pulse width of 250 millisecond minimum. The third function is a watch dog timer. The DS – 1232 has an internal timer that forces the reset signal to the active state if the strobe input is not driven low prior to time out. The watch timer function can be set to operate on time settings of 150 milliseconds, 600 milliseconds and 1.2 seconds.

BLOCK DIAGRAM Figure 1



3.2 FEATURES:

- ❖ Halts and restarts an out of control microprocessor.
- ❖ Holds microprocessor incheck during power transients.
- ❖ Automatically restarts microprocessor after power failure.
- ❖ Monitors push button for external override.
- ❖ Accurate 5% or 10% microprocessor power supply monitoring.

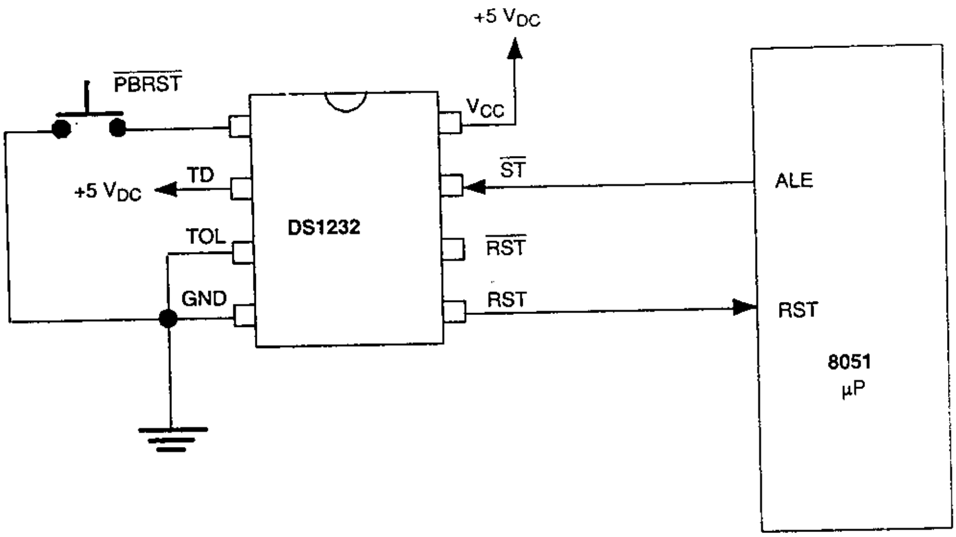
3.3 POWER MONITORING – OPERATION:

The DS – 1232 detects out – of – tolerance power supply conditions and warns a processor – based system of impending power failure. When Vcc falls below a preset level as defined by T_{OL} (Pin 3), the Vcc comparator outputs the signals RST (Pin 5) and $\overline{RST}$ signals become active as Vcc falls below 4.75 Volts. When T_{OL} is connected to Vcc, the $\overline{RST}$ and RST signals become active a s Vcc falls below 4.5 Volts. The RST and $\overline{RST}$ are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid Vcc. On power – up, RST and $\overline{RST}$ are kept active for a minimum of 250 milliseconds to allow the power supply and processor to stabilize.

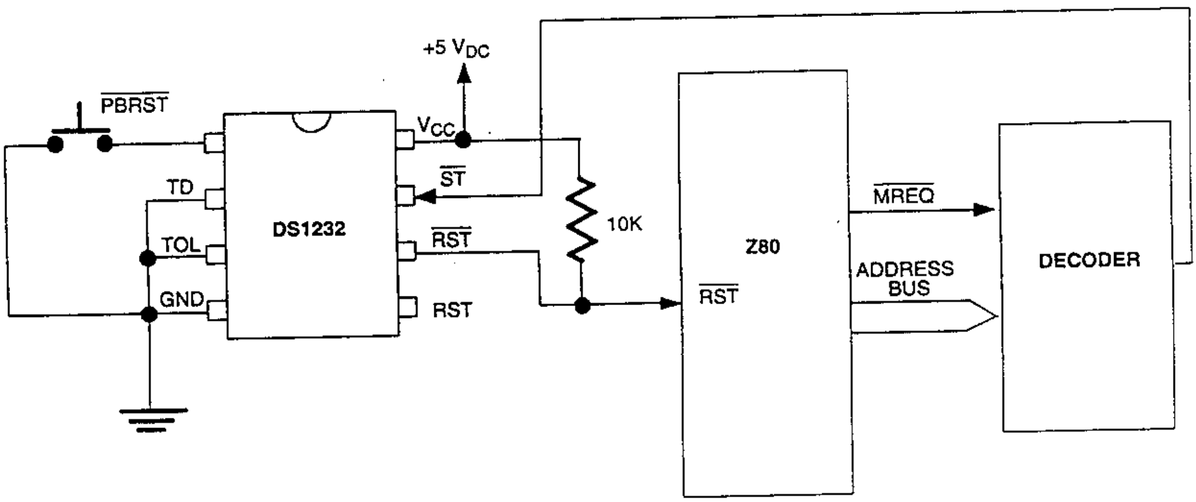
3.4 PUSH BUTTON RESET – OPERATION:

The DS – 1232 provides an input pin for direct connection for a push button (Fig 2.). The push button reset input requires a active low

PUSHBUTTON RESET Figure 2



WATCHDOG TIMER Figure 3



MAX 232

4. MAX 232

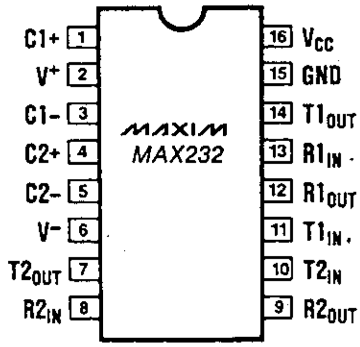
RS 232 DRIVERS/RECEIVERS

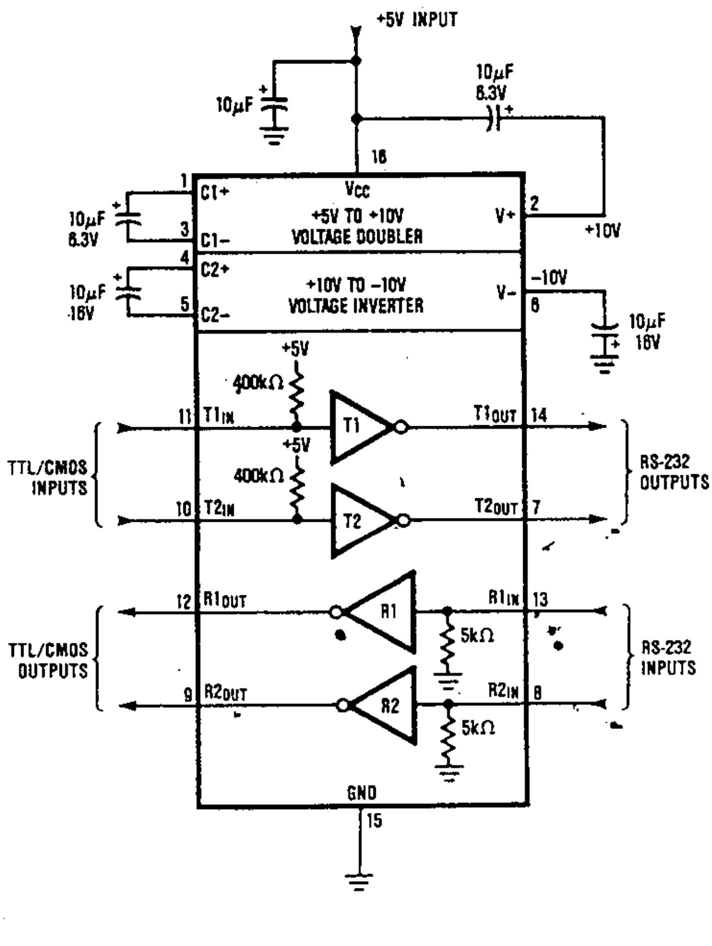
4.1 GENERAL DESCRIPTION:

MAX 232 belongs to the MAXIM family in which the line drivers/receivers are intended for all RS 232 and V.28/V.24 communications interface and in particular for those applications where +/-12 Volts is not available. Since nearly all RS 232 applications need both line drivers and receivers, the family includes both receivers and drivers in one package. Both the receivers and the line drivers (transmitters) meet all EIA RS 232 and CCIT V.28 specifications. The MAX 232 consists of three sections – the transmitters, the receivers and the charge pump DC – DC voltage converters.

4.2 FEATURES:

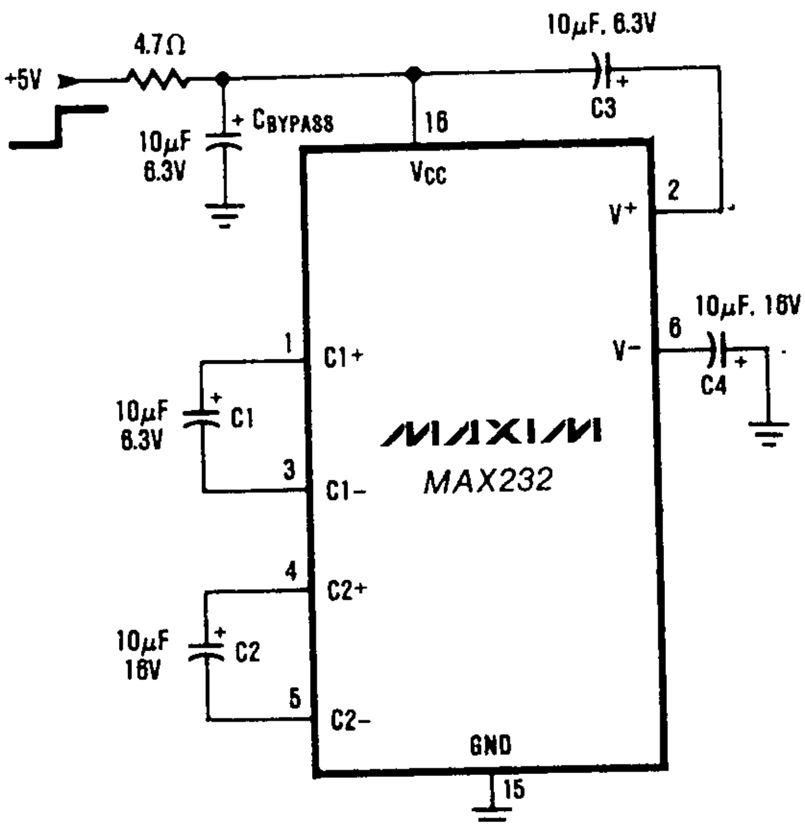
- ❖ Operates from single 5 volts supply.
- ❖ Meets all RS – 232C and V.28 specifications.
- ❖ Multiple drivers and receivers.
- ❖ On board DC – DC converter.
- ❖ +/- 9 volts output swing with 5 volts supply.
- ❖ Low power shut down - <1micro amps (typ).
- ❖ Three state TTL/CMOS receiver outputs.
- ❖ +/- 30 volts receiver input levels.


C1+
V+
C1-
C2+
C2-
V-
T2OUT
R2IN
MAXIM
MAX232
VCC
GND
T1OUT
R1IN
R1OUT
T1IN
T2IN
R2OUT


+5V INPUT
10μF
10μF
6.3V
16
VCC
C1+
C1-
+5V TO +10V
VOLTAGE DOUBLER
V+
+10V
10μF
6.3V
C2+
C2-
+10V TO -10V
VOLTAGE INVERTER
V-
-10V
10μF
16V
10μF
16V
+5V
400kΩ
T1IN
T1
T1OUT
+5V
400kΩ
T2IN
T2
T2OUT
TTL/CMOS
INPUTS
RS-232
OUTPUTS
R1OUT
R1
R1IN
5kΩ
R2OUT
R2
R2IN
5kΩ
TTL/CMOS
OUTPUTS
RS-232
INPUTS
GND
15

4.3 DUAL CHARGE PUMP VOLTAGE CONVERTER:

The RS 232 drivers/receivers have on - board charge pump voltage converters which convert the +/- 5 volts input power to the +/- 10 volts needed to generate the RS 232 output levels. This + 5 volts to +/- 10 volts conversion is performed by two charge pump voltage converters. The first uses capacitor C1 to double the + 5 volts to + 10 volts, storing the + 10 volts on the V^+ output filter capacitor, C3. The second charge pump voltage converter uses capacitor C2 to invert the + 10 volts to – 10 volts, storing the – 10 volts on the V^- output filter capacitor, C4. A small amount of power may be drawn from the + 10 volts (V^+) and – 10 volts (V^-) outputs to power external circuitry.



4.4 DRIVER (TRANSMITTER) SECTION:

The transmitters or the line drivers are inverting level translators which convert the CMOS/TTL input levels to RS 232 or V.28 voltage levels. With + 5 volts Vcc , the typical output voltage swing is +/- 9 volts when loaded with a nominal 5kilo ohms input resistance of an RS 232 receiver. The output swing is guaranteed to meet the RS 232/V.28 specification of +/- 5 volts minimum output swing under the worst case conditions of all transmitters during the 3 kilo ohms minimum allowable load impedance Vcc = 4.5 volts and maximum operating ambient temperature. The open circuit output voltage swing in the transmitter is set to be from (V^+ - 0.6 volts) to V^-.

The input thresholds are both CMOS/TTL compatible, with a logic threshold of about 25% of Vcc. The inputs of unused driver section can be left unconnected, an internal 400 kilo ohms input pull up resistor to Vcc will pull the inputs high, forcing the unused transmitter outputs low. The input pull up resistors source about 12 micro amps and the driver inputs should be driven high or open circuited to minimize power supply current in the slow down mode.

When in the low power shut down mode , the driver outputs are turned off and their leakage current is less than 1micro amps with driver output pulled to ground. The driver output leakage remains less than 1 micro amps even if the transmitter output is back driven between 0 Volts and (Vcc + 6 volts). Below – 0.5 volts the transmitter is diode clamped to ground with 1 kilo ohm series impedance. The transmitter is also zener clamped to approximately Vcc + 6 volts, with a series impedance of 1 kilo ohms. As required by RS 232 and V.28 the slew rate is limited to less than 30Volts /micro seconds. This limits the maximum usable baud rate to 19200 bauds.

4.5 RECEIVER SECTION:

All but the MAX 230 and MAX 234 contain RS 232/V.28 receivers. These receivers convert the +5 volts to +15 volts RS 232 signals to 5 volts TTL/CMOS outputs. Since the RS 232C/ V.28 specifications define a voltage level greater than +3volts as a zero, the receiver are inverting. These receivers are able to respond to both RS 232/V.28 levels and TTL level inputs. The receivers are protected against input over voltage upto + 30 volts.

The lower threshold has a guaranteed value of 0.8 volts. This value is important in the sense that the receiver will have a logic one output if the receiver is not being driven. This is because the equipment containing the line driver is turned off or disconnected if the connecting cable has a open circuit or short circuit. In the other words the receiver implements type one interpretation of fault conditions. While or even a –3volts receiver threshold would not give proper indication on the control lines such a s DTR and DSR. The receiver on the other hand have a full 0.8V noise margin for detecting the power down or the cable connected states.

The receiver have a hysteresis of approximately of 0.5 Volts with a minimum guaranteed hysteresis 200 milli volts. This aids is obtaining clean output transitions even with slow rise and fall line input signals with moderate amount of noise and ringing, The propagation delays of the receivers are 350 nano seconds for negative going input signals and 650 nano seconds for positive going input signals.

LM 339

SFH 600

HARDWARE

7. HARDWARE

7.1 HARDWARE DESCRIPTION:

The operation of line driver circuit during the transmission and reception of the data is elaborated below:

Once the power is switched ON, active HIGH signal is available at P1.0 of 87C51 which enables the gate A of 74LS126 and gate B is disabled because of active LOW signal at P1.1. The enabling and disabling of the gates are indicated by the status of LED 5 and LED 6. A trigger pulse is available at P1.2 if the microcontroller is functioning properly. In case the microcontroller is not functioning properly, a RESET output signal from the DS1232 resets the microcontroller.

When data is sent from the PC, it enters the circuit through two paths. One path is to the microcontroller through the MAX232 IC and the other is to the transmitting section of the circuit. The data from the PC is in the from RS232C standard. Its voltage levels are -12V and +12V. The –12V and +12V in RS232C standards is equivalent to binary 1 and 0 respectively.

When the HIGH is transmitted, the following sequence of operations take place. The –12V being transmitted on reaching the base of transistor T8, makes it saturated. Due to this saturation, the same –12V is applied to the 2nd pin of SFH600-2 (IC 1). This makes the LED inside it

A −12V signal is obtained at the output of the comparator. This is fed to the pin 2 of SFH600-1, which makes the internal LED forward biased and the optically coupled transistor saturated. Thus a signal of −12V is obtained at pin 5 of the SFH 600-1 (IC 2).

MAX232 IC converts the −12V at point A into its corresponding TTL signal. This TTL signal is fed to the gate B of 74LS126. The code sent from the PC is compared with the code set in the microcontroller. If both the codes match, gate A is disabled and the gate B of 74LS126 is enabled. MAX232 IC reconverts the data back into RS232 signal. This leads to the reception of the data transmitted from the data station in the PC.

When the $\overline{\text{DATA}}$ terminal is +12V and DATA terminal is −12V, the following operations would take place. As in the above case, the potential divider network gives an output of +1.2V at pin 9 and −1.2V at pin 8 of comparator LM339. A +12V signal from the output of the comparator is applied to the 2nd pin of SFH 600-1(IC2), which makes the internal LED to become reverse biased and the transistor inside is cut off. Thus the +12V signal from the power supply is available at point A. This +12V signal is fed to the MAX 232 IC and all the other operations performed above take place and the corresponding data is received in the PC.

7.2 POWER SUPPLY CIRCUIT DESCRIPTION:

The power supply circuit is used to provide a regulated ripple free +12V, -12V and +5V supply for the entire circuit. It consists of a step down transformer, metal oxide varistor, bridge rectifier, regulating IC's and capacitor filters.

The transformer steps down the supply voltage from 230V A.C to 0V to 15V A.C supply. Next to the transformer a metal oxide varistor is connected which suppresses any transient voltage more than 40V. The output from the transformer is rectified using a bridge rectifier and is fed to the regulating IC's 7812 and 7912.

The IC's 7812 and 7912 give a regulated +12V and –12V at the respective output terminals. The +12V obtained from IC 7812 is fed to the regulating IC 7805 and a regulated +5V is obtained at its output terminal.

The capacitors are used before and after the regulating IC's in order to reduce oscillations and ripples. The diodes D5 and D6 are employed to provide a fly back path for the discharge of excess capacitance available at the output terminals of the regulating IC's.

Thus the output from the power supply circuit is a constant or regulated D.C voltages of +12V, -12V and +5V.

SOFTWARE

8. SOFTWARE

```
TMOD_VALUE   DATA 20H
PCON         EQU 87H
SCON_VALUE   DATA 50H
FLAG         EQU 30H

ORG 0H
LJMP START
ORG 03H
RETI
ORG 0BH
RETI
ORG 13H
RETI
ORG 1BH
RETI
ORG 23H
LJMP SRL

ORG 0200H
```

```
START:
        MOV SP, #60H
        MOV PSW, #0H
        SETB EA
        SETB ET1
        CLR TR1
        SETB ES
        MOV TMOD, #TMOD_VALUE
        MOV SCON, #SCON_VALUE
        SETB P1.0
        CLR P1.1
        CPL P1.2
        MOV TL1, #0F3H
        MOV TH1, #0F3H
        SETB TR1
        CPL P1.2
MAIN_PR:
        MOV A, FLAG
        CPL P1.2
        CJNE A, #55H,MAIN_PR
        CPL P1.2
```

```
        SETB P1.1
        CLR P1.0
        CPL P1.2
        MOV FLAG, #0H
        LJMP MAIN_PR
SRL:
        JB RI, XX
        CLR TI
        CPL P1.2
        RET I
XX:
        CLR RI
        PUSH ACC
        CPL P1.2
        MOV A, SBUF
        CJNE A, #'a', LOCK_IT
        MOV FLAG, #O55H
        CLR TI
        MOV SBUF, #'E'
```

```
TX1:
        JNB TI, TX1
        CLR TI
        JMP SKIP
LOCK_IT:
        MOV FLAG, #0H
SKIP:
        CPL P1.2
        SETB ES
        POP ACC
        CPL P1.2
        RETI
END
```

PCB DESIGN

9. REALISATION OF THE DESIGN:

With the completion of the circuit diagram, the process of realization of the design started with the selection of suitable software for the design of PCB. This lead to the selection of a software called "CADSTAR".

The 1st step in this is to draw the PCB schematic. This schematic obtained is checked for errors. Errors, if present, are rectified, and we proceed on to the 2nd stage, i.e., PCB design itself. The size of the board is selected and the placement of different chips in the required position is done. The final stage is "Routing". With the routing completed, the design obtained is given for fabrication.

Once the PCB is obtained, the board is checked for short circuits and track discontinuity. After this phase, the soldering procedure starts. The components that are to be soldered are checked for the proper operation and its characteristics are verified. Then the components are soldered on the board. Once soldering is over, the next step involved is that of loading the software into the EPROM. This procedure consists of erasing the previous contents of the EPROM which is done by exposing the chip to UV rays.

Once the erasure procedure is over this is then loaded into a universal programmer which loads the necessary program into the EPROM. The PCB is set into the cabinet and after connecting the necessary power supply connection and connecting the PC with this system, the cabinet is closed. Thus an explanation of hardware is given above.

CONCLUSION

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11. BIBLIOGRAPHY

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11. PHILIPS SEMICONDUCTORS
12. OPTO COUPLERS - SIEMENS

ANNEXURE

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . −40°C to +85°C
Storage Temperature .... −65°C to +150°C
Voltage on $\overline{EA}/V_{PP}$ Pin to V_{SS} .... 0V to +13.0V
Voltage on Any Other Pin to V_{SS} .. −0.5V to +6.5V
Maximum I_{OL} per I/O Pin .... 15 mA
Power Dissipation.......................... 1.5W
(Based on package heat transfer limitations, not device power consumption.)

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

OPERATING CONDITIONS

Symbol	Description	Min	Max	Unit
T_A	Ambient Temperature Under Bias Commercial Express	 0 −40	 +70 +85	 °C °C
V_{CC}	Supply Voltage	4.5	5.5	V
f_{OSC}	Oscillator Frequency 87C51/BH 87C51-1/BH-1 87C51-2/BH-2 87C51-24/BH-24	 3.5 3.5 0.5 3.5	 12 16 12 24	MHz

DC CHARACTERISTICS (Over Operating Conditions)

All parameter values apply to all devices unless otherwise indicated.

Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage Commercial Express	 −0.5 −0.5		 0.2 V_{CC} − 0.1 0.2 V_{CC} − 0.15	 V V	
V_{IL1}	Input Low Voltage $\overline{EA}$ Commercial Express	 0 −0.5		 0.2 V_{CC} − 0.3 0.2 V_{CC} − 0.35	 V V	
V_{IH}	Input High Voltage (Except XTAL1, RST) Commercial Express	 0.2 V_{CC} + 0.9 0.2 V_{CC} + 1		 V_{CC} + 0.5 V_{CC} + 0.5	 V V	
V_{IH1}	Input High Voltage (XTAL1, RST) Commercial Express	 0.7 V_{CC} 0.7 V_{CC} + 0.1		 V_{CC} + 0.5 V_{CC} + 0.5	 V V	
V_{OL}	Output Low Voltage(6) (Ports 1, 2, 3)			0.3	V	I_{OL} = 100 μA(2)
				0.45	V	I_{OL} = 1.6 mA(2)
				1.0	V	I_{OL} = 3.5 mA(2)

DC CHARACTERISTICS (Over Operating Conditions) (Continued)

Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
V_{OL1}	Output Low Voltage(6) (Port 0, ALE, $\overline{PSEN}$)			0.3	V	$I_{OL} = 200\ \mu A$(2)
				0.45	V	$I_{OL} = 3.2$ mA (2)
				1.0	V	$I_{OL} = 7.0$ mA(2)
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, $\overline{PSEN}$)	$V_{CC} - 0.3$			V	$I_{OH} = -10\ \mu A$(3)
		$V_{CC} - 0.7$			V	$I_{OH} = -30\ \mu A$(3)
		$V_{CC} - 1.5$			V	$I_{OH} = -60\ \mu A$(3)
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	$V_{CC} - 0.3$			V	$I_{OH} = -200\ \mu A$(3)
		$V_{CC} - 0.7$			V	$I_{OH} = -3.2$ mA(3)
		$V_{CC} - 1.5$			V	$I_{OH} = -7.0$ mA(3)
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3) Commercial Express			 −50 −75	 μA μA	$V_{IN} = 0.45V$
I_{LI}	Input Leakage Current (Port 0)			±10	μA	$0.45 < V_{IN} < V_{CC}$
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3) Commercial Express			 −650 −750	 μA μA	$V_{IN} = 2V$
RRST	RST Pulldown Resistor	40		225	kΩ	
C_{IO}	Pin Capacitance		10		pF	@ 1 MHz, 25°C
I_{CC}	Power Supply Current Active Mode @ 12 MHz (Figure 5) @ 16 MHz @ 24 MHz Idle Mode @ 12 MHz (Figure 5) @ 16 MHz @ 24 MHz Power Down Mode		 11.5 3.5 5	 20 26 38 7.5 9.5 13.5 50	 mA mA mA mA mA mA μA	(Note 4)

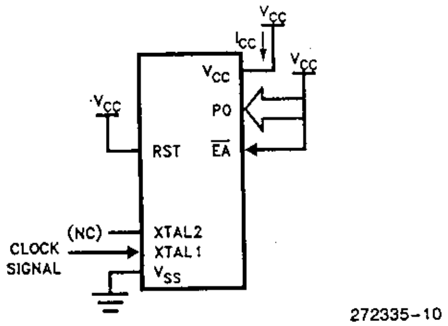


Figure 6. I_{CC} Test Condition, Active Mode. All other pins are disconnected.

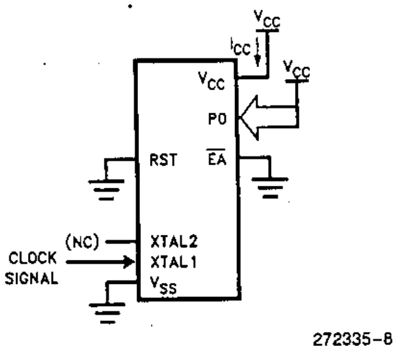


Figure 7. I_{CC} Test Condition, Idle Mode. All other pins are disconnected.

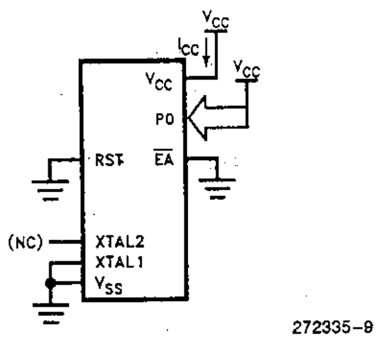


Figure 9. I_{CC} Test Condition, Power Down Mode. All other pins are disconnected. V_{CC} = 2V to 5.5V.

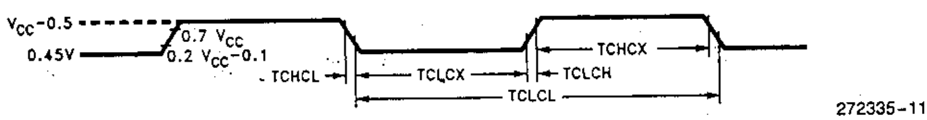


Figure 8. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes
TCLCH = TCHCL = 5 ns

NOTES:

1. "Typicals" are based on a limited number of samples taken from early manufacturing lots and are not guaranteed. The values listed are at room temp, 5V.
2. Capacitive loading on Ports 0 and 2 may cause noise pulses above 0.4V to be superimposed on the V_{OL}s of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger, or CMOS-level input logic.
3. Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{CC}$ specification when the address bits are stabilizing.
4. See Figures 6 through 8 for I_{CC} test conditions. Minimum V_{CC} for Power Down is 2V.
5. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum I_{OL} per port pin:	10 mA
Maximum I_{OL} per 8-bit port—	
Port 0:	26 mA
Ports 1, 2, and 3:	15 mA
Maximum total I_{OL} for all output pins:	71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink greater than the listed test conditions.

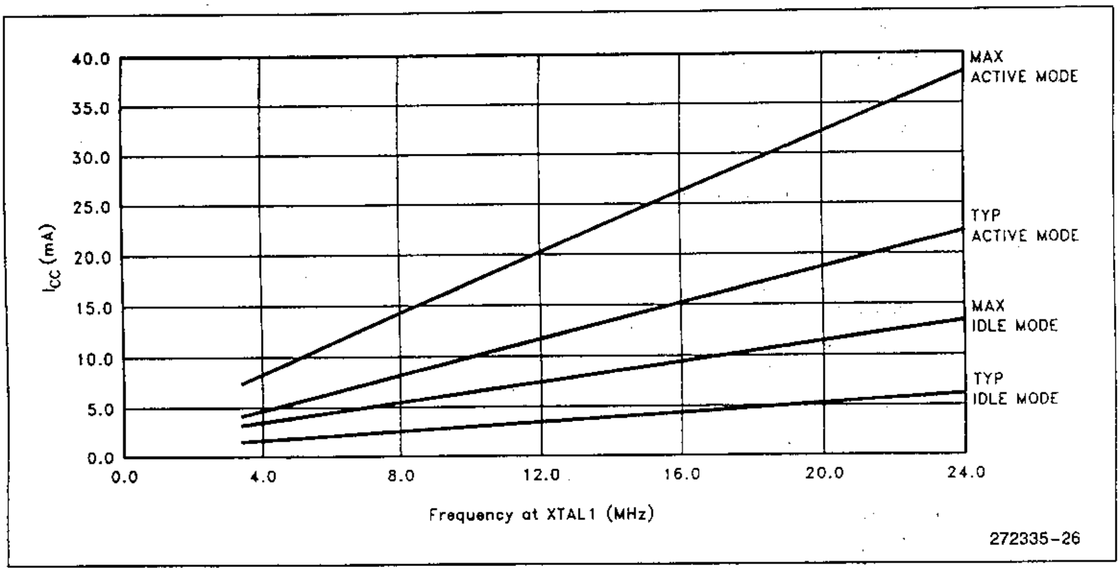


Figure 5. 87C51/BH I_{CC} vs Frequency

EXTERNAL MEMORY CHARACTERISTICS

All parameter values apply to all devices unless otherwise indicated. In this table, 87C51/BH refers to 87C51/BH, 87C51-1/BH-1 and 87C51-2/BH-2. (Continued)

Symbol	Parameter	Oscillator						Units
		12 MHz		24 MHz		Variable		
		Min	Max	Min	Max	Min	Max	
TPXIX	Input Instr Hold After $\overline{PSEN}$	0		0		0		ns
TPXIZ	Input Instr Float After $\overline{PSEN}$							
	87C51/BH		59				TCLCL − 25	ns
	87C51-24/BH-24				21		TCLCL − 20	ns
TAVIV	Address to Valid Instr In		312		103		5TCLCL − 105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	400		150		6TCLCL − 100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		150		6TCLCL − 100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In							
	87C51/BH		252				5TCLCL − 165	ns
	87C51-24/BH-24				113		5TCLCL − 95	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		0		ns
TRHDZ	Data Float After $\overline{RD}$		107		23		2TCLCL − 60	ns
TLLDV	ALE Low to Valid Data In							
	87C51/BH		517				8TCLCL − 150	ns
	87C51-24/BH-24				243		8TCLCL − 90	ns
TAVDV	Address to Valid Data In							
	87C51/BH		585				9TCLCL − 165	ns
	87C51-24/BH-24				285		9TCLCL − 90	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	75	175	3TCLCL − 50	3TCLCL + 50	ns
TAVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low							
	87C51/BH	203				4TCLCL − 130		ns
	87C51-24/BH-24			77		4TCLCL − 90		ns
TQVWX	Data Valid to $\overline{WR}$ Transition							
	87C51/BH	33				TCLCL − 50		ns
	80C51-24/BH-24			12		TCLCL − 30		ns

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A:Address.
C:Clock.
D:Input data.
H:Logic level HIGH.
I:Instruction (program memory contents).
L:Logic level LOW, or ALE.
P:$\overline{\mathrm{PSEN}}$.
Q:Output data.
R:$\overline{\mathrm{RD}}$ signal.
T:Time.
V:Valid.
W:$\overline{\mathrm{WR}}$ signal.
X:No longer a valid logic level.
Z:Float.

For example,

TAVLL = Time from Address Valid to ALE Low.
TLLPL = Time from ALE Low to PSEN Low.

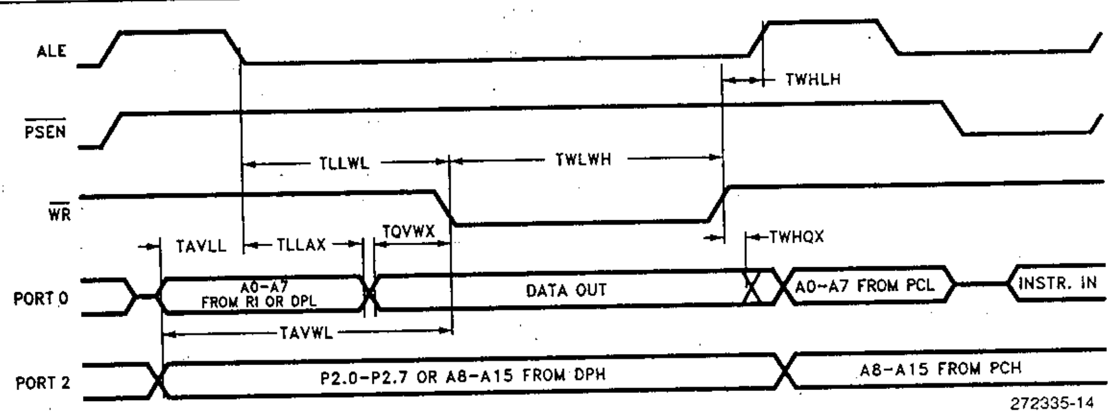
AC CHARACTERISTICS: (Over Operating Conditions; Load Capacitance for Port 0, ALE, and $\overline{\mathrm{PSEN}}$ = 100 pF; Load Capacitance for All Other Outputs = 80 pF)

EXTERNAL MEMORY CHARACTERISTICS

All parameter values apply to all devices unless otherwise indicated. In this table, 87C51/BH refers to 87C51/BH, 87C51-1/BH-1 and 87C51-2/BH-2.

Symbol	Parameter	Oscillator						Units
		12 MHz		24 MHz		Variable		
		Min	Max	Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency 87C51/BH 87C51-1/BH-1 87C51-2/BH-2 87C51-24/BH-24					 3.5 3.5 0.5 3.5	 12 16 12 24	 MHz MHz MHz MHz
TLHLL	ALE Pulse Width	127		43		2TCLCL − 40		ns
TAVLL	Address Valid to ALE Low 87C51/BH 87C51-24/BH-24	 43		 12		 TCLCL − 40 TCLCL − 30		 ns ns
TLLAX	Address Hold After ALE Low	53		12		TCLCL − 30		ns
TLLIV	ALE Low to Valid Instr In 87C51/BH 87C51-24/BH-24		 234		 91		 4TCLCL − 100 4TCLCL − 75	 ns ns
TLLPL	ALE Low to $\overline{\mathrm{PSEN}}$ Low	53		12		TCLCL − 30		ns
TPLPH	$\overline{\mathrm{PSEN}}$ Pulse Width	205		80		3TCLCL − 45		ns
TPLIV	$\overline{\mathrm{PSEN}}$ Low to Valid Instr In 87C51/BH 87C51-24/BH-24		 145		 35		 3TCLCL − 105 3TCLCL − 90	 ns ns

EXTERNAL DATA MEMORY WRITE CYCLE



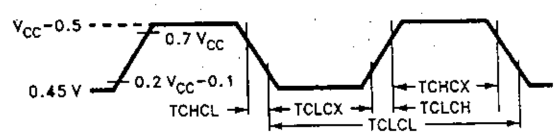
272335-14

EXTERNAL CLOCK DRIVE

All parameter values apply to all devices unless otherwise indicated. In this table, 87C51/BH refers to 87C51/BH, 87C51-1/BH-1 and 87C51-2/BH-2.

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency			
	87C51/BH	3.5	12	MHz
	87C51-1/BH-1	3.5	16	MHz
	87C51-2/BH-2	0.5	12	MHz
	87C51-24/BH-24	3.5	24	MHz
TCHCX	High Time			
	87C51/BH	20		ns
	8751-24/BH-24	0.35TCLCL	0.65TCLCL	ns
TCLCX	Low Time			
	87C51/BH	20		ns
	87C51-24/BH-24	0.35TCLCL	0.65TCLCL	ns
TCLCH	Rise Time			
	87C51/BH		20	ns
	87C51-24/BH-24		10	ns
TCHCL	Fall Time			
	87C51/BH		20	ns
	87C51-24/BH-24		10	ns

EXTERNAL CLOCK DRIVE WAVEFORM



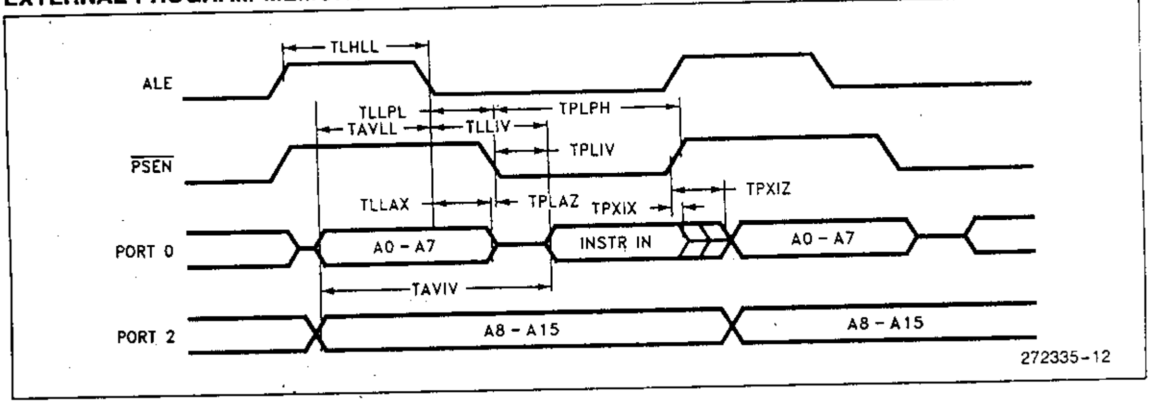
272335-15

EXTERNAL MEMORY CHARACTERISTICS

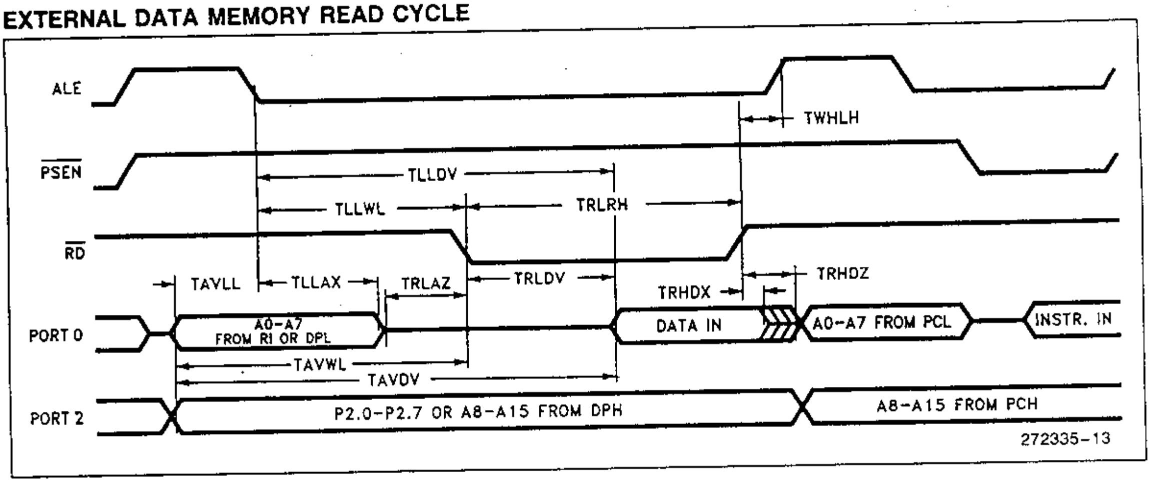
All parameter values apply to all devices unless otherwise indicated. In this table, 87C51/BH refers to 87C51/BH, 87C51-1/BH-1 and 87C51-2/BH-2. (Continued)

Symbol	Parameter	Oscillator 12 MHz Min	12 MHz Max	24 MHz Min	24 MHz Max	Variable Min	Variable Max	Units
TWHQX	Data Hold After $\overline{WR}$ 87C51/BH 87C51-24/BH-24	33		7		TCLCL − 50 TCLCL − 35		ns ns
TQVWH	Data Valid to $\overline{WR}$ High 87C51/BH 87C51-24/BH-24	433		222		7TCLCL − 150 7TCLCL − 70		ns ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High 87C51/BH 87C51-24/BH-24	43	123	12	71	TCLCL − 40 TCLCL − 30	TCLCL + 40 TCLCL + 30	ns ns

EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



80C51 FAMILY INSTRUCTION SET

Table 7. 80C51 Instruction Set Summary

· Interrupt Response Time: Refer to Hardware Description Chapter.

Instructions that Affect Flag Settings(1)

Instruction	C	OV	AC	Instruction	C	OV	AC
ADD	X	X	X	CLR C	0		
ADDC	X	X	X	CPL C	X		
SUBB	X	X	X	ANL C,bit	X		
MUL	0	X		ANL C,/bit	X		
DIV	0	X		ORL C,bit	X		
DA	X			ORL C,/bit	X		
RRC	X			MOV C,bit	X		
RLC	X			CJNE	X		
SETB C	1						

(1)Note that operations on SFR byte address 208 or bit addresses 209-215 (i.e., the PSW or bits in the PSW) will also affect flag settings.

Notes on instruction set and addressing modes:

Rn	Register R7-R0 of the currently selected Register Bank.
direct	8-bit internal data location's address. This could be an Internal Data RAM location (0-127) or a SFR [i.e., I/O port, control register, status register, etc. (128-255)].
@Ri	8-bit internal data RAM location (0-255) addressed indirectly through register R1 or R0.
#data	8-bit constant included in the instruction.
#data 16	16-bit constant included in the instruction
addr 16	16-bit destination address. Used by LCALL and LJMP. A branch can be anywhere within the 64k-byte Program Memory address space.
addr 11	11-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2k-byte page of program memory as the first byte of the following instruction.
rel	Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is −128 to +127 bytes relative to first byte of the following instruction.
bit	Direct Addressed bit in Internal Data RAM or Special Function Register.

MNEMONIC		DESCRIPTION	BYTE	OSCILLATOR PERIOD
ARITHMETIC OPERATIONS				
ADD	A,Rn	Add register to Accumulator	1	12
ADD	A,direct	Add direct byte to Accumulator	2	12
ADD	A,@Ri	Add indirect RAM to Accumulator	1	12
ADD	A,#data	Add immediate data to Accumulator	2	12
ADDC	A,Rn	Add register to Accumulator with carry	1	12
ADDC	A,direct	Add direct byte to Accumulator with carry	2	12
ADDC	A,@Ri	Add indirect RAM to Accumulator with carry	1	12
ADDC	A,#data	Add immediate data to A_{CC} with carry	2	12
SUBB	A,Rn	Subtract Register from A_{CC} with borrow	1	12
SUBB	A,direct	Subtract direct byte from A_{CC} with borrow	2	12
SUBB	A,@Ri	Subtract indirect RAM from A_{CC} with borrow	1	12
SUBB	A,#data	Subtract immediate data from A_{CC} with borrow	2	12
INC	A	Increment Accumulator	1	12
INC	Rn	Increment register	1	12

Table 7. 80C51 Instruction Set Summary (Continued)

MNEMONIC		DESCRIPTION	BYTE	OSCILLATOR PERIOD
ARITHMETIC OPERATIONS (Continued)				
INC	direct	Increment direct byte	2	12
INC	@Ri	Increment indirect RAM	1	12
DEC	A	Decrement Accumulator	1	12
DEC	Rn	Decrement Register	1	12
DEC	direct	Decrement direct byte	2	12
DEC	@Ri	Decrement indirect RAM	1	12
INC	DPTR	Increment Data Pointer	1	24
MUL	AB	Multiply A and B	1	48
DIV	AB	Divide A by B	1	48
DA	A	Decimal Adjust Accumulator	1	12
LOGICAL OPERATIONS				
ANL	A,Rn	AND Register to Accumulator	1	12
ANL	A,direct	AND direct byte to Accumulator	2	12
ANL	A,@Ri	AND indirect RAM to Accumulator	1	12
ANL	A,#data	AND immediate data to Accumulator	2	12
ANL	direct,A	AND Accumulator to direct byte	2	12
ANL	direct,#data	AND immediate data to direct byte	3	24
ORL	A,Rn	OR register to Accumulator	1	12
ORL	A,direct	OR direct byte to Accumulator	2	12
ORL	A,@Ri	OR indirect RAM to Accumulator	1	12
ORL	A,#data	OR immediate data to Accumulator	2	12
ORL	direct,A	OR Accumulator to direct byte	2	12
ORL	direct,#data	OR immediate data to direct byte	3	24
XRL	A,Rn	Exclusive-OR register to Accumulator	1	12
XRL	A,direct	Exclusive-OR direct byte to Accumulator	2	12
XRL	A,@Ri	Exclusive-OR indirect RAM to Accumulator	1	12
XRL	A,#data	Exclusive-OR immediate data to Accumulator	2	12
XRL	direct,A	Exclusive-OR Accumulator to direct byte	2	12
XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	24
CLR	A	Clear Accumulator	1	12
CPL	A	Complement Accumulator	1	12
RL	A	Rotate Accumulator left	1	12
RLC	A	Rotate Accumulator left through the carry	1	12
RR	A	Rotate Accumulator right	1	12
RRC	A	Rotate Accumulator right through the carry	1	12
SWAP	A	Swap nibbles within the Accumulator	1	12
DATA TRANSFER				
MOV	A,Rn	Move register to Accumulator	1	12
MOV	A,direct	Move direct byte to Accumulator	2	12
MOV	A,@Ri	Move indirect RAM to Accumulator	1	12

Table 7. 80C51 Instruction Set Summary (Continued)

MNEMONIC		DESCRIPTION	BYTE	OSCILLATOR PERIOD
DATA TRANSFER (Continued)				
MOV	A,#data	Move immediate data to Accumulator	2	12
MOV	Rn,A	Move Accumulator to register	1	12
MOV	Rn,direct	Move direct byte to register	2	24
MOV	RN,#data	Move immediate data to register	2	12
MOV	direct,A	Move Accumulator to direct byte	2	12
MOV	direct,Rn	Move register to direct byte	2	24
MOV	direct,direct	Move direct byte to direct	3	24
MOV	direct,@Ri	Move indirect RAM to direct byte	2	24
MOV	direct,#data	Move immediate data to direct byte	3	24
MOV	@Ri,A	Move Accumulator to indirect RAM	1	12
MOV	@Ri,direct	Move direct byte to indirect RAM	2	24
MOV	@Ri,#data	Move immediate data to indirect RAM	2	12
MOV	DPTR,#data16	Load Data Pointer with a 16-bit constant	3	24
MOVC	A,@A+DPTR	Move Code byte relative to DPTR to A_{CC}	1	24
MOVC	A,@A+PC	Move Code byte relative to PC to A_{CC}	1	24
MOVX	A,@Ri	Move external RAM (8-bit addr) to A_{CC}	1	24
MOVX	A,@DPTR	Move external RAM (16-bit addr) to A_{CC}	1	24
MOVX	A,@Ri,A	Move A_{CC} to external RAM (8-bit addr)	1	24
MOVX	@DPTR,A	Move A_{CC} to external RAM (16-bit addr)	1	24
PUSH	direct	Push direct byte onto stack	2	24
POP	direct	Pop direct byte from stack	2	24
XCH	A,Rn	Exchange register with Accumulator	1	12
XCH	A,direct	Exchange direct byte with Accumulator	2	12
XCH	A,@Ri	Exchange indirect RAM with Accumulator	1	12
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A_{CC}	1	12
BOOLEAN VARIABLE MANIPULATION				
CLR	C	Clear carry	1	12
CLR	bit	Clear direct bit	2	12
SETB	C	Set carry	1	12
SETB	bit	Set direct bit	2	12
CPL	C	Complement carry	1	12
CPL	bit	Complement direct bit	2	12
ANL	C,bit	AND direct bit to carry	2	24
ANL	C,/bit	AND complement of direct bit to carry	2	24
ORL	C,bit	OR direct bit to carry	2	24
ORL	C,/bit	OR complement of direct bit to carry	2	24
MOV	C,bit	Move direct bit to carry	2	12
MOV	bit,C	Move carry to direct bit	2	24
JC	rel	Jump if carry is set	2	24
JNC	rel	Jump if carry not set	2	24

Table 7. 80C51 Instruction Set Summary (Continued)

MNEMONIC		DESCRIPTION	BYTE	OSCILLATOR PERIOD
BOOLEAN VARIABLE MANIPULATION (Continued)				
JB	rel	Jump if direct bit is set	3	24
JNB	rel	Jump if direct bit is not set	3	24
JBC	bit,rel	Jump if direct bit is set and clear bit	3	24
PROGRAM BRANCHING				
ACALL	addr11	Absolute subroutine call	2	24
LCALL	addr16	Long subroutine call	3	24
RET		Return from subroutine	1	24
RETI		Return from interrupt	1	24
AJMP	addr11	Absolute jump	2	24
LJMP	addr16	Long jump	3	24
SJMP	rel	Short jump (relative addr)	2	24
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	24
JZ	rel	Jump if Accumulator is zero	2	24
JNZ	rel	Jump if Accumulator is not zero	2	24
CJNE	A,direct,rel	Compare direct byte to A_{CC} and jump if not equal	3	24
CJNE	A,#data,rel	Compare immediate to A_{CC} and jump if not equal	3	24
CJNE	RN,#data,rel	Compare immediate to register and jump if not equal	3	24
CJNE	@Ri,#data,rel	Compare immediate to indirect and jump if not equal	3	24
DJNZ	Rn,rel	Decrement register and jump if not zero	2	24
DJNZ	direct,rel	Decrement direct byte and jump if not zero	3	24
NOP		No operation	1	12

+5V Powered RS-232 Drivers/Receivers

ABSOLUTE MAXIMUM RATINGS

V_{CC} .... -0.3V to +6V
V^+ .... (V_{CC} - 0.3V) to +15V
V^- .... +0.3V to -15V
Input Voltages
  T_{IN} .... -0.3 to (V_{CC} + 0.3V)
  R_{IN} .... ±30V
Output Voltages
  T_{OUT} .... (V^+ + 0.3V) to (V^- - 0.3V)
  R_{OUT} .... -0.3V to (V_{CC} + 0.3V)
Short Circuit Duration
  T_{OUT} .... continuous
Power Dissipation
  CERDIP 675mW
    (derate 9.5mW/°C above +70°C)
  Plastic DIP 375mW
    (derate 7mW/°C above +70°C)
  Small Outline (SO) 375mW
    (derate 7mW/°C above +70°C)
Lead Temperature (soldering 10 seconds) .... +300°C
Storage Temperature .... -65°C to +160°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

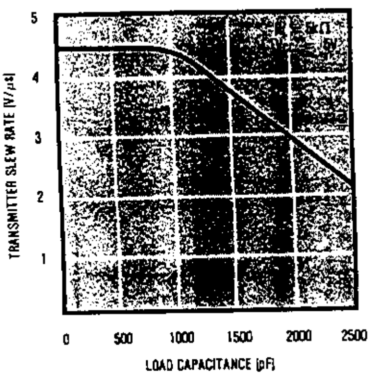
(MAX232, 234, 236, 237, 238, 240, 241 V_{CC} = 5V ± 10%; MAX233, 235 V_{CC} = 5V ± 5%; MAX231, 239 V_{CC} = 5V ± 10%, V^+ = 7.5V to 13.2V; T_A = Operating Temperature Range, Figures 3-14, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Output Voltage Swing	All Transmitter Outputs loaded with 3kΩ to Ground		±5	±9		V
V_{CC} Power Supply Current	No load, T_A = +25°C			5	10	mA
	MAX231, MAX239			0.4	1	
V^+ Power Supply Current	No load, MAX231 and MAX239 only	MAX231		1.8	5	mA
		MAX239		5	15	
Shutdown Supply Current	Figure 1, T_A = +25°C			1	10	µA
Input Logic Threshold Low	T_{IN}, $\overline{EN}$, Shutdown				0.8	V
Input Logic Threshold High	T_{IN}		2.0			V
	$\overline{EN}$, Shutdown		2.4			
Logic Pullup Current	T_{IN} = 0V			15	200	µA
RS-232 Input Voltage Operating Range			-30		+30	V
RS-232 Input Threshold Low	V_{CC} = 5V, T_A = +25°C		0.8	1.2		V
RS-232 Input Threshold High	V_{CC} = 5V, T_A = +25°C			1.7	2.4	V
RS-232 Input Hysteresis	V_{CC} = 5V		0.2	0.5	1.0	V
RS-232 Input Resistance	T_A = +25°C, V_{CC} = 5V		3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 1.6mA (MAX231-233, I_{OUT} = 3.2mA)				0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1.0mA		3.5			V
TTL/CMOS Output Leakage Current	$\overline{EN}$ = V_{CC}, 0V ≤ R_{OUT} ≤ V_{CC}			0.05	±10	µA
Output Enable Time (Figure 2)	MAX235, MAX236, MAX239, MAX240, 241			400		ns
Output Disable Time (Figure 2)	MAX235, MAX236, MAX239, MAX240, 241			250		ns
Propagation Delay	RS-232 to TTL			0.5		µs
Instantaneous Slew Rate	C_L = 10pF, R_L = 3-7kΩ, T_A = +25°C (Note 1)				30	V/µs
Transition Region Slew Rate	R_L = 3kΩ, C_L = 2500pF Measured from +3V to -3V or -3V to +3V			3		V/µs
Output Resistance	V_{CC} = V^+ = V^- = 0V, V_{OUT} = ±2V		300			Ω
RS-232 Output Short Circuit Current				±10		mA

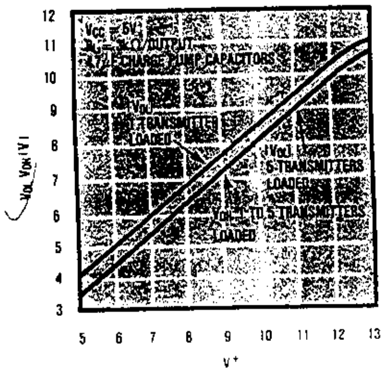
Note 1: Sample tested.

Typical Operating Characteristics

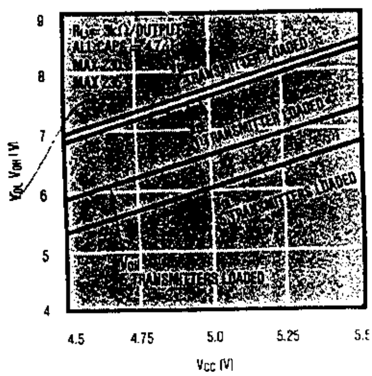
TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



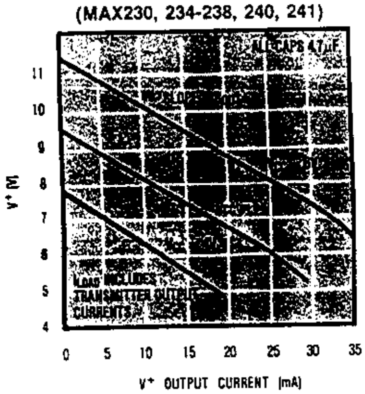
MAX239 TRANSMITTER OUTPUT VOLTAGE vs. V^+ VOLTAGE



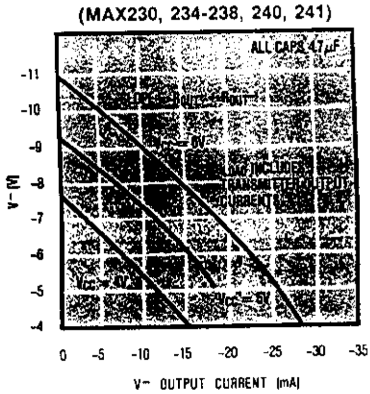
TRANSMITTER OUTPUT VOLTAGE vs. V_{CC} VOLTAGE



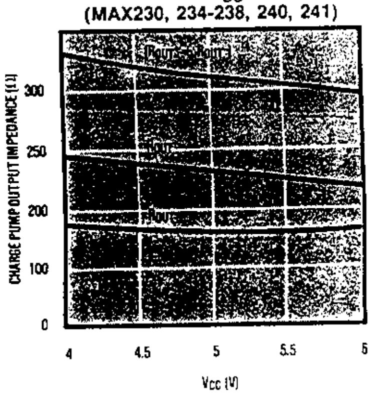
V^+ SUPPLY VOLTAGE vs. LOAD CURRENT (MAX230, 234-238, 240, 241)



V^- SUPPLY VOLTAGE vs. LOAD CURRENT (MAX230, 234-238, 240, 241)



CHARGE PUMP OUTPUT IMPEDANCE vs. V_{CC} (MAX230, 234-238, 240, 241)



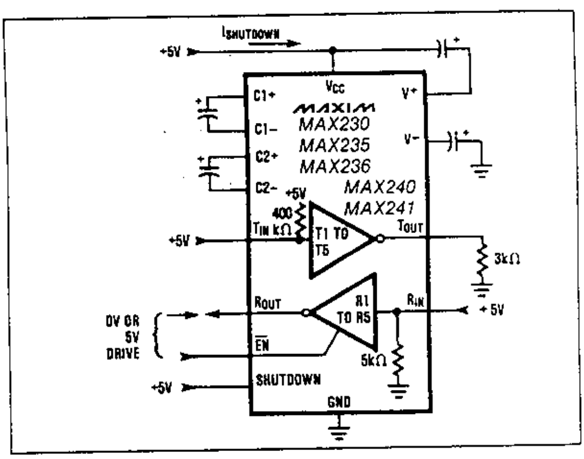


Figure 1. Shutdown Current Test Circuit

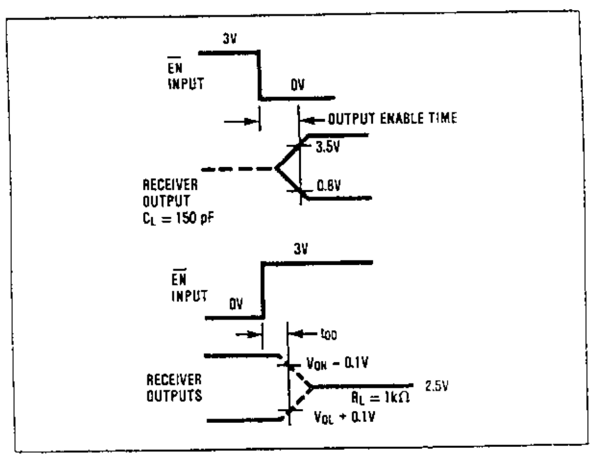


Figure 2. Receiver Output Enable and Disable Timing

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	-0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	0°C to 70°C
Operating Temperature (Industrial Version)	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
$\overline{ST}$ and $\overline{PBRST}$ Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1
$\overline{ST}$ and $\overline{PBRST}$ Input Low Level	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1.0		+1.0	µA	3
Output Current @ 2.4V	I_{OH}	-8	-10		mA	5
Output Current @ 0.4V	I_{OL}	8	10		mA	
Low Level @ RST	V_{OL}			0.4	V	1
Output Voltage @ -500 µA	V_{OH}	V_{CC} -0.5V	V_{CC} -0.1V		V	1, 7
Operating Current	I_{CC}		0.5	2.0	mA	2
V_{CC} Trip Point (TOL = GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL = V_{CC})	V_{CCTP}	4.25	4.37	4.49	V	1

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

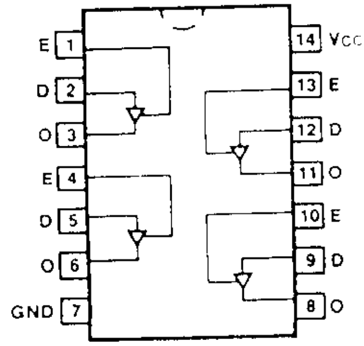
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{PBRST} = V_{IL}$	t_{PB}	20			ms	
RESET Active Time	t_{RST}	250	610	1000	ms	
$\overline{ST}$ Pulse Width	t_{ST}	20			ns	6, 8
V_{CC} Fail Detect to RST and $\overline{RST}$	t_{RPD}	40	100	175	µs	
V_{CC} Slew Rate 4.75V to 4.25V	t_F	300			µs	
V_{CC} Detect to RST and $\overline{RST}$ Transition	t_{RPU}	250	610	1000	ms	4
V_{CC} Slew Rate 4.25V to 4.75V	t_R	0	5		µs	
$\overline{PBRST}$ Stable Low to RST and $\overline{RST}$	t_{PDLY}			20	ms	

NOTES:

1. All voltages referenced to ground.
2. Measured with outputs open.
3. $\overline{PBRST}$ is internally pulled up to V_{CC} with an internal impedance of 10K typical.
4. t_R = 5 µs.
5. $\overline{RST}$ is an open drain output.
6. Must not exceed t_{TD} minimum. See Table 1.
7. RST remains within 0.5V of V_{CC} on power-down until V_{CC} drops below 2.0V. $\overline{RST}$ remains within 0.5V of GND on power-down until V_{CC} drops below 2.0V.
8. Watchdog can not be disabled. It must be strobed to avoid resets.

54/74126
54LS/74LS126
QUAD BUS BUFFER GATE
(With 3-State Outputs)

CONNECTION DIAGRAM
PINOUT A



DERING CODE: See Section 9

KGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
tic (P)	A	74126PC, 74LS126PC		9A
amic (D)	A	74126DC, 74LS126DC	54126DM, 54LS126DM	6A
pak)	A	74126FC, 74LS126FC	54126FM, 54LS126FM	31

TRUTH TABLE

INPUTS		OUTPUT
E	D	
H	L	L
H	H	H
L	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

UT LOADING/FAN-OUT: See Section 3 for U.L. definitions

NS	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
uts tputs	1.0/1.0 130/10 (50)	0.5/0.25 65/15 (25)/(7.5)

AND AC CHARACTERISTICS: See Section 3*

MBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
H	Output HIGH Voltage	XM	2.4				V	I_{OH} = -2.0 mA	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}
		XC	2.4					I_{OH} = -5.2 mA	
		XM			2.4			I_{OH} = -1.0 mA	
		XC			2.4			I_{OH} = -2.6 mA	
S	Output Short Circuit Current	XM	-30	-70	-30	-130	mA	V_{CC} = Max	
		XC	-28	-70	-30	-130			
C	Power Supply Current					24	mA	Outputs LOW, V_E = 4.5 V	V_{CC} = Max V_{IN} = Gnd
				62		20		Outputs OFF, V_E = 0 V	
LH HL	Propagation Delay Data to Output			13 18		15 18	ns	Figs. 3-3, 3-5	
ZH ZL	Output Enable Time			18 25		20 30	ns	Figs. 3-3, 3-11, 3-12	
LZ HZ	Output Disable Time			16 18		30 30	ns	Figs. 3-3, 3-11, 3-12	

C limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

PNP SILICON ANNULAR HERMETIC TRANSISTORS

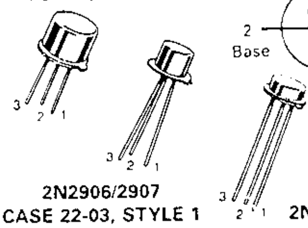
designed for high-speed switching circuits, DC to VHF amplifier applica-
s and complementary circuitry.

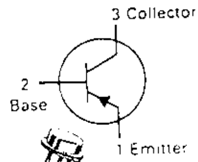
- igh DC Current Gain Specified — 0.1 to 500 mAdc
- igh Current-Gain — Bandwidth Product —
  f_T = 200 MHz (Min) @ I_C = 50 mAdc
- ow Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.4 Vdc (Max) @ I_C = 150 mAdc
- N2904, A thru 2N2907, A Complement to NPN 2N2218, A,
  2N2219, A, 2N2221, A, 2N2222, A
- AN, JANTX Available for 2N2904, A thru 2N2907, A

2N2904, A thru 2N2907, A 2N3485, A, 2N3486, A

JAN, JTX, JTXV AVAILABLE*

CASE 79-04, STYLE 1
TO-39 (TO-205AD)





2N2906/2907
CASE 22-03, STYLE 1
TO-18 (TO-206AA)

2N3485/3486
CASE 26-03, STYLE 1
TO-46 (TO-206AB)

GENERAL PURPOSE TRANSISTORS

PNP SILICON

***ALSO AVAILABLE JANS 2N2905AL AND JANS 2N2907A**

MAXIMUM RATINGS

Rating	Symbol	Non-A Suffix		A-Suffix	Unit
ollector-Emitter Voltage	V_{CEO}	40		60	Vdc
ollector-Base Voltage	V_{CBO}	60			Vdc
mitter-Base Voltage	V_{EBO}	5.0			Vdc
ollector Current — Continuous	I_C	600			mAdc
		2N2904,A 2N2905,A	2N2906,A 2N2907,A	2N3485,A 2N3486,A	
otal Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	600 3.43	400 2.28	400 2.28	mW mW/°C
otal Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	3.0 17.2	1.8 10.3	2.0 11.43	Watts mW/°C
)perating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200			°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage(1) (I_C = 10 mAdc, I_B = 0)	Non-A Suffix A-Suffix	$V_{(BR)CEO}$	40 60	— —	— —	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)		$V_{(BR)CBO}$	60	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)		$V_{(BR)EBO}$	5.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0.5 Vdc)		I_{CEX}	—	—	50	nAdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0)	Non-A Suffix A-Suffix	I_{CBO}	— —	— —	0.02 0.01	μAdc
(V_{CB} = 50 Vdc, I_E = 0, T_A = 150°C)	Non-A Suffix A-Suffix		— —	— —	20 10	
Base Current (V_{CE} = 30 Vdc, V_{BE} = 0.5 Vdc)		I_B	—	—	50	nAdc
ON CHARACTERISTICS						
DC Current Gain (I_C = 0.1 mAdc, V_{CE} = 10 Vdc)	2N2904, 2N2906, 2N3485 2N2905, 2N2907, 2N3486 2N2904A, 2N2906A, 2N3485A 2N2905A, 2N2907A, 2N3486A	h_{FE}	20 35 40 75	— — — —	— — — —	—
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)	2N2904, 2N2906, 2N3485 2N2905, 2N2907, 2N3486 2N2904A, 2N2906A, 2N3485A 2N2905A, 2N2907A, 2N3486A		25 50 40 100	— — — —	— — — —	
(I_C = 10 mAdc, V_{CE} = 10 Vdc)	2N2904, 2N2906, 2N3485 2N2905, 2N2907, 2N3486 2N2904A, 2N2906A, 2N3485A 2N2905A, 2N2907A, 2N3486A		35 75 40 100	— — — —	— — — —	

(continued)

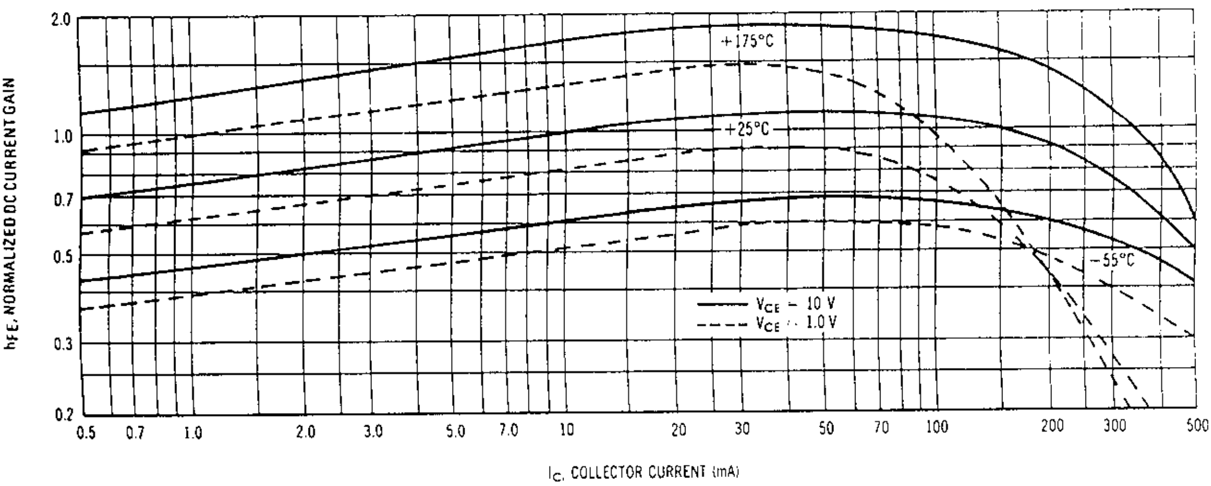
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS (continued)						
DC Current Gain (I_C = 150 mAdc, V_{CE} = 10 Vdc)(1)	2N2904A, 2N2906A, 2N3485A 2N2905A, 2N2907A, 2N3486A	h_{FE}	40 100	— —	120 300	
(I_C = 500 mAdc, V_{CE} = 10 Vdc)(1)	2N2904, 2N2906, 2N3485 2N2905, 2N2907, 2N3486 2N2904A, 2N2906A, 2N3485A 2N2905A, 2N2907A, 2N3486A		20 30 40 50	— — — —	— — — —	
Collector-Emitter Saturation Voltage(1) (I_C = 150 mAdc, I_B = 15 mAdc) (I_C = 500 mAdc, I_B = 50 mAdc)		$V_{CE(sat)}$	— —	— —	0.4 1.6	Vdc
Base-Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 15 mAdc)(1) (I_C = 500 mAdc, I_B = 50 mAdc)		$V_{BE(sat)}$	— —	— —	1.3 2.6	Vdc
DYNAMIC CHARACTERISTICS						
Current-Gain — Bandwidth Product(2) (I_C = 50 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)		f_T	200	—	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	—	—	8.0	pF
Input Capacitance (V_{BE} = 2.0 Vdc, I_C = 0, f = 100 kHz)		C_{ib}	—	—	30	pF
SWITCHING CHARACTERISTICS						
Turn-On Time	(V_{CC} = 30 Vdc, I_C = 150 mAdc, I_{B1} = 15 mAdc) (Figure 15a)	t_{on}	—	26	45	ns
Delay Time		t_d	—	6.0	10	
Rise Time		t_r	—	20	40	
Turn-Off Time	(V_{CC} = 6.0 Vdc, I_C = 150 mAdc, I_{B1} = I_{B2} = 15 mAdc) (Figure 15b)	t_{off}	—	70	100	ns
Storage Time		t_s	—	50	80	
Fall Time		t_f	—	20	30	

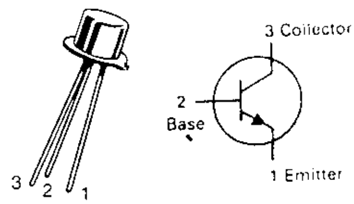
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

FIGURE 1 – NORMALIZED DC CURRENT GAIN



BC107, A, B, C
thru
BC109, A, B, C

CASE 22-03, STYLE 1
TO-18 (TO-206AA)



TRANSISTORS
NPN SILICON

MAXIMUM RATINGS

Rating	Symbol	BC 107	BC 108	BC 109	Unit
Collector-Emitter Voltage	V_{CEO}	45	25	25	Vdc
Collector-Base Voltage	V_{CBO}	50	30	30	Vdc
Emitter-Base Voltage	V_{EBO}	6	5	5	Vdc
Collector Current — Continuous	I_C	0.2			Amp
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	0.6 2.28			Watt mW/°C
Total Device Dissipation @ $T_C = 25°C$ $T_C = 100°C$ Derate above 25°C	P_D	1 6.67			Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	175	°C/W

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector Base Leakage Current ($I_E = 0$, $V_{CB} = 45$ V) ($I_E = 0$, $V_{CB} = 45$ V, $T_{Amb} = 125°C$) ($I_E = 0$, $V_{CB} = 25$ V) ($I_E = 0$, $V_{CB} = 25$ V, $T_{Amb} = 125°C$)	 BC107 BC107 BC108/109 BC108/109	I_{CBO}			 15 4 15 4	 nA μA nA μA
Emitter Base Breakdown Voltage ($I_E = 10$ μA, $I_C = 0$)	 BC107 BC108/109	$V_{(BR)EBO}$	 6 5			V
Collector Emitter Breakdown Voltage ($I_C = 2$ mA, $I_E = 0$)	 BC107 BC108/109	$V_{(BR)CEO}$	 45 25			V
ON CHARACTERISTICS						
DC Current gain ($V_{CE} = 5$ V, $I_C = 2$ mA) ($V_{CE} = 5$ V, $I_C = 10$ μA)	BC107 BC108 BC109 A group B group C group B group C group	h_{FE}	110 110 200 110 200 420 40 100		450 800 800 220 450 800	
Base Emitter Saturation Voltage ($I_C = 10$ mA, $I_B = 0.5$ mA) ($I_C = 100$ mA, $I_B = 5$ mA)		$V_{BE(sat)}$		 0.7 1.0	 0.83 1.05	V
Collector Emitter Saturation Voltage ($I_C = 10$ mA, $I_B = 0.5$ mA) ($I_C = 100$ mA, $I_B = 5$ mA)		$V_{CE(sat)}$			 0.25 0.60	V
Base Emitter on Voltage ($I_C = 2$ mA, $V_{CE} = 5$ V) ($I_C = 10$ mA, $V_{CE} = 5$ V)		$V_{BE(on)}$	 0.55		 0.70 0.77	V
Collector Knee Voltage ($I_C = 10$ mA, I_B = the value for which $I_C = 11$ mA at $V_{CE} = 1$ V)		$V_{CE(K)}$		0.4	0.6	V
DYNAMIC CHARACTERISTICS						
Transition Frequency ($I_C = 10$ mA, f = 100 MHz, $V_{CE} = 5$ V)		f_T	150	300		MHz
Noise Figure ($V_{CE} = 5$ V, $I_C = 0.2$ mA, $R_g = 2$ KΩ) F = 30 Hz to 15 kHz F = 1 kHz, ΔF = 200 Hz	 BC109 BC109 BC107/108	NF			 4 4 10	dB

BC107, A, B, C thru BC109, A, B, C

ECTRICAL CHARACTERISTICS (continued) (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
put Capacitance (V_{CB} = 10 V, f = 1 MHz)		C_{obo}			4.5	pF
e Parameters (V_{CE} = 5 V, I_C = 2 mA, f = 1 kHz)	BC107/108 BC109	h_{21e}	125 240		500 900	
	A group B group C group		125 240 450		260 500 900	
1e Parameters (V_{CE} = 5 V, I_C = 2 mA, f = 1 kHz)	A group B group C group	h_{11e}	1.6 3.2 6.0		4.5 8.5 15	KΩ
2e Parameters (V_{CE} = 5 V, I_C = 2 mA, f = 1 kHz)	A group B group C group	h_{22e}			30 60 110	µhos

FIGURE 1 — EMITTER-BASE CAPACITANCE
COLLECTOR-BASE CAPACITANCE

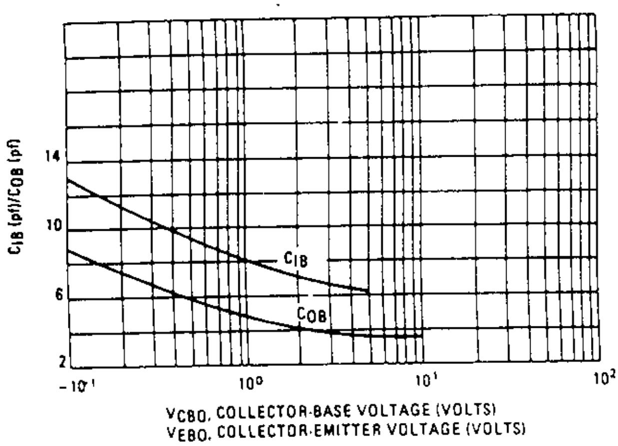


FIGURE 2 — CURRENT GAIN — BANDWIDTH PRODUCT

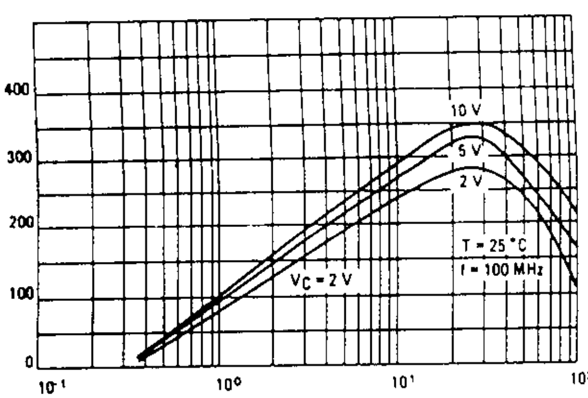
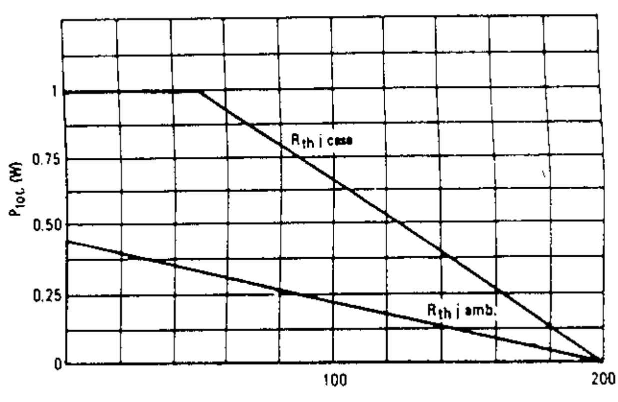


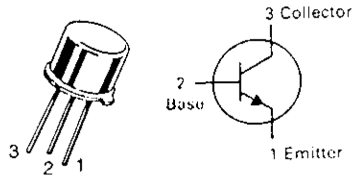
FIGURE 3 — TOTAL PERMISSIBLE POWER DISSIPATION



2N1711 For Specifications, See 2N718A Data.

2N1893

CASE 79-04, STYLE 1
TO-39 (TO-205AD)



GENERAL PURPOSE TRANSISTOR

NPN SILICON

Refer to 2N3019 for graphs.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	80	Vdc
Collector-Emitter Voltage	V_{CER}	100	Vdc
Collector-Base Voltage	V_{CBO}	120	Vdc
Emitter-Base Voltage	V_{EBO}	7.0	Vdc
Collector Current — Continuous	I_C	0.5	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	0.8 4.57	Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	3.0 17.2	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	58.3	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	219	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, R_{BE} = 10 ohms)	$V_{CER(sus)}$	100	—	Vdc
Collector-Emitter Sustaining Voltage(1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	80	—	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	$V_{(BR)CBO}$	120	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	$V_{(BR)EBO}$	7.0	—	Vdc
Collector Cutoff Current (V_{CB} = 90 Vdc, I_E = 0) (V_{CB} = 90 Vdc, I_E = 0, T_A = 150°C)	I_{CBO}	— —	0.01 15	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	0.01	μAdc
ON CHARACTERISTICS				
DC Current Gain(1) (I_C = 0.1 mAdc, V_{CE} = 10 Vdc) (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 10 mAdc, V_{CE} = 10 Vdc, T_A = −55°C) (I_C = 150 mAdc, V_{CE} = 10 Vdc)	h_{FE}	20 35 20 40	— — — 120	—
Collector-Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 5.0 mAdc) (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{CE(sat)}$	— —	1.2 5.0	Vdc
Base-Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 5.0 mAdc) (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{BE(sat)}$	— —	0.9 1.3	Vdc
SMALL-SIGNAL CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)	f_T	50	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, 100 kHz ≤ f ≤ 1.0 MHz)	C_{obo}	—	15	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, 100 kHz ≤ f ≤ 1.0 MHz)	C_{ibo}	—	85	pF
Input Impedance (I_C = 1.0 mAdc, V_{CB} = 5.0 Vdc, f = 1.0 kHz) (I_C = 5.0 mAdc, V_{CB} = 10 Vdc, f = 1.0 kHz)	h_{ib}	20 4.0	30 8.0	Ohms
Voltage Feedback Ratio (I_C = 1.0 mAdc, V_{CB} = 5.0 Vdc, f = 1.0 kHz) (I_C = 5.0 mAdc, V_{CB} = 10 Vdc, f = 1.0 kHz)	h_{rb}	— —	1.25 1.5	$\times 10^{-4}$
Small-Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz) (I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	30 45	100 —	—
Output Admittance (I_C = 1.0 mAdc, V_{CB} = 5.0 Vdc, f = 1.0 kHz) (I_C = 5.0 mAdc, V_{CB} = 10 Vdc, f = 1.0 kHz)	h_{ob}	— —	0.5 0.5	μmho

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

QUAD VOLTAGE COMPARATOR

LM139/239/339 MC3302/LM2901

DESCRIPTION

he LM139 series consists of four inde-endent precision voltage comparators vith an offset voltage specification as low as .0mV max for each comparator which were esigned specifically to operate from a ingle power supply over a wide range of oltages. Operation from split power sup-lies is also possible and the low power upply current drain is independent of the nagnitude of the power supply voltage. hese comparators also have a unique haracteristic in that the input common node voltage range includes ground, even hough operated from a single power supply oltage.

The LM139 series was designed to directly interface with TTL and CMOS. When oper-ated from both plus and minus power sup-plies, the LM139 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard com-parators.

FEATURES

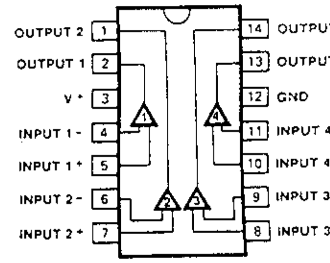
- Wide single supply voltage range 2.0Vdc to 36Vdc or dual supplies ±1.0Vdc to ±18Vdc
- Very low supply current drain (0.8mA) independent of supply voltage (1.0mW/-comparator at 5.0Vdc)
- Low input biasing current 25nA
- Low input offset currrent ±5nA and offset voltage ±2mV
- Input common-mode voltage range In-cludes ground
- Differential input voltage range equal to the power supply voltage.
- Low output 250mV at 4mA saturation voltage
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic sys-tems.

APPLICATIONS

- A/D converters
- Wide range VCO
- MOS clock generator
- High voltage logic gate
- Multivibrators

PIN CONFIGURATION

D,F,N PACKAGE



TOP VIEW

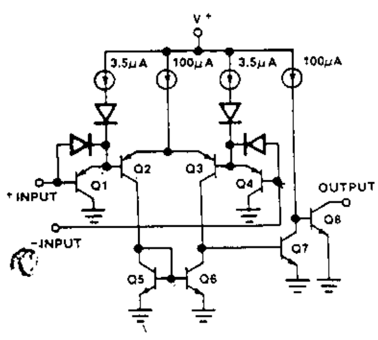
ORDER NUMBERS
LM139/239/339F,N LM2901F,N
MC3302F,N LM339D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Vcc supply voltage	36 or ±18	
Differential input voltage	36	
Input voltage	-0.3 to +36	
Power dissipation[1]		
Molded DIP	570	mW
CERDIP	900	mW
Output short circuit to ground[2]	Continuous	
Input current ($V_{IN} < -0.3Vdc$)[3]	50	mA
Operating temperature range		
LM139	-55 to +125	°C
LM239	-25 to +85	°C
LM339	0 to +70	°C
LM2901/MC3302	-40 to +85	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 10 sec.)	300	°C

EQUIVALENT CIRCUIT

(1 Comparator Only)



ELECTRICAL CHARACTERISTICS

$V+ = 5Vdc$, LM139: $-55°C \leq T_A \leq 125°C$ unless otherwise specified
LM239: $-25°C \leq T_A \leq 85°C$ unless otherwise specified
LM339: $0°C \leq T_A \leq 70°C$ unless otherwise specified

	PARAMETER	TEST CONDITIONS	LM139			LM239/339			UNIT
			Min	Typ	Max	Min	Typ	Max	
s	Input offset voltage[5]	$T_A = 25°C$ Over temp.		±2.0	±5.0 9.0		±2.0	±5.0 9.0	mV
M	Input common mode voltage range[6]	$T_A = 25°C$ Over temp.	0 0		V+-1.5 V+-2.0	0 0		V+-1.5 V+-2.0	V
R	Differential input voltage[4]	Keep all V_{IN}'s ≥ 0Vdc (or V- if used)			V+			V+	V
	Input bias current[7]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25°C$ Over temp.		25	100 300		25	250 400	nA
s	Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25°C$ Over temp.		±3.0	±25 ±100		±5.0	±50 ±150	nA nA
L	Output sink current	$V_{IN(-)} \geq 1Vdc$, $V_{IN(+)} = 0$, $V_O \leq 1.5Vdc$, $T_A = 25°C$	6.0	16		6.0	16		mA
H	Output leakage current	$V_{IN(+)} \geq 1Vdc$, $V_{IN(-)} = 0$ $V_O = 5Vdc$, $T_A = 25°C$ $V_O = 30Vdc$, over temp.		0.1	 1.0		0.1	 1.0	nA µA
C	Supply current	$R_L = \infty$ on all comparators, $T_A = 25°C$		0.8	2.0		0.8	2.0	mA
V	Voltage gain	$R_L \geq 15k\Omega$, $V+ = 15Vdc$ $T_A = 25°C$	50	200		50	200		V/mV
OL	Saturation voltage	$V_{IN(-)} \geq 1Vdc$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4mA$ $T_A = 25°C$ Over temp.		250	400 700		250	400 700	mV
LSR	Large signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4Vdc$, $V_{RL} = 5Vdc$, $R_L = 5.1k\Omega$, $T_A = 25°C$		300			300		ns
R	Response time[8]	$V_{RL} = 5Vdc$, $R_L = 5.1k\Omega$, $T_A = 25°C$		1.3			1.3		µs

TES

For operating at high temperatures, the LM339/339A, LM2901 and MC3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM139/139A/239/239A must be derated on a 150°C maximum junction temperature. The low power dissipation and the "On-Off" characteristics of the outputs keep the chip dissipation very small ($P_D \leq 100mW$), provided the output transistors are allowed to saturate.

Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V+.

This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3Vdc.

4. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3Vdc (or 0.3Vdc below the magnitude of the negative power supply, if used).
5. At output switch point, $V_O \approx 1.4Vdc$, $R_S = 0\Omega$ with V+ from 5Vdc to 30Vdc; and over the full input common-mode range (0Vdc to V+ -1.5Vdc).
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ -1.5V, but either or both inputs can go to 30Vdc without damage.
7. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
8. The response time specified is for a 100mV input step with a 5mV overdrive. For larger overdrive signals, 300ns can be obtained, see typical performance characteristics section.

ELECTRICAL CHARACTERISTICS

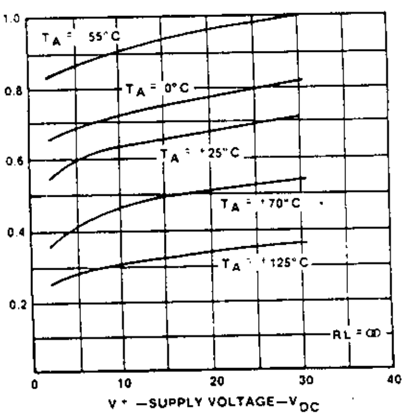
$V+ = 15Vdc$, MC3302
LM2901/MC3302: $-40°C \leq T_A \leq 85°C$ unless otherwise specified

PARAMETER		TEST CONDITIONS	LM2901			MC3302			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[5]	$T_A = 25°C$ Over temp.		±2.0 ±9	±7.0 ±15		±3.0	±20 ±40	mV
V_{CM}	Input common mode voltage range[6]	$T_A = 25°C$ Over temp.	0 0		V+-1.5 V+-2.0			V+-1.5 V+-2.0	V
V_{IDR}	Differential input voltage[4]	Keep all V_{IN}'s $\geq$ 0Vdc (or V- if need)			V+			V+	V
I_B	Input bias current[7]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25°C$ Over temp.		25 200	250 500		25	500 1000	nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25°C$ Over temp.		±5 ±50	±50 ±200		±5		nA nA
I_{OL}	Output sink current	$V_{IN(-)} \geq 1Vdc$, $V_{IN(+)} = 0$, $V_O \leq 1.5Vdc$, $T_A = 25°C$ $V_O = 800mV$, Over temp.	6.0	16		2.0			mA
I_{OH}	Output leakage current	$V_{IN(+)} \geq 1Vdc$, $V_{IN(-)} = 0$ $V_O = 5Vdc$, $T_A = 25°C$ $V_O = 30V$ Over temp. $V_O = 28V$ $T_A = 25°C$		0.1	1.0		0.1	1.0	nA μA
I_{CC}	Supply current	$R_L = \infty$ on comparators, $V+ = 5Vdc$, $T_A = 25°C$ $V+ = 30V$, $T_A = 25°C$ $V+ = 5$ to 28 Vdc, $T_A = 25°C$		0.8 1.0	2.0 2.5		0.8	2.0	mA
A_V	Voltage gain	$R_L \geq 15k\Omega$, $V+ = 15Vdc$ $T_A = 25°C$	25	100		2	100		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)} \geq 1Vdc$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4mA$ $T_A = 25°C$ Over temp. $I_{SINK} = 2mA$, $V+ = 5V$ to 28V, $T_A = 25°C$		400	400 700		150	400	mV
T_{LSR}	Large signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4Vdc$, $V_{RL} = 5Vdc$, $R_L = 5.1k\Omega$, $T_A = 25°C$		300			300		ns
T_R	Response time[8]	$V_{RL} = 5Vdc$, $R_L = 5.1k\Omega$, $T_A = 25°C$		1.3			1.3		μs

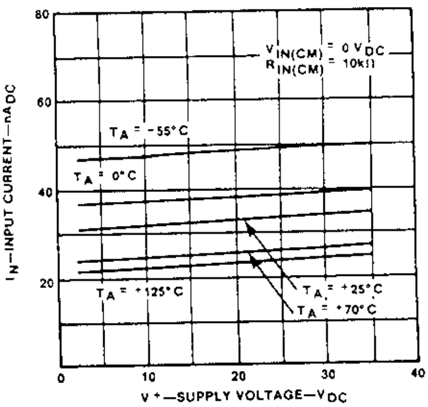
otes 1-8, refer to preceding page.

PICAL PERFORMANCE CHARACTERISTICS

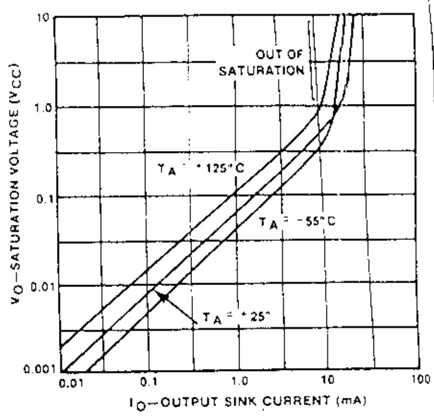
SUPPLY CURRENT



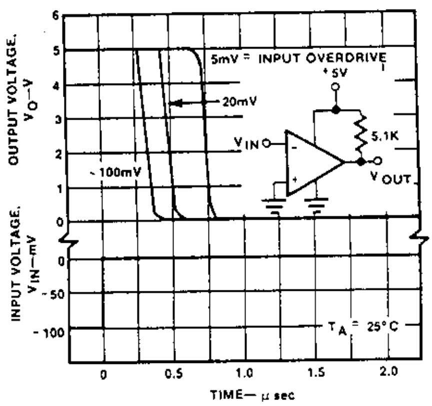
INPUT CURRENT



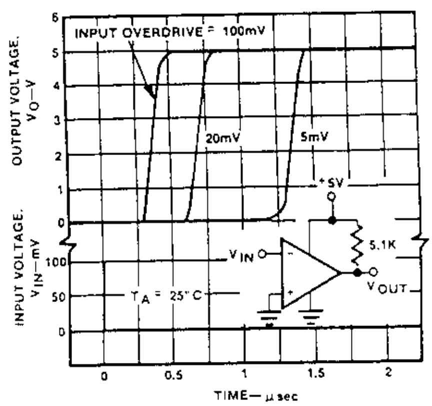
OUTPUT SATURATION VOLTAGE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES— NEGATIVE TRANSITION



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES— POSITIVE TRANSITION



SIEMENS

SFH600 SERIES

TRIOS®* PHOTOTRANSISTOR OPTOCOUPLER

FEATURES

- **High Current Transfer Ratios**
  SFH600-0, 40 to 80%
  SFH600-1, 63 to 125%
  SFH600-2, 100 to 200%
  SFH600-3, 160 to 320%
- **Withstand Test Voltage (1 Minute), 5300 V**
- **V_{CEsat} 0.25 (≤0.4) V, I_F=10 mA, I_C=2.5 mA**
- **High Quality Premium Device**
- **Long Term Stability**
- **Storage Temperature, –55° to +150°C**
- **Underwriters Lab File #E52744**
- **Options Available: 1, 2, 3, 4, 6, 7, 9**

DESCRIPTION

The SFH600 is an optocoupler with a GaAs LED emitter which is optically coupled with a silicon planar phototransistor detector. The component is packaged in a plastic plug-in case, 20 AB DIN 41866.

The coupler transmits signals between two electrically isolated circuits. The potential difference between the circuits to be coupled is not allowed to exceed the maximum permissible insulating voltage.

Maximum Ratings

Emitter

Reverse Voltage .... 6 V
DC Forward Current .... 60 mA
Surge Forward Current (t_p=10 µs) .... 2.5 A
Total Power Dissipation .... 100 mW

Detector

Collector-Emitter Voltage .... 70 V
Emitter-Base Voltage .... 7 V
Collector Current .... 50 mA
Collector Current (t=1 ms) .... 100 mA
Power Dissipation .... 150 mW

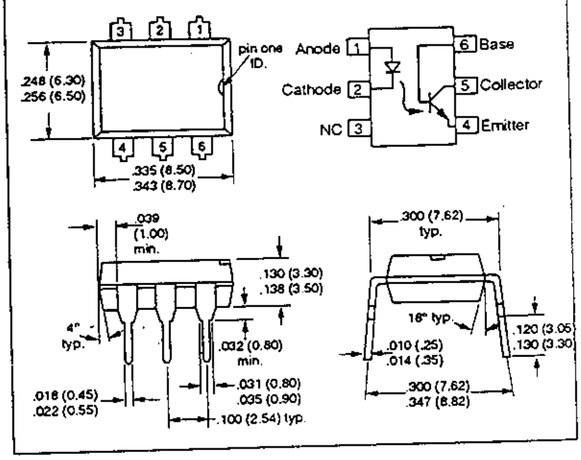
Package

Isolation Test Voltage between Emitter and Detector referred to Climate DIN 40046, part 2, Nov. 74 .... 5300 VDC
Creepage Distance .... ≥7 mm
Clearance Distance .... ≥7 mm
Isolation Thickness between Emitter & Detector . ≥0.4 mm
Comparative Tracking Index per DIN IEC 112/VDE0303, part 1 175
Insulation Resistance
V_{IO}=500 V, T_A=25°C .... ≥10^{12} Ω
V_{IO}=500 V, T_A=100°C .... ≥10^{11} Ω

Package

Storage Temperature Range .... –55°C to +150°C
Ambient Temperature Range .... –55°C to +100°C
Junction Temperature .... 100°C
Soldering Temperature (max. 10 s, dip soldering: distance to seating plane ≥1.5 mm) .... 260°C

Package Dimensions in Inches (mm)



Characteristics (T_A=25°C)

	Symbol		Unit	Condition
Emitter				
Forward Voltage	V_F	1.25 (≤1.65)	V	I_F=60 mA
Breakdown Voltage	V_{BR}	≥6	V	I_R=10 µA
Reverse Current	I_R	0.01 (≤10)	µA	V_R=6 V
Capacitance	C_O	25	pF	V_R=0 V, f=1 MHz
Thermal Resistance	R_{THJamb}	750	°C/W	
Detector				
Capacitance			pF	f=1 MHz
Collector-Emitter	C_{CE}	5.2		V_{CE}=5 V
Collector-Base	C_{CB}	6.5		V_{CB}=5 V
Emitter-Base	C_{EB}	9.5		V_{EB}=5 V
Thermal Resistance	R_{THJamb}	500	°C/W	
Package				
Collector-Emitter Saturation Voltage	V_{CEsat}	0.25 (≤0.4)	V	I_F=10 mA, I_C=2.5 mA
Coupling Capacitance	C_{IO}	0.6	pF	V_{IO}=0, f=1 MHz

*TRIOS–TRansparent IOn Shield