PC BASED ECG MONITOR

Project work

submitted by

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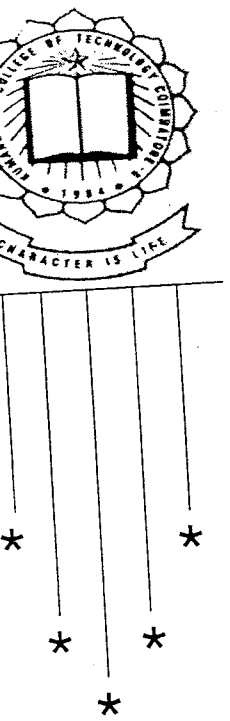

2000 - 2001

Under the Guidance of
Prof.K.RAM PRAKASH, M.E.,M.I.S.T.E.,

in partial fulfilment of the requirements
for the award of the Degree of
BACHELOR OF ENGINEERING IN
ELECTRONICS AND COMMUNICATION ENGINEERING
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Coimbatore-641 046.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
Kumaraguru College Of Technology
COIMBATORE- 641 006
2000-2001

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

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COIMBATORE-641006.

(Affiliated to Bharathiyar University)

CERTIFICATE

This is to certify that the Project Report entitled

PC BASED ECG MONITOR

has been submitted by

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in partial fulfillment for the award of the degree of Bachelor of Engineering in **ELECTRONICS AND COMMUNICATION ENGINEERING** Branch of the Bharathiar University, Coimbatore – 641 006 during the academic year 2000-2001

Faculty Guide

Head of the Department

Certified that the Candidate was examined by us in the project work viva-voce Examination held on 12.03.2001 and the university register No. was _____.

Internal Examiner

12/3

12.03.2k

External Examiner

ACKNOWLEDGEMENT

Our project report would be duly complete only if we thank our beloved principal **Dr.K.K.PADMANABHAN, B.Sc.(Engg.) M.Tech.,Ph.D** for all his well wishes and inspiring thoughts.

Our Head of the department, **PROF.M.RAMASAMY M.E,** has always guided us with his ever valuable suggestions.We express our sincere gratitude for helping us to complete this project in a successful manner.

We would like to express our sincere thanks to our project guide **PROF.K.RAMPRAKASH M.E,MISTE,**who had lent us his fullest support during the progress of our project. He had always been ready to clear our skeptics. Without his inspiring guidance , we would not have completed the project.

We would also like to thank our class advisor **Mrs.S.LATHA B.E** and all the staff members of ECE department for their constant support in our endeavour.

SYNOPSIS

Our system involves the analysis and evaluation of Electrocardiogram which measures the output from an unknown system as they are affected by various combinations of inputs with the objective to learn the nature and characterstics of human body.

The analysis of electrocardiogram is of great importance to the medical practices. This is due to the fact that a large percentage of deaths occurring in the world are mostly due to the disorder associated with cardiovascular system. Though many systems are available commercially our system provides the analysis of multiple patients using a computer.

Since the pc's have become an essential tool in daily life, this would simply be an additional facility to the user especially the cardiologist. The computer enables enhancement of the ECG signal from the background of noise and artifacts and makes it possible to derive the accurate measurement.

In our system we have the provision of monitoring ECG of multiple patients. The patient and lead selection is made Programmable . The data of all patients are stored temporarily in buffer memory. The computer reads the buffer memory through an input port and is displayed on the monitor. The software for acquiring the ECG data and displaying is written in C language.

However this project is an attempt to satisfy the need for a simple and inexpensive method of monitoring the ECG which will result in saving time and effort for both the patient and physician.

CONTENTS

INTRODUCTION

Most of the ECG machines used for clinical purpose are single channel machines . such machines usually carry a multiposition switch , by means of which the desired lead connection can be selected. only one lead at a time can be recorded with such type of instruments.

Multichannel ECG machines carry several amplifier channels and a corresponding number of recording pens. This facilitates recording of several ECG leads simultaneously and thus considerably reduce the time required to a complete set of recordings.Another advantage of multichannel recording is that the waveforms are recorded simultaneously and they can be shown in their proper time relationship with respect to each other.

We have in this project a system for monitoring ECG of multiple patients using computer . The patient and lead selection is made programmable and a differential amplifier is used for amplifying ECG ,band limited to 100Hz.

1.1 BLOCK DIAGRAM DESCRIPTION

Simplified block diagram of PC based ECG monitoring system is shown in figure. The multi-patient ECG monitoring developed will replace bed side monitors. With this system any lead of the patients as desired by the physician can be monitored. The signals from each patient is picked up by the sensor and are connected to the patient and lead selecting circuitry and this will generate select lines and address lines for the memory.

The differential signals are obtained from various combinations of right arm, left arm, leg leg and right leg grounded always. The signals obtained from these combination is given to pre-amplifier section where electrical noise picked up with ECG signal has to be eliminated. The noise free signal is given to filter section to provide consistent filtering inspite of variations in the load.

The as an electrolyte between the skin and the electrodes. There are four types of electrode systems. Electrodes used to sense ECG are of many types. Pre-filtered signal is given to analog to digital converter which is used to translate the value of current or voltage into corresponding binary number. This digitized signals of all patients is temporarily stored in the buffer memory.

The computer reads the buffer memory through an input port nd is displayed on the monitor. The interface with the computer is achieved sing a standard bus Add -on card installed in the computer. The software or acquiring the ECG data and displaying is written in C language.

The computerized ECG analysis system must comprise of the following subsystems:

1. ECG Amplifier, Filter, ADC .
2. Reduction of ECG signals.
3. Recognition of QRS complex.
4. Determining whether the beat is normal / abnormal.

In our system we have tried to implement the subsystems accordingly. Pre-jelled electrodes are used to pick the ECG signals. The signals are fed through a high pass filter with a cutoff at 0.05 Hz f ollowed by a low pass filter at 100 Hz.The ECG signal is digitized using an ADC. This is done for a period of around 4 sec during which the data is fed to the computer for analysis.

The detailed description of all the incorporated sub systems of the system block diagram shown in the figure 1.1.1

.1.1 Leads and Electrodes

The potentials generated in the heart are conducted to the body surface. The potential distribution changes in the body surface . The potential distribution changes in a regular and complex manner during each cardiac cycle. To record the electrocardiogram the jelly used in the electrodes acts jelled Disposable, Limb, Floating , Pasteless are few examples of these. Since floating electrodes are non-toxic, stable for a l ong period or time and non-polarisable, they are used here. Skin contact impedance of theselectrodes ranges between 2 to 5 Kohms. The difference of voltage measured between the two limb electrodes is always with reference to a third electrode. This is always connected to the right leg and acts as a reference point . The earth potential picked here are passed on to the next stage.

1.1.2 Signal Conditioning Circuitry

ECG Amplifier :

The electrical noise picked up with the ECG signal has to be eliminated . This circuit consists of the amplifying and filtering stages.A differential amplifier is used in the first stage.This has been basically owing to the excellent common mode interference rejection capabilities of the difference in the heart generated voltages which are ranging in amplitudes at

different rates and patterns.Besides these amplifiers exhibit good stability and versatility. Hence an operational amplifier with high input impedance, high CMRR is used in the differential configuration.

The total gain from the pre amplifier stage upto the low pass filter is around 20 . To further boost the amplitude of the heart signal an amplifier in non-inverting mode is used.The gain of this stage is 1000

The filters used in the system are active filters . An active for employs transistor or op-amp in addition to resistor and capacitor.

Active are used here because of the following advantages :

1. Gain and frequency adjustment feasibility.
2. More economical than passive filters
3. Eliminates the need of high cost inductors.
4. Does not cause loading of source or load.
5. Provides consistent filtering inspite of variations in the load.

High Pass Filter :

High pass filter is used to eliminate the low frequency signals,such as contact potentials and offset voltages. These signals would have otherwise resulted in saturation of sucessive stages.Since the desired ECG signal lies between 0.05 Hz and 100 Hz , the cut off frequency has been chosen to lie at 0.05 Hz . The gain of the circuit is 21. This stage also

In our system we have chosen one of the most widely used 12 bit Successive Approximation type ADC. This is chosen on the basis of its speed, cost and accuracy. Hence the conversion of analogue ECG signals into digital is carried out in a highly accurate manner. The data sheet of the converter is also given for reference.

1.1.5 Interfacing Unit

The interface with the computer is one of the most important constituent of the system.. The main parts of an interfacing unit are ADC and Peripheral Interface.It also has buffers,comparators, decorders and latches. Its also called as I / O card or ADD - ON Card. The comparator is used for fixing the base address.They are usually used for amplifying current or power. Here we are using bi- directionals buffers for data bus and uni-directional buffers for address bus. The signal from the ADC is given to the personal computerand the signal is processed in the CPU of the PC.

1.1.6 Software And Display Unit

Software for acquiring ECG data and displaying it on the PC is written in C language. This software facilitates the selection of leads as required by the doctor. With this facility we can also print the patient name as well as bed number with respect to the corresponding ECG waveform.

BLOCK DIAGRAM

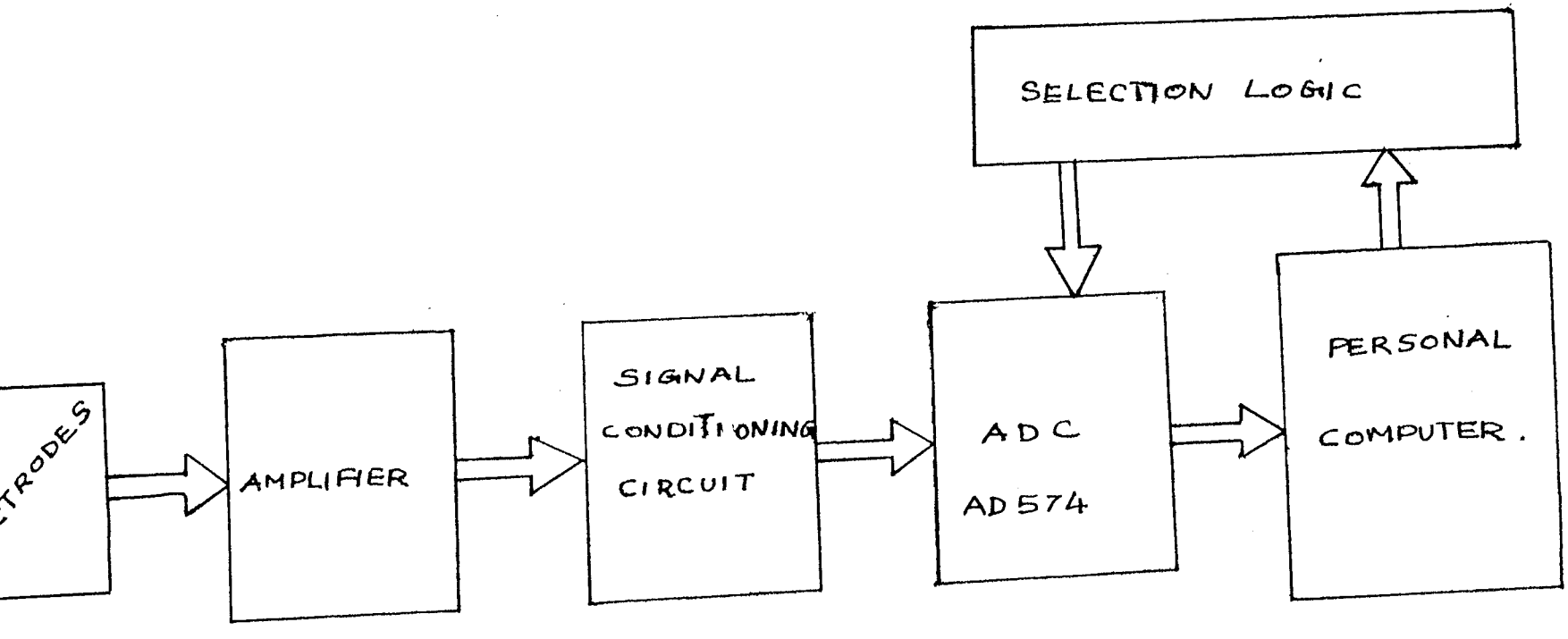


FIG. 1-1

CIRCUIT DESCRIPTION

Under this chapter, we shall be dealing with in depth design aspects of the circuitry of the various blocks mentioned in brief in the chapter system overview. The following discussion constitutes the requirements and the actual calculation of each.

2.1 ELECTRODES

A pair of electrodes are needed to convert the ionic potential in the body into equivalent electrical voltage.

The following points are to be considered while selecting the electrodes.

- Electrode offset voltage
- Contact impedance
- Artifacts
- Stability

The electrodes which we have chosen for the purpose of recording the bio-potentials generated by the heart are CLIP ON PLATE ELECTRODES which is of FLOATING type, with which the leads, which are reusable , are attached.

Although some disposable electrodes can be reuses several times , their cost is usually low enough that cleaning for reuse is not warranted. This electrode is used for the following reason :

- The possibility of slippage of electrode or movement is avoided
- They have a typically low contact of 2K ohm to 5K ohm.
- They have the lowest electrode offset potential . They do not get polarized when current is passed through them
- They are most stable.

2.2 POWER SUPPLY UNIT

This gives detailed description of various units of hardware which are meant for providing the necessary power supply to the various analog boards.

+ 12 Volt and -12 Volt Power Supply:

The components in the circuit are transformer, a full wave rectifier circuit with diodes, a voltage regulator, IC (7812), IC (7912) and necessary capacitors for filtering.

RANSFORMER:

A step down transformer is used for this purpose. The main voltage ust be reduced to a required value using a transformer which also isolates the emaining power supply block from the mains. The transformer which steps lown the 230 volt AC supply to 15-0-15 AC supply is used here, with current ating of 1 A.

FULL WAVE RECTIFIER:

The rectifier converts the alternating secondary current to an un- smoothed but unidirectional DC current. This function is performed by two or more diodes arranged in various configurations. The arrangement used in this project is a full wave rectifier circuit for dual polarity supply. We can get both + 15 Volts, -15 Volts from the transformer. These positive and negative voltages are rectified to produce a unidirectional +15 volts and -15 volts supply.

VOLTAGE REGULATOR:

Voltage regulator is a circuit that supplies the constant voltage regardless of changes in load current. Although voltage regulators can be designed using Op-Amps, it is quicker and easier to use IC voltage regulator. Further more IC voltage regulators are versatile and relatively inexpensive and are available with features such as programmable output current / voltage boosting, internal short circuit limiting, thermal shut down and floating operation for high voltage applications. In IC voltage regulators except switching regulators, all other types of regulators are called linear regulators.

DESIGN :

Vm = 15 volt (from transformer secondary).....(2.2.1)

substituting 2.2.1 in 2.2.2

Vdc = 2Vm / 3.14 = 0.636 Vm = 9.554 volts.....(2.2.2)

We know ,

Vdc = Vm - (Idc / 4 fC) ..... (2.2.3)

Idc = 1 Amps (transformer rated current).....(2.2.4)

rearranging 2.2.3 ,

C = Idc / (4f (Vm - Vdc)).

= 1 / (4 * 50 (15 - 9.554))

= 915.75 micro farad

Since the standard value available is 1000 microfarad , we are using this.

Vm = 12 Volt.....(2.2.5)

Vdc = 0.636 Vm.....(2.2.6)

substituting 2.2.5 in 2.2.6 ,

Vdc = 7.632 Volt

Idc =0.1 amps (from the regulator)

therefore the value of output capacitor ,

C = Idc / (4f * (Vm - Vdc))

$C = 0.1 / (4 * 50 * (12 - 7.632))$

$C = 114.47$ micro farad.

nce the std. value available is 100 micro farad , we have chosen it.

.3 ECG AMPLIFIER

The first stage of the ECG amplifier is the sensor which is used to ick the ionic potential from the body containing noises . This signal is given to the Instrumentation amplifier .The circuit diagram of the amplifier and filter circuitry developed is shown in fig 2.3.1. The objective is to remove base line drift , 50 Hz interference noise and high frequency interference while simultaneously minimizing distortion of the signal of interest . To obviate the possibility of electric shock , the electronics is designed to operate with a very low amperage of +12 battery system.

The problem of base line drift and electrochemical potentials can be alleviated with the help of suitably designed high pass filter. the design considerations require that the base line drift be eliminated while incurring insignificant distortion in the ECG signal . A good compromise is obtained with R1 = 300 K and C1 = 0.47 micro farad . The corner frequency of this filter is given by

$fc = 1 / (2 * 3.14 R1 * C)$ with $C = C1 / 2$.

With values already assigned , fc = 0.068 H z.

To amplify the signal a differential amplifier shown as in the figure is used . In addition to provide amplification , the amplifier does an excellent job of eliminating 50 Hz common mode interference because of high common mode rejection ratio of the operational amplifiers used for the design. Besides this a non - common mode 50 Hz interference associated with the signal is formidable. A high Q 50 Hz notch filter was designed to filter out this interference.

DESIGN OF ECG AMPLIFIER:

1. INSTRUMENTATION AMPLIFIER

We know ,

$$Vo = (1 + 2 R1 / R) Ro / R2 (V1 - V2)$$

A wide range of gains may be implemented merely by adjusting R .

Let , R1 = R2 = Ro = 22 K ohms

Substituting this value in the previous equation ,

$$20 = (1 + 2 * 22{,}000 / R) 22{,}000 / 22{,}000$$

Therefore R = 2.2 K ohms

VOLTAGE FOLLOWER

The gain is given by , $A = 1 + (Rf / R1)$

Since the gain of voltage follower is 1 and substituting it ,we get

$$1 = 1 + (Rf / R1)$$

i.e,

$$Rf / R1 = 0$$

Therefore $Rf = 0$.

3. HIGH PASS FILTER

Let ,

$$R1 = R3 = 750 \text{ K ohm}$$

For minimum dc offset ,

$$R2 = (R1 * R3) / (R1 + R3)$$

$$R2 = (750 \text{ K ohms} * 750 \text{ K ohms}) / (750 \text{ K ohms} + 750 \text{ K ohms})$$

$$R2 = 0.9 \text{ K ohms.}$$

Since the nearest value of resistance available is 1 K ohms , we are using it.

Now ,

$$R1 = b / (Wc * C)$$

where ,

b is the normalised coefficient.

Wc is the cutoff frequency

From table b / Wc = 0.35

Therefore C = 0.35 / (750 * 1000) = 0.47 micro farad.

4. LOWPASS FILTER

Let ,

R2 = 1 K ohm , R3 = 100 K ohm.

We know that ,

$$R1 = (R2 * R3) / (R2 + R3)$$

$$R1 = (1 * 100 * 1000) / (101 * 1000)$$

$$R1 = \underline{20 \text{ K ohms.}}$$

Now ,

$$R1 = 1 / (b * Wc * C)$$

$$R1 = 1 / (Wc * C) \quad \{ b = 1 \text{ for first order filter and } Wc = 106.7 \text{ Hz} \}$$

Therefore,

$$20 * 1000 = 1 / (106.7 * C)$$

$$C = \underline{0.47 \text{ micro farad}}.$$

5. NOTCH FILTER

Capacitance value is chosen arbitrarily , preferably near 10 micro farad .

Then the resistance's are as follows :

From the circuit ,

$$R1 = 1 / (2 * Q * Wd * C) = \underline{12 \text{ K ohms.}}$$

$$R2 = 2\,Q / (Wd * C) = 4.7\ K + 27\ K = \underline{31.7\ K\ ohms}$$

$$R3 = (R1 * R2)/(R1+R2) = (12K * 31.7K)/(12K+31.7K)$$

$$R3 = \underline{1.2\ K\ ohms}.$$

A TYPICAL ECG AMPLIFIER:

The most important consideration in ECG design is to provide amplification to the ECG signal without distorting it , and at the same time to minimize all unwanted artifacts.

Consider the table given below :

GAIN	1000
BAND WIDTH	0.05 TO 100 Hz
<u>INPUT IMPEDANCE</u>	
DIFFERENTIAL	> 2.5 M ohms
COMMON MODE	> 100 M ohms
CMRR	> 20,000
INPUT RISK CURRENT	< 10 micro amps
OVER VOLTAGE PROTECTION	< 5000 volts (Defibrillator Discharge)

It follows from the table that the ECG amplifier should have the following important features ,

- Specified high gain.
- Very high input impedance
- Rejection of common mode signals
- Good low frequency response

The amplifying component is usually , an operational amplifier which uses esistors and capacitors to form a complete amplifier circuit. OP - AMPS are used because of the following advantages :

- Infinite open loop gain
- Very high input impedance and negligible output impedance
- Stability throughout the range of operation
- Infinite CMRR
- Negligible dc offset
- Negligible noise , drift and other temperature related effects

Modern OP - AMPS exhibit close to ideal performance and therefore make the task of designing an ECG amplifier somewhat easy . The IC design permits us to build amplifiers using very few components and to attain a respectable performance with some degree of assurance.

.4 DESIGN OF ADC:

The choice of an ADC has been already mentioned. The commercially available 574 has been used in our circuitry which is a 12 – bit successive approximation type converter. Since our project involves multi channel selection, different channels can be selected by providing the required signal to ADDA, ADDB and ADDC. The negative reference Vg is shorted to ground which limits the maximum negative voltage. The positive reference voltage is directly connected to +Vcc which is +5volts for ADC, thus limiting the input variations from 0 to +5volts.

A 7805 is used for the purpose of +Vcc for ADC. The input to it is taken from the + Vcc of the chassis i.e., at + 15 volts output of + 5volts is then fed to the ADC as well as the clock as the Vcc. 74123 is used as a clock for the ADC. It is basically a Schmitt trigger NAND gate. The clock of 640 kHz is derived from this using a resistor and Capacitor at pins 2 and 3 as frequency selective components. The value is chosen for them are derived by the following formulae :

$$t = Rc \ln [Vp (Vdd - Vn) / Vn (Vdd - Vp)]$$

where,

Vp = Peak positive value of Hystersis voltage

Vn = Peak negative value of Hystersis voltage

Vdd = Supply voltage

This is eventually approximated at

$t = 2.52\ RC = 1 / f$

$f = 640$ KHz , therefore

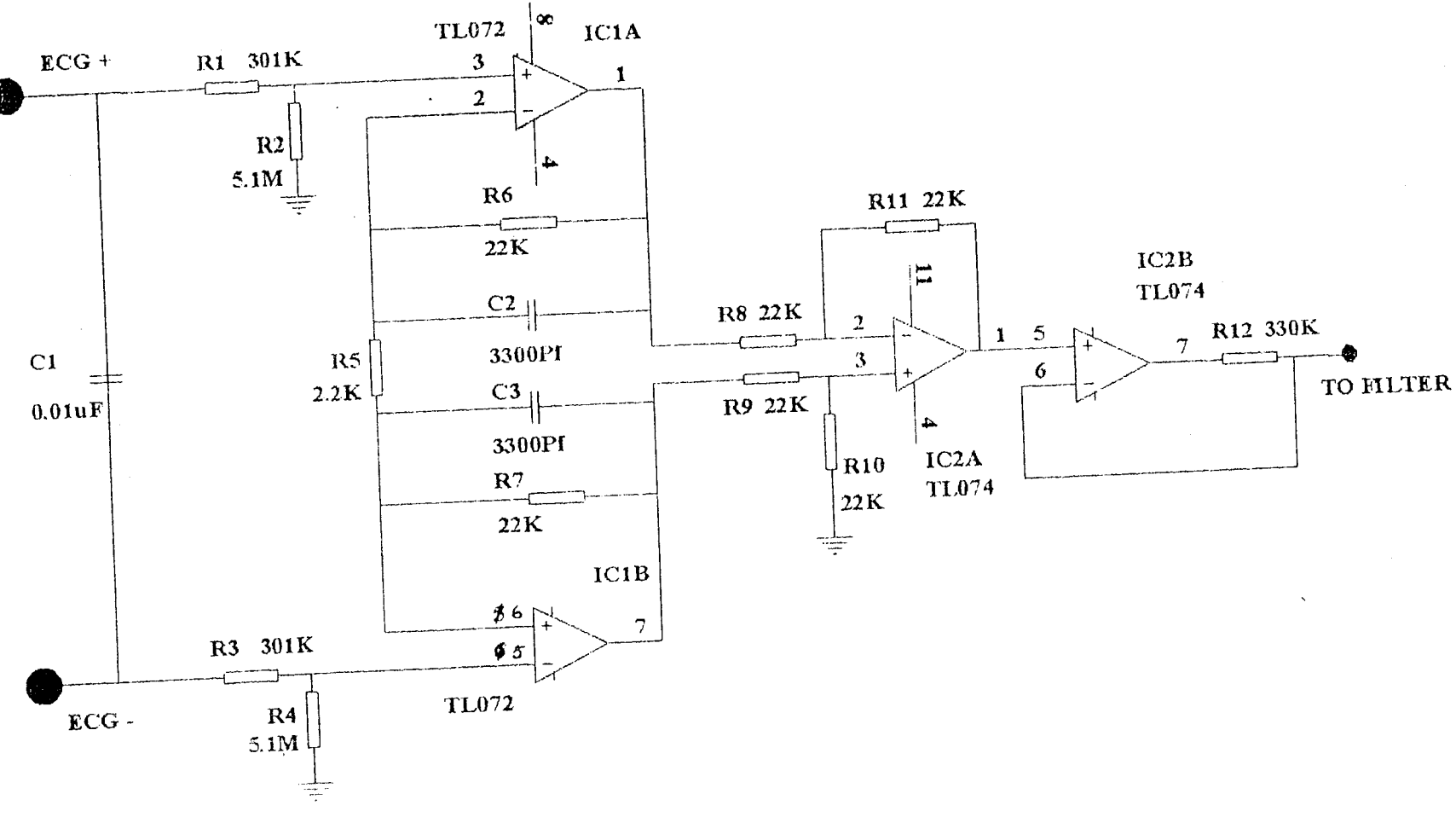
$t = 1 / 640$ KHz $= 1.5$ micro sec.

Taking $R = 22$ K , we get

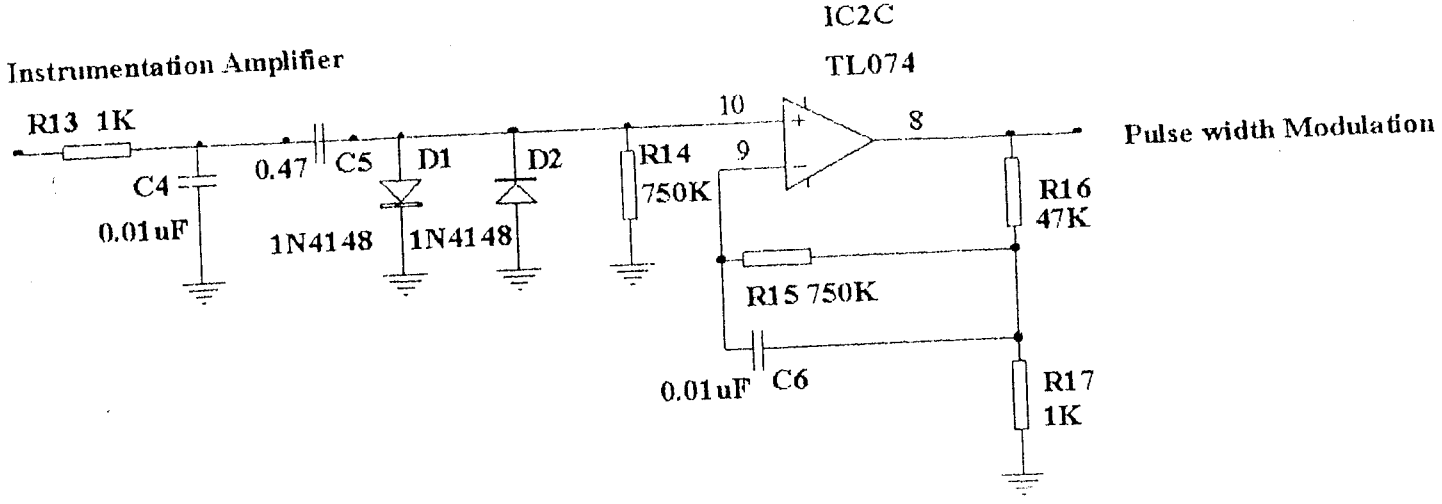
$C = 1.5 * 10 - 6 / 2.52 * 22 * 103 = 27$ pf.

The start of conversion signal for ADC is derived from computer through software using the output port.

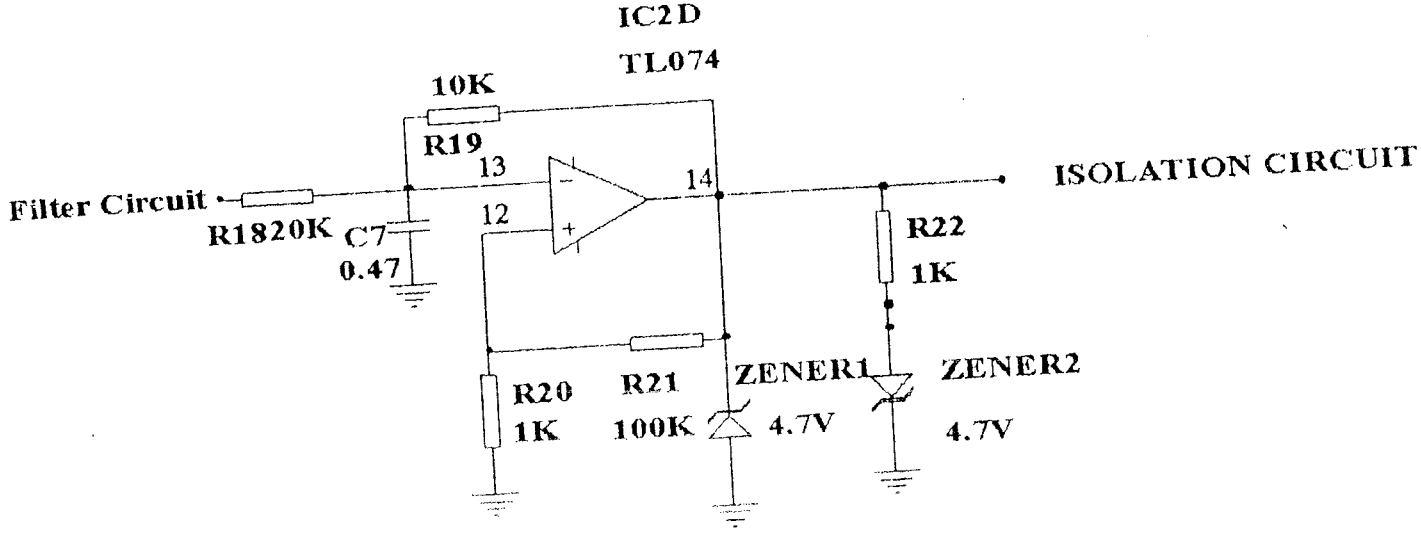
INSTRUMENTATION AMPLIFIER



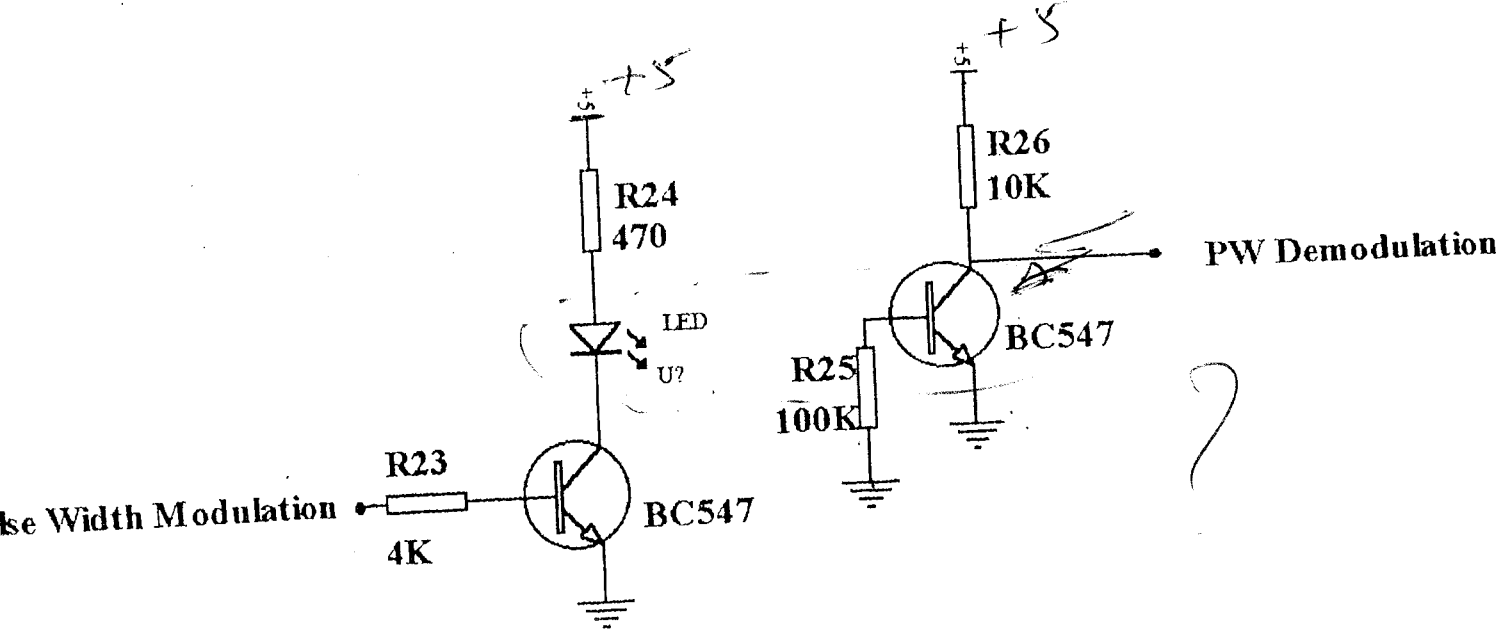
FILTER CIRCUIT



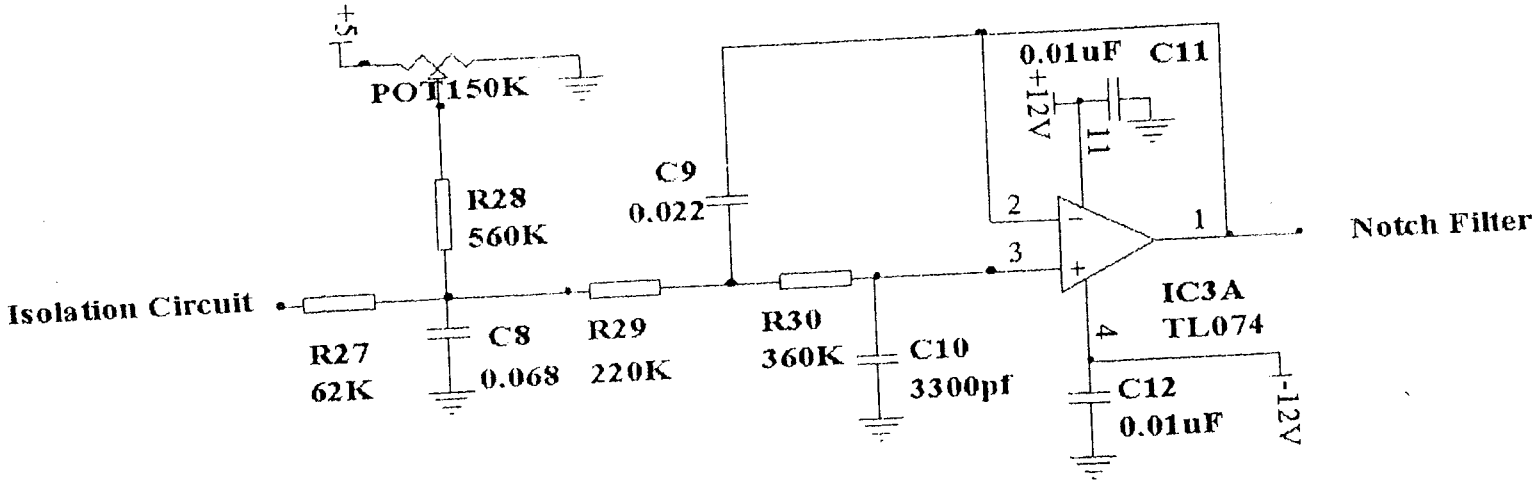
PULSE WIDTH MODULATION



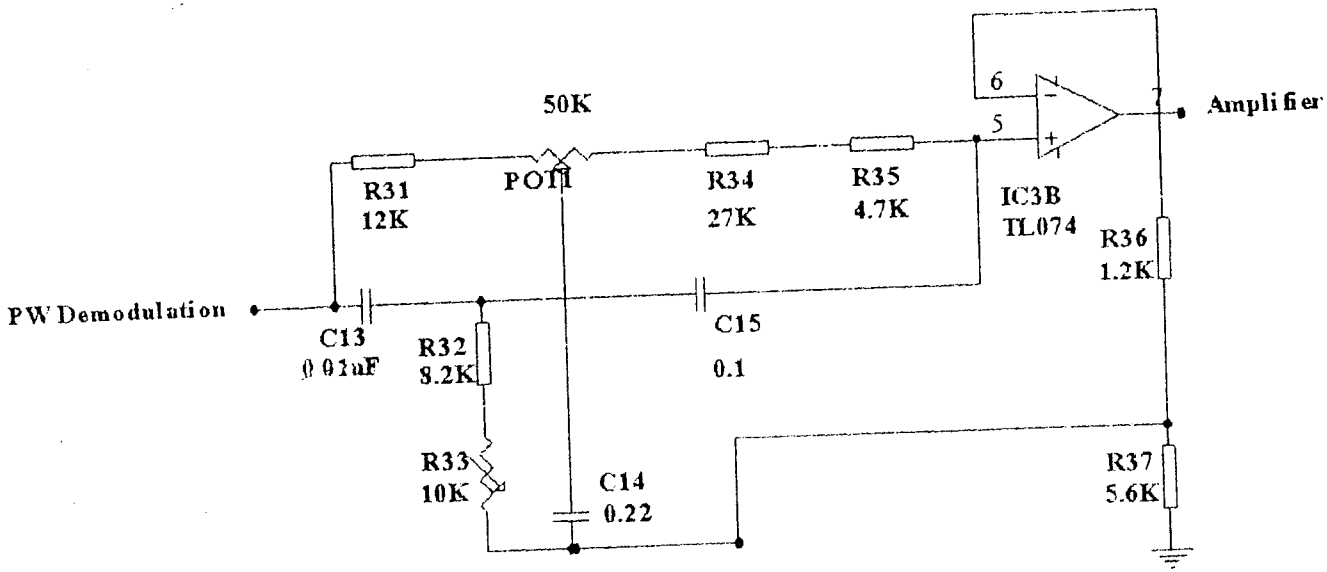
ISOLATION CIRCUIT

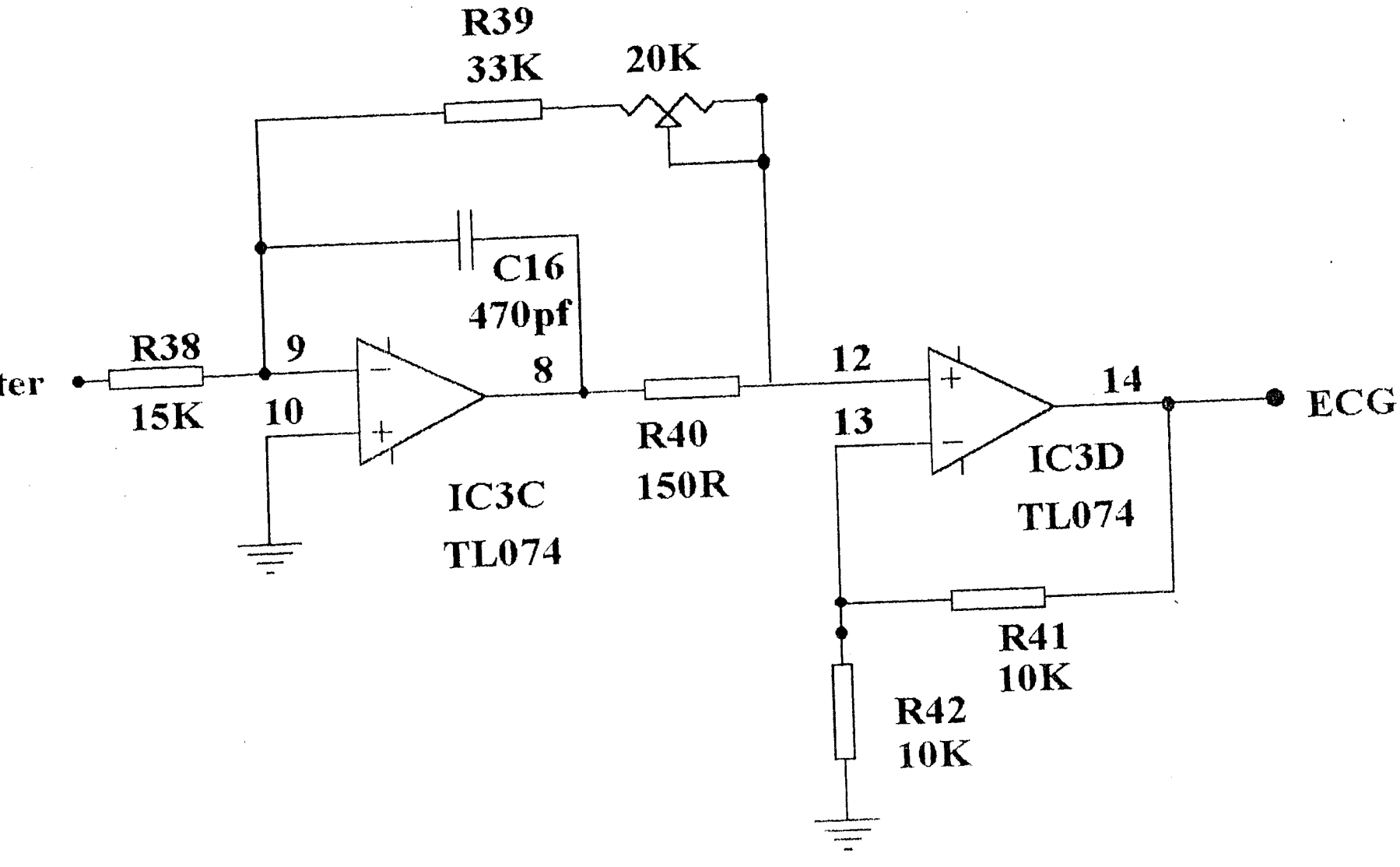


PW DEMODULATION



NOTCH FILTER




R39
33K
20K
C16
470pf
R38
15K
9
10
8
IC3C
TL074
R40
150R
12
13
14
IC3D
TL074
ECG
R41
10K
R42
10K

THE ELECTROCARDIOGRAM

The electrocardiogram is a reflection of the electrical activity of heart. The ECG is a quasi-periodically rhythmically repeating signal synchronized by the function of the heart , which acts as a generator of bio- electric events. The potentials originating in the individual fibres of the heart muscles are added to produce the ECG wave form. This generated signal can be described by means of a simple electric dipole consisting of a pair of a positive and negative charge. The dipole generates a field vector , changing nearly periodically in time and space and its effects are measured on the surface. Thus an ECG reflects the rhythmic electrical depolarization and repolarisation of the myocardium (heart muscle) associated with the contraction of the artria and venticles. The shape, time interval and amplitude of the ECG give the details of state of the heart.

Any form of arrythmia (disturbance in heart rhythm) can be easily diagnosed using the electrocardiogram. The heart is unique among the muscles of the body in that it possesses the property of automatic rhythmic contraction . The impulses necessary to maintain the pulsation , arise from a specified location interior to the heart . The heart beat is a spontaneous ,

periodic, electrical potential orginating in a small area of the heart muscle tissue , the sinoartrial node. The fundamental beat generated in a S.A node first travels through the heart muscle of artria , causing them to simultaneously contract. The electric wave then travel to the atrioventricular node which permits transmission of the contraction of muscle fibres through out the myocardium . The impulse formation and conduction also produces weak electric currents conducted to the body surface, from where this can be measured by connecting electrodes , because they travel through the body which is an infinite homogenous conductor . The ECG recorded as a differential sum of the outputs of the various electrodes placed at different location in the body.

3.1 ECG LEAD CONFIGURATIONS

To record an electrocardiogram , a number of electrodes, usually twelve are affixed to the body of the patient. These leads are placed in three standardized electrode position.

- Bipolar limb leads or standard leads
- Augmented unipolar limb leads
- chest leads or precordial leads

BIPOLAR LIMB LEADS

These consists of standard leads I , II and III. The three bipolar limp leads were first introduced by EINTHOVEN . In these , the potentials are tapped from four locations of the body:

a) Right arm (RA)

b) Left arm (LA)

c) Right leg (RL)

d) Left leg (LL)

Usually the right leg electrode acts as ground reference electrode . The lead positions are as follows,

Lead I : Left arm and Right arm

Lead II : Left leg and Right arm

Lead III: Left leg and Left arm

The closed path RA to LA to LL and back to RA is called the EINTHOVEN TRIANGLE . According to EINTHOVEN , in the frontal Plane of the body, the cardiac electric field vector is a two dimensional one . The ECG measured from any one of the three limb leads is a time variant single dimension component of the vector. Along the sides of this triangle , the three projections of the ECG vector are measured . Further the vector sum

of the projection in all the three sides is equal to zero. The relation between three leads is expressed algebraically by EINTHOVEN'S equation .

Lead II = Lead I + Lead III

This is based on the Kirchoff's law, which states that the algebraic sum of all the potential differences in a closed circuit is zero . If EINTHOVEN had reversed the polarity of lead II ,the three Bipolar lead axis would result in closed circuit and leads I + II + III ,would equals zero. However, since EINTHOVEN did make this alteration in the polarity of Lead II axis , the equation becomes I - II + III = 0 . Hence, II = I + III.

The electric potential that is recorded from any one extremity will be the same no matter where the electrode is placed . The electrodes are usually applied just above the wrists , and ankles.

AUGMENTED UNIPOLAR LIMB LEAD

In this system , introduced by Wilson the ECG is recorded between a single exploratory electrode , and the central terminal , which has a potential that is obtained by connecting the three active limb electrodes together through the resistor of simple value . In unipolar limb leads , one of the limb electrodes is used as exploratory electrode as well as contributing to the central terminal. This double use results in an ECG signal , that has a

very small amplitude . By means of augmented ECG lead connections , a small increase in the ECG voltage can be realized . The augmented lead connections are

- aVR - Augmented voltage Right arm
- aVL - Augmented voltage Left arm
- aVF - Augmented voltage foot

UNIPOLAR CHEST LEADS

In the case of unipolar chest leads the exploratory electrode is obtained from one of the chest electrode . The chest electrode are placed , on six different points of the chest , closed to the heart.These chest positions called the PRECORDIAL UNIPOLAR LEADS and are designated ,V1 to V6. All the three are active limb electrodes are used to obtain the central terminal ,while a separate chest electrode is used as an exploratory electrode.

The common precordial electrode position used are:

V1 : Fourth intercostal space at right sternal margin.

V2 : Fourth intercostal space at left sternal margin.

V3 : Midway between V2 and V4.

V4 : Fifth intercostal space in the Mid-calvicular line.

V5 : Anterior auxiliary line.

V6 : Mid auxiliary line.

3.2 COLOUR CODE

Normally, ECG potential are measured with colour coded leads, according to convention ,to facilitate easy identification . The placement of electrodes as well as the colour codes used to identify each electrode is shown in figure.

White -- Right arm

Black -- Left arm

Green -- Right leg

Red -- Left leg

Brown -- Chest

3.3 BI-POTENTIAL SENSORS

The most type of electrodes used for recording ECG are rectangular or circular surface electrodes . The material used is German silver,Nickel silver or Nickel plated steel. They are applied to the surface of the body with electrode jelly . The typical value of contact impedance of this electrodes of normal size is nearly 2 to 5 kohms, when measured at 10 Hz .

All types of bio-potential electrodes have a metal-electrolyte interface.

In each case , an electrode potential is developed across the interface proportional to the exchange of ions between the metal and electrolytes of an ion is given by Nernst equation ,

$$E = - (RT / NF) \ln [C1F1/ C2F2]$$

where,

R - Gas constant
T - Absolute Temperature
n - Valency of ion
F - Faraday constant (96500c)

C1,C2 - Two concentrations of the ion on the two sides of the membrane.

F1,F2 - Respective activity coefficients of the ion on the two sides of the membrane.

The measurement of bio electric potential require two electrodes . The voltage measured is really the difference of bio electric potential between the instantaneous potential of the two electrode . If the electrode are of the same type the output is the actual difference of ionic potential between the two points of the body . Mis-match of the two electrode results in an electrode offset voltage , often mistaken for a true physiological event . Also chemical activity within an electrode can cause fluctuation appearing as noise

on a bio-signal . It is found that Silver – Silver chloride electrode is very stable , so this is normally used for various application.

PURPOSE OF ELECTRODE JELLY

The dry out skin of the body is a highly non conductive and will not establish a good electrical contact with an electrode. So the area of contact should be coated with an electrically conductive paste called the electrode jelly. Thus the electrode jelly reduces the impedance of contact and also reduces the artifacts resulting from the movement of electrode or patient . Generally the conductivity of skin is directly proportional to the moisture of the skin . For example , the ECG electrode contact impedance on dry skin is about 100 K ohms and the equivalent capacitance is about 0.01 micro farad . After the application of electrode paste , the contact impedance is reduced to 10 K ohms and the capacitance is increased to 0.1 micro farad.

3.4 TYPICAL ELECTROCARDIOGRAM COMPLEX

Normal ECG comprise a regular sequence of P , QRS , and T wave segment as shown in figure . The P , QRS and T waves reflects the rhythmic electrical depolarisation and repolarisation of heart muscles. To the clinician , the shape and duration of each feature of the ECG are significant . The wave form however , depends greatly on the lead configuration used .

The physiological nature of ECG wave form is shown in the figure.

3.5 PRACTICAL CONSIDERATIONS OF ECG RECORDING

Several practical aspects must be observed in order to obtain a useful electrocardiogram.

ARTIFACTS

Since the ECG unit is a sensitive device , it can pick-up unwanted electrical signals which may modify the actual ECG. Therefore, the operator should check the following things before recording the ECG.

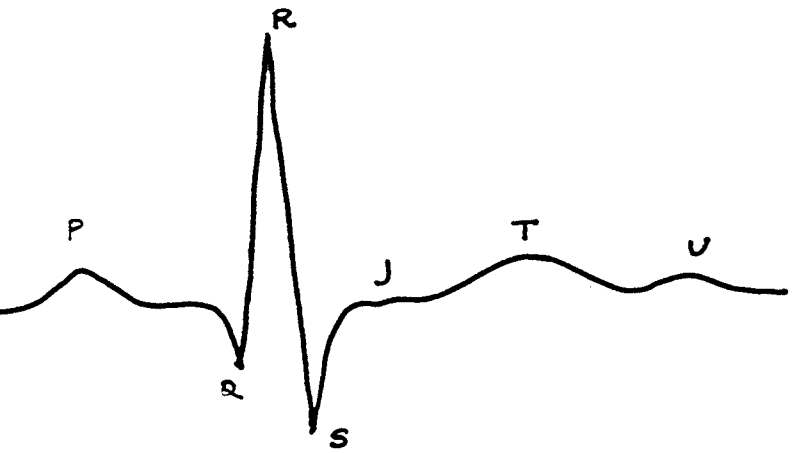
- Be sure the patient does not touch any metal object
- Remove any other electrical appliances in thr vicinity of the patient
- Make sure that all the electrodes have been applied, with the right amount of jelly and all electrode straps are tied
- Be sure that the patient is in comfortable and relaxed position. Otherwise, unsteady trace may be produced.

BASE LINE DRIFT

A wandering base line is usually due to the gross movements of patients or from mechanical strain on the electrode wires . This can be eliminated by insuring that the patient lies relaxed and the electrodes are properly placed.

The most critical component of the ECG recorder is the patient cable. Cables made of silicon - rubber are used to provide better elasticity over longer periods of time.

ECG WAVEFORM :



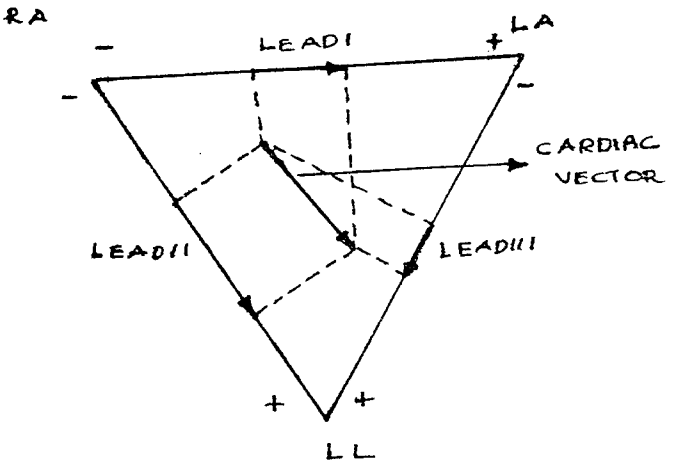
AMPLITUDE :

P	wave	0.25 mv.
R	wave	1.60 mv.
Q	wave	25% of R.
T	wave	0.1 to 0.5 mv.

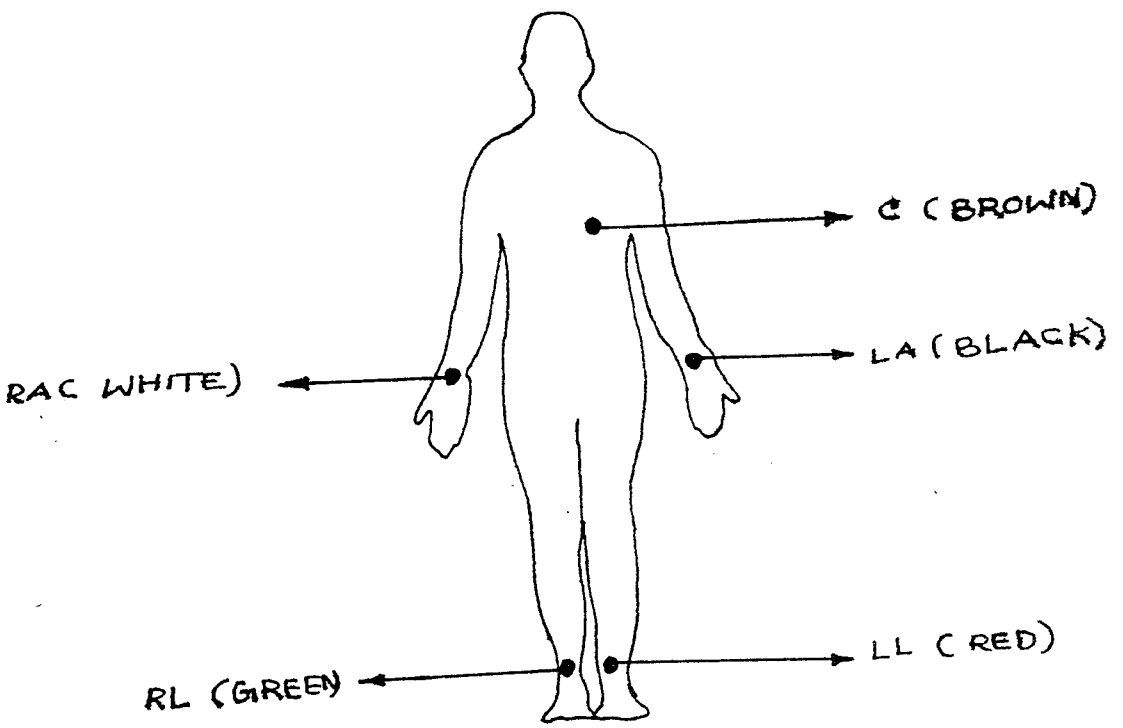
DURATION :

P-R	interval	0.12 to 0.20 sec.
Q-T	interval	0.35 to 0.44 sec.
S-T	segment	0.05 to 0.15 sec.
P	wave interval	0.11 sec.
QRS	interval	0.09 sec.

THE EINTHOVEN TRIANGLE:



ABBREVIATIONS AND COLOUR CODES:



SOFTWARE DEVELOPMENT

Software plays the crucial link by actively interacting the hardware and the PC. Hence this core part is required to be powerful enough to cater to our needs of waveform generation ,detection and analysis . These functions entailed a close interaction with the hardware and so the language chosen had to have the necessary facilities for this task. The C language with its powerful pointer facility chose itself for this purpose . The software has been designed to perform the following functions.

4.1 ADD ON CARD DESCRIPTION

Generally all the personal computers have ISA, ESIA and PCI slots to use add on cards. At present there is no ISA slots available, the ISA slots are modified and extended to handle more datas than ISA slot are called as EISA slots. Both the ISA and EISA slot will occupy more space in the PC mother board, the mother board manufacturers are trying to minimize the board size, so that they go for a compact slot with all the signals which are available in EISA slots.We are planning to use EISA slots for our application. For our application we need an ADC to convert our analog data into digital format.

The number of I/o slots varies in different PC models. The original IBM PC have five expansion slots. The IBM-XT have eight expansion slots. In all these cases the I/O slots follow the standards observed by the IBM. Using a SIP pull up resistor terminates the data bus. The resistor set/SIP pack is mounted prior to the last slot.

To design the add-on card with the selection facility we have to use an eight-bit comparator. One input of the comparator is given to the address bus of the PC another one is given to the DIP switches, with the help of the DIP switches the address can be selected. After the comparator is selected with

the desired address, the comparator output will enable the decoder. The decoder in our design will be three to eight decoders. After enabling this three to eight decoder the three inputs from the address bus is given to the decoder. Depends on the decoder input eight outputs will be selected. The input is A, B and C, when all the inputs are in '0' state the output Y0 will be selected. Then depends on the input binary signal the output will be selected from Y0 to Y7. These Y0 to Y7 outputs are connected to the chip enable (CE) pins of the ADC.

INTERFACING CIRCUIT:

This block is used to interface the analog signals and the digital pulses with the computer. The main parts of an interfacing circuit are analog to digital converter, digital to analog converter and peripheral interface. It also has buffers, comparators, decoders, and latches. It is also called as I/O card or ADD-ON card. The comparator is used for fixing the base address. The are usually used for amplifying current or power. Here we are using bi-directional buffers for data bus and unidirectional buses for the address bus. The decoder is used to select the desired part of the ADD-ON card for proper working by the help of address bus. The latches are used as chip select to which is not available in certain I.Cs. The signal from the ADC is given to the

personal computer(P.C) and the signal is processed in the CPU of the P.C .

PERSONAL COMPUTER:

The personal computer is the controller part of our project. It has the controller algorithm. The algorithm is developed in "C" language. The interfacing circuit i.e. the ADD-ON card is connected in the expansion slots of the computer. The setpoint is given to the P.C. The controller algorithm gives out the proper control action and is given to the final control element.

4.2 COMPUTER INTERFACING TECHNIQUE :

FEATURES OF COMPUTER INTERFACING:

The personal computer has taken up prominent place in the lab as well as office. A variety of plug-in cards are available which can convert a PC into a digital storage oscilloscope, data acquisition system of an instrument controlled.

The large verity of plug-ins, add-ons and external equipment's force the user to look a little carefully into hardware and software interfacing of various peripherals to a PC. The open architecture of the IBM PC has helped its 62 pin and 10 channel bus in becoming a universally accepted interface standard, for joining an extra hardware to a PC. A peripheral in the strict

sense is a piece of equipment which itself is a generate entity and gets attached to the PC through the specific connection protocol called interface standard. All the socket originate from printed circuit cards, which share a connection bus called I/O channel bus and sometimes PC bus -a name given to the set of signals available on 62 pin edge connectors on the PC motherboard.

PERIPHERAL INTERFACES:

The data transfer by and large involves a series of 8 bit bytes or given wider to be transferred over a set of physical wires or optical fiber. The data transfer may take place in bit serial or bit parallel word form. The serial transfer requires a less number of physical interconnection as compared to the parallel, and the user is tempted to choose it for the sake of sheer simplicity. However the speed of transfer is degraded by a factor of eight, which may be alternating factor for quiet a few cases.

PARALLEL INTERFACE:

Since speed should be frequently monitored in outline we go for this parallel communication. The use of 8 individual wires for each of the data lines obviously increases the data transfer rate, for similar line by a factor of eight. The bundle of wires get quiet thick and parallel interface is therefore used in those cases where data transfer rate is the main consideration.

The different types of parallel interface is given :

The I/O Card is inserted in one of the motherboard slots.

I/O slot signals:

The number of I/O slot vary in different PC model. The IBM PC has free expansion connection. The IBM PC XT's have eight expansion slots. In all these cases, the I/O slot follow the standard observed by IBM. The data bus is terminated using SIP (single in package) registers. The register set/SIP pack is mounted prior to the last slot.

I/O card:

This is inserted into one of the slots of motherboard. The IC's used in I/O cards are:

- Programmable Peripheral Interface
- ADC
- 8bit negative components
- 3 to 8 decoder

4.3 HARDWARE:

Hardware is nothing but an ADD-ON card, which is slotted into the expansion of the PC motherboard.

EXPANSION SLOTS:

The PC's expansion slots are provided for connecting ADD-ON boards to expand the system by the peripherals. For example: display adapter card, floppy disc controller card, serial / parallel port adapter card etc are connected to the mother board through the I/O slots for providing communication path between ADD-ON cards and CPU.

The pin diagram of the expansion slot shows that there are 62 pins and they are grouped into two namely, slot A and slot B. In side, A address and data signals are provided and in side B control signals are provided. All I/O slots are connected in parallel; that is some signals are available in I/O slots.

EXPANSION SLOT SIGNALS :

Address Bus(A0-A10):

The address bus signals are available at these pins. These signals are unidirectional coming from the motherboard to the ADD-ON card. These signals are generated either by CPU or by DMA controller. For normal operation these signals must be pulsing always.

Data Bus(D0-D17):

The data bus signals of the motherboard are available at these pins. These signals are bi-directional. The CPU for reading or writing data from memory or I/O ports uses the data bus. For normal operation these signals should be pulsing.

Control Bus:

MEMW:

These signals indicate the process of memory operation. The CPU or the DMA controller generates this signal. Memory uses these signals for storing the data available in the bus in the location specified by the address available in the address bus. For normal operation these signals should be pulsing.

MEMR:

These signals indicate the process of memory read operation. This signal is generated either by CPU or by DMA controller. When this signal is low, memory is on the address bus. For normal operation the signal should be pulsing.

I/O Read:

The signal indicates the selected input port to send data to the data bus. The signal is generated either by the CPU or by the DMA controller. For normal operation the signals should be pulsing.

I/O Write:

This signal indicates the selected output port to take data from the data bus. This signal is generated either by the CPU or by the DMA controller. For normal operation the signals should be pulsing.

Address Latch Enable(ALE):

This signal is generated by in the motherboard to latch address from CPU. This signal is provided at the I/O port to indicate the CPU bus cycle. For normal operation the signal should be pulsing.

Clock signal:

Oscillator:

This 14.318 MHz signal is available at this pin. The signal is produced in the CPU card. The duty cycle of this signal is 50%. For normal operation the signal should be pulsing.

Clock:

The 4.77 MHz signal generated is available at this pin. The CPU uses this signal as its clock input. The duty signal of this signal is 33%. For normal operation the signal should be pulsing.

Interrupt Signal:

IRQ 2:

This signal is not used in PC's.

IRQ 3:

The first serial port COM 1 raises this signal. This signal should be pulsing during COM 1 operation.

IRQ 4:

This signal is the interrupt raised by second serial port COM 2. The signal should be during COM 2 operation.

IRQ 5:

This signal is the interrupt raised by hard disk controller. The signal should be pulsing for hard disk operation.

IRQ 6:

This signal is the interrupt raised by the floppy disk controller. The signal should be pulsing for floppy disk controller.

IRQ 7:

This signal is the interrupt raised by pointer controller as a request for data transfer. This signal should be pulsing during printer operation.

DMA signals:

DACK 0 (DMA acknowledge):

This is the DMA acknowledgement signal for DRQ 0 request for DRAM refresh.

DEQ 1(DMA request):

This signal is not used in PC.

DACK ! (DMA request):

This signal is not used in PC.

DRQ 2:

Floppy disk controller for every byte of data transferred generates this signal. This signal should be pulsing for floppy disk operation. This is related to IRQ 6 signal.

DACK 2:

This is an acknowledge signal from DMA controller in response to the request made by the floppy disk controller. This signal should be pulsing for normal floppy disk operation.

DRQ 3:

This signal is generated by the hard disk controller for every byte transfer to request the DMA that a data transfer is required. This signal should be pulsing during hard disk operation. This signal is related to IRQ 5 signal.

DACK 3:

This is an acknowledge signal from the DMA controller in response to the request made by hard disk controller. This signal should be pulsing during hard disk operation.

AEN:

This signal is generated by the mother board when HOLD signal is given by controller. When AEN is high it means that DMA controller has been given control of the bus. AT this time the address, 'date and control signals are generated by DMA controller. For normal operation the signal should be pulsing.

Terminal Count:

At the end of every DMA operation an EOP signal is generated by DMA controller. T/c signal is generated in the motherboard using EOP signal. This pulse indicated the DMA operation for one of the active DMA channels is completed, i.e. count had become zero.

POWER:

GND,+5v,-5v,+12v & -12v; we get it from SMPS. These voltages are used by ADD-ON card connected in I/O slot.

OTHERSIGNALS:

Reset DRV:

This signal is generated by clock generator during manual reset or power on reset. This is used by all ADD-ON cards connected in the I/O slot to rest or initialize their internal circuit when the system is reset.

I/O Channel Check:

This signal is made low when RAM parity error is detected by a memory board in the I/O slot. The signal is used to generate NMI interrupt to the CPU to indicate a parity error.

I/O Channel Ready:

This signal made low by the slow I/O device to make the CPU to introduce WAIT state. Whenever the signal is low, the CPU will not perform any bus operation.

The slot configuration of expansion slot are:

Slot No.			
	A2-A9	-	Data line
	A11	-	AEN
	A28	-	A3
	A29	-	A2
	A30	-	A0
	A31	-	A1
	B31	-	GND
	B2	-	RST
	B3 & 29	-	Vcc
	B13	-	WR
	B14	-	RD
	B22-B27	-	A9-A4

BUFFER:

The buffer is login circuit which amplifies the current or power. It has one i/p line and one o/p line. The login level of is same as that of i/p, logic 1 input provides to give 1 output.

The buffer is primarily used to increase the driving capacity of login circuit. The buffer is used to increase the driving capacity of data bus and address bus.

Tristate Buffer:

Tristate logic device has 3 logic states: logic 0, logic 1 and high impedance state. The term Tristate is trademark of natural semiconductor and used to represent 3 logic states. A tristate device has a third line called enable. When this is activated, the tristate device function the same way as the logic device. When the third line is disabled, the login device goes into high impedance state.

HARDWARE OPERATIONS:

Base Address Switching:

The base address is set by jumpers available at hardware PCB.

Address Comparison:

The base address is compared with DC addressing using comparator. If they are equal, a drive signal is given to decoder.

Control Flow from CPU :

At once the drive arrives, the decoder is fed with PC Bus signal. The o/p of PAL is enabled or disabled as per software.

Chip Selection:

The chip select signal from decoder selects any one of both 8255A as per software and connects to the bi-directional buffer control signal from PC bus is given to the through unidirectional buffer.

Double Hand Shake Data Transfer:

When more co-ordination is required between the sending system and the receiving system, a double handshake data transfer method is used. In this the sending device asserts its STB line low to ask' Are you ready'. The receiving systems raises its ACK line to say 'I am ready'. The peripheral device then sends the byte of data and raises its STB line high to say' Here is same valid data for you'. After it has read in the data the receiving system drops it. ACK line is low to say, 'I have the data, thank you and I wait your request to send the next byte of data. The STB or ACK signals for these handshake transfer can be produced on a port pin by instruction in the program. The port devices have been designed so that they can be programmed to automatically manage the handshake operation.

4.4 PROGRAM

ALGORITHM

1. Start
2. Display 'KCT' and ECG Monitor
3. Draw reference line. Initiate starting pixel
4. Read the value from port 304 & 305
5. combine the port outputs.
6. Compute the next pixel position using ADC output as

   Y=((4000-out)/75)+100;
7. Draw a line between there points
8. Repeat the steps from 4 to 7 1000 time to get 1000 page display
9. End of the program.

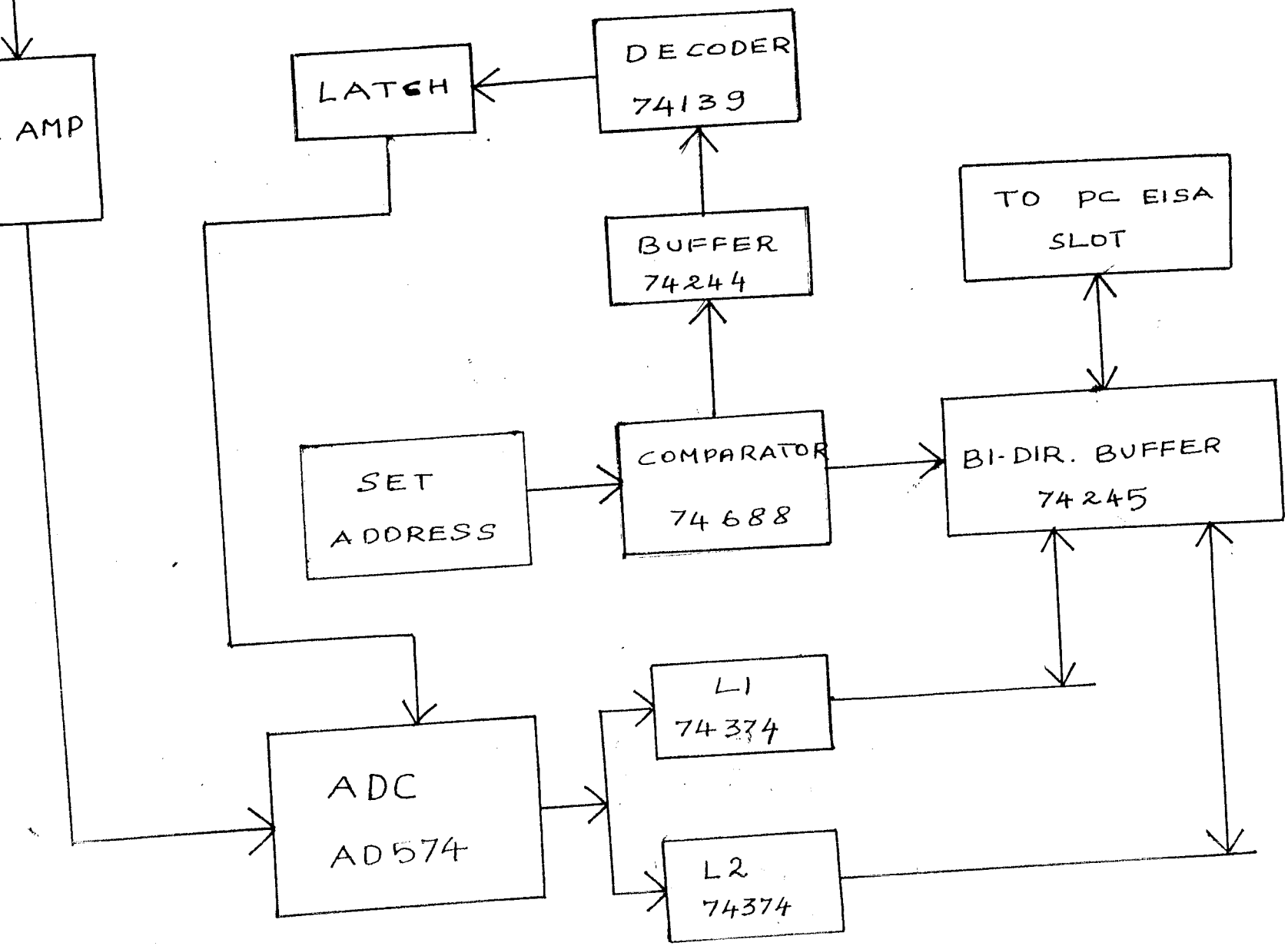
```
lude<graphics.h>
lude<conio.h>
lude<dos.h>
lude<stdio.h>
()

t gd=DETECT,gm,i,y,x1=0,x2=0,y1=200,y2=200;
t hi,hh,k;
ng out;
itgraph(&gd,&gm,"");
ar name[50]="KUMARAGURU COLLEGE OF TECH.";
ar title[50]="  ECG ANALYSER";
etch();
etch();
or(k=0;k<=1000;k++)

leardevice();
ettextstyle(TRIPLEX_FONT,HORIZ_DIR,3);
uttextxy(100,10,name);
ettextstyle(TRIPLEX_FONT,HORIZ_DIR,2);
uttextxy(100,50,title);
2=0;y1=200;y2=200;x1=0;
ine(0,300,680,300);
or(i=0;i<=680;i++)

=i+2;
utport(0x307,0x00);
elay(10);
i=inport(0x304);
h=inport(0x305);
ut=((hh<<8&0xf00)|hi)&0x0fff;
  printf("\n%d",out);*/
=((4000-out)/75)+100;
2=i;
2=y;
 putpixel(i,y,7);*/
ine(x1,y1,x2,y2);
1=i-1;
1=y2;
delay(10);
  } }

  for(i=50;i<350;i++)
{
 setcolor(m);
 circle(i,250,50);
 outtextxy(i,230,"HELLO!");
 m=m+1;
 cleardevice();
 }       */
getch();
closegraph();
return 0;
```



BLOCK DIAGRAM

MERITS OF THE SYSTEM

Such a system when developed , is bound to have various advantages over conventional ones . This is due to the effective utilization which the PC facilities . Few of the merits of our system may be enumerated as follows.

5.1. ECONOMIC CRITERION

This is the most important aspect of our system . It is so because, though expensive equipment specifically for the purpose of ECG are available commercially , the use of PC reduces the cost of the same effectively . The system becomes an additional facility for the users .

5.2 SIMPLE RELIABLE

The reliability obtained with the inherent accuracy of the computer adds with its simplicity as a result of its wide spread use in today's life is of high degree.

5.3 FLEXIBILITY

The system developed of its high level of flexibility since same PC may also utilized for enormous purpose , apart from its specific use.

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5.3 FLEXIBILITY

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5.4 NO EXPERTISE RECQUIRED

Another important aspect of the system is that the user need not to be a physician necessarily, but can also be the patient himself . It can be accessed by any person who is conversant with the use of PC.

5.5 CENTRAL MONITORING

The PC may also be interfaced to the main computer center in any hospital through modems so that the doctor can diagnose the same .

5.6 MULTIPLE PATIENT MONITORING

In our system the ECG of two patients can be obtained on a single PC, thus saving the time of physician . we can select any particular lead of the patients as required by the physician .

APPLICATIONS

a) It can be used for arrhythmia monitor

b) It can be used during heart surgery

c) It can be used in intensive unit.

d) It can be used to reveal the condition of the heart.

FUTURE DEVELOPMENT

Our system , the PC based cardiac monitor is highly versatile and expandable . Though our system holds a lot of promise , the areas were future development could help in modifying the present system are

7.1 DIGITAL SIGNAL PROCESSING

Digital filters can be incorperated instead of active filters. This would help in harmonic analysis of the individual segments of the ECG signal .

7.2 PHOTO CARDIOGRAM

Relatively new technique were in only the echo from the heart are sensed , converted into electrical signals and transmitted serially over telephone lines . Analysis is done at a central monitoring unit.

7.3 MULTICHANNEL MONITORING

This system can be expanded to monitor all 12- leads commonly used .

7.4 MULTI-PATIENT MONITORING

The number of patients monitoring on thePC can be expanded by using proper multiplexing circuitry and suitable alterations in the software program.

7.5 BIO-TELEMETRY

An important technique which can be used in ambulatory patient monitoring helps to analyse the heart conditions during normal day to day activities.

7.6 COUNTERACTING THE ALARMS

External circuitry can be activated using the computer to cater to various alarm conditions.

CONCLUSION

A new method for monitoring multiple patient ECG is presented in this report . The emphasis of the work has been on the development of the associated hardware . Filtering and amplifying circuitry is designed to extract ECG signals and it is shown that the citcuitry designed does not cause any significant distortion .

The usage of high speed computer offers flexibility in selecting patients and leads , and also for displaying the leads of any patient continously . This system can be expanded to any number of patients by using a analog to digital converter . Though the software written is only for reading and displaying it can be extended for the identification of life threatening arrythmias based on RR intervals as well as morphology of the ECG depending on the inter sample interval.

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ANALOG DEVICES

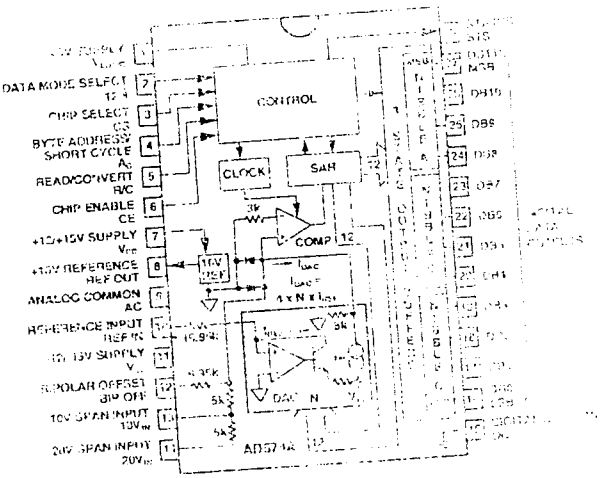
Complete 12-Bit A/D Converter

AD574A*

FEATURES

- Complete 12-Bit A/D Converter with Reference and Clock
- 8- and 16-Bit Microprocessor Bus Interface
- Guaranteed Linearity Over Temperature
  - 0°C to +70°C – AD574AJ, K, L
  - –55°C to +125°C – AD574AS, T, U
- No Missing Codes Over Temperature
- 35 µs Maximum Conversion Time
- Buried Zener Reference for Long-Term Stability and Low Gain T.C. 10 ppm/°C max AD574AL
  12.5 ppm/°C max AD574AU
- Ceramic DIP, Plastic DIP or PLCC Package
- Available in Higher Speed, Pinout-Compatible Versions (15 µs AD674B, 80 µs AD774B; 10 µs (with SHA) AD1674)
- Available in Versions Compliant with MIL-STD-883 and JAN QPL

BLOCK DIAGRAM AND PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD574A is a complete 12-bit successive-approximation analog-to-digital converter with 3-state output buffer circuitry for direct interface to an 8- or 16-bit microprocessor bus. A high precision voltage reference and clock are included on-chip, and the circuit guarantees full-rated performance without external circuitry or clock signals.

The AD574A design is implemented using Analog Devices' Bipolar/I^2L process, and integrates all analog and digital functions on one chip. Offset, linearity and scaling errors are minimized by active laser-trimming of thin-film resistors at the wafer stage. The voltage reference uses an implanted buried Zener for low noise and low drift. On the digital side, I^2L logic is used for the successive-approximation register, control circuitry and 3-state output buffers.

The AD574A is available in six different grades. The AD574AJ, K, and L grades are specified for operation over the 0°C to +70°C temperature range. The AD574AS, T, and U are specified for the –55°C to +125°C range. All grades are available in a 28-pin hermetically-sealed ceramic DIP. Also, the J, K, and L grades are available in a 28-pin plastic DIP and PLCC, and the J and K grades are available in ceramic LCC.

The S, T, and U grades in ceramic DIP or LCC are available with optional processing to MIL-STD-883C Class B; the T and U grades are available as JAN QPL. The Analog Devices' Military Products Databook should be consulted for details on /883B testing of the AD574A.

PRODUCT HIGHLIGHTS

1. The AD574A interfaces to most 8- or 16-bit microprocessors. Multiple-mode three-state output buffers connect directly to the data bus while the read and convert commands are taken from the control bus. The 12 bits of output data can be read either as one 12-bit word or as two 8-bit bytes (one with 8 data bits, the other with 4 data bits and 4 trailing zeros).
2. The precision, laser-trimmed scaling and bipolar offset resistors provide four calibrated ranges: 0 volts to +10 volts and 0 volts to +20 volts unipolar, –5 volts to +5 volts and –10 volts to +10 volts bipolar. Typical bipolar offset and full-scale calibration errors of ±0.1% can be trimmed to zero with one external component each.
3. The internal buried Zener reference is trimmed to 10.00 volts with 0.2% maximum error and 15 ppm/°C typical T.C. The reference is available externally and it can drive up to 1.5 mA beyond the requirements of the reference and bipolar offset resistors.
4. AD674B (15 µs) and AD774B (8 µs) provide higher speed, pin compatibility; AD1674 (10 µs) includes on-chip Sample-Hold Amplifier (SHA).

*Protected by U.S. Patent Nos. 3,803,590; 4,213,806; 4,511,413; RE 28,633.

REV. B

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Tel: 617/329-4700
Fax: 617/326-8703

74A–SPECIFICATIONS (@ +25°C with V_{CC} = +15 V or +12 V, V_{LOGIC} = +5 V, V_{EE} = –15 V or –12 V unless otherwise noted)

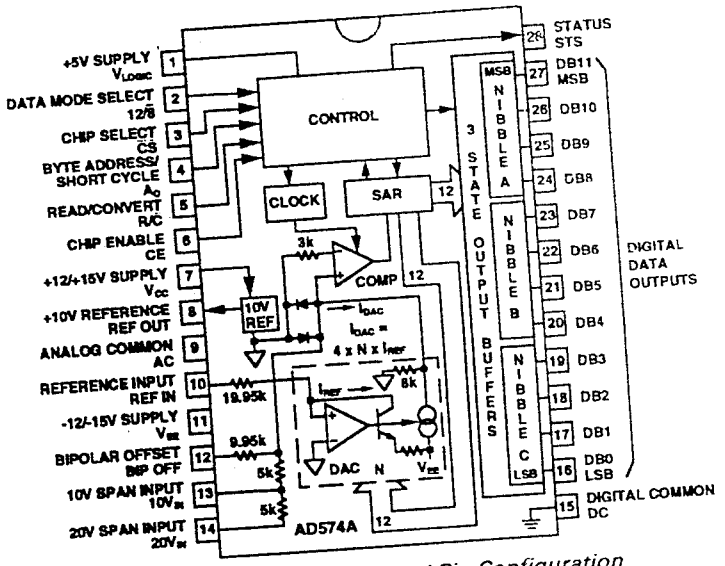
	AD574AJ			AD574AK			AD574AL			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
			12			12			12	Bits
TION			±1			±1/2			±1/2	LSB
TY ERROR @ +25°C			±1			±1/2			±1/2	LSB
T_{MAX}										
ENTIAL LINEARITY ERROR num Resolution for Which No g Codes are Guaranteed)	11			12			12			Bits
$_{N}$ to T_{MAX}			±2			1			1	LSB
LAR OFFSET (Adjustable to Zero)			±4			1			1	LSB
R OFFSET (Adjustable to Zero)										
SCALE CALIBRATION ERROR Fixed 50 Ω Resistor from REF OUT to REF IN) ustable to Zero)			0.25			0.25			0.25	%
	0		+70	0		+70	0		+70	°C
ERATURE RANGE										
ERATURE COEFFICIENTS ng Internal Reference) $_{MIN}$ to T_{MAX} Unipolar Offset Bipolar Offset Full-Scale Calibration			±2 (10) ±2 (10) ±9 (50)			±1 (5) ±1 (5) ±5 (27)			±1 (5) ±1 (5) ±5 (27)	ppm/°C LSB LSB LSB
ER SUPPLY REJECTION x Change in Full-Scale Calibration V_{CC} = 15 V ± 1.5 V or 12 V ± 0.6 V V_{LOGIC} = 5 V ± 0.5 V V_{EE} = –15 V ± 1.5 V or –12 V ± 0.6 V			±2 ±1/2 ±2			±1 ±1/2 ±1			±1 ±1/2 ±1	LSB LSB LSB
LOG INPUT put Ranges Bipolar Unipolar nput Impedance 10 Volt Span 20 Volt Span	–5 –10 0 0 3 6	5 10	+5 +10 +10 +20 — 7 14	–5 –10 0 0 3 6	5 10	+5 +10 +10 +20 7 11	–5 –10 0 0 3 6	5 10	+5 +10 +10 +20 7 11	Volts Volts Volts Volts kΩ kΩ
GITAL CHARACTERISTICS[1] (T_{MIN}–T_{MAX}) nputs[2] (CE, $\overline{CS}$, R/$\overline{C}$, A_0) Logic "1" Voltage Logic "0" Voltage Current Capacitance Output (DB11–DB0, STS) Logic "1" Voltage (I_{SOURCE} ≤ 500 µA) Logic "0" Voltage (I_{SINK} ≤ 1.6 mA) Leakage (DB11–DB0, High-Z State) Capacitance	+2.0 –0.5 –20 +2.4 –20	5 5	+5.5 +0.8 +20 +0.4 +20	+2.0 –0.5 20 +2.4 –20	5 5	+5.5 +0.8 +20 +0.4 +20	+2.0 0.5 20 +2.4 20	5 5	+5.5 +0.8 +20 +0.4 +20	Volts Volts µA pF Volts Volts µA pF
OWER SUPPLIES Operating Range V_{LOGIC} V_{CC} V_{EE} Operating Current I_{LOGIC} I_{CC} I_{EE}	+4.5 +11.4 –11.4 30 2 18		+5.5 +16.5 –16.5 40 5 30	+4.5 +11.4 –11.4 30 2 18		+5.5 +16.5 –16.5 40 5 30	+4.5 +11.4 –11.4 30 2 18		+5.5 +16.5 –16.5 40 5 30	Volts Volts Volts mA mA mA
POWER DISSIPATION		390	725		390	725		390	725	mW
INTERNAL REFERENCE VOLTAGE Output Current (Available for External Loads)[3] (External Load Should not Change During Conversion)	9.98	10.0	10.02 1.5	9.99	10.0	10.02 1.5	9.99	10.0	10.01 1.5	Volts mA
PACKAGE OPTIONS[4] Ceramic (D-28) Plastic (N-28) PLCC (P-28A) LCC (E-28A)		AD574ASD AD574AJN AD574AJP AD574AJE			AD574AKD AD574AKN AD574AKP AD574AKE			AD574ALD AD574ALN AD574ALP AD574ALE		

NOTES
[1]Detailed Timing Specifications appear in the Timing Section.
[2]12/8 Input is not TTL-compatible and must be hard wired to V_{LOGIC} or Digital Common.
[3]The reference should be buffered for operation on ± 12 V supplies.
[4]D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier.

Specifications subject to change without notice.

	AD574AS			AD574AT			AD574AU			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
ION			12			12			12	Bits
Y ERROR @ +25°C			±1			±1/2			±1/2	LSB
T_{MAX}			±1			±1			±1	LSB
NTIAL LINEARITY ERROR m Resolution for Which No Codes are Guaranteed)	11			12			12			Bits
to T_{MAX}			±2			±1			±1	LSB
AR OFFSET (Adjustable to Zero)			±4			±4			±2	LSB
OFFSET (Adjustable to Zero)										
CALE CALIBRATION ERROR ixed 50 Ω Resistor from REF OUT to REF IN) able to Zero)			0.25			0.25			0.125	% of FS
RATURE RANGE	-55		+125	-55		+125	-55		+125	°C
RATURE COEFFICIENTS Internal Reference) N to T_{MAX}) Unipolar Offset Bipolar Offset Full-Scale Calibration			±2 (5) ±4 (10) ±20 (50)			±1 (2.5) ±2 (5) ±10 (25)			±1 (2.5) ±1 (2.5) ±5 (12.5)	LSB (ppm/°C) LSB (ppm/°C) LSB (ppm/°C)
SUPPLY REJECTION Change in Full-Scale Calibration V_{CC} = 15 V ± 1.5 V or 12 V ± 0.6 V V_{LOGIC} = 5 V ± 0.5 V V_{EE} = -15 V ± 1.5 V or -12 V ± 0.6 V			±2 ±1/2 ±2			1 1/2 1			1 1/2 1	LSB LSB LSB
OG INPUT Ranges ipolar nipolar t Impedance 0 Volt Span 0 Volt Span	-5 -10 0 0 3 6	5 10	+5 +10 +10 +20 7 14	-5 -10 0 0 3 6	5 10	+5 +10 +10 +20 7 14	5 10 0 0 3 6	5 10	+5 +10 +10 +20 7 14	Volts Volts Volts Volts kΩ kΩ
TAL CHARACTERISTICS[1] (T_{MIN}-T_{MAX}) ut[2] (CE, $\overline{CS}$, R/$\overline{C}$, A_0) Logic "1" Voltage Logic "0" Voltage Current Capacitance	+2.0 -0.5 -20	5	+5.5 +0.8 +20	+2.0 -0.5 -20	5	+5.5 +0.8 +20	+2.0 -0.5 -20	5	+5.5 +0.8 +20	Volts Volts μA pF
tput (DB11-DB0, STS) Logic "1" Voltage (I_{SOURCE} ≤ 500 μA) Logic "0" Voltage (I_{SINK} ≤ 1.6 mA) Leakage (DB11-DB0, High-Z State) Capacitance	+2.4 -20	5	+0.4 +20	+2.4 -20	5	+0.4 +20	+2.4 -20	5	+0.4 +20	Volts Volts μA pF
VER SUPPLIES perating Range V_{LOGIC} V_{CC} V_{EE} perating Current I_{LOGIC} I_{CC} I_{EE}	+4.5 +11.4 -11.4	30 2 18	+5.5 +16.5 -16.5 40 5 30	+4.5 +11.4 -11.4	30 2 18	+5.5 +16.5 -16.5 40 5 30	+4.5 +11.4 -11.4	30 2 18	+5.5 +16.5 -16.5 40 5 30	Volts Volts Volts mA mA mA
WER DISSIPATION		390	725		390	725		390	725	mW
TERNAL REFERENCE VOLTAGE Output Current (Available for External Loads)[3] (External Load Should not Change During Conversion)	9.98	10.0	10.02 1.5	9.98	10.0	10.02 1.5	9.99	10.0	10.01 1.5	Volts mA
CKAGE OPTION[4] Ceramic (D-28)		AD574ASD			AD574ATD			AD574AUD		

OTES
Detailed Timing Specifications appear in the Timing Section.
12/$\overline{8}$ Input is not TTL-compatible and must be hard wired to V_{LOGIC} or Digital Common.
The reference should be buffered for operation on ±12 V supplies.
D = Ceramic DIP.
pecifications subject to change without notice.



AD574A Block Diagram and Pin Configuration

OLUTE MAXIMUM RATINGS*

ifications apply to all grades, except where noted)

to Digital Common	0 V to +16.5 V
to Digital Common	0 V to −16.5 V
	0 V to +7 V
GIC to Digital Common	±1 V
log Common to Digital Common	
trol Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to	
Digital Common	−0.5 V to V_{LOGIC} + 0.5 V
log Inputs (REF IN, BIP OFF, 10 V_{IN}) to	
Analog Common	V_{EE} to V_{CC}
	±24 V
V_{IN} to Analog Common	Indefinite Short to Common
F OUT	Momentary Short to V_{CC}
Chip Temperature	175°C
Power Dissipation	825 mW
Lead Temperature (Soldering, 10 sec)	+300°C
Storage Temperature (Ceramic)	−65°C to +150°C
(Plastic)	−25°C to +100°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model[1]	Temperature Range	Linearity Error Max (T_{MIN} to T_{MAX})	Resolution No Missing Codes (T_{MIN} to T_{MAX})	Max Full Scale T.C. (ppm/°C)
AD574AJ(X)	0°C to +70°C	±1 LSB	11 Bits	50.0
AD574AK(X)	0°C to +70°C	±1/2 LSB	12 Bits	27.0
AD574AL(X)	0°C to +70°C	±1/2 LSB	12 Bits	10.0
AD574AS(X)[2]	−55°C to +125°C	±1 LSB	11 Bits	50.0
AD574AT(X)[2]	−55°C to +125°C	±1 LSB	12 Bits	25.0
AD574AU(X)[2]	−55°C to +125°C	±1 LSB	12 Bits	12.5

NOTES

[1]X = Package designator. Available packages are: D (D-28) for all grades. E (E-28A) for J and K grades and /883B processed S, T and U grades. N (N-28) for J, K, and L grades. P (P-28A) for PLCC in J, K grades. Example: AD574AKN is K grade in plastic DIP.

[2]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to Analog Devices Military Products Databook.

REV. B

E AD574A OFFERS GUARANTEED MAXIMUM LINEARITY ERROR OVER THE FULL OPERATING MPERATURE RANGE

FINITIONS OF SPECIFICATIONS

IEARITY ERROR

earity error refers to the deviation of each individual code n a line drawn from "zero" through "full scale". The point d as "zero" occurs 1/2 LSB (1.22 mV for 10 volt span) be- e the first code transition (all zeros to only the LSB "on"). ull scale" is defined as a level 1 1/2 LSB beyond the last code nsition (to all ones). The deviation of a code from the true aight line is measured from the middle of each particular de.

he AD574AK, L, T, and U grades are guaranteed for maxi- um nonlinearity of ±1/2 LSB. For these grades, this means at an analog value which falls exactly in the center of a given ode width will result in the correct digital output code. Values earer the upper or lower transition of the code width may pro- uce the next upper or lower digital output code. The AD574AJ nd S grades are guaranteed to ±1 LSB max error. For these rades, an analog value which falls within a given code width vill result in either the correct code for that region or either djacent one.

Note that the linearity error is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the AD574AK, L, T, and U grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The AD574AJ and S grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

UNIPOLAR OFFSET

The first transition should occur at a level 1/2 LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following two pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

BIPOLAR OFFSET

In the bipolar mode the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2 LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±1/2 LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

LEFT-JUSTIFIED DATA

The data format used in the AD574A is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

FULL-SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1 1/2 LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full-scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05% to 0.1% of full scale, can be trimmed out as shown in Figures 3 and 4.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

POWER SUPPLY REJECTION

The standard specifications for the AD574A assume use of +5.00 V and ±15.00 V or ±12.00 V supplies. The only effect of power supply error on the performance of the device will be a small change in the full-scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum full-scale change from the initial value with the supplies at the various limits.

CODE WIDTH

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full-scale range or 2.44 mV out of 10 volts for a 12-bit ADC.

UIT OPERATION

AD574A is a complete 12-bit A/D converter which requires ternal components to provide the complete successive- ximation analog-to-digital conversion function. A block am of the AD574A is shown in Figure 1.

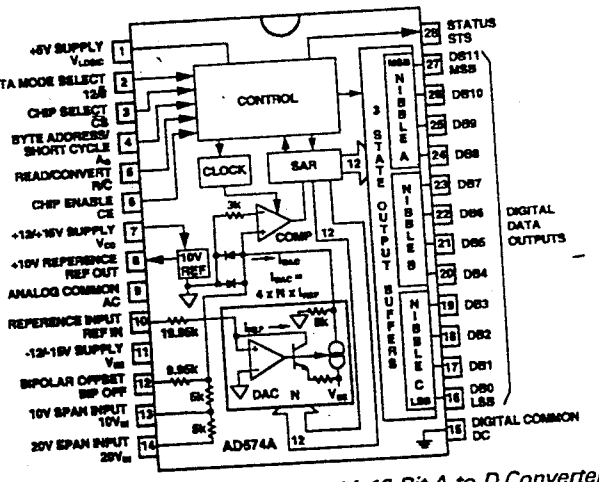


Figure 1. Block Diagram of AD574A 12-Bit A-to-D Converter

When the control section is commanded to initiate a conversion (as described later), it enables the clock and resets the successive-approximation register (SAR) to all zeros. Once a conversion cycle has begun, it cannot be stopped or restarted and data is not available from the output buffers. The SAR, timed by the clock, will sequence through the conversion cycle and return an end-of-convert flag to the control section. The control section will then disable the clock, bring the output status flag low, and enable control functions to allow data read functions by external command.

During the conversion cycle, the internal 12-bit current output DAC is sequenced by the SAR from the most significant bit (MSB) to least significant bit (LSB) to provide an output current which accurately balances the input signal current through the 5 kΩ (or 10 kΩ) input resistor. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±1/2 LSB.

The temperature-compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10.00 volts ±0.2%; it can supply up to 1.5 mA to an external load in addition to the requirements of the reference input resistor (0.5 mA) and bipolar offset resistor (1 mA) when the AD574A is powered from ±15 V supplies. If the AD574A is used with ±12 V supplies, or if external current must be supplied over the full temperature range, an external buffer amplifier is recommended. Any external load on the AD574A reference must remain constant during conversion. The thin-film application resistors are trimmed to match the full-scale output current of the DAC. There are two 5 kΩ input scaling resistors to allow either a 10 volt or 20 volt span. The 10 kΩ bipolar offset resistor is grounded for unipolar operation and connected to the 10 volt reference for bipolar operation.

DRIVING THE AD574 ANALOG INPUT

The internal circuitry of the AD574 dictates that its analog input be driven by a low source impedance. Voltage changes at the current summing node of the internal comparator result in abrupt modulations of the current at the analog input. For accurate 12-bit conversions the driving source must be capable of holding a constant output voltage under these dynamically changing load conditions.

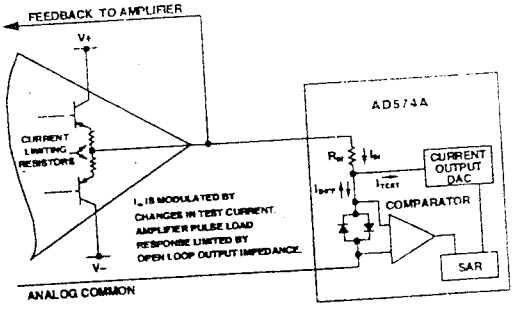


Figure 2. Op Amp – AD574A Interface

The output impedance of an op amp has an open-loop value which, in a closed loop, is divided by the loop gain available at the frequency of interest. The amplifier should have acceptable loop gain at 500 kHz for use with the AD574A. To check whether the output properties of a signal source are suitable, monitor the AD574's input with an oscilloscope while a conversion is in progress. Each of the 12 disturbances should subside in 1 µs or less.

For applications involving the use of a sample-and-hold amplifier, the AD585 is recommended. The AD711 or AD544 op amps are recommended for dc applications.

SAMPLE-AND-HOLD AMPLIFIERS

Although the conversion time of the AD574A is a maximum of 35 µs, to achieve accurate 12-bit conversions of frequencies greater than a few Hz requires the use of a sample-and-hold amplifier (SHA). If the voltage of the analog input signal driving the AD574A changes by more than 1/2 LSB over the time interval needed to make a conversion, then the input requires a SHA.

The AD585 is a high linearity SHA capable of directly driving the analog input of the AD574A. The AD585's fast acquisition time, low aperture and low aperture jitter are ideally suited for high-speed data acquisition systems. Consider the AD574A converter with a 35 µs conversion time and an input signal of 10 V p-p: the maximum frequency which may be applied to achieve rated accuracy is 1.5 Hz. However, with the addition of an AD585, as shown in Figure 3, the maximum frequency increases to 26 kHz.

The AD585's low output impedance, fast-loop response, and low droop maintain 12-bits of accuracy under the changing load conditions that occur during a conversion, making it suitable for use in high accuracy conversion systems. Many other SHAs cannot achieve 12-bits of accuracy and can thus compromise a system. The AD585 is recommended for AD574A applications requiring a sample and hold.

An alternate approach is to use the AD1674, which combines the ADC and SHA on one chip, with a total throughput time of 10 µs.

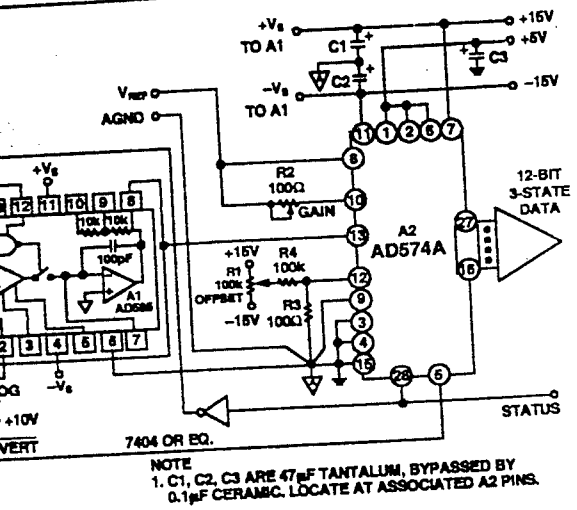


Figure 3. AD574A with AD585 Sample and Hold

PPLY DECOUPLING AND LAYOUT NSIDERATIONS

critically important that the AD574A power supplies be fil-d, well regulated, and free from high frequency noise. Use of sy supplies will cause unstable output codes. Switching ver supplies are not recommended for circuits attempting to ieve 12-bit accuracy unless great care is used in filtering any tching spikes present in the output. Remember that a few llivolts of noise represents several counts of error in a 12-bit DC.

ecoupling capacitors should be used on all power supply pins; e +5 V supply decoupling capacitor should be connected rectly from Pin 1 to Pin 15 (digital common) and the $+V_{CC}$ d $-V_{EE}$ pins should be decoupled directly to analog common in 9). A suitable decoupling capacitor is a 4.7 μF tantalum pe in parallel with a 0.1 μF disc ceramic type.

ircuit layout should attempt to locate the AD574A, associated alog input circuitry, and interconnections as far as possible om logic circuitry. For this reason, the use of wire-wrap circuit onstruction is not recommended. Careful printed circuit con-truction is preferred.

GROUNDING CONSIDERATIONS

The analog common at Pin 9 is the ground reference point for the internal reference and is thus the "high quality" ground for the AD574A; it should be connected directly to the analog refer-ence point of the system. In order to achieve all of the high accuracy performance available from the AD574A in an envi-ronment of high digital noise content, the analog and digital commons should be connected together at the package. In some situations, the digital common at Pin 15 can be connected to the most convenient ground reference point; analog power return is preferred.

UNIPOLAR RANGE CONNECTIONS FOR THE AD574A

The AD574A contains all the active components required to perform a complete 12-bit A/D conversion. Thus, for most situ-ations, all that is necessary is connection of the power supplies (+5 V, +12 V/+15 V and –12 V/–15 V), the analog input, and the conversion initiation command, as discussed on the next page. Analog input connections and calibration are easily ac-complished; the unipolar operating mode is shown in Figure 4.

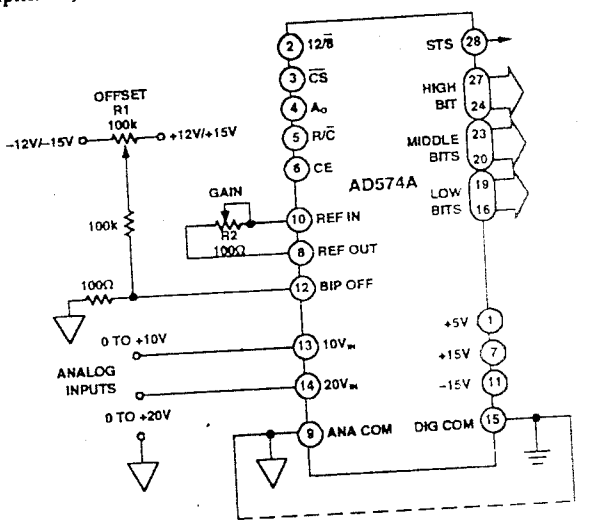


Figure 4. Unipolar Input Connections

All of the thin-film application resistors of the AD574A are trimmed for absolute calibration. Therefore, in many applica-tions, no calibration trimming will be required. The absolute accuracy for each grade is given in the specification tables. For example, if no trims are used, the AD574AK guarantees ±1 LSB max zero offset error and ±0.25% (10 LSB) max full-scale error. (Typical full-scale error is ±2 LSB.) If the offset trim is not required, Pin 12 can be connected directly to Pin 9; the two resistors and trimmer for Pin 12 are then not needed. If the full-scale trim is not needed, a 50 Ω ± 1% metal film resistor should be connected between Pin 8 and Pin 10.

The analog input is connected between Pin 13 and Pin 9 for a 0 V to +10 V input range, between 14 and Pin 9 for a 0 V to +20 V input range. The AD574A easily accommodates an input signal beyond the supplies. For the 10 volt span input, the LSB has a nominal value of 2.44 mV; for the 20 volt span, 4.88 mV. If a 10.24 V range is desired (nominal 2.5 mV/bit), the gain trimmer (R2) should be replaced by a 50 Ω resistor, and a 200 Ω trimmer inserted in series with the analog input to Pin 13 for a full-scale range of 20.48 V (5 mV/bit), use a 500 Ω trim-mer into Pin 14. The gain trim described below is now done with these trimmers. The nominal input impedance into Pin 13 is 5 kΩ, and 10 kΩ into Pin 14.

UNIPOLAR CALIBRATION

The AD574A is intended to have a nominal 1/2 LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above and below it). Thus, the first transition (from 0000 0000 0000 to 0000 0000 0001) will occur for an input level of +1/2 LSB (1.22 mV for 10 V range).

If Pin 12 is connected to Pin 9, the unit will behave in this man-ner, within specifications. If the offset trim (R1) is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give ap-proximately ±15 mV of offset trim range.

full-scale trim is done by applying a signal 1 1/2 LSB below nominal full scale (9.9963 for a 10 V range). Trim R2 to the last transition (1111 1111 1110 to 1111 1111 1111).

OLAR OPERATION

connections for bipolar ranges are shown in Figure 5. in, as for the unipolar ranges, if the offset and gain specifica- s are sufficient, one or both of the trimmers shown can be aced by a 50 Ω ± 1% fixed resistor. Bipolar calibration is lar to unipolar calibration. First, a signal 1/2 LSB above ative full scale (–4.9988 V for the ±5 V range) is applied and is trimmed to give the first transition (0000 0000 0000 to 0 0000 0001). Then a signal 1 1/2 LSB below positive full e (+4.9963 V the ±5 V range) is applied and R2 trimmed to the last transition (1111 11111110 to 1111 1111 1111).

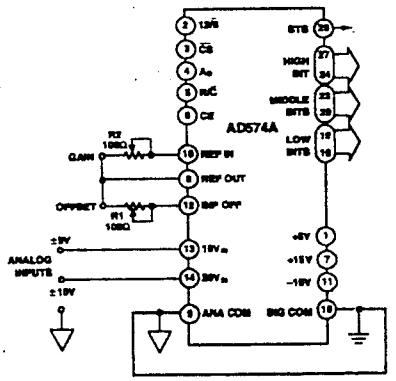


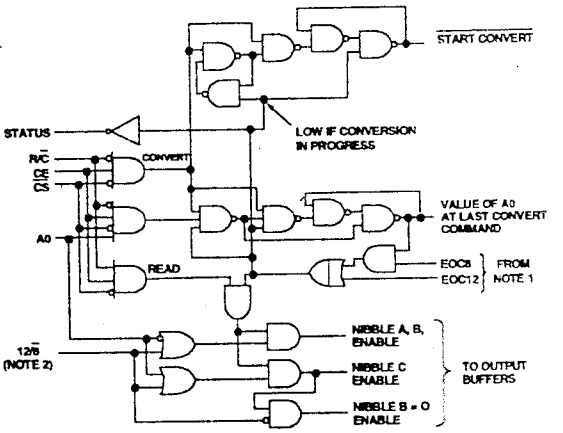
Figure 5. Bipolar Input Connections

NTROL LOGIC

e AD574A contains on-chip logic to provide conversion ini- ion and data read operations from signals commonly avail- e in microprocessor systems. Figure 6 shows the internal ic circuitry of the AD574A.

e control signals CE, $\overline{CS}$, and R/$\overline{C}$ control the operation of converter. The state of R/$\overline{C}$ when CE and $\overline{CS}$ are both erted determines whether a data read (R/$\overline{C}$ = 1) or a convert $\overline{C}$ = 0) is in progress. The register control inputs A_0 and $\overline{8}$ control conversion length and data format. The A_0 line is ually tied to the least significant bit of the address bus. If a nversion is started with A_0 low, a full 12-bit conversion cycle nitiated. If A_0 is high during a convert start, a shorter 8-bit nversion cycle results. During data read operations, A_0 deter- nes whether the three-state buffers containing the 8 MSBs of conversion result (A_0 = 0) or the 4 LSBs (A_0 = 1) are abled. The 12/$\overline{8}$ pin determines whether the output data is be organized as two 8-bit words (12/$\overline{8}$ tied to DIGITAL OMMON) or a single 12-bit word (12/$\overline{8}$ tied to V_{LOGIC}). The $\overline{8}$ pin is not TTL-compatible and must be hard-wired to her V_{LOGIC} or DIGITAL COMMON. In the 8-bit mode, the te addressed when A_0 is high contains the 4 LSBs from the nversion followed by four trailing zeroes. This organization ows the data lines to be overlapped for direct interface to bit buses without the need for external three-state buffers.

is not recommended that A_0 change state during a data read eration. Asymmetrical enable and disable times of the ree-state buffers could cause internal bus contention resulting potential damage to the AD574A.



NOTE 1: WHEN START CONVERT GOES LOW, THE EOC (END OF CONVERSION) SIGNALS GO LOW. EOC8 RETURNS HIGH AFTER AN 8-BIT CONVERSION CYCLE IS COMPLETE, AND EOC12 RETURNS HIGH WHEN ALL 12-BITS HAVE BEEN CONVERTED. THE EOC SIGNALS PREVENT DATA FROM BEING READ DURING CONVERSIONS.

NOTE 2: 12/$\overline{8}$ IS NOT A TTL-COMPATABLE INPUT AND SHOULD ALWAYS BE WIRED DIRECTLY TO V_{LOGIC} OR DIGITAL COMMON.

Figure 6. AD574A Control Logic

An output signal, STS, indicates the status of the converter. STS goes high at the beginning of a conversion and returns low when the conversion cycle is complete.

Table I. AD574A Truth Table

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	Operation
0	X	X	X	X	None
X	1	X	X	X	None
1	0	0	X	0	Initiate 12-Bit Conversion
1	0	0	X	1	Initiate 8-Bit Conversion
1	0	1	Pin 1	X	Enable 12-Bit Parallel Output
1	0	1	Pin 15	0	Enable 8 Most Significant Bits
1	0	1	Pin 15	1	Enable 4 LSBs + 4 Trailing Zeroes

TIMING

The AD574A is easily interfaced to a wide variety of microprocessors and other digital systems. The following discussion of the timing requirements of the AD574A control signals should provide the system designer with useful insight into the operation of the device.

Table II. Convert Start Timing—Full Control Mode

Symbol	Parameter	Min	Typ	Max	Units
t_{DSC}	STS Delay from CE			400	ns
t_{HEC}	CE Pulse Width	300			ns
t_{SSC}	$\overline{CS}$ to CE Setup	300			ns
t_{HSC}	$\overline{CS}$ Low During CE High	200			ns
t_{SRC}	R/$\overline{C}$ to CE Setup	250			ns
t_{HRC}	R/$\overline{C}$ Low During CE High	200			ns
t_{SAC}	A_0 to CE Setup	0			ns
t_{HAC}	A_0 Valid During CE High	300			ns
t_C	Conversion Time				
	8-Bit Cycle	10		24	µs
	12-Bit Cycle	15		35	µs

ıre 7 shows a complete timing diagram for the AD574A con- start operation. R/$\overline{C}$ should be low before both CE and $\overline{CS}$ asserted; if R/$\overline{C}$ is high, a read operation will momentarily ur, possibly resulting in system bus contention. Either CE or may be used to initiate a conversion; however, use of CE is ommended since it includes one less propagation delay than and is the faster input. In Figure 7, CE is used to initiate the version.

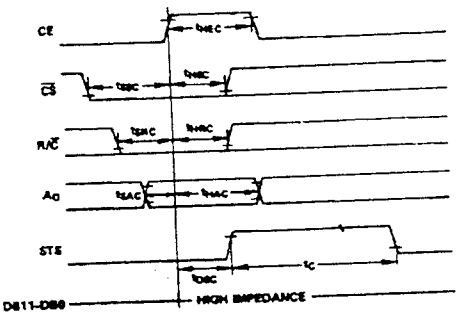


Figure 7. Convert Start Timing

nce a conversion is started and the STS line goes high, convert art commands will be ignored until the conversion cycle is omplete. The output data buffers cannot be enabled during onversion.

igure 8 shows the timing for data read operations. During data ead operations, access time is measured from the point where E and R/$\overline{C}$ both are high (assuming $\overline{CS}$ is already low). If $\overline{CS}$ s used to enable the device, access time is extended by 100 ns.

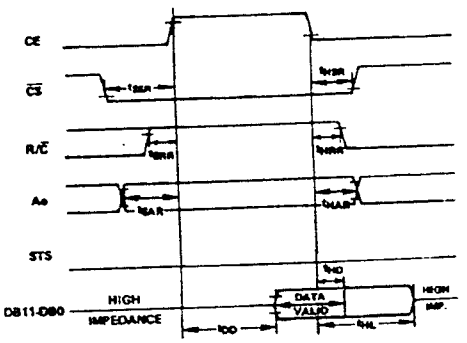


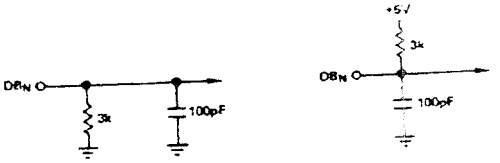
Figure 8. Read Cycle Timing

In the 8-bit bus interface mode (12/$\overline{8}$ input wired to DIGITAL COMMON), the address bit, A_0, must be stable at least 150 ns prior to $\overline{CE}$ going high and must remain stable during the entire read cycle. If A_0 is allowed to change, damage to the AD574A output buffers may result.

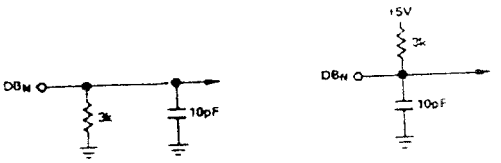
Table III. Read Timing—Full Control Mode

Symbol	Parameter	Min	Typ	Max	Units
t_{DD}[1]	Access Time (from CE)			200	ns
t_{HD}	Data Valid After CE Low	25			ns
t_{HL}[2]	Output Float Delay			100	ns
t_{SSR}	$\overline{CS}$ to CE Setup	150			ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0			ns
t_{SAR}	A_0 to CE Setup	150			ns
t_{HSR}	$\overline{CS}$ Valid After CE Low	50			ns
t_{HRR}	R/$\overline{C}$ High After CE Low	0			ns
t_{HAR}	A_0 Valid After CE Low	50			ns

NOTES
[1] t_{DD} is measured with the load circuit of Figure 9 and defined as the time required for an output to cross 0.4 V or 2.4 V.
[2] t_{HL} is defined as the time required for the data lines to change 0.5 V when loaded with the circuit of Figure 10.



a. High-Z to Logic 1 *b. High-Z to Logic 0*
Figure 9. Load Circuit for Access Time Test



a. Logic 1 to High-Z *b. Logic 0 to High-Z*
Figure 10. Load Circuit for Output Float Delay Test

"STAND-ALONE" OPERATION

The AD574A can be used in a "stand-alone" mode, which is useful in systems with dedicated input ports available and thus not requiring full bus interface capability.

In this mode, CE and 12/$\overline{8}$ are wired high, $\overline{CS}$ and A_0 are wired low, and conversion is controlled by R/$\overline{C}$. The three-state buffers are enabled when R/$\overline{C}$ is high and a conversion starts when R/$\overline{C}$ goes low. This allows two possible control signals—a high pulse or a low pulse. Operation with a low pulse is shown in Figure 11. In this case, the outputs are forced into the high impedance state in response to the falling edge of R/$\overline{C}$ and return

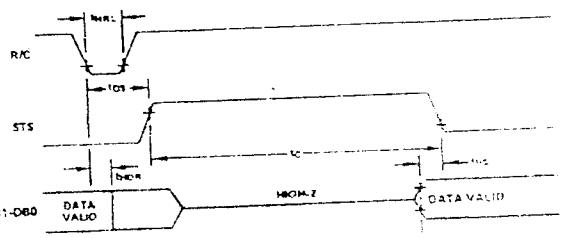
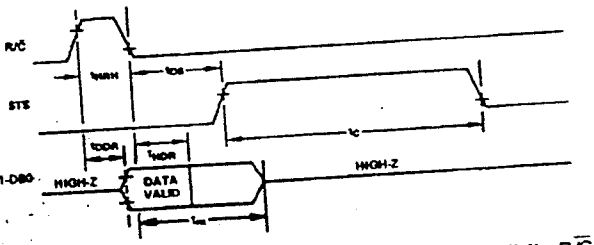


Figure 11. Low Pulse for R/$\overline{C}$—Outputs Enabled After Conversion

d logic levels after the conversion cycle is completed. The ne goes high 600 ns after R/$\overline{C}$ goes low and returns low after data is valid.

version is initiated by a high pulse as shown in Figure 12, ta lines are enabled during the time when R/$\overline{C}$ is high. alling edge of R/$\overline{C}$ starts the next conversion, and the data return to three-state (and remain three-state) until the next pulse of R/$\overline{C}$.



ure 12. High Pulse for R/$\overline{C}$—Outputs Enabled While R/$\overline{C}$ gh, Otherwise High-Z

Table IV. Stand-Alone Mode Timing

mbol	Parameter	Min	Typ	Max	Units
RL	Low R/$\overline{C}$ Pulse Width	250			ns
S	STS Delay from R/$\overline{C}$			600	ns
DR	Data Valid After R/$\overline{C}$ Low	25			ns
HL	Output Float Delay			150	ns
HS	STS Delay After Data Valid	300		1000	ns
HRH	High R/$\overline{C}$ Pulse Width	300			ns
DDR	Data Access Time			250	ns

Usually the low pulse for R/$\overline{C}$ stand-alone mode will be used. Figure 13 illustrates a typical stand-alone configuration for 8086 type processors. The addition of the 74F/S374 latches improves bus access/release times and helps minimize digital feedthrough to the analog portion of the converter.

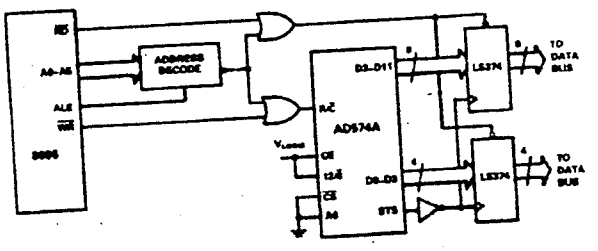


Figure 13. 8086 Stand-Alone Configuration

INTERFACING THE AD574A TO MICROPROCESSORS

The control logic of the AD574A makes direct connection to most microprocessor system buses possible. While it is impossible to describe the details of the interface connections for every microprocessor type, several representative examples will be described here.

GENERAL A/D CONVERTER INTERFACE CONSIDERATIONS

A typical A/D converter interface routine involves several operations. First, a write to the ADC address initiates a conversion. The processor must then wait for the conversion cycle to complete, since most ADCs take longer than one instruction cycle to complete a conversion. Valid data can, of course, only be read after the conversion is complete. The AD574A provides an output signal (STS) which indicates when a conversion is in progress. This signal can be polled by the processor by reading it through an external three-state buffer (or other input port). The STS signal can also be used to generate an interrupt upon completion of conversion, if the system timing requirements are critical (bear in mind that the maximum conversion time of the AD574A is only 35 microseconds) and the processor has other tasks to perform during the ADC conversion cycle. Another possible time-out method is to assume that the ADC will take 35 microseconds to convert, and insert a sufficient number of "do-nothing" instructions to ensure that 35 microseconds of processor time is consumed.

Once it is established that the conversion is finished, the data can be read. In the case of an ADC of 8-bit resolution (or less), a single data read operation is sufficient. In the case of converters with more data bits than are available on the bus, a choice of data formats is required, and multiple read operations are needed. The AD574A includes internal logic to permit direct interface to 8-bit or 16-bit data buses, selected by connection of the 12/$\overline{8}$ input. In 16-bit bus applications (12/$\overline{8}$ high) the data lines (DB11 through DB0) may be connected to either the 12 most significant or 12 least significant bits of the data bus. The remaining four bits should be masked in software. The interface to an 8-bit data bus (12/$\overline{8}$ low) is done in a left-justified format. The even address (A0 low) contains the 8 MSBs (DB11 through DB4). The odd address (A0 high) contains the 4 LSBs (DB3 through DB0) in the upper half of the byte, followed by four trailing zeroes, thus eliminating bit masking instructions.

It is not possible to rearrange the AD574A data lines for right justified 8-bit bus interface.

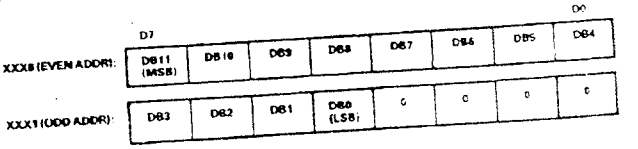


Figure 14. AD574A Data Format for 8-Bit Bus

SPECIFIC PROCESSOR INTERFACE EXAMPLES

Z-80 System Interface

The AD574A may be interfaced to the Z-80 processor in an I/O or memory mapped configuration. Figure 15 illustrates an I/O or mapped configuration. The Z-80 uses address lines A0–A7 to decode the I/O port address.

An interesting feature of the Z-80 is that during I/O operations a single wait state is automatically inserted, allowing the AD574A to be used with Z-80 processors having clock speeds up to 4 MHz. For applications faster than 4 MHz use the wait state generator in Figure 16. In a memory mapped configuration the AD574A may be interfaced to Z-80 processors with clock speeds of up to 2.5 MHz.

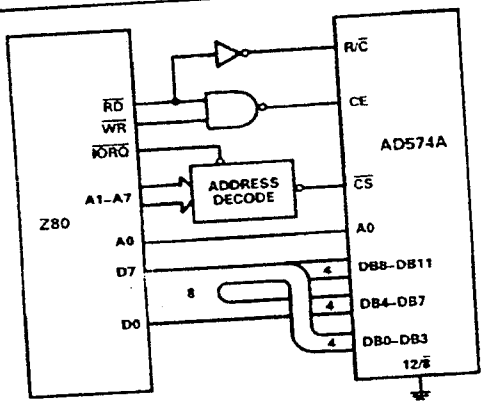


Figure 15. Z80—AD574A Interface

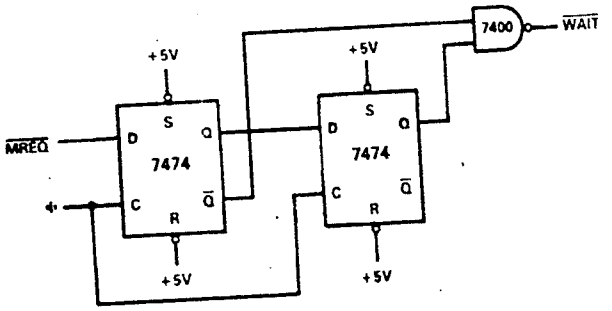


Figure 16. Wait State Generator

IBM PC Interface

The AD574A appears in Figure 17 interfaced to the 4 MHz 8088 processor of an IBM PC. Since the device resides in I/O space, its address is decoded from only the lower ten address lines and must be gated with AEN (active low) to mask out internal DMA cycles which use the same I/O address space. This active low signal is applied to $\overline{CS}$. $\overline{IOR}$ and $\overline{IOW}$ are used to initiate the conversion and read, and are gated together to drive the chip enable, CE. Because the data bus width is limited to 8 bits, the AD574A data resides in two adjacent addresses selected by A0.

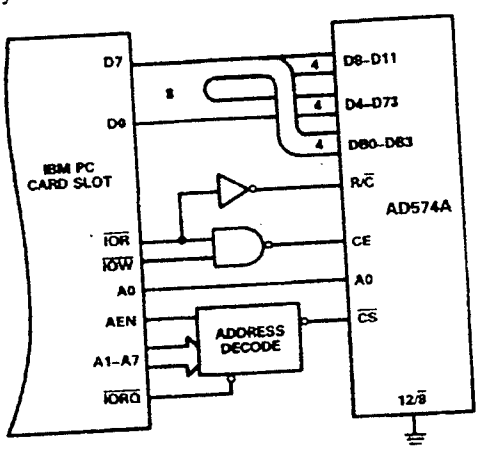


Figure 17. IBM PC—AD574A Interface

Note: Due to the large number of options that may be installed in the PC, the I/O bus loading should be limited to one Schottky TTL load. Therefore, a buffer/driver should be used when interfacing more than two AD574As to the I/O bus.

8086 Interface

The data mode select pin (12/$\overline{8}$) of the AD574A should be connected to V_{LOGIC} to provide a 12-bit data output. To prevent possible bus contention, a demultiplexed and buffered address/data bus is recommended. In the cases where the 8-bit short conversion cycle is not used, A0 should be tied to digital common. Figure 18 shows a typical 8086 configuration.

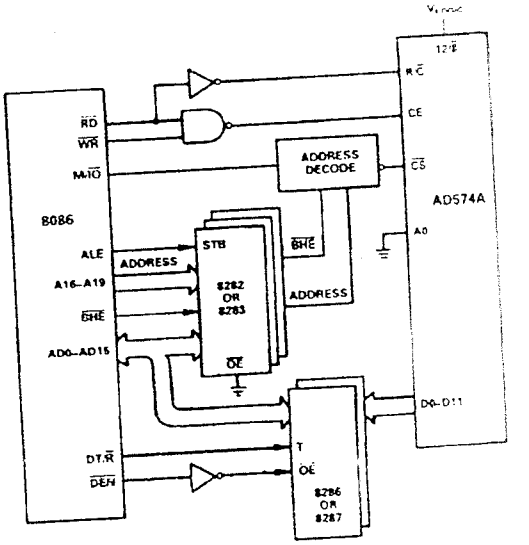


Figure 18. 8086—AD574A with Buffered Bus Interface

For clock speeds greater than 4 MHz wait state insertion similar to Figure 16 is recommended to ensure sufficient CE and R/$\overline{C}$ pulse duration.

The AD574A can also be interfaced in a stand-alone mode (see Figure 13). A low going pulse derived from the 8086's $\overline{WR}$ signal logically ORed with a low address decode starts the conversion. At the end of the conversion, STS clocks the data into the three-state latches.

68000 Interface

The AD574, when configured in the stand-alone mode, will easily interface to the 4 MHz version of the 68000 microprocessor. The 68000 R/$\overline{W}$ signal combined with a low address decode initiates conversion. The $\overline{UDS}$ or $\overline{LDS}$ signal, with the decoded address, generates the $\overline{DTACK}$ input to the processor, latching in the AD574A's data. Figure 19 illustrates this configuration.

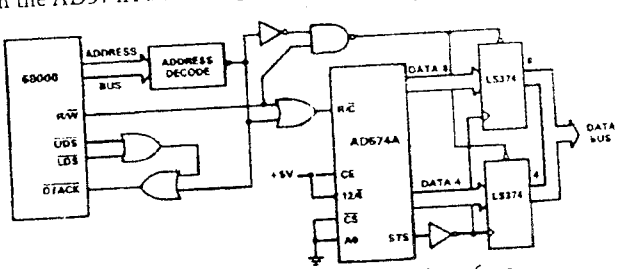
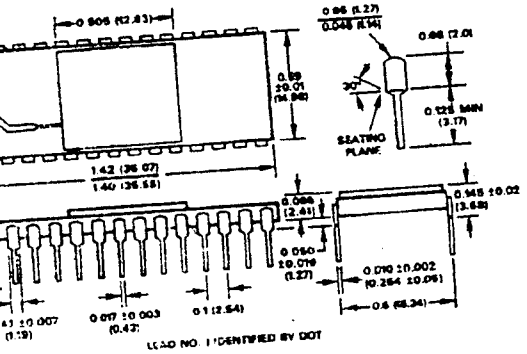


Figure 19. 68000—AD574A Interface

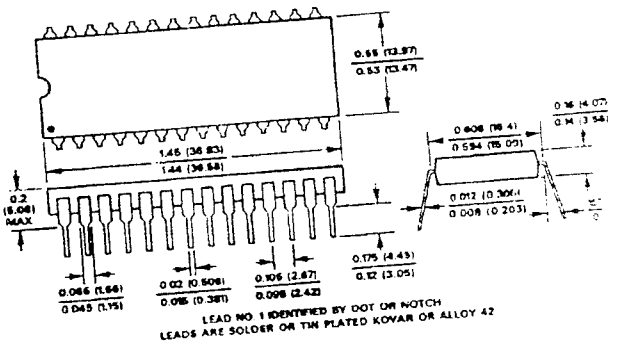
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

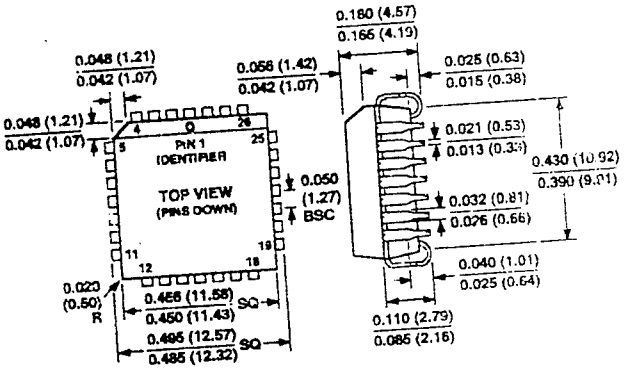
28-Pin Ceramic DIP Package (D-28)



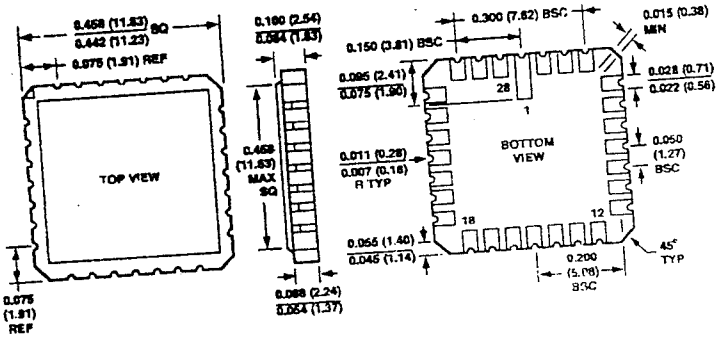
28-Lead Plastic DIP Package (N-28A)



28-Terminal PLCC Package (P-28A)

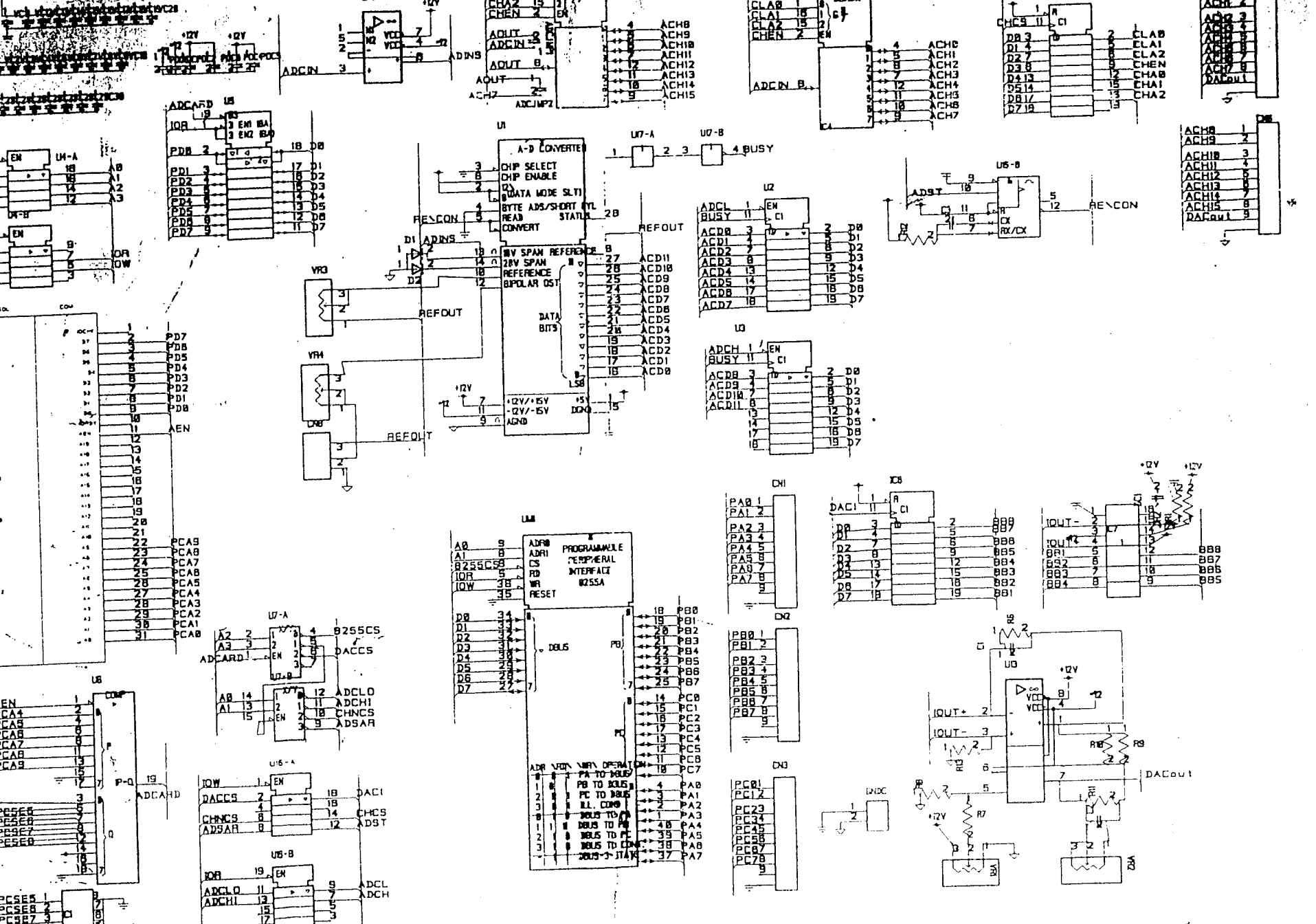


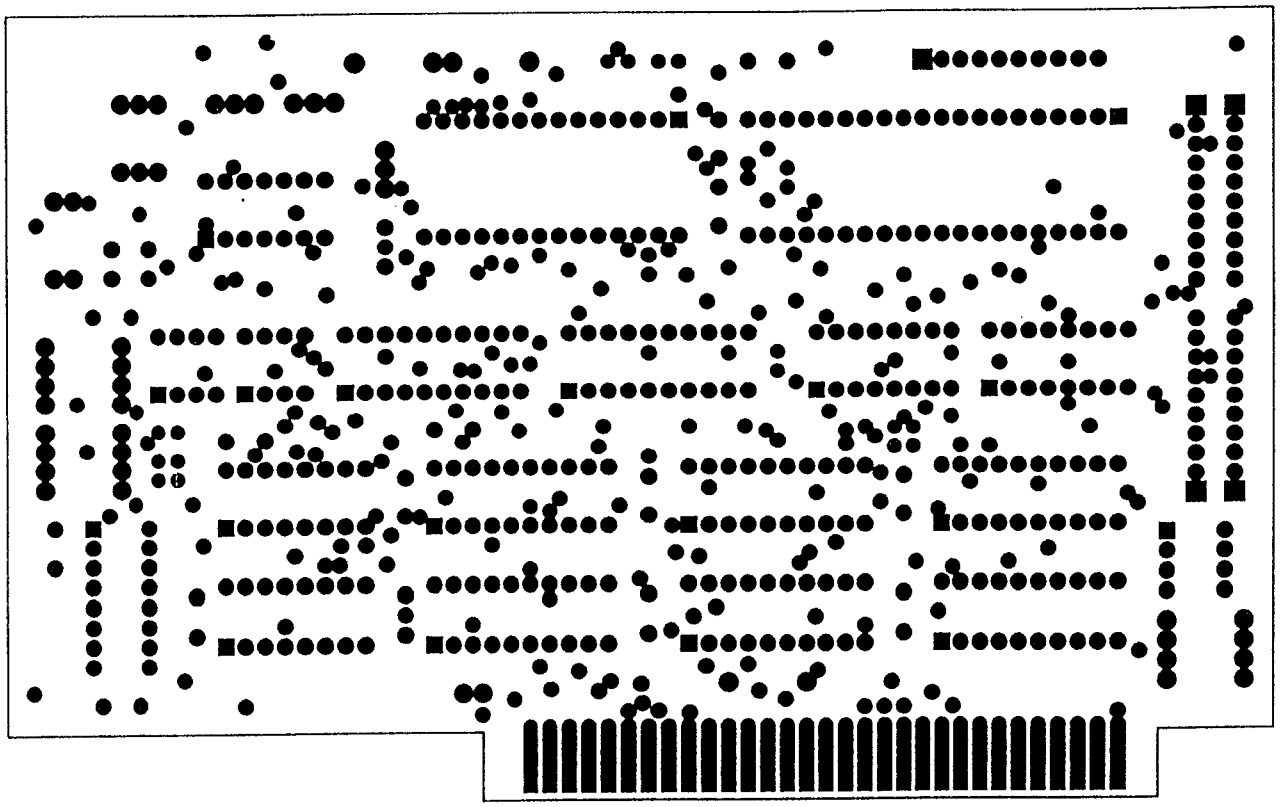
28-Terminal LCC Package (E-28A)

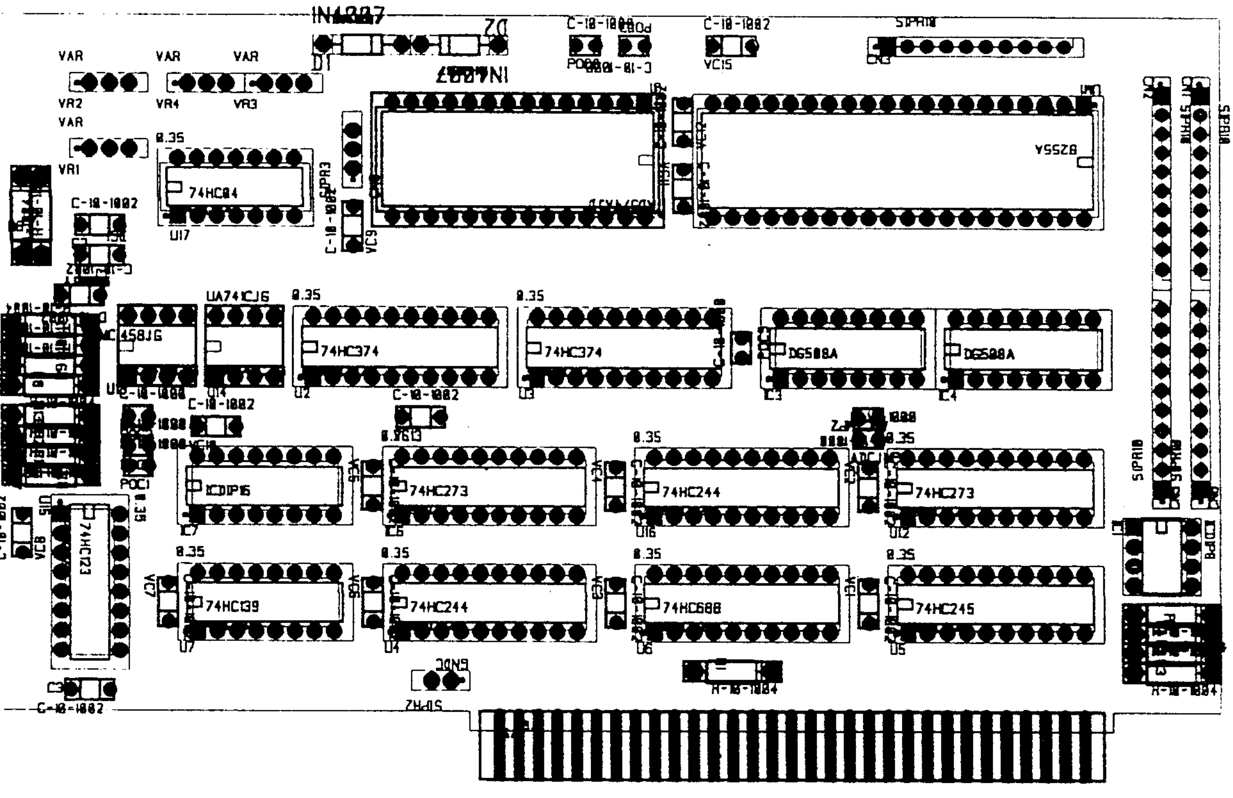


C704d-10-8/88

REV. B







IN4007
D1
D2
C-10-1000
PO00
C-10-1002
VC15
SIPR10
CN3
VAR
VR2
VR4
VR3
VR1
0.35
74HC04
U17
C-10-1002
VC9
8255A
UA741CJ6
MC1458JG
74HC374
DG508A
IC3
IC4
U14
U2
U3
ICDIP16
74HC273
74HC244
74HC273
IC7
IC6
U16
U12
POC1
U15
74HC123
VC8
74HC139
74HC244
74HC688
74HC245
U7
U4
U6
U5
VC7
GNDC
SIPR2
R-10-1004
C-10-1002

Add on Board.