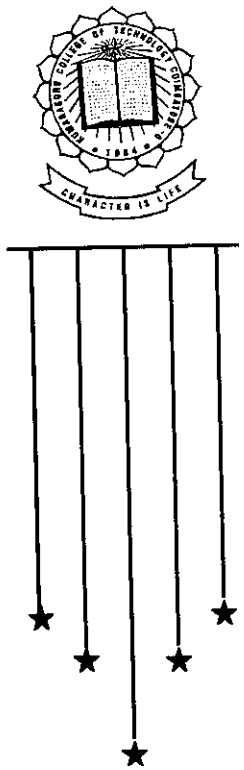
AUTOMATIC HUMIDITY CONTROLLER



P-1397

ISO 9001:2000 Certified

PROJECT REPORT

SUBMITTED BY

NAVEEN KUMAR K

RUMYA R

SELVA KUMAR D

SUGANYA N

2002 - 2003

GUIDED BY

Mrs.LATHA M.E.,

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE AWARD OF THE DEGREE OF

BACHELOR OF ENGINEERING IN ELECTRONICS & COMMUNICATION ENGINEERING OF THE BHARATHIAR UNIVERSITY, COIMBATORE.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

KUMARAGURU COLLEGE OF TECHNOLOGY

COIMBATORE - 641 006.

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Coimbatore – 641006.

Department of Electronics & Communication Engineering

CERTIFICATE

This is to certify that the project entitled

AUTOMATIC HUMIDITY CONTROLLER

has been submitted by

NAVEEN KUMAR . K (9927D0143)
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SUGANYA . N (9927D0172)

in partial fulfillment of the requirements for the award of the degree of

Bachelor of Engineering in **Electronics & Communication Engineering**

branch of **BHARATHIAR UNIVERSITY, Coimbatore**

during the academic year 2002-2003.

R. Lall 17/3/03.

(Internal guide) **(Head of the Department)**

Certified that the candidate was examined by us in the project work

Viva – Voce Examination held on 18.3.03.

(Internal Examiner) **(External Examiner)**

Statex

Statex Electronics

TO WHOMSOEVER IT MAY CONCERN

This is to certify that the following final year B.E."Electronis and Communication Engineering" Students of Kumaraguru College of Technology, Coimbatore have completed the project in our organisation.

1. K.NAVEEN KUMAR
2. R.RUMYA
3. D.SELVAKUMAR
4. N.SUGANYA

Project Title : "AUTOMATIC HUMIDITY CONTROLLER"

Project Period : JULY 2002 TO MARCH 2003

During this project , their attendance, conduct and behaviour were found to be GOOD.

Thanking you

Yours faithfully
for STATEX ELECTRONICS,

16/8/2003

AUTHORISED SINGNATORY.

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ACKNOWLEDGEMENT

We are greatly indebted to our beloved Principal **Dr.K.K. Padmanabhan B. Sc. (Engg.), M. Tech., Ph. D.,** who has been the backbone of all our deeds.

We earnestly express our gratitude and sincere thanks to our guide **Mrs.Latha M.E., Department of Electronics & Communication Engineering** for her consummate technical guidance, with constant encouragement and suggestions in carrying out this project successfully.

We would also like to thank **Prof.M.Muthuraman Ramaswamy M.E.,FIE,.FIETE.,MIEEE(USA).,MISTE.,MBMESI.,C.ENG.(I)., Head of the Department of Electronics & Communication Engineering** for lending a helping hand in this project.

We also express our sincere thanks to **Mr.V.Duraisami, Vice President , Statex Electronics , Coimbatore ,** for giving us an opportunity to do this project in their organization. We express our deepest gratitude to him and the staff members of the company for lending a helping hand in the successful completion of this project.

We also express our thanks to **all the faculty members of the Department of Electronics and Communication Engineering** for their support.

We owe much to our **parents and friends** for their moral support and valuable help rendered to us.

SYNOPSIS

A firmware has been developed to replace the manual humidity control processes in a textile mill. The manual monitoring and control system has been automated.

The humidity is controlled with the 8051F020 Cygnal series micro-controller, as the controlling unit. The outputs from the relative humidity sensor and temperature sensor are given as analog inputs to the micro-controller where it is compared with the ideal value. Depending upon the result humidity is controlled by the driver circuit with TTL logic.

The results are displayed in PC, through serial communication. The software code for this interface is written in 'C – language'.

CONTENTS

INTRODUCTION

An automatic humidity controller is one which is designed to maintain the humidity within the required range. In addition to humidity control, there is a provision for temperature monitoring also.

In this project, humidity is sensed and a control unit is designed. Humidity sensor is of analog type and 8051F020 micro-controller acts as control unit.

The sensor output is given to a controller circuit which compares it with the stored ideal data and correspondingly controls the relay circuit.

This project can be employed in various industries where humidity maintenance is an essential requirement, especially in textile industries.

CHAPTER 2

HUMIDITY CONTROL AND ITS NEED

2.1 WHAT IS HUMIDITY

Humidity is the measure of water vapour content in air or some other gases. It may be expressed in various forms such as absolute humidity, relative humidity or dew point temperature.

Absolute humidity is the amount of water vapour actually present in air.

Relative Humidity (RH) is the best known and perhaps the most widely used way of expressing the water vapour content of air. Formally, elative humidity is defined as the ratio of water vapour actually present in the air to the maximum amount of water that the air could possibly hold at the same temperature, it is usually expressed as a percentage, 100% relative humidity means that air contains all the moisture that it can hold.

Dew point is defined as the saturation temperature of the mixture at the corresponding vapour pressure.

In this project the measurement and control is concerned with Relative Humidity though generally mentioned as humidity.

2.2 NEED FOR HUMIDITY CONTROL

Knowledge of the amount of water vapour in the air is very important in the operation and/or control of many industrial processes. In some cases the moisture contained in the ambient air is important, in the other cases the moisture contained in the product itself is more important to the success of the industrial process.

Relative humidity in a textile mill has to be maintained within a specified range otherwise which the following factors are affected.

- QUALITY OF YARN:

If the humidity is not within the range and if it is lesser, the threads are prone to easier cutting and if humidity is more they start spinning inside the machine itself.

- WEIGHT LOSS:

A standard quality fiber contains about seven and half percentage moisture in it. Any variation in humidity will cause weight loss in the fiber.

- WORKER'S EFFICIENCY:

The humidity range is fixed taking into account the human working conditions. Any deviation may affect the worker causing fatigue and exhaustion. This degrades the performance of the industry.

Thus to improve the standard of the industry and quality of the product humidity has to be controlled and maintained.

2.3 CURRENT PROCESS

The process of humidity measurement and control is done manually at present.

MEASUREMENT:

Relative humidity is measured with the help of a hygrometer. It is made up of two bulbs - a wet bulb and a dry bulb protectively held in a wooden case. The average of the two bulb readings gives the relative humidity of air at that point. The measurements are noted down by the supervisor once every hour and necessary steps are taken depending on the humidity measured.

CONTROL MECHANISM:

a) When the measured humidity is less:

Air with high force is made to blow from the fan provided. A pumping motor is provided inside the water tank. It makes the water to come up with force. The air that falls on the shaft mixes up with the water and small droplets are formed. These droplets are passed through windows and various pipes from the windows carry it to various departments in the industry. The required one could be opened and cooled air goes to that department. Thus humidity is raised and maintained in the optimum range.

b) When the measured humidity is more:

Since the humidity is more, the outside air is not allowed. The windows are closed. So the inside air is re-circulated. First the air is made to blow with the help of a fan. The window provided to allow air from inside the industry to outside is opened. Thus the hot air mixes with the air and goes through the window to the required department. Since, only the same air is re-circulated, humidity is controlled.

2.4 PROJECT REQUIREMENTS

The manual method of humidity monitor and control suffers the following drawbacks:

- No continuous monitoring:

Humidity is measured only once in an hour. Within this period of time there may be humidity variations which goes unnoticed.

- Delay in control:

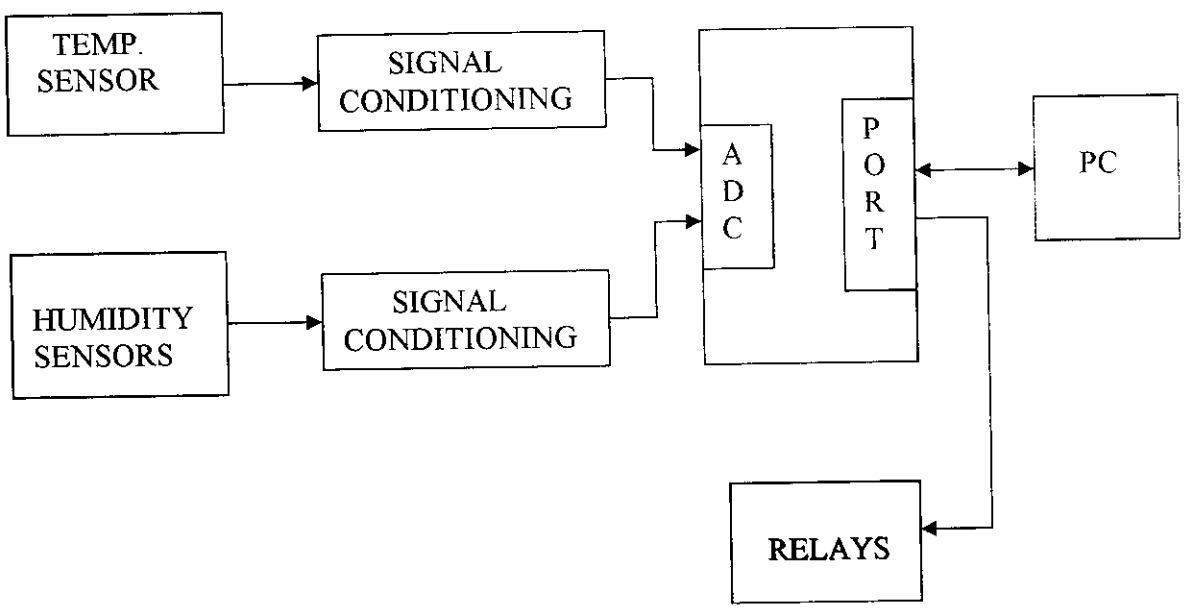
The time factor involved in the control mechanism is very high. This again leads to degradation of industrial standards.

- Less accuracy:

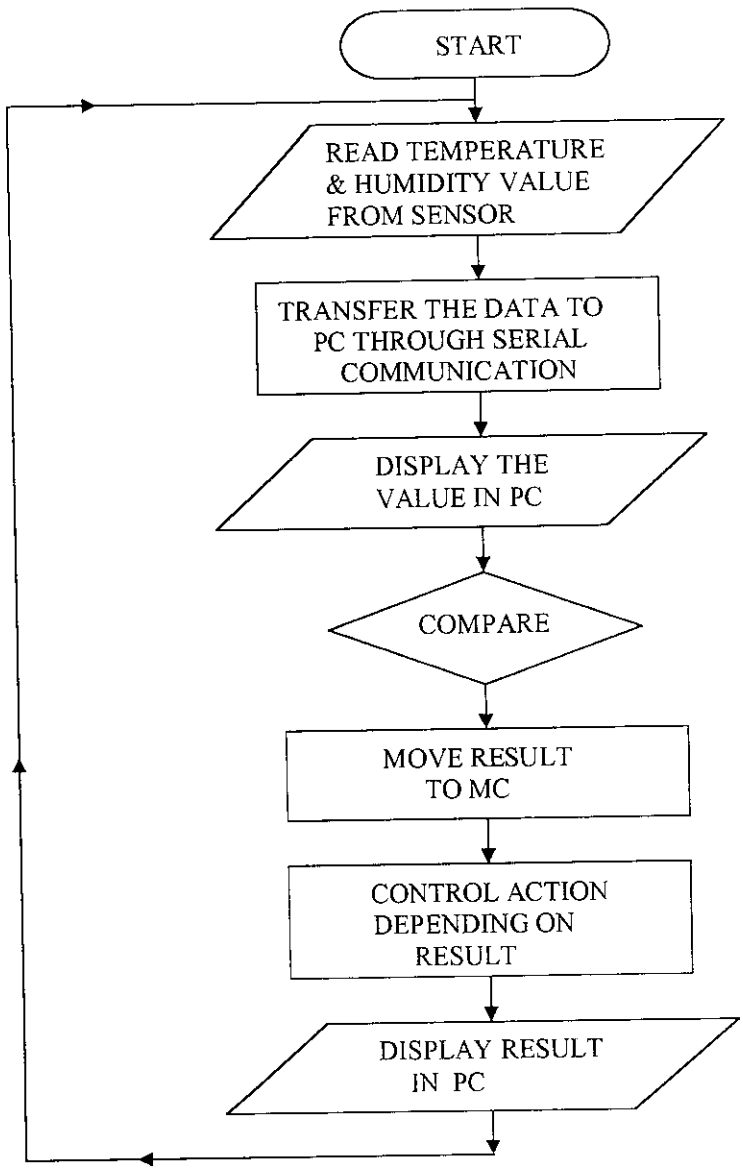
Since monitor and control mechanism are done by manual labor it may lead to variations in accuracy.

Thus the main requirement of an automatic humidity controller is to overcome these setbacks. In an automatic humidity controller continuous monitoring is possible and the control mechanisms are also activated quickly. Since no manual work is involved the controller works with great deal of efficiency.

3.1 BLOCK DIAGRAM



3.2 FLOWCHART



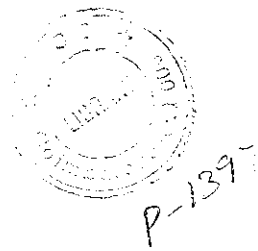
3.3 MEASUREMENT

1. TEMPERATURE MEASUREMENT:

In the process of humidity measurement, temperature measurement also becomes an essential requirement. The higher the temperature of the air the more water vapour it can hold, so relative humidity measurement needs knowledge of the temperature and of the amount of water vapour that the air will hold at various temperatures.

Temperature is the main physical quantity which describes the state of a thermodynamic system. The measurement of temperature is based on the fact that all objects - and consequently also temperature sensors - are exchanging energy with the environment. For an ideal temperature measurement, the temperature sensor and its environment are in thermal equilibrium, there is no energy transfer to or from the sensor. The temperature of the sensor is equal to the temperature of the surroundings.

The temperature can be measured mechanically or electronically. Mechanical methods are based e.g. on bimetal, liquid thermometers or gas thermometers. In the industrial measurement technology the electronic methods are preferred. These are mainly based on the variation of an electrical resistor as function of temperature.



HUMIDITY MEASUREMENT:

Humidity sensing has been the subject of a great deal of study over recent years. The increased use of microelectronics in everyday life means that the importance of sensor technology in general is growing and will continue to do so. Most methods used for measurement of humidity are based on the fact that certain substances change the dimensions with the change in humidity. Apart from this, electrical type humidity transducers are also available and they are more suitable for continuous recording and control of humidity. Depending on the electrical quantity required electrical transducers are available in various types. Whatever may be the type, it should be resistant to irradiation, mechanically strong and chemically stable in the presence of most common contaminants.

3.4 MICROCONTROLLER

A microcontroller is a device that integrates a number of the components of a microprocessor system onto a single microchip. It consists of powerful CPU tightly coupled with memory (RAM, ROM or EPROM), various I/O features such as serial ports, parallel ports, timers /counters, interrupt controller, data acquisition interfaces, analog to digital converters (ADC), digital to analog converters (DAC) everything integrated to a single silicon chip.

Depending upon the need and area of application for which the chip is designed, the on chip features present in it may or may not include all the individual sections mentioned above.

A designer will use a Microcontroller to:

- Gather input from various sensors
- Process this input into a set of actions
- Use the output mechanisms on the Microcontroller to do something useful

Any microcontroller system requires memory to store a sequence of instructions making up a program, parallel port or a serial port for communicating with an external system, timer/counter for generating time delays, apart from the controlling unit called the control processing unit (CPU).

A general purpose Microcontroller is a very powerful tool that allows a designer to create a special purpose design. The design becomes partially hardware and partially software. There is great flexibility in the software end, as the designer can create practically unlimited variations on the design.

ADVANTAGES OF MICROCONTROLLER:

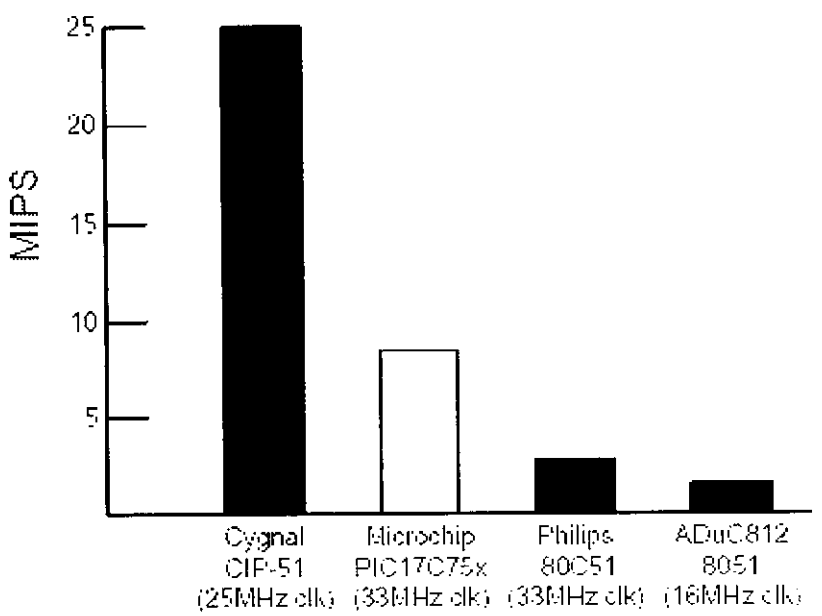
If a system is developed with a microprocessor, the designer will have to go for external memories such as RAM, ROM/EPROM and peripherals and the size of the PCB will be large enough to hold all the required peripherals. But the microcontroller has all these peripheral facilities on a single chip. So, development of a similar system with a microcontroller reduces the PCB size, cost of the design and reduces the number of components.

One of the major differences between the microcontroller and microprocessor is that a controller deals with bits, not with bytes as in the real world applications. For example, switch contacts can only be opened or closed and motors can either be turned ON or OFF.

Microcontroller ports can be used to operate LEDs and relays, as well as input the state of switches and logic circuit inputs (not shown in this figure). Not all microcontroller port outputs are able to drive an LED directly; some need to be interfaced via a buffer such as a 7406 open collector inverting buffer.

In this project the microcontroller employed is ***C8051F020***.

This device is fully integrated mixed-signal System-on-a-Chip with 64 digital I/O pins. Each MCU is specified for 2.7V to 3.6V operation over the industrial temperature range (-45 to +85 degree Celsius). The C8051F020 family utilizes Cygnal's proprietary CIP-51 microcontroller core. The CIP-51 employs a pipelined architecture that greatly increased its instruction throughput over the standard 8051 architecture. It has a total of 109 instructions. With the CIP-51's maximum system clock at 25MHz, it has a peak throughput of 25 MIPS. The below figure shows a comparison of peak throughputs of various 8-bit microcontroller cores with their maximum system clocks.



3.5 CONTROL MECHANISM:

Control mechanism employs relay circuits. Relays are EM devices by which operation of one or more circuits are controlled by the operation of some other circuits. Relays are provided with some mechanical contacts and with their help they control the operation of other circuits. Relay consists of core and the coil is wounded over the core. When the current is passed, coil is energized and the core is magnetized. The armature placed near the core is attached to it and the contact is made. When the electricity is removed demagnetization of core occurs and the contact is removed.

Relay has three states

- NO
- NC
- Common

According to the result obtained in the microcontroller after comparison the relays are activated to obtain the required control action. The control action may be -switching on the motor for fans and dampers or switching off the already running motors depending on whether the humidity is low or high. In this project we make use of DP57 series relay.

3.6 SERIAL COMMUNICATION:

Serial Communication is of two types – Synchronous serial communication and asynchronous serial communication. In this project asynchronous serial communication has been employed.

ASYNCHRONOUS SERIAL COMMUNICATION:

Asynchronous communication requires nothing more than a transmitter, a receiver and a wire. It is thus the simplest of serial communication protocols, and the least expensive to implement. asynchronous communication is performed between two (or more) devices which operate on independent clocks.

In asynchronous communication, data is preceded with a start bit which indicates to the receiver that a word (a chunk of data broken up into individual bits) is about to begin. To avoid confusion with other bits, the start bit is twice the size of any other bit in the transmission. The end of a word is followed by a stop bit, which tells the receiver that the word has come to an end, that it should begin looking for the next start bit, and that any bits it receives before getting the start bit should be ignored. To insure data integrity, a parity bit is often added between the last bit of data and the stop bit. The parity bit makes sure that the data received is composed of the same number of bits in the same order in which they were sent.

At the heart of every asynchronous serial system is the Universal Asynchronous Receiver/Transmitter or UART. The UART is responsible for implementing the asynchronous communication process described above as both a transmitter and a receiver (both encoding and decoding data frames). The UART not only controls the transfer of data, but the speed at which communication takes place

Serial communication here is done through a standard nine pin RS – 232 cable using MAX-232.

3.7 DISPLAY IN PC

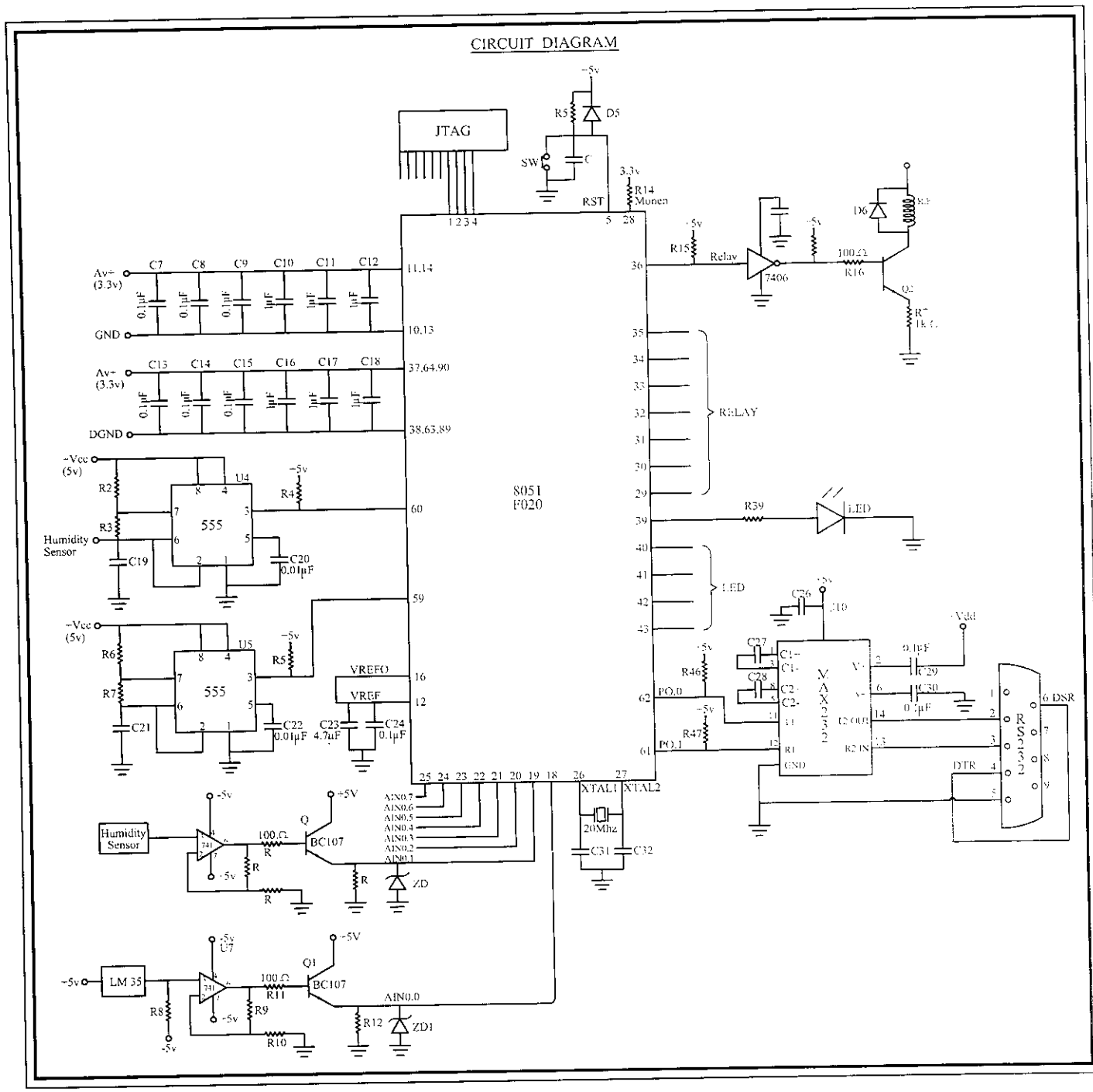
PC is used to perform two operations – comparison and display. Among these two, PC plays a very vital role in displaying the necessary information to the user. The displayed information include:

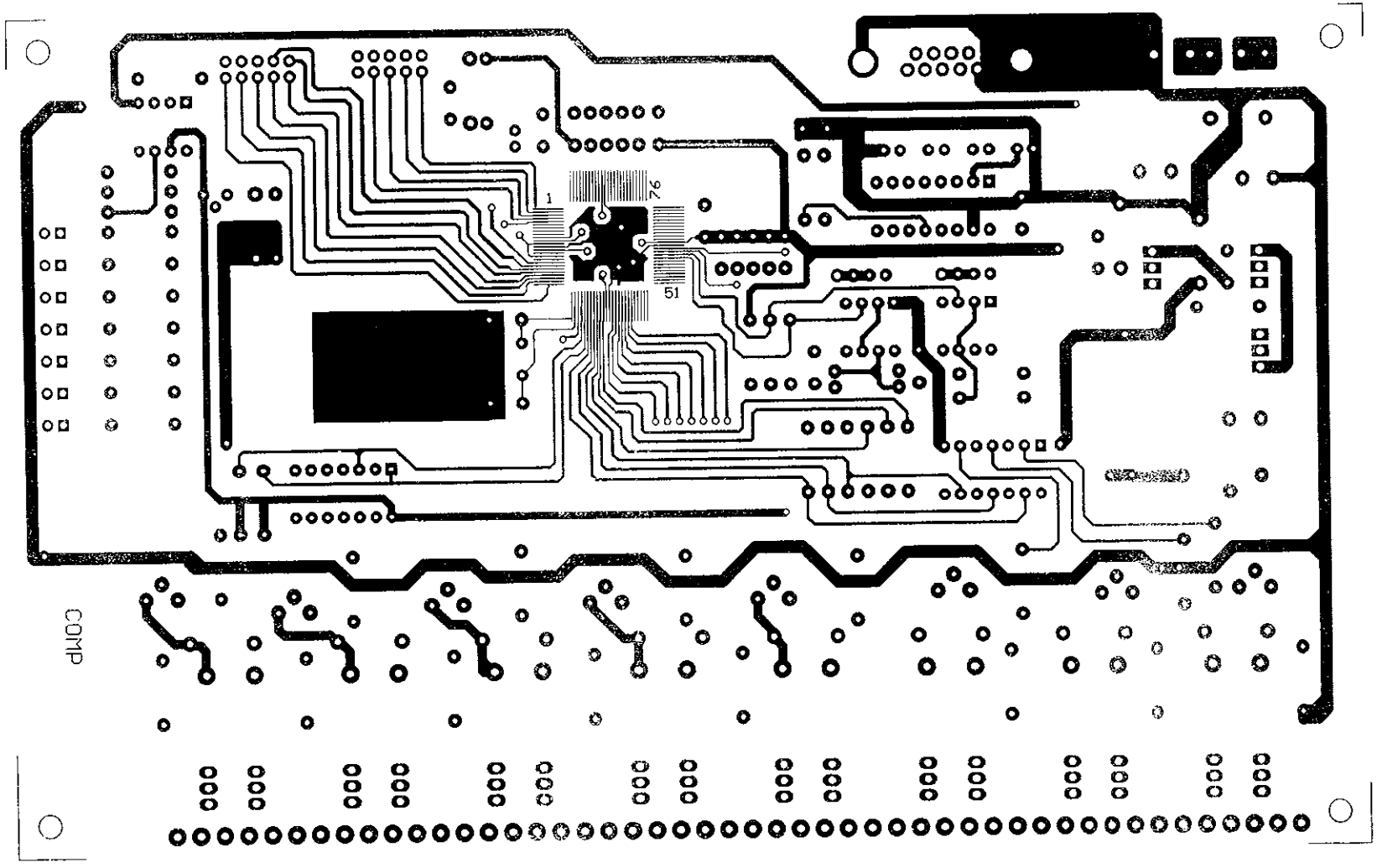
- Humidity range to be maintained
- Sensed humidity and temperature values
- Controlling action

While the first information is user interactive the data for the rest is exchanged between the PC and microcontroller using serial communication techniques.

This is programmed in 'C' language and the DOS mode serves as the screen.

CIRCUIT DIAGRAM





VIEW FROM COMP SIDE SIZE = 8.5 X 5.225 (132.7 X 215.9 MM)

VIEW FROM COMP SIDE SIZE = 8.8 X 5.522 (133.7 X 212.8 MM)

5.1 POWER SUPPLY

Many discrete and IC circuits require bipolar supplies. This is done with two three-terminal regulators.

The schematic diagram of the dual power supply provides an output voltage of +5V and –5V. Regulated power supply consists of

- Transformer
- Rectifier
- Filter
- Regulator

TRANSFORMER:

It is used to step up and step down the voltage. In this project a step down transformer is utilized. The AC voltage of 230V is stepped down to 12V in the output side of the transformer.

RECTIFIER:

A device that is capable of converting the sinusoidal input waveform into unidirectional waveforms with non-zero average component is called Rectifier.

Rectifiers are of two types:

- Half wave rectifier
- Full wave rectifier

FULL WAVE RECTIFIER:

Diode D1 and D2 constitute a full wave rectifier. Diode D1 conducts on the positive half cycle and diode D2 conducts on the negative half cycle. As a result, the rectified load current flows during both half cycles. The circuit is called a full wave rectifier because it has changed the both cycles of ac input voltage to the pulsating dc output voltage.

FILTERS:

Filters used are capacitors. Shunting the load with capacitor frequently affects filtering. The action of this system depends upon the fact that the capacitors store energy during the conducting period. In this way the time during which the current passes through the load and the ripple is considerably decreased. The ripple voltage is defined as the deviation for the load voltage from its average or DC value.

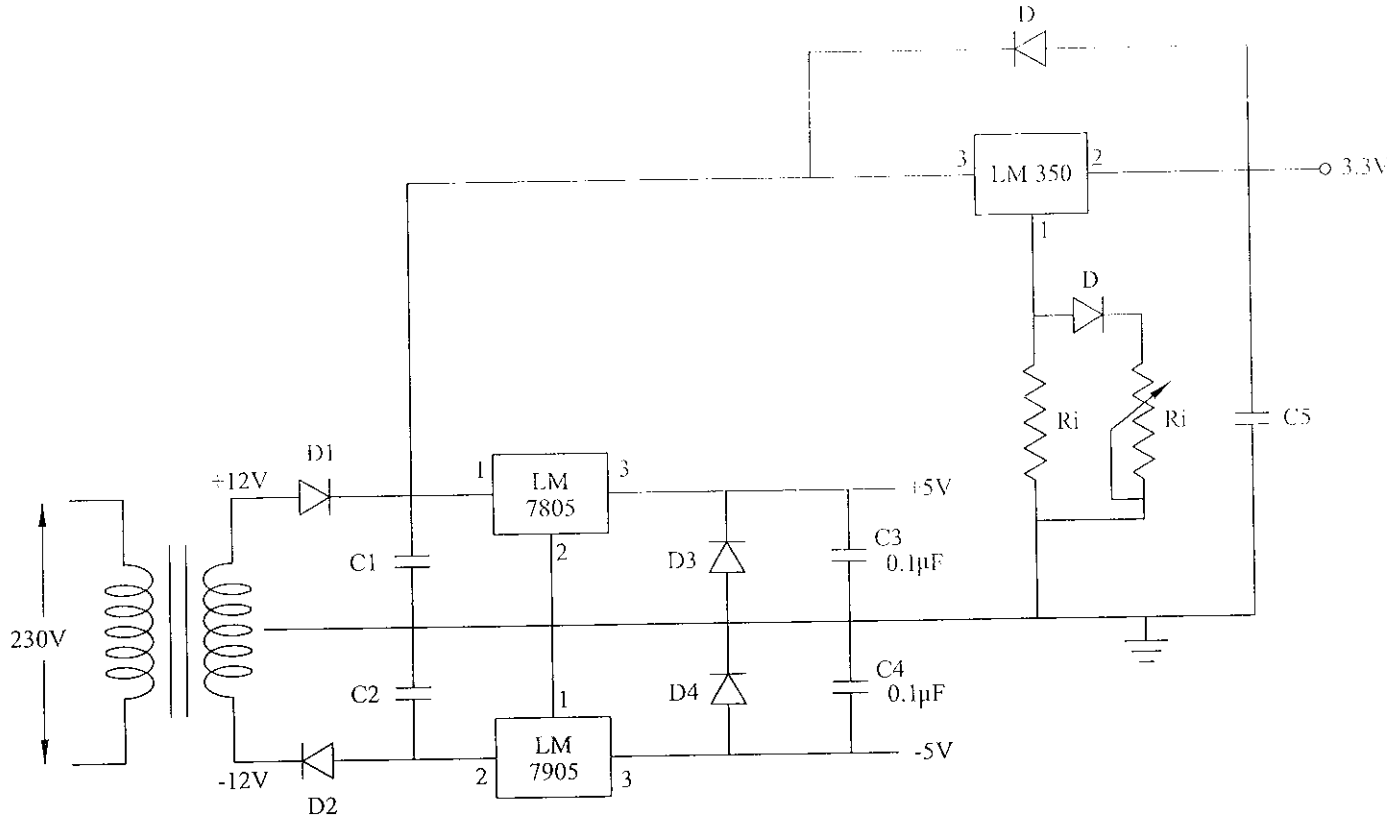
VOLTAGE REGULATOR:

A voltage regulator supplies a constant voltage regardless of changes in load currents. IC voltage regulators are versatile and inexpensive. The 7800 series consists of three terminals. The LM7805 voltage regulator is simple to use. Connect the positive lead of the unregulated DC power supply (anything from 9VDC to 24VDC) to the Input pin, connect the negative lead to the Common pin and then when power is turned on, a 5 volt supply from the Output pin is got. Similarly the negative supply is regulated by LM7905.

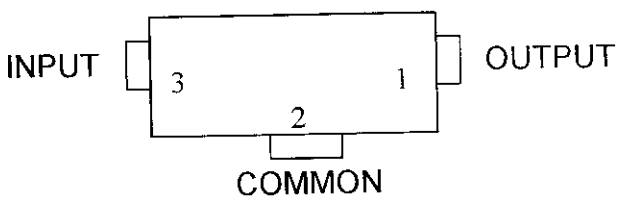
Diodes D3 and D4 provide protection against the situation when both the regulators may not turn on simultaneously. If there is a load between the two outputs, the faster one will try to reverse the polarity of the other and cause it to latch up unless it is properly clamped. This clamping function is done by the diodes. Once the regulator start operating properly, both diodes will be reverse biased and will no longer have any effect on the circuit.

Apart from the dual supply, a positive supply of 3.3V is required for many circuits. This is simultaneously obtained from the same power supply circuit using IC LM350.The LM350 is an adjustable three-terminal positive voltage regulator capable of supplying in excess of 3V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow-out proof.

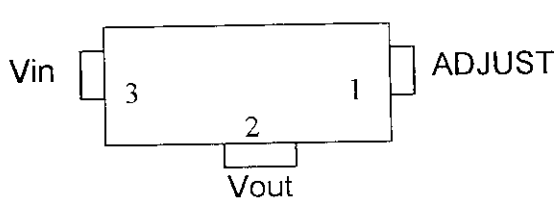
POWER SUPPLY



LM7805



LM350



5.2 TEMPERATURE SENSOR

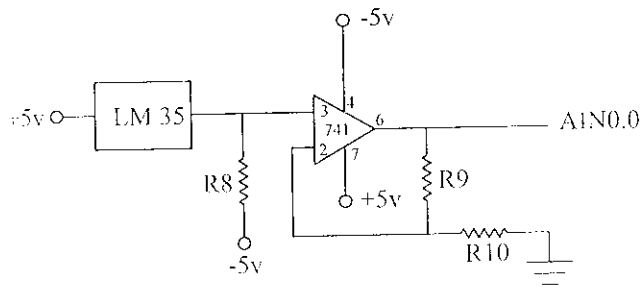
The LM35 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM35 thus has an advantage over linear temperature sensors calibrated in ° Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Centigrade scaling. The LM35 does not require any external calibration or trimming to provide typical accuracies of ±¼°C at room temperature and ±¾°C over a full -55 to +150°C temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM35's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies, or with plus and minus supplies. As it draws only 60 µA from its supply, it has very low self-heating, less than 0.1°C in still air. The LM35 is rated to operate over a -55° to +150°C temperature range, while the LM35C is rated for a -40° to +110°C range (-10° with improved accuracy). The LM35 series is available packaged in hermetic TO-46 transistor packages.

FEATURES:

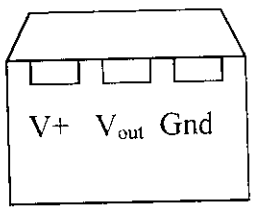
- Calibrated directly in ° Celsius (Centigrade)
- Linear + 10.0 mV/°C scale factor
- 0.5°C accuracy guaranteeable (at +25°C)
- Rated for full -55° to +150°C range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 4 to 30 volts
- Less than 60 μA current drain
- Low self-heating, 0.08°C in still air
- Nonlinearity only ±¼°C typical
- Low impedance output, 0.1 Ohm for 1 mA load

AMPLIFIER:

The output from the temperature sensor is amplified using IC 741 in non-inverting mode. The amplifying factor depends on the value of resistors R2 and R3. IC741 is an eight-pin IC requiring dual supply voltage. The voltage may range from about +/-5V to +/-22V.

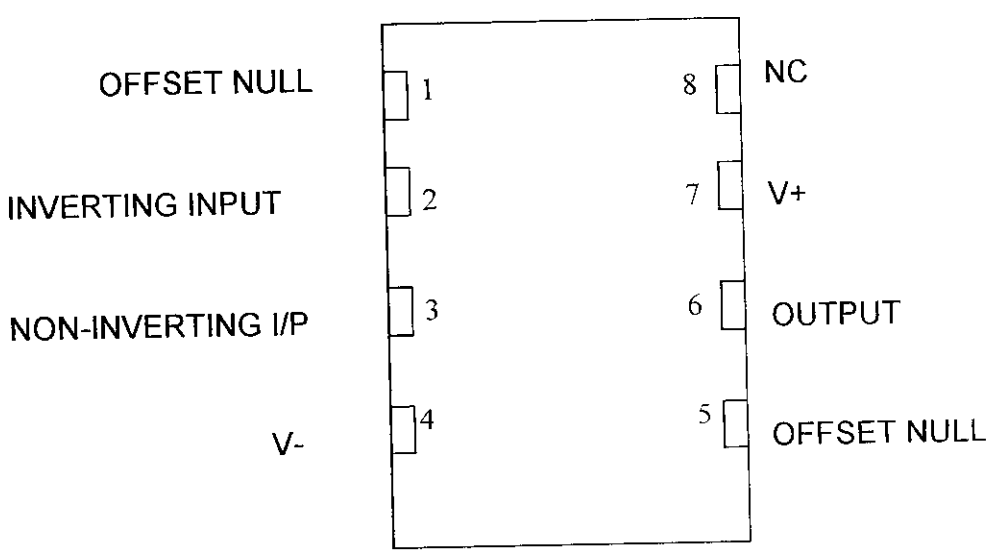

-5v
+5v
LM 35
741
3
2
4
7
6
A1N0.0
R8
R9
R10
+5v
-5v

LM35



T0 – 92 plastic package

IC 741



5.3 HUMIDITY SENSOR

The humidity sensor employed here is HUMITHERM-842M. It is a highly sophisticated, accurate and reliable instrument to give the value of relative humidity. It is an extremely reliable thermohygrometer that uses a polymeric humidity sensor, developed specially to detect relative humidity. These instruments are compact in size and can be easily fitted into control panels.

SPECIFICATION:

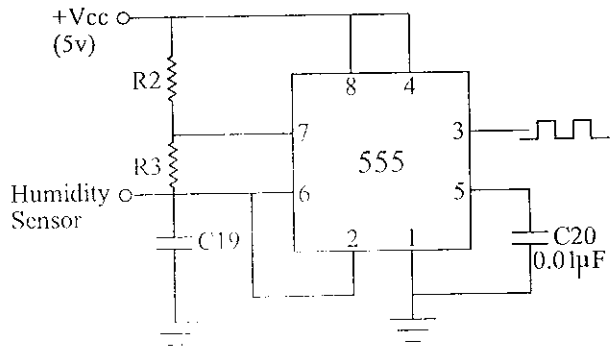
- ✓ Range : 20% to99% RH
- ✓ Accuracy : -2% to +2% at 25 degree Celsius
- ✓ Sampling rate: 3 samples per second
- ✓ Power supply: 230v, 50 Hz, single phase, AC mains
- ✓ Construction : metallic with plastic Bezel
- ✓ Weight : 2 kg

FREQUENCY GENERATION:

Apart from a direct humidity sensor there is provision for a capacitive humidity sensor. According to the availability any one can be used. In a capacitive humidity sensor, change in humidity is reflected as change in capacitance. This is then converted to frequency using a 555timer circuit.

The frequency generation circuit generates frequency based on the capacitance value present in the circuit. The capacitive humidity transducer is kept in parallel to the capacitanceC1. Any change in the capacitance will be reflected to the circuit frequency. The input to the frequency generator circuit is through this transducer. The changes in capacitance, due to dielectric variation the frequency varies and act as a control signal to the microcontroller.

The pin 3 is the output from which the frequency is given to the microcontroller. The resistance and capacitance values are chosen depending upon the frequency range required. By changing the resistance R3 and R2 the square wave can be achieved.

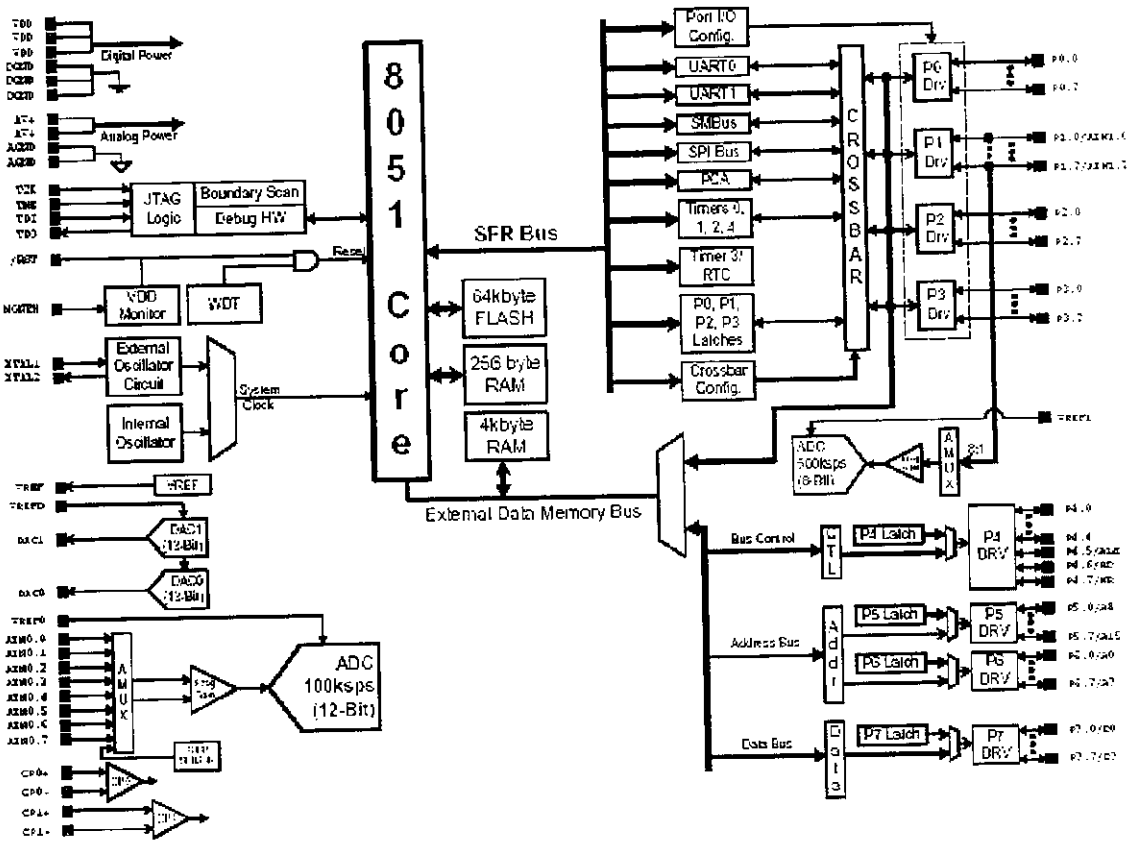

+Vcc
(5v)
R2
R3
Humidity
Sensor
C19
8
4
7
3
555
6
5
2
1
C20
0.01μF

5.4 MICROCONTROLLER C8051F020

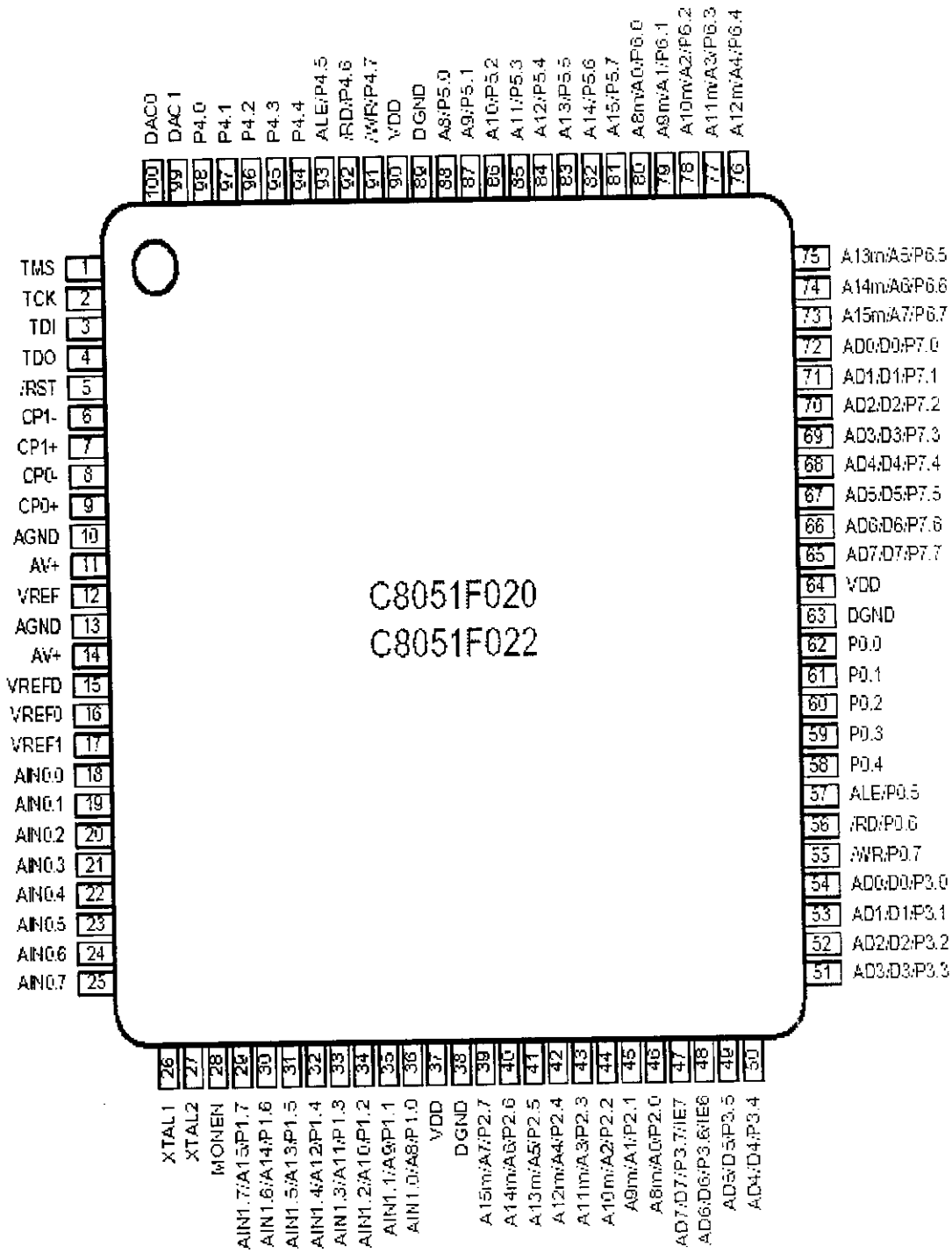
FEATURES:

- High-Speed pipelined 8051-compatible CIP-51 microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- True 12-bit (C8051F020/1) or 10-bit (C8051F022/3) 100 ksps 8-channel ADC with PGA and analog multiplexer
- True 8-bit ADC 500 ksps 8-channel ADC with PGA and analog multiplexer
- Two 12-bit DACs with programmable update scheduling
- 64k bytes of in-system programmable FLASH memory
- 4352 (4096 + 256) bytes of on-chip RAM
- External Data Memory Interface with 64k byte address space
- SPI, SMBus/I2C, and (2) UART serial interfaces implemented in hardware
- Five general purpose 16-bit Timers
- Programmable Counter/Timer Array with five capture/compare modules
- On-chip Watchdog Timer, VDD Monitor, and Temperature Sensor

C8051F020 BLOCK DIAGRAM



PINOUT DIAGRAM

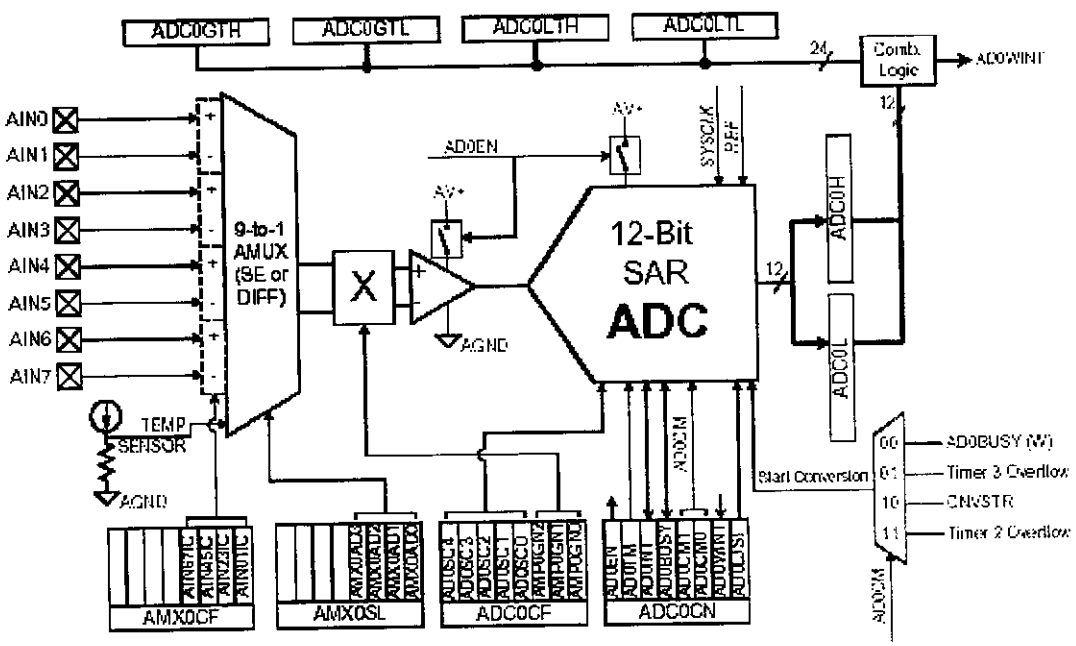


ADC (12-BIT):

The ADC0 subsystem consists of:

- 9 – channel
- configurable analog multiplexer
- programmable gain amplifier
- 12-bit successive approximation register

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION:

Eight of the AMUX channels are available for external measurements while the ninth channel is internally connected to an on-chip temperature sensor. AMUX input pairs can be programmed to operate in either differential or single-ended mode. This allows the user to select the best measurement technique for each input channel, and even accommodates mode changes "on-the-fly". The AMUX defaults to all single-ended inputs upon reset. The PGA amplifies the AMUX output signal can be determined through suitable programming in the ADC0 configuration register.it can be software-programmed for gains of 0.5,2,4,6,8 or 16. Gain defaults to unity on reset.

UART:

UART0 is an enhanced serial port with frame error detection and address recognition hardware. UART0 may operate in full-duplex asynchronous or half-duplex synchronous modes, and multiprocessor communication is fully supported. Receive data is buffered in a holding register, allowing UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte. A Receive Overrun bit indicates when new received data is latched into the receive buffer before the previous received byte is read.

UART0 is accessed via its associated SFRs, Serial Control (SCON0) and Serial Data Buffer (SBUF0). The single SBUF0 location provides access to both transmit and receive registers. Reads access the Receive register and writes access the Transmit register automatically. UART0 may be operated in polled or interrupt mode. UART0 has two sources of interrupts: a Transmit Interrupt flag, TI0 (SCON0.1) set when transmission of a data byte is complete, and a Receive Interrupt flag, RI0 (SCON0.0) set when reception of a data byte is complete. UART0 interrupt flags are not cleared by hardware when the CPU vectors to the interrupt service routine; they must be cleared manually by software. This allows software to determine the cause of the UART0 interrupt (transmit complete or receive complete).

EXTERNAL OSCILLATOR:

A crystal is used as an external oscillator source for the microcontroller unit. The crystal here uses 18.432MHz. In the microcontroller the Crystal Valid Flag is set to logic 1 by hardware when the external crystal oscillator is running and stable. This detection circuit requires a startup time of at least 1ms. Crystal oscillators require quite sensitive PCB layout. The crystal should be placed as close as possible to the XTAL pins on the device, as should the loading capacitors on the crystal pins.

RESET SOURCE:

Reset circuitry allows the controller to be placed in a predefined default condition. On entry to this reset state the following occur – CIP-51 halts program execution, SFRs are initialized to their defined reset values, External port pins are forced to a known state, Interrupts and timers are disabled. There are seven sources for putting the MCU into the reset state.Here EXTERNAL RESET is used. The RST pin is for external reset. Asserting the RST pin low will cause the MCU to enter the reset state. It is desirable to provide an external pull-up to avoid noise-induced resets. The MCU will remain in reset until at least 12 clock cycles after the active low RST signal is removed.

5.5 57DP RELAY

- Power Relay
- CSA Approved
- Style: PC
- Contact:1C/ 2C
- Rating : 6 / 2 A at 24 VDC/230 VAC

SPECIFICATIONS:

Enclosures	:	Polycarbonate
Contact forms	:	A,B or C
Contact arrangement	:	1pole & 2pole
Contact material	:	Silver cadmium oxide
Life expectancy:Mechanical	:	10^6 operations
Ambient temperature	:	-40 to 65 degree centigrade
Dielectic strength	:	750 volts RMS
Max. operation time	:	0.012 sec
Max. release time	:	0.008 sec
Coil dissipation	:	1.5W
Sensitivity	:	0.75W

The above specified relay will control another relay which in turn controls the motor action. The motor in the concerned Textile mill has the following specification.

FAN MOTOR:

SUPPLY	:	415V,50Hz
POWER RATING	:	5.5Kw
CURRENT RATING	:	11 A
SPEED	:	1,400 rpm

PUMPING MOTOR:

POWER RATING	:	5.5kw, 7.5hp
CURRENT RATING	:	11.4 A
SPEED	:	2,800 rpm

5.6 RS-232

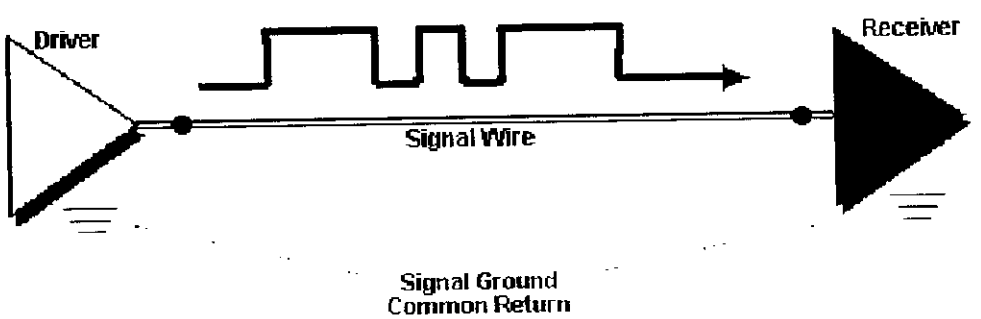
RS-232 stands for Recommend Standard number 232 and C is the latest revision of the standard. The serial ports on most computers use a subset of the RS-232C standard. It sends and receives data using twisted pair cable. The full RS-232C standard specifies a 25-pin "D" connector of which 22 pins are used. Most of these pins are not needed for normal PC communications, and indeed, most new PCs are equipped with male D type connectors having only nine pins.

Pin Number	Direction of signal:
1	Carrier Detect (CD) (from DCE) Incoming signal from a modem
2	Received Data (RD) Incoming Data from a DCE
3	Transmitted Data (TD) Outgoing Data to a DCE
4	Data Terminal Ready (DTR) Outgoing handshaking signal
5	Signal Ground Common reference voltage
6	Data Set Ready (DSR) Incoming handshaking signal
7	Request To Send (RTS) Outgoing flow control signal
8	Clear To Send (CTS) Incoming flow control signal
9	Ring Indicator (RI) (from DCE) Incoming signal from a modem

RS-232 uses an unbalanced signal communication method. That is, there is one signal wire for each circuit with a common return for all signals. This method is somewhat susceptible to electrical noise.

To communicate, the device sends a series of binary signals to the receiver. These binary pulses make up predefined words that indicate either control commands or status conditions.

The RS-232 communication standard supports only one transmitter driver and a receiver. Distance is limited to 50 feet.



5.7 MAX 232

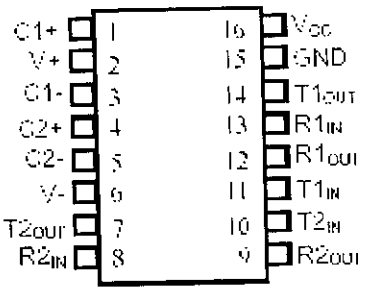
FEATURES:

- High data rate - 250 kbits/sec under load
- 16-pin DIP or SOIC package
- 20-pin TSSOP package for height restricted applications
- Operate from single +5V power
- Meets all EIA-232E and V0.28 specifications
- Uses small capacitors: 0.1 □F
- Optional industrial temperature range available (-40□C to +85□C)

DESCRIPTION:

The MAX232 is a dual RS-232 driver/receiver pair that generates RS-232 voltage levels from a single +5-volt power supply. Additional □12-volt supplies are not needed since the MAX232 uses on-board charge pumps to convert the +5-volt supply to □10 volts. The MAX232 is fully compliant with EIA RS-232E andV0.28/V0.24 standards. The MAX232 contains two drivers and two receivers. Driver slew rates and data rates are guaranteed up to 250k bits/sec. The MAX232 operates with only 0.1 microF charge pump capacitors.

PIN CONFIGURATION:



16-Pin DIP AND SOIC

PIN DESCRIPTION:

VCC	-	+5-Volt Supply
GND	-	Ground
V+	-	Positive Supply Output
V-	-	Negative Supply Output
T1IN, T2IN	-	RS-232 Driver Inputs
T1OUT, T2OUT	-	RS-232 Driver Outputs
R1IN, R2IN	-	Receiver Inputs
R1OUT, R2OUT	-	Receiver Outputs
C1+, C1-	-	Capacitor 1 Connections
C2+, C2-	-	Capacitor 2 Connections

PIN DESCRIPTIONS:

VCC, GND: DC power is provided to the device on these pins. VCC is the +5-volt input.

V+: Positive supply output (RS-232). V+ requires an external storage charge capacitor of at least 0.1 microF. A larger capacitor (up to 10 microF) can be used to reduce supply ripple.

V-: Negative supply output (RS-232). V- requires an external storage capacitor of at least 0.1 microF. A larger capacitor (up to 10 microF) can be used to reduce supply ripple.

T1IN, T2 IN: Standard TTL/CMOS inputs for the RS-232 drivers. The inputs of unused drivers can be left unconnected since each input has a 400kΩ pull-up resistor.

T1OUT, T2 OUT: Driver outputs at RS-232 levels. Driver output swing meets RS-232 levels for loads up to 3 kΩ These driver outputs provide current necessary to meet RS-232 levels for loads up to 2500 pF.

R1 IN, R2 IN: Receiver inputs. These inputs accept RS-232 level signals (±25 volts) into a protected 5 kΩ terminating resistor. Each receiver provides 0.5V hysteresis (typical) for noise immunity.

R1 OUT, R2 OUT: Receiver outputs at TTL/CMOS levels.

C1+, C1-, C2+, C2-: Charge pump capacitor inputs. These pins require two external capacitors (0.1 microF minimum, 10 microF maximum and should be the

same size as C3 and C4). Capacitor 1 is connected between C1+ and C1-. Capacitor 2 is connected between C2+ and C2-. Capacitor C1 can be omitted if +12 volts is connected directly to V+. Likewise, C2 can be omitted if -12V is connected directly to V-.

DUAL CHARGE PUMP CONVERTERS

The DS232A has a two-stage on-board charge pump circuit that is used to generate □10 volts from a single +5-volt supply. In the first stage, capacitor C1 doubles the +5V supply to +10 volts which is then stored on capacitor C3. The second stage uses capacitor C2 to invert the +10V potential to -10V. This charge is then stored on capacitor C4. The □10-volt supplies allow the DS232A to provide the necessary output levels for RS-232 communication. The DS232A will operate with charge pump capacitors as low as 0.1 □F. Larger capacitors (up to 10 □F) can be used to reduce supply ripple.

RS-232 DRIVERS

The two RS-232 drivers are powered by the internal □10-volt supplies generated by the on-board charge pump. The driver inputs are both TTL and CMOS compatible. Each input has an internal 400 k□ pullup resistor so that unused transmitter inputs can be left unconnected. The open circuit output voltage swing is from (V+ - 0.6) to V- volts. Worst case conditions for EIA-232E/V.28 of □5-volt driving a 3 k□ load and 2500 pF are met at maximum

operating temperature and VCC equal to 4.5 volts. Typical voltage swings of +/-8 volts occur when loaded with a nominal 5 k=RS-232 receiver. As required by EIA-232E and V.28 specifications, the slew rate at the output is limited to less than 30 volts/s. Typical slew rates are 20 volts/s unloaded and 12 volts/s with 3 k=and 2500pF load. These slew rates allow for bit rates of over 250k bits/s. Driver outputs maintain high impedance when power is off.

RS-232 RECEIVERS

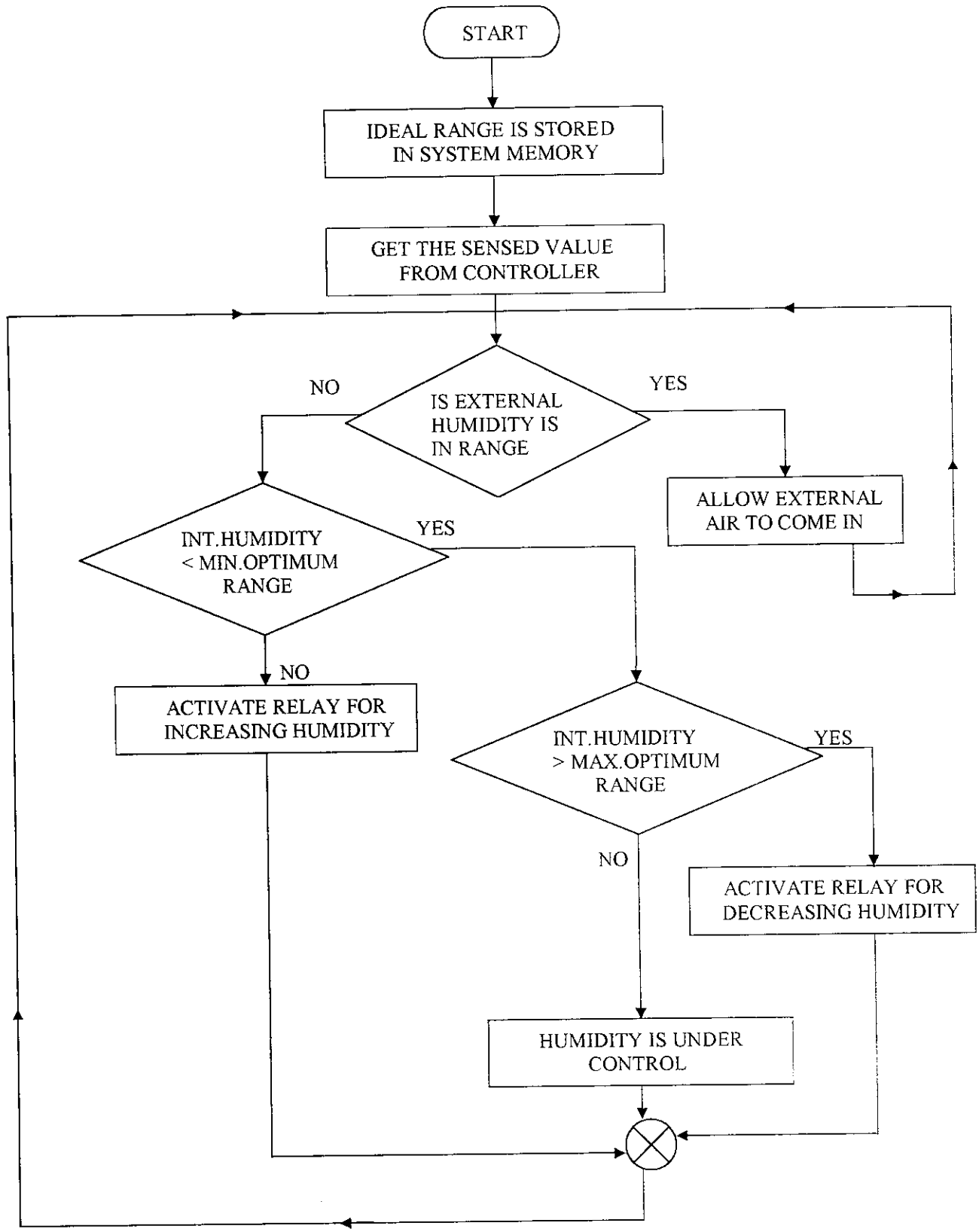
The two receivers conform fully to the RS-232E specifications. The input impedance is typically 5k=and can withstand up to =25 volts with or without VCC applied. The input switching thresholds are within the =3-volt limit of RS-232E specification with an input threshold low of 0.8 volts and an input threshold high of 2.4 volts. The receivers have 0.5 volts of hysteresis (typical) to improve noise rejection. The TTL/CMOS compatible outputs of the receivers will be low whenever the RS-232 input is greater than 2.4 volts. The receiver output will be high when the input is floating or driven between +0.8 volts and -25 volts.

6.1 PROGRAMMING ASPECTS

'C'-An Insight

The software was programmed in Microchip's version of 'C'. 'C' was preferred as the development medium due to its wide popularity, ease of use as compared to assembly language, good programming constructs, rich reference language, rich reference sources, high performance and it offers very good hardware interaction due to its close relationship with assembly language. Summing it up, it offers the best of both low level assembly language, by providing raw programming power of assembly language and the understandable programming style of high level languages. By suitably changing the compiler options, the same 'C' code can be easily ported to different microcontrollers by making little or no changes in the source code.

6.2 FLOWCHART



6.3 MICROCONTROLLER CODING

```
# include<c8051f020.h>
# include<stdio.h>

// 16 bit SFR definitions

# define BAUDRATE 9600
# define SYSCLK    20000000

// function prototypes

void SYSCLK_init(void);
void PORT_init(void);
void UART0_init(void);
void ADC0_init(void);
void ADC01_complete(void);
void ADC01_enable(void);
```

```
// main routine
void main(void)
{
WDTCN = 0xde;
WDTCN = 0xad;

SYSCLK_init();
Port_init();
UART0_init();
ADC01_init();
ADC0_enable();
ADC0_complete();

ADC02_init();
ADC0_enable();
ADC0_complete();

ADC03_init();
ADC0_enable();
ADC0_complete();
```

```
While(IRI) {}
Tempr = SUBF0;
PRT2 = 0X00;
PRT3 = 0X00;
}

void ADC0_init(void)
{
     ADC0CN = 0X10;
     REF0CN = 0X03;
     AMX0SL = 0X00;
     ADC0CF = 0X80;
  }

 void ADC0_enable(void)
  {
       ADC0CN1 = 0X90;
   }

  void ADC0_complete(void)
```

```
{
            while(AD0BUY)
            {}
             ADC0H = Temp;
             ADC0L = Temp;
             SBUF0 = ADC0H;
             While(!TI0)
               TI = 0;
             SBUF0 = ADC0L;
             While(!TI0);
               TI = 0;
          }


    void SYSCLK_init(void)
         {
              inti;
              OSCXCN = 0X67;
              For(I=0;I<256;I++);
              While(!(OSCXCN & 0X85));
              OSC1CN = 0X88;
         }
```

```
void Port_init(void)
     {
          XBR0 = 0X04;
          XBR1 = 0X00;
          XBR2 = 0X40;
          PRT0CF1 = 01;
          PRT2CF1 = 01;
          PRT3CF1 = 01;
     }

void UART_init(void)
     {
          SCON = 0X50;
          TMOD = 0X20;
          TH1 = 256-(SYSCLK/BAUDRATE/16);
          TR1 = 1;
          CKCON1 = 0X10;
          PCON1 = 0X80;
     }
```

6.4 PC PROGRAMMING

```
# include<dos.h>
# include<stdio.h>
# include<conio.h>
# define PORT1 0x3F8

void main(void)
{
int c,q;
float setma,setmin;
int state;
int ch1[7],ch[7];
int i=0; int x=0;
clrscr();
outportb(PORT1+1,0);
outportb(PORT1+3,0x80);
outportb(PORT1+0,0x0c);
outportb(PORT1+1,0x00);
outportb(PORT1+3,0x03);
outportb(PORT1+2,0xc7);
outportb(PORT1+4,0x0b);
```

```
printf("ENTER THE MAX & MIN VALUES");
printf("\n**************************");
printf("\n");
scanf("%f %f",&setma,&setmin);
clrscr();

do
{
clrscr();
printf("THE CURRENT HUMIDITY RANGE %f \t
%f",setma,setmin);
printf("\n\nDO U WANT TO CHANGE? \n IF YES PRESS
'1' ELSE PRESS '2'");
if (kbhit())

if(getch()=='1')
 {
  clrscr();
  printf("ENTER THE MAX & MIN VALUES");
  printf("\n**************************");
  printf("\n");
```

```
  scanf("%f %f",&setma,&setmin);
  goto s;
  }
else
s:
 do
 {
   c=inportb(PORT1+5);

 if (c&1)
    {
    ch[i]=inportb(PORT1);
    }
    i++;
   }while(i<=5);
   ch[0]=ch[0]<<4+ch[1];
   ch[2]=ch[2]<<4+ch[3];
   ch[4]=ch[4]<<4+ch[5];
   ch1[0]=(ch[0]*2.4)/(4096*40);
   printf("\n\n\n\n\t\tTEMPERATURE IN DEGREES\t
  %f",ch1[0]);
```

```
  ch1[2]=(ch[2]*2.4)/4096;
  printf("\n\n\t\tEXTERNAL HUMIDITY\t
%f",ch1[2]);
  ch1[4]=(ch[4]*2.4)/4096;
  printf("\n\n\t\tINTERNAL HUMIDITY\t
%f",ch1[4]);delay(1000);
  int eh;
  if((ch[2]>setmin)&&(ch[2]<setma))
  {
  eh = 0xA9;
  outportb(PORT1,eh);
  printf("\n\n\n \t ALLOW EXTERNAL HUMIDITY
 INSIDE");
  printf("\n \t ------------------------------");
  delay(1000);
  }
  else if(ch[4]<setmin)
  {
   eh=0x96;
   outportb(PORT1,eh);
```



```
   printf("\n\n\n \t HUMIDITY IS LOW");
```

```
    printf("\n \t ---------------");
    printf("\n\t\t\tcontrolling...");
    delay(1000);
    }
    else if(ch[4]>setma)
    {
    eh=0x64;
    outportb(PORT1,eh);
    printf("\n\n\n \t HUMIDITY IS HIGH");
    printf("\n \t ----------------");
    printf("\n\t\t\tcontrolling...");
    delay(1000);
    }
else
    {
    printf("\n\n\n \t HUMIDITY IS CONTROLLED");
    printf("\n \t ----------------------");
    delay(1000);}
    }while(x==0);
     getch();
   }
```

CONCLUSION:

This project provides the advantage of improving the quality of product (yarn) manufactured. The manual process involved as been automated.

The automatic humidity controller gives the methods for efficient maintenance of humidity in the industry. Continuous monitoring and controlling has been achieved.

This project can be further developed by the inclusion of additional features like storing data, drawing graphs between previous data and present data and then comparing them for better production.

PRELIMINARY

C8051F020/1/2/3

Mixed-Signal ISP FLASH MCU Family

ANALOG PERIPHERALS

- **SAR ADC**
  - 12-Bit (C8051F020/1)
  - 10-Bit (C8051F022/3)
  - ± 1 LSB INL
  - Programmable Throughput up to 100 ksps
  - Up to 8 External Inputs; Programmable as Single-Ended or Differential
  - Programmable Amplifier Gain: 16, 8, 4, 2, 1, 0.5
  - Data-Dependent Windowed Interrupt Generator
  - Built-in Temperature Sensor (± 3°C)
- **8-bit ADC**
  - Programmable Throughput up to 500 ksps
  - 8 External Inputs
  - Programmable Amplifier Gain: 4, 2, 1, 0.5
- **Two 12-bit DACs**
  - Can Synchronize Outputs to Timers for Jitter-Free Waveform Generation
- **Two Analog Comparators**
- **Voltage Reference**
- **Precision VDD Monitor/Brown-Out Detector**

ON-CHIP JTAG DEBUG & BOUNDARY SCAN

- On-Chip Debug Circuitry Facilitates Full- Speed, Non-Intrusive In-Circuit/In-System Debugging
- Provides Breakpoints, Single-Stepping, Watchpoints, Stack Monitor; Inspect/Modify Memory and Registers
- Superior Performance to Emulation Systems Using ICE-Chips, Target Pods, and Sockets
- IEEE1149.1 Compliant Boundary Scan
- Low-Cost, **Complete** Development Kit

HIGH SPEED 8051 µC CORE

- Pipelined Instruction Architecture; Executes 70% of Instruction Set in 1 or 2 System Clocks
- Up to 25 MIPS Throughput with 25 MHz Clock
- 22 Vectored Interrupt Sources

MEMORY

- 4352 Bytes Internal Data RAM (4k + 256)
- 64k Bytes FLASH; In-System programmable in 512-byte Sectors
- External 64k Byte Data Memory Interface (programmable multiplexed or non-multiplexed modes)

DIGITAL PERIPHERALS

- 8 Byte-Wide Port I/O (C8051F020/2); 5V tolerant
- 4 Byte-Wide Port I/O (C8051F021/3); 5V tolerant
- Hardware SMBus™ (I^2C™ Compatible), SPI™, and Two UART Serial Ports Available Concurrently
- Programmable 16-bit Counter/Timer Array with 5 Capture/Compare Modules
- 5 General Purpose 16-bit Counter/Timers
- Dedicated Watch-Dog Timer; Bi-directional Reset Pin

CLOCK SOURCES

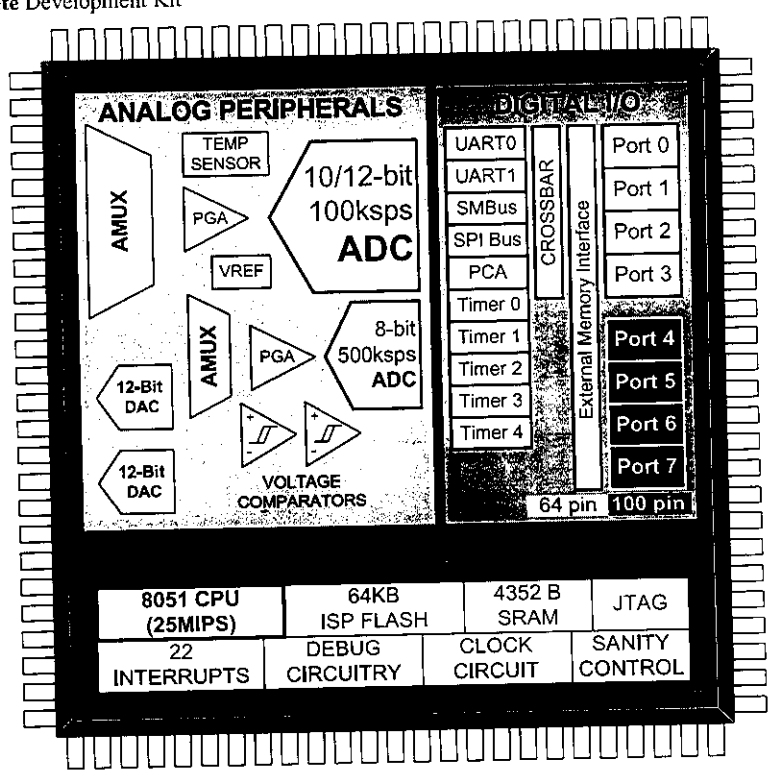
- Internal Programmable Oscillator: 2-to-16 MHz
- External Oscillator: Crystal, RC, C, or Clock
- Real-Time Clock Mode using Timer 3 or PCA

SUPPLY VOLTAGE ..... 2.7V TO 3.6V

- Typical Operating Current: 10 mA @ 20 MHz
- Multiple Power Saving Sleep and Shutdown Modes

100-Pin TQFP and 64-Pin TQFP Packages Available

Temperature Range: -40°C to +85°C



1. SYSTEM OVERVIEW

The C8051F020/1/2/3 devices are fully integrated mixed-signal System-on-a-Chip MCUs with 64 digital I/O pins (C8051F020/2) or 32 digital I/O pins (C8051F021/3). Highlighted features are listed below; refer to Table 1.1 for specific product feature selection.

- High-Speed pipelined 8051-compatible CIP-51 microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- True 12-bit (C8051F020/1) or 10-bit (C8051F022/3) 100 ksps 8-channel ADC with PGA and analog multiplexer
- True 8-bit ADC 500 ksps 8-channel ADC with PGA and analog multiplexer
- Two 12-bit DACs with programmable update scheduling
- 64k bytes of in-system programmable FLASH memory
- 4352 (4096 + 256) bytes of on-chip RAM
- External Data Memory Interface with 64k byte address space
- SPI, SMBus/I^2C, and (2) UART serial interfaces implemented in hardware
- Five general purpose 16-bit Timers
- Programmable Counter/Timer Array with five capture/compare modules
- On-chip Watchdog Timer, VDD Monitor, and Temperature Sensor

With on-chip VDD monitor, Watchdog Timer, and clock oscillator, the C8051F020/1/2/3 devices are truly stand-alone System-on-a-Chip solutions. All analog and digital peripherals are enabled/disabled and configured by user firmware. The FLASH memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware.

On-board JTAG debug circuitry allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug system supports inspection and modification of memory and registers, setting breakpoints, watchpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using JTAG.

Each MCU is specified for 2.7 V-to-3.6 V operation over the industrial temperature range (-45° C to +85° C). The Port I/Os, /RST, and JTAG pins are tolerant for input signals up to 5 V. The C8051F020/2 are available in a 100-pin TQFP package (see block diagrams in Figure 1.1 and Figure 1.3). The C8051F021/3 are available in a 64-pin TQFP package (see block diagrams in Figure 1.2 and Figure 1.4).

Table 1.1. Product Selection Guide

	MIPS (Peak)	FLASH Memory	RAM	External Memory Interface	SMBus/I^2C	SPI	UARTS	Timers (16-bit)	Programmable Counter Array	Digital Port I/O's	12-bit 100ksps ADC Inputs	10-bit 100ksps ADC Inputs	8-bit 500ksps ADC Inputs	Voltage Reference	Temperature Sensor	DAC Resolution (bits)	DAC Outputs	Analog Comparators	Package
C8051F020	25	64k	4352	✓	✓	✓	2	5	✓	64	8	-	8	✓	✓	12	2	2	100TQFP
C8051F021	25	64k	4352	✓	✓	✓	2	5	✓	32	8	-	8	✓	✓	12	2	2	64TQFP
C8051F022	25	64k	4352	✓	✓	✓	2	5	✓	64	-	8	8	✓	✓	12	2	2	100TQFP
C8051F023	25	64k	4352	✓	✓	✓	2	5	✓	32	-	8	8	✓	✓	12	2	2	64TQFP

2. ABSOLUTE MAXIMUM RATINGS

Table 2.1. Absolute Maximum Ratings*

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Ambient temperature under bias		-55		125	°C
Storage Temperature		-65		150	°C
Voltage on any Pin (except VDD and Port I/O) with respect to DGND		-0.3		VDD + 0.3	V
Voltage on any Port I/O Pin or /RST with respect to DGND		-0.3		5.8	V
Voltage on VDD with respect to DGND		-0.3		4.2	V
Maximum Total current through VDD, AV+, DGND, and AGND				800	mA
Maximum output current sunk by any Port pin				100	mA
Maximum output current sunk by any other I/O pin				50	mA
Maximum output current sourced by any Port pin				100	mA
Maximum output current sourced by any other I/O pin				50	mA

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

3. GLOBAL DC ELECTRICAL CHARACTERISTICS

Table 1.1. Global DC Electrical Characteristics

-40°C to +85°C, 25 MHz System Clock unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Supply Voltage	(Note 1)	2.7	3.0	3.6	V
Analog Supply Current	AV+=2.7 V, Internal REF, ADC, DAC, Comparators all active		1.7		mA
Analog Supply Current with analog sub-systems inactive	AV+=2.7 V, Internal REF, ADC, DAC, Comparators all disabled, oscillator disabled, VDD Monitor disabled		0.2		µA
Analog-to-Digital Supply Delta (|VDD - AV+|)				0.5	V
Digital Supply Voltage		2.7	3.0	3.6	V
Digital Supply Current with CPU active	VDD=2.7 V, Clock=25 MHz VDD=2.7 V, Clock=1 MHz VDD=2.7 V, Clock=32 kHz		10 0.5 20		mA mA µA
Digital Supply Current with CPU inactive (not accessing FLASH)	VDD=2.7 V, Clock=25 MHz VDD=2.7 V, Clock=1 MHz VDD=2.7 V, Clock=32 kHz		5 0.2 10		mA mA µA
Digital Supply Current (shut-down)	VDD=2.7 V, Oscillator not running, VDD Monitor disabled		0.2		µA
Digital Supply RAM Data Retention Voltage			1.5		V
Specified Operating Temperature Range		-40		+85	°C

Note 1: Analog Supply AV+ must be greater than 1 V for VDD monitor to operate.

4. PINOUT AND PACKAGE DEFINITIONS

Table 4.1. Pin Definitions

[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
VDD	37, 64, 90	24, 41, 57		Digital Supply Voltage. Must be tied to +2.7 to +3.6 V.
DGND	38, 63, 89	25, 40, 56		Digital Ground. Must be tied to Ground.
AV+	11, 14	6		Analog Supply Voltage. Must be tied to +2.7 to +3.6 V.
AGND	10, 13	5		Analog Ground. Must be tied to Ground.
TMS	1	58	D In	JTAG Test Mode Select with internal pull-up.
TCK	2	59	D In	JTAG Test Clock with internal pull-up.
TDI	3	60	D In	JTAG Test Data Input with internal pull-up. TDI is latched on the rising edge of TCK.
TDO	4	61	D Out	JTAG Test Data Output with internal pull-up. Data is shifted out on TDO on the falling edge of TCK. TDO output is a tri-state driver.
/RST	5	62	D I/O	Device Reset. Open-drain output of internal VDD monitor. Is driven low when VDD is <2.7 V and MONEN is high. An external source can initiate a system reset by driving this pin low.
XTAL1	26	17	A In	Crystal Input. This pin is the return for the internal oscillator circuit for a crystal or ceramic resonator. For a precision internal clock, connect a crystal or ceramic resonator from XTAL1 to XTAL2. If overdriven by an external CMOS clock, this becomes the system clock.
XTAL2	27	18	A Out	Crystal Output. This pin is the excitation driver for a crystal or ceramic resonator.
MONEN	28	19	D In	VDD Monitor Enable. When tied high, this pin enables the internal VDD monitor, which forces a system reset when VDD is < 2.7 V. When tied low, the internal VDD monitor is disabled.
VREF	12	7	A I/O	Bandgap Voltage Reference Output (all devices). DAC Voltage Reference Input (F021/3 only).
VREFA		8	A In	ADC0 and ADC1 Voltage Reference Input.
VREF0	16		A In	ADC0 Voltage Reference Input.
VREF1	17		A In	ADC1 Voltage Reference Input.
VREFD	15		A In	DAC Voltage Reference Input.

Table 4.1. Pin Definitions

[redacted]				
AIN0.0	18	9	A In	ADC0 Input Channel 0 (See ADC0 Specification for complete description).
AIN0.1	19	10	A In	ADC0 Input Channel 1 (See ADC0 Specification for complete description).
AIN0.2	20	11	A In	ADC0 Input Channel 2 (See ADC0 Specification for complete description).
AIN0.3	21	12	A In	ADC0 Input Channel 3 (See ADC0 Specification for complete description).
AIN0.4	22	13	A In	ADC0 Input Channel 4 (See ADC0 Specification for complete description).
AIN0.5	23	14	A In	ADC0 Input Channel 5 (See ADC0 Specification for complete description).
AIN0.6	24	15	A In	ADC0 Input Channel 6 (See ADC0 Specification for complete description).
AIN0.7	25	16	A In	ADC0 Input Channel 7 (See ADC0 Specification for complete description).
CP0+	9	4	A In	Comparator 0 Non-Inverting Input.
CP0-	8	3	A In	Comparator 0 Inverting Input.
CP1+	7	2	A In	Comparator 1 Non-Inverting Input.
CP1-	6	1	A In	Comparator 1 Inverting Input.
DAC0	100	64	A Out	Digital to Analog Converter 0 Voltage Output. (See DAC Specification for complete description).
DAC1	99	63	A Out	Digital to Analog Converter 1 Voltage Output. (See DAC Specification for complete description).
P0.0	62	55	D I/O	Port 0.0. See Port Input/Output section for complete description.
P0.1	61	54	D I/O	Port 0.1. See Port Input/Output section for complete description.
P0.2	60	53	D I/O	Port 0.2. See Port Input/Output section for complete description.
P0.3	59	52	D I/O	Port 0.3. See Port Input/Output section for complete description.
P0.4	58	51	D I/O	Port 0.4. See Port Input/Output section for complete description.
ALE/P0.5	57	50	D I/O	ALE Strobe for External Memory Address bus (multiplexed mode) Port 0.5 See Port Input/Output section for complete description.

Table 4.1. Pin Definitions

/RD/P0.6	56	49	D I/O	/RD Strobe for External Memory Address bus Port 0.6 See Port Input/Output section for complete description.
/WR/P0.7	55	48	D I/O	/WR Strobe for External Memory Address bus Port 0.7 See Port Input/Output section for complete description.
AIN1.0/A8/P1.0	36	29	A In D I/O	ADC1 Input Channel 0 (See ADC1 Specification for complete description). Bit 8 External Memory Address bus (Non-multiplexed mode) Port 1.0 See Port Input/Output section for complete description.
AIN1.1/A9/P1.1	35	28	A In D I/O	Port 1.1. See Port Input/Output section for complete description.
AIN1.2/A10/P1.2	34	27	A In D I/O	Port 1.2. See Port Input/Output section for complete description.
AIN1.3/A11/P1.3	33	26	A In D I/O	Port 1.3. See Port Input/Output section for complete description.
AIN1.4/A12/P1.4	32	23	A In D I/O	Port 1.4. See Port Input/Output section for complete description.
AIN1.5/A13/P1.5	31	22	A In D I/O	Port 1.5. See Port Input/Output section for complete description.
AIN1.6/A14/P1.6	30	21	A In D I/O	Port 1.6. See Port Input/Output section for complete description.
AIN1.7/A15/P1.7	29	20	A In D I/O	Port 1.7. See Port Input/Output section for complete description.
A8m/A0/P2.0	46	37	D I/O	Bit 8 External Memory Address bus (Multiplexed mode) Bit 0 External Memory Address bus (Non-multiplexed mode) Port 2.0 See Port Input/Output section for complete description.
A9m/A1/P2.1	45	36	D I/O	Port 2.1. See Port Input/Output section for complete description.
A10m/A2/P2.2	44	35	D I/O	Port 2.2. See Port Input/Output section for complete description.
A11m/A3/P2.3	43	34	D I/O	Port 2.3. See Port Input/Output section for complete description.
A12m/A4/P2.4	42	33	D I/O	Port 2.4. See Port Input/Output section for complete description.
A13m/A5/P2.5	41	32	D I/O	Port 2.5. See Port Input/Output section for complete description.

Table 4.1. Pin Definitions

A14m/A6/P2.6	40	31	D I/O	Port 2.6. See Port Input/Output section for complete description.
A15m/A7/P2.7	39	30	D I/O	Port 2.7. See Port Input/Output section for complete description.
AD0/D0/P3.0	54	47	D I/O	Bit 0 External Memory Address/Data bus (Multiplexed mode) Bit 0 External Memory Data bus (Non-multiplexed mode) Port 3.0 See Port Input/Output section for complete description.
AD1/D1/P3.1	53	46	D I/O	Port 3.1. See Port Input/Output section for complete description.
AD2/D2/P3.2	52	45	D I/O	Port 3.2. See Port Input/Output section for complete description.
AD3/D3/P3.3	51	44	D I/O	Port 3.3. See Port Input/Output section for complete description.
AD4/D4/P3.4	50	43	D I/O	Port 3.4. See Port Input/Output section for complete description.
AD5/D5/P3.5	49	42	D I/O	Port 3.5. See Port Input/Output section for complete description.
AD6/D6/P3.6/IE6	48	39	D I/O	Port 3.6. See Port Input/Output section for complete description.
AD7/D7/P3.7/IE7	47	38	D I/O	Port 3.7. See Port Input/Output section for complete description.
P4.0	98		D I/O	Port 4.0. See Port Input/Output section for complete description.
P4.1	97		D I/O	Port 4.1. See Port Input/Output section for complete description.
P4.2	96		D I/O	Port 4.2. See Port Input/Output section for complete description.
P4.3	95		D I/O	Port 4.3. See Port Input/Output section for complete description.
P4.4	94		D I/O	Port 4.4. See Port Input/Output section for complete description.
ALE/P4.5	93		D I/O	ALE Strobe for External Memory Address bus (multiplexed mode) Port 4.5 See Port Input/Output section for complete description.
/RD/P4.6	92		D I/O	/RD Strobe for External Memory Address bus Port 4.6 See Port Input/Output section for complete description.
/WR/P4.7	91		D I/O	/WR Strobe for External Memory Address bus Port 4.7 See Port Input/Output section for complete description.
A8/P5.0	88		D I/O	Bit 8 External Memory Address bus (Non-multiplexed mode) Port 5.0 See Port Input/Output section for complete description.
A9/P5.1	87		D I/O	Port 5.1. See Port Input/Output section for complete description.
A10/P5.2	86		D I/O	Port 5.2. See Port Input/Output section for complete description.

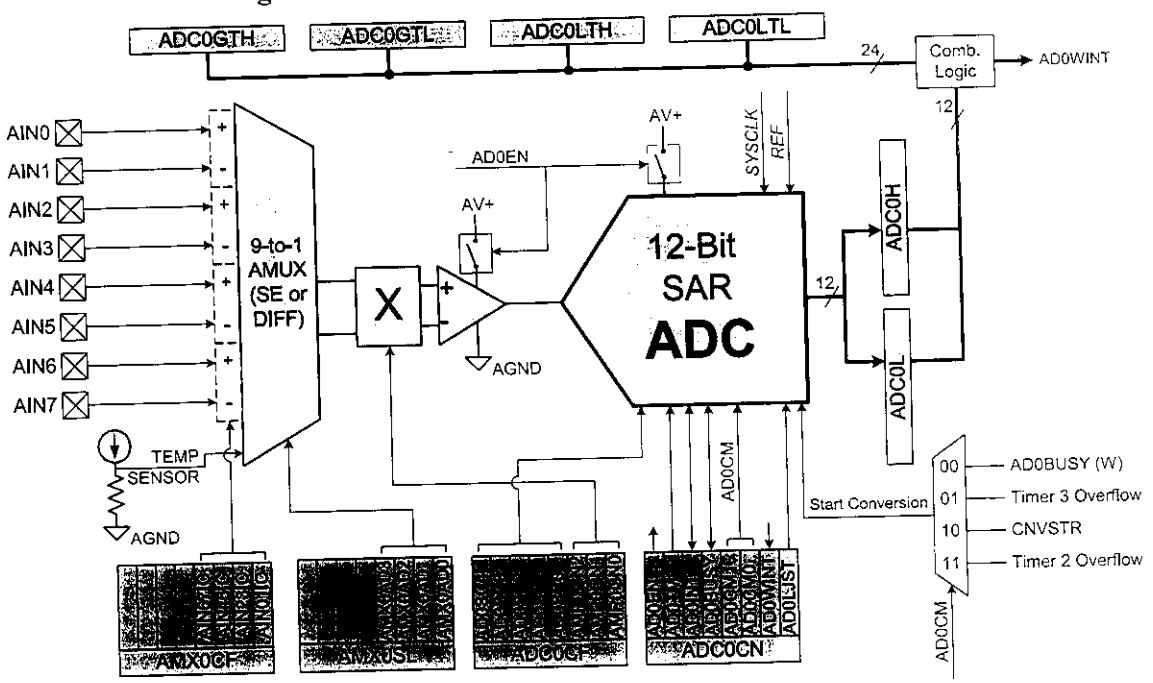
Table 4.1. Pin Definitions

A11/P5.3	85		D I/O	Port 5.3. See Port Input/Output section for complete description.
A12/P5.4	84		D I/O	Port 5.4. See Port Input/Output section for complete description.
A13/P5.5	83		D I/O	Port 5.5. See Port Input/Output section for complete description.
A14/P5.6	82		D I/O	Port 5.6. See Port Input/Output section for complete description.
A15/P5.7	81		D I/O	Port 5.7. See Port Input/Output section for complete description.
A8m/A0/P6.0	80		D I/O	Bit 8 External Memory Address bus (Multiplexed mode) Bit 0 External Memory Address bus (Non-multiplexed mode) Port 6.0 See Port Input/Output section for complete description.
A9m/A1/P6.1	79		D I/O	Port 6.1. See Port Input/Output section for complete description.
A10m/A2/P6.2	78		D I/O	Port 6.2. See Port Input/Output section for complete description.
A11m/A3/P6.3	77		D I/O	Port 6.3. See Port Input/Output section for complete description.
A12m/A4/P6.4	76		D I/O	Port 6.4. See Port Input/Output section for complete description.
A13m/A5/P6.5	75		D I/O	Port 6.5. See Port Input/Output section for complete description.
A14m/A6/P6.6	74		D I/O	Port 6.6. See Port Input/Output section for complete description.
A15m/A7/P6.7	73		D I/O	Port 6.7. See Port Input/Output section for complete description.
AD0/D0/P7.0	72		D I/O	Bit 0 External Memory Address/Data bus (Multiplexed mode) Bit 0 External Memory Data bus (Non-multiplexed mode) Port 7.0 See Port Input/Output section for complete description.
AD1/D1/P7.1	71		D I/O	Port 7.1. See Port Input/Output section for complete description.
AD2/D2/P7.2	70		D I/O	Port 7.2. See Port Input/Output section for complete description.
AD3/D3/P7.3	69		D I/O	Port 7.3. See Port Input/Output section for complete description.
AD4/D4/P7.4	68		D I/O	Port 7.4. See Port Input/Output section for complete description.
AD5/D5/P7.5	67		D I/O	Port 7.5. See Port Input/Output section for complete description.
AD6/D6/P7.6	66		D I/O	Port 7.6. See Port Input/Output section for complete description.
AD7/D7/P7.7	65		D I/O	Port 7.7. See Port Input/Output section for complete description.

5. ADC0 (12-BIT ADC, C8051F020/1 ONLY)

The ADC0 subsystem for the C8051F020/1 consists of a 9-channel, configurable analog multiplexer (AMUX0), a programmable gain amplifier (PGA0), and a 100 ksps, 12-bit successive-approximation-register ADC with integrated track-and-hold and Programmable Window Detector (see block diagram in Figure 5.1). The AMUX0, PGA0, Data Conversion Modes, and Window Detector are all configurable under software control via the Special Function Registers shown in Figure 5.1. The voltage reference used by ADC0 is selected as described in Section "9. VOLTAGE REFERENCE (C8051F020/2)" on page 91 for C8051F020/2 devices, or Section "10. VOLTAGE REFERENCE (C8051F021/3)" on page 93 for C8051F021/3 devices. The ADC0 subsystem (ADC0, track-and-hold and PGA0) is enabled only when the AD0EN bit in the ADC0 Control register (ADC0CN) is set to logic 1. The ADC0 subsystem is in low power shutdown when this bit is logic 0.

Figure 5.1. 12-Bit ADC0 Functional Block Diagram



5.1. Analog Multiplexer and PGA

Eight of the AMUX channels are available for external measurements while the ninth channel is internally connected to an on-chip temperature sensor (temperature transfer function is shown in Figure 5.2). AMUX input pairs can be programmed to operate in either differential or single-ended mode. This allows the user to select the best measurement technique for each input channel, and even accommodates mode changes "on-the-fly". The AMUX defaults to all single-ended inputs upon reset. There are two registers associated with the AMUX: the Channel Selection register AMX0SL (Figure 5.6), and the Configuration register AMX0CF (Figure 5.7). The table in Figure 5.6 shows AMUX functionality by channel, for each possible configuration. The PGA amplifies the AMUX output signal by an amount determined by the states of the AMP0GN2-0 bits in the ADC0 Configuration register, ADC0CF (Figure 5.7). The PGA can be software-programmed for gains of 0.5, 2, 4, 8 or 16. Gain defaults to unity on reset.

Figure 5.5. AMX0CF: AMUX0 Configuration Register (C8051F020/1)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	AIN67IC	AIN45IC	AIN23IC	AIN10IC	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xBA

Bits7-4: UNUSED. Read = 0000b; Write = don't care

Bit3: AIN67IC: AIN6, AIN7 Input Pair Configuration Bit
0: AIN6 and AIN7 are independent single-ended inputs
1: AIN6, AIN7 are (respectively) +, - differential input pair

Bit2: AIN45IC: AIN4, AIN5 Input Pair Configuration Bit
0: AIN4 and AIN5 are independent single-ended inputs
1: AIN4, AIN5 are (respectively) +, - differential input pair

Bit1: AIN23IC: AIN2, AIN3 Input Pair Configuration Bit
0: AIN2 and AIN3 are independent single-ended inputs
1: AIN2, AIN3 are (respectively) +, - differential input pair

Bit0: AIN01IC: AIN0, AIN1 Input Pair Configuration Bit
0: AIN0 and AIN1 are independent single-ended inputs
1: AIN0, AIN1 are (respectively) +, - differential input pair

NOTE: The ADC0 Data Word is in 2's complement format for channels configured as differential.

Figure 5.6. AMX0SL: AMUX0 Channel Select Register (C8051F020/1)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	AMX0AD3	AMX0AD2	AMX0AD1	AMX0AD0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xBB

Bits7-4: UNUSED. Read = 0000b; Write = don't care
Bits3-0: AMX0AD3-0: AMX0 Address Bits
0000-1111b: ADC Inputs selected per chart below

AMX0CF Bits 3-0	AMX0AD3-0 = 0000	0001	0010	0011	0100	0101	0110	0111	1xxx
0000	AIN0	AIN1	AIN2	AIN3	AIN4	AIN5	AIN6	AIN7	TEMP SENSOR
0001	+(AIN0) -(AIN1)		AIN2	AIN3	AIN4	AIN5	AIN6	AIN7	TEMP SENSOR
0010	AIN0	AIN1	+(AIN2) -(AIN3)		AIN4	AIN5	AIN6	AIN7	TEMP SENSOR
0011	+(AIN0) -(AIN1)		+(AIN2) -(AIN3)		AIN4	AIN5	AIN6	AIN7	TEMP SENSOR
0100	AIN0	AIN1	AIN2	AIN3	+(AIN4) -(AIN5)		AIN6	AIN7	TEMP SENSOR
0101	+(AIN0) -(AIN1)		AIN2	AIN3	+(AIN4) -(AIN5)		AIN6	AIN7	TEMP SENSOR
0110	AIN0	AIN1	+(AIN2) -(AIN3)		+(AIN4) -(AIN5)		AIN6	AIN7	TEMP SENSOR
0111	+(AIN0) -(AIN1)		+(AIN2) -(AIN3)		+(AIN4) -(AIN5)		AIN6	AIN7	TEMP SENSOR
1000	AIN0	AIN1	AIN2	AIN3	AIN4	AIN5	+(AIN6) -(AIN7)		TEMP SENSOR
1001	+(AIN0) -(AIN1)		AIN2	AIN3	AIN4	AIN5	+(AIN6) -(AIN7)		TEMP SENSOR
1010	AIN0	AIN1	+(AIN2) -(AIN3)		AIN4	AIN5	+(AIN6) -(AIN7)		TEMP SENSOR
1011	+(AIN0) -(AIN1)		+(AIN2) -(AIN3)		AIN4	AIN5	+(AIN6) -(AIN7)		TEMP SENSOR
1100	AIN0	AIN1	AIN2	AIN3	+(AIN4) -(AIN5)		+(AIN6) -(AIN7)		TEMP SENSOR
1101	+(AIN0) -(AIN1)		AIN2	AIN3	+(AIN4) -(AIN5)		+(AIN6) -(AIN7)		TEMP SENSOR
1110	AIN0	AIN1	+(AIN2) -(AIN3)		+(AIN4) -(AIN5)		+(AIN6) -(AIN7)		TEMP SENSOR
1111	+(AIN0) -(AIN1)		+(AIN2) -(AIN3)		+(AIN4) -(AIN5)		+(AIN6) -(AIN7)		TEMP SENSOR

Figure 5.7. ADC0CF: ADC0 Configuration Register (C8051F020/1)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
AD0SC4	AD0SC3	AD0SC2	AD0SC1	AD0SC0	AMP0GN2	AMP0GN1	AMP0GN0	11111000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xBC

Bits7-3: AD0SC4-0: ADC0 SAR Conversion Clock Period Bits
SAR Conversion clock is derived from system clock by the following equation, where *AD0SC* refers to the 5-bit value held in AD0SC4-0, and CLK_{SAR0} refers to the desired ADC0 SAR clock. See Table 5.1 on page 57 for SAR clock setting requirements.

$$AD0SC = \frac{SYSCLK}{CLK_{SAR0}} - 1$$

Bits2-0: AMP0GN2-0: ADC0 Internal Amplifier Gain (PGA)
000: Gain = 1
001: Gain = 2
010: Gain = 4
011: Gain = 8
10x: Gain = 16
11x: Gain = 0.5

Figure 5.8. ADC0CN: ADC0 Control Register (C8051F020/1)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
AD0EN	AD0TM	AD0INT	AD0BUSY	AD0CM1	AD0CM0	AD0WINT	AD0LJST	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (bit addressable)	SFR Address: 0xE8

Bit7: AD0EN: ADC0 Enable Bit.
0: ADC0 Disabled. ADC0 is in low-power shutdown.
1: ADC0 Enabled. ADC0 is active and ready for data conversions.

Bit6: AD0TM: ADC Track Mode Bit
0: When the ADC is enabled, tracking is continuous unless a conversion is in process
1: Tracking Defined by ADSTM1-0 bits

Bit5: AD0INT: ADC0 Conversion Complete Interrupt Flag.
This flag must be cleared by software.
0: ADC0 has not completed a data conversion since the last time this flag was cleared.
1: ADC0 has completed a data conversion.

Bit4: AD0BUSY: ADC0 Busy Bit.
Read:
0: ADC0 Conversion is complete or a conversion is not currently in progress. AD0INT is set to logic 1 on the falling edge of AD0BUSY.
1: ADC0 Conversion is in progress.
Write:
0: No Effect.
1: Initiates ADC0 Conversion if AD0STM1-0 = 00b

Bit3-2: AD0CM1-0: ADC0 Start of Conversion Mode Select.
If AD0TM = 0:
00: ADC0 conversion initiated on every write of '1' to AD0BUSY.
01: ADC0 conversion initiated on overflow of Timer 3.
10: ADC0 conversion initiated on rising edge of external CNVSTR.
11: ADC0 conversion initiated on overflow of Timer 2.
If AD0TM = 1:
00: Tracking starts with the write of '1' to AD0BUSY and lasts for 3 SAR clocks, followed by conversion.
01: Tracking started by the overflow of Timer 3 and last for 3 SAR clocks, followed by conversion.
10: ADC0 tracks only when CNVSTR input is logic low; conversion starts on rising CNVSTR edge.
11: Tracking started by the overflow of Timer 2 and last for 3 SAR clocks, followed by conversion.

Bit1: AD0WINT: ADC0 Window Compare Interrupt Flag.
This bit must be cleared by software.
0: ADC0 Window Comparison Data match has not occurred since this flag was last cleared.
1: ADC0 Window Comparison Data match has occurred.

Bit0: AD0LJST: ADC0 Left Justify Select.
0: Data in ADC0H:ADC0L registers are right-justified.
1: Data in ADC0H:ADC0L registers are left-justified.

MEMORY" on page 137). The External Memory Interface provides a fast access to off-chip XRAM (or memory-mapped peripherals) via the MOVX instruction. Refer to Section "16. EXTERNAL DATA MEMORY INTERFACE AND ON-CHIP XRAM" on page 143 for details.

Table 12.1. CIP-51 Instruction Set Summary

Mnemonic	Description	Bytes	Clock Cycles
ARITHMETIC OPERATIONS			
ADD A, Rn	Add register to A	1	1
ADD A, direct	Add direct byte to A	2	2
ADD A, @Ri	Add indirect RAM to A	1	2
ADD A, #data	Add immediate to A	2	2
ADDC A, Rn	Add register to A with carry	1	1
ADDC A, direct	Add direct byte to A with carry	2	2
ADDC A, @Ri	Add indirect RAM to A with carry	1	2
ADDC A, #data	Add immediate to A with carry	2	2
SUBB A, Rn	Subtract register from A with borrow	1	1
SUBB A, direct	Subtract direct byte from A with borrow	2	2
SUBB A, @Ri	Subtract indirect RAM from A with borrow	1	2
SUBB A, #data	Subtract immediate from A with borrow	2	2
INC A	Increment A	1	1
INC Rn	Increment register	1	1
INC direct	Increment direct byte	2	2
INC @Ri	Increment indirect RAM	1	2
DEC A	Decrement A	1	1
DEC Rn	Decrement register	1	1
DEC direct	Decrement direct byte	2	2
DEC @Ri	Decrement indirect RAM	1	2
INC DPTR	Increment Data Pointer	1	1
MUL AB	Multiply A and B	1	4
DIV AB	Divide A by B	1	8
DA A	Decimal adjust A	1	1
LOGICAL OPERATIONS			
ANL A, Rn	AND Register to A	1	1
ANL A, direct	AND direct byte to A	2	2
ANL A, @Ri	AND indirect RAM to A	1	2
ANL A, #data	AND immediate to A	2	2
ANL direct, A	AND A to direct byte	2	2
ANL direct, #data	AND immediate to direct byte	3	3
ORL A, Rn	OR Register to A	1	1
ORL A, direct	OR direct byte to A	2	2
ORL A, @Ri	OR indirect RAM to A	1	2
ORL A, #data	OR immediate to A	2	2
ORL direct, A	OR A to direct byte	2	2
ORL direct, #data	OR immediate to direct byte	3	3
XRL A, Rn	Exclusive-OR Register to A	1	1
XRL A, direct	Exclusive-OR direct byte to A	2	2
XRL A, @Ri	Exclusive-OR indirect RAM to A	1	2

Table 12.1. CIP-51 Instruction Set Summary

Mnemonic	Description	Bytes	Clock Cycles
XRL A, #data	Exclusive-OR immediate to A	2	2
XRL direct, A	Exclusive-OR A to direct byte	2	2
XRL direct, #data	Exclusive-OR immediate to direct byte	3	3
CLR A	Clear A	1	1
CPL A	Complement A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through Carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through Carry	1	1
SWAP A	Swap nibbles of A	1	1
	DATA TRANSFER		
MOV A, Rn	Move Register to A	1	1
MOV A, direct	Move direct byte to A	2	2
MOV A, @Ri	Move indirect RAM to A	1	2
MOV A, #data	Move immediate to A	2	2
MOV Rn, A	Move A to Register	1	1
MOV Rn, direct	Move direct byte to Register	2	2
MOV Rn, #data	Move immediate to Register	2	2
MOV direct, A	Move A to direct byte	2	2
MOV direct, Rn	Move Register to direct byte	2	2
MOV direct, direct	Move direct byte to direct byte	3	3
MOV direct, @Ri	Move indirect RAM to direct byte	2	2
MOV direct, #data	Move immediate to direct byte	3	3
MOV @Ri, A	Move A to indirect RAM	1	2
MOV @Ri, direct	Move direct byte to indirect RAM	2	2
MOV @Ri, #data	Move immediate to indirect RAM	2	2
MOV DPTR, #data16	Load DPTR with 16-bit constant	3	3
MOVC A, @A+DPTR	Move code byte relative DPTR to A	1	3
MOVC A, @A+PC	Move code byte relative PC to A	1	3
MOVX A, @Ri	Move external data (8-bit address) to A	1	3
MOVX @Ri, A	Move A to external data (8-bit address)	1	3
MOVX A, @DPTR	Move external data (16-bit address) to A	1	3
MOVX @DPTR, A	Move A to external data (16-bit address)	1	3
PUSH direct	Push direct byte onto stack	2	2
POP direct	Pop direct byte from stack	2	2
XCH A, Rn	Exchange Register with A	1	1
XCH A, direct	Exchange direct byte with A	2	2
XCH A, @Ri	Exchange indirect RAM with A	1	2
XCHD A, @Ri	Exchange low nibble of indirect RAM with A	1	2
	BOOLEAN MANIPULATION		
CLR C	Clear Carry	1	1
CLR bit	Clear direct bit	2	2
SETB C	Set Carry	1	1
SETB bit	Set direct bit	2	2
CPL C	Complement Carry	1	1

Table 12.1. CIP-51 Instruction Set Summary

		Bytes	Clock Cycles
CPL bit	Complement direct bit	2	2
ANL C, bit	AND direct bit to Carry	2	2
ANL C, /bit	AND complement of direct bit to Carry	2	2
ORL C, bit	OR direct bit to carry	2	2
ORL C, /bit	OR complement of direct bit to Carry	2	2
MOV C, bit	Move direct bit to Carry	2	2
MOV bit, C	Move Carry to direct bit	2	2/3
JC rel	Jump if Carry is set	2	2/3
JNC rel	Jump if Carry is not set	3	3/4
JB bit, rel	Jump if direct bit is set	3	3/4
JNB bit, rel	Jump if direct bit is not set	3	3/4
JBC bit, rel	Jump if direct bit is set and clear bit		
	PROGRAM BRANCHING		
ACALL addr11	Absolute subroutine call	2	3
LCALL addr16	Long subroutine call	3	4
RET	Return from subroutine	1	5
RETI	Return from interrupt	1	5
AJMP addr11	Absolute jump	2	3
LJMP addr16	Long jump	3	4
SJMP rel	Short jump (relative address)	2	3
JMP @A+DPTR	Jump indirect relative to DPTR	1	3
JZ rel	Jump if A equals zero	2	2/3
JNZ rel	Jump if A does not equal zero	2	2/3
CJNE A, direct, rel	Compare direct byte to A and jump if not equal	3	3/4
CJNE A, #data, rel	Compare immediate to A and jump if not equal	3	3/4
CJNE Rn, #data, rel	Compare immediate to Register and jump if not equal	3	3/4
CJNE @Ri, #data, rel	Compare immediate to indirect and jump if not equal	3	4/5
DJNZ Rn, rel	Decrement Register and jump if not zero	2	2/3
DJNZ direct, rel	Decrement direct byte and jump if not zero	3	3/4
NOP	No operation		

Table 13.1. Reset Electrical Characteristics

-40°C to +85°C unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
/RST Output High Voltage	I_{OH} = -3 mA	VDD - 0.7			V
/RST Output Low Voltage	I_{OL} = 8.5 mA, VDD = 2.7 V to 3.6 V			0.6	V
/RST Input High Voltage		0.7 x VDD			V
/RST Input Low Voltage				0.3 x VDD	
/RST Input Leakage Current	/RST = 0.0 V		50		µA
VDD for /RST Output Valid		1.0			V
AV+ for /RST Output Valid		1.0			V
VDD POR Threshold (V_{RST})		2.40	2.55	2.70	V
Minimum /RST Low Time to Generate a System Reset		10			ns
Reset Time Delay	/RST rising edge after VDD crosses V_{RST} threshold	80	100	120	ms
Missing Clock Detector Timeout	Time from last system clock to reset initiation	100	220	500	µs

14. OSCILLATORS

Each MCU includes an internal oscillator and an external oscillator drive circuit, either of which can generate the system clock. The MCUs operate from the internal oscillator after any reset. This internal oscillator can be enabled/disabled and its frequency can be set using the Internal Oscillator Control Register (OSCICN) as shown in Figure 14.1. The internal oscillator's electrical specifications are given in Table 14.1.

Both oscillators are disabled when the /RST pin is held low. The MCUs can run from the internal oscillator permanently, or can switch to the external oscillator if desired using CLKSL bit in the OSCICN Register. The external oscillator requires an external resonator, crystal, capacitor, or RC network connected to the XTAL1/XTAL2 pins (see Table 14.1). The oscillator circuit must be configured for one of these sources in the OSCXCN register. An external CMOS clock can also provide the system clock; in this configuration, the XTAL1 pin is used as the CMOS clock input. The XTAL1 and XTAL2 pins are NOT 5V tolerant.

Figure 14.1. Oscillator Diagram

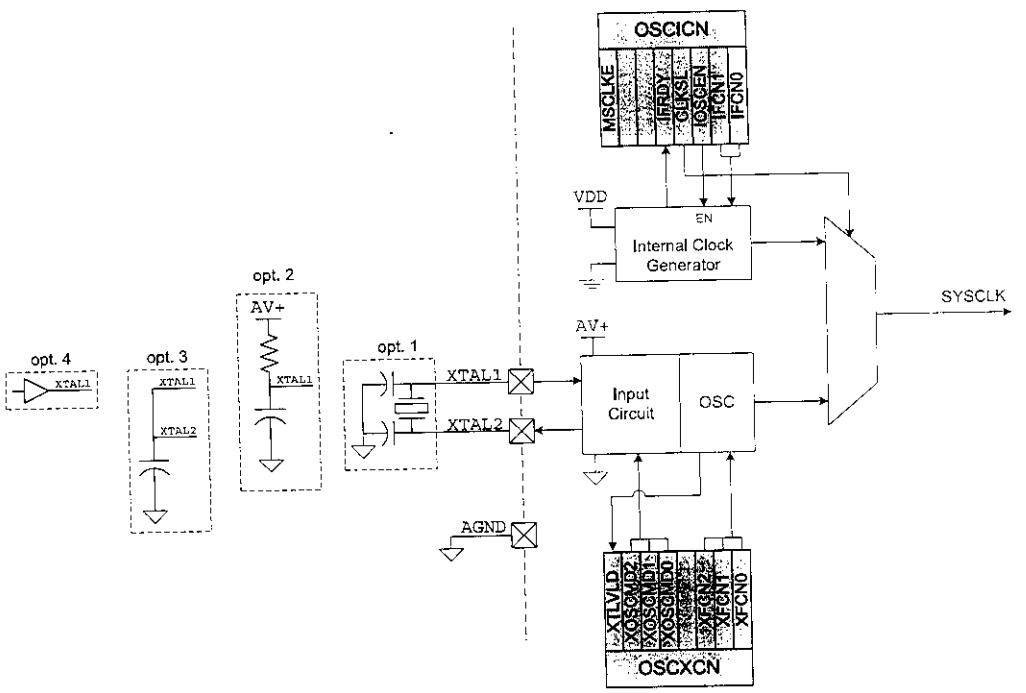


Figure 14.2. OSCICN: Internal Oscillator Control Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
MSCLKE	-	-	IFRDY	CLKSL	IOSCEN	IFCN1	IFCN0	00010100
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xB2

Bit7: MSCLKE: Missing Clock Enable Bit
0: Missing Clock Detector Disabled
1: Missing Clock Detector Enabled; reset triggered if clock is missing for more than 100 µs

Bits6-5: UNUSED. Read = 00b, Write = don't care

Bit4: IFRDY: Internal Oscillator Frequency Ready Flag
0: Internal Oscillator Frequency not running at speed specified by the IFCN bits.
1: Internal Oscillator Frequency running at speed specified by the IFCN bits.

Bit3: CLKSL: System Clock Source Select Bit
0: Uses Internal Oscillator as System Clock.
1: Uses External Oscillator as System Clock.

Bit2: IOSCEN: Internal Oscillator Enable Bit
0: Internal Oscillator Disabled
1: Internal Oscillator Enabled

Bits1-0: IFCN1-0: Internal Oscillator Frequency Control Bits
00: Internal Oscillator typical frequency is 2 MHz.
01: Internal Oscillator typical frequency is 4 MHz.
10: Internal Oscillator typical frequency is 8 MHz.
11: Internal Oscillator typical frequency is 16 MHz.

Table 14.1. Internal Oscillator Electrical Characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Internal Oscillator Frequency	OSCICN.[1:0] = 00	1.5	2	2.4	MHz
	OSCICN.[1:0] = 01	3.1	4	4.8	
	OSCICN.[1:0] = 10	6.2	8	9.6	
	OSCICN.[1:0] = 11	12.3	16	19.2	
Internal Oscillator Current Consumption (from VDD)	OSCICN.2 = 1		200		µA

Figure 14.3. OSCXCN: External Oscillator Control Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
XTLVLD	XOSCMD2	XOSCMD1	XOSCMD0	-	XFCN2	XFCN1	XFCN0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xB1

Bit7: XTLVLD: Crystal Oscillator Valid Flag
(Valid only when XOSCMD = 11x.)
0: Crystal Oscillator is unused or not yet stable
1: Crystal Oscillator is running and stable

Bits6-4: XOSCMD2-0: External Oscillator Mode Bits
00x: Off. XTAL1 pin is grounded internally.
010: System Clock from External CMOS Clock on XTAL1 pin.
011: System Clock from External CMOS Clock on XTAL1 pin divided by 2.
10x: RC/C Oscillator Mode with divide by 2 stage.
110: Crystal Oscillator Mode
111: Crystal Oscillator Mode with divide by 2 stage.

Bit3: RESERVED. Read = undefined, Write = don't care

Bits2-0: XFCN2-0: External Oscillator Frequency Control Bits
000-111:

XFCN	Crystal (XOSCMD = 11x)	RC (XOSCMD = 10x)	C (XOSCMD = 10x)
000	f < 12 kHz	f < 25 kHz	K Factor = 0.44
001	12 kHz < f ≤ 30 kHz	25 kHz < f ≤ 50 kHz	K Factor = 1.4
010	30 kHz < f ≤ 95 kHz	50 kHz < f ≤ 100 kHz	K Factor = 4.4
011	95 kHz < f ≤ 270 kHz	100 kHz < f ≤ 200 kHz	K Factor = 13
100	270 kHz < f ≤ 720 kHz	200 kHz < f ≤ 400 kHz	K Factor = 38
101	720 kHz < f ≤ 2.2 MHz	400 kHz < f ≤ 800 kHz	K Factor = 100
110	2.2 MHz < f ≤ 6.7 MHz	800 kHz < f ≤ 1.6 MHz	K Factor = 420
111	f > 6.7 MHz	1.6 MHz < f ≤ 3.2 MHz	K Factor = 1400

CRYSTAL MODE (Circuit from Figure 14.1, Option 1; XOSCMD = 11x)
Choose XFCN value to match the crystal or ceramic resonator frequency.

RC MODE (Circuit from Figure 14.1, Option 2; XOSCMD = 10x)
Choose oscillation frequency range where:
$f = 1.23(10^3) / (R * C)$, where
f = frequency of oscillation in MHz
C = capacitor value in pF
R = Pull-up resistor value in kΩ

C MODE (Circuit from Figure 14.1, Option 3; XOSCMD = 10x)
Choose K Factor (KF) for the oscillation frequency desired:
f = KF / (C * AV+), where
f = frequency of oscillation in MHz
C = capacitor value on XTAL1, XTAL2 pins in pF
AV+ = Analog Power Supply on MCU in volts

17. PORT INPUT/OUTPUT

The C8051F020/1/2/3 are fully integrated mixed-signal System on a Chip MCUs with 64 digital I/O pins (C8051F020/2) or 32 digital I/O pins (C8051F021/3), organized as 8-bit Ports. The lower ports: P0, P1, P2, and P3, are both bit- and byte-addressable through their corresponding Port Data registers. The upper ports: P4, P5, P6, and P7 are byte-addressable. All Port pins are 5 V-tolerant, and all support configurable Open-Drain or Push-Pull output modes and weak pull-ups. A block diagram of the Port I/O cell is shown in Figure 17.1. Complete Electrical Specifications for the Port I/O pins are given in Table 16.1.

Figure 17.1. Port I/O Cell Block Diagram

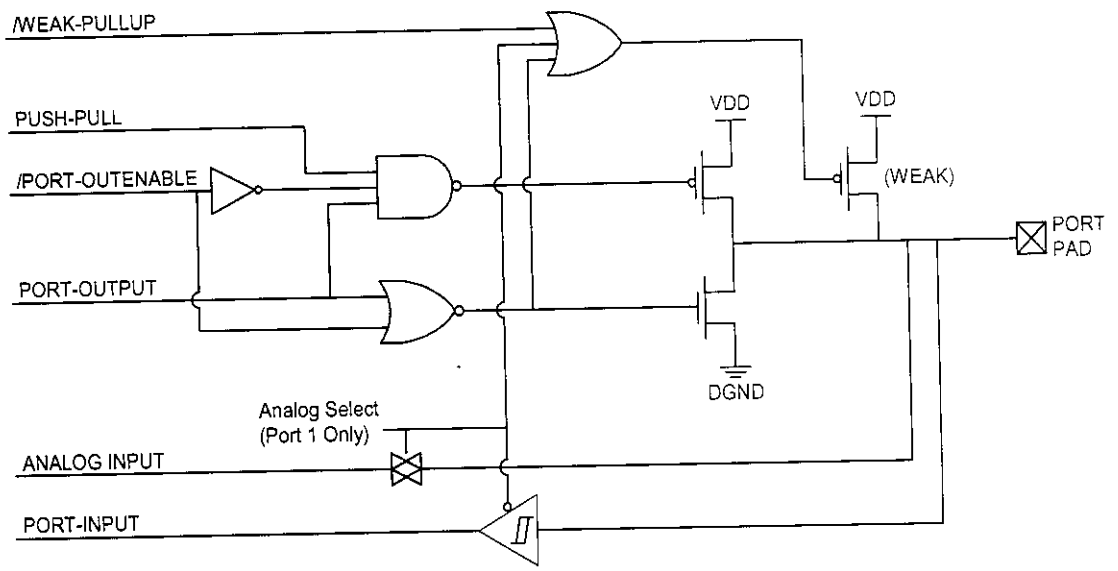


Table 17.1. Port I/O DC Electrical Characteristics

VDD = 2.7 V to 3.6 V, -40°C to +85°C unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage (V_{OH})	I_{OH} = -10 µA, Port I/O Push-Pull I_{OH} = -3 mA, Port I/O Push-Pull I_{OH} = -10 mA, Port I/O Push-Pull	VDD - 0.1 VDD - 0.7	 VDD - 0.8		V
Output Low Voltage (V_{OL})	I_{OL} = 10 µA I_{OL} = 8.5 mA I_{OL} = 25 mA		 1.0	0.1 0.6	V
Input High Voltage (VIH)		0.7 x VDD			V
Input Low Voltage (VIL)				0.3 x VDD	V
Input Leakage Current	DGND < Port Pin < VDD, Pin Tri-state Weak Pull-up Off Weak Pull-up On		 10	 = 1	µA
Input Capacitance			5		pF

Figure 17.7. XBR0: Port I/O Crossbar Register 0

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
CP0E	ECI0E	PCA0ME			UART0EN	SPI0EN	SMB0EN	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xE1

Bit7: CP0E: Comparator 0 Output Enable Bit.
0: CP0 unavailable at Port pin.
1: CP0 routed to Port pin.

Bit6: ECI0E: PCA0 External Counter Input Enable Bit.
0: PCA0 External Counter Input unavailable at Port pin.
1: PCA0 External Counter Input (ECI0) routed to Port pin.

Bits5-3: PCA0ME: PCA0 Module I/O Enable Bits.
000: All PCA0 I/O unavailable at Port pins.
001: CEX0 routed to Port pin.
010: CEX0, CEX1 routed to 2 Port pins.
011: CEX0, CEX1, and CEX2 routed to 3 Port pins.
100: CEX0, CEX1, CEX2, and CEX3 routed to 4 Port pins.
101: CEX0, CEX1, CEX2, CEX3, and CEX4 routed to 5 Port pins.
110: RESERVED
111: RESERVED

Bit2: UART0EN: UART0 I/O Enable Bit.
0: UART0 I/O unavailable at Port pins.
1: UART0 TX routed to P0.0, and RX routed to P0.1.

Bit1: SPI0EN: SPI0 Bus I/O Enable Bit.
0: SPI0 I/O unavailable at Port pins.
1: SPI0 SCK, MISO, MOSI, and NSS routed to 4 Port pins.

Bit0: SMB0EN: SMBus0 Bus I/O Enable Bit.
0: SMBus0 I/O unavailable at Port pins.
1: SMBus0 SDA and SCL routed to 2 Port pins.

Figure 17.8. XBR1: Port I/O Crossbar Register 1

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
SYSCKE	T2EXE	T2E	INT1E	T1E	INT0E	T0E	CP1E	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xE2

Bit7: SYSCKE: /SYSCLK Output Enable Bit.
0: /SYSCLK unavailable at Port pin.
1: /SYSCLK routed to Port pin.

Bit6: T2EXE: T2EX Input Enable Bit.
0: T2EX unavailable at Port pin.
1: T2EX routed to Port pin.

Bit5: T2E: T2 Input Enable Bit.
0: T2 unavailable at Port pin.
1: T2 routed to Port pin.

Bit4: INT1E: /INT1 Input Enable Bit.
0: /INT1 unavailable at Port pin.
1: /INT1 routed to Port pin.

Bit3: T1E: T1 Input Enable Bit.
0: T1 unavailable at Port pin.
1: T1 routed to Port pin.

Bit2: INT0E: /INT0 Input Enable Bit.
0: /INT0 unavailable at Port pin.
1: /INT1 routed to Port pin.

Bit1: T0E: T0 Input Enable Bit.
0: T0 unavailable at Port pin.
1: T0 routed to Port pin.

Bit0: CP1E: CP1 Output Enable Bit.
0: CP1 unavailable at Port pin.
1: CP1 routed to Port pin.

Figure 17.9. XBR2: Port I/O Crossbar Register 2

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
WEAKPUD	XBARE	-	T4EXE	T4E	UART1E	EMIFLE	CNVSTE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xE3

Bit7: WEAKPUD: Weak Pull-Up Disable Bit.
0: Weak pull-ups globally enabled.
1: Weak pull-ups globally disabled.

Bit6: XBARE: Crossbar Enable Bit.
0: Crossbar disabled. All pins on Ports 0, 1, 2, and 3, are forced to Input mode.
1: Crossbar enabled.

Bit5: UNUSED. Read = 0, Write = don't care.

Bit4: T4EXE: T4EX Input Enable Bit.
0: T4EX unavailable at Port pin.
1: T4EX routed to Port pin.

Bit3: T4E: T4 Input Enable Bit.
0: T4 unavailable at Port pin.
1: T4 routed to Port pin.

Bit2: UART1E: UART1 I/O Enable Bit.
0: UART1 I/O unavailable at Port pins.
1: UART1 TX and RX routed to 2 Port pins.

Bit1: EMIFLE: External Memory Interface Low-Port Enable Bit.
0: P0.7, P0.6, and P0.5 functions are determined by the Crossbar or the Port latches.
1: If EMI0CF.4 = '0' (External Memory Interface is in Multiplexed mode)
P0.7 (/WR), P0.6 (/RD), and P0.5 (ALE) are 'skipped' by the Crossbar and their output states are determined by the Port latches and the External Memory Interface.
1: If EMI0CF.4 = '1' (External Memory Interface is in Non-multiplexed mode)
P0.7 (/WR) and P0.6 (/RD) are 'skipped' by the Crossbar and their output states are determined by the Port latches and the External Memory Interface.

Bit0: CNVSTE: External Convert Start Input Enable Bit.
0: CNVSTR unavailable at Port pin.
1: CNVSTR routed to Port pin.

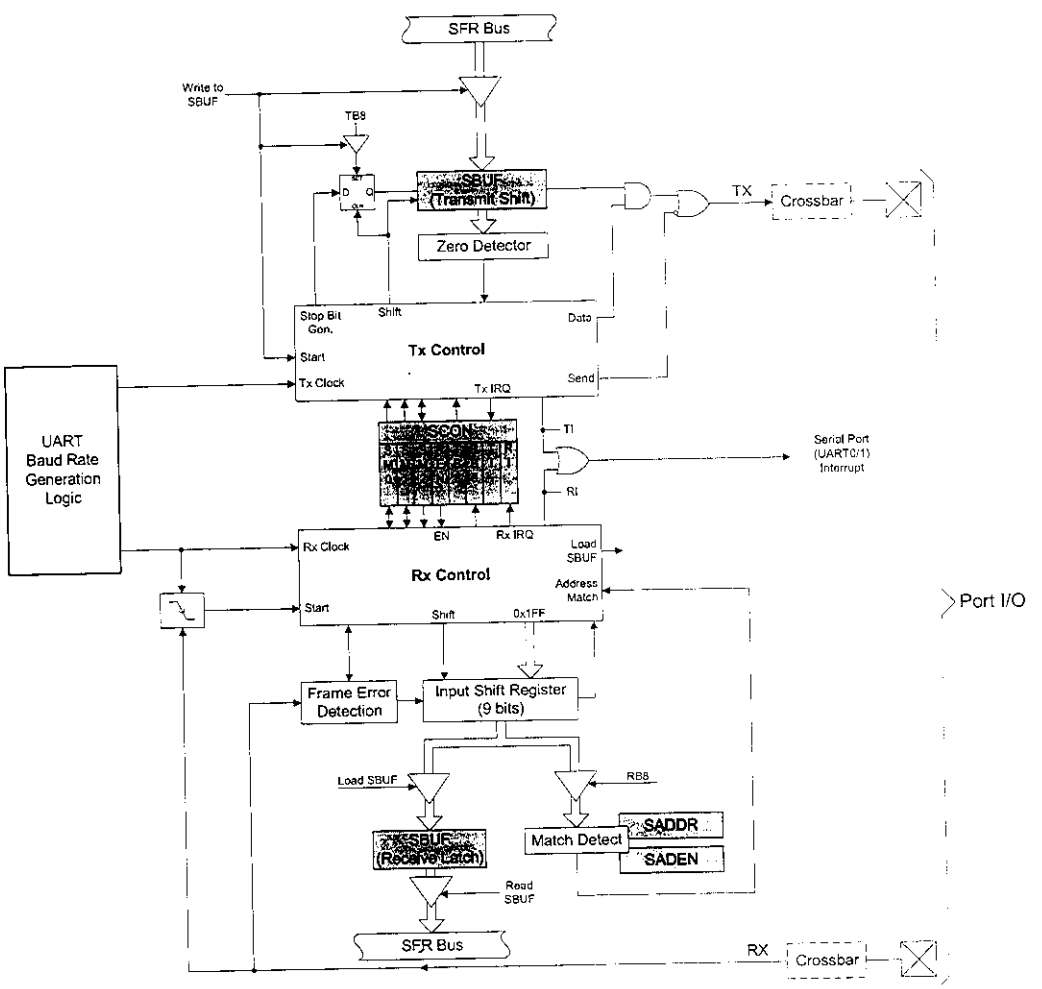
20. UART0

UART0 is an enhanced serial port with frame error detection and address recognition hardware. UART0 may operate in full-duplex asynchronous or half-duplex synchronous modes, and mutiprocecessor communication is fully supported. Receive data is buffered in a holding register, allowing UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte. A Receive Overrun bit indicates when new received data is latched into the receive buffer before the previous received byte is read.

UART0 is accessed via its associated SFRs, Serial Control (SCON0) and Serial Data Buffer (SBUF0). The single SBUF0 location provides access to both transmit and receive registers. Reads access the Receive register and writes access the Transmit register automatically.

UART0 may be operated in polled or interrupt mode. UART0 has two sources of interrupts: a Transmit Interrupt flag, TI0 (SCON0.1) set when transmission of a data byte is complete, and a Receive Interrupt flag, RI0 (SCON0.0) set when reception of a data byte is complete. UART0 interrupt flags are not cleared by hardware when the CPU vectors to the interrupt service routine; they must be cleared manually by software. This allows software to determine the cause of the UART0 interrupt (transmit complete or receive complete).

Figure 20.1. UART0 Block Diagram



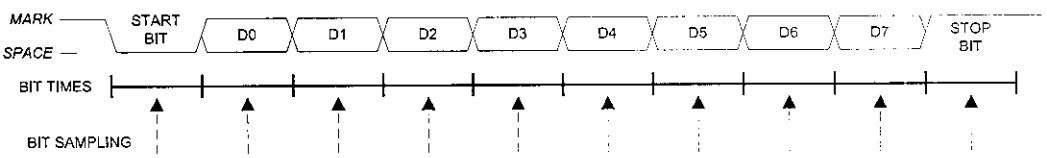
20.1.2. Mode 1: 8-Bit UART, Variable Baud Rate

Mode 1 provides standard asynchronous, full duplex communication using a total of 10 bits per data byte: one start bit, eight data bits (LSB first), and one stop bit. Data are transmitted from the TX0 pin and received at the RX0 pin. On receive, the eight data bits are stored in SBUF0 and the stop bit goes into RB80 (SCON0.2).

Data transmission begins when an instruction writes a data byte to the SBUF0 register. The TI0 Transmit Interrupt Flag (SCON0.1) is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN0 Receive Enable bit (SCON0.4) is set to logic 1. After the stop bit is received, the data byte will be loaded into the SBUF0 receive register if the following conditions are met: RI0 must be logic 0, and if SM20 is logic 1, the stop bit must be logic 1.

If these conditions are met, the eight bits of data are stored in SBUF0, the stop bit is stored in RB80 and the RI0 flag is set. If these conditions are not met, SBUF0 and RB80 will not be loaded and the RI0 flag will not be set. An interrupt will occur if enabled when either TI0 or RI0 is set.

Figure 20.4. UART0 Mode 1 Timing Diagram



The baud rate generated in Mode 1 is a function of timer overflow, shown in Equation 20.1 and Equation 20.2. UART0 can use Timer 1 operating in *8-Bit Auto-Reload Mode*, or Timer 2 operating in *Baud Rate Generator Mode* to generate the baud rate (note that the TX and RX clocks are selected separately). On each timer overflow event (a roll-over from all ones - (0xFF for Timer 1, 0xFFFF for Timer 2) - to zero) a clock is sent to the baud rate logic.

Timer 2 is selected as TX and/or RX baud clock source by setting the TCLK0 (T2CON.4) and/or RCLK0 (T2CON.5) bits, respectively (see **Section "22. TIMERS" on page 223** for complete timer configuration details). When either TCLK0 or RCLK0 is set to logic 1, Timer 2 is forced into *Baud Rate Generator Mode*, with SYSCLK / 2 as its clock source. If TCLK0 and/or RCLK0 is logic 0, Timer 1 acts as the baud clock source for the TX and/or RX circuits, respectively.

The Mode 1 baud rate equations are shown below, where T1M is the Timer 1 Clock Select bit (register CKCON), TH1 is the 8-bit reload register for Timer 1, SMOD0 is the UART0 baud rate doubler (register PCON) and [RCAP2H , RCAP2L] is the 16-bit reload register for Timer 2.

Equation 20.1. Mode 1 Baud Rate using Timer 1

$$BaudRate = \left(\frac{2^{SMOD0}}{32}\right) \times \left(\frac{SYSCLK \times 12^{(T1M-1)}}{(256 - TH1)}\right)$$

Equation 20.2. Mode 1 Baud Rate using Timer 2

$$BaudRate = \frac{SYSCLK}{32 \times (65536 - [RCAP2H, RCAP2L])}$$

Figure 20.8. SCON0: UART0 Control Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
SM00/FE0	SM10/RXOV0	SM20/TXCOL0	REN0	TB80	RB80	TI0	RI0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x98

Bits7-6: The function of these bits is determined by the SSTAT0 bit in register PCON.
If SSTAT0 is logic 1, these bits are UART0 status indicators as described in Section 20.3.
If SSTAT0 is logic 0, these bits select the Serial Port Operation Mode as shown below.
SM00-SM10: Serial Port Operation Mode:

SM00	SM10	Mode
0	0	Mode 0: Synchronous Mode
0	1	Mode 1: 8-Bit UART, Variable Baud Rate
1	0	Mode 2: 9-Bit UART, Fixed Baud Rate
1	1	Mode 3: 9-Bit UART, Variable Baud Rate

Bit5: SM20: Multiprocessor Communication Enable.
The function of this bit is dependent on the Serial Port Operation Mode.
Mode 0: No effect.
Mode 1: Checks for valid stop bit.
0: Logic level of stop bit is ignored.
1: RI0 will only be activated if stop bit is logic level 1.
Modes 2 and 3: Multiprocessor Communications Enable.
0: Logic level of ninth bit is ignored.
1: RI0 is set and an interrupt is generated only when the ninth bit is logic 1 and the received address matches the UART0 address or the broadcast address.

Bit4: REN0: Receive Enable.
This bit enables/disables the UART0 receiver.
0: UART0 reception disabled.
1: UART0 reception enabled.

Bit3: TB80: Ninth Transmission Bit.
The logic level of this bit will be assigned to the ninth transmission bit in Modes 2 and 3. It is not used in Modes 0 and 1. Set or cleared by software as required.

Bit2: RB80: Ninth Receive Bit.
The bit is assigned the logic level of the ninth bit received in Modes 2 and 3. In Mode 1, if SM20 is logic 0, RB80 is assigned the logic level of the received stop bit. RB8 is not used in Mode 0.

Bit1: TI0: Transmit Interrupt Flag.
Set by hardware when a byte of data has been transmitted by UART0 (after the 8th bit in Mode 0, or at the beginning of the stop bit in other modes). When the UART0 interrupt is enabled, setting this bit causes the CPU to vector to the UART0 interrupt service routine. This bit must be cleared manually by software

Bit0: RI0: Receive Interrupt Flag.
Set by hardware when a byte of data has been received by UART0 (as selected by the SM20 bit). When the UART0 interrupt is enabled, setting this bit causes the CPU to vector to the UART0 interrupt service routine. This bit must be cleared manually by software.

22. TIMERS

The C8051F020/1/2/3 devices contain 5 counter/timers: three are 16-bit counter/timers compatible with those found in the standard 8051, and two are 16-bit auto-reload timers for use with the ADCs, SMBus, UART1, or for general purpose use. These can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. Timer 2 offers additional capabilities not available in Timers 0 and 1. Timer 3 is similar to Timer 2, but without the capture or Baud Rate Generator modes. Timer 4 is identical to Timer 2, and can supply baud-rate generation capabilities to UART1.

Timer 0 and Timer 1:	**Timer 2:**	**Timer 3:**	**Timer 4**
13-bit counter/timer	16-bit counter/timer with auto-reload	16-bit timer with auto-reload	16-bit counter/timer with auto-reload
16-bit counter/timer	16-bit counter/timer with capture		16-bit counter/timer with capture
8-bit counter/timer with auto-reload	Baud rate generator for UART0		Baud rate generator for UART1
Two 8-bit counter/timers (Timer 0 only)			

When functioning as a timer, the counter/timer registers are incremented on each clock tick. Clock ticks are derived from the system clock divided by either one or twelve as specified by the Timer Clock Select bits (T4M-T0M) in CKCON, shown in Figure 22.1. The twelve-clocks-per-tick option provides compatibility with the older generation of the 8051 family. Applications that require a faster timer can use the one-clock-per-tick option.

When functioning as a counter, a counter/timer register is incremented on each high-to-low transition at the selected input pin. Events with a frequency of up to one-fourth the system clock's frequency can be counted. The input signal need not be periodic, but it should be held at a given level for at least two full system clock cycles to ensure the level is sampled.

Figure 22.5. TCON: Timer Control Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
							(bit addressable)	0x88

Bit7: TF1: Timer 1 Overflow Flag.
Set by hardware when Timer 1 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 1 interrupt service routine.
0: No Timer 1 overflow detected.
1: Timer 1 has overflowed.

Bit6: TR1: Timer 1 Run Control.
0: Timer 1 disabled.
1: Timer 1 enabled.

Bit5: TF0: Timer 0 Overflow Flag.
Set by hardware when Timer 0 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 0 interrupt service routine.
0: No Timer 0 overflow detected.
1: Timer 0 has overflowed.

Bit4: TR0: Timer 0 Run Control.
0: Timer 0 disabled.
1: Timer 0 enabled.

Bit3: IE1: External Interrupt 1.
This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 1 service routine if IT1 = 1. This flag is the inverse of the /INT1 input signal's logic level when IT1 = 0.

Bit2: IT1: Interrupt 1 Type Select.
This bit selects whether the configured /INT1 signal will detect falling edge or active-low level-sensitive interrupts.
0: /INT1 is level triggered.
1: /INT1 is edge triggered.

Bit1: IE0: External Interrupt 0.
This flag is set by hardware when an edge/level of type defined by IT0 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 0 service routine if IT0 = 1. This flag is the inverse of the /INT0 input signal's logic level when IT0 = 0.

Bit0: IT0: Interrupt 0 Type Select.
This bit selects whether the configured /INT0 signal will detect falling edge or active-low level-sensitive interrupts.
0: /INT0 is level triggered.
1: /INT0 is edge triggered.

Figure 22.6. TMOD: Timer Mode Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
GATE1	C/T1	T1M1	T1M0	GATE0	C/T0	T0M1	T0M0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x89

Bit7: GATE1: Timer 1 Gate Control.
0: Timer 1 enabled when TR1 = 1 irrespective of /INT1 logic level.
1: Timer 1 enabled only when TR1 = 1 AND /INT1 = logic 1.

Bit6: C/T1: Counter/Timer 1 Select.
0: Timer Function: Timer 1 incremented by clock defined by T1M bit (CKCON.4).
1: Counter Function: Timer 1 incremented by high-to-low transitions on external input pin (T1).

Bits5-4: T1M1-T1M0: Timer 1 Mode Select.
These bits select the Timer 1 operation mode.

T1M1	T1M0	Mode
0	0	Mode 0: 13-bit counter/timer
0	1	Mode 1: 16-bit counter/timer
1	0	Mode 2: 8-bit counter/timer with auto-reload
1	1	Mode 3: Timer 1 inactive

Bit3: GATE0: Timer 0 Gate Control.
0: Timer 0 enabled when TR0 = 1 irrespective of /INT0 logic level.
1: Timer 0 enabled only when TR0 = 1 AND /INT0 = logic 1.

Bit2: C/T0: Counter/Timer Select.
0: Timer Function: Timer 0 incremented by clock defined by T0M bit (CKCON.3).
1: Counter Function: Timer 0 incremented by high-to-low transitions on external input pin (T0).

Bits1-0: T0M1-T0M0: Timer 0 Mode Select.
These bits select the Timer 0 operation mode.

T0M1	T0M0	Mode
0	0	Mode 0: 13-bit counter/timer
0	1	Mode 1: 16-bit counter/timer
1	0	Mode 2: 8-bit counter/timer with auto-reload
1	1	Mode 3: Two 8-bit counter/timers

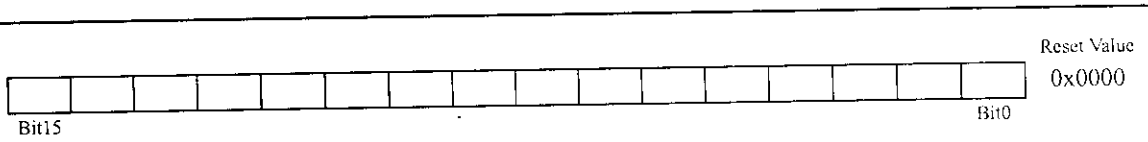
24. JTAG (IEEE 1149.1)

Each MCU has an on-chip JTAG interface and logic to support boundary scan for production and in-system testing, Flash read/write operations, and non-intrusive in-circuit debug. The JTAG interface is fully compliant with the IEEE 1149.1 specification. Refer to this specification for detailed descriptions of the Test Interface and Boundary-Scan Architecture. Access of the JTAG Instruction Register (IR) and Data Registers (DR) are as described in the Test Access Port and Operation of the IEEE 1149.1 specification.

The JTAG interface is accessed via four dedicated pins on the MCU: TCK, TMS, TDI, and TDO.

Through the 16-bit JTAG Instruction Register (IR), any of the eight instructions shown in Figure 1.1 can be commanded. There are three DR's associated with JTAG Boundary-Scan, and four associated with Flash read/write operations on the MCU.

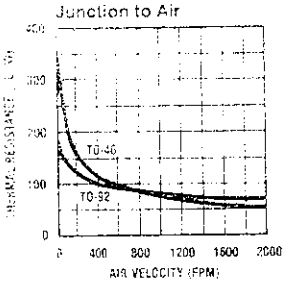
Figure 24.1. IR: JTAG Instruction Register



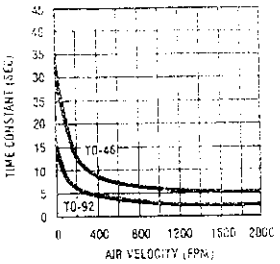
IR Value	Instruction	Description
0x0000	EXTEST	Selects the Boundary Data Register for control and observability of all device pins
0x0002	SAMPLE/ PRELOAD	Selects the Boundary Data Register for observability and presetting the scan-path latches
0x0004	IDCODE	Selects device ID Register
0xFFFF	BYPASS	Selects Bypass Data Register
0x0082	Flash Control	Selects FLASHCON Register to control how the interface logic responds to reads and writes to the FLASHDAT Register
0x0083	Flash Data	Selects FLASHDAT Register for reads and writes to the Flash memory
0x0084	Flash Address	Selects FLASHADR Register which holds the address of all Flash read, write, and erase operations
0x0085	Flash Scale	Selects FLASHSCL Register which controls the Flash one-shot timer and read-always enable

Typical Performance Characteristics

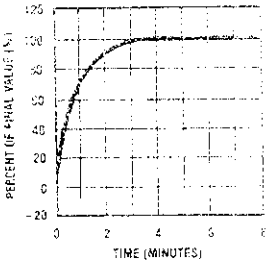
Thermal Resistance Junction to Air



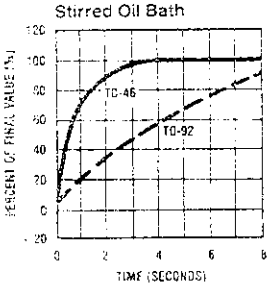
Thermal Time Constant



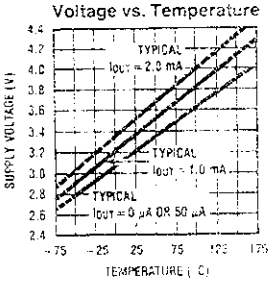
Thermal Response in Still Air



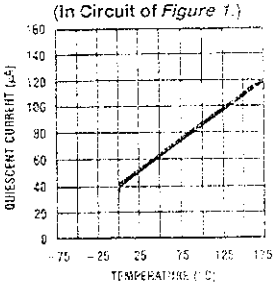
Thermal Response in Stirred Oil Bath



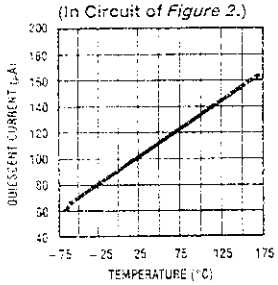
Minimum Supply Voltage vs. Temperature



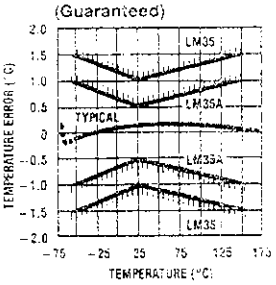
Quiescent Current vs. Temperature (In Circuit of *Figure 1*.)



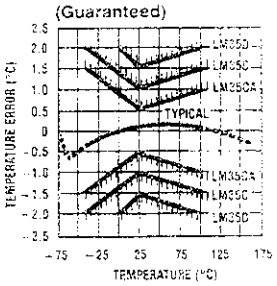
Quiescent Current vs. Temperature (In Circuit of *Figure 2*.)



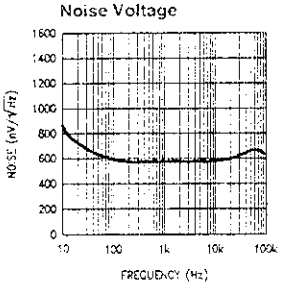
Accuracy vs. Temperature (Guaranteed)



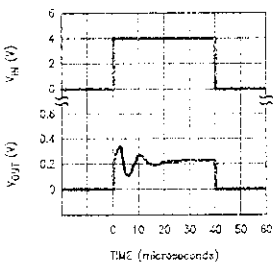
Accuracy vs. Temperature (Guaranteed)



Noise Voltage



Start-Up Response



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input–Output Voltage Differential	$V_I–V_O$	35	Vdc
Power Dissipation	P_D	Internally Limited	W
Operating Junction Temperature Range	T_J	−40 to +125	C
Storage Temperature Range	T_{stg}	−65 to +150	C
Soldering Lead Temperature (10 seconds)	T_{solder}	300	C

ELECTRICAL CHARACTERISTICS ($V_I–V_O$ = 5.0 V; I_L = 1.5 A; T_J = T_{low} to T_{high}; P_{max} [Note 1], unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Line Regulation (Note 2) T_A = 25 C, 3.0 V ≤ $V_I–V_O$ ≤ 35 V	1	Reg_{line}	–	0.0005	0.03	%/V
Load Regulation (Note 2) T_A = 25°C, 10 mA < I_L ≤ 3.0 A	2	Reg_{load}				
V_O ≤ 5.0 V				5.0	25	mV
V_O ≥ 5.0 V			–	0.1	0.5	% V_O
Thermal Regulation, Pulse = 20 ms, (T_A = +25°C)		Reg_{therm}	–	0.002	–	% V_O/W
Adjustment Pin Current	3	I_{Adj}	–	50	100	μA
Adjustment Pin Current Change 3.0 V ≤ $V_I–V_O$ ≤ 35 V 10 mA < I_L ≤ 3.0 A, P_D ≤ P_{max}	1,2	ΔI_{Adj}	–	0.2	5.0	μA
Reference Voltage 3.0 V ≤ $V_I–V_O$ ≤ 35 V 10 mA ≤ I_O ≤ 3.0 A, P_D ≤ P_{max}	3	V_{ref}	1.20	1.25	1.30	V
Line Regulation (Note 2) 3.0 V ≤ $V_I–V_O$ ≤ 35 V	1	Reg_{line}	–	0.02	0.07	%/V
Load Regulation (Note 2) 10 mA < I_L ≤ 3.0 A	2	Reg_{load}				
V_O ≤ 5.0 V			–	20	70	mV
V_O ≥ 5.0 V			–	0.3	1.5	% V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	–	1.0	–	% V_O
Minimum Load Current to Maintain Regulation ($V_I–V_O$ = 35 V)	3	$I_{L,min}$	–	3.5	10	mA
Maximum Output Current $V_I–V_O$ ≤ 10 V, P_D ≤ P_{max} $V_I–V_O$ = 30 V, P_D ≤ P_{max}, T_A = 25°C	3	I_{max}	 3.0 0.25	 4.5 1.0	 – –	A
RMS Noise, % of V_O T_A= 25°C, 10 Hz ≤ f ≤ 10 kHz		N	–	0.003	–	% V_O
Ripple Rejection, V_O = 10 V, f = 120 Hz (Note 3) Without C_{Adj} C_{Adj} = 10 μF	4	RR	 – 66	 65 80	 – –	dB
Long Term Stability, T_J = T_{high} (Note 4) T_A= 25°C for Endpoint Measurements	3	S	–	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance, Junction–to–Case Peak (Note 5) Average (Note 6)		$R_{\theta JC}$	 – –	 2.0 –	 – 1.5	C/W

NOTES: 1. T_{low} to T_{high} = 0° to +125°C; P_{max} = 25 W for LM350T; T_{low} to T_{high} = −40° to +125°C, P_{max} = 25 W for LM350BT.
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
3. C_{Adj}, when used, is connected between the adjustment pin and ground.
4. Since Long–Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
5. Thermal Resistance evaluated measuring the hottest temperature on the die using an infrared scanner. This method of evaluation yields very accurate thermal resistance values which are conservative when compared to the other measurement techniques.
6. The average die temperature is used to derive the value of thermal resistance junction to case (average).

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Input Voltage (for V_O = 5V to 18V) (for V_O = 24V)	V_I V_I	35 40	V V
Thermal Resistance Junction-Cases (TO-220)	$R_{\theta JC}$	5	°C/W
Thermal Resistance Junction-Air (TO-220)	$R_{\theta JA}$	65	°C/W
Operating Temperature Range	T_{OPR}	0 ~ +125	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

Electrical Characteristics (MC7805/LM7805)

(Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I = 10V. C_I= 0.33µF, C_O= 0.1µF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7805/LM7805 Min.	Typ.	Max.	Unit
Output Voltage	V_O	T_J =+25 °C		4.8	5.0	5.2	V
		5.0mA ≤ I_O ≤ 1.0A, P_O ≤ 15W V_I = 7V to 20V		4.75	5.0	5.25	V
Line Regulation (Note1)	Regline	T_J=+25 °C	V_O = 7V to 25V	-	4.0	100	mV
			V_I = 8V to 12V	-	1.6	50	mV
Load Regulation (Note1)	Regload	T_J=+25 °C	I_O = 5.0mA to1.5A	-	9	100	mV
			I_O =250mA to 750mA	-	4	50	mV
Quiescent Current	I_Q	T_J =+25 °C		-	5.0	8.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1.0A		-	0.03	0.5	mA
		V_I= 7V to 25V		-	0.3	1.3	mA
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O= 5mA		-	-0.8	-	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A=+25 °C		-	42	-	µV/V
Ripple Rejection	RR	f = 120Hz V_O = 8V to 18V		62	73	-	dB
Dropout Voltage	V_{Drop}	I_O = 1A, T_J =+25 °C		-	2	-	V
Output Resistance	r_O	f = 1KHz		-	15	-	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A =+25 °C		-	230	-	mA
Peak Current	I_{PK}	T_J =+25 °C		-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (Note 1) (Note 6) (Continued)

Parameter	Conditions	LM35			LM35C, LM35D			Units (Max.)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy, LM35, LM35C (Note 7)	T_A = +25°C	±0.4	±1.0		±0.4	±1.0		°C
	T_A = −10°C	±0.5			±0.5		±1.5	°C
	T_A = T_{MAX}	+0.8	+1.5		±0.8		1.5	°C
	T_A = T_{MIN}	±0.8		±1.5	±0.8		±2.0	°C
Accuracy, LM35D (Note 7)	T_A = +25°C				±0.6	±1.5		°C
	T_A = T_{MAX}				±0.9		±2.0	°C
	T_A = T_{MIN}				±0.9		±2.0	°C
Nonlinearity (Note 8)	$T_{MIN} \le T_A \le T_{MAX}$	**±0.3**		**±0.5**	**±0.2**		**±0.5**	°C
Sensor Gain (Average Slope)	$T_{MIN} \le T_A \le T_{MAX}$	**+10.0**	**+9.8, +10.2**		**+10.0**		**+9.8, +10.2**	mV/°C
Load Regulation (Note 3) $0 \le I_L \le 1$ mA	T_A = +25°C	±0.4	+2.0		±0.4	±2.0		mV/mA
	$T_{MIN} \le T_A \le T_{MAX}$	**±0.5**		**±5.0**	**±0.5**		**±5.0**	mV/mA
Line Regulation (Note 3)	T_A = +25°C	±0.01	±0.1		±0.01	±0.1		mV/V
	$4V \le V_S \le 30V$	**±0.02**		**0.2**	**±0.02**		**0.2**	mV/V
Quiescent Current (Note 9)	V_S = +5V, +25°C	56	80		56	80		µA
	V_S = +5V	**105**		**158**	**91**		**138**	µA
	V_S = +30V, +25°C	56.2	82		56.2	82		µA
	V_S = +30V	**105.5**		**161**	**91.5**		**141**	µA
Change of Quiescent Current (Note 3)	$4V \le V_S \le 30V$, +25°C	0.2	2.0		0.2	2.0		µA
	$4V \le V_S \le 30V$	**0.5**		**3.0**	**0.5**		**3.0**	µA
Temperature Coefficient of Quiescent Current		**+0.39**		**+0.7**	**+0.39**		**+0.7**	µA/°C
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, I_L = 0	+1.5		+2.0	+1.5		+2.0	°C
Long Term Stability	T_J = T_{MAX}, for 1000 hours	±0.08			±0.08			°C

Note 3: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Note 4: Tested Limits are guaranteed and 100% tested in production.

Note 5: Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Specifications in **boldface** apply over the full rated temperature range.

Note 7: Accuracy is defined as the error between the output voltage and 10mV/°C times the device's case temperature, at specified conditions of voltage, current, and temperature (expressed in °C).

Note 8: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line, over the device's rated temperature range.

Note 9: Quiescent current is defined in the circuit of *Figure 1*.

Note 10: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. See Note 1.

Note 11: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 12: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

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