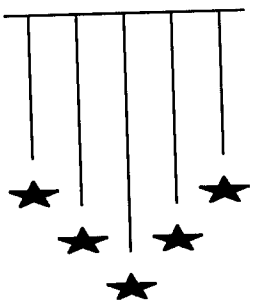
THERMAL PRINTER INTERFACE FOR A GPS BASED CLOCK SYSTEM

PROJECT REPORT 2002-03



P-1398

Submitted by:

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Submitted in partial fulfillment of the requirement for the degree of

BACHELOR OF ENGINEERING

ELECTRONICS & COMMUNICATION ENGINEERING

Bharathiar University, Coimbatore.

Department of Electronics & Communication Engineering

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CERTIFICATE

This is to certify that the project report entitled

THERMAL PRINTER INTERFACE FOR A GPS BASED CLOCK SYSTEM

has been submitted by

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In partial fulfillment for the award of the degree of Bachelor of Engineering in the Electronics and Communication Engineering branch of the Bharathiar University, Coimbatore-641 046 during the academic year 2002-2003.

G Amutha Gow.

(Guide)

(Head of the Department)

Certified that the above candidates were examined by us in the project work viva-voce examination held on 18-03-2003

(Internal Examiner) 18/3

18/3/03

(External Examiner)

Unity Electro Systems

CERTIFICATE

TO WHOMSOEVER IT MAY CONCERN

This is to certify that **Ms.P.Arul Priya**, **Mr.M.Ramesh**, and **Mr.T.Ramesh** and **Ms.T.V.Viji**, final year students of Electronics and Communication Engineering department, Kumaraguru College of Technology, Coimbatore, have successfully completed the project titled **"THERMAL PRINTER INTERFACE FOR A GPS BASED CLOCK"** during the academic year 2002-03 as a part of their curriculum for the Bachelor of Engineering degree in our organization.

They have exhibited tremendous energy and initiative and have performed outstanding work on a challenging project. I take this opportunity to congratulate them and wish these promising engineers all the very best for a bright future.

Place : Coimbatore

Date : 15:03:2003

(Mr.R.Mahalingam)

Director

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We are also extremely thankful to **Ms.G. Amrithagowri M.E.**, our internal guide for her keen interest and untiring efforts towards the completion of our project.

We take the privilege in thanking **Mr. R. Mahalingam and Mr. J. Balamurugan**, Managing Directors of **Unity Electro Systems Pvt. Ltd, Coimbatore** who despite of their tight schedule has offered us excellent practical guidance in the technical field. We also thank all other staff members of **Unity Electro Systems** who offered to guide and helped us throughout the project.

We are also grateful to **Mr. T. Kannaiyyan**, M.Sc., M.Tech., for his unsparing guidance and motivation without whom this project would not have seen the light of the day.

We sincerely thank **Mr. G. C. Thiagarajan** for having guided us in every way and also teaching and non-teaching staff members of the **E.C.E dept** for their constant encouragement during the course of our project.

Last but not the least we thank our parents and friends who have supported us in every way.

SYNOPSIS

Our project sponsor **Unity Electro Systems, Cbe,** has developed a **GPS** based clock system. The GPS based clock system comprises of an arrangement in which a satellite receiver is connected to the clock unit. This unit is done so as to ensure complete synchronization of the International clock time. The purpose of this clock is to record the details of a rally such as time, car number, code number, etc. Our role in the project is to interface a **Thermal Printer** with that clock to print the timing details. This printer, unlike the ordinary printer is compact, functions with low noise and has high printing capabilities and prints on a specialized thermal paper.

In the course of our project, we have assembled a **Stepper Motor Driver** circuit and a high rating **Power Supply (5A)** circuit for energizing the printer. The patterns for numeral generation are user defined and has also been developed.

This interfacing is done with the help of **Atmel 89C52** microcontroller which is a derivative of the 8051 series and the programming is done in **C** with the help of **Keil C** which is a cross compiler between C and 8051 assembly set.

Contents

Software Description

5. Software

- 5.1 State diagram
- 5.2 Generation of stepper sequence
- 5.3 Interrupt handling
- 5.4 Pattern generation
- 5.5 Pattern retrieval and printing
- 5.6 Source coding

Conclusion

Future Developments

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Introduction

Micro-controllers have made a tremendous impact on every aspect of our lives and they play a significant role in the daily functioning of all industrialized societies. Due to their processing power and speed, they have found their niche in the design of stand-alone products and have become the backbone of the workstations that are becoming the revolutionary tool of an engineer.

Our project deals with interfacing a **Thermal Line Printer** to a **GPS** based clock system using the **Atmel 89C52** microcontroller. The GPS based clock system comprises of an arrangement in which a satellite receiver is connected to the clock unit. This unit is done so as to ensure complete synchronization of the International clock time (displayed in the LCD unit) with the IST, which leads the GMT by 5.30 hours. Thus the timing details recorded by the clock reveals a high degree of accuracy, several such clock units are placed at different check points (such as starting point, flying finish, end point, etc.) along the length of the track across which the rally is held.

At the instant a vehicle crosses the system, a manual trigger is given and thereby the corresponding clock unit records the instantaneous time. The car number and service number is then typed using the keypad which is integrated with the clock circuitry and the time displayed in the LCD unit is recorded, as well as the time displayed in the LCD unit is printed via the **Thermal Printer**.

Introduction:

The thermal line printers are ideal for applications, which involve very high resolution-labeling electronic components, telecommunication assemblies, computer peripherals, small pharmaceutical packaging, diagnostic research samples and much more. The print head ensures 'graphics and bar codes' print clarity and therefore these printers are the industrial strength printers for bar code automation and centralized printers within industrial environments. They also enable printing of receipts with logos or rebate certificates while decreasing the customer wait time.

Epson M-T51:

Several series of thermal printers are available in the market like the MTP series, STP series, etc. The major advantages of these printers are that they are compact, inexpensive and their high-speed line head.

EPSON M-51 best suits our application because it incorporates several additional features which have been mentioned below.

Features:

- Low noise
- High speed printing: 52 mm/s (7.5 v, 25°C)
- Compact and light mass: 69.15(W) x 51.2(D) x 17.3(H) mm
- High quality printing: 6 dots/mm
- Strong and Durable

General Specifications:

Printing method: Thermal line dot printing

Total no. Of dots: 288 dots /dot line

Printing format:

Dot Pitch Vertical direction : 0.167 mm
Horizontal direction: 0.174 mm

Example printing:

Character structure: 8(W) x20 (H) dots font
(Including a horizontal 2-dot space)

Character size :1.67 x 4.17 mm

Column pitch :2.00 mm

Line pitch :5.21mm

Number of columns: 20(8 x20 dots per character)

Printing speed:

Maximum 52 mm/s
(Approximately 10 lps at a line pitch of 5.2 mm at 7.5v of the motor terminal voltage)
[lps : lines per second]

Paper feeding:

Paper feed method : **Friction** feed (unidirectional)

Minimum paper feed pitch : 0.087 mm

Feeding speed : 52 mm/s

Control Method : **Stepping** motor

Paper feed direction : Forward

Paper roll supply load : 0.59 N (60 gf or less at paper entrance)

Paper type:

Paper type : Single-ply thermal paper roll

Specified paper :

Original Paper No.	Manufacturer
KF50	KANZAN
TF50KS-E2C	Nippon Paper industries
P350	KSP

Size : 57.5 ± 0.5(width) mm

Specification for paper roll:

Paper roll diameter : Maximum 80 mm

Paper surface direction: The colored surface of the paper should be on the Outside.

Paper end termination: The tip of the paper should not be pasted to the Paper spool.

Paper end mark : When printing a paper end mark on the colored Surface; never use ink that affects printing quality or that may damages the print head.

Motor:

Paper feed motor : 4-phase bipolar stepping motor

Mass : Approximately 70 g

Power supply voltage:

Power supply voltage : 7.5 + .5 / - 1.5 V (at terminal of FFC)
(The same power source must be used for both the Print head and the motor)

Circuit input voltage : 5 ± 0.25 V DC (at terminal of FFC)

Print head specifications:

Head element density : 6 dots / mm (.167 mm/dot)

Total number of head elements : 288 dots / dot line

Available printing width : 48 mm

Heat element typical resistance value: 210 ± 8.4 ohms

Reliability:

Life : 6,000,000 lines
End of life is defined as the point at which the printer Reaches the beginning of the wear out period.

MCBF: 15,000,000 lines
Average failure interval based on failures relating to the life of 6 million lines and accidental failures

Printer head:

Structure:

Total number of heat elements : 288 dots

Heat element density : 6 dot/mm (0.167 mm/dot)

Heat element typical resistance value : 210 ± 8.4 ohms(including heat element only)

Specifications:

Current consumption:

Peak current : 4.5 A (the moment 144 dots energizing)

VH max: Head connector terminal voltage Max 8 V

R min: Head resistance value minimum 201.6 ohms

R com: Common resistance value 0.05 ohms

R ic : Driver-on resistance value 50 ohms

R icad : Lead resistance value 10 ohms

Mean current : Approximately 2.1 A
(Head terminal voltage VH=7.5V,printing ratio of 25%, Energizing pulse width 1.351 ms, Cycle 1.667ms).

Formula – head drive current:

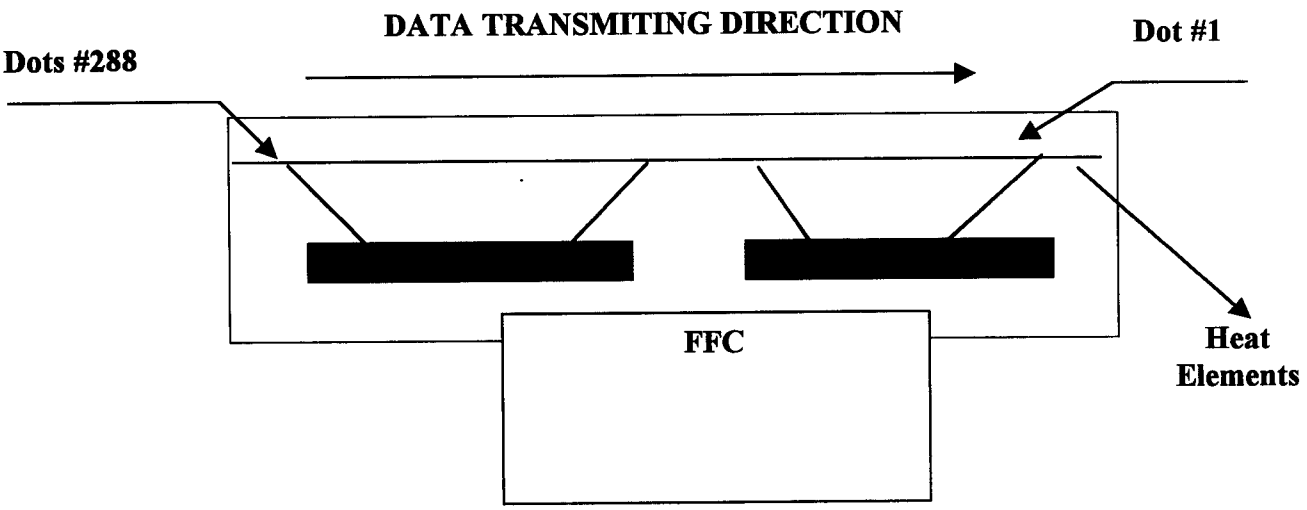
The following formula is used to obtain the head drive current.

$$I_{mean} = \frac{\text{Head terminal voltage}}{\text{Mean resistance of head resistance value}} \times 288 \text{ dots} \times \text{printing ratio} \times \frac{\text{Energizing pulse width}}{\text{Cycle}}$$

Printing ratio: the no. Of printing dots (energizing) /dot line

Print duty : the no. Of printing dots (energizing pulses)/ element / paper Feed amount (two steps including nonprinting area)

Print head diagram:



Thermal head characteristics:

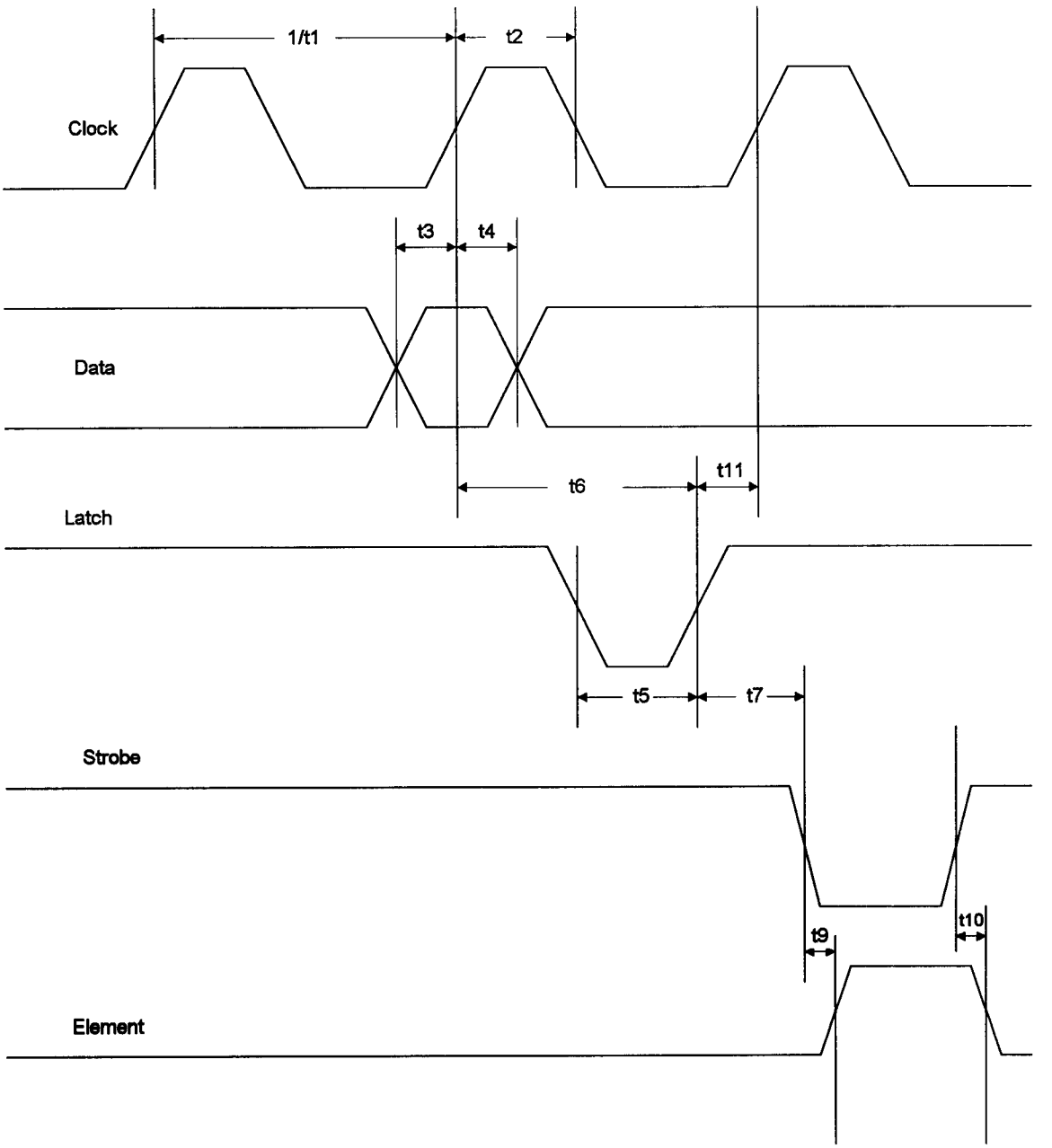
1. Absolute maximum ratings:

Item	Symbol	Terms	Rated Value	Units
Circuit Power Supply	Vdd		7.0	V
Input Voltage	Vin		-0.5 to Vdd to +0.5	V
Power Supply Voltage	Vh		8.5	V
Number of dots energized simultaneously		At Vh=8.5V	144	Dot
Maximum supply energy			0.50	My/dot

2. Allowable Operating Range (T=25°C, Vdd = 5.0V)

Item	Symbol		Terms	Std value			unit
				MIN	TYP	MAX	
Circuit Power Supply	Vdd			4.75	5.0	5.25	
Clock Frequency	T1	f CLK	When connecting cascade	_	_	4	MHz
Clock Pulse Width	T2	tw CLK		120	_	_	ns
Setup Time (D1.Clk)	T3	t setup DI		5	_	_	ns
Setup Time (Clk.LAT)	T6	t setup LAT		200	_	_	ns
Setup Time (LAT.STB)	T7	t STB		300	_	_	ns
Hold Time (Clk.DI)	T4	t hold DI		20	_	_	ns
Latch Pulse Width	T5	tw LAT		100	_	_	ns
Latch hold Time	T11	t hold LAT		50	_	_	ns
Output Delay Time (STB 2 Element)	T9 T10	tpd ELEMENT		_	_	5	µs

Timing diagram:

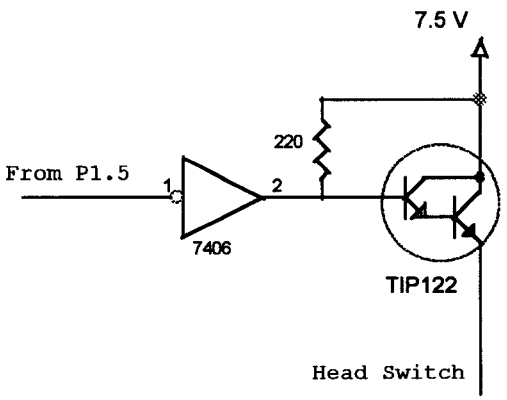


Electrical Characteristics (T =25°C, Vdd=5.0V):

Item	Symbol	Terminals	Terms	Standard value			Units
				MIN	TYP	MAX	
High Input voltage	V_H	CLK, DI, LAT, STB		0.8Vdd	-	Vdd	V
Low input voltage	V_L	CLK, DI, LAT, STB		0	-	0.2Vdd	V
High input current	I_{H1}	STB		-	-	0.5	μA
	I_{H2}	CLK, LAT		-	-	1.0	μA
	I_{H3}	DI		-	-	0.5	μA
Low input current	I_{L1}	STB		-	-	-30	μA
	I_{L2}	CLK, LAT		-	-	-1.0	μA
	I_{L3}	DI		-	-	-0.5	μA
Low output voltage	V_{OL}	Element		-	1.0	-	V
Current consumption	I_{DD}	Vdd	When each stops fDI = fCLK/2	-	-	12	MA

Print head control switch:

The print head should be energized only at the time of printing. For this purpose this switch has been designed.



Print head energizing pulse width:

A standard pulse width is applied for printing when a 144 dots or less heat element is simultaneously energized and the heat element is not partially energized.

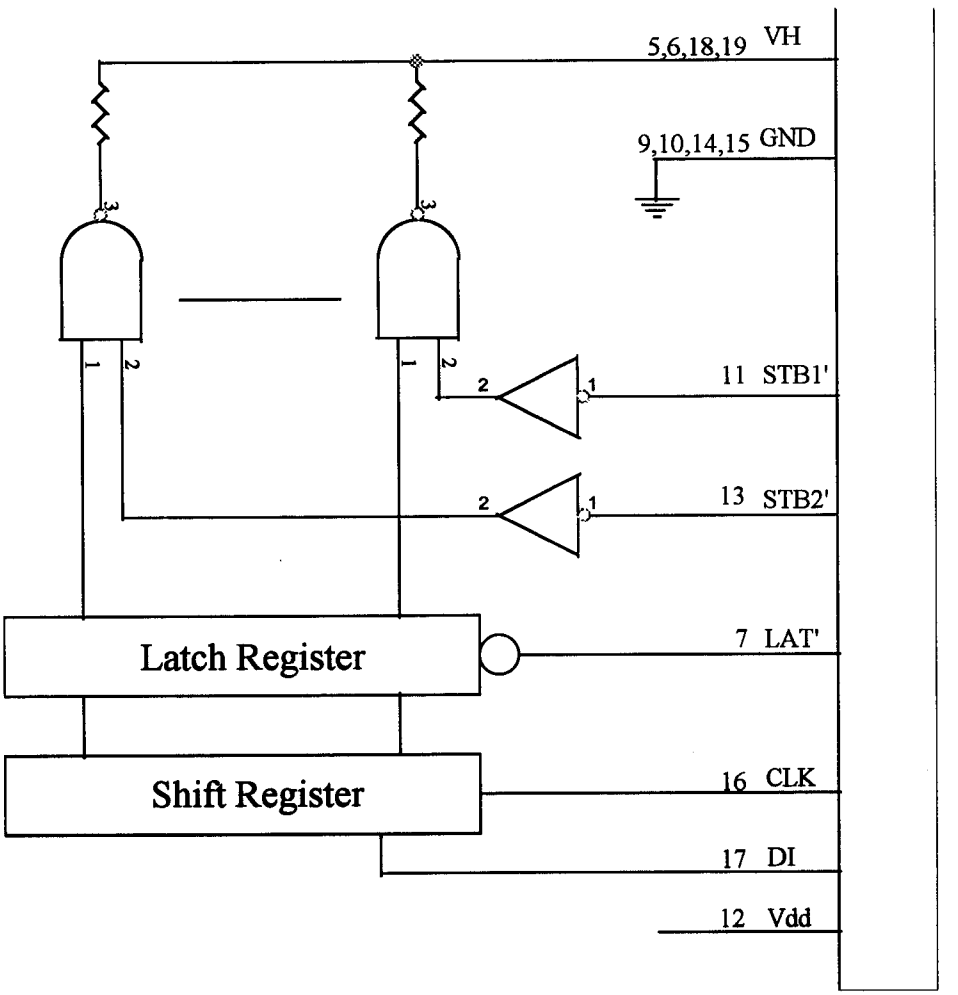
Temp.	Print Head energizing pulse width (μs)		
	V_H= 6v	V_H=7v	V_H=8v
5	3797	2249	1431
10	3552	2100	1363
15	3311	1952	1294
20	3073	1807	1225
25	2839	1665	1156
30	2609	1525	1088
35	2383	1426	1019
40	2161	1330	950
45	2035	1274	910

Strobe signal partition:

Depending on the number of energizing elements for one dot line simultaneously a partition of the strobe signals is made as shown in the following table.

Number of elements energized simultaneously	Number of partitions strobe signal
1 – 144	1
145 – 288	2

Print head block diagram:



STB1, STB2, LAT, CLK are the control signals given to printer.

STB1: is active low and it is used to energize the first 144 elements of the print head.

STB2: is also active low and it is used to energize the next 144 elements of the print head.

LAT : is an active low signal, which is used to latch the incoming data in the latch register.

CLK : is the timing signal which controls the operation of latching and printing data.

V_H : the print head control voltage which activates the printing process.

The print head comprises of 288 heating elements, each element corresponds to a print dot. Each character has a size of 8(W) x 20(H) dots. The first row of dots of the characters to be printed is first shifted to the shift register from which they are latched using the latch register. Simultaneously the second row of dots is passed onto the shift register. The data in the latch and the strobe line (via an inverting buffer) form the inputs to a nand gate. There are 288 such distinct arrangements corresponding to each printing element. The bits in the latch register corresponding to the positions where the dot has to be printed are high and wherever there is a blank space the corresponding bits are 0.

When the STB signal is activated, (STB is active low), the data gets nanded along with it to produce a low voltage at the output of the nand gate. When the V_H line is high, a potential difference is developed between the output of the nand gate and the V_H line. As a result, current flows through the heating element and produces a dot on the thermal paper.

The thermal paper is aluminium coated and a black dot is formed on it only when the area is subjected to heat. The current passing through the heating element produces the required heat.

Stepper motor:

Specifications:

Type : 4 phase bipolar 20 step PM stepping motor

Power supply : 7.5+0.5/-1.5 V DC (at terminal of FFC)

Coil resistance : 21 ± 1Ω (25°C {77°F}/Phase)

Current consumption : Peak current 770 mA
Mean current 430 mA

Drive method : Constant voltage driving using 2 –2 phase excitation

Motor drive sequence:

	Motor Signal Name			
Step	**A**	**B**	**A'**	**B'**
1	ON	ON	OFF	OFF
2	OFF	ON	ON	OFF
3	OFF	OFF	ON	ON
4	ON	OFF	OFF	ON

Two-phase signals are sequentially energized in order to rotate the motor in clockwise direction. To prevent damage to the motor coil due to overheating, continuous energizing to the same phase must not exceed 100ms.Print paper is fed 0.087mm per step.

Voltage regulator:

A voltage regulator is an electronic circuit that provides a stable dc voltage independent of the load current, temperature and ac line voltage variations. Voltage regulators are classified as:

1. **Series regulators**
2. **Switching regulators**

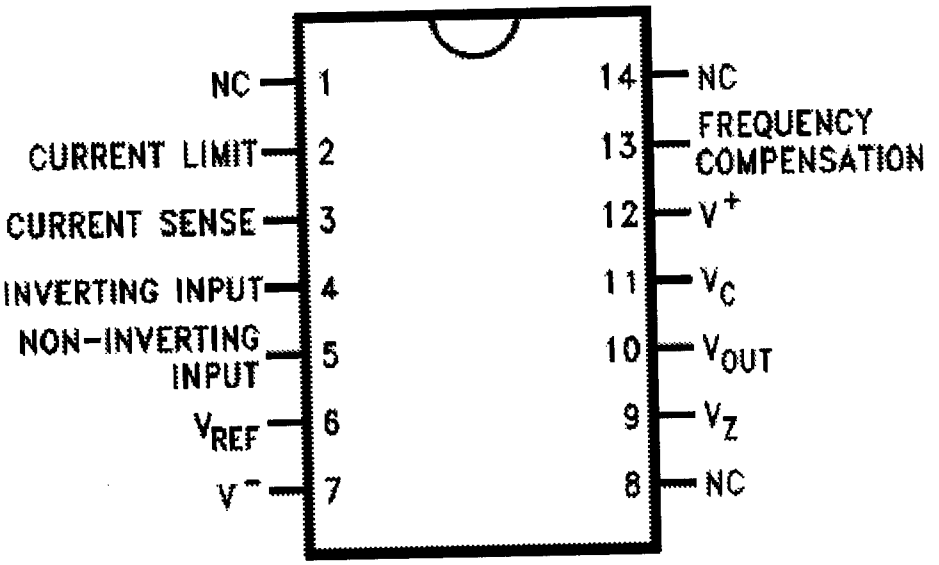
Series regulators use a power transistor connected in series between the unregulated dc input and the load. The continuous voltage drop taking place across the series pass transistors controls the output voltage. Since the transistor conducts in the active or linear region, these regulators are also called linear regulators. Linear regulators may have fixed or variable output voltage and could be positive or negative.

Switching regulators, on the other hand, operate the power transistor as a high frequency on/off switch; so that the power transistor does not conduct current continuously. this gives improved efficiency over series regulators.

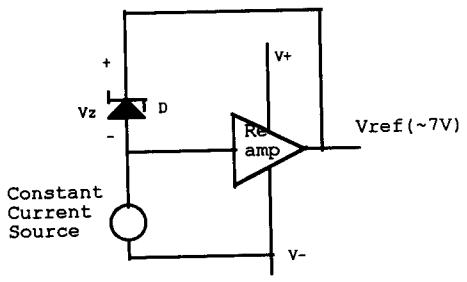
723 General-purpose regulators:

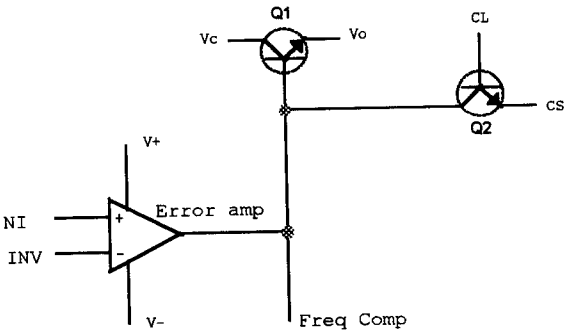
The limitations of the three terminal regulators like no short circuit protection , output voltage is fixed have been overcome in the 723 general purpose regulator, which can be adjusted over a wide range of both positive or negative regulated voltage . This IC is inherently low current device, but can be boosted to provide 5amps or more current by connecting external components. The limitation of 723 is that it has no in-built thermal protection .it also has no short circuit current limits.

723-pin diagram:



723 Functional diagrams:





The 723 regulator has two separate sections. The zener diode, a constant current source and reference amplifier produce a fixed voltage of about 7volts at the terminal Vref .The constant current source forces the zener to operate at a fixed point so that the zener outputs a fixed voltage.

The other section of the IC consists of an error amplifier, a series pass transistor Q1 and a current limit transistor Q2 .The error amplifier compares a sample of the output voltage applied at the INV input terminal to the reference voltage Vref applied at the NI input terminal. The error signal controls the conduction of Q1 .The difference between non-inverting voltage and the output voltage which is directly fed back to the inverting terminal is amplified by the error amplifier. The output of the error amplifier drives the pass transistor Q1 so as to minimize the difference between

The NI and INV inputs of error amplifier.

In high voltage regulator the NI terminal is connected directly to Vref through R3 .so the voltage at the NI terminal is Vref .The error amplifier operates as a non-inverting amplifier with a voltage gain of

$$Av = 1+(R1/R2)$$

So the output voltage for the circuit is

$$Vo = 7.15(1+R1/R2)$$

Specifications:

Input voltage : 12 V dc

Output voltage: 7.5 V dc at 5 A
5 V dc at 500 mA

Design for 7.5 V:

Vo = Vref (1+R1/R2)

Where,

Vo = Output voltage

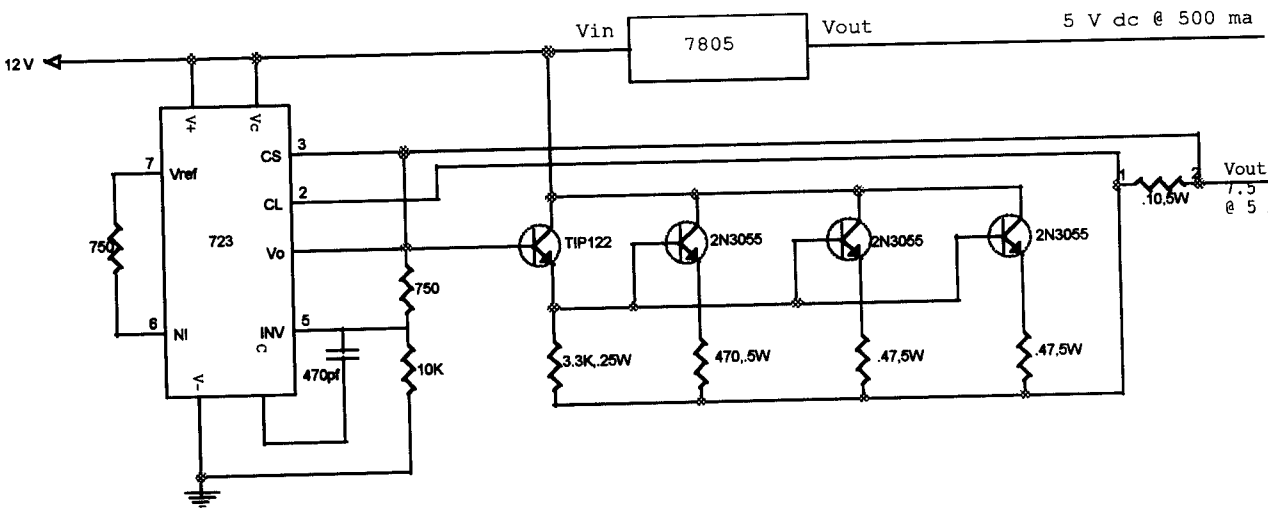
Vref = Reference voltage

Let R1=10 Kohms, R2=750 ohms

Vo = 7.15(1+10000/750)

Vo = 7.5 V

Circuit diagram:



Circuit explanation:

The input to the regulator is 12V, which is taken from Switched Mode Power Supply. The output of 723 is designed for 7.5V. The current needed for energizing the printer head is about 5A, but the 723 will source only about 150mA. In order to increase the current rating to the required level series pass power transistors are used namely **TIP 122**, **TIP 2N3055**, which are in the **Emitter follower** configuration.

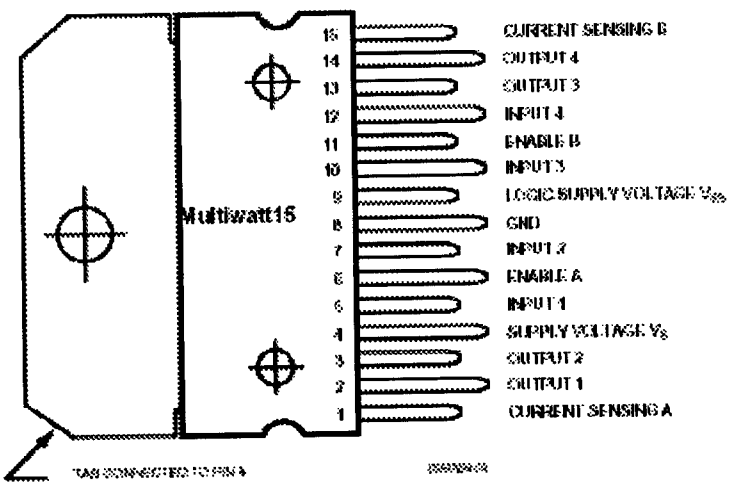
The output taken from 723 is given to the base of TIP 122. The TIP 122 has a β value ranging from 800 – 1000. The TIP 2N3055 has a β value ranging from 20 – 70.This amplified current is given to three TIP 2N3055, which further amplifies the current to the required level. These three (TIP 2N3055) are used to share the load current. The resistor Rs is the current limiting which shuts down the output voltage when the power supply is loaded above the rated value. As the output current is high, the resistors used are chosen in such a way that it can withstand the power.

The 12V from Switched Mode Power Supply is given as input to 7805 whose output is 5V.

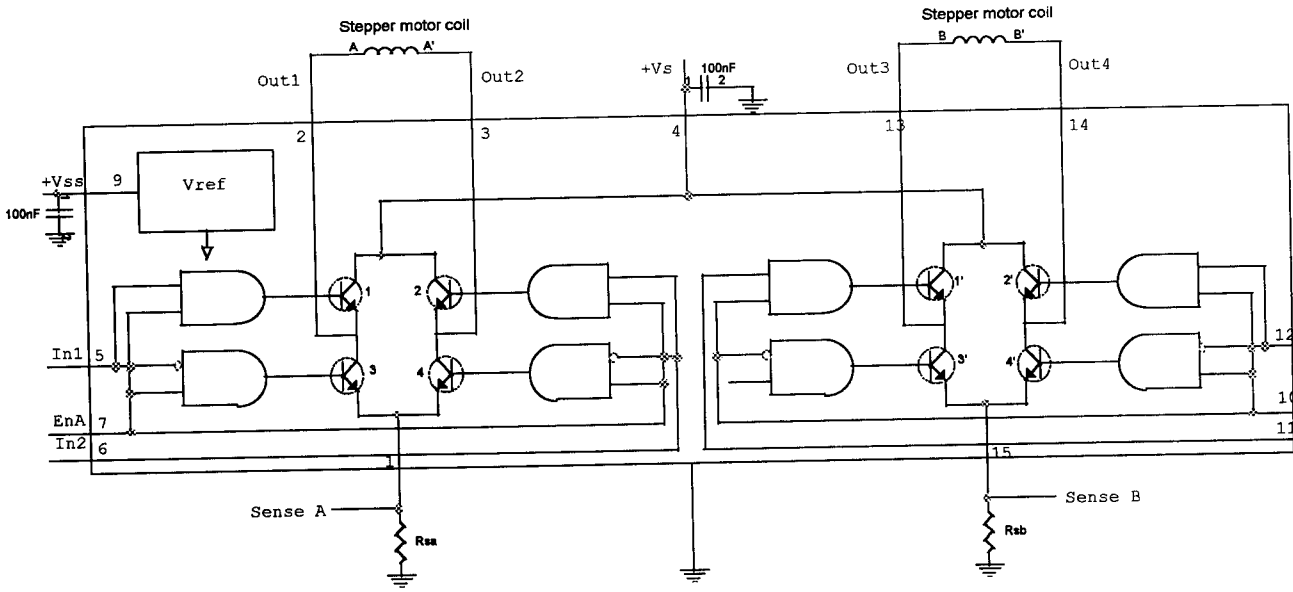
Introduction:

The L298 is an integrated monolithic circuit in a 15-lead Multiwatt and PowerSO20 packages. It is a high voltage, high current dual full-bridge driver designed to accept standard TTL logic levels and drive inductive loads such as relays, solenoids, DC and stepping motors. Two enable inputs are provided to enable or disable the device independently of the input signals. The emitters of the lower transistors of each bridge are connected together and the corresponding external terminal can be used for the connection of an external sensing resistor. An additional supply input is provided so that the logic works at a lower voltage.

Pin diagram:



Internal configuration:

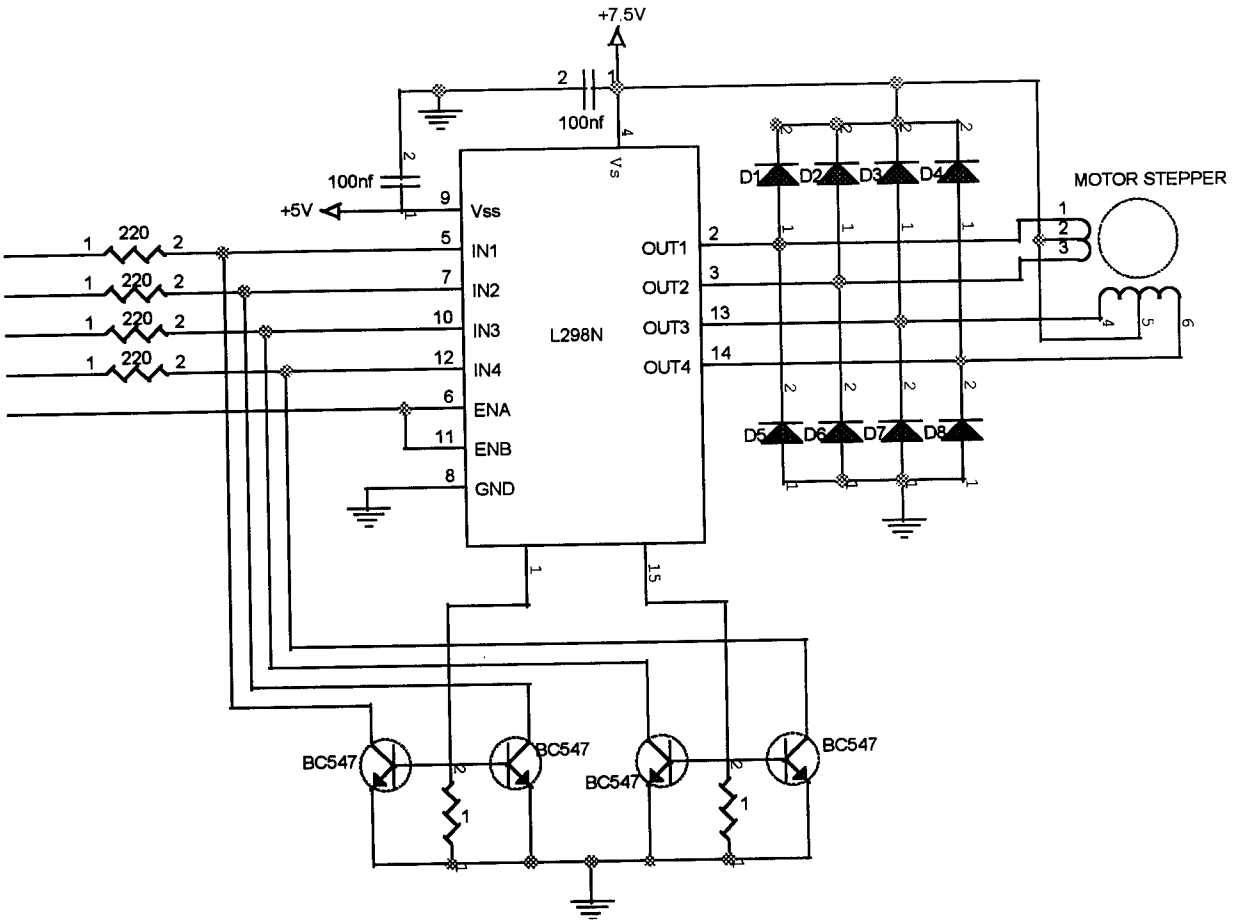


Operation of hex bridge A:

The coil of the stepper motor is connected across OUT 1 and OUT 2. The main operation of hexbridge is to change the direction of current flow through the coil for every sequence. This is done by making the transistor 1 and transistor 4 ON for one direction and transistor 2 and ON for other direction. For clockwise direction, IN 1 should be 1 and IN 2 should be 0, so that the transistor 1 and 4 will be made ON and transistor 2 and 3 will be made OFF. For anticlockwise direction IN 1 should be 0 and IN 2 should be 1, so that the transistor 2 and 3 are made ON and transistor 1 and 4 made OFF.For all outputs to be generated ENABLE should be HIGH.

The operation of hexbridge B is similar to that of A.

Circuit Diagram:



Circuit explanation:

The inputs to L298 driver is given from microcontroller and the outputs of L298 are given as inputs to the stepper motor of the printer. Pins 1 and 15 are grounded through sense resistors. The transistor and sense resistor forms current limiting for a stepper motor.

Design of sense resistor:

$$Rs = \frac{.7}{I}$$

Where,

.7 = base emitter voltage of transistor.

I = maximum current that can flow through the Stepper motor.

Rs = .7 / (770 mA)

Rs = 1 ohm

When the maximum current flow through the resistor, the voltage across the resistor is 0.7V that turns ON the transistor thus grounding the inputs of the driver that prevents energizing the stepper motor coil. The diodes D1 to D8 are called as flywheel diode. When the transistor turns OFF, the collapsing magnetic field in the inductor keeps the current flowing for a while. This current cannot flow through the transistor because it is OFF. Instead, this current develops a voltage across the inductor. This induced voltage, called, as **"inductive kick"** will usually be large enough to breakdown the transistor. When the coil is conducting, the diode is reverse biased, so it doesn't conduct. However, as soon as the induced voltage reaches .7V, the diode turns ON, supplies a return path for the induced current. The voltage across the inductor then is clamped at .7v, the voltage across a conducting dode, so the transistor is saved.

Introduction:

A Micro controller consists of a powerful CPU tightly coupled with memory (RAM, ROM, or EPROM), various Input features such as serial ports, parallel ports, timers/counters, interrupt controller, data acquisition interface, Analog to Digital converter (ADC), Digital to Analog converter (DAC), everything integrated into single silicon chip.

It does not mean that any Microcontroller should have all the above said features on chip. Depending on the need and area of application for which it is designed, the on chip features present in it may or may not include all the individual section mentioned above.

Any Microcontroller requires memory to store a sequence of instruction making up a program, Parallel port or serial port for communication with an external system, timer/counter for control purpose like generating time delay and rate for the serial port apart from the controlling unit called the Central Processing Unit (CPU).

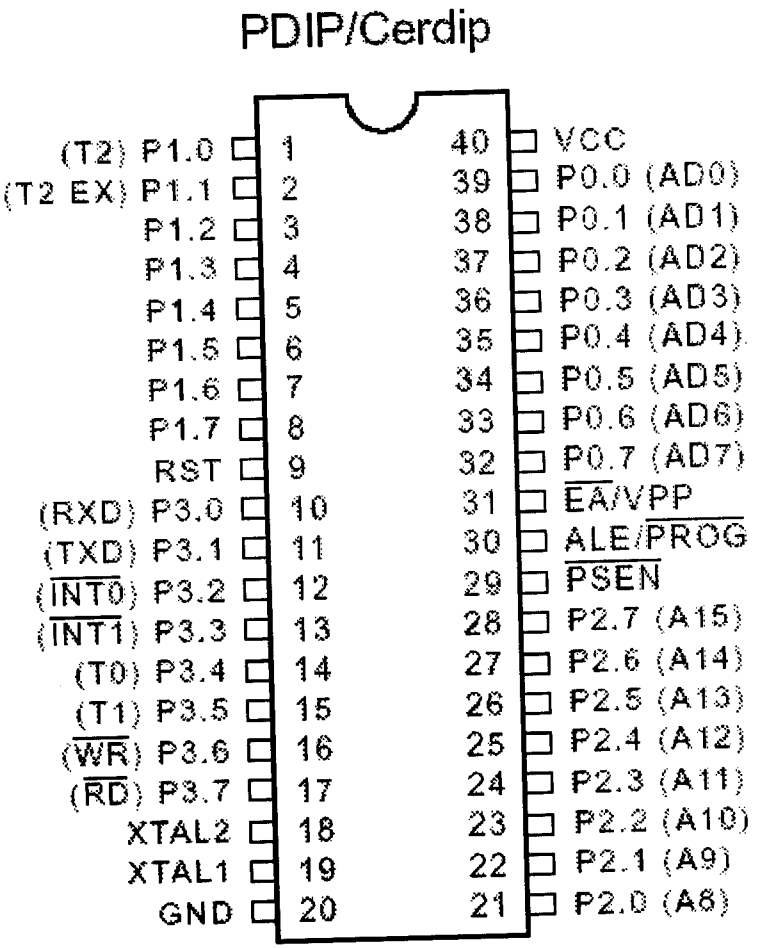
Atmel 89C52:

The AT89C52 is a low-power, high-performance CMOS 8-bit microcomputer with 8 Kbytes of Flash programmable and erasable read only memory (PEROM). The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry standard 80C51 and 80C52 instruction set and pin out. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the AtmelAT89C52 is a powerful microcomputer, which provides a highly flexible and cost effective solution to many embedded control applications.

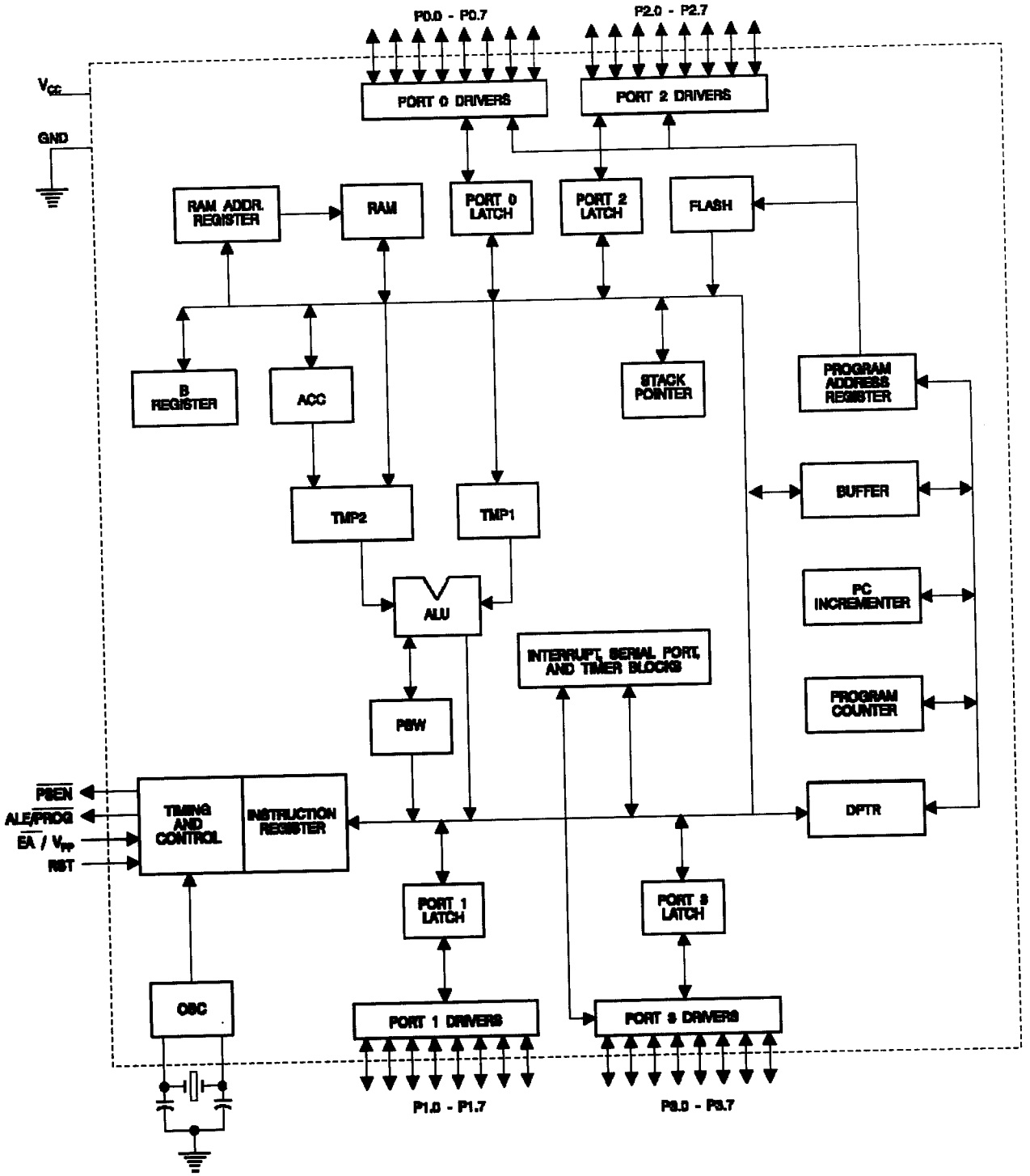
Features:

- Compatible with MCS-51TM Products
- 8 Kbytes of In-System Reprogram able Flash Memory
- Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-Level Program Memory Lock
- 256 x 8-Bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-Bit Timer/Counters
- Eight Interrupt Sources
- Programmable Serial Channel
- Low Power Idle and Power Down Modes

Pin diagram:


PDIP/Cerdip
(T2) P1.0 1
(T2 EX) P1.1 2
P1.2 3
P1.3 4
P1.4 5
P1.5 6
P1.6 7
P1.7 8
RST 9
(RXD) P3.0 10
(TXD) P3.1 11
(INT0) P3.2 12
(INT1) P3.3 13
(T0) P3.4 14
(T1) P3.5 15
(WR) P3.6 16
(RD) P3.7 17
XTAL2 18
XTAL1 19
GND 20
40 VCC
39 P0.0 (AD0)
38 P0.1 (AD1)
37 P0.2 (AD2)
36 P0.3 (AD3)
35 P0.4 (AD4)
34 P0.5 (AD5)
33 P0.6 (AD6)
32 P0.7 (AD7)
31 EA/VPP
30 ALE/PROG
29 PSEN
28 P2.7 (A15)
27 P2.6 (A14)
26 P2.5 (A13)
25 P2.4 (A12)
24 P2.3 (A11)
23 P2.2 (A10)
22 P2.1 (A9)
21 P2.0 (A8)

Architecture:



Memory organization:

The 89C52 maintains separate address space for program memory and the data memory. The program memory can be up to 64KB, of which lowest 8KB are in the on chip ROM. The data memory consists of 128 bytes of on chip RAM, plus 21 special function registers, in addition to which the device is capable of accessing up to 64KB of external data memory.

The program memory uses 16-bit address. The external data memory can use either 8-bit address, which provides a 256-location address space. The lower 128 address accesses the on chip RAM. The SFR's occupy various locations in the upper 128 bytes of the same address space.

The lowest 32 bytes in the internal RAM are divided into 4 banks of registers, each consisting of 8 bytes. Any one of these can be selected to be the "working address" of the CPU and can be by a 3-bit address is the same byte as the opcode of an instruction.

The next higher 16 bytes of the internal RAM have individually addressable bits. These are provided for use as software flags or 1-bit (Boolean) processing. This bit addressing capability is an important feature of 89C52. In addition to the 128 individually addressable bits in RAM, 11 of the SFR's also have individually addressable bits.

Pin description:

RST:

Reset input, a high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/PROG:

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory. If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

PSEN:

Program Store Enable is the read strobe to external program memory. When the AT89C52 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

EA/VPP:

External Access Enable EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on

reset. EA should be strapped to VCC for internal program executions. This pin also receives the 12-volt programming enable voltage (VPP) during Flash programming when 12-volt programming is selected.

XTAL1:

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2:

Output from the inverting oscillator amplifier.

Peripherals:

Ports:

Ports play an important role in providing communication between the microcontroller and the external world. There are 4 ports of each 8 bits thus providing 32 I/O lines.

Port 0:

Port 0 is an 8-bit open drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs. Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups. Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pull-ups are required during program verification.

Port 1:

Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the

internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL) because of the internal pull-ups. In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively, as shown in the following table.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)

It receives the low-order address bytes during Flash programming and program verification.

Port 2:

Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit ad-dresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3:

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL) because of the pull-ups.

Port 3 also serves the functions of various special features of the AT89C51, as shown in the following table.

Port pins	Alternate functions
P3.0	RXD (Serial port input)
P3.1	TXD (Serial output port)
P3.2	INT0 (External interrupt 0)
P3.3	INT1 (External interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	TI (Timer 1 external input)
P3.6	WR (External data memory write strobe)
P3.7	RD (External data memory read strobe)

Port 3 also receives some control signals for Flash programming and programming verification.

Timers:

Timer 0 and 1:

Timer 0 and Timer 1 in the AT89C52 operate the same way as Timer 0 and Timer 1 in the AT89C51.

Timer 2:

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/T2 in the SFR T2CON (shown in Table 2). Timer 2

has three operating modes: **capture, auto-reload (up or down counting), and baud rate generator**. Bits in T2CON, as shown in table, select the modes.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the Counter function, the register is incremented in response to a l-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

Operational modes:

RCLK + TCLK	CP/RL2	TR2	Mode
0	0	1	16 Bit auto reload
0	1	1	16 Bit capture
1	X	1	Baud rate generator
X	X	0	Off

Capture mode:

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 per-forms the same operation, but

a l-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt.

Auto reload mode :(Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 4). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in RCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a l-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 3. In this mode, the T2EX pin controls the direction of the count. Logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

Logic 0 at T2EX makes Timer 2 count down. The timer under-flows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers. The EXF2 bit toggles whenever Timer 2

overflows or under-flows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

Baud rate generator:

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON. Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be re-loaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes l and 3 are determined by Timer 2's overflow rate according to the following equation.

Modes 1 and 3 Baud Rates = □Timer 2 Overflow Rate /16

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation (CP/T2 = 0). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H, RCAP2L})]}$$

Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a l-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers

Interrupts:

The AT89C52 has a total of six interrupt vectors: **two external interrupts (INT0 and INT1), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt.**
Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

(MSB) (LSB)

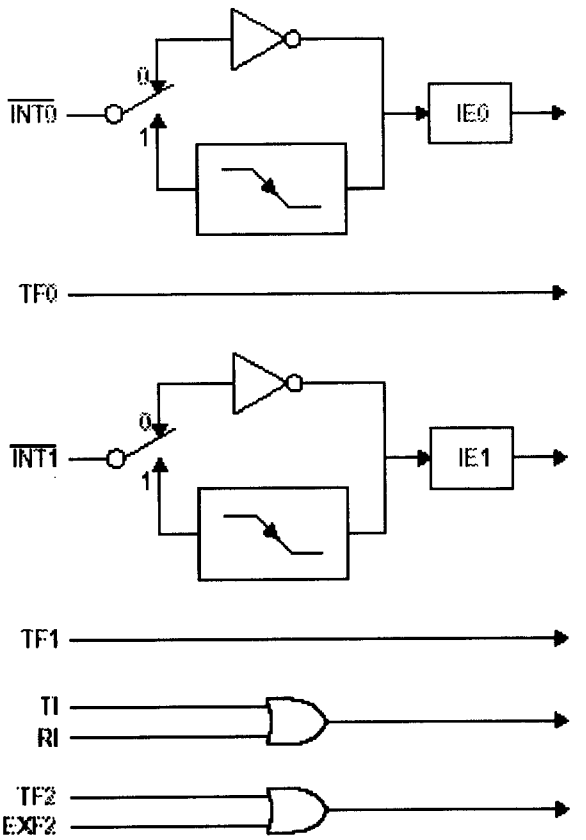
EA	.....	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.
Enable Bit = 0 disables the interrupt.

In the AT89C51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TFI, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.



Oscillator characteristics:

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 8. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle mode:

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

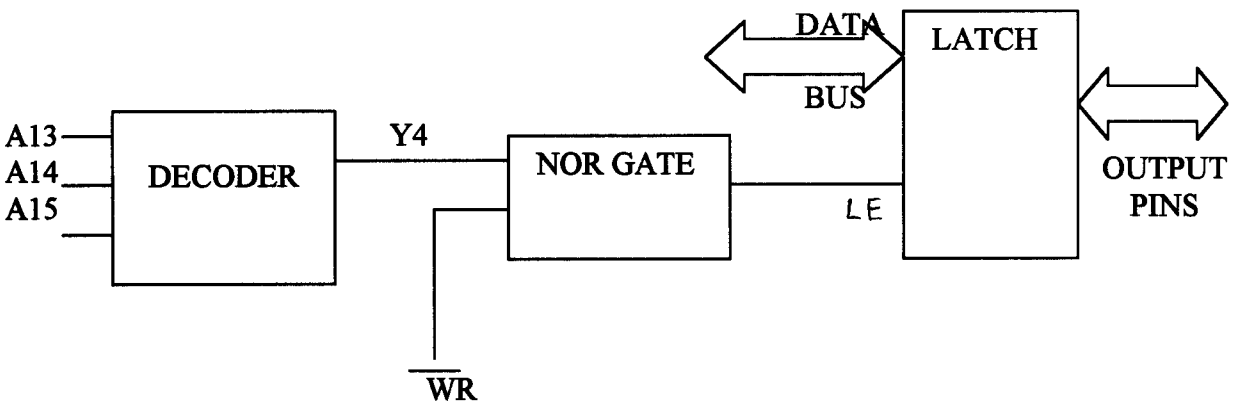
Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Power down mode:

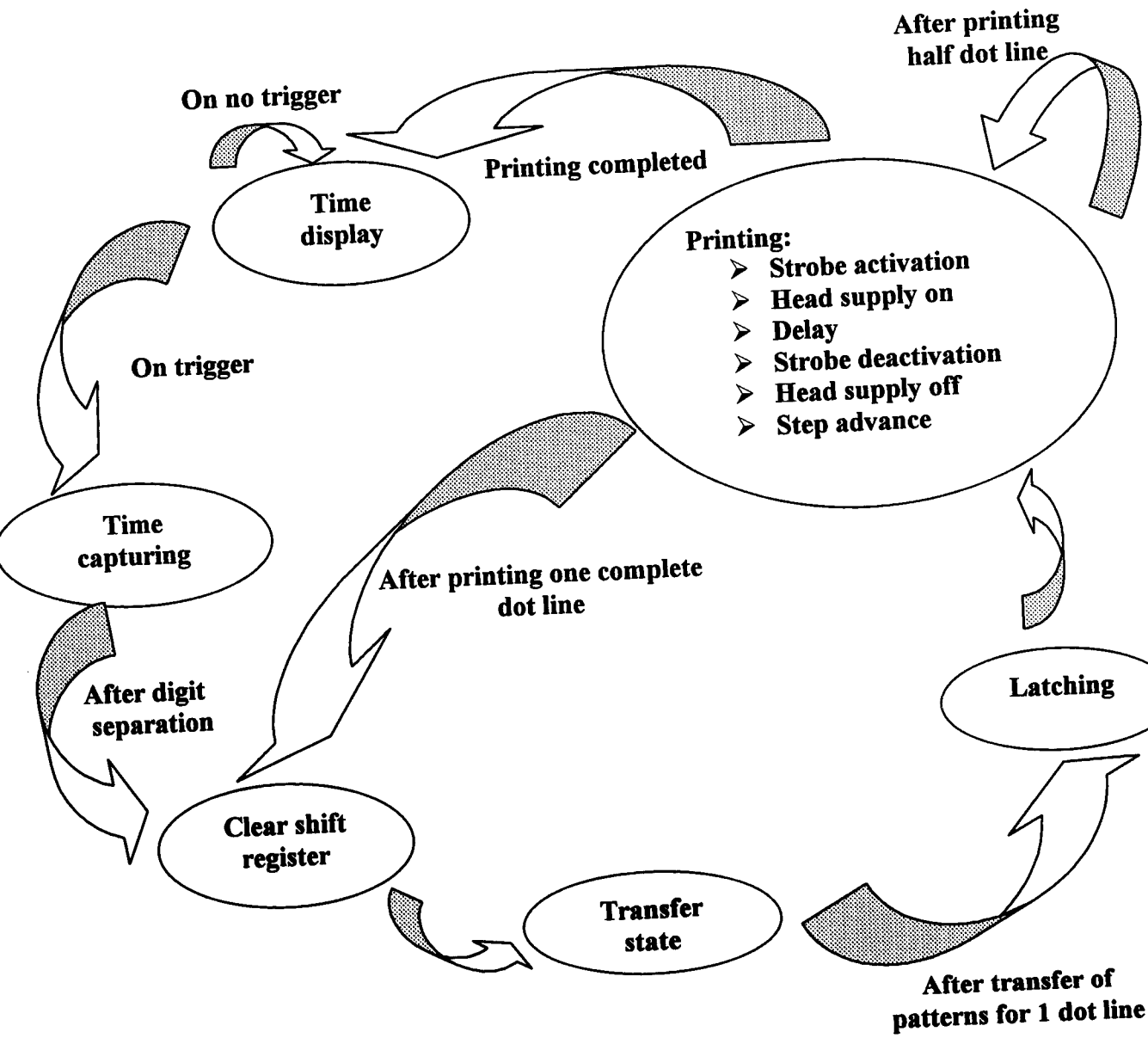
In the power down mode, the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. The only exit from power down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before VCC is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Port expansion unit:

For GPS service the port pins are widely used, hence for interfacing the printer the memory mapping technique is used by assigning the address 8000H to expand the ports. The decoder output acts as latch enable signal.



State diagram:



Generation of stepper sequence:

The latch output 4, 5, 6, 7 and 1 are connected to the inputs IN 1, IN 2, IN 3, IN 4 and enable of the driver respectively. The sequence of the stepper motor is coded as follows,

Code	In4	In3	In2	In1			ENA		OUT4	OUT3	OUT2	OUT1
	7	6	5	4	3	2	1	0				
0xa2H	1	0	1	0	0	0	1	0	ON	OFF	ON	OFF
0x62H	0	1	1	0	0	0	1	0	OFF	ON	ON	OFF
0x52H	0	1	0	1	0	0	1	0	OFF	ON	OFF	ON
0x92H	1	0	0	1	0	0	1	0	ON	OFF	OFF	ON

Proper duration is maintained between each sequence by means of delay. These 4 steps should be repeated in sequence for continuous steps.

Interrupt handling:

External interrupt:

The external interrupt INT 0 is used for printing process. This is configured in edge-triggered mode (falling edge). On interrupting printing process takes place.

Timer 1:

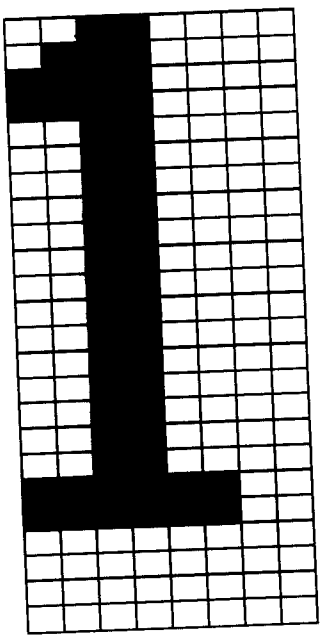
The main purpose of TIMER 1 is providing delay. This is configured in auto reload mode. The timer register is intialised to zero. The interrupt occurs for every 255-machine cycle. A variable is assigned which provides the necessary delay according to the timer. For every timer overflow the value gets decremented by one. Once it reaches zero the required delay will be obtained.

Pattern generation:

The generation of patterns is fully user defined and changing the pattern generation code, which is formed, can alter the fonts. The procedure used for pattern generation has been mentioned below:

First, the required matrix is drawn as shown below with specified rows and columns. Then the patterns are formed in the matrix by suitably shading the cells. After the pattern is formed, the binary code is generated corresponding to each row. Here the un-shaded cell represents a 0 and a shaded cell represents a 1.The binary is then transformed into the hex codes. These hex codes for all the rows of the matrix are grouped together to form a pattern code.

An example printing has been illustrated here. The letter 1 is encoded into hex data matrix by framing the letter in a 24 x 8 matrix as shown below.



00110000	30
01110000	70
11110000	F0
11110000	F0
00110000	30
00110000	30
00110000	30
00110000	30
00110000	30
00110000	30
00110000	30
00110000	30
00110000	30
00110000	30
00110000	30
00110000	30
00110000	30
00110000	30
11111111	FF
11111111	FF
00000000	00
00000000	00
00000000	00
00000000	00

Pattern retrieval and printing:

On triggering the timing details gets stored in an array. The storing process

Involves digit seperation.

For example,

Hr : min : sec

00 : 18 : 03

Logic used

Unit digit get retrieved by means of using modulo (%) 10 operation tens digit get retrieved by means of using division (/) operation and the digits are stored in a single dimension array.

Initially the shift registers are cleared. The numbers in the array corresponds to the row of the corresponding pattern in the pattern array. The first row of the first number is sent to the shift register. Similarly the first rows of all the numbers are sent. After one row gets transferred these bits are latched in latch register. Then strobe signals are activated. After this the printer head switch is made ON for 2 ms. Then the strobe signals are deactivated and the head switch is made OFF. Advance by one step is given. This completes printing half dot line. With the same data in latch register, printing is done once again to complete on dot line.

This process is repeated for remaining rows, thus printing one complete character line.

Source coding:

```
#include<reg52.h>
#include<stdio.h>

//port1
sbit sdata    = P1^0;  //yellow
sbit clock    = P1^1;  //orange
sbit strobe2  = P1^2;  //red
sbit strobe1  = P1^3;  //brown
sbit latch    = P1^4;  //black
sbit energy   = P1^5;

//global declaration
#define INITIALSTATE  1
#define TRANSFER      2
#define PRINT         3
#define WAIT          4

//function prototype
void iniatialise(void);
void stepperout(void);
void clocklow(void);
void clockhigh(void);
void papersensor_int(void);
void timer1_int(void);

//Global variable declarations
unsigned char xdata *a=0x8000;
int bitcount,countdelay;                    //countdelay=stepper pulse duration,
                                            // bitcount=total no. of bits to be transferred

char stepcount=1,control,loop,loop1,inter=1;
unsigned char steps,count1,temp,i,ii;       //count1 is data pointer in lookup
char state,row1,column,patterns[][20],temphr,temphr1,temphr2;
char zzz[10],tempsec,tempsec1,tempsec2,tempmin,tempmin1,tempmin2;

//initialisation at start up of the system
void initialise()
{
*a=0;
sdata=clock=0;
latch=strobe1=strobe2=1;
energy=1;                                   //head switch off
TMOD=0x22;                                  //timer1 in mode 2
TL0=0x06;                                   //250 ms
TH0=0x06;
```

```
TH1=0x00;
EA=ET1=ET0=1;                          //enable global,timer1 interrupt
EX0=1;                                 //external interrupt on falling edge
IT0=1;                                 //stepper input duration
countdelay=13;
steps=50;
count1=0;
test=0;
TR1=0;
}

//timer1 interrupt
void timer1_int() interrupt 3
{
        countdelay--;
}

//stepper motor output
void stepperout(void)
{
switch(stepcount)
 {
    case 1:
        *a=0xa2;//enable=1,stepper_A=1,stepper_B=1,stepper_A1=0,stepper_B1=0
         break;

    case 2:
         *a=0x62;//enable=1,stepper_A=0,stepper_B=1,stepper_A1=1,stepper_B1=0
          break;

    case 3:
         *a=0x52;//enable=1,stepper_A=0,stepper_B=0,stepper_A1=1,stepper_B1=1
          break;

    case 4:
         *a=0x92;//enable=1,stepper_A=1,stepper_B=0,stepper_A1=0,stepper_B1=1
          break;
   }
  if (stepcount++==4)
    stepcount=1;
 }

 //clock high time
 void clockhigh()
 {
       for (i=0;i<10;i++){}
 }
```

```
//clock low time
void clocklow()
{
        for (i=0;i<5;i++){}
}

//shift register initialise with zeros
void shiftreg_init()
{
        bitcount=288;
        sdata=0;//data to shift register is always 0
        while(bitcount)
        {
                clock=1;//clock high
                clockhigh();
                clock=0;//clock low
                clockhigh();
                --bitcount;
        }
  }

  //lookup patterns for numbers
  code char num[][20]={

  /*0*/{0x78,0x48,0x84,0x84,0x84,0x84,0x84,0x84,0x84,0x84,0x84,0x84,0x84,0x84,0x84,0x84
        ,0x84,0x84,0x48,0x78},
  /*1*/{0x08,0x18,0x38,0x78,0x58,0x58,0x18,0x18,0x18,0x18,0x18,0x18,0x18,0x18,0x18,0x18
        0x18,0x18,0xfc,0xfc},
  /*2*/{0x7c,0xfc,0xc4,0xc4,0xc4,0x04,0x18,0x18,0x18,0x30,0x30,0x70,0xe0,0xe0,0xe0,0xc0
        ,0xc0,0xc4,0xfc,0xfc},
  /*3*/{0x38,0x3c,0xcc,0xcc,0x0c,0x0c,0x0c,0x0c,0x18,0x78,0x78,0x18,0x0c,0x0c,0x0c,0x0c
        ,0x0c,0xcc,0xfc,0x38},
  /*4*/{0x0c,0x0c,0x0c,0x0c,0x1c,0x14,0x14,0x34,0x24,0x24,0x64,0x44,0xc4,0x84,0xfc,0xfc
        ,0x04,0x04,0x04,0x04},
  /*5*/{0xfc,0xfc,0xc0,0xc0,0xc0,0xc0,0xc0,0xc0,0xf8,0x7c,0x0c,0x0c,0x0c,0x0c,0x0c,0x0c
        ,0xcc,0xcc,0xfc,0xf8},
  /*6*/{0xfc,0xfc,0xcc,0xcc,0xc0,0xc0,0xc0,0xc0,0xfc,0xfc,0xcc,0xcc,0xcc,0xcc,0xcc,0xcc
        ,0xcc,0xcc,0xfc,0xfc},
  /*7*/{0xfc,0xfc,0x0c,0x0c,0x0c,0x18,0x18,0x18,0x30,0x30,0x30,0x30,0x60,0x60,0x60,0x60
        ,0xc0,0xc0,0xc0,0xc0},
  /*8*/{0x30,0x48,0xcc,0xcc,0xcc,0xcc,0xcc,0xcc,0x78,0x30,0x78,0xcc,0xcc,0xcc,0xcc,0xcc
        ,0xcc,0xcc,0x48,0x30},
  /*9*/{0x7c,0xcc,0xcc,0xcc,0xcc,0xcc,0xcc,0x7c,0x7c,0x0c,0x0c,0x0c,0x0c,0x0c,0x0c,0x0c
        ,0xcc,0xcc,0xfc,0xfc},
  /*:*/{0x00,0x00,0x00,0x30,0x30,0x30,0x30,0x00,0x00,0x00,0x00,0x00,0x00,0x30,0x30,0x30,
        0x30,0x00,0x00,0x00}
        };
```

```
//LCD routines
// Defins for the ACTimer
#define MILLI_SEC      400
#define TRUE            1
#define FALSE           0
#define LCD1            0
#define LCD2            1
#define MILLI_SEC      400

/*****for LCD Display ********/

#define FUNCTION_SET       0x38
#define ENTRY_MODE         0x06
#define CURSOR_MOVE        0x04
#define DISPLAY_CONTROL    0x0e
#define DD_RAM_ADDR1       0x80
#define DD_RAM_ADDR2       0xc0
#define DD_RAM_ADDR3       0x94
#define DD_RAM_ADDR4       0xd4
#define CLEAR_DISPLAY      0x01
#define LCD_HOME           0x02
#define LEADZERO           0
#define NOLEADZERO         1
typedef unsigned char UCHAR;
typedef unsigned int   UINT;
UINT delaycount=0;
UINT PBRelCount=0;
UCHAR Prev10MSec;
UCHAR  Hr=0,Min=0,Sec=0;
UINT MSec,tMSec;
UCHAR Rec_ptr;
UCHAR Disp_Ptr=0;
bit    UpdateDisplay=0;
UCHAR  xdata  *LCD_Cmd  =0x4000;
UCHAR  xdata  *LCD_Data  =0x4001;
UCHAR  xdata  *RPTR = 0x1001;

// Function Prototypes
void vDelay_Msec      (UINT k) ;
void vLCD_Init        (void);
void vLCD_PutChar     (UCHAR) ;
void vLCD_PutData     (UCHAR) ;
void putsxy           (char,char,char *) ;
void gotoxy           (char,char) ;
void convert_number   (int,char,char,char *) ;
void print_number     (char,char,char,char,int) ;
void clrscr           (void);
```

```
void ext_int() interrupt 0
{
inter=0;
zzz[0]=Hr/10;          //10's digit
zzz[1]=Hr%10;          //unit digit
zzz[2]=10;
zzz[3]=Min/10;         //10's digit
zzz[4]=Min%10;         //unit digit
zzz[5]=10;
zzz[6]=Sec/10;         //10's digit
zzz[7]=Sec%10;         //unit digit
}

void vTimer0_Int (void) interrupt 1
{
static UCHAR mscount=3;
if (mscount) mscount--;
   else{
      if (MSec < 1000) MSec++;
      else{
          MSec=0;
          Sec++;
          if (Sec > 59 )
              {
              Sec=0;
              Min++;
                  if (Min  > 59 )
                      {
                      Min=0;
                      Hr++;
                      if (Hr > 23 )Hr=0;
                      }
               }
              if (delaycount)  delaycount--;
              mscount = 3;
     }

   }

   bit aa=0;
   void main()
   {
   test=1;
   initialise();
   vLCD_Init();
   clrscr();
   TR0=1;
```

```
TR1=0;
putsxy(LCD1,0,"Unity Electro");
state=INITIALSTATE;
while(1)
{
if(inter)
  {
   print_number(LCD2,5,2,0,Hr);
   putsxy(LCD2,7,":");
   print_number(LCD2,8,2,0,Min);
   putsxy(LCD2,10,":");
   print_number(LCD2,11,2,0,Sec);
   }
 else
   {
   TR1=1;
    loop=1;
    while(loop)
      {
          switch(state)
             {

            case INITIALSTATE:

                if(!countdelay)
                {
                   if(steps==0)
                     {
                     *a=*a & 0x0d;        //stepper off
                     TL1=0x00;
                     TR1=0;               //turn OFF timer1
                     state=TRANSFER;
                     break;
                     }
                  stepperout();
                  if(--steps==0)  countdelay=52;
                  else countdelay=13;
                   }
                  break;

             case TRANSFER:

                 shiftreg_init();
                 for(ii=0;ii<8;ii++)
                    {
                    bitcount=10;
                     row1=zzz[ii];
```

```
temp=num[row1][column];
while(bitcount)
 {
 temp=temp<<1;
 if (CY==1) sdata=1;     //data bit=1
 else sdata=0;           //data bit=0
 clocklow();
 clock=1;                //clock high
 clockhigh();
 clock=0;                //clock low
 clocklow();
 --bitcount;
 }
 }
 bitcount=150;
 sdata=0;                //data to shift register is always 0
 while(bitcount)
 {
 clock=1;                //clock high
 clockhigh();
 clock=0;                //clock low
 clockhigh();
 --bitcount;
 }
 latch=0;                //latch enable
 for(i=0;i<5;i++){}
 latch=1;                //latch disable
 column++;
 state=PRINT;
 break;

case PRINT:

 for(loop1=0;loop1<2;loop1++)
 {
 TL1=0;
 strobe1=strobe2=0;      //strobe activation
 for(i=0;i<2;i++){}      //5 microsecond delay
 energy=0;               //head switch on
 countdelay=6;
 TR1=1;                  //timer1 on
 while(countdelay){}
 TR1=0;                  //timer1 off
 strobe1=strobe2=1;      //strobe deactivation
 for(i=0;i<2;i++){}      //5 microsecond delay
 energy=1;               //head switch off
 countdelay=4;
```

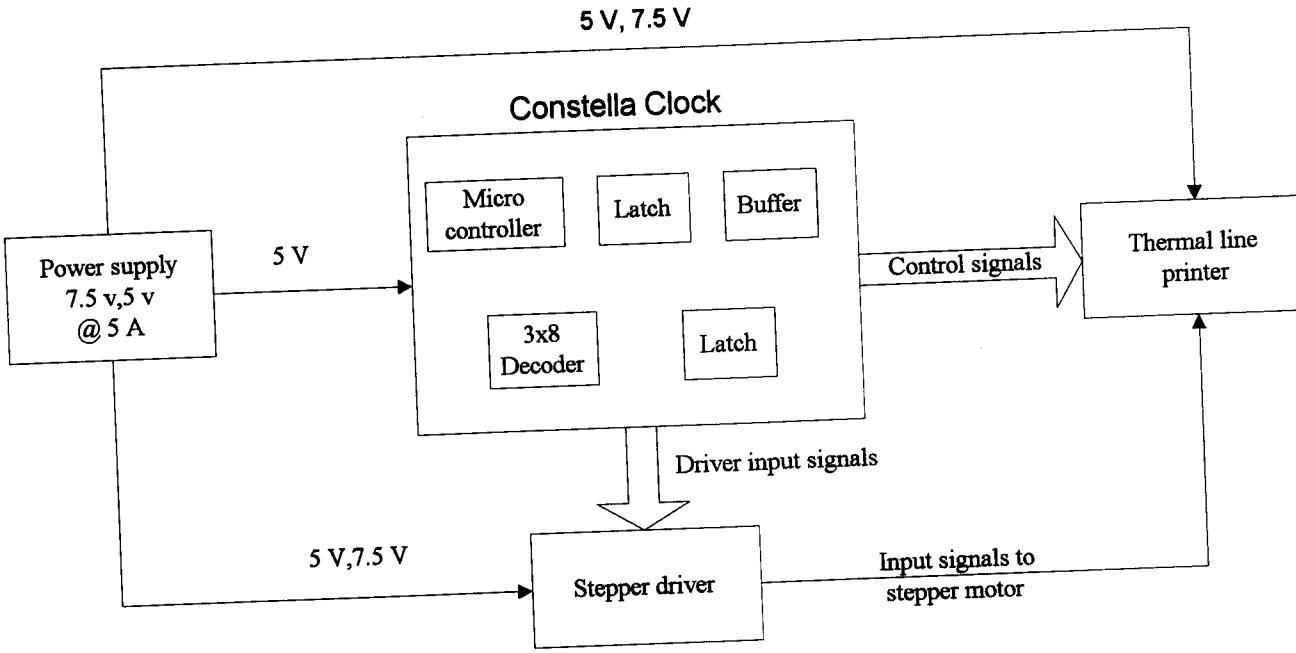
```
TR1=1;
 while(countdelay){}
TR1=0;
strobe1=strobe2=0;          //strobe activation
for(i=0;i<2;i++){}          //5 microsecond delay
energy=0;                   //head switch on
 countdelay=6;
TR1=1;                       //timer1 on
while(countdelay){}
TR1=0;                       //timer1 off
strobe1=strobe2=1;          //strobe deactivation
for(i=0;i<2;i++){}          //5 microsecond delay
energy=1;                    //head switch off
TL1=0;
countdelay=3;
stepperout();
TR1=1;                       //timer1 on
while(countdelay){}
TR1=0;                       //timer1 off
TL1=0;
countdelay=4;
TR1=1;                       //timer1 on
while(countdelay){}
TR1=0;                       //timer1 off
 }
*a=0;
if(column<20)
  state=TRANSFER;
else
  {
  inter=1;
  loop=0;
  for(i=0;i<10;i++)
       {
       stepperout();
       TL1=0;
       countdelay=25;
       TR1=1;
       while(countdelay){}
       TR1=0;
       }
   *a=0;
   column=0;
   }
  break;
 }
}}}}
```

```
void vDelay_Msec(UINT k)
{
     UINT i,j;
     for ( j = 0; j < k; j++)
     for (i = 0; i <= MILLI_SEC;)      // 1 millisecond
          {
          i++;
          }
 }

 void vLCD_Init (void)
 {
     vDelay_Msec(100);
     vLCD_PutChar(FUNCTION_SET);
     vDelay_Msec(100);
     vLCD_PutChar(FUNCTION_SET);
     vDelay_Msec(100);
      vLCD_PutChar(FUNCTION_SET);
      vDelay_Msec(100);
      vLCD_PutChar(ENTRY_MODE);
      vDelay_Msec(50);
      vLCD_PutChar(DISPLAY_CONTROL);
      vDelay_Msec(50);
      vLCD_PutChar(CLEAR_DISPLAY);
      vDelay_Msec(50);
      vLCD_PutChar(DD_RAM_ADDR1);
      vDelay_Msec(50);
   }

   void vLCD_PutChar(UCHAR display)
   {
       *LCD_Cmd=display;
   }

   void vLCD_PutData(UCHAR display)
   {
       *LCD_Data=display;
   }

   void gotoxy(char row,char col)      // modified by vs
   {
        UCHAR val;
        if (row==0) val=col;
        else if (row==1) val=0x40+col;
        else if (row==2) val=0x14+col;
        else if (row==3) val=0x54+col;
        val=val|0x80;
```

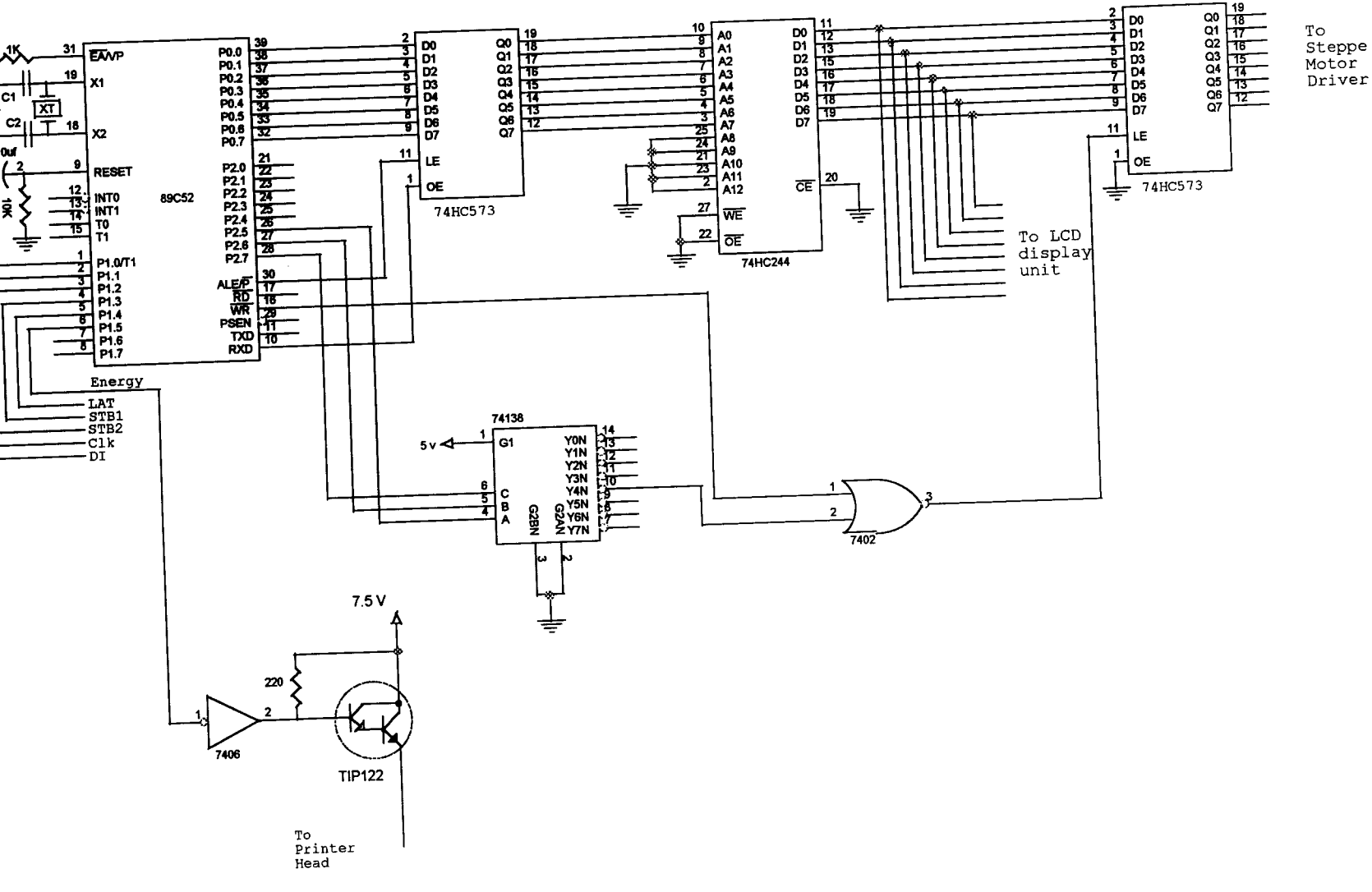
```
    vLCD_PutChar(val);
    vDelay_Msec(5);         //must
}

void convert_number(int a, char n, char lzflag, char *buffer)
{
      char j;
      j=n-1;
      if(a==0)
        {
        buffer[j--]='0';
        }
      else
        {
        while((a>0) || (j>=0))
            {
            buffer[j--]=0x30+a%10;
            a=a/10;
            }
        }
     while(j>=0)
     {
        if(lzflag)
        {
        buffer[j--]=32;
        }
        else
        {
        buffer[j--]='0';
        }
      }
     buffer[n]=0;
     }

   void print_number(char r, char c, char n, char lz, int a)
   {
      char buff[5];
      convert_number(a,n,lz,buff);
      putsxy(r,c,buff);
   }

   void clrscr()
   {
      vLCD_PutChar(0x01);
      vDelay_Msec(1);
   }
```

```
void putsxy(char r, char c, char *s)
{
      gotoxy(r,c);
      while(*s)
      {
       vDelay_Msec(1);// must
       vLCD_PutData(*s);
       s++;
      }
vDelay_Msec(1); //must
}
```

Block diagram:



Circuit Diagram



CONCLUSION

This project titled "**Thermal Printer Interface For GPS Based Clock System**" has helped us in consolidating the knowledge gained in micro controllers and basic electronics. We have become familiar with the, the working and specifications of the Epson MT51 thermal line printer, the AT89C52 microcontroller and the various other ICs employed in the design. The experience gained by working in a professional environment has further enriched our passion in exploring the new trends in the field of electronics and communication. We once again thank our faculties and the staff of Unity Electro Systems who have been supportive during the entire course of our project.

FUTURE DEVELOPMENTS

Our role in the project is to interface the Thermal Printer with a GPS based clock system and to print the timing details. This can be extended further to print the details such as **car number, code number, etc**. Sensors such as **paper end sensor, head unload sensor, temperature sensor** can be used in future as preventing measures. At present manual triggering is used in the rally. Our plan is to avoid manual triggering and to adopt **automatic triggering.**

BIBLIOGRAPHY

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- **Introduction to 8051 Microcontroller – Kenneth Ayala**
- **Programming and customizing the 8051 Microcontroller - Myke Predko**
- **Let Us C – Yashavant Kanetkar**
- **Epson.com**
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- **Design-Net.com**
- **Ni.com**

Features

- Compatible with MCS-51™ Products
- 8 Kbytes of In-System Reprogrammable Flash Memory
  - Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-Level Program Memory Lock
- 256 x 8-Bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-Bit Timer/Counters
- Eight Interrupt Sources
- Programmable Serial Channel
- Low Power Idle and Power Down Modes

8-Bit Microcontroller with 8 Kbytes Flash

Description

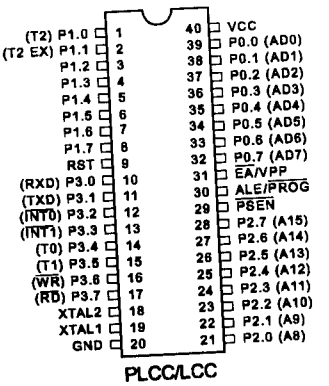
The AT89C52 is a low-power, high-performance CMOS 8-bit microcomputer with 8 Kbytes of Flash programmable and erasable read only memory (PEROM). The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard 80C51 and 80C52 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C52 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

The AT89C52 provides the following standard features: 8 Kbytes of Flash, 256 bytes of RAM, 32 I/O lines, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89C52 is

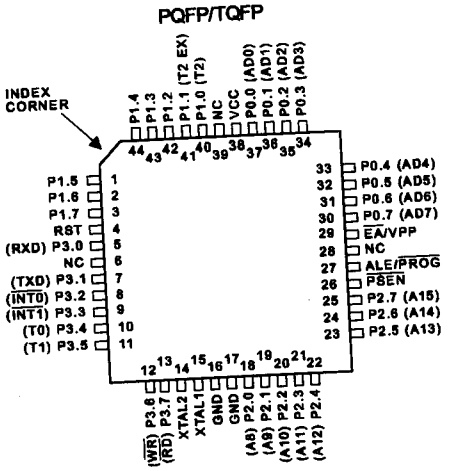
(continued)

Pin Configurations

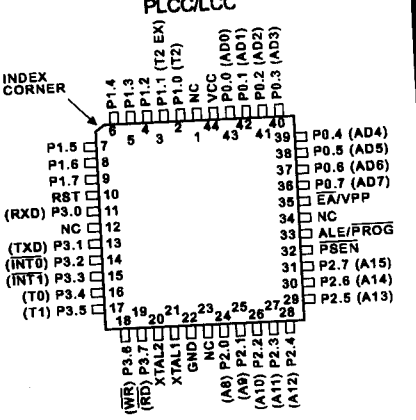
PDIP/Cerdip



PQFP/TQFP

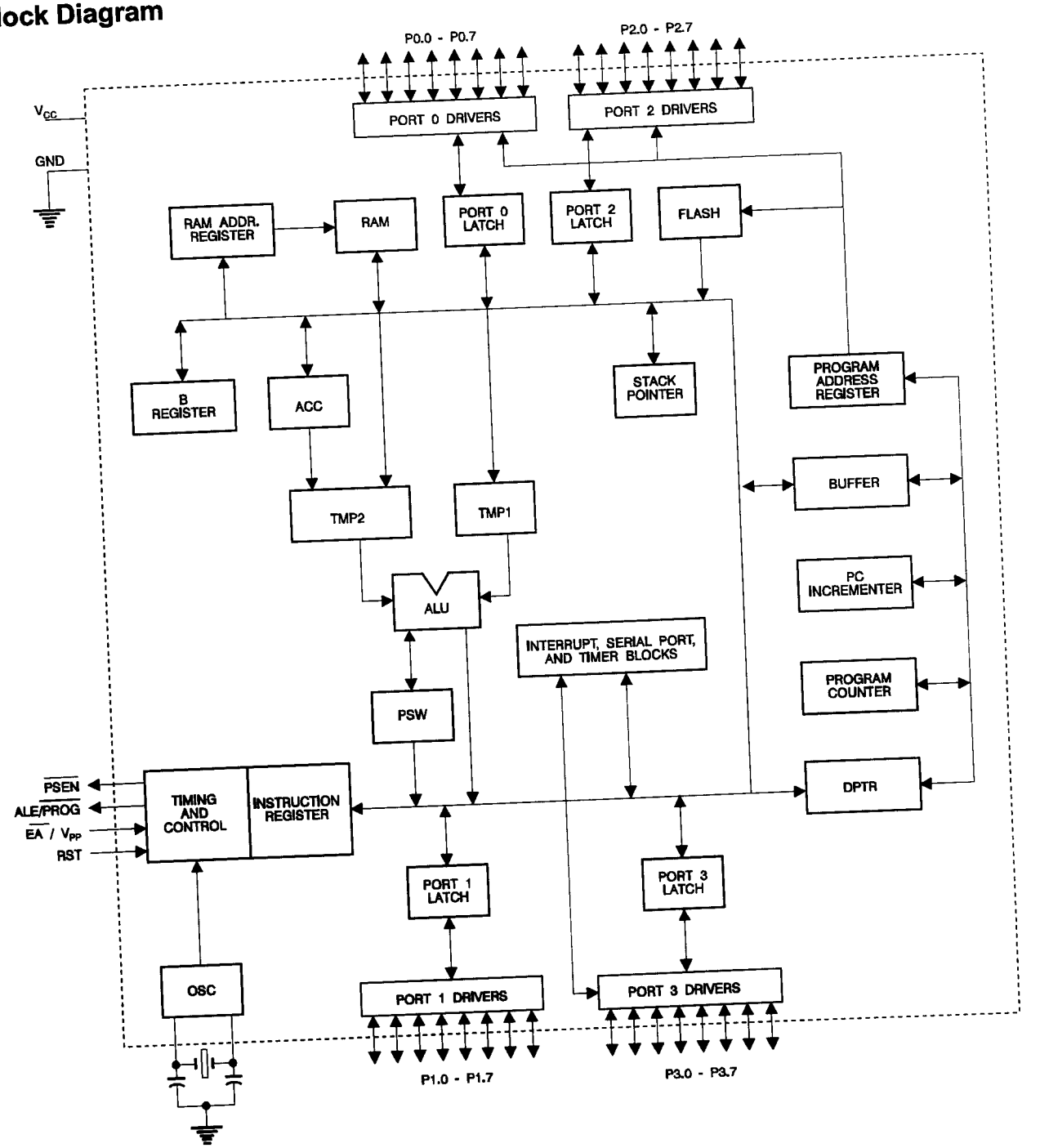


PLCC/LCC



0313E

Block Diagram



Description (Continued)

designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next hardware reset.

Pin Description

VCC

Supply voltage.

GND

Ground.

Port 0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively, as shown in the following table.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)

Port 1 also receives the low-order address bytes during Flash programming and program verification.

Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and programming verification.

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcrontroller is in external execution mode.

$\overline{PSEN}$

Program Store Enable is the read strobe to external program memory.

When the AT89C52 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

(continued)

Pin Description (Continued)

$\overline{EA}$/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to VCC for internal program executions.

This pin also receives the 12-volt programming enable voltage (VPP) during Flash programming when 12-volt programming is selected.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 4) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode. *(continued)*

Table 1. AT89C52 SFR Map and Reset Values

0F8H								0FFH
0F0H	B 00000000							0F7H
0E8H								0EFH
0E0H	ACC 00000000							0E7H
0D8H								0DFH
0D0H	PSW 00000000							0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000		0CFH
0C0H								0C7H
0B8H	IP XX000000							0BFH
0B0H	P3 11111111							0B7H
0A8H	IE 0X000000							0AFH
0A0H	P2 11111111							0A7H
98H	SCON 00000000	SBUF XXXXXXXX						9FH
90H	P1 11111111							97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000		8FH
80H	P0 11111111	SP 00000111	DPL 00000000	DPH 00000000			PCON 0XXX0000	87H

Table 2. T2CON—Timer/Counter 2 Control Register

T2CON Address = 0C8H — Reset Value = 0000 0000B

Bit Addressable

Bit	7	6	5	4	3	2	1	0
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
C/$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
CP/$\overline{RL2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/RL2 = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Special Function Registers (Continued)

Interrupt Registers The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the six interrupt sources in the IP register.

Data Memory

The AT89C52 implements 256 bytes of on-chip RAM. The upper 128 bytes occupy a parallel address space to the Special Function Registers. That means the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions that use direct addressing access SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

MOV 0A0H, #data

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

MOV @R0, #data

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

Timer 0 and 1

Timer 0 and Timer 1 in the AT89C52 operate the same way as Timer 0 and Timer 1 in the AT89C51.

Timer 2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 3.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

Table 3. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-Bit Auto-Reload
0	1	1	16-Bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

Auto-Reload (Up or Down Counter)

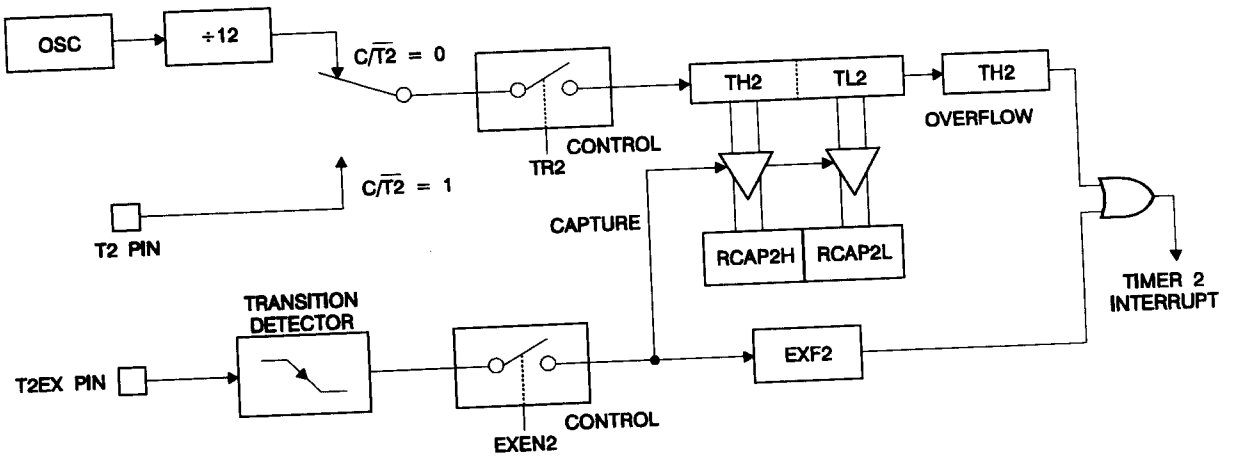
Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 4). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

Figure 2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in RCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 3. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

(continued)

Figure 1. Timer 2 in Capture Mode



Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0 V to +7.0 V
Maximum Operating Voltage	6.6 V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 5.0 V ± 20%, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
V_{OL}	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low Voltage[1] (Port 0, ALE, PSEN)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, PSEN)	I_{OH} = -60 µA, V_{CC} = 5 V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5 V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45 V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2 V		-650	µA
I_{LI}	Input Leakage Current (Port 0, EA)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power Down Mode[2]	V_{CC} = 6 V		100	µA
		V_{CC} = 3 V		40	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin:10 mA
Maximum I_{OL} per 8-bit port:
Port 0:26 mA
Ports 1,2, 3:15 mA
Maximum total IOL for all output pins:71 mA
If IOL exceeds the test condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power Down is 2 V.

A.C. Characteristics

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
1/t_{CLCL}	Oscillator Frequency			0	24	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	28		t_{CLCL}-13		ns
t_{LLAX}	Address Hold After ALE Low	48		t_{CLCL}-20		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-13		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-20		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-45	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-10	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CLCL}$-55	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-20		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-120		ns
t_{WHQX}	Data Hold After $\overline{WR}$	33		t_{CLCL}-20		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-20	t_{CLCL}+25	ns

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT573
Octal D-type transparent latch; 3-state

December 1990

Product specification
File under Integrated Circuits, IC06

PHILIPS

Octal D-type transparent latch; 3-state

74HC/HCT573

FEATURES

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors/microcomputers
- 3-state non-inverting outputs for bus oriented applications
- Common 3-state output enable input
- Functionally identical to the "563" and "373"
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT573 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT573 are octal D-type transparent latches featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications.
A latch enable ($\overline{LE}$) input and an output enable ($\overline{OE}$) input are common to all latches.

The "573" consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the D_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE.
When $\overline{OE}$ is LOW, the contents of the 8 latches are available at the outputs.
When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state.
Operation of the $\overline{OE}$ input does not affect the state of the latches.

The "573" is functionally identical to the "563" and "373", but the "563" has inverted outputs and the "373" has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	D_n to Q_n		14	17	ns
	LE to Q_n		15	15	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	26	26	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF; V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}; for HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5, 6, 7, 8, 9	D_0 to D_7	data inputs
11	LE	latch enable input (active HIGH)
1	$\overline{OE}$	3-state output enable input (active LOW)
10	GND	ground (0 V)
19, 18, 17, 16, 15, 14, 13, 12	Q_0 to Q_7	3-state latch outputs
20	V_{CC}	positive supply voltage

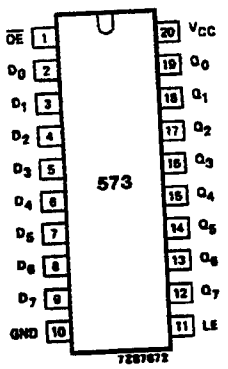


Fig.1 Pin configuration.

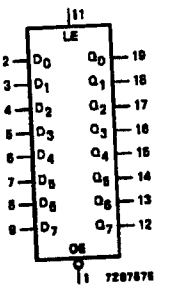


Fig.2 Logic symbol.

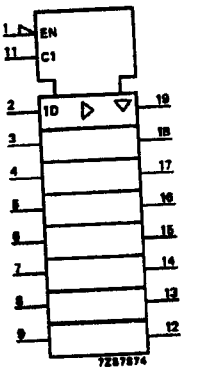


Fig.3 IEC logic symbol.

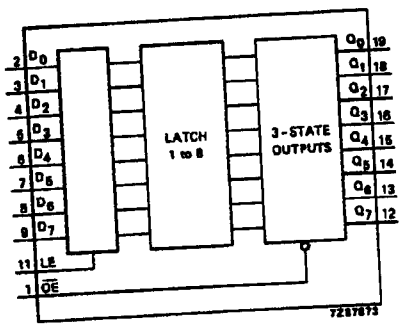


Fig.4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	D_N		Q_0 to Q_7
enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
latch and read register	L	L	l	L	L
	L	L	h	H	H
latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

Notes

1. H = HIGH voltage level
   h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
   L = LOW voltage level
   l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
   Z = high impedance OFF-state

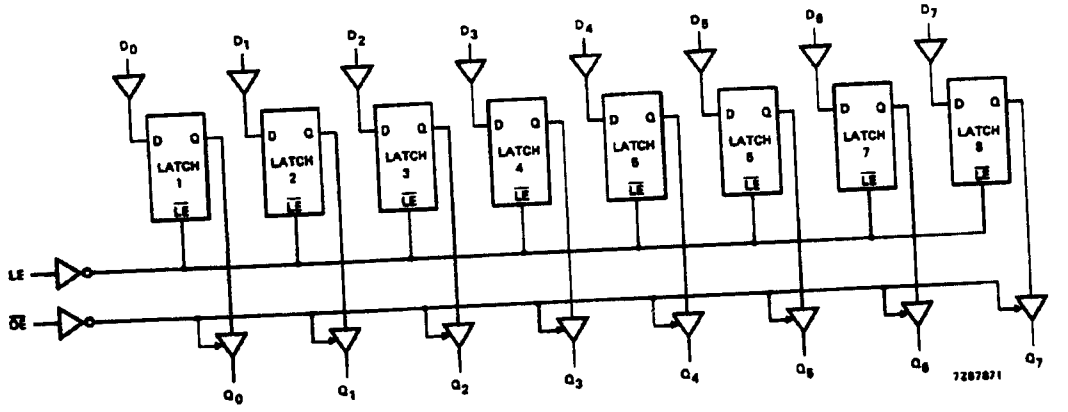


Fig.5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay D_n to Q_n		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay LE to Q_n		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.7
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n		44 16 13	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig.8
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n		55 20 16	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.8
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.6
t_W	enable pulse width HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t_{su}	set-up time D_n to LE	50 10 9	11 4 3		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.9
t_h	hold time D_n to LE	5 5 5	3 1 1		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig.9

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

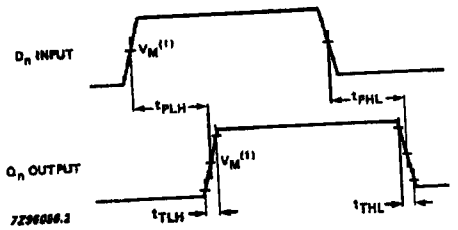
INPUT	UNIT LOAD COEFFICIENT
D_n	0.35
LE	0.65
$\overline{OE}$	1.25

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

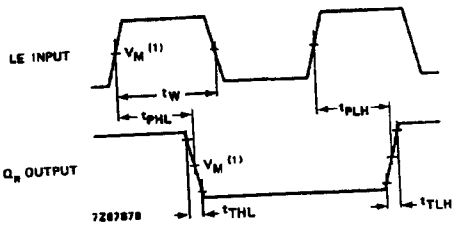
SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay D_n to Q_n		20	35		44		53	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay LE to Q_n		18	35		44		53	ns	4.5	Fig.7
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n		17	30		38		45	ns	4.5	Fig.8
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n		18	30		38		45	ns	4.5	Fig.8
t_{THL}/ t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig.6
t_W	enable pulse width HIGH	16	5		20		24		ns	4.5	Fig.7
t_{su}	set-up time D_n to LE	13	7		16		20		ns	4.5	Fig.9
t_h	hold time D_n to LE	9	4		11		14		ns	4.5	Fig.9

AC WAVEFORMS



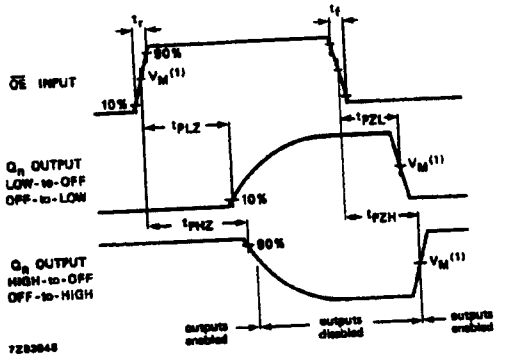
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.6 Waveforms showing the data input (D_n) to output (Q_n) propagation delays and the output transition times.



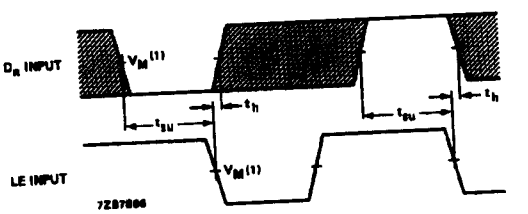
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays and the output transition times.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.8 Waveforms showing the 3-state enable and disable times.



The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.9 Waveforms showing the data set-up and hold times for D_n input to LE input.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

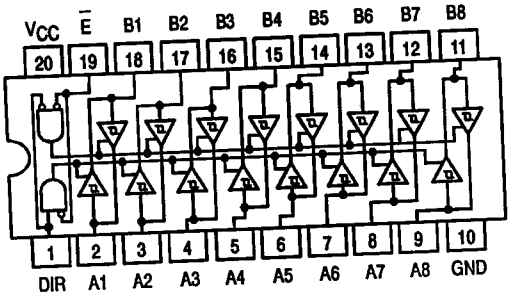
SN74LS245

Octal Bus Transceiver

The SN74LS245 is an Octal Bus Transmitter/Receiver designed for 8-line asynchronous 2-way data communication between data buses. Direction Input (DR) controls transmission of Data from bus A to bus B or bus B to bus A depending upon its logic level. The Enable input ($\overline{E}$) can be used to isolate the buses.

- Hysteresis Inputs to Improve Noise Immunity
- 2-Way Asynchronous Data Bus Communication
- Input Diodes Limit High-Speed Termination Effects
- ESD > 3500 Volts

LOGIC AND CONNECTION DIAGRAMS DIP (TOP VIEW)



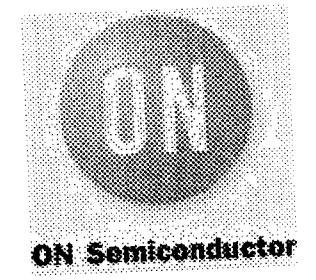
TRUTH TABLE

INPUTS		OUTPUT
$\overline{E}$	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

GUARANTEED OPERATING RANGES

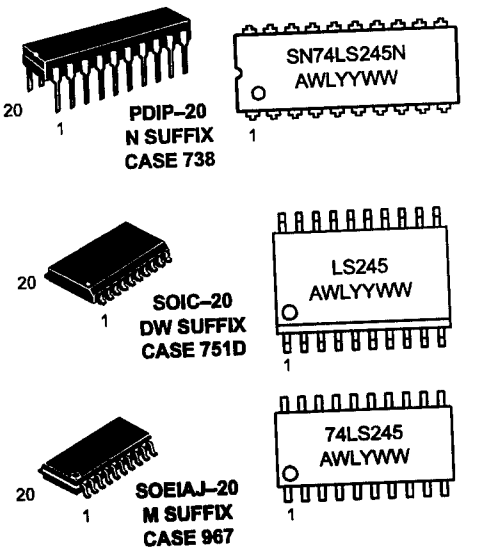
Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			–3.0	mA
				–15	mA
I_{OL}	Output Current – Low			24	mA



http://onseml.com

LOW POWER SCHOTTKY

MARKING DIAGRAMS



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
SN74LS245N	PDIP–20	1440 Units/Box
SN74LS245DW	SOIC–WIDE	38 Units/Rail
SN74LS245DWR2	SOIC–WIDE	2500/Tape & Reel
SN74LS245M	SOEIAJ–20	See Note 1.
SN74LS245MEL	SOEIAJ–20	See Note 1.

1. For ordering information on the EIAJ version of the SOIC package, please contact your local ON Semiconductor representative.

Publication Order Number:

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage for All Inputs	
$V_{T+}-V_{T-}$	Hysteresis		0.2	0.4		V	V_{CC} = MIN	
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage		2.4	3.4		V	V_{CC} = MIN, I_{OH} = −3.0 mA	
			2.0			V	V_{CC} = MIN, I_{OH} = MAX	
V_{OL}	Output LOW Voltage			0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
				0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V	
I_{OZL}	Output Off Current LOW				−200	μA	V_{CC} = MAX, V_{OUT} = 0.4 V	
I_{IH}	Input HIGH Current	A or B, DR or E			20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
		$\overline{DR}$ or E			0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
		$\overline{A}$ or B			0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V	
I_{IL}	Input LOW Current				−0.2	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 2.)		−40		−225	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH				70	mA	V_{CC} = MAX	
	Total, Output LOW				90			
	Total at HIGH Z				95			

2. Not more than one output should be shorted at a time, nor for more than 1 second.

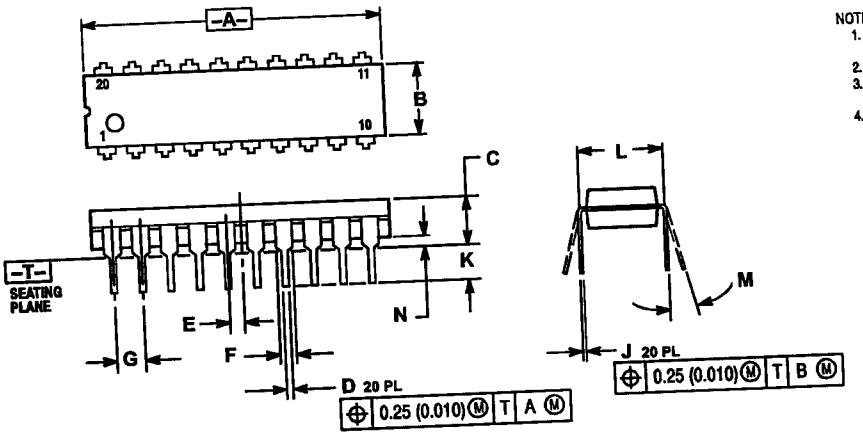
AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, $T_{RISE}/T_{FALL} \leq$ 6.0 ns)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		8.0 8.0	12 12	ns	C_L = 45 pF, R_L = 667 Ω
t_{PZH}	Output Enable Time to HIGH Level		25	40	ns	
t_{PZL}	Output Enable Time to LOW Level		27	40	ns	
t_{PLZ}	Output Disable Time from LOW Level		15	25	ns	C_L = 5.0 pF, R_L = 667 Ω
t_{PHZ}	Output Disable Time from HIGH Level		15	25	ns	

SN74LS245

PACKAGE DIMENSIONS

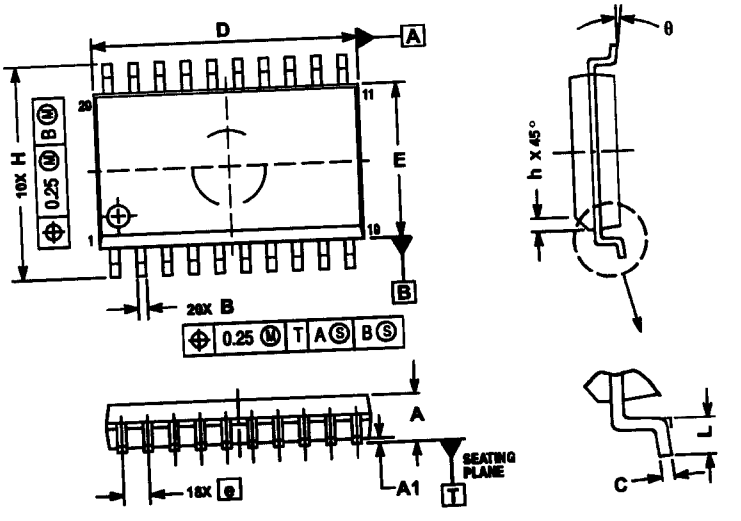
N SUFFIX
PLASTIC PACKAGE
CASE 738–03
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D–05
ISSUE F



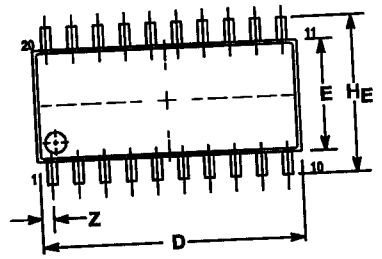
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

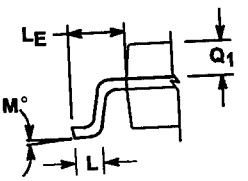
DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

SN74LS245

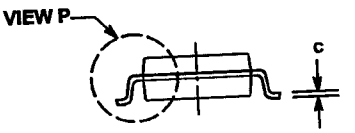
PACKAGE DIMENSIONS

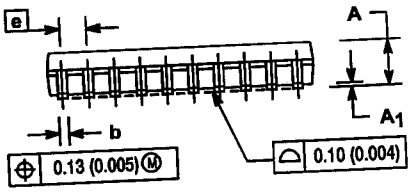
M SUFFIX
SOEIAJ PACKAGE
CASE 967–01
ISSUE O





DETAIL P





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q_1	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

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TEXAS INSTRUMENTS
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CHS147C

CD54/74HC138, CD54/74HCT138, CD54/74HC238, CD54/74HCT238

High Speed CMOS Logic 3-to-8 Line Decoder/ Demultiplexer Inverting and Non-Inverting

October 1997 - Revised August 2001

Features

- Select One Of Eight Data Outputs Active Low for 138, Active High for 238
- I/O Port or Memory Selector
- Three Enable Inputs to Simplify Cascading
- Typical Propagation Delay of 13ns at V_{CC} = 5V, C_L = 15pF, T_A = 25°C
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility, V_{IL} = 0.8V (Max), V_{IH} = 2V (Min)
  - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}

Description

The 'HC138, 'HC238, 'HCT138, and 'HCT238 are high speed silicon gate CMOS decoders well suited to memory address decoding or data routing applications. Both circuits feature low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL logic. Both circuits have three binary select inputs (A0, A1 and A2). If the device is enabled, these inputs determine which one of the eight normally high outputs of the HC/HCT138 series will go low or which of the normally low outputs of the HC/HCT238 series will go high.

Two active low and one active high enables ($\overline{E1}$, $\overline{E2}$, and E3) are provided to ease the cascading of decoders. The decoder's 8 outputs can drive 10 low power Schottky TTL equivalent loads.

Ordering Information

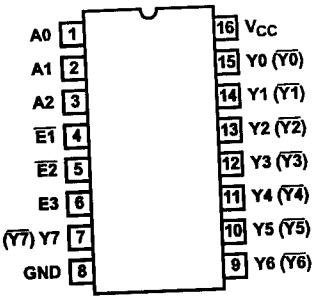
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC138F	-55 to 125	16 Ld CERDIP
CD54HC138F3A	-55 to 125	16 Ld CERDIP
CD74HC138E	-55 to 125	16 Ld PDIP
CD74HC138M	-55 to 125	16 Ld SOIC
CD74HC138SM	-55 to 125	16 Ld SSOP
CD54HCT138F	-55 to 125	16 Ld CERDIP
CD54HCT138F3A	-55 to 125	16 Ld CERDIP
CD74HCT138E	-55 to 125	16 Ld PDIP
CD74HCT138M	-55 to 125	16 Ld SOIC
CD54HC238F3A	-55 to 125	16 Ld CERDIP
CD74HC238E	-55 to 125	16 Ld PDIP
CD74HC238M	-55 to 125	16 Ld SOIC
CD54HCT238F3A	-55 to 125	16 Ld CERDIP
CD74HCT238E	-55 to 125	16 Ld PDIP
CD74HCT238M	-55 to 125	16 Ld SOIC

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

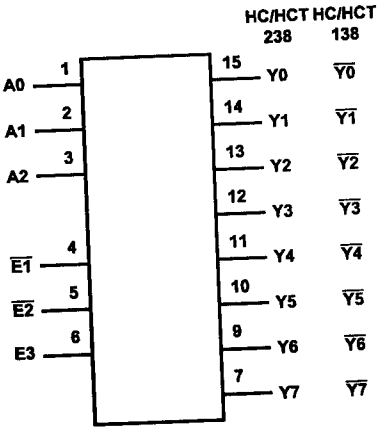
Pinout

CD54HC138, CD54HCT138, CD54HC238, CD54HCT238
(CERDIP)
CD74HC138, CD74HCT138, CD74HC238, CD74HCT238
(PDIP, SOIC)
TOP VIEW



Signal names in parentheses are for 'HC138 and 'HCT138.

Functional Diagram



TRUTH TABLE 'HC138, 'HCT138

INPUTS						OUTPUTS							
ENABLE			ADDRESS										
E3	$\overline{E2}$	$\overline{E1}$	A2	A1	$\overline{A0}$	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care

TRUTH TABLE 'HC238, 'HCT238

INPUTS						OUTPUTS							
ENABLE			ADDRESS										
E3	$\overline{E2}$	$\overline{E1}$	A2	A1	$\overline{A0}$	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	L	H	H	L	L	L	H	L	L	L	L
H	L	L	H	L	L	L	L	L	L	H	L	L	L
H	L	L	H	L	H	L	L	L	L	L	H	L	L
H	L	L	H	H	L	L	L	L	L	L	L	H	L
H	L	L	H	H	H	L	L	L	L	L	L	L	H

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} ..... -0.5V to 7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V ..... ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V ..... ±20mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V ..... ±25mA
DC V_{CC} or Ground Current, I_{CC} or I_{GND} ..... ±50mA

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
PDIP Package	90
SOIC Package	115
SSOP Package	155

Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range (T_A) ..... -55°C to 125°C
Supply Voltage Range, V_{CC}
HC Types ..... 2V to 6V
HCT Types ..... 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O ..... 0V to V_{CC}
Input Rise and Fall Time
2V ..... 1000ns (Max)
4.5V ..... 500ns (Max)
6V ..... 400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} and GND	0	5.5	-		±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 4)	ΔI_{CC}	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE:

4. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
A0-A2	1.5
$\overline{E1}$, $\overline{E2}$	1.25
$\overline{E3}$	1

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360µA max at 25°C.

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HC TYPES											
Propagation Delay Address to Output	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	150	-	190	-	225	ns
			4.5	-	-	30	-	38	-	45	ns
		C_L = 15pF	5	-	13	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	26	-	33	-	38	ns

Switching Specifications Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Enable to Output HC/HCT138	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	150	-	190	-	265	ns
			4.5	-	-	30	-	38	-	53	ns
			6	-	-	26	-	33	-	45	ns
Output Transition Time (Figure 1)	t_{TLH}, t_{THL}	C_L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Power Dissipation Capacitance, (Notes 5, 6)	C_{PD}	C_L = 15pF	5	-	67	-	-	-	-	-	pF
Input Capacitance	C_{IN}	-	-	-	-	10	-	10	-	10	pF
HCT TYPES											
Propagation Delay Address to Output	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	35	-	44	-	53	ns
		C_L = 15pF	5	-	14	-	-	-	-	-	ns
Enable to Output HC/HCT138	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	35	-	44	-	53	ns
Enable to Output HC/HCT238	t_{PLH}, t_{PHL}	C_L = 15pF	4.5	-	-	40	-	50	-	60	ns
Output Transition Time (Figure 2)	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	-	15	-	19	-	22	ns
Power Dissipation Capacitance, (Notes 5, 6)	C_{PD}	C_L = 15pF	5	-	67	-	-	-	-	-	pF
Input Capacitance	C_{IN}	-	-	-	-	10	-	10	-	10	pF

NOTES:

5. C_{PD} is used to determine the dynamic power consumption, per gate.
6. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where: f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms

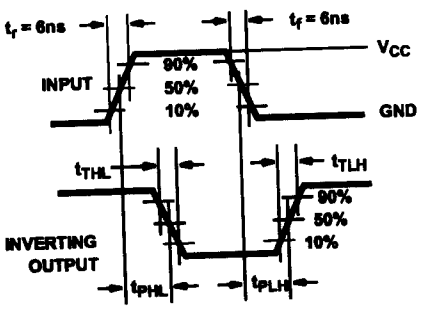


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

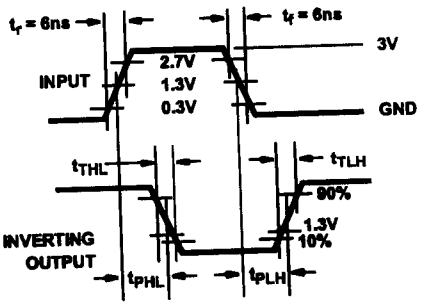
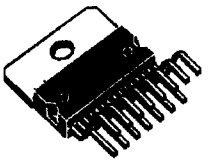


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

L298

DUAL FULL-BRIDGE DRIVER

- OPERATING SUPPLY VOLTAGE UP TO 46 V
- TOTAL DC CURRENT UP TO 4 A
- LOW SATURATION VOLTAGE
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5 V (HIGH NOISE IMMUNITY)



Multiwatt15

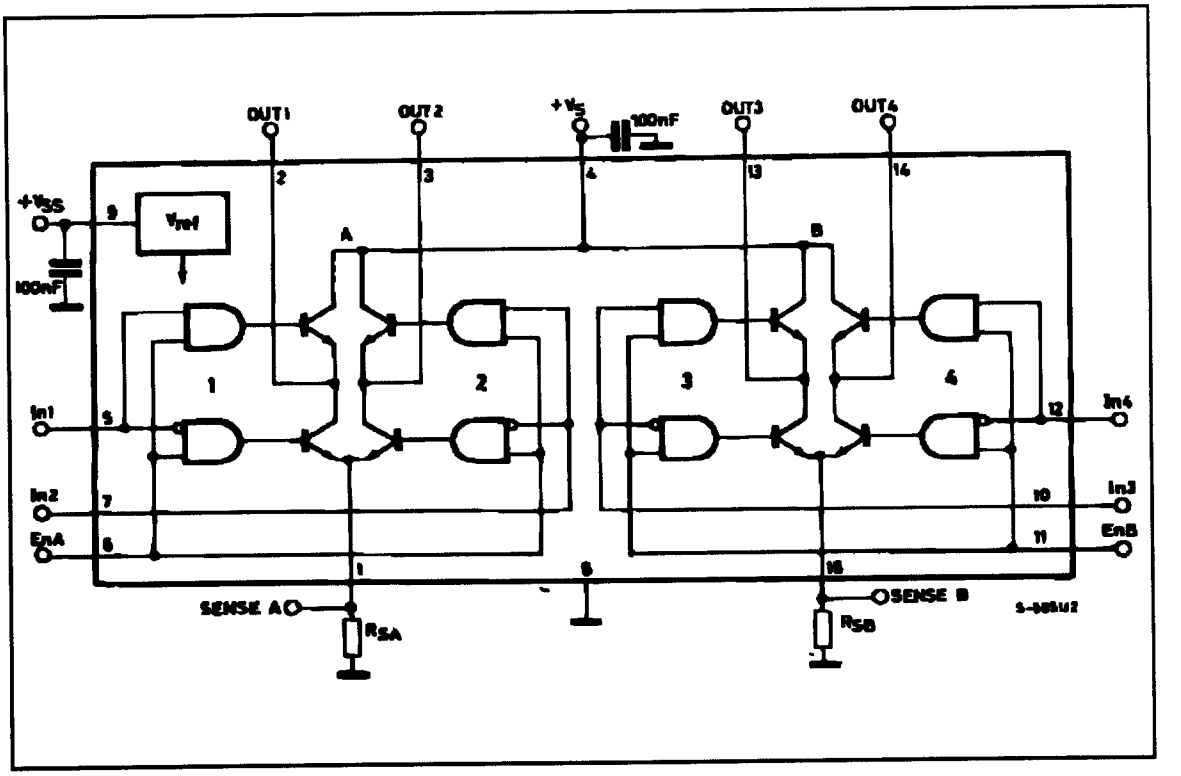
PowerSO20

ORDERING NUMBERS : L298N (Multiwatt Vert.)
L298HN (Multiwatt Horiz.)
L298P (PowerSO20)

DESCRIPTION

The L298 is an integrated monolithic circuit in a 15-lead Multiwatt and PowerSO20 packages. It is a high voltage, high current dual full-bridge driver designed to accept standard TTL logic levels and drive inductive loads such as relays, solenoids, DC and stepping motors. Two enable inputs are provided to enable or disable the device independently of the input signals. The emitters of the lower transistors of each bridge are connected together and the corresponding external terminal can be used for the connection of an external sensing resistor. An additional supply input is provided so that the logic works at a lower voltage.

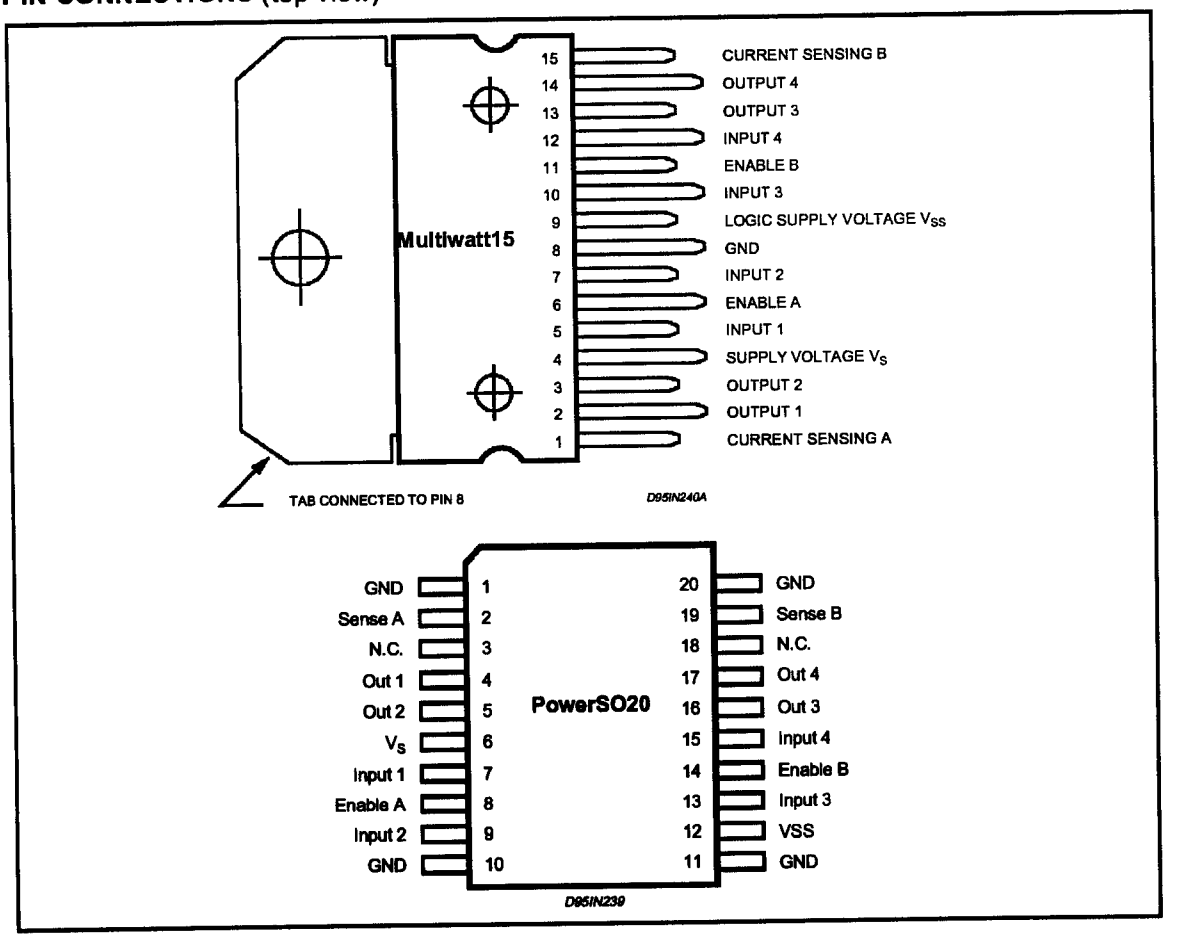
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Power Supply	50	V
V_{SS}	Logic Supply Voltage	7	V
V_i,V_{en}	Input and Enable Voltage	–0.3 to 7	V
I_O	Peak Output Current (each Channel) – Non Repetitive (t = 100µs) –Repetitive (80% on –20% off; t_{on} = 10ms) –DC Operation	 3 2.5 2	 A A A
V_{sens}	Sensing Voltage	–1 to 2.3	V
P_{tot}	Total Power Dissipation (T_{case} = 75°C)	25	W
T_{op}	Junction Operating Temperature	–25 to 130	°C
T_{stg}, T_j	Storage and Junction Temperature	–40 to 150	°C

PIN CONNECTIONS (top view)



THERMAL DATA

Symbol	Parameter		PowerSO20	Multiwatt15	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max.	–	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	13 (*)	35	°C/W

(*) Mounted on aluminum substrate

PIN FUNCTIONS (refer to the block diagram)

MW.15	PowerSO	Name	Function
1;15	2;19	Sense A; Sense B	Between this pin and ground is connected the sense resistor to control the current of the load.
2;3	4;5	Out 1; Out 2	Outputs of the Bridge A; the current that flows through the load connected between these two pins is monitored at pin 1.
4	6	V_S	Supply Voltage for the Power Output Stages. A non-inductive 100nF capacitor must be connected between this pin and ground.
5;7	7;9	Input 1; Input 2	TTL Compatible Inputs of the Bridge A.
6;11	8;14	Enable A; Enable B	TTL Compatible Enable Input: the L state disables the bridge A (enable A) and/or the bridge B (enable B).
8	1,10,11,20	GND	Ground.
9	12	VSS	Supply Voltage for the Logic Blocks. A100nF capacitor must be connected between this pin and ground.
10; 12	13;15	Input 3; Input 4	TTL Compatible Inputs of the Bridge B.
13; 14	16;17	Out 3; Out 4	Outputs of the Bridge B. The current that flows through the load connected between these two pins is monitored at pin 15.
–	3;18	N.C.	Not Connected

ELECTRICAL CHARACTERISTICS (V_S = 42V; V_{SS} = 5V, T_j = 25°C; unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_S	Supply Voltage (pin 4)	Operative Condition		V_{IH} +2.5		46	V
V_{SS}	Logic Supply Voltage (pin 9)			4.5	5	7	V
I_S	Quiescent Supply Current (pin 4)	V_{en} = H; I_L = 0	V_i = L		13	22	mA
			V_i = H		50	70	mA
		V_{en} = L	V_i = X			4	mA
I_{SS}	Quiescent Current from V_{SS} (pin 9)	V_{en} = H; I_L = 0	V_i = L		24	36	mA
			V_i = H		7	12	mA
		V_{en} = L	V_i = X			6	mA
V_{iL}	Input Low Voltage (pins 5, 7, 10, 12)			–0.3		1.5	V
V_{iH}	Input High Voltage (pins 5, 7, 10, 12)			2.3		VSS	V
I_{iL}	Low Voltage Input Current (pins 5, 7, 10, 12)	V_i = L				–10	µA
I_{iH}	High Voltage Input Current (pins 5, 7, 10, 12)	Vi = H ≤ V_{SS} –0.6V			30	100	µA
V_{en} = L	Enable Low Voltage (pins 6, 11)			–0.3		1.5	V
V_{en} = H	Enable High Voltage (pins 6, 11)			2.3		V_{SS}	V
I_{en} = L	Low Voltage Enable Current (pins 6, 11)	V_{en} = L				–10	µA
I_{en} = H	High Voltage Enable Current (pins 6, 11)	V_{en} = H ≤ V_{SS} –0.6V			30	100	µA
$V_{CEsat(H)}$	Source Saturation Voltage	I_L = 1A		0.95	1.35	1.7	V
		I_L = 2A			2	2.7	V
$V_{CEsat(L)}$	Sink Saturation Voltage	I_L = 1A (5)		0.85	1.2	1.6	V
		I_L = 2A (5)			1.7	2.3	V
V_{CEsat}	Total Drop	I_L = 1A (5)		1.80		3.2	V
		I_L = 2A (5)				4.9	V
V_{sens}	Sensing Voltage (pins 1, 15)			–1 (1)		2	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_1 (V_i)	Source Current Turn-off Delay	0.5 V_i to 0.9 I_L (2); (4)		1.5		µs
T_2 (V_i)	Source Current Fall Time	0.9 I_L to 0.1 I_L (2); (4)		0.2		µs
T_3 (V_i)	Source Current Turn-on Delay	0.5 V_i to 0.1 I_L (2); (4)		2		µs
T_4 (V_i)	Source Current Rise Time	0.1 I_L to 0.9 I_L (2); (4)		0.7		µs
T_5 (V_i)	Sink Current Turn-off Delay	0.5 V_i to 0.9 I_L (3); (4)		0.7		µs
T_6 (V_i)	Sink Current Fall Time	0.9 I_L to 0.1 I_L (3); (4)		0.25		µs
T_7 (V_i)	Sink Current Turn-on Delay	0.5 V_i to 0.9 I_L (3); (4)		1.6		µs
T_8 (V_i)	Sink Current Rise Time	0.1 I_L to 0.9 I_L (3); (4)		0.2		µs
fc (V_i)	Commutation Frequency	I_L = 2A		25	40	KHz
T_1 (V_{en})	Source Current Turn-off Delay	0.5 V_{en} to 0.9 I_L (2); (4)		3		µs
T_2 (V_{en})	Source Current Fall Time	0.9 I_L to 0.1 I_L (2); (4)		1		µs
T_3 (V_{en})	Source Current Turn-on Delay	0.5 V_{en} to 0.1 I_L (2); (4)		0.3		µs
T_4 (V_{en})	Source Current Rise Time	0.1 I_L to 0.9 I_L (2); (4)		0.4		µs
T_5 (V_{en})	Sink Current Turn-off Delay	0.5 V_{en} to 0.9 I_L (3); (4)		2.2		µs
T_6 (V_{en})	Sink Current Fall Time	0.9 I_L to 0.1 I_L (3); (4)		0.35		µs
T_7 (V_{en})	Sink Current Turn-on Delay	0.5 V_{en} to 0.9 I_L (3); (4)		0.25		µs
T_8 (V_{en})	Sink Current Rise Time	0.1 I_L to 0.9 I_L (3); (4)		0.1		µs

1) 1)Sensing voltage can be –1 V for t ≤ 50 µsec; in steady state V_{sens} min ≥ –0.5 V.
2) See fig. 2.
3) See fig. 4.
4) The load must be a pure resistor.

Figure 1 : Typical Saturation Voltage vs. Output Current.

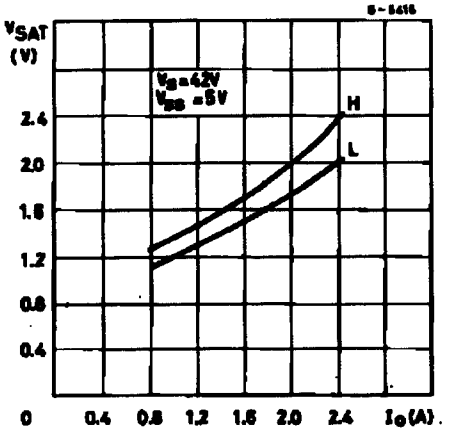
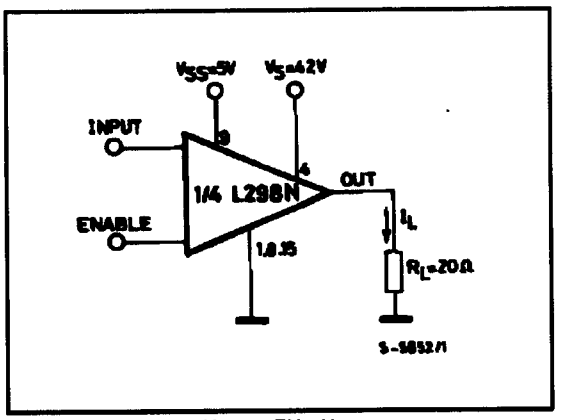


Figure 2 : Switching Times Test Circuits.



Note : For INPUT Switching, set EN = H
For ENABLE Switching, set IN = H