TEMPERATURE MONITORING AND PROFILE GENERATION FOR THE REFLOW SOLDERING SYSTEM AND THE TEST CABINS

P - 1402

PROJECT REPORT

Submitted by

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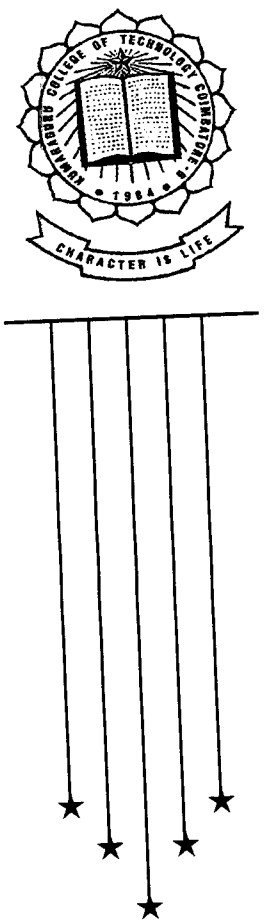

2002-2003

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE AWARD OF THE DEGREE OF
BACHELOR OF ENGINEERING IN
ELECTRONICS AND COMMUNICATION ENGINEERING
OF BHARATHIAR UNIVERSITY

Department of Electronics & Communication Engineering
College of Technology

KUMARAGURU COLLEGE OF TECHNOLOGY

Coimbatore - 641 038

Department of Electronics and communication engineering

Certificate

This is to certify that this project entitled

Temperature monitoring and Profile Generation for the Reflow Soldering System and the Test Cabins

Has been submitted by

Ms. / Mr. .....

In partial fulfillment of the requirements for the award of the Degree of Bachelor of Engineering in the Electronics and Communication Engineering Branch of Bharathiar University, Coimbatore - 641 046 during the Academic year 2002-03

B. D... 17/3/03

(Guide)

.....

(Head of the Department)

Certified that, the candidate was examined by us in the Project Work. Viva-Voce Examination held on ...MARCH 18, 2003.....

University Register Number

.....

.....

(Internal Examiner)

.....

(External Examiner)

PREMIER

CERTIFICATE

This is to certify that the following B.E [Branch: Electronics and Communication Engineering] students of KUMARAGURU COLLEGE OF TECHNOLOGY, Coimbatore, had undertaken their project '**Temperature monitoring and Profile Generation for the Reflow Soldering System and the Test Cabins**', from April 2002 to February 2003 at our industry and have successfully completed it.

1.Ms. Kanthimathi Gayatri S
2.Ms. Kousalya Devi S
3.Ms. Krishnaveni B
4.Ms. Preethi Gopu

Their performance during that period was found to be good. We wish them all success.

Place: Coimbatore
Date: 17/03/03

Industry Seal

Premier Polytronics Pvt. Limited
304, Trichy Road, Singanallur,
COIMBATORE - 641 005.

B Shanmuga Sundaram
Manager - OFC

Synopsis

SYNOPSIS:

This project is aimed at generating the temperature profile for the Reflow Soldering System (4036 – 1.7) SEHO Seitz & Hohnerlein and the test cabins at Premier Polytronics Pvt. Ltd.

The profile generated, provides the temperature that existed in the heating zones, through which the Printed Circuit Boards passed through, for the soldering of the surface mountable devices or components. This can be compared with the ideal values, depending on which, the Printed Circuit Board soldered could be rejected or sent for further testing.

This project caters to the need at Premier Polytronics Pvt. Ltd. for temperature monitoring and profile generation for the Reflow Soldering System and the test cabins.

The same system designed for the Reflow Soldering System could be used to monitor the temperature within the test cabins where products, involving transducers, manufactured by Premier Polytronics Pvt. Ltd., are caliberated.

Acknowledgement

ACKNOWLEDGEMENT:

We express our sincere thanks to our principal, *Dr. K K Padmanaban, B.Sc. (Engg.), M.Tech., Ph.D.*, for all the facilities provided for carrying out our project work..

We express our profound gratitude and indebtedness to our respected *Head of the Department* and *Prof. M.Ramasamy, M.E.,(Ph.D), MIEEE, MISTE,*for his technical guidance, timely suggestions and support provided during the project.

We express our thanks and heartfelt gratitude to our guide *Mrs. B Devi, M.E.*, for providing her suggestions, support and for being with us throughout the project.

We thank the organization, *Premier Polytronics Pvt. Ltd.*, for facilitating us to obtain hands-on experience in the industry by providing us an opportunity to cater to their need through this project.

We also express our sincere thanks to *Mr. B Shanmugasundaram, OFC,* at *Premier Polytronics Pvt. Ltd.*, for his guidance and timely help during the project.

We express our thanks and gratitude to *Mrs. M Kalpana* at *Premier Polytronics Pvt. Ltd.*, for the immense amount of technical support provided for the project.

We conclude the acknowledgement by thanking all the *teaching and non-teaching staff* for the guidance provided throughout the project, without whom our project would not have been a success.

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The need for the Project

THE NEED FOR THIS PROJECT:

1. The products that are tested at the test cabins employ a variety of transducers to convert physical parameters into electrical signals. These transducers need to be calibrated at a specific condition for ensuring its performance over the entire range of measurement values in either a linear form or as per a curve that is characteristic in nature of the transducer.

2. To eliminate the assignable causes that could influence the performance of the transducer with respect to temperature.

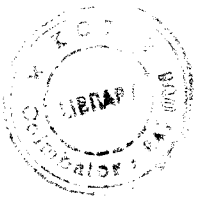
3. To control the process variations in terms of the ambient conditions, with respect to temperature, that could influence the decision of accepting or rejecting a transducer produced.

4. To reduce the assignable causes with respect to soldering of the devices onto the Printed Circuit Board in terms of solder temperature variation that is acceptable by the device.

5. As the number of Printed Circuit Boards to be soldered is of varied dimensions and component count, the profile of heat applied to solder needs to be changed and hence to arrive at a profile suitable for each type of PCB, the profile generator needs to be deployed.

Introduction

INTRODUCTION:



This project is aimed at generating the profile of the temperature that existed in the Reflow Soldering System heating zones, when a batch of Printed Circuit Boards are sent through it. The system is used to solder the Surface Mountable Devices or components on to the Printed Circuit Boards.

When the Surface Mountable Devices are to be soldered, they pass through three heating zones and a cooling zone. In the first zone, the heating is up to approximately 145 ^{0}C with a gradual change of 2 ^{0}C per second as the conveyor belt moves on. The purpose of this zone is the evaporation of solvents. The Printed Circuit Boards exist in the second zone for duration range of 60 to 120 seconds. Here the temperature is maintained at 145 ^{0}C for the activation of fluxes and chemical reduction. In the third zone, the temperature is raised to approximately 210 ^{0}C to 225 ^{0}C. The purpose of it is to melt the metallic content in the solder paste. After the peak is attained, the Printed Circuit Board is cooled using a fan and the maximum temperature is 183 ^{0}C and is gradually reduced for 60 seconds. This is done to prevent any

thermal shock on the temperature sensitive components. The grouping of the heating zones and a sample profile are shown on page 14.

Though the Reflow Soldering System is designed to cause no errors, the actual temperature existing in the machine might vary and this can cause damages to the Mountable Devices or can cause faulty soldering which will lead to the improper working of the entire Printed Circuit Board. The faulty boards are generally detected by testing each board individually. Instead of the usual routine, the profile of the heat that existed during soldering could be generated and the Printed Circuit Boards could be directly rejected without testing or sent for further testing depending on the profile obtained. This leads to our project.

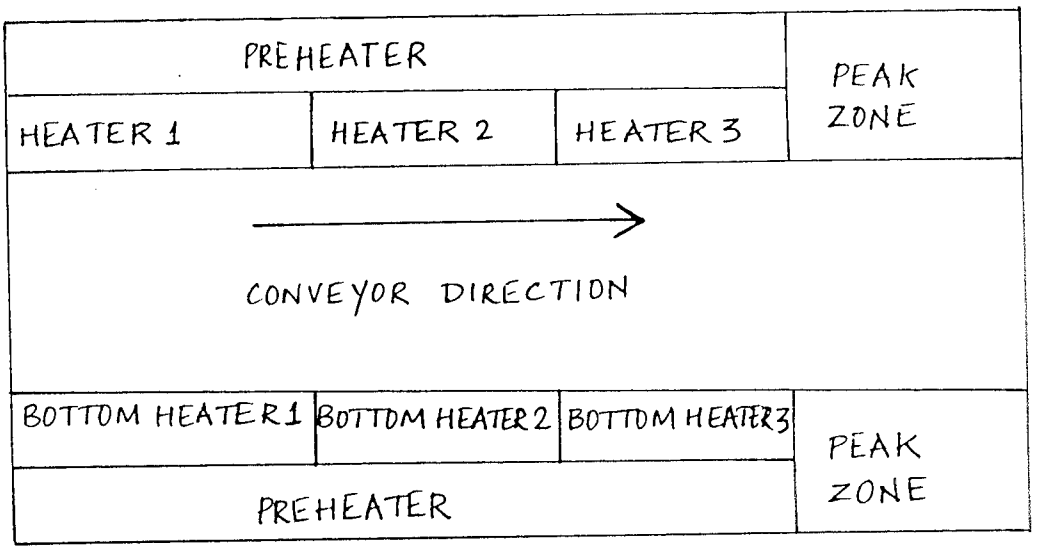
To accomplish the profile generation, we use a thermocouple as the temperature sensor. This is passed through the Reflow Soldering System, along with the Printed Circuit Boards. The electrical signal generated by the thermocouple in response to the temperature variations, is digitized and processed at the thermocouple end using a processing unit. This signal is transmitted to the Personal Computer located far apart from the Reflow

Soldering System and near the user, by UART. The received signal at the Personal Computer end is processed, and the profile generated.

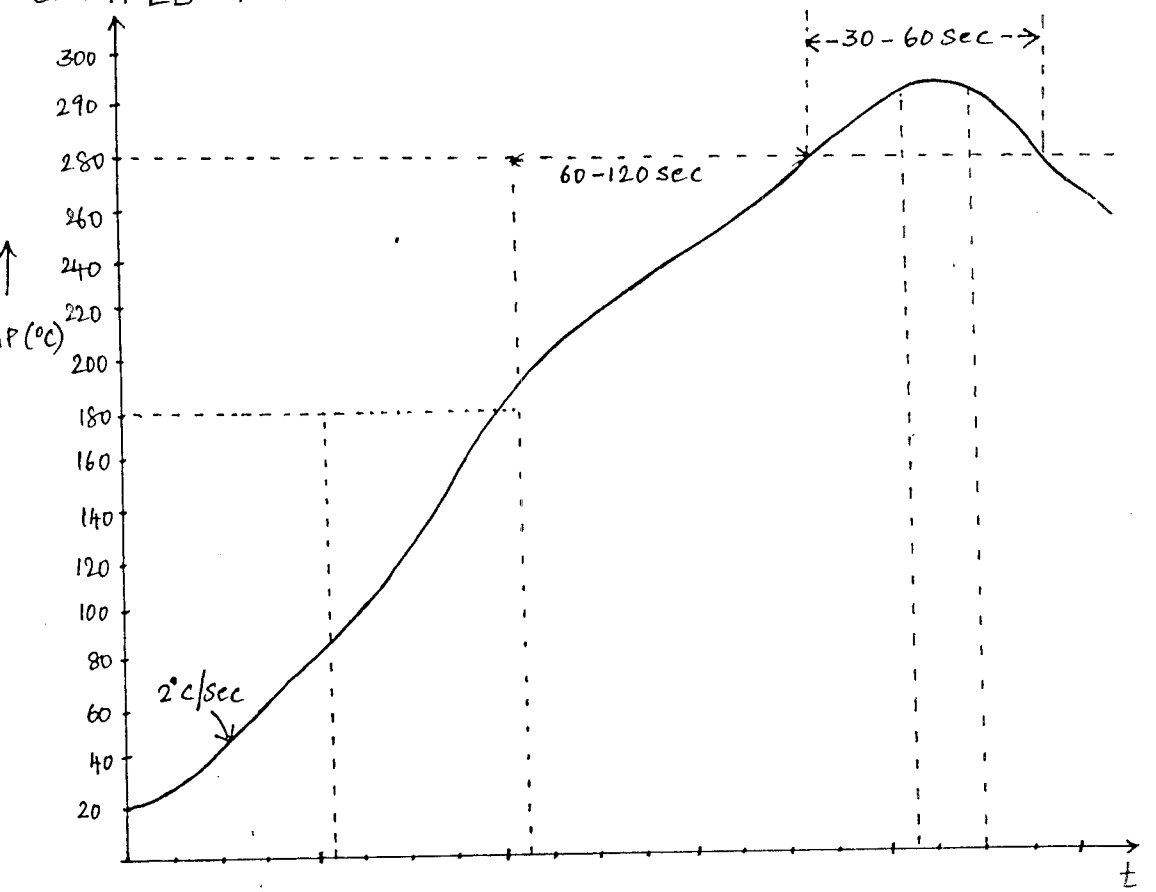
The block or modular diagram of the profile generation process is shown on page 15.

The same system can be used to monitor the temperature existing within the test cabins, where the transducer involving products manufactured by Premier Polytronics Pvt. Ltd. are calibrated.

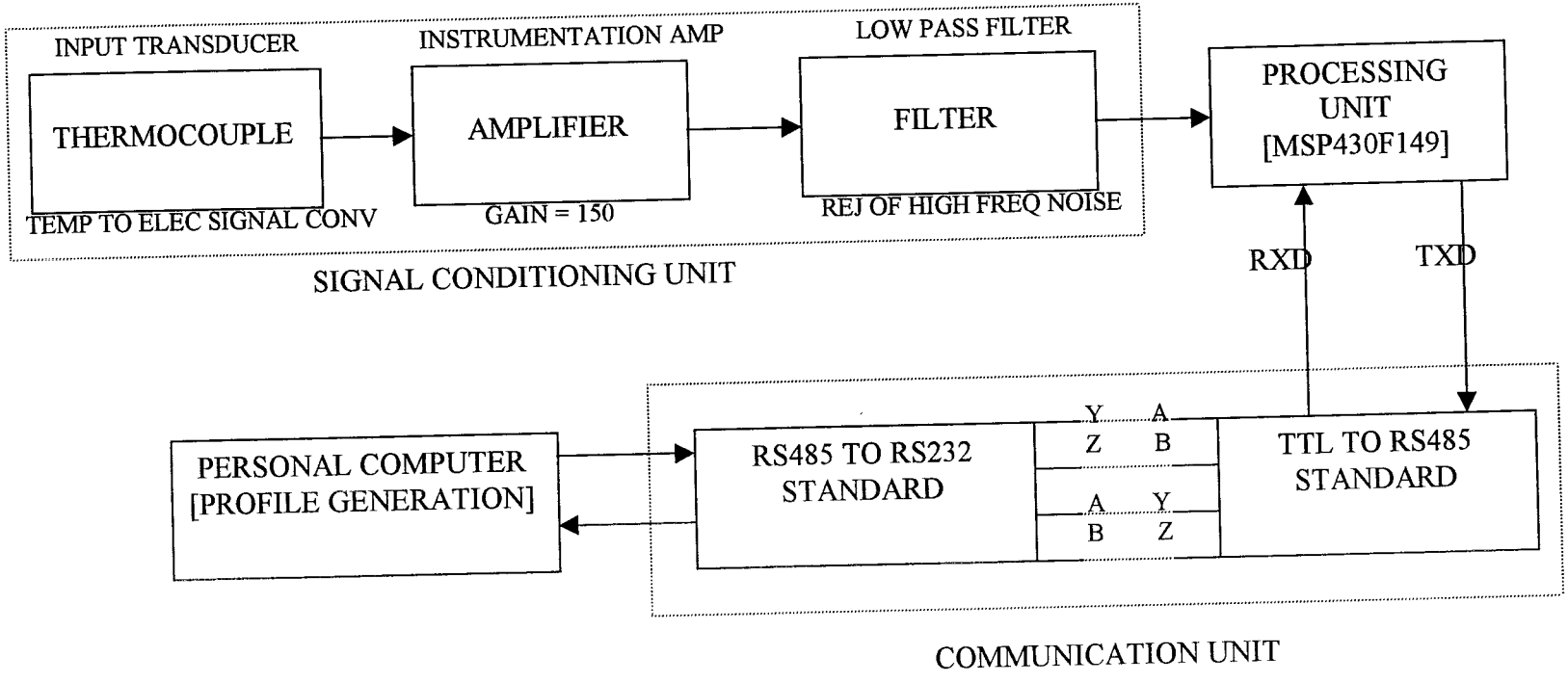
GROUPING OF HEATING ZONES:



SAMPLE PROFILE



MODULAR DIAGRAM:



Project Modules

PROJECT MODULES:

The entire project can be sub-divided into different modules depending on the functionality. The modules are:

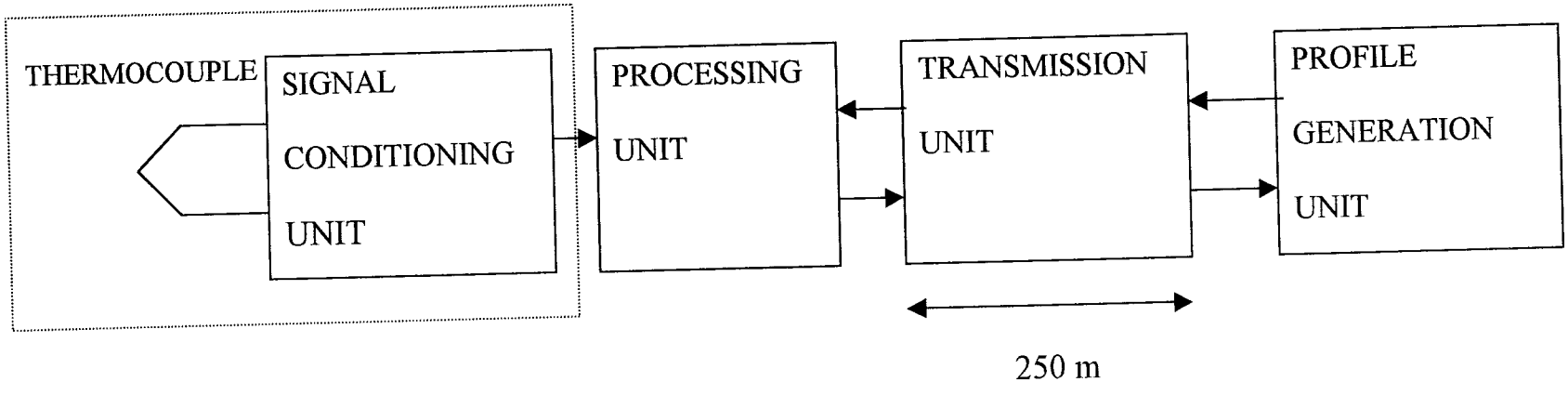
1. Signal Conditioning Unit
2. Processing Unit
3. Communication Unit
4. Profile Generation Unit

The Signal Conditioning Unit and the Processing Unit are attached to the end of the Thermocouple. The Processing Unit is present immediately after the Signal Conditioning Unit, since the sensor output is feeble. This reduces the errors.

The Communication Unit consists of the Transmission Circuitry at the Processing Unit end and the Reception Circuitry at the Personal Computer end.

The Profile Generation Unit consists of the Personal Computer with the necessary coding in C language for reception of data and profile generation.

BLOCK DIAGRAM:



SIGNAL CONDITIONING UNIT:

The Signal Conditioning Unit consists of three parts, the thermocouple, the amplifier and the filter.

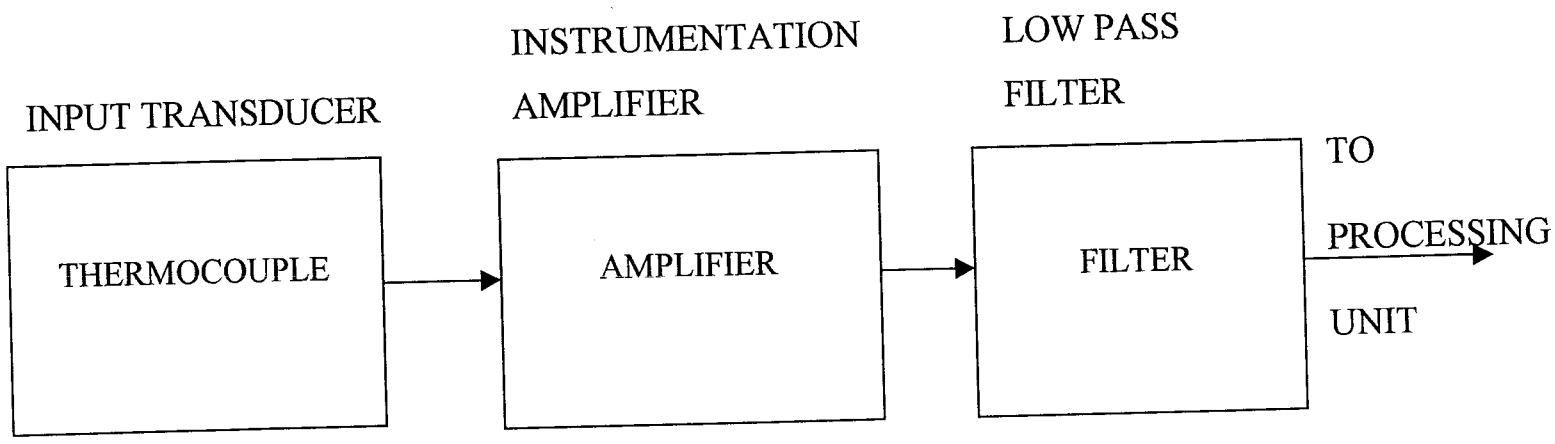
The thermocouple to be used for this project has been selected to be the K-Type thermocouple. The choice has been made, after analyzing the properties of various thermocouples. The range of temperature to which the thermocouple is to be subjected to is 0 ^{0}C to 300 ^{0}C. The output of the thermocouple is directly connected to the input of the amplifier.

The block diagram of the Signal Conditioning Unit is provided on the next page.

The amplifier used here is the Instrumentation amplifier. This amplifier is chosen to reduce errors. The circuit diagram of the amplifier is provided on page 28.

The amplifier output is fed to the Low Pass Filter. The filter is included to remove all the high frequency noise signals. The output of this stage is fed to the Processing Unit.

BLOCK DIAGRAM OF THE SIGNAL CONDITIONING UNIT:



PROCESSING UNIT:

The function of the Processing Unit is to digitize the signal, process it and transmit it by asynchronous transmission.

The Processing Unit mainly consists of the MSP430F149 microcontroller. Considering its features, which tend to reduce the circuitry necessitated by the Processing Unit, this microcontroller is chosen.

The Features of MSP430F149:

1. Low supply voltage range
2. Ultra low power consumption
3. Low operating current
4. 16-bit RISC architecture
5. 12-bit A/D converter with internal reference, sample-and-hold and autoscan feature.
6. 16-bit Timer with three capture/compare registers
7. On-chip comparator

The input from the Signal Conditioning Unit is fed into channel a0 of the analog multiplexer inputs of the microcontroller.

The microcontroller is programmed to digitize the input at channel a0. The input signal range is set to be within 0V to 1.5V. The microcontroller has a built in clock, which is used here for sampling.

The 12 - bit analog to digital converter is built in. Each channel has a separate memory to store the corresponding digital value. The cabin inputs could be connected to other channels.

The digital three-nibble value is separated into individual nibbles. A conversion is performed on each nibble. The ASCII value of each is obtained through programming and this is transmitted. A zero nibble is added in front of the three nibbles to make it a 2-byte data. The ASCII value of Space is transmitted between each data for clarity at the reception side.

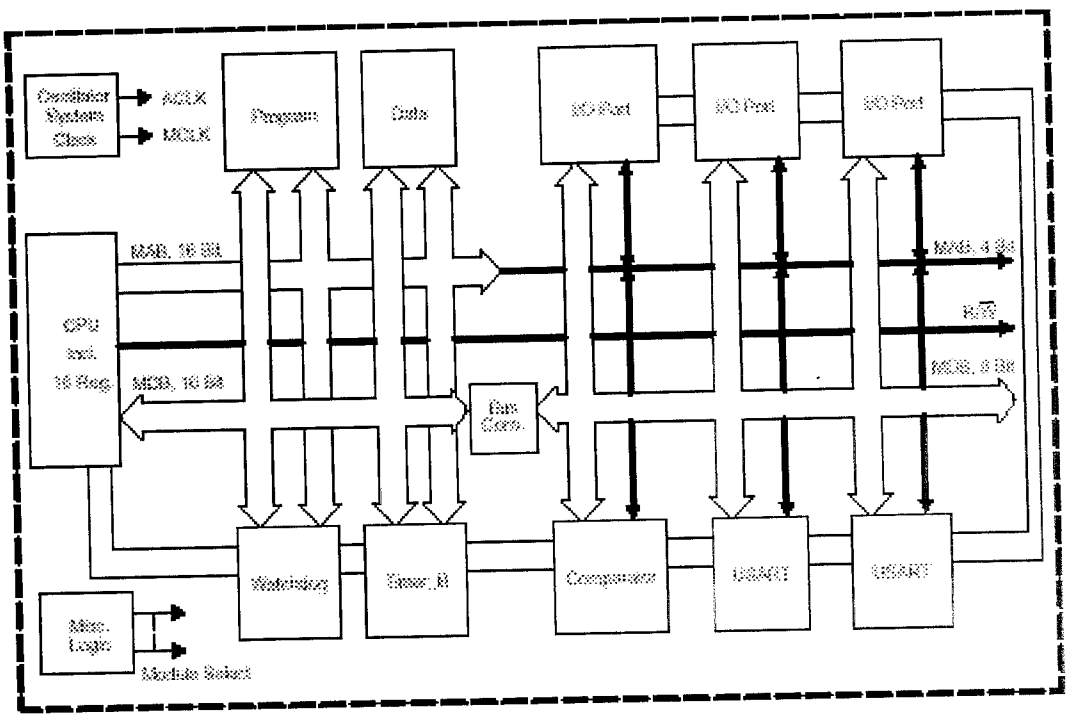
The transmission is done in the UART mode. The MSP430F149 is configured for Asynchronous Transmission. The output of the microcontroller is of the TTL level. This voltage level is feeble for transmission over a distance of 250 meters. This difficulty is overcome in the Communication Unit.

The circuitry for the Processing Unit is provided on page 29. The coding for the microcontroller programming is provided on page 37.

ARCHITECTURAL OVERVIEW:

The architecture of the MSP430 family is based on a memory-to-memory architecture, a common address space for all functional blocks, and a reduced instruction set applicable to all functional blocks. The MSP430 von-Neumann architecture has RAM, ROM, and peripherals in one address space, both using a single address and data bus. This allows using the same instruction to access RAM, ROM, or peripherals and also allows code execution from RAM.

The following diagram shows the architecture of MSP430F149:



CENTRAL PROCESSING UNIT:

The CPU incorporates a reduced and highly transparent instruction set and a highly orthogonal design. It consists of a 16-bit arithmetic logic unit (ALU), 16 registers, and instruction control logic. Four of these registers are used for special purposes. These are the program counter (PC), stack pointer (SP), status register (SR), and constant generator (CGx). The constant generator supplies instruction constants, and is not used for data storage. The CPU control over the program counter, the status register, and the stack pointer (with the reduced instruction set) allows the development of applications with sophisticated addressing modes and software algorithms.

PROGRAM MEMORY:

Instruction fetches from program memory are always 16-bit accesses, whereas data memory can be accessed using word (16-bit) or byte (8-bit) instructions. Any access uses the 16-bit memory data bus (MDB) and as any of the least-significant address lines of the memory address bus (MAB) as required to access the memory locations. Blocks of memory are automatically selected through module-enable signals. This technique

reduces overall current consumption. Program memory is integrated as programmable or mask-programmed memory. In addition to program code, data may also be placed in the ROM section of the memory map and may be accessed using word or byte instructions; this is useful for data tables, for example. This unique feature gives the MSP430 an advantage over other microcontrollers, because the data tables do not have to be copied to RAM for usage. Sixteen words of memory are reserved for reset and interrupt vectors at the top of the 64-kilobytes address space from 0FFFFh down to 0FFE0h.

DATA MEMORY:

The data memory is connected to the CPU through the same two buses as the program memory (ROM): the memory address bus (MAB) and the memory data bus (MDB). The data memory can be accessed with full (word) data width or with reduced (byte) data width. Additionally, because the RAM and ROM are connected to the CPU via the same busses, program code can be loaded into and executed from RAM. This is another unique feature of the MSP430 devices, and provides valuable, easy-to-use debugging capability.

CPU REGISTERS:

Sixteen 16-bit registers (R0, R1, and R4 to R15) are used for data and addresses and are implemented in the CPU. They can address up to 64 Kbytes without any segmentation.

SPECIAL FUNCTION REGISTERS:

THE PROGRAM COUNTER (PC):

The 16-bit program counter points to the next instruction to be executed. Each instruction uses an even number of bytes (two, four, or six), and the program counter is incremented accordingly. Instruction accesses are performed on word boundaries, and the program counter is aligned to even addresses.

THE SYSTEM STACK POINTER (SP):

The system stack pointer must always be aligned to even addresses because the stack is accessed with word data during an interrupt request

service. The system SP is used by the CPU to store the return addresses of subroutine calls and interrupts. It uses a predecrement, postincrement scheme. The advantage of this scheme is that the item on the top of the stack is available. The SP can be used by the user software (PUSH and POP instructions), but the user should remember that the CPU also uses the SP.

THE STATUS REGISTER (SR):

The status register SR contains the CPU status bits. They are:

- V — Overflow bit
- SCG1 — System clock generator control bit 1
- SCG0 — System clock generator control bit 0
- OscOff — Crystal oscillator off bit
- CPUOff — CPU off bit
- GIE — General interrupt enable bit
- N — Negative bit
- Z — Zero bit
- C — Carry bit

THE CONSTANT GENERATOR REGISTERS CG1 AND CG2:

Commonly used constants are generated with the constant generator registers R2 and R3, without requiring an additional 16-bit word of program code. The constant used for immediate values is defined by the addressing mode bits.

OSCILLATOR AND SYSTEM CLOCK:

Three clocks are used in the system - the main system (master) clock (MCLK) used by the CPU and the system, the subsystem (master) clock (SMCLK) used by the peripheral modules, and the auxiliary clock (ACLK) originated by LFXT1CLK (crystal frequency) and used by the peripheral modules.

DIGITAL I/O:

There are six 8-bit I/O ports implemented—ports P1 through P6. Ports P1 and P2 use seven control registers, while ports P3, P4, P5, and P6 use

only four of the control registers to provide maximum digital input/output flexibility to the application:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Interrupt processing of external events is fully implemented for all eight bits of ports P1 and P2.
- Read/write access to all registers using all instructions is possible.

WATCHDOG TIMER:

The primary function of the Watchdog Timer (WDT) module is to perform a controlled system restart after software upset has occurred. A system reset is generated if the selected time interval expires. If an application does not require this watchdog function, the module can work as an interval timer, which generates an interrupt after a selected time interval. The Watchdog Timer counter (WDTCNT) is a 15/16-bit up-counter not directly accessible by software.

USART0 and USART1:

There are two USART peripherals implemented in the MSP430x14x: USART0 and USART1. They use different pins to communicate, and different registers for module control. Registers with identical functions have different addresses. The universal synchronous/asynchronous interface is a dedicated peripheral module used in serial communications. The USART supports synchronous SPI and asynchronous UART communication protocols, using double-buffered transmit and receive channels.

TIMER A:

The timer module offers one sixteen-bit counter and three capture/compare registers. The timer can be fully controlled (in word mode)—it can be halted, read, and written; it can be stopped, run continuously, or made to count up or up/down using one compare block to determine the period. The blocks are configured by the application to run in capture or compare mode. The capture mode is mostly used to individually measure internal or external events from any combination of positive, negative, or positive and negative edges. The compare mode is mostly used

o generate timing for the software or application hardware, or to generate pulse-width modulated output signals for various purposes like D/A conversion functions or motor control.

TIMER B:

Timer B is identical to Timer A, except for the following:

The timer counter can be configured to operate in 8, 10, 12, or 16-bit mode. The function of the capture/compare registers is slightly different when in compare mode. In Timer B, the compare data is written to the capture/compare register, but is then transferred to the associated compare latch for the comparison. Timer B has seven capture compare registers.

A/D CONVERTER:

The 12-bit analog-to-digital converter (ADC) uses a 10-bit weighted capacitor array plus a 2-bit resistor string. The CMOS threshold detector in the successive-approximation conversion technique determines each bit by examining the charge on a series of binary-weighted capacitors. The features

- 12-bit converter with ±1 LSB linearity
- Built-in sample-and-hold
- Eight external and four internal analog channels.
- Internal reference voltage V REF+ of 1.5 V or 2.5 V.
- Internal-temperature sensor for temperature measurement
- T = (V_SENSOR(T) – V_SENSOR(0C)) / TC_SENSOR in °C

The conversion result is stored in one of sixteen registers. The sixteen registers have individual addresses and can be accessed via software. Each of the sixteen registers is linked to an 8-bit register that defines the positive and negative reference source and the channel assigned.

FLASH MEMORY:

Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size. Segments 0 to n may be erased in one step or each segment may be individually erased. Segments A and B can be erased individually, or as a group with segments 0–n. Segments A and B are also called *information memory.* Program and erase timing is controlled by

program or erase, no code can be executed from flash memory and all interrupts must be disabled. If a user program requires execution concurrent with a flash program or erase operation, the program must be executed from memory other than the flash memory (e.g., boot ROM, RAM).

GLOBAL INTERRUPT STRUCTURE:

There are four types of interrupts:

System reset, Maskable, Non-maskable & Maskable

Maskable interrupts are caused by:

- A watchdog-timer overflow (if timer mode is selected)
- Other modules with interrupt capability

Non-maskable interrupts are not maskable in any way. No individual interrupt enable bit is implemented for them, and the general interrupt enable bit (GIE) has no effect on them.

Maskable interrupts are not masked by the general interrupt enable bit (GIE) but are individually enabled or disabled by an individual interrupt enable bit. The RETI (return from interrupt) instruction has no effect on the individual enable bits of the maskable interrupts.

COMMUNICATION UNIT:

The Communication Unit comprises of the circuitry involved in the communication of data between the Processing Unit and the Profile Generation Unit.

The output of the microcontroller is the TTL level. Since this is low, it has to be converted to another standard for efficient communication. Since the distance of transmission is around 250 meters, the RS485 standard is chosen. The standard accepted by the Personal Computer is the RS232 standard. So the Communication Unit is divided into two sub modules:

1. TTL to RS485 Conversion sub module
2. RS485 to RS232 Conversion sub module

The TTL to RS485 Conversion sub module is at the Processing Unit end. The RS485 to RS232 Conversion sub module is connected to the TTL to RS485 Conversion sub module by a 250-meter cable. The RS485 to RS232 Conversion sub module output is connected to the Personal Computer.

TTL to RS485 Conversion sub module:

The TxD signal from the microcontroller is fed into this module. This signal is fed to the comparator to produce logic 1 or logic 0 signals depending on the input level. This is done to correct the levels, if they have suffered attenuation. This signal is fed to an optical isolator, which electrically isolates the rest of the circuit from the comparator and the microcontroller. The signal from the optical isolator is fed to a TTL to RS485 converter, MAX488. The output of this is sent to the RS485 to RS232 Conversion sub module.

Circuit has also been designed to receive signal from the RS485 to RS232 Conversion sub module. This is fed to the comparator through an optical isolator and then to the microcontroller. This has been provided for future development.

The TTL to RS485 Conversion sub module circuitry is provided on page 30. The block diagram of the Communication Unit is on page 25.

RS485 to RS232 Conversion sub module:

Here the RS485 standard is converted to the Personal Computer compatible RS232 standard. The received RS485 standard signal is fed to the MAX488 IC to convert it to the TTL level. This signal is again fed to the MAX232 IC to convert it to the RS232 level. This signal is fed to the Personal Computer through a 9-pin connector.

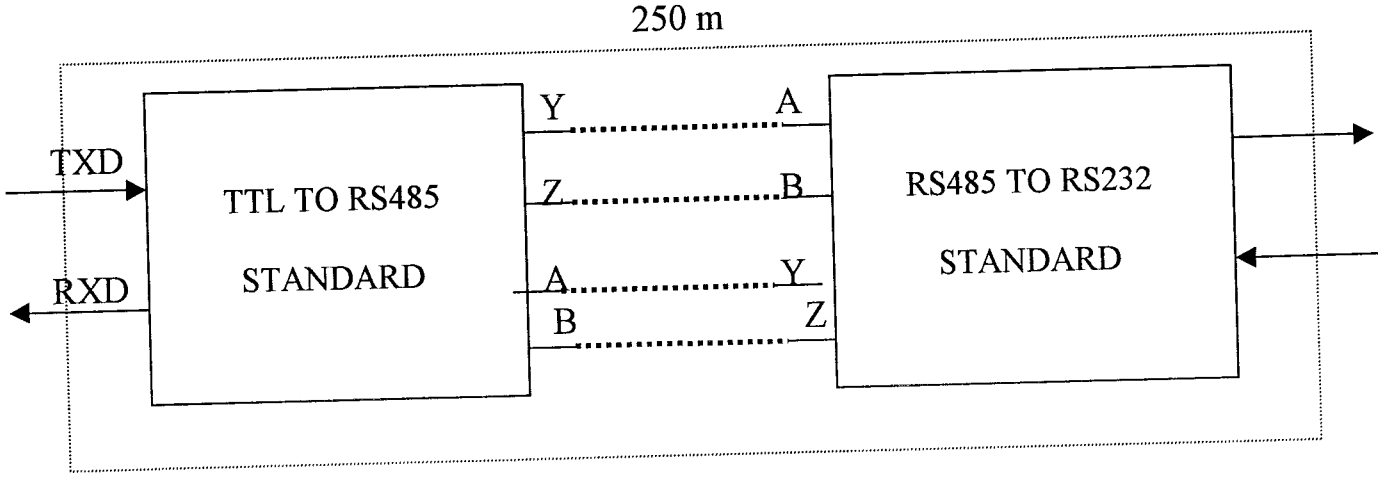
Signal from the Personal Computer can also be fed to the TTL to RS485 Conversion sub module through the MAX232 and MAX485 ICs.

The RS485 to RS232 Conversion sub module circuitry is provided on page 31. The block diagram of the Communication Unit is on page 25.

COMMUNICATION UNIT:

FROM AND TO
PROCESSING UNIT

TO AND FROM
PROFILE
GENERATION UNIT



RS – 485:

RS 485 allows multiple devices (upto 32) to communicate at half duplex on a single pair of wires plus a ground wire at distances upto 1200 metres. RS 485 uses a different principle: Each signal uses one twisted pair (TP) line - two wires twisted around themselves - 'Differential voltage transmission'. It uses differential transmitters with alternating voltages 0 and 5V.

RS 485 is used for multipoint communications. More devices may be connected to a single signal cable - similar to e.g. ETHERNET networks, which use coaxial cable. Most RS 485 systems use Master/Slave architecture, where each slave unit has its unique address and responds only to packets addressed to this unit. These packets are generated by Master (e.g. PC), which periodically polls all connected slave units.

For a basic RS 485 system, an I/O driver with differential outputs and an I/O receiver with differential inputs is required. Noise and interference is introduced into the line; however, since the signal is transferred via a twisted pair of wires, the voltage difference (between A and B) of this interference is

almost zero. Due to the differential function of the RS 485 input amplifier of the receiver, this interference is eliminated.

RS 485 circuits are more complex, and thus more expensive. Higher data transfer speeds require correctly connected and matched terminations, which can be a problem in systems where the number of connected devices changes. Since the data transfer is bidirectional, the line needs to have a terminating resistor at both ends.

From a network point of view, the RS 485 incorporates a bus topology. Since Slave stations have no means of starting the communication without a risk of collision, they need to be assigned a 'right to transmit' by the Master station.

RS 485 networks can typically maintain correct data with a difference of -7 to +12 V. If the grounds differ more than this amount, the data will be lost and the port will be damaged. Hence common ground is used. If the differences between the signal grounds are too much, optical isolation is preferred.

RS-232:

RS-232 provides serial connections using single ended signals, which may vary between -3 to -25 volts to +3 to +25 volts. Minimal signals for bi-directional communication are signal ground/common, Transmit (Tx) and Receive (Rx) Data or TD and RD. IBM PC compatible RS-232C ports provide handshaking lines, DSR and DTR and flow control handshaking lines, CTS and RTS. Modem control lines for RI (Ring Indicator) and CD (Carrier Detector) are supported. Data is transferred serially using Asynchronous data, with a start bit, data bits, stop bit/bits. Flow control can be performed by software using X-On/X-Off, or by hardware handshaking if available.

The truth table for RS232 is:

Signal > +3v = 0

Signal < -3v = 1

The output signal level usually swings between +12v and -12v. The "dead area" between +3v and -3v is designed to absorb line noise. Many receivers designed for RS-232 are sensitive to differentials of 1 volt or less.

The standards for RS-232 and similar interfaces usually restrict RS-232 to 20kbps or less and line lengths of 15m (50 ft) or less. RS-232 is simple, universal, well understood and supported everywhere. However, it has some serious shortcomings as an electrical interface.

Firstly, the interface presupposes a common ground between the DTE and DCE. This is a reasonable assumption where a short cable connects a DTE and DCE in the same room. There are some spectacular electrical events causes by "uncommon grounds".

Secondly, a signal on a single line is impossible to screen effectively for noise. By screening the entire cable one can reduce the influence of outside noise, but internally generated noise remains a problem. As the baud rate and line length increase, the effect of capacitance between the cables introduces serious crosstalk until a point is reached where the data itself is unreadable.

Crosstalk can be reduced by using low capacitance cable. Also, as it is the higher frequencies that are the problem, control of slew rate in the signal also decreases the crosstalk. These limitations are largely eliminated by using balanced line interface.

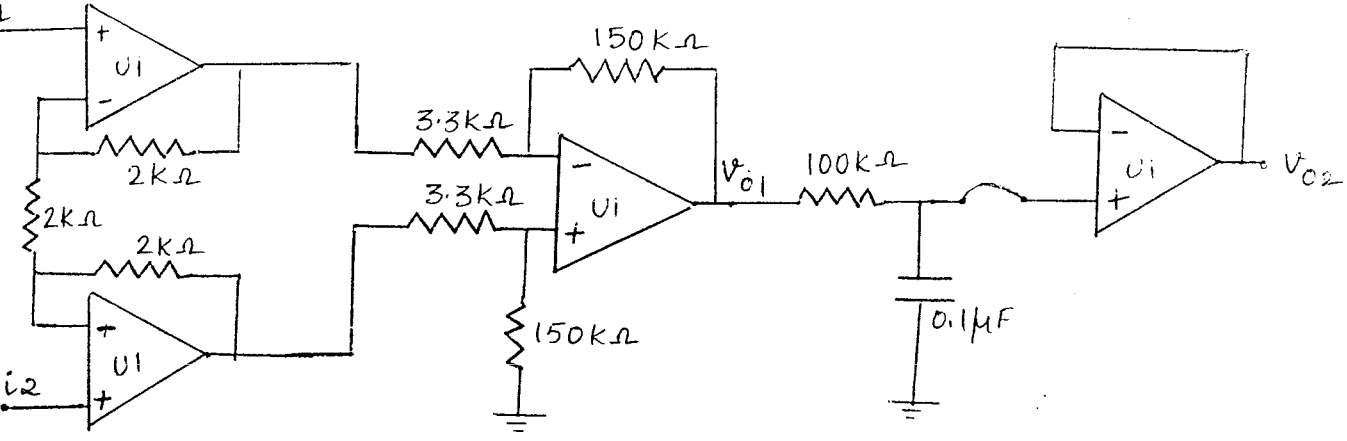
PROFILE GENERATION UNIT:

The profile generation is done using the C language. The received data is converted to its equivalent in temperature using conversion formula obtained form the thermocouple properties and the amplification used.

Using graphics, the temperature profile and the graph are displayed to the user.

The coding in the C language is provided on page 41.

Hardware



V_{i1}, V_{i2} – THERMOCOUPLE INPUTS

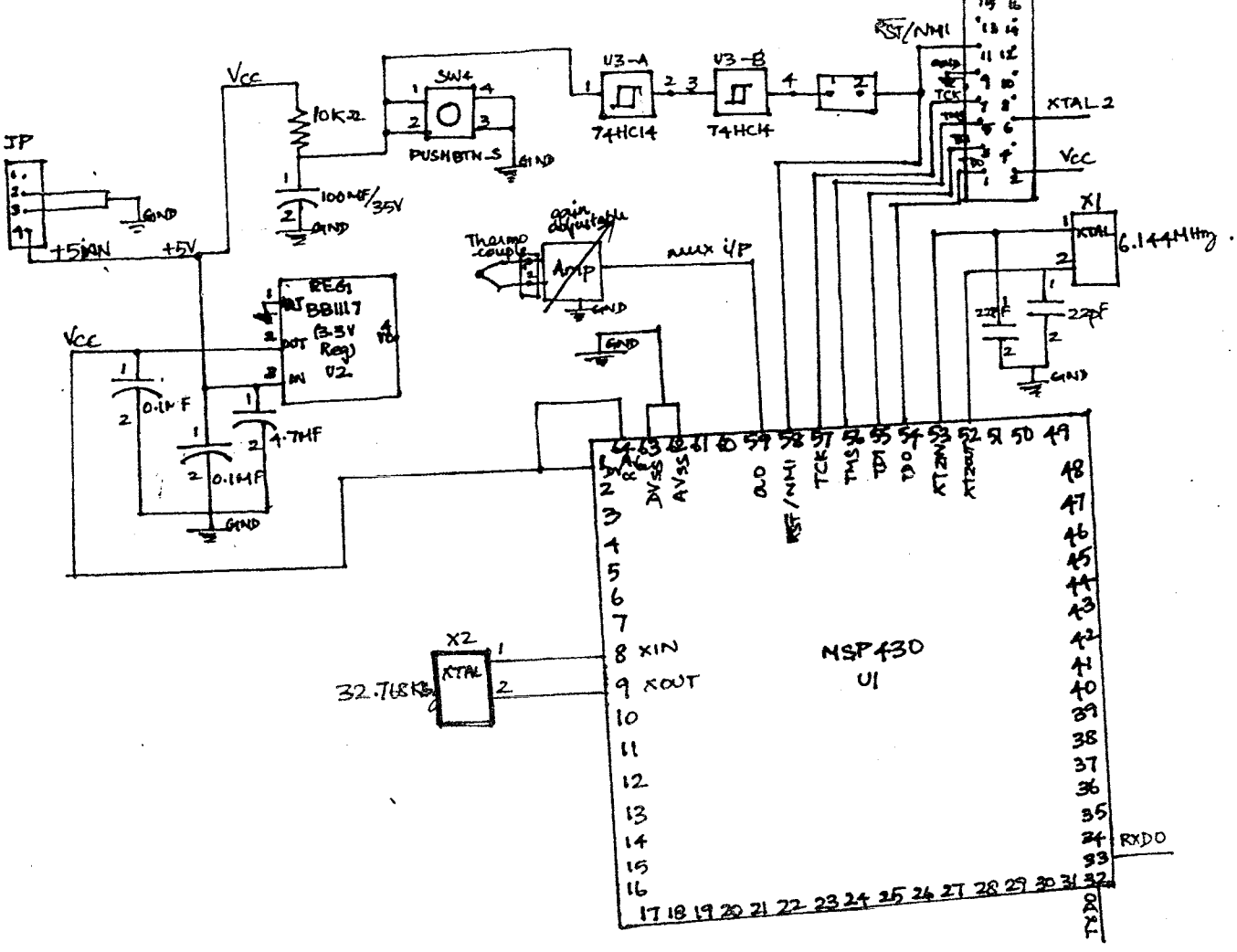
V_{o1} – OUTPUT OF INSTRUMENTATION AMPLIFIER

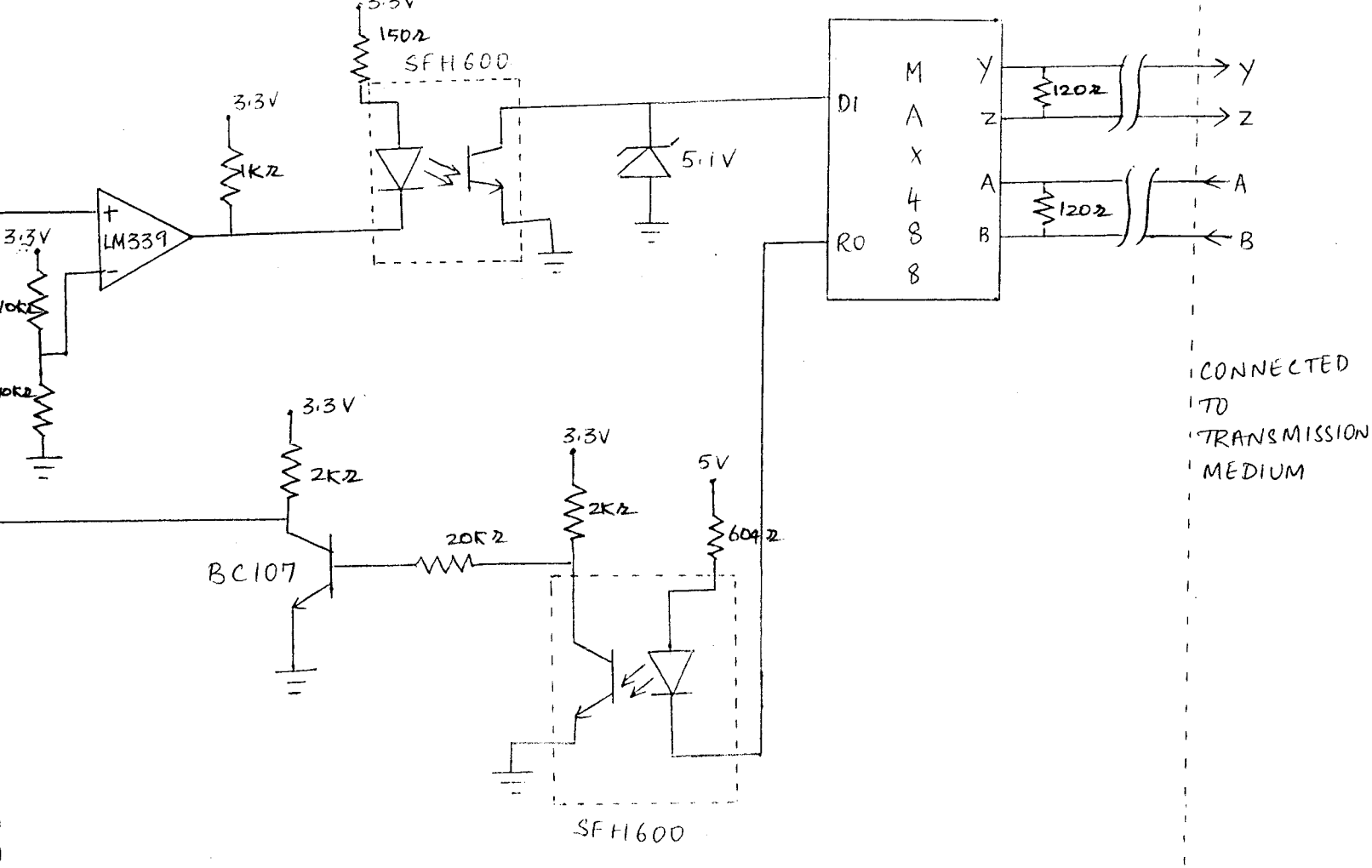
V_{o2} – OUTPUT OF LOW PASS FILTER

U1 - OP07C

SIGNAL CONDITIONING CIRCUITRY :

PROCESSING UNIT CIRCUITRY:

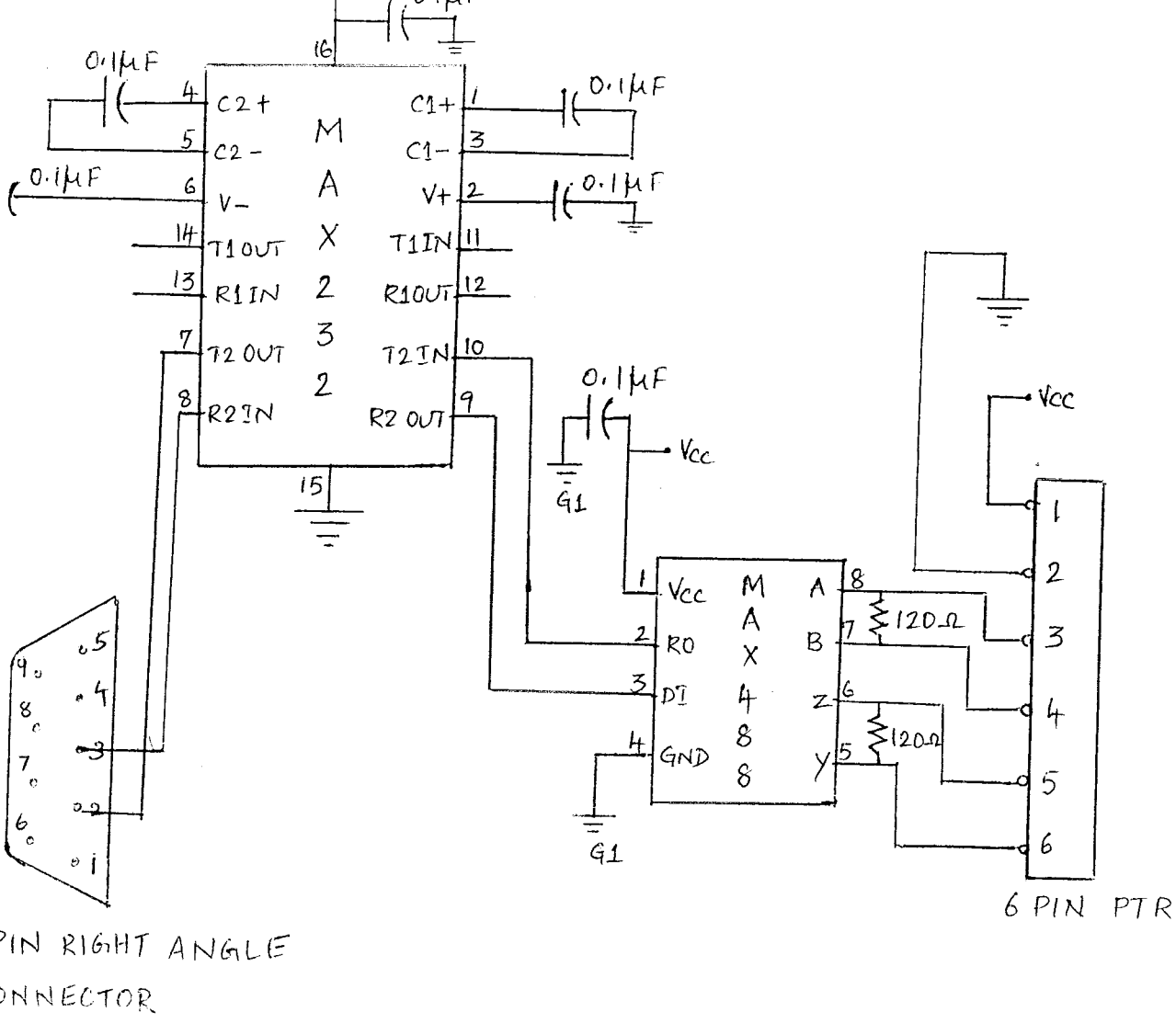




TO RS485 CONVERSION CIRCUITRY:

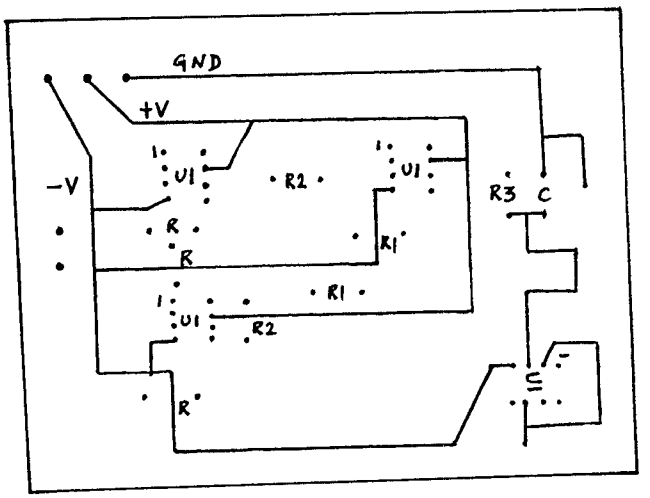
CONNECTED TO TRANSMISSION MEDIUM

RS485 TO RS232 CONVERSION CIRCUITRY :



PRINTED CIRCUIT BOARD FOR THE HAND ETCHED SIGNAL CONDITIONING UNIT:

SIDE 1



R = 2·2 KΩ

R1 = 150 KΩ

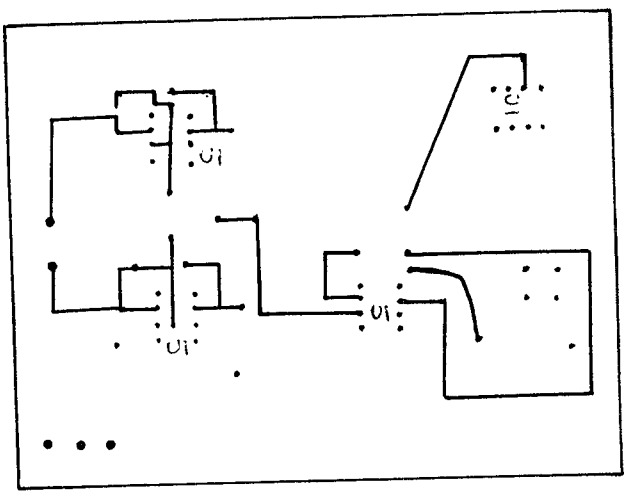
R2 = 3·3 KΩ

R3 = 100 KΩ

C = 0·1 μF

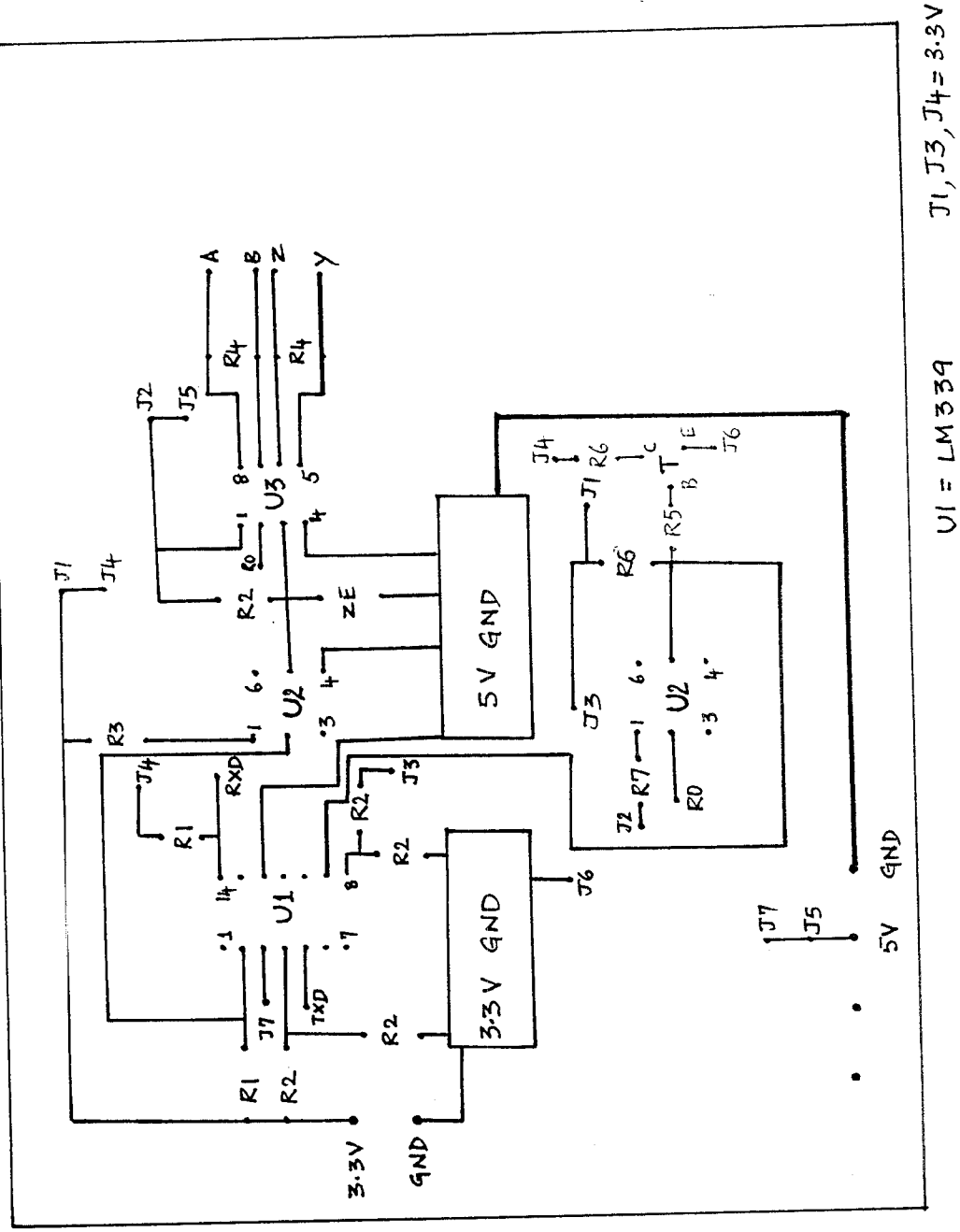
U1 = OP07 C

SIDE 2



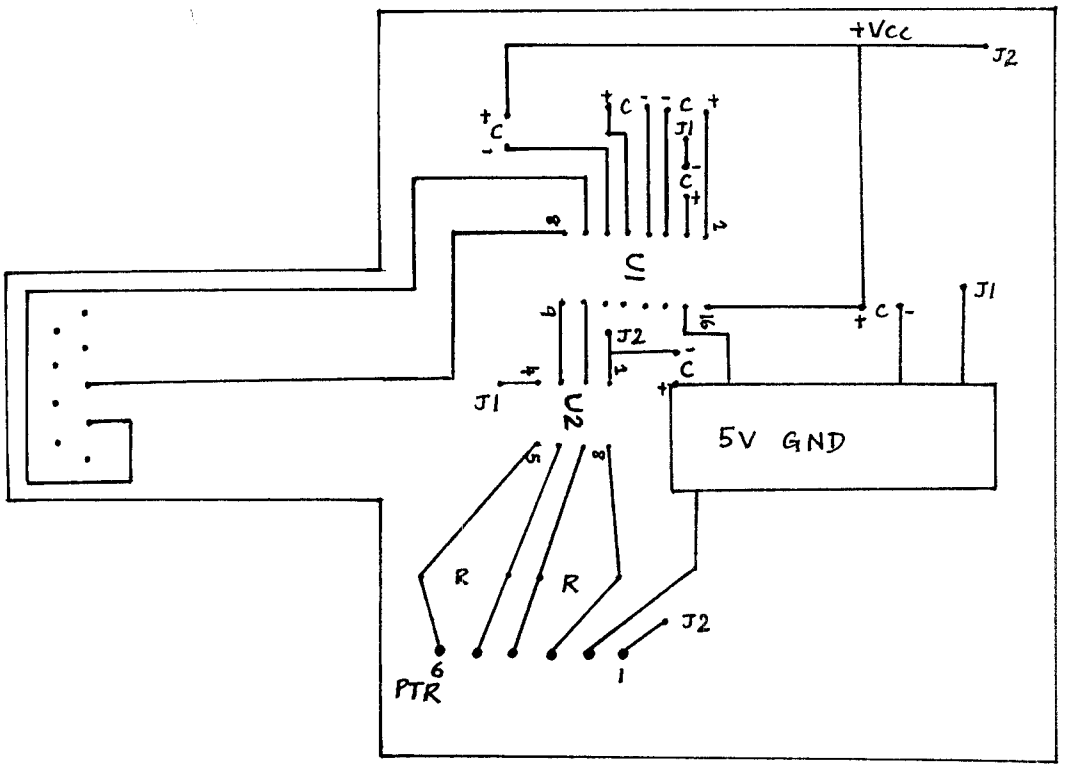
RINTED CIRCUIT BOARD FOR THE HAND ETCHED

TTL TO RS485 CONVERSION CIRCUITRY:



U1 = LM339
U2 = SFH600
U3 = MAX488
R1 = 1KΩ
R2 = 10KΩ
R3 = 150Ω
R4 = 120Ω
J1, J3, J4 = 3.3V
J6 = 3.3V GND
J2, J5, J7 = 5V
R5 = 20KΩ
R6 = 2KΩ
R7 = 604Ω
T = BC107

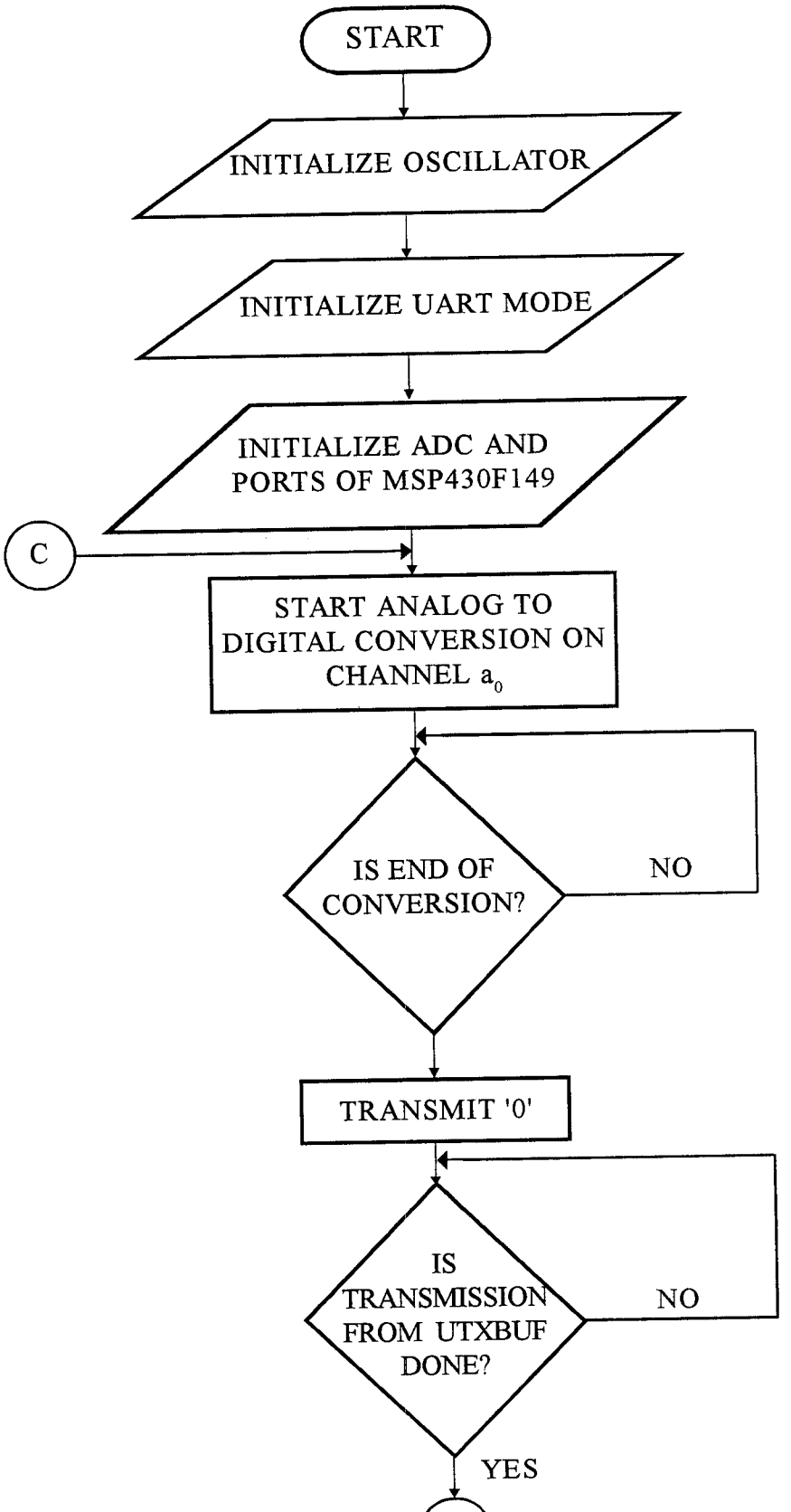
PRINTED CIRCUIT BOARD FOR THE HAND ETCHED RS485 TO RS232 CONVERSION CIRCUITRY :

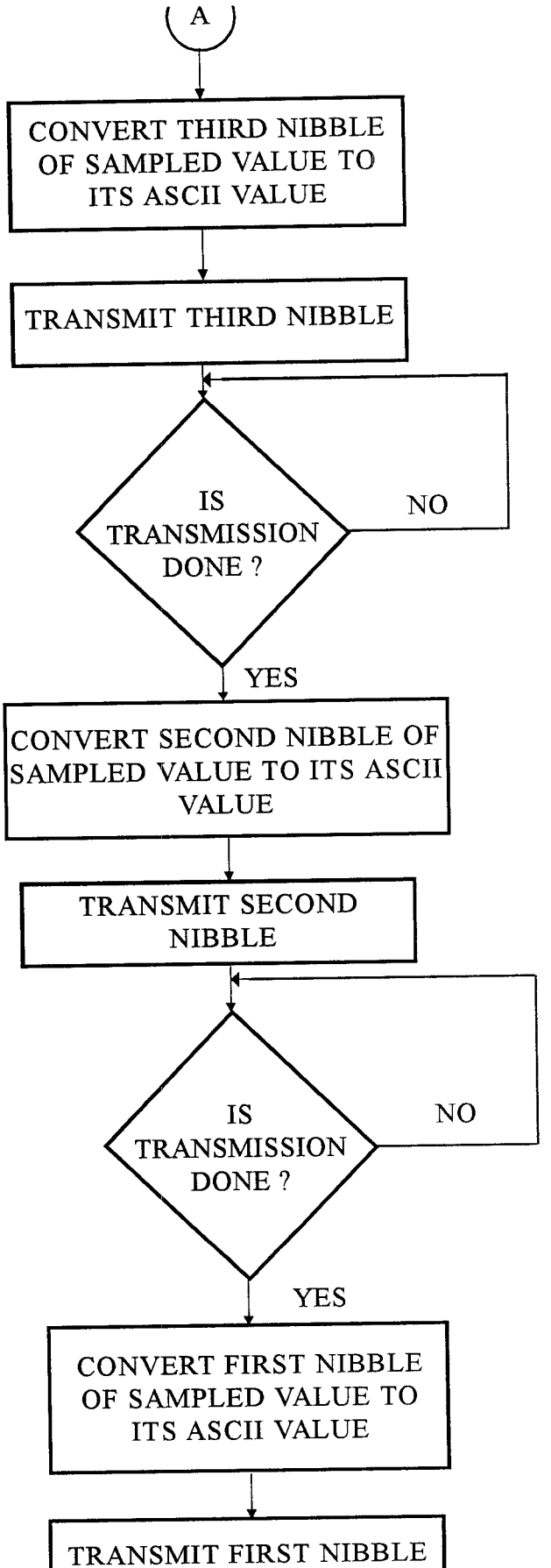


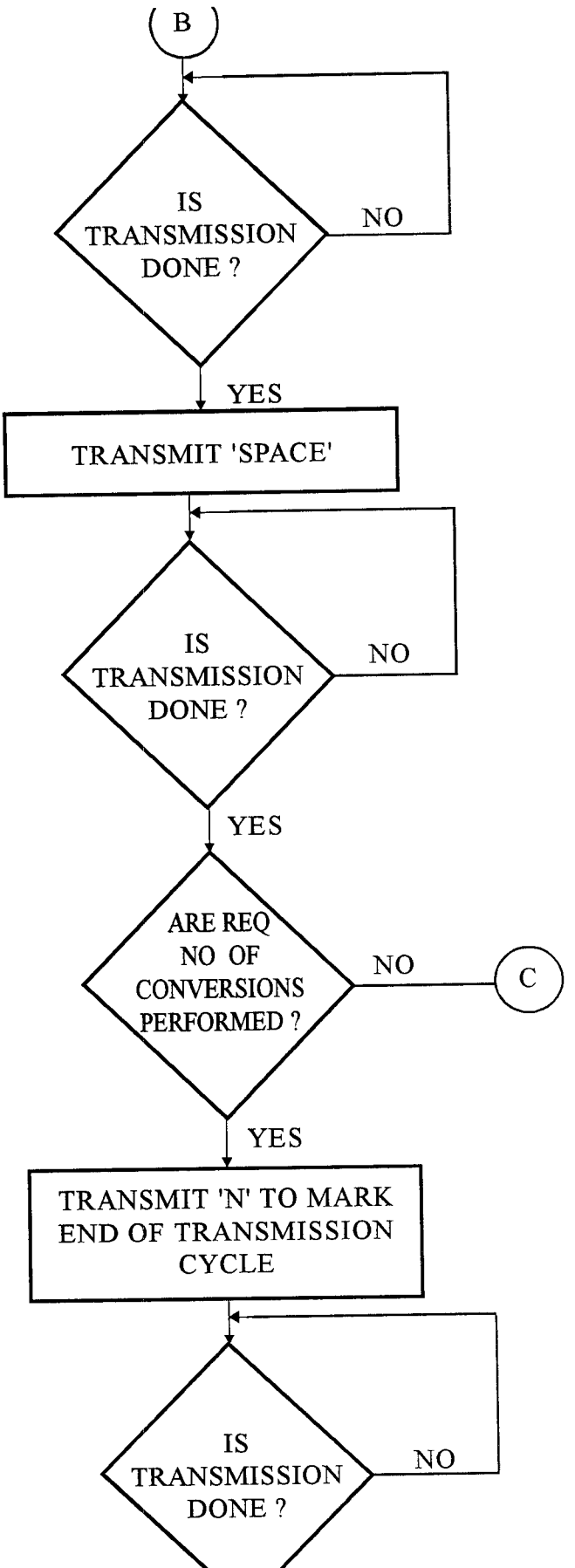
R = 120Ω
C = 0.1μF
U1 = MAX 232
U2 = MAX 488
J1 = 5V GND
J2 = +5V

Software

ASM FLOW CHART :




A
CONVERT THIRD NIBBLE OF SAMPLED VALUE TO ITS ASCII VALUE
TRANSMIT THIRD NIBBLE
IS TRANSMISSION DONE ?
NO
YES
CONVERT SECOND NIBBLE OF SAMPLED VALUE TO ITS ASCII VALUE
TRANSMIT SECOND NIBBLE
IS TRANSMISSION DONE ?
NO
YES
CONVERT FIRST NIBBLE OF SAMPLED VALUE TO ITS ASCII VALUE
TRANSMIT FIRST NIBBLE


B
IS TRANSMISSION DONE ?
NO
YES
TRANSMIT 'SPACE'
IS TRANSMISSION DONE ?
NO
YES
ARE REQ NO OF CONVERSIONS PERFORMED ?
NO
C
YES
TRANSMIT 'N' TO MARK END OF TRANSMISSION CYCLE
IS TRANSMISSION DONE ?
NO

ASM CODING:

```
# include       "msp430x14x.h"    // standard equations
;-------------------------------------------------------------------------------
                RSEG        CSTACK
                DS          0
;-------------------------------------------------------------------------------
NAME            ADC12_01
                RSEG        CODE
;-------------------------------------------------------------------------------
Setup           ; Set up modules
;-------------------------------------------------------------------------------
RESET           mov         #SFE(CSTACK), SP ; Initialize Stack pointer

StopWDT         mov         #WDTPW+WDTHOLD, &WDTCTL; Stop
                                                        Watchdog

SetupBC         bic.b       #XTOFF, &BCSCTL1; XT2 on

SetupOsc        bic.b       #OFIFG, &IFG1; Clear Osc fault flag
                mov.w       #0FFh, R15 ; R15 = delay

SetupOsc1       dec.w       R15 ; additional delay to ensure start
                jnz         SetupOsc1
                bit.b       #OFIFG, &IFG1 ; Osc fault flag set?
                jnz         SetupOsc ; Osc fault, clear flag again
                bis.b       #SELM1+SELS, BCSCTL2 ; MCLK = SMCLK =
                                                        XT2

SetupUART0      mov.b       #CHAR, &UCTL0 ; 8-bit characters
                mov.b       #SSEL1, &UTCTL0 ; UCLK = SMCLK
                mov.b       #000h, &UBR00 ; 6.144 Mhz / 2400 -2560
                mov.b       #00Ah, &UBR10;
                mov.b       #00h, &UMCTL0 ; No Modulation
                bis.b       #UTXE0+URXE0, &ME1 ; Enable USART0
                                                        TXD/RXD

SetupP3         bis.b       #010h,&P3SEL ; P3.4 = USART0 option select
                bic.b       #010h, &P3OUT ; Set transmission pin to low

SetupADC12      mov         #SHP+ADC12SSEL_1, &ADC12CTL1 ; use
                                                        sample timer, ADC core
```

```
                                        ; runs at ALCK, single channel
                mov.b   #00h, &ADC12MCTL0 ; end of sequence(EOS)
                                        ; = 0 is not required for single channel
                                        ; mode, Vref+ = AVcc, Vref- = Avss
                                        ; input channel A0.
                bis.b   #01h, &P6SEL ; set port 6.0 pin to ADC function

; NOTE : Loading of ADC12MCTL0 not actually required in this example since it
        powers up as all zeros just included here in remainder

                mov     #REFON+ADC12ON+ENC, & ADC12CTL0
                                ;Sample time x1, single sample

; NOTE: ADC12CTL0 set ENC last, since set ENC bit prevents some bits in
        ADC12CTL1, ADC12CTL0 & ADC12MCTLx from being changed.

                bis     #ENC, &ADC12CTL0 ; Set ENC bit
;-------------------------------------------------------------------------------
Main Loop       ;       Take ADC reading on channel 0
;-------------------------------------------------------------------------------
                mov     #01FEh, R15

testdelay       mov     #0FFFFh, R8

delay7a         dec     R8
                cmp     #0h, R8
                jnz     delay7a
                dec     R15
                cmp     #0h, R15
                jnz     testdelay

                mov     #504, R9

Loop            nop

                bis     #ADC12SC, &ADC12CTL0 ; Start A/D conversion

testEOC         bit     #BIT0, &ADC12IFG  ; End of convert?
                                          ; (ADC12IFG.0 = 1?)
                jz      testEOC  ; no, test again
                mov     &ADC12MEM0, R4  ; yes, result moved to R4, flag
                                          ; is automatically cleared

                mov.b   #48h, &TXBUF0  ; tx 0-Digit 3
```

```
txck        mov.b   #0FEh, R5  ; Tx check
            bic.b   &UTCTL0, R5
            cmp.b   #01h, R5
            jz      txck

            mov     #09C40h, R8  ; delay
delay1a     dec     R8
            cmp     #0h, R8
            jnz     delay1a

            mov     #09C40h, R8  ; delay
delay1b     dec     R8
            cmp     #0h, R8
            jnz     delay1b

            mov     #09C40h, R8  ; delay
delay1c     dec     R8
            cmp     #0h, R8
            jnz     delay1c

            mov     #09C40h, R8  ; delay
delay1d     dec     R8
            cmp     #0h, R8
            jnz     delay1d


            mov     #09C40h, R8  ; delay
delay1e     dec     R8
            cmp     #0h, R8
            jnz     delay1e

TX1         bit.b   #UTXIFG0, &IFG1  ; USART0 TX buffer ready?
            jz      TX1  ; Jump if TX buffer not ready.

            mov     R4, R5
            rra     R5  ; Transmit digit 2
            rra     R5
            rra     R5
            rra     R5
            rra     R5
            rra     R5
            rra     R5
```

```
                rra     R5

                bic.b   #0F0h, R5  ; hta2
                mov.b   #0Ah, R6
                cmp.b   R6, R5
                jge     hta22
                add     #48, R5
                mov.b   R5, &TXBUF0
                jmp     hta21

hta22           sub.b   #10, R5
                add.b   #65, R5
                mov.b   R5, &TXBUF0

hta21           nop

tx2             mov.b   #0FEh, R7     ; transmit check
                bic.b   &UTCTL0, R7
                cmp.b   #01h, R7
                jz      tx2

                mov     #09C40h, R8  ; delay
delay2a         dec     R8
                cmp     #0h, R8
                jnz     delay2a

                mov     #09C40h, R8  ; delay
delay2b         dec     R8
                cmp     #0h, R8
                jnz     delay2b

                mov     #09C40h, R8  ; delay
delay2c         dec     R8
                cmp     #0h, R8
                jnz     delay2c

                mov     #09C40h, R8  ; delay
delay2d         dec     R8
                cmp     #0h, R8
                jnz     delay2d


                mov     #09C40h, R8  ; delay
```

```
delay2e     dec     R8
            cmp     #0h, R8
            jnz     delay2e

TX2         bit.b   #UTXIFG0, &IFG1  ; USART0 TX buffer ready?
            jz      TX2  ; Jump if TX buffer not ready.

            mov     R4, R5
            rra     R5   ; transmit digit1
            rra     R5
            rra     R5
            rra     R5
            bic.b   #0F0h, R5  ; hta1
            mov.b   #0Ah, R6
            cmp.b   R6, R5
            jge     hta12
            add     #48, R5
            mov.b   R5, &TXBUF0
            jmp     hta11

hta12       sub.b   #10, R5
            add.b   #65, R5
            mov.b   R5, &TXBUF0

hta11       nop

tx1         mov.b   #0FEh, R7     ; transmit check
            bic.b   &UTCTL0, R7
            cmp.b   #01h, R7
            jz      tx1

            mov     #09C40h, R8  ; delay
delay3a     dec     R8
            cmp     #0h, R8
            jnz     delay3a

            mov     #09C40h, R8
delay3b     dec     R8
            cmp     #0h, R8
            jnz     delay3b

            mov     #09C40h, R8
delay3c     dec     R8
```

```
                cmp     #0h, R8
                jnz     delay3c

                mov     #09C40h, R8
delay3d         dec     R8
                cmp     #0h, R8
                jnz     delay3d

                mov     #09C40h, R8
delay3e         dec     R8
                cmp     #0h, R8
                jnz     delay3e

TX3             bit.b   #UTXIFG0, &IFG1 ; USART0 TX buffer ready?
                jz      TX3  ; Jump if TX buffer not ready.


                mov     R4, R5  ; transmit digit 0
                bic.b   #0F0h, R5  ; hta0
                mov.b   #0Ah, R6
                cmp.b   R6, R5
                jge     hta02
                add     #48, R5
                mov.b   R5, &TXBUF0
                jmp     hta01

hta02           sub.b   #10, R5
                add.b   #65, R5
                mov.b   R5, &TXBUF0

hta01           nop

tx0             mov.b   #0FEh, R7     ; transmit check
                bic.b   &UTCTL0, R7
                cmp.b   #01h, R7
                jz      tx0

                mov     #09C40h, R8  ; delay
delay4a         dec     R8
                cmp     #0h, R8
                jnz     delay4a

                mov     #09C40h, R8
```

```
delay4b     dec     R8
            cmp     #0h, R8
            jnz     delay4b

            mov     #09C40h, R8
delay4c     dec     R8
            cmp     #0h, R8
            jnz     delay4c

            mov     #09C40h, R8
delay4d     dec     R8
            cmp     #0h, R8
            jnz     delay4d

            mov     #09C40h, R8
delay4e     dec     R8
            cmp     #0h, R8
            jnz     delay4e

TX4         bit.b   #UTXIFG0, &IFG1  ; USART0 TX buffer ready?
            jz      TX4  ; Jump if TX buffer not ready.


            mov.b   #32, &TXBUF0  ; transmit space
txck2       mov.b   #0FEh, R5
            bic.b   &UTCTL0, R5
            cmp.b   #01h, R5
            jz      txck2

            mov     #09C40h, R8  ; delay
delay5a     dec     R8
            cmp     #0h, R8
            jnz     delay5a

            mov     #09C40h, R8
delay5b     dec     R8
            cmp     #0h, R8
            jnz     delay5b

            mov     #09C40h, R8
delay5c     dec     R8
            cmp     #0h, R8
            jnz     delay5c
```

```
                mov     #09C40h, R8
delay5d         dec     R8
                cmp     #0h, R8
                jnz     delay5d

                mov     #09C40h, R8
delay5e         dec     R8
                cmp     #0h, R8
                jnz     delay5e

TX5             bit.b   #UTXIFG0, &IFG1  ; USART0 TX buffer ready?
                jz      TX5  ; Jump if TX buffer not ready.


                dec     R9
                cmp     #0, R9
                jnz     Loop

                mov.b   #78, &TXBUF0  ; transmit  N for end
txck3           mov.b   #0FEh, R5
                bic.b   &UTCTL0, R5
                cmp.b   #01h, R5
                jz      txck3


                mov     #09C40h, R8  ; delay
delay6a         dec     R8
                cmp     #0h, R8
                jnz     delay6a

                mov     #09C40h, R8
delay6b         dec     R8
                cmp     #0h, R8
                jnz     delay6b

                mov     #09C40h, R8
delay6c         dec     R8
                cmp     #0h, R8
                jnz     delay6c

                mov     #09C40h, R8
delay6d         dec     R8
```

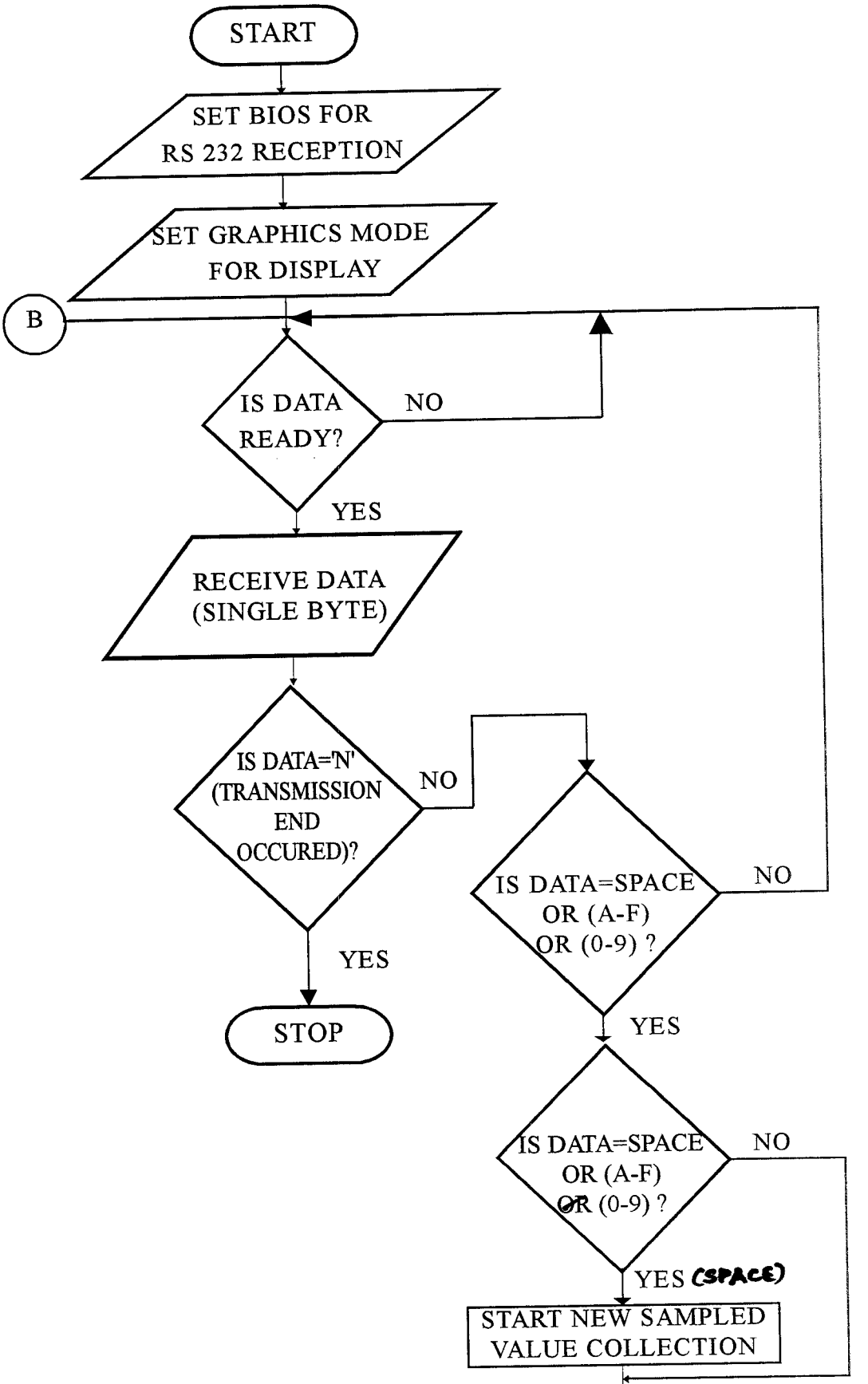
```
                cmp     #0h, R8
                jnz     delay6d

                mov     #09C40h, R8
delay6e         dec     R8
                cmp     #0h, R8
                jnz     delay6e

TX6             bit.b   #UTXIFG0, &IFG1  ; USART0 TX buffer ready?
                jz      TX6  ; Jump if TX buffer not ready.

hlt1            jmp     hlt1
                jmp     Main Loop      ; Loop again
;-------------------------------------------------------------------------------
                COMMON  INTVEC  ; Interrupt Vectors
;-------------------------------------------------------------------------------
                ORG     RESET_VECTOR
                DW      RESET
;-------------------------------------------------------------------------------
                END
```

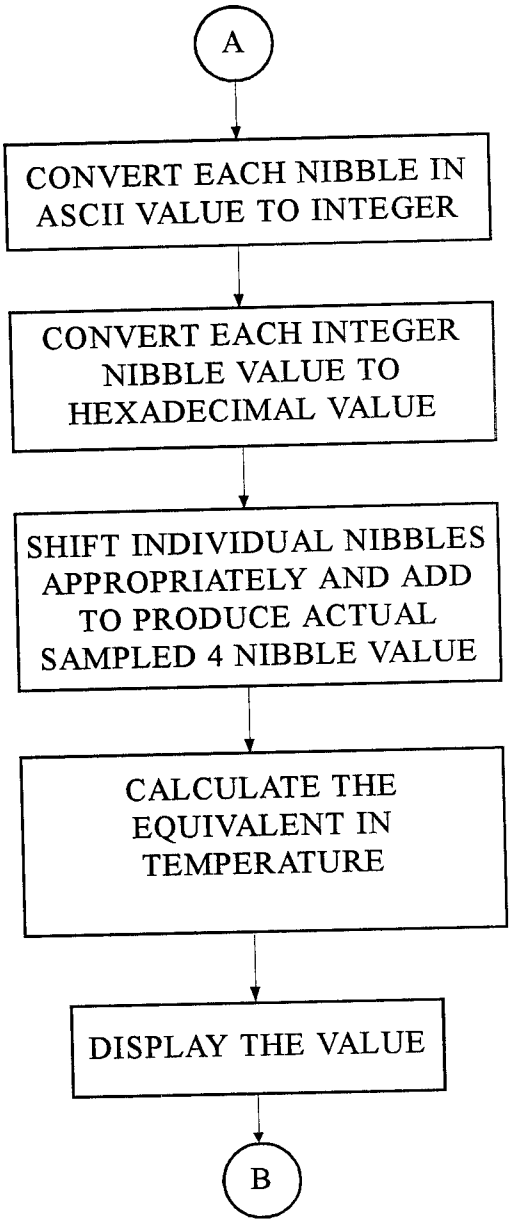
C PLUS PLUS (C++):

C++ has been chosen as the programming language for profile generation at the Personal Computer end, due to its capability to the access of the hardware through software and data encapsulation. C plus plus can be used to program the Personal Computer to receive data by serial communication in the RS232 standard. Graphics is used to display the profile in this project.

The coding in C++ for this project has been provided on the next page.

C PLUS PLUS FLOW CHART FOR PROFILE GENERATION:




A
CONVERT EACH NIBBLE IN ASCII VALUE TO INTEGER
CONVERT EACH INTEGER NIBBLE VALUE TO HEXADECIMAL VALUE
SHIFT INDIVIDUAL NIBBLES APPROPRIATELY AND ADD TO PRODUCE ACTUAL SAMPLED 4 NIBBLE VALUE
CALCULATE THE EQUIVALENT IN TEMPERATURE
DISPLAY THE VALUE
B

CPP CODING:

```
# include<stdio.h>
# include<conio.h>
# include<bios.h>
# include<dos.h>
# include<graphics.h>
# include<stdlib.h>

# define COM1 0
# define DATA_READY 0x100
# define SETTINGS (0xA0|0x03|0x00|0x18)
# define YELLOW 14

static int xx = 55;
FILE *fp;

void disp(int result)
{
        double mulfac, temp;
        int yyy, yy;
        mulfac = 5.0 / 4095.0;
        mulfac / = 150.0;
        mulfac = (mulfac / 40.0) * 1000000.0;
        temp = (mulfac*result) + 25;
        yyy = 1.3 * (temp +18.0);
        yy = 417 – yyy;

                if (xx = = 55)
                        moveto(55, 417);
                if (xx = = 559)
                        xx = 55;
         lineto(xx, yy);
         xx + = 1;
}

static int count = 0;
static int temp = 0;

void convinttohex (int x, int y, int z, int w)
{
         int x1, y1, z1,w1, result;
```

```
        if (x>9)
                x1 = 0xA + (x-10);
        else
                x1 = 0x0 + x;

        if (y>9)
                y1 = 0xA + (y-10);
        else
                y1 = 0x0 + y;

        if (z>9)
                z1 = 0xA + (z-10);
        else
                z1 = 0x0 + z;

        if (w>9)
                w1 = 0xA + (w-10);
        else
                w1 = 0x0 + w;

z1 = z1<<4;
y1 = y1<<8;
x1 = x1<<12;
result = x1 + y1 + z1 + w1;

switch(count)
        {
                case 0:
                        temp = result;
                        count++;
                        break;
                case 1:
                        temp += result;
                        count++;
                        break;
                case 2:
                        temp += result;
                        count++;
                        break;
                case 3:
                        temp += result;
                        count++;
                        break;
                case 4:
```

```
                temp += result;
                count++;
                break;
        case 5:
                temp += result;
                count++;
                break;
        case 6:
                temp += result;
                count++;
                break;
        case 7:
                temp += result;
                count++;
                break;
        case 8:
                temp += result;
                count++;
                break;
        case 9:
                temp += result;
                count++;
                break;
        case 10:
                temp += result;
                count++;
                break;
        case 11:
                temp += result;
                count++;
                break;
        case 12:
                temp += result;
                count++;
                break;
        case 13:
                temp += result;
                temp/=14;
                count = 0;
                disp(temp);
                break;
        default:
                ;
}
```

```
}

int convatoint (int p)
{
        int retval;

                if ((p<65) && (p>=48))
                        retval = p-48;
                else
                        retval = 10+p-65;
        return retval;
}

static int jj = 0, aa, bb, cc, dd;
static int flag;
static int no;

void send (unsigned in)
{
        if ((in = = 32) && (jj = = 0))
                {
                        flag = 1;
                        jj =1;
                }

        if ((in = = 32) && (jj! = 0))
                {
                        flag = 1;
                        jj = 1;
                }

        if (( in! = 32) && (flag = = 1))
                {
                        switch (jj)
                                {
                                        case 1:
                                        aa = convatoint (in);
                                        jj ++;
                                        putc (in, fp);
                                        break;

                                        case 2:
                                        bb = convatoint (in);
                                        jj ++;
```

```
                                        putc (in, fp);
                                        break;

                                        case 3:
                                        cc = convatoint (in);
                                        putc (in,fp);
                                        jj ++;
                                        break;

                                        case 4:
                                        dd = convatoint (in);
                                        jj = 0;
                                        putc (in, fp);
                                        unsigned iin;
                                        iin = 32;
                                        putc (iin, fp);
                                        flag = 0;
                                        no ++;
                                        convinttohex (aa, bb, cc, dd);
                                        break;

                                        default:
                                        ;
                                }
                        }
}

int main (void)
{
        int gdriver = DETECT, gmode, errorcode;
        int x, y;
        initgraph (&driver, &gmode, "");
        errorcode = graphresult();
                if errorcode != grok)
                        {
                                printf("Graphics error ! %s\n",grapherrormsg(errorcode));
                                printf("Press any key to halt:");
                                getch();
                                exit(1);
                        }

 setcolor(CYAN);
 outtextxy(242, 15, "PROFILE GENERATION");
 setcolor(getmaxcolor());
```

```
ine(55, 40, 55, 417); // y-axis left
outtextxy(30, 37, "272"); // loc of 272°
outtextxy(30, 414, "-18"); // loc of -18°
outtextxy(30, 288, "79"); // loc of 79°
setcolor(LIGHT GREEN);
outtextxy(30, 196, "150"); // loc of 150°
setcolor(WHITE);
outtextxy(30, 162, "176"); // loc of 176°
setcolor(LIGHT BLUE);
outtextxy(30, 154, "182"); // loc of 182°
setcolor(LIGHT RED);
outtextxy(30, 118, "210"); // loc of 210°
setcolor(CYAN);
outtextxy(15, 395, "Deg C"); // loc of Deg C
outtextxy(525, 430, "Time"); // loc of Time
setcolor(WHITE);
line(55, 417, 559, 417); // x bottom
line(55, 40, 559, 40); // x top
line(559, 40, 559, 417); // y right
line(87, 419, 87, 427); // t1
outtextxy(89, 420, "00:00 m");
line(182, 419, 182, 427); // t2
outtextxy(184, 420, "01:00 m");
line(276, 419, 276, 427); // t3
outtextxy(278, 420, "02:00 m");
line(370, 419, 370, 427); // t4
outtextxy(372, 420, "03:00 m");
line(465, 419, 465, 427); // t5
outtextxy(467, 420, "04:00 m");
setcolor(LIGHT RED);
line(87, 413, 163, 413); // Heating Zone 1
line(87, 411, 163, 411); // Heating Zone 1
outtextxy(95, 401, "Heating 1");
setcolor(LIGHT BLUE);
line(163, 413, 239, 413); // Heating Zone 2
line(163, 411, 239, 411); // Heating Zone 2
outtextxy(171, 401, "Heating 2");
setcolor(LIGHT GREEN);
line(239, 413, 315, 413); // Heating Zone 3
line(239, 411, 315, 411); // Heating Zone 3
outtextxy(247, 401, "Heating 3");
setcolor(LIGHT GRAY);
line(315, 413, 334, 413); // Leer
line(315, 411, 334, 411); // Leer
```

```
outtextxy(311, 401, "Leer");
line(315, 398, 334, 398); // Leer
setcolor(LIGHT MAGENTA);
line(334, 413, 410, 413); // Peak
line(334, 411, 410, 411); // Peak
outtextxy(360, 401, "Peak");
setcolor(BROWN);
line(410, 413, 559, 413); // Cooling
line(410, 411, 559, 411); // Cooling
outtextxy(455, 401, "Cooling");
setcolor(WHITE);
setlinestyle(USERBIT_LINE, 1, 1);
line(55, 291, 559, 291); // Horizontal
setcolor(LIGHT GREEN);
line(55, 199, 559, 199); // Horizontal
setcolor(WHITE);
line(55, 165, 559, 165); // Horizontal
setcolor(LIGHT BLUE);
line(55, 157, 559, 157); // Horizontal
setcolor(LIGHT RED);
line(55, 121, 559, 121); // Horizontal
setcolor(WHITE);
line(87, 40, 87, 417); // Vertical
line(163, 40, 163, 417); // Vertical
line(239, 40, 239, 417); // Vertical
line(315, 40, 315, 417); // Vertical
line(334, 40, 334, 417); // Vertical
line(410, 40, 410, 417); // Vertical
setlinestyle(SOLID_LINE, 0, 1); // End of graph formatting

setcolor(YELLOW);

int l = 30;
unsigned in, out, status;
_bios_serialcom(0, COM1, SETTINGS);
sleep(5);
cprintf("_BIOS_SERIALCOM [ESC] to exit \r\n");
fp = fopen("prjadc.txt","w+");

        while(l)
                {
                        status = _bios_serialcom(3, COM1, 0);

                                if (status & DATA_READY)
```

```
                    if ((out = _bios_serialcom(2, COM1, 0) & 0x7F)!=0)
                            {

                                    if ((out!='N') && ((out!=' ') || (out!='A') ||
                            (out!='B') || (out!='C') || (out!='D') || (out!='E') ||
                            (out!='F') || (out!='0') || (out!='1') || (out!='2') ||
                            (out!='3') || (out!='4') || (out!='5') || (out!='6') ||
                            (out!='7') || (out!='8') || (out!='9') || (out!='a') ||
                            (out!='b') || (out!='c') || (out!='d') || (out!='e') ||
                            (out!='f')))
                                            {
                                                    send (out);
                                            }
                                    else
                                            if (out = = 'N')
                                                    break;
                             }
            }
fclose(fp);
getchar();
return 0;
}
```

Future development

FUTURE DEVELOPMENT:

This project could be further developed into an advanced system by

1. Providing numerous user inputs at the Reflow Soldering System end for better performance.
2. Multiple machines could be connected to the same Personal Computer to monitor various activities simultaneously.

Conclusion

CONCLUSION:

The project replaces the void left for the profile generation for the Reflow Soldering System and the monitoring of the temperature within the test cabins, at Premier Polytronics Pvt. Ltd.

The project could be further developed into a stand-alone system, which would benefit the industry, in general.

References

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1. 'Temperature Measurement in Engineering' by H Dean Baker Ryder.
2. 'Fundamentals of Temperature Flow & Pressure Measurement' by Roder P. Benedic.
3. 'Operational Amplifiers & Linear IC's' by Coughlin Fredrick.
4. 'Transducers & instrumentation' by D V S Murthy.
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12. slau049.pdf for MSP430F149.

Appendix

OP07C

VERY LOW OFFSET SINGLE BIPOLAR OPERATIONAL AMPLIFIER

- EXTREMELY LOW OFFSET : 150µV/ max.
- LOW INPUT BIAS CURRENT : 1.8nA
- LOW V_{io} DRIFT : 0.5µV/°C
- ULTRA STABLE WITH TIME : 2µV/month max.
- WIDE SUPPLY VOLTAGE RANGE : ±3V to ±22V

N
DIP8
(Plastic Package)

DESCRIPTION

The OP07 is a very high precision op amp with an offset voltage maximum of 150µV.

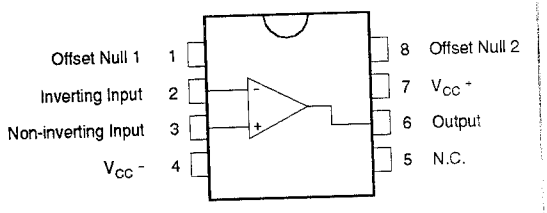
Offering also low input current (1.8nA) and high gain (400V/mV), the OP07C is particularly suitable for instrumentation applications.

ORDER CODE

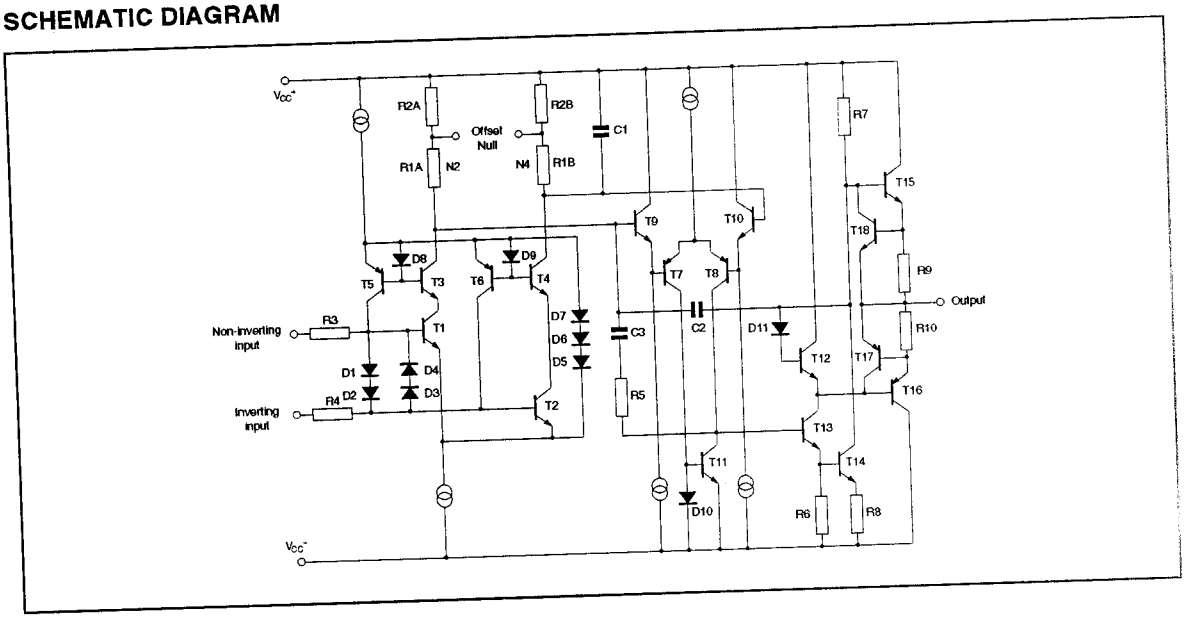
Part Number	Temperature Range	Package
		N
OP07C	-40°C, +105°C	•

N = Dual in Line Package (DIP)

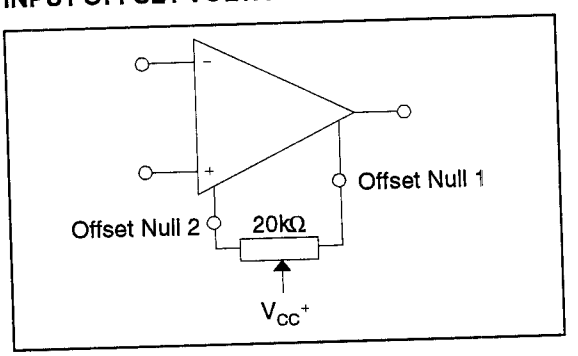
PIN CONNECTIONS (top view)



SCHEMATIC DIAGRAM



INPUT OFFSET VOLTAGE NULLING CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	±22	V
V_{id}	Differential Input Voltage	±30	V
V_i	Input Voltage	±22	V
T_{oper}	Operating Temperature	-40 to +105	°C
T_{stg}	Storage Temperature	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

V_{CC} = ±15V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage 0°C ≤ T_{amb} ≤ +105°C		60	150 250	µV
	Long Term Input Offset - Voltage Stability - note [1]		0.4	2	µV/Mo
DV_{io}	Input Offset Voltage Drift		0.5	1.8	µV/°C
I_{io}	Input Offset Current (V_{ic} = 0V) 0°C ≤ T_{amb} ≤ +105°C		0.8	6 7	nA
DI_{io}	Input Offset Current Drift		15	50	pA/°C
DI_{ib}	Input Bias Current Drift		15	50	pA/°C
R_o	Open Loop Output Resistance		60		Ω
R_{id}	Differential Input Resistance		33		MΩ
R_{ic}	Common Mode Input Resistance		120		GΩ
V_{icm}	Input Common Mode Voltage Range 0°C ≤ T_{amb} ≤ +105°C	±13 ±13	±13.5		V
CMR	Common-mode Rejection Ratio (V_{ic} = $V_{icm\ min.}$) 0°C ≤ T_{amb} ≤ +105°C	100 97	120		dB
SVR	Supply Voltage Rejection Ratio (V_{CC} = ±3 to ±18V) 0°C ≤ T_{amb} ≤ +105°C	90 86	104		dB
A_{vd}	Large Signal Voltage Gain V_{CC} = ±15, R_L = 2kΩ, V_O = ±10V 0°C ≤ T_{amb} ≤ +105°C V_{CC} = ±3, R_L = 500Ω, V_O = ±0.5V	120 100 100	400 400		V/mV
V_{opp}	Output Voltage Swing R_L = 10kΩ R_L = 2kΩ R_L = 1kΩ 0°C ≤ T_{amb} ≤ +105°C R_L = 2kΩ	±12 ±11.5 ±11	±13 ±12.8 ±12		V
SR	Slew Rate (R_L = 2kΩ, C_L = 100pF)		0.17		V/µs
GBP	Gain Bandwidth Product (R_L = 2kΩ, C_L = 100pF, f = 100kHz)		0.5		MHz
I_{CC}	Supply Current - no load 0°C ≤ T_{amb} ≤ +105°C V_{CC} = ±3V		2.7 0.67	5 6 1.3	mA
e_n	Equivalent Input Noise Voltage f = 10kHz f = 100Hz f = 1kHz		11 10.5 10	20 13.5 11.5	$\frac{nV}{\sqrt{Hz}}$
i_n	Equivalent Input Noise Current f = 10kHz f = 100Hz f = 1kHz		0.3 0.2 0.1	0.9 0.3 0.2	$\frac{pA}{\sqrt{Hz}}$

1. Long term input offset voltage stability refers to the average trend line of Vio vs time over extended periods after the first 30 days of operation.

MSP430x13x, MSP430x14x
MIXED SIGNAL MICROCONTROLLER

SLAS272C – JULY 2000 – REVISED FEBRUARY 2001

- Low Supply-Voltage Range, 1.8 V . . . 3.6 V
- Ultralow-Power Consumption:
  - Standby Mode: 1.6 μA
  - RAM Retention Off Mode: 0.1 μA
- Low Operating Current:
  - 2.5 μA at 4 kHz, 2.2 V
  - 280 μA at 1 MHz, 2.2 V
- Five Power-Saving Modes
- Wake-Up From Standby Mode in 6 μs
- 16-Bit RISC Architecture, 125-ns Instruction Cycle Time
- 12-Bit A/D Converter With Internal Reference, Sample-and-Hold and Autoscan Feature
- 16-Bit Timer With Seven Capture/Compare-With-Shadow Registers, Timer_B
- 16-Bit Timer With Three Capture/Compare Registers, Timer_A
- On-Chip Comparator
- Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse
- Family Members Include:
  - MSP430F133: 8KB+256B Flash Memory, 256B RAM
  - MSP430F135: 16KB+256B Flash Memory, 512B RAM
  - MSP430F147: 32KB+256B Flash Memory, 1KB RAM
  - MSP430F148: 48KB+256B Flash Memory, 2KB RAM
  - MSP430F149: 60KB+256B Flash Memory, 2KB RAM
- Available in 64-Pin Quad Flat Pack (QFP)

description

The Texas Instruments MSP430 series is an ultralow-power microcontroller family consisting of several devices featuring different sets of modules targeted to various applications. The microcontroller is designed to be battery operated for use in extended-time applications. The MSP430 achieves maximum code efficiency with its 16-bit RISC architecture, 16-bit CPU-integrated registers, and a constant generator. The digitally-controlled oscillator provides wake-up from low-power mode to active mode in less than 6 μs. The MSP430x13x and the MSP430x14x series are microcontroller configurations with two built-in 16-bit timers, a fast 12-bit A/D converter, one or two universal serial synchronous/asynchronous communication interfaces (USART), and 48 I/O pins.

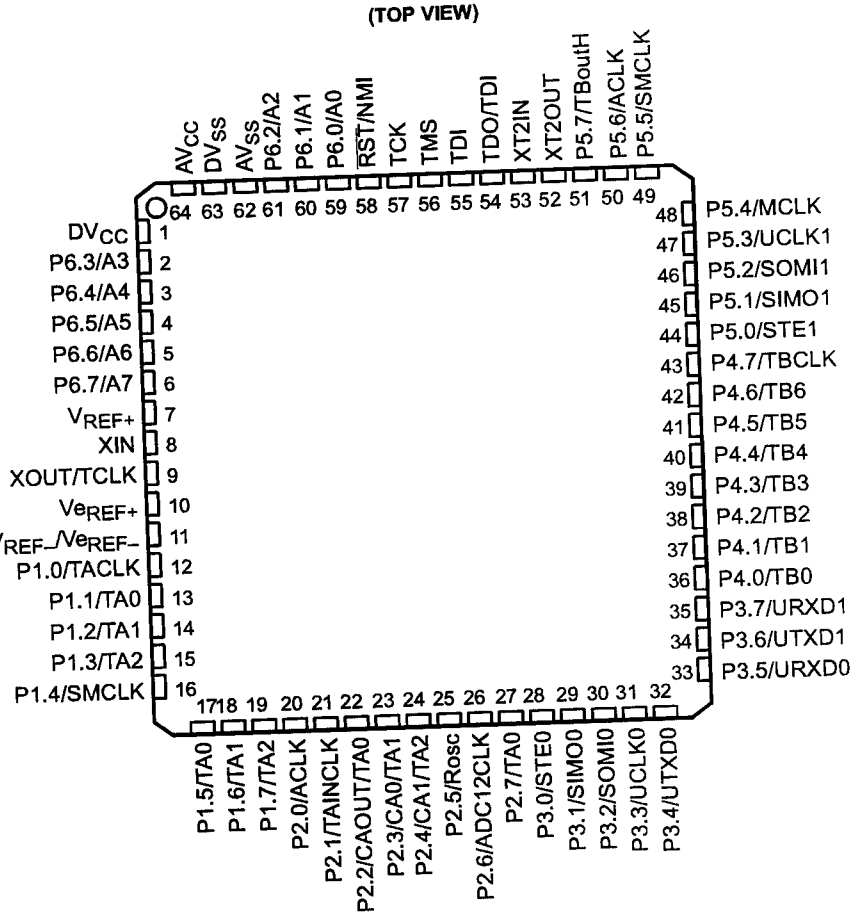
Typical applications include sensor systems that capture analog signals, convert them to digital values, and process and transmit the data to a host system. The timers make the configurations ideal for industrial control applications such as ripple counters, digital motor control, EE-meters, hand-held meters, etc. The hardware multiplier enhances the performance and offers a broad code and hardware-compatible family solution.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	PLASTIC 64-PIN QFP (PM)
–40°C to 85°C	MSP430F133IPM MSP430F135IPM MSP430F147IPM MSP430F148IPM MSP430F149IPM

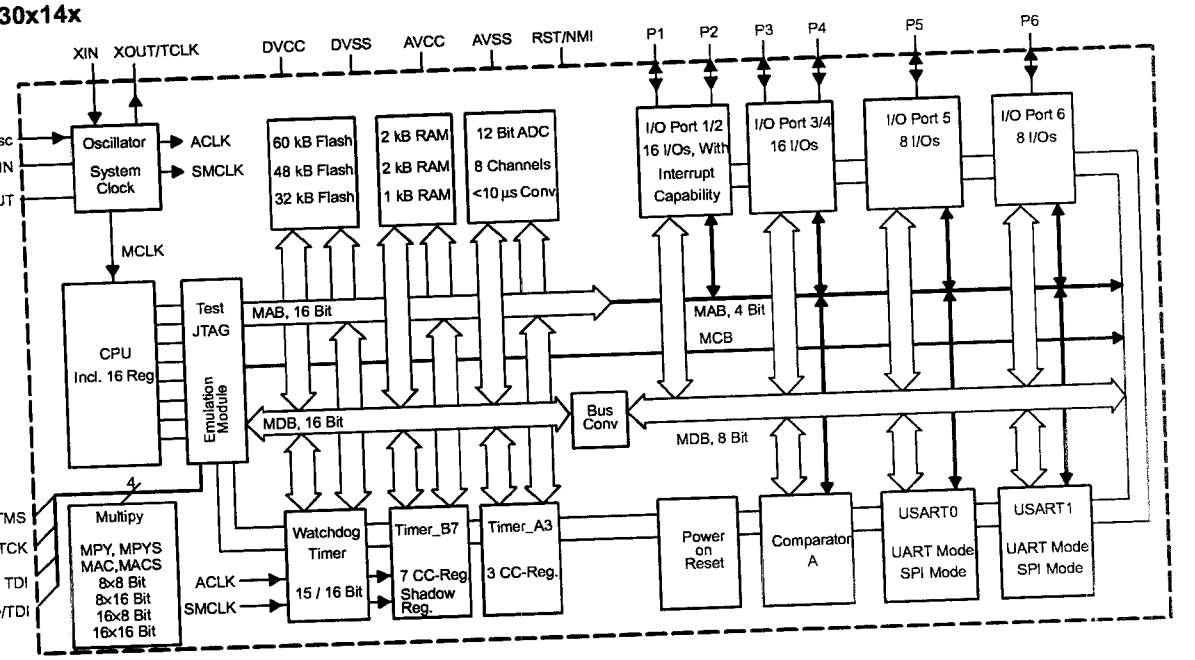
in designation, MSP430F147, MSP430F148, MSP430F149

PM PACKAGE
(TOP VIEW)

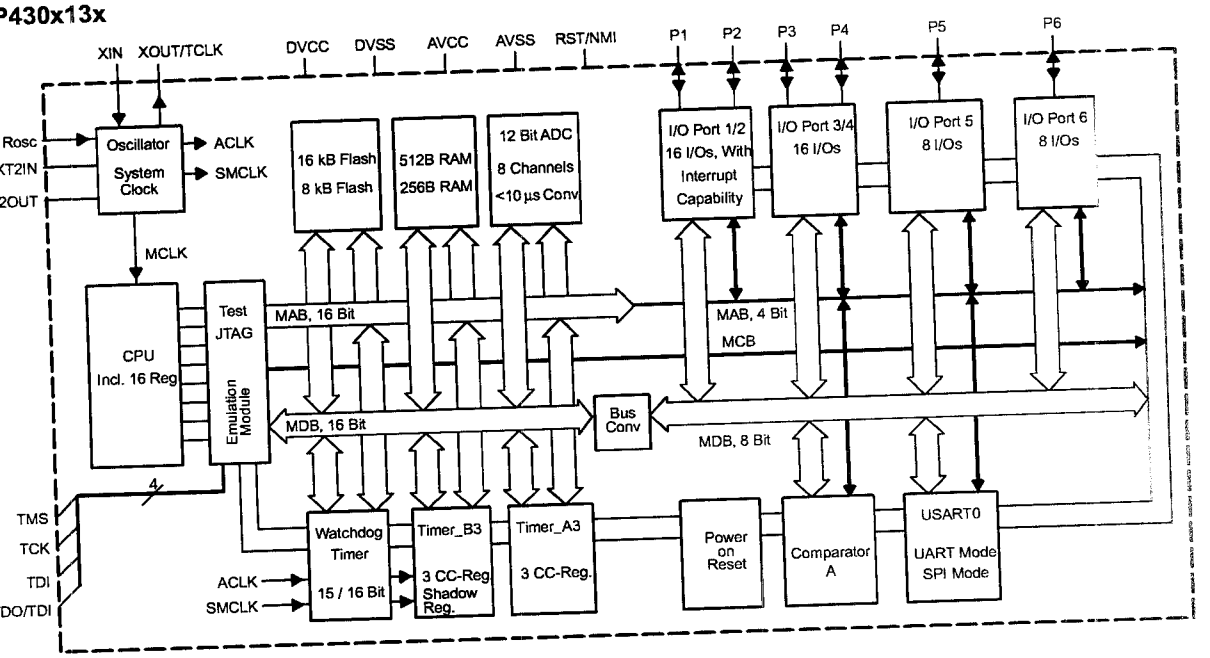


onal block diagrams

30x14x



P430x13x



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AV_{CC}	64		Analog supply voltage, positive terminal. Supplies only the analog portion of the analog-to-digital converter.
AV_{SS}	62		Analog supply voltage, negative terminal. Supplies only the analog portion of the analog-to-digital converter.
DV_{CC}	1		Digital supply voltage, positive terminal. Supplies all digital parts.
DV_{SS}	63		Digital supply voltage, negative terminal. Supplies all digital parts.
P1.0/TACLK	12	I/O	General digital I/O pin/Timer_A, clock signal TACLK input
P1.1/TA0	13	I/O	General digital I/O pin/Timer_A, capture: CCI0A input, compare: Out0 output
P1.2/TA1	14	I/O	General digital I/O pin/Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/TA2	15	I/O	General digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK	16	I/O	General digital I/O pin/SMCLK signal output
P1.5/TA0	17	I/O	General digital I/O pin/Timer_A, compare: Out0 output
P1.6/TA1	18	I/O	General digital I/O pin/Timer_A, compare: Out1 output
P1.7/TA2	19	I/O	General digital I/O pin/Timer_A, compare: Out2 output/
P2.0/ACLK	20	I/O	General digital I/O pin/ACLK output
P2.1/TAINCLK	21	I/O	General digital I/O pin/Timer_A, clock signal at INCLK
P2.2/CAOUT/TA0	22	I/O	General digital I/O pin/Timer_A, capture: CCI0B input/Comparator_A output
P2.3/CA0/TA1	23	I/O	General digital I/O pin/Timer_A, compare: Out1 output/Comparator_A input
P2.4/CA1/TA2	24	I/O	General digital I/O pin/Timer_A, compare: Out2 output/Comparator_A input
P2.5/Rosc	25	I/O	General-purpose digital I/O pin, input for external resistor defining the DCO nominal frequency
P2.6/ADC12CLK	26	I/O	General digital I/O pin, conversion clock – 12-bit ADC
P2.7/TA0	27	I/O	General digital I/O pin/Timer_A, compare: Out0 output
P3.0/STE0	28	I/O	General digital I/O, slave transmit enable – USART0/SPI mode
P3.1/SIMO0	29	I/O	General digital I/O, slave in/master out of USART0/SPI mode
P3.2/SOMI0	30	I/O	General digital I/O, slave out/master in of USART0/SPI mode
P3.3/UCLK0	31	I/O	General digital I/O, external clock input – USART0/UART or SPI mode, clock output – USART0/SPI mode
P3.4/UTXD0	32	I/O	General digital I/O, transmit data out – USART0/UART mode
P3.5/URXD0	33	I/O	General digital I/O, receive data in – USART0/UART mode
P3.6/UTXD1†	34	I/O	General digital I/O, transmit data out – USART1/UART mode
P3.7/URXD1†	35	I/O	General digital I/O, receive data in – USART1/UART mode
P4.0/TB0	36	I/O	General-purpose digital I/O, capture I/P or PWM output port – Timer_B7 CCR0
P4.1/TB1	37	I/O	General-purpose digital I/O, capture I/P or PWM output port – Timer_B7 CCR1
P4.2/TB2	38	I/O	General-purpose digital I/O, capture I/P or PWM output port – Timer_B7 CCR2
P4.3/TB3†	39	I/O	General-purpose digital I/O, capture I/P or PWM output port – Timer_B7 CCR3
P4.4/TB4†	40	I/O	General-purpose digital I/O, capture I/P or PWM output port – Timer_B7 CCR4
P4.5/TB5†	41	I/O	General-purpose digital I/O, capture I/P or PWM output port – Timer_B7 CCR5
P4.6/TB6†	42	I/O	General-purpose digital I/O, capture I/P or PWM output port – Timer_B7 CCR6
P4.7/TBCLK	43	I/O	General-purpose digital I/O, input clock TBCLK – Timer_B7
P5.0/STE1†	44	I/O	General-purpose digital I/O, slave transmit enable – USART1/SPI mode
P5.1/SIMO1†	45	I/O	General-purpose digital I/O slave in/master out of USART1/SPI mode
P5.2/SOMI1†	46	I/O	General-purpose digital I/O, slave out/master in of USART1/SPI mode
P5.3/UCLK1†	47	I/O	General-purpose digital I/O, external clock input – USART1/UART or SPI mode, clock output – USART1/SPI mode
P5.4/MCLK	48	I/O	General-purpose digital I/O, main system clock MCLK output
P5.5/SMCLK	49	I/O	General-purpose digital I/O, submain system clock SMCLK output

† 14x devices only

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ACLK	50	I/O	General-purpose digital I/O, auxiliary clock ACLK output
TboutH	51	I/O	General-purpose digital I/O, switch all PWM digital output ports to high impedance – Timer_B7 TB0 to TB6
A0	59	I/O	General digital I/O, analog input a0 – 12-bit ADC
A1	60	I/O	General digital I/O, analog input a1 – 12-bit ADC
A2	61	I/O	General digital I/O, analog input a2 – 12-bit ADC
A3	2	I/O	General digital I/O, analog input a3 – 12-bit ADC
A4	3	I/O	General digital I/O, analog input a4 – 12-bit ADC
A5	4	I/O	General digital I/O, analog input a5 – 12-bit ADC
A6	5	I/O	General digital I/O, analog input a6 – 12-bit ADC
A7	6	I/O	General digital I/O, analog input a7 – 12-bit ADC
NMI	58	I	Reset input, nonmaskable interrupt input port, or bootstrap loader start (in Flash devices).
	57	I	Test clock. TCK is the clock input port for device programming test and bootstrap loader start (in Flash devices).
	55	I	Test data input. TDI is used as a data input port. The device protection fuse is connected to TDI.
/TDI	54	I/O	Test data output port. TDO/TDI data output or programming data input terminal
S	56	I	Test mode select. TMS is used as an input port for device programming and test.
REF+	10	I/P	Input for an external reference voltage to the ADC
EF+	7	O	Output of positive terminal of the reference voltage in the ADC
EF–/VeREF–	11	O	Negative terminal for the ADC's reference voltage for both sources, the internal reference voltage, or an external applied reference voltage
	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
UT/TCLK	9	I/O	Output terminal of crystal oscillator XT1 or test clock input
2IN	53	I	Input port for crystal oscillator XT2. Only standard crystals can be connected.
2OUT	52	O	Output terminal of crystal oscillator XT2

ort-form description

ocessing unit

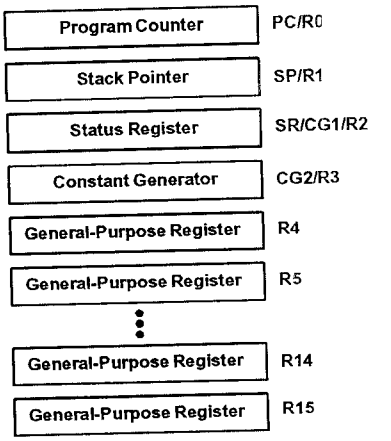
The processing unit is based on a consistent and orthogonal CPU and instruction set. This design structure results in a RISC-like architecture, highly transparent to the application development and notable for its ease of programming. All operations other than program-flow instructions are consequently performed as register operations in conjunction with seven addressing modes for source and four modes for destination operand.

PU

The CPU has sixteen registers that provide reduced instruction execution time. This reduces the register-to-register operation execution time to one cycle of the processor frequency.

Four of the registers are reserved for special use as program counter, stack pointer, status register, and constant generator. The remaining registers are available as general-purpose registers.

Peripherals are connected to the CPU using a data address and control bus, and can be easily handled with all memory manipulation instructions.



hort-form description (continued)

struction set

The instruction set for this register-to-register architecture constitutes a powerful and easy-to-use assembler language. The instruction set consists of 51 instructions with three formats and seven address modes. Table 1 provides a summary and example of the three types of instruction formats; the address modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g. ADD R4,R5	R4 + R5 —> R5
Single operands, destination only	e.g. CALL R8	PC —>(TOS), R8—> PC
Relative jump, un/conditional	e.g. JNE	Jump-on-equal bit = 0

Each instruction operating on word and byte data is identified by the suffix B.

Examples:	WORD INSTRUCTIONS		BYTE INSTRUCTIONS	
	MOV	EDE, TONI	MOV.B	EDE,TONI
	ADD	#235h,&MEM	ADD.B	#35h,&MEM
	PUSH	R5	PUSH.B	R5
	SWPB	R5	—	

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 —> R11
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)—> M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) —> M(TONI)
Absolute	✓	✓	MOV &MEM,&TCDAT		M(MEM) —> M(TCDAT)
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) —> M(Tab+R6)
Indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) —> R11 R10 + 2—> R10
Immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 —> M(TONI)

NOTE: S = source D = destination

Computed branches (BR) and subroutine call (CALL) instructions use the same address modes as other instructions. These address modes provide *indirect* addressing, which is ideally suited for computed branches and calls. The full use of this programming capability results in a program structure which is different from structures used with conventional 8- and 16-bit controllers. For example, numerous routines can be easily designed to deal with pointers and stacks instead of using flag-type programs for flow control.

operating modes and interrupts

The MSP430 operating modes provide advanced support of the requirements for ultralow-power and ultralow-energy consumption. This goal is achieved by intelligent management during the different operating modes of modules and CPU states and is fully supported during interrupt event handling. An interrupt event awakes the system from each of the various operating modes and returns, using the *RETI* instruction, to the mode that was selected before the interrupt event occurred. The different requirements on CPU and modules—driven by system cost and current consumption objectives—require the use of different clock signals:

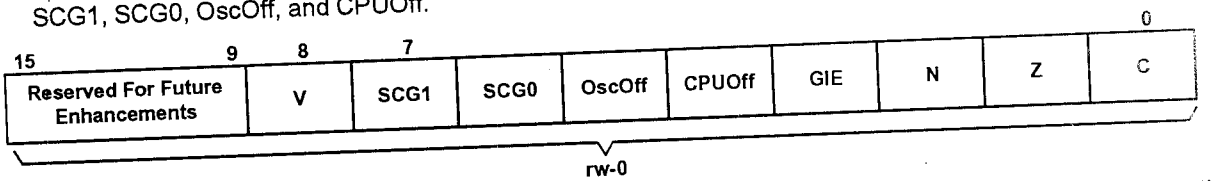
- Auxiliary clock ACLK, sourced by LFXT1CLK (crystal frequency) and used by the peripheral modules
- Main system clock MCLK, used by the CPU and system
- Subsystem clock SMCLK, used by the peripheral modules

w-power consumption capabilities

The various operating modes are handled by software by controlling the operation of the internal clock system. This clock system provides a large combination of hardware and software capabilities to run the application while maintaining the lowest power consumption and optimizing system costs. This is accomplished by:

- Use of the internal clock (DCO) generator without any external components
- Selection of an external crystal or ceramic resonator for lowest frequency and cost
- Selection and activation of the proper clock signals (LFXT1CLK, XT2Off, and/or DCOCLK) and clock predivider function. Control bit XT2Off is embedded in control register BCSCTL1.
- Application of an external clock source

The control bits that most influence the operation of the clock system and support fast turnon from low power operating modes are located in the status register SR. Four bits control the CPU and the system clock generator: SCG1, SCG0, OscOff, and CPUOff.



CPUOff, SCG1, SCG0, and OscOff are the most important bits in low-power control when the basic function of the system clock generator is established. They are pushed to the stack whenever an interrupt is accepted and saved for returning to the operation before an interrupt request. They can be manipulated via indirect access to the data on the stack during execution of an interrupt handler so that program execution can resume in another power operating mode after return-from-interrupt.

CPUOff: Clock signal MCLK, used with the CPU, is active when the CPUOff bit is reset or stopped when set.

SCG1: Clock signal SMCLK, used with peripherals, is enabled when the SCG1 bit is reset or stopped when set.

OscOff: Crystal oscillator LFXT1 is active when the OscOff bit is reset. The LFXT1 oscillator can be inactive only when the OscOff bit is set and it is not used for MCLK. The setup time to start a crystal oscillation requires special consideration when the off option is used. Mask-programmable devices can disable this feature and the oscillator can never be switched off by software.

SCG0: The dc generator is active when the SCG0 bit is reset. The DCO can be inactive only if the SCG0 bit is set and the DCOCLK signal is not used as MCLK or SMCLK. The dc current consumed by the dc generator defines the basic frequency of the DCOCLK.

When the current is switched off (SCG0=1) the start of the DCOCLK is slightly delayed. This delay is in the microsecond range.

DCOCLK: Clock signal DCOCLK is stopped if not used as MCLK or SMCLK. There are two situations when the SCG0 bit can not switch the DCOCLK signal off:

The DCOCLK frequency is used as MCLK (CPUOff=0 and SELM.1=0), or the DCOCLK frequency is used as SMCLK (SCG1=0 and SELS=0).

If DCOCLK is required for operation, the SCG0 bit can not switch the dc generator off.

ıpt vector addresses

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh – 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

NTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External Reset Watchdog Flash memory	WDTIFG KEYV (see Note 1)	Reset	0FFFEh	15, highest
NMI Oscillator Fault sh memory access violation	NMIIFG (see Notes 1 & 4) OFIFG (see Notes 1 & 4) ACCVIFG (see Notes 1 & 4)	(Non)maskable (Non)maskable (Non)maskable	0FFFCh	14
Timer_B7 (see Note 5)	BCCIFG0 (see Note 2)	Maskable	0FFFAh	13
Timer_B7 (see Note 5)	BCCIFG1 to BCCIFG6 TBIFG (see Notes 1 & 2)	Maskable	0FFF8h	12
Comparator_A	CAIFG	Maskable	0FFF6h	11
Watchdog timer	WDTIFG	Maskable	0FFF4h	10
USART0 receive	URXIFG0	Maskable	0FFF2h	9
USART0 transmit	UTXIFG0	Maskable	0FFF0h	8
ADC	ADCIFG (see Notes 1 & 2)	Maskable	0FFEEh	7
Timer_A3	CCIFG0 (see Note 2)	Maskable	0FFECh	6
Timer_A3	CCIFG1, CCIFG2, TAIFG (see Notes 1 & 2)	Maskable	0FFEAh	5
I/O port P1 (eight flags)	P1IFG.0 (see Notes 1 & 2) To P1IFG.7 (see Notes 1 & 2)	Maskable	0FFE8h	4
USART1 receive	URXIFG1	Maskable	0FFE6h	3
USART1 transmit	UTXIFG1		0FFE4h	2
I/O port P2 (eight flags)	P2IFG.0 (see Notes 1 & 2) To P2IFG.7 (see Notes 1 & 2)	Maskable	0FFE2h	1
			0FFE0h	0, lowest

TES: 1. Multiple source flags
2. Interrupt flags are located in the module.
3. Nonmaskable: neither the individual nor the general interrupt-enable bit will disable an interrupt event.
4. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable can not disable it.
5. Timer_B7 in MSP430x14x family has 7 CCRs; Timer_B3 in MSP430x13x family has 3 CCRs; in Timer_B3 there are only interrupt flags CCIFG0, 1, and 2, and the interrupt-enable bits CCIE0, 1, and 2 integrated.

ecial function registers

Most interrupt and module-enable bits are collected in the lowest address space. Special-function register bits not allocated to a functional purpose are not physically present in the device. This arrangement provides simple software access.

le enable registers 1 and 2

dress

7	6	5	4	3	2	1	0
UTXE0	URXE0 USPIE0						
rw-0	rw-0						

URXE0: USART0, UART receive enable

UTXE0: USART0, UART transmit enable

USPIE0: USART0, SPI (synchronous peripheral interface) transmit and receive enable

ddress
h

7	6	5	4	3	2	1	0
		UTXE1	URXE1 USPIE1				
		rw-0	rw-0				

URXE1: USART1, UART receive enable

UTXE1: USART1, UART transmit enable

USPIE1: USART1, SPI (synchronous peripheral interface) transmit and receive enable

gend: rw: Bit Can Be Read and Written
rw-0: Bit Can Be Read and Written. It Is Reset by PUC.
SFR Bit Not Present in Device

mory organization

		MSP430F133	MSP430F135	MSP430F147	MSP430F148	MSP430F149
mory n: interrupt vector n: code memory	Size Flash Flash	8kB 0FFFFh – 0FFE0h 0FFFFh – 0E000h	16kB 0FFFFh – 0FFE0h 0FFFFh – 0C000h	32kB 0FFFFh – 0FFE0h 0FFFFh – 08000h	48kB 0FFFFh – 0FFE0h 0FFFFh – 04000h	60kB 0FFFFh – 0FFE0h 0FFFFh – 01100h
ormation memory	Size Flash	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h
ot memory	Size ROM	1kB 0FFFh – 0C00h	1kB 0FFFh – 0C00h	1kB 0FFFh – 0C00h	1kB 0FFFh – 0C00h	1kB 0FFFh – 0C00h
AM	Size	256 Byte 02FFh – 0200h	512 Byte 03FFh – 0200h	1kB 05FFh – 0200h	2kB 09FFh – 0200h	2kB 09FFh – 0200h
ripherals	16-bit 8-bit 8-bit SFR	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h

oot ROM containing bootstrap loader

The intention of the bootstrap loader is to download data into the flash memory module. Various write, read, and erase operations are needed for a proper download environment. The bootstrap loader is only available on F devices.

nctions of the bootstrap loader:

Definition of read: Apply and transmit data of peripheral registers or memory to pin P1.1 (BSLTX)
write: Read data from pin P2.2 (BSLRX) and write them into flash memory

nprotected functions

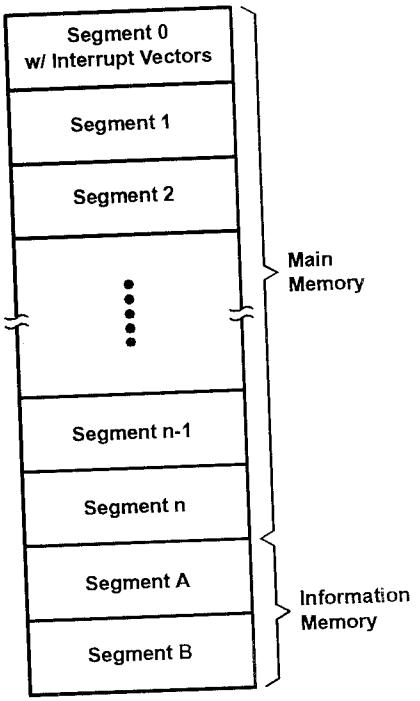
Mass erase, erase of the main memory (segment 0 to segment n) and information memory (segment A and segment B)
Access to the MSP430 via the bootstrap loader is protected. It must be enabled before any protected function can be performed. The 256 bits in 0FFE0h to 0FFFFh provide the access key.

ash memory

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0–n.
  Segments A and B are also called *information memory.*
- A security fuse burning is irreversible; no further access to JTAG is possible afterwards
- Internal generation of the programming/erase voltage: no external V_{PP} has to be applied, but V_{CC} increases the supply current requirements.
- Program and erase timing is controlled by hardware in the flash memory – no software intervention is needed.
- The control hardware is called the flash-timing generator. The input frequency of the flash–timing generator should be in the proper range and should be maintained until the write/program or erase operation is completed.
- During program or erase, no code can be executed from flash memory and all interrupts must be disabled by setting the GIE, NMIIE, ACCVIE, and OFIE bits to zero. If a user program requires execution concurrent with a flash program or erase operation, the program must be executed from memory other than the flash memory (e.g., boot ROM, RAM). In the event a flash program or erase operation is initiated while the program counter is pointing to the flash memory, the CPU will execute JMP $ instructions until the flash program or erase operation is completed. Normal execution of the previously running software then resumes.
- Unprogrammed, new devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to first use.

memory (continued)

8 kB	16 kB	32 kB	48 kB	60 kB
0FFFFh	0FFFFh	0FFFFh	0FFFFh	0FFFFh
0FE00h 0FDFFh	0FE00h 0FDFFh	0FE00h 0FDFFh	0FE00h 0FDFFh	0FE00h 0FDFFh
0FC00h 0FBFFh	0FC00h 0FBFFh	0FC00h 0FBFFh	0FC00h 0FBFFh	0FC00h 0FBFFh
0FA00h 0F9FFh	0FA00h 0F9FFh	0FA00h 0F9FFh	0FA00h 0F9FFh	0FA00h 0F9FFh
0E400h 0E3FFh	0C400h 0C3FFh	08400h 083FFh	04400h 043FFh	01400h 013FFh
0E200h 0E1FFh	0C200h 0C1FFh	08200h 081FFh	04200h 041FFh	01200h 011FFh
0E000h 010FFh	0C000h 010FFh	08000h 010FFh	04000h 010FFh	01100h 010FFh
01080h 0107Fh	01080h 0107Fh	01080h 0107Fh	01080h 0107Fh	01080h 0107Fh
01000h	01000h	01000h	01000h	01000h

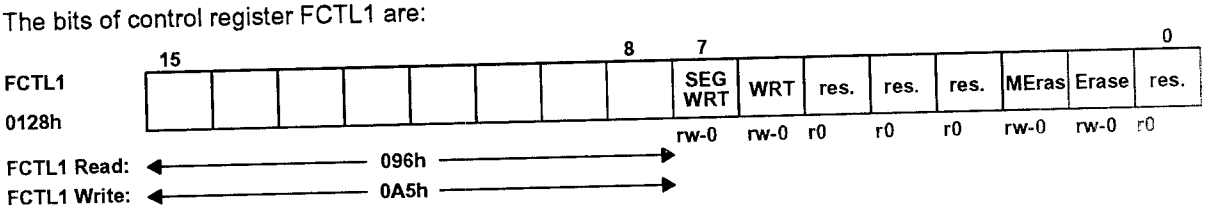


lash memory, control register FCTL1

All control bits are reset during PUC. PUC is active after application of V_{CC}, application of a reset condition to the RST/NMI pin, expiration of the Watchdog Timer, occurrence of a watchdog access violation, or execution of an improper flash operation. A more detailed description of the control-bit functions is found in the flash-memory module description (in the MSP430x1xx user's guide, literature number SLAU049). Any write to control register FCTL1 during erase, mass erase, or write (programming) will end in an access violation with ACCVIFG=1. In an active segment-write mode the control register can be written if the wait mode is active (WAIT=1). Special conditions apply during segment-write mode. See the MSP430x1xx user's guide for details.

Read access is possible at any time without restrictions.

The bits of control register FCTL1 are:



Erase 0128h, bit1 Erase a segment

0: No segment erase will be started.

1: Erase of one segment is enabled. The segment to be erased is defined by a *dummy* write into any address within the segment. The erase bit is automatically reset when the erase operation is completed. See Note 8.

MEras 0128h, bit2 Mass erase, Segment0 to Segmentn are erased together.

0: No erase will be started

1: Erase of Segment0 to Segmentn is enabled. A dummy write to any address in Segment0 to Segmentn starts mass erase. The MEras bit is automatically reset when the erase operation is completed. See Note 8.

WRT 0128h, bit6 Bit WRT should be set for a successful write operation.

An access violation occurs and ACCVIFG is set if bit WRT is reset and write access to the flash memory is performed. See Note 8.

SEGWRT 0128h, bit7 Bit SEGWRT may be used to reduce total programming time.

Segment-write bit SEGWRT is useful when larger sequences of data have to be programmed. After completion of programming of one segment, a reset and set sequence has to be performed to enable access to the next segment. The WAIT bit must be high before executing the next write instruction.

0: No segment write accelerate is selected.

1: Segment write is used. This bit needs to be reset and set between segment borders.

NOTE 8: Only instruction-fetch access is allowed during program, erase, or mass-erase cycles. Any other access to the flash memory during these cycles will result in setting the ACCVIFG bit. An NMI interrupt should handle such violations.

memory, control register FCTL1 (continued)

Table 3. Valid Combinations of Control Bits for Flash Memory Access (see Note 9)

FUNCTION PERFORMED	SEGWRT	WRT	MERAS	ERASE	BUSY	WAIT	LOCK
word or byte	0	1	0	0	0	0	0
word or byte in same segment, segment write mode	1	1	0	0	0	1	0
e one segment by writing to any address in the target segment	0	0	0	1	0	0	0
e all segments (0 to n) but not the information memory (segments A 3)	0	0	1	0	0	0	0
e all segments (0 to n, and A and B) by writing to any address in ash memory module	0	0	1	1	0	0	0

E 9: The table shows all possible combinations of control bits SEGWRT, WRT, MEras, Erase, and BUSY. All other combinations will result in an access violation.

h memory, timing generator, control register FCTL2

The timing generator (Figure 1) produces all the timing signals necessary for write, erase, and mass erase (see NOTE below) from the selected clock source. One of three different clock sources may be selected by control bits SSEL0 and SSEL1 in control register FCTL2. The selected clock source should be divided to meet the frequency requirements specified in the recommended operating conditions.

NOTE:

The mass erase duration generated by the flash timing generator is at least 11.1 ms. The cummulative mass erase time needed is 200 ms. This can be achieved by repeating the mass erase operation until the cumulative mass erase time is met (a minimum of 19 cycles may be required).

The flash-timing generator is reset with PUC. It is also reset if the emergency exit bit EMEX is set. Control register FCTL2 may not be written to if the BUSY bit is set; otherwise, an access violation will occur (ACCVIFG=1).

Read access is possible at any time without restrictions.

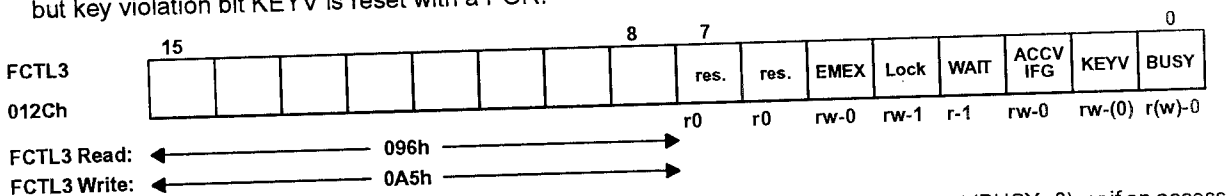
	15							8	7							0
FCTL2									SSEL1	SSEL0	FN5	FN4	FN3	FN2	FN1	FN0
012Ah									rw-0	rw-1	rw-0	rw-0	rw-0	rw-0	rw-1	rw-0
FCTL2 Read:	← 096h →															
FCTL2 Write:	← 0A5h →															

The control bits are:

FN0 to FN5	012Ah, bit0 012Ah, bit5	These six bits determine the division rate of the clock signal. The division rate is 1 to 64, depending on the value of FN5 to FN0 plus one.
SSEL0 SSEL1	012Ah, bit0	Determine the clock source 0: ACLK 1: MCLK 2: SMCLK 3: SMCLK

lash memory control register FCTL3

There are no restrictions on modifying this control register. The control bits are reset or set (WAIT) by a PUC, but key violation bit KEYV is reset with a POR.



BUSY 012Ch, bit0 The BUSY bit shows if an access to the flash memory is correct (BUSY=0), or if an access violation has taken place. The BUSY bit should be tested before each write and erase cycle.

0: Flash memory is not busy.

1: Flash memory is busy. It remains in busy state if segment-write function is in *wait* mode.

KEYV, 012Ch, bit1 Key violated

0: Key 0A5h (high byte) was not violated.

1: Key 0A5h (high byte) was violated. Violation occurs when a write access to register FCTL1, FCTL2, or FCTL3 is executed and the *high byte* is not equal to 0A5h. If the security key is violated, bit KEYV is set and a PUC is performed.

ACCVIFG, 012Ch, bit2 Access-violation interrupt flag

The access-violation interrupt flag is set only when a write or erase operation is active. Access violation can only happen if the flash-memory module is written or read while it is busy. An instruction can be fetched during write, erase, and mass erase, but not during segment write. When the access-violation interrupt-enable bit is set, the interrupt-service request is accepted and the program continues at the NMI interrupt-vector address.

Reading the control registers will not set the ACCVIFG bit.

WAIT, 012Ch, bit3 In the segment-write mode, the WAIT bit indicates that the flash memory is prepared to receive the (next) data for programming. The WAIT bit is read only, but a write to WAIT bit is allowed.

0: Segment-write operation is started and programming is in progress

1: Segment write operation is active and programming of data has been completed

Lock 012Ch, bit4 The lock bit may be set during any write, erase of a segment, or *mass* erase request. The active sequence is completed normally. In segment-write mode, the SEGWRT and WAIT bits are reset and the mode ends in the regular manner. The software or hardware controls the lock bit. If an access violation occurs during segment-write mode, the ACCVIFG and LOCK bits may be set.

0: Flash memory may be read, programmed, erased, and *mass* erased.

1: Flash memory may be read but not programmed, erased, and mass-erased. A current program, erase, or *mass*-erase operation will complete normally. The access-violation interrupt flag ACCVIFG is set when the flash-memory module is accessed while the lock bit is set.

EMEX, 012Ch, bit5 Emergency exit. The emergency exit should only be used if a flash memory write or erase operation is out of control.

0: No function

1: Stops the active operation immediately and shuts down all internal parts in the flash memory controller. Current consumption immediately drops back to the active mode level. All bits in control register FCTL1 are reset. Since the EMEX bit is automatically reset by hardware, the software always reads EMEX as 0.

peripherals

Peripherals are connected to the CPU through data, address, and control busses, and can be easily handled using all memory-manipulation instructions.

oscillator and system clock

Three clocks are used in the system—the main system (master) clock (MCLK) used by the CPU and the system, the subsystem (master) clock (SMCLK) used by the peripheral modules, and the auxiliary clock (ACLK) originated by LFXT1CLK (crystal frequency) and used by the peripheral modules.

Following a POR the DCOCLK is used by default, the DCOR bit is reset, and the DCO is set to the nominal initial frequency. Additionally, if either LFXT1CLK (with XT1 mode selected by XTS=1) or XT2CLK fails as the source for MCLK, DCOCLK is automatically selected to ensure fail-safe operation.

SMCLK can be generated from XT2CLK or DCOCLK. ACLK is always generated from LFXT1CLK.

Crystal oscillator LFXT1 can be defined to operate with watch crystals (32,768 Hz) or with higher-frequency ceramic resonators or crystals. The crystal or ceramic resonator is connected across two terminals. No external components are required for watch-crystal operation. If the high-frequency XT1 mode is selected, external capacitors from XIN to VSS and XOUT to VSS are required, as specified by the crystal manufacturer.

The LFXT1 oscillator starts after application of VCC. If the OscOff bit is set to 1, the oscillator stops when it is not used for MCLK.

Crystal oscillator XT2 is identical to oscillator LFXT1, but only operates with higher-frequency ceramic resonators or crystals. The crystal or ceramic resonator is connected across two terminals. External capacitors from XT2IN to VSS and XT2OUT to VSS are required as specified by the crystal manufacturer.

The XT2 oscillator is off after application of VCC, since the XT2 oscillator control bit XT2Off is set. If bit XT2Off is set to 1, the XT2 oscillator stops when it is not used for MCLK or SMCLK.

Clock signals ACLK , MCLK, and SMCLK may be used externally via port pins.

Different application requirements and system conditions dictate different system-clock requirements, including:

- High frequency for quick reaction to system hardware requests or events
- Low frequency to minimize current consumption, EMI, etc.
- Stable peripheral clock for timer applications, such as real-time clock (RTC)
- Start-stop operation that can be enabled with minimum delay

multiplication

The multiplication operation is supported by a dedicated peripheral module. The module performs 16x16, 16x8, 8x16, and 8x8 bit operations. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

digital I/O

There are six 8-bit I/O ports implemented—ports P1 through P6. Ports P1 and P2 use seven control registers, while ports P3, P4, P5, and P6 use only four of the control registers to provide maximum digital input/output flexibility to the application:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Interrupt processing of external events is fully implemented for all eight bits of ports P1 and P2.
- Read/write access to all registers using all instructions is possible.

l I/O (continued)

The seven control registers are:

- Input register — 8 bits at ports P1 through P6
- Output register — 8 bits at ports P1 through P6
- Direction register — 8 bits at ports P1 through P6
- Interrupt edge select — 8 bits at ports P1 and P2
- Interrupt flags — 8 bits at ports P1 and P2
- Interrupt enable — 8 bits at ports P1 and P2
- Selection (port or module) — 8 bits at ports P1 through P6

Each one of these registers contains eight bits. Two interrupt vectors are implemented: one commonly used for any interrupt event on ports P1.0 to P1.7, and another commonly used for any interrupt event on ports P2.0 to P2.7.

Ports P3, P4, P5, and P6 have no interrupt capability.

chdog Timer

The primary function of the Watchdog Timer (WDT) module is to perform a controlled system restart after a software upset has occurred. A system reset is generated if the selected time interval expires. If an application does not require this watchdog function, the module can work as an interval timer, which generates an interrupt after a selected time interval.

The Watchdog Timer counter (WDTCNT) is a 15/16-bit up-counter not directly accessible by software. The WDTCNT is controlled using the Watchdog Timer control register (WDTCTL), which is an 8-bit read/write register. Writing to WDTCTL in either operating mode (watchdog or timer) is only possible when using the correct password (05Ah) in the high-byte. If any value other than 05Ah is written to the high-byte of the WDTCTL, a system reset PUC is generated. The password is read as 069h to minimize accidental write operations to the WDTCTL register. The low-byte stores data written to the WDTCTL. In addition to the Watchdog Timer control bits, there are two bits included in the WDTCTL that configure the NMI pin.

ART0 and USART1

There are two USART peripherals implemented in the MSP430x14x: USART0 and USART1; but only one in the MSP430x13x configuration: USART0. Both have an identical function as described in the applicable chapters of the *MSP430x1xx User's Guide*. They use different pins to communicate, and different registers for module control. Registers with identical functions have different addresses.

The universal synchronous/asynchronous interface is a dedicated peripheral module used in serial communications. The USART supports synchronous SPI (3- or 4-pin), and asynchronous UART communication protocols, using double-buffered transmit and receive channels. Data streams of 7 or 8 bits in length can be transferred at a rate determined by the program, or by an external clock. Low-power applications are optimized by UART mode options which allow for the reception of only the first byte of a complete frame. The application software should then decide if the succeeding data is to be processed. This option reduces power consumption.

Two dedicated interrupt vectors are assigned to each USART module—one for the receive and one for the transmit channels.

parator_A

The control bits are:

CAOUT,	05Ah, bit0	Comparator output
CAF,	05Ah, bit1	The comparator output is transparent or fed through a small filter
P2CA0,	05Ah, bit2	0: Pin P2.3/CA0/TA1 is not connected to Comparator_A. 1: Pin P2.3/CA0/TA1 is connected to Comparator_A.
P2CA1,	05Ah, bit3	0: Pin P2.4/CA1/TA2 is not connected to Comparator_A. 1: Pin P2.4/CA1/TA2 is connected to Comparator_A.
CACTL2.4 to CATCTL2.7	05Ah, bit4 to 05Ah, bit7	Bits are implemented but do not control any hardware in this device.
CAIFG,	059h, bit0	Comparator_A interrupt flag
CAIE,	059h, bit1	Comparator_A interrupt enable
CAIES,	059h, bit2	Comparator_A interrupt edge select bit 0: The rising edge sets the Comparator_A interrupt flag CAIFG 1: The falling edge set the Comparator_A interrupt flag CAIFG
CAON,	059h, bit3	The comparator is switched on.
CAREF,	059h, bit4,5	Comparator_A reference 0: Internal reference is switched off, an external reference can be applied. 1: 0.25 × VCC reference selected. 2: 0.50 × VCC reference selected. 3: A diode reference selected.
CARSEL,	059h, bit6	An internal reference V_{CAREF}, selected by CAREF bits, can be applied to signal path CA0 or CA1. The signal V_{CAREF} is only driven by a voltage source if the value of CAREF control bits is 1, 2, or 3.
CAEX,	059h, bit7	The comparator inputs are exchanged, used to measure and compensate the offset of the comparator.

Eight additional bits are implemented into the Comparator_A module. They enable the software to switch off the input buffer of Port P2. A CMOS input buffer can dissipate supply current when the input is not near V_{SS} or V_{CC}. Control bits CAPI0 to CAIP7 are initially reset and the port input buffer is active. The port input buffer is inactive if the corresponding control bit is set.

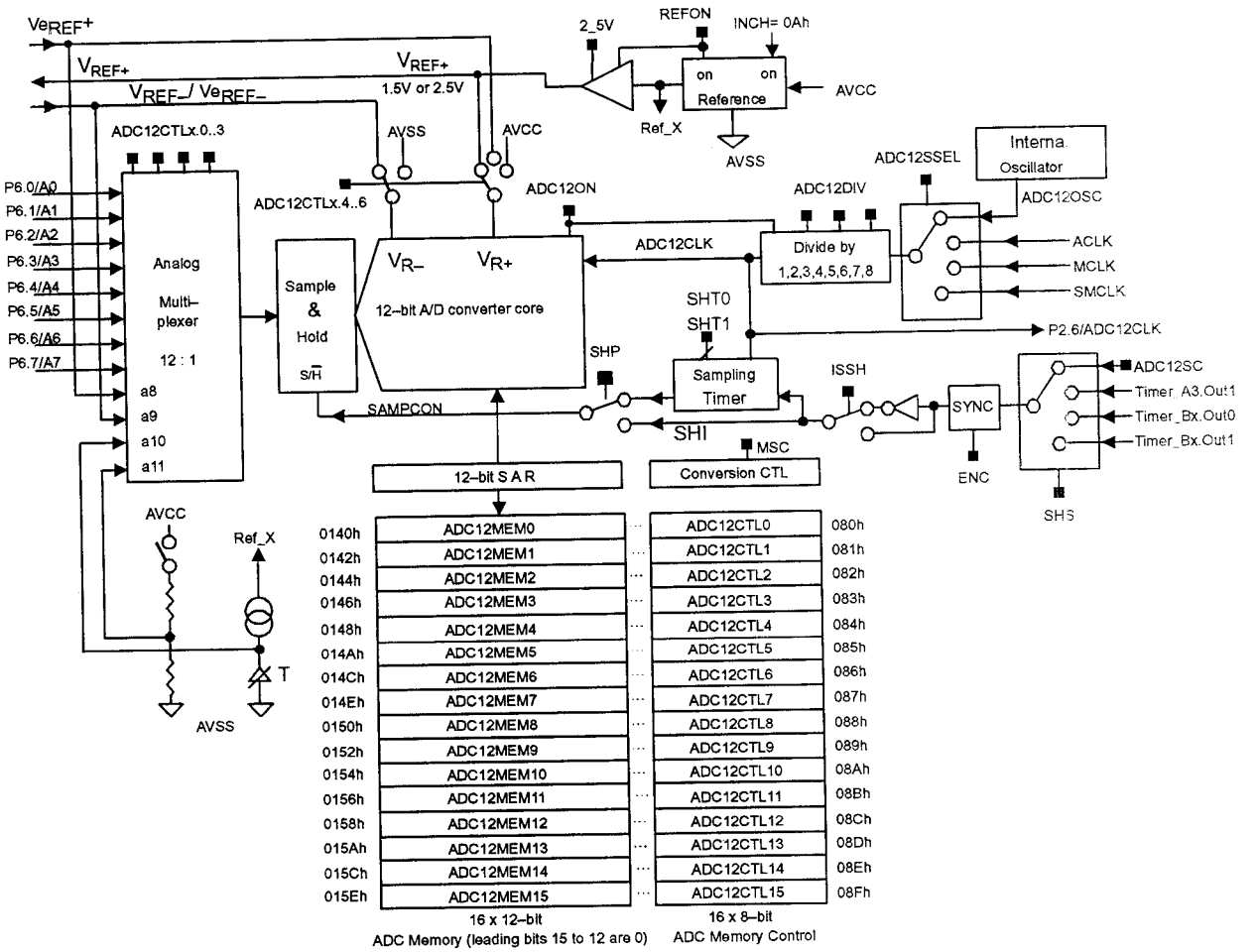
D converter

The 12-bit analog-to-digital converter (ADC) uses a 10-bit weighted capacitor array plus a 2-bit resistor string. The CMOS threshold detector in the successive-approximation conversion technique determines each bit by examining the charge on a series of binary-weighted capacitors. The features of the ADC are:

- 12-bit converter with ±1 LSB linearity
- Built-in sample-and-hold
- Eight external and four internal analog channels. The external ADC input terminals are shared with digital port I/O pins.
- Internal reference voltage V_{REF+} of 1.5 V or 2.5 V, software-selectable by control bit 2_5V
- Internal-temperature sensor for temperature measurement
  T = (V_SENSOR(T) – V_SENSOR(0°C)) / TC_SENSOR in °C
- Battery-voltage measurement: $N = 0.5 \times (AV_{CC} - AV_{SS}) \times 4096/1.5V$; V_{REF+} is selected for 1.5 V.
- Source of positive reference voltage level V_{R+} can be selected as internal (1.5 V or 2.5 V), external, or AV_{CC}. The source is selected individually for each channel.

A/D converter (continued)

- Source of negative reference voltage level V_{R-} can be selected as external or AV_{SS}. The source is selected individually for each channel.
- Conversion time can be selected from various clock sources: ACLK, MCLK, SMCLK, or the internal ADC12CLK oscillator. The clock source is divided by an integer from 1 to 8, as selected by software.
- Channel conversion: individual channels, a group of channels, or repeated conversion of a group of channels. If conversion of a group of channels is selected, the sequence, the channels, and the number of channels in the group can be defined by software. For example, a1-a2-a5-a2-a2-....
- The conversion is enabled by the ENC bit, and can be triggered by software via sample and conversion control bit ADC12SC, Timer_A3, or Timer_Bx. Most of the control bits can be modified only if ENC control bit is low. This prevents unpredictable results caused by unintended modification.
- Sampling time can be 4 × n0 × ADC12CLK or 4 × n1 × ADC12CLK. It can be selected to sample as long as the sample signal is high (ISSH=0) or low (ISSH=1). SHT0 defines n0 and SHT1 defines n1.
- The conversion result is stored in one of sixteen registers. The sixteen registers have individual addresses and can be accessed via software. Each of the sixteen registers is linked to an 8-bit register that defines the positive and negative reference source and the channel assigned.



converter (continued)

Table 4. Reference Voltage Configurations

SREF	VOLTAGE AT VR+	VOLTAGE AT VR–
0	AV_{CC}	AV_{SS}
1	V_{REF+} (internal)	AV_{SS}
2, 3	Ve_{REF+} (external)	AV_{SS}
4	AV_{CC}	V_{REF-}/Ve_{REF-} (internal or external)
5	V_{REF+} (internal)	V_{REF-}/Ve_{REF-} (internal or external)
6, 7	Ve_{REF+} (external)	V_{REF-}/Ve_{REF-} (internal or external)

trol registers ADC12CTL0 and ADC12CTL1

All control bits are reset during POR. POR is active after V_{CC} or a reset condition is applied to pin RST/NMI. A more detailed description of the control bit functions is found in the ADC12 module description (in the user's guide). Most of the control bits in registers ADC12CTL0, ADC12CTL1, and ADC12MCTLx can only be modified if ENC is low.

The following illustration highlights these bits. Six bits are excluded and can be unrestrictedly modified: ADC12SC, ENC, ADC12TOVIE, ADC12OVIE, and CONSEQ.

The control bits of control registers ADC12CTL0 and ADC12CTL1 are:

ADC12CTL0
01A0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHT1				SHT0				MSC	2_5 V	REF ON	ADC12 ON	ADC12 OVIE	ADC12 TOVIE	ENC	ADC12 SC
rw–(0)				rw–(0)				rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)

ADC12SC
01A0h, bit0

Sample and convert. The ADC12SC bit is used to control the conversion by software. It is recommended that ISSH=0.

SHP=1: Changing the ADC12SC bit from 0 to 1 starts the sample and conversion operation. Bit ADC12SC is automatically reset when the conversion is complete (BUSY=0).

SHP=0: A high level of bit ADC12SC determines the sample time. Conversion starts once it is reset (by software). The conversion takes 13 ADC12CLK cycles.

ENC
01A0h, bit1

Enable conversion. A conversion can be started by software (via ADC12SC) or by external signals, only if the enable conversion bit ENC is high. Most of the control bits in ADC12CTL0 and ADC12CTL1, and all the bits in ADCMCTL.x can only be changed if ENC is low.

0 : No conversion can be started. This is the initial state.

1: The first sample and conversion starts with the first rising edge of the sampling signal. The operation selected proceeds as long as ENC is set.

control registers ADC12CTL0 and ADC12CTL1

ADC12TOVIE
01A0h, bit2

Conversion time overflow interrupt enable.
The timing overflow takes place and a timing overflow vector is generated if another start of sample and conversion is requested while the current conversion or sequence of conversions is still active. The timing overflow enable, if set, may request an interrupt.

ADC12OVIE
01A0h, bit3

Overflow interrupt enables the individual enable for the overflow-interrupt vector.
The overflow takes place if the next conversion result is written into ADC memory ADC12MEMx but the previous result was not read. If an overflow vector is generated, the overflow-interrupt enable flag ADC12OVIE and the general-interrupt enable GIE are set and an interrupt service is requested.

ADC12ON
01A0h, bit4

Switch on the 12-bit ADC core. Make sure that the settling timing constraints are met if ADC core is powered up.

0: Power consumption of the core is off. No conversion is started.

1: ADC core is supplied with power. If no A/D conversion is required, ADC12ON can be reset to conserve power.

REFON
01A0h, bit5

Reference voltage on

0: The internal reference voltage is switched off. No power is consumed by the reference voltage generator.

1: The internal reference voltage is switched on and consumes additional power. The settling time of the reference voltage should be over before the first sample and conversion is started.

2_5V
01A0h, bit6

Reference voltage level

0: The internal-reference voltage is 1.5 V if REFON = 1.

1: The internal-reference voltage is 2.5 V if REFON = 1.

MSC
01A0h, bit7

Multiple sample and conversion. Works only when the sample timer is selected to generate the sample signal and to repeat single channel, sequence of channel, or when repeat sequence of channel (CONSEQ≠0) is selected.

0 :Only one sample is taken.

1 :If SHP is set and CONSEQ = {1, 2, or 3}, then the rising edge of the sample timer's input signal starts the repeat and/or the sequence of channel mode. Then the second and all further conversions are immediately started after the current conversion is completed.

SHT0
01A0h, bit8–11

Sample-and-hold Time0

SHT1
01A0h, bit12–15

Sample-and-hold Time1

The sample time is a multiple of the ADC12CLK × 4:

$$t_{sample} = 4 \times ADC12CLK \times n$$

SHT0/1	0	1	2	3	4	5	6	7	8	9	10	11	12–15
n	1	2	4	8	16	24	32	48	64	96	128	192	256

The sampling time defined by SHT0 is used when ADC12MEM0 through ADC12MEM7 are used during conversion. The sampling time defined by SHT1 is used when ADC12MEM8 through ADC12MEM15 are used during conversion.

rol registers ADC12CTL0 and ADC12CTL1 (continued)

ADC12CTL1
01A2h

15			8	7			0
CSStartAdd	SHS	SHP	ISSH	ADC12DIV	ADC12SSEL	CONSEQ	ADC12 BUSY
rw–(0) rw–(0) rw–(0) rw–(0) rw–(0) rw–(0) rw–(0) rw–(0)				rw–(0) rw–(0) rw–(0)	rw–(0) rw–(0)	rw–(0) rw–(0)	r –(0)

ADC12BUSY
01A2h, bit0

The BUSY signal indicates an active sample and conversion operation.

0: No conversion is active. The enable conversion bit ENC can be reset normally.

1: A sample period. Conversion or conversion sequence is active.

CONSEQ
01A2h, bit1/2

Select the conversion mode. Repeat mode is on if CONSEQ.1 (bit 1) is set.

0: One single channel is converted
1: One single sequence of channels is converted
2: Repeating conversion of one single channel
3: Repeating conversion of a sequence of channels

ADC12SSEL
01A2h, bit3/4

Selects the clock source for the converter core

0: Internal oscillator embedded in the ADC12 module
1: ACLK
2: MCLK
3: SMCLK

ADC12DIV
01A2h, bit5,6,7

Selects the division rate for the clock source selected by ADC12SSEL. The clock-operation signal ADC12CLK is used in the converter core. The conversion, without sampling time, requires 13 ADC12CLK clocks.

0 to 7: Divide selected clock source by integer from 1 to 8

ISSH
01A2h, bit8

Invert source for the sample signal

0: The source for the sample signal is not inverted.

1: The source for the sample signal is inverted.

SHP
01A2h, bit9

Sample-and-hold pulse, programmable length of sample pulse

0: The sample operation lasts as long as the sample-and-hold signal is 1. The conversion operation starts if the sample-and-hold signal goes from 1 to 0.

1: The sample time (sample signal is high) is defined by $nx4x(1/f_{ADC12CLK})$. SHTx holds the data for n. The conversion starts when the sample signal goes from 1 to 0.

SHS
01A2h, bit10/11

Source for sample-and-hold

0: Control bit ADC12SC triggers sample-and-hold followed by the A/D conversion.

1: The trigger signal for sample-and-hold and conversion comes from Timer_A3.EQU1.

2: The trigger signal for sample-and-hold and conversion comes from Timer_B.EQU0.

3: The trigger signal for sample-and-hold and conversion comes from Timer_B.EQU1.

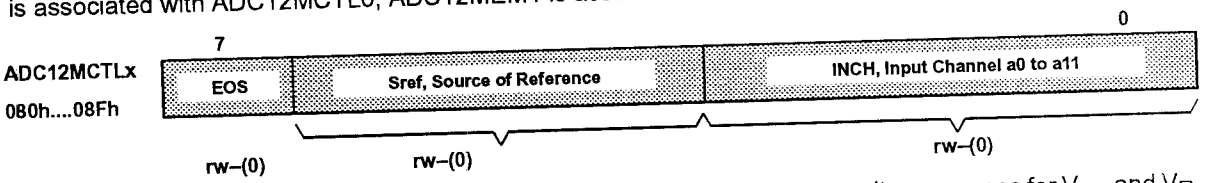
CStartAdd
01A2h, bit12 to bit15

Conversion start address CstartAdd is used to define which ADC12 control memory is used to start a (first) conversion. The value of CstartAdd ranges from 0 to 0Fh, corresponding to ADC12MEM0 to ADC12MEM15 and the associated control registers ADC12MCTL0 to ADC12MCTL15.

control register ADC12MCTLx and conversion memory ADC12MEMx

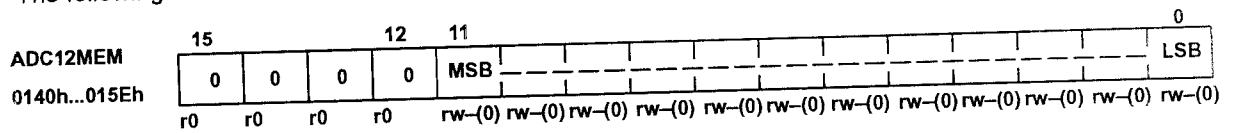
All control bits are reset during POR. POR is active after application of V_{CC}, or after a reset condition is applied to pin RST/NMI. Control registers ADC12MCTL.x can be modified only if enable conversion control bit ENC is reset. Any instruction that writes to an ADC12MCTLx register while the ENC bit is reset has no effect. A more detailed description of the control bit functions is found in the ADC12 module description (in the *MSP430x1xx User's Guide*).

There are sixteen ADC12MCTLx 8-bit memory control registers and sixteen ADC12MEMx 16-bit registers. Each of the memory control registers is associated with one ADC12MEMx register; for example, ADC12MEM0 is associated with ADC12MCTL0, ADC12MEM1 is associated with ADC12MCTL1, etc.



The control register bits are used to select the analog channel, the reference voltage sources for V_{R+} and V_{R-}, and a control signal which marks the last channel in a group of channels. The sixteen 16-bit registers ADC12MEMx are used to hold the conversion results.

The following illustration shows the conversion-result registers ADC12MEM0 to ADC12MEM15:



ADC12MEM0 to ADC12MEM15	0140h, bit0, 015Eh, bit15	The 12 bits of the conversion result are stored in 16 control registers ADC12MEM0 to ADC12MEM15. The 12 bits are right-justified and the upper four bits are always read as 0.

ADC12 interrupt flags ADC12IFG.x and enable registers ADC12IEN.x

There are 16 ADC12IFG.x interrupt flags, 16 ADC12IE.x interrupt-enable bits, and one interrupt-vector word. The 16 interrupt flags and enable bits are associated with the 16 ADC12MEMx registers. For example, register ADC12MEM0, interrupt flag ADC12IFG.0, and interrupt-enable bit ADC12IE.0 form one conversion-result block.

ADC12IFG.0 has the highest priority and ADC12IFG.15 has the lowest priority.

All interrupt flags and interrupt-enable bits are reset during POR. POR is active after application of V_{CC} or after a reset condition is applied to the RST/NMI pin.

ADC12 interrupt vector register

The 12-bit ADC has one interrupt vector for the overflow flag, the timing overflow flag, and sixteen interrupt flags. This vector indicates that a conversion result is stored into registers ADC12MEMx. Handling of the 18 flags is assisted by the interrupt-vector word. The 16-bit vector word ADC12IV indicates the highest pending interrupt. The interrupt-vector word is used to add an offset to the program counter so that the interrupt-handler software continues at the corresponding program location according to the interrupt event. This simplifies the interrupt-handler operation and assigns each interrupt event the same five-cycle overhead.

pheral file map

PERIPHERALS WITH WORD ACCESS			
Watchdog	Watchdog Timer control	WDTCTL	0120h
Timer_B7 Timer_B3 (see Note 10)	Timer_B interrupt vector	TBIV	011Eh
	Timer_B control	TBCTL	0180h
	Capture/compare control 0	CCTL0	0182h
	Capture/compare control 1	CCTL1	0184h
	Capture/compare control 2	CCTL2	0186h
	Capture/compare control 3	CCTL3	0188h
	Capture/compare control 4	CCTL4	018Ah
	Capture/compare control 5	CCTL5	018Ch
	Capture/compare control 6	CCTL6	018Eh
	Timer_B register	TBR	0190h
	Capture/compare register 0	CCR0	0192h
	Capture/compare register 1	CCR1	0194h
	Capture/compare register 2	CCR2	0196h
	Capture/compare register 3	CCR3	0198h
	Capture/compare register 4	CCR4	019Ah
	Capture/compare register 5	CCR5	019Ch
	Capture/compare register 6	CCR6	019Eh
Timer_A3	Timer_A interrupt vector	TAIV	012Eh
	Timer_A control	TACTL	0160h
	Capture/compare control 0	CCTL0	0162h
	Capture/compare control 1	CCTL1	0164h
	Capture/compare control 2	CCTL2	0166h
	Reserved		0168h
	Reserved		016Ah
	Reserved		016Ch
	Reserved		016Eh
	Timer_A register	TAR	0170h
	Capture/compare register 0	CCR0	0172h
	Capture/compare register 1	CCR1	0174h
	Capture/compare register 2	CCR2	0176h
	Reserved		0178h
	Reserved		017Ah
	Reserved		017Ch
	Reserved		017Eh
Multiply In MSP430x14x only	Sum extend	SumExt	013Eh
	Result high word	ResHi	013Ch
	Result low word	ResLo	013Ah
	Second operand	OP_2	0138h
	Multiply signed +accumulate/operand1	MACS	0136h
	Multiply+accumulate/operand1	MAC	0134h
	Multiply signed/operand1	MPYS	0132h
	Multiply unsigned/operand1	MPY	0130h

NOTE 10: Timer_B7 in MSP430x14x family has 7 CCR, Timer_B3 in MSP430x13x family has 3 CCR.

peripheral file map (continued)

PERIPHERALS WITH WORD ACCESS (CONTINUED)			
Flash	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
ADC12 See also *Peripherals with Byte Access*	Conversion memory 15	ADC12MEM15	015Eh
	Conversion memory 14	ADC12MEM14	015Ch
	Conversion memory 13	ADC12MEM13	015Ah
	Conversion memory 12	ADC12MEM12	0158h
	Conversion memory 11	ADC12MEM11	0156h
	Conversion memory 10	ADC12MEM10	0154h
	Conversion memory 9	ADC12MEM9	0152h
	Conversion memory 8	ADC12MEM8	0150h
	Conversion memory 7	ADC12MEM7	014Eh
	Conversion memory 6	ADC12MEM6	014Ch
	Conversion memory 5	ADC12MEM5	014Ah
	Conversion memory 4	ADC12MEM4	0148h
	Conversion memory 3	ADC12MEM3	0146h
	Conversion memory 2	ADC12MEM2	0144h
	Conversion memory 1	ADC12MEM1	0142h
	Conversion memory 0	ADC12MEM0	0140h
	Interrupt-vector-word register	ADC12IV	01A8h
	Inerrupt-enable register	ADC12IE	01A6h
	Inerrupt-flag register	ADC12IFG	01A4h
	Control register 1	ADC12CTL1	01A2h
	Control register 0	ADC12CTL0	01A0h
ADC12	ADC memory-control register15	ADC12MCTL15	08Fh
	ADC memory-control register14	ADC12MCTL14	08Eh
	ADC memory-control register13	ADC12MCTL13	08Dh
	ADC memory-control register12	ADC12MCTL12	08Ch
	ADC memory-control register11	ADC12MCTL11	08Bh
	ADC memory-control register10	ADC12MCTL10	08Ah
	ADC memory-control register9	ADC12MCTL9	089h
	ADC memory-control register8	ADC12MCTL8	088h
	ADC memory-control register7	ADC12MCTL7	087h
	ADC memory-control register6	ADC12MCTL6	086h
	ADC memory-control register5	ADC12MCTL5	085h
	ADC memory-control register4	ADC12MCTL4	084h
	ADC memory-control register3	ADC12MCTL3	083h
	ADC memory-control register2	ADC12MCTL2	082h
	ADC memory-control register1	ADC12MCTL1	081h
	ADC memory-control register0	ADC12MCTL0	080h

pheral file map (continued)

PERIPHERALS WITH BYTE ACCESS			
UART1 (Only in 'x14x)	Transmit buffer	UTXBUF.1	07Fh
	Receive buffer	URXBUF.1	07Eh
	Baud rate	UBR1.1	07Dh
	Baud rate	UBR0.1	07Ch
	Modulation control	UMCTL.1	07Bh
	Receive control	URCTL.1	07Ah
	Transmit control	UTCTL.1	079h
	UART control	UCTL.1	078h
UART0	Transmit buffer	UTXBUF.0	077h
	Receive buffer	URXBUF.0	076h
	Baud rate	UBR1.0	075h
	Baud rate	UBR0.0	074h
	Modulation control	UMCTL.0	073h
	Receive control	URCTL.0	072h
	Transmit control	UTCTL.0	071h
	UART control	UCTL.0	070h
Comparator_A	Comp._A port disable	CAPD	05Bh
	Comp._A control2	CACTL2	05Ah
	Comp._A control1	CACTL1	059h
System Clock	Basic clock system control2	BCSCTL2	058h
	Basic clock system control1	BCSCTL1	057h
	DCO clock frequency control	DCOCTL	056h
Port P6	Port P6 selection	P6SEL	037h
	Port P6 direction	P6DIR	036h
	Port P6 output	P6OUT	035h
	Port P6 input	P6IN	034h
Port P5	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h
Port P4	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
Port P3	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS			
Port P1	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt-edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Functions	SFR module enable 2	ME2	005h
	SFR module enable 1	ME1	004h
	SFR interrupt flag2	IFG2	003h
	SFR interrupt flag1	IFG1	002h
	SFR interrupt enable2	IE2	001h
	SFR interrupt enable1	IE1	000h

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Voltage applied at V_{CC} to V_{SS} ..... –0.3 V to + 4.1 V
Voltage applied to any pin (referenced to V_{SS}) ..... –0.3 V to V_{CC}+0.3 V
Diode current at any device terminal . ..... ±2 mA
Storage temperature (unprogrammed device) ..... –55°C to 150°C
Storage temperature (programmed device) ..... –40°C to 85°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltages referenced to V_{SS}.

ommended operating conditions

PARAMETER			MIN	NOM	MAX	UNITS
ply voltage during program execution, V_{CC} (AV_{CC} = DV_{CC} = V_{CC})		MSP430F13x, MSP430F14x	1.8		3.6	V
ply voltage during flash memory programming, V_{CC} $_{CC}$ = DV_{CC} = V_{CC})		MSP430F13x, MSP430F14x	2.7		3.6	V
ply voltage, V_{SS}			0.0		0.0	V
rating free-air temperature range, T_A		MSP430x13x MSP430x14x	–40		85	°C
T1 crystal frequency, $f_{(LFXT1)}$ e Notes 10 and 11)	LF selected, XTS=0	Watch crystal		32768		Hz
	XT1 selected, XTS=1	Ceramic resonator	450		8000	kHz
	XT1 selected, XTS=1	Crystal	1000		8000	kHz
2 crystal frequency, $f_{(XT2)}$		Ceramic resonator	450		8000	kHz
		Crystal	1000		8000	
cessor frequency (signal MCLK), $f_{(System)}$		V_{CC} = 1.8 V	DC		4.15	MHz
		V_{CC} = 3.6 V	DC		8	
sh-timing-generator frequency, $f_{(FTG)}$		MSP430F13x, MSP430F14x	257		476	kHz
mulative program time, $t_{(CPT)}$ (see Note 13)		V_{CC} = 2.7 V/3.6 V MSP430F13x MSP430F14x			3	ms
ss erase time, t(MEras) (See also the *flash memory, timing generator, ntrol register FCTL2* section, see Note 14)		V_{CC} = 2.7 V/3.6 V	200			ms
w-level input voltage (TCK, TMS, TDI, RST/NMI), V_{IL} (excluding Xin, Xout)		V_{CC} = 2.2 V/3 V	V_{SS}		V_{SS} +0.6	V
gh-level input voltage (TCK, TMS, TDI, RST/NMI), V_{IH} cluding Xin, Xout)		V_{CC} = 2.2 V/3 V	0.8V_{CC}		V_{CC}	V
ut levels at Xin and Xout	$V_{IL(Xin, Xout)}$	V_{CC} = 2.2 V/3 V	V_{SS}		0.2×V_{SS}	V
	$V_{IH(Xin, Xout)}$		0.8×V_{CC}		V_{CC}	

TES: 11. In LF mode, the LFXT1 oscillator requires a watch crystal and the LFXT1 oscillator requires a 5.1-MΩ resistor from XOUT to VSS when VCC < 2.5 V. In XT1 mode, the LFXT1. and XT2 oscillators accept a ceramic resonator or a 4-MHz crystal frequency at $V_{CC} \geq 2.2$ V. In XT1 mode, the LFXT1 and XT2 oscillators accept a ceramic resonator or an 8-MHz crystal frequency at $V_{CC} \geq 2.8$ V.

12. In LF mode, the LFXT1 oscillator requires a watch crystal. In XT1 mode, FXT1 accepts a ceramic resonator or a crystal.
13. The cumulative program time must not be exceeded during a segment-write operation. This parameter is only relevant if segment write option is used.
14. The mass erase duration generated by the flash timing generator is at least 11.1 ms. The cummulative mass erase time needed is 200 ms. This can be achieved by repeating the mass erase operation until the cumulative mass erase time is met (a minimum of 19 cycles may be required).

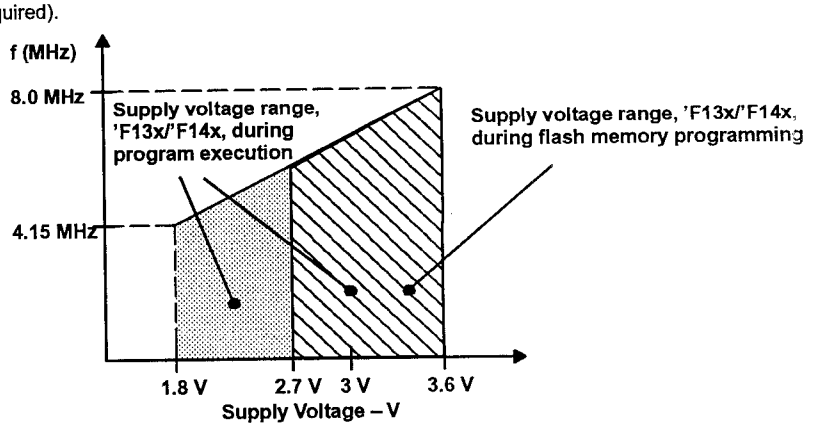


Figure 3. Frequency vs Supply Voltage, MSP430F13x or MSP430F14x

rical characteristics over recommended operating free-air temperature (unless otherwise d) (continued)

Current consumption of active mode versus system frequency, F-version

$I(AM) = I(AM)\ [1\ MHz] \times f(System)\ [MHz]$

Current consumption of active mode versus supply voltage, F-version

$I_{(AM)} = I_{(AM)}\ [3\ V] + 175\ \mu A/V \times (V_{CC} - 3\ V)$

MITT-trigger inputs – Ports P1, P2, P3, P4, P5, and P6

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Positive-going input threshold voltage	V_{CC} = 2.2 V	1.1		1.5	V
		V_{CC} = 3 V	1.5		1.9	
	Negative-going input threshold voltage	V_{CC} = 2.2 V	0.4		0.9	V
		V_{CC} = 3 V	0.90		1.3	
s	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)	V_{CC} = 2.2 V	0.3		1.1	V
		V_{CC} = 3 V	0.5		1	

ndard inputs – RST/NMI; JTAG: TCK, TMS, TDI, TDO/TDI

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low-level input voltage	V_{CC} = 2.2 V / 3 V	V_{SS}		V_{SS}+0.6	V
High-level input voltage		0.8×V_{CC}		V_{CC}	V

puts – Ports P1, P2, P3, P4, P5, and P6

	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
H	High-level output voltage	$I_{OH(max)}$ = –1 mA,	V_{CC} = 2.2 V,	See Note 17	V_{CC}–0.25		V_{CC}	V
		$I_{OH(max)}$ = –3.4 mA,	V_{CC} = 2.2 V,	See Note 18	V_{CC}–0.6		V_{CC}	
		$I_{OH(max)}$ = –1 mA,	V_{CC} = 3 V,	See Note 17	V_{CC}–0.25		V_{CC}	
		$I_{OH(max)}$ = –3.4 mA,	V_{CC} = 3 V,	See Note 18	V_{CC}–0.6		V_{CC}	
L	Low-level output voltage	$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 2.2 V,	See Note 17	V_{SS}		V_{SS}+0.25	V
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 2.2 V,	See Note 18	V_{SS}		V_{SS}+0.6	
		$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 3 V,	See Note 17	V_{SS}		V_{SS}+0.25	
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 3 V,	See Note 18	V_{SS}		V_{SS}+0.6	

TES: 17. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±6 mA to satisfy the maximum specified voltage drop.

18. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±24 mA to satisfy the maximum specified voltage drop.

utputs – Ports P1, P2, P3, P4, P5, and P6 (continued)

TYPICAL LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

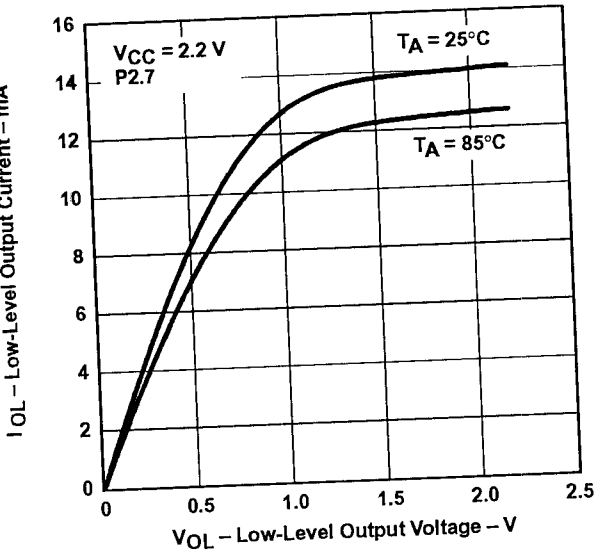


Figure 4

TYPICAL LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

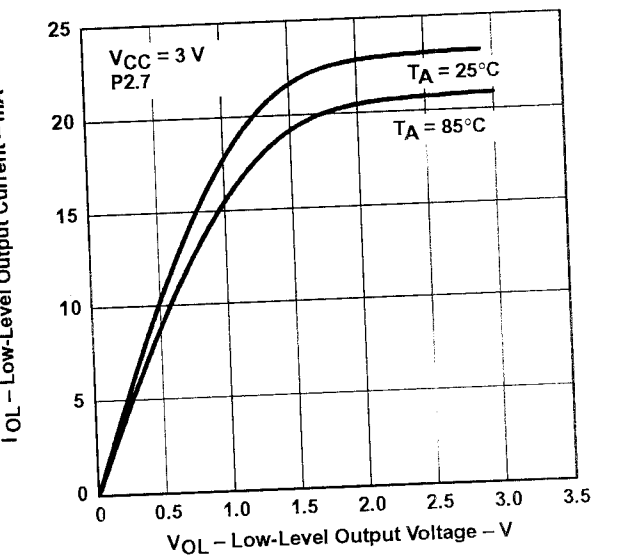


Figure 5

TYPICAL HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

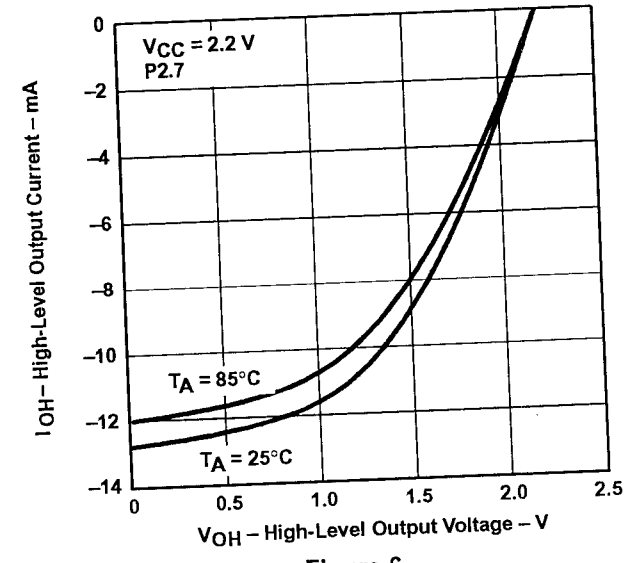


Figure 6

TYPICAL HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

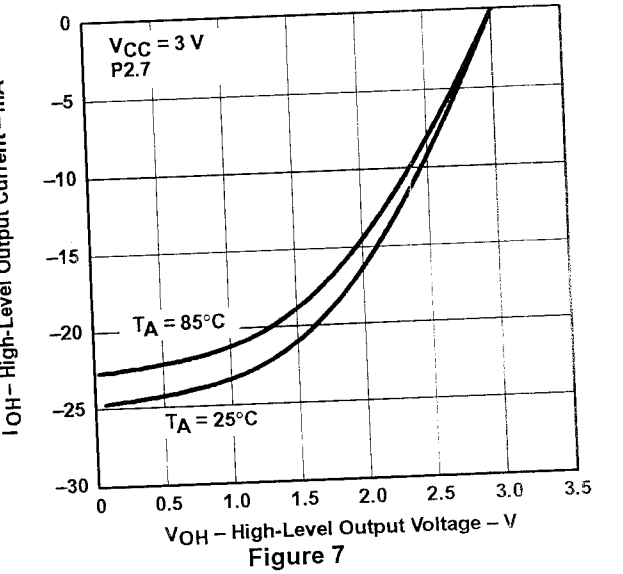


Figure 7

rical characteristics over recommended operating free-air temperature (unless otherwise d) (continued)

frequency – Ports P1, P2, P3, P4, P5, and P6

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
	$t_{(h)} = t_{(L)}$	V_{CC} = 2.2 V			8	MHz
		V_{CC} = 3 V			10	

ure timing _ Timer_A3: TA0, TA1, TA2; Timer_B7: TB0 to TB6

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Ports P2, P4: External trigger signal for the interrupt flag (see Notes 19 and 20)	V_{CC} = 2.2 V/3 V	1.5			Cycle
	V_{CC} = 2.2 V	62			ns
	V_{CC} = 3 V	50			

ES: 19. The external signal sets the interrupt flag every time $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$. The conditions to set the flag must be met independently of this timing constraint. $t_{(int)}$ is defined in MCLK cycles.
20. The external signal needs additional timing because of the maximum input-frequency constraint.

ut frequency

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
k	TA0..2, TB0–TB6, Internal clock source, SMCLK signal applied (see Note 21)	C_L = 20 pF		DC		f_{System}	MHz
LK, LK, ICLK	P5.6/ACLK, P5.4/MCLK, P5.5/SMCLK	C_L = 20 pF				f_{System}	
	Duty cycle of output frequency,	P2.0/ACLK C_L = 20 pF, V_{CC} = 2.2 V / 3 V	$f_{ACLK} = f_{LFXT1} = f_{XT1}$	40%		60%	
			$f_{ACLK} = f_{LFXT1} = f_{LF}$	30%		70%	
			$f_{ACLK} = f_{LFXT1/n}$		50%		
lc		P1.4/SMCLK, C_L = 20 pF, V_{CC} = 2.2 V / 3 V	$f_{SMCLK} = f_{LFXT1} = f_{XT1}$	40%		60%	
			$f_{SMCLK} = f_{LFXT1} = f_{LF}$	35%		65%	
			$f_{SMCLK} = f_{LFXT1/n}$	50%–15 ns	50%	50%–15 ns	
			$f_{SMCLK} = f_{DCOCLK}$	50%–15 ns	50%	50%–15 ns	

TE 21: The limits of the system clock MCLK has to be met; the system (MCLK) frequency should not exceed the limits. MCLK and SMCLK frequencies can be different.

ternal interrupt timing

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Ports P1, P2: nt) External trigger signal for the interrupt flag (see Notes 22 and 23)	V_{CC} = 2.2 V/3 V	1.5			Cycle
	V_{CC} = 2.2 V	62			ns
	V_{CC} = 3 V	50			

OTES: 22. The external signal sets the interrupt flag every time $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$. The conditions to set the flag must be met independently of this timing constraint. $t_{(int)}$ is defined in MCLK cycles.
23. The external signal needs additional timing because of the maximum input-frequency constraint.

ake-up LPM3

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
(LPM3)	Delay time	f = 1 MHz	V_{CC} = 2.2 V/3 V			6	µs
		f = 2 MHz				6	
		f = 3 MHz				6	

ectrical characteristics over recommended operating free-air temperature (unless otherwise ɔted) (continued)

ain DCO characteristics

- Individual devices have a minimum and maximum operation frequency. The specified parameters for fDCOx0 to fDCOx7 are valid for all devices.
- All ranges selected by Rsel(n) overlap with Rsel(n+1): Rsel0 overlaps with Rsel1, ... Rsel6 overlaps with Rsel7.
- DCO control bits DCO0, DCO1, and DCO2 have a step size as defined by parameter SDCO.
- Modulation control bits MOD0 to MOD4 select how often fDCO+1 is used within the period of 32 DCOCLK cycles. The frequency f(DCO) is used for the remaining cycles. The frequency is an average equal to f(DCO) × ($2^{MOD/32}$).

crystal oscillator, LFXT1 oscillator (see Note 31)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
X_{CIN}	Integrated input capacitance	XTS=0; LF oscillator selected V_{CC} = 2.2 V/3 V		12		pF
		XTS=1; XT1 oscillator selected V_{CC} = 2.2 V/3 V		2		
X_{COUT}	Integrated output capacitance	XTS=0; LF oscillator selected V_{CC} = 2.2 V/3 V		12		pF
		XTS=1; XT1 oscillator selected V_{CC} = 2.2 V/3 V		2		
X_{INL}	Input levels at XIN, XOUT	V_{CC} = 2.2 V/3 V	V_{SS}		$0.2 \times V_{CC}$	V
X_{INH}		V_{CC} = 2.2 V/3 V	$0.8 \times V_{CC}$		V_{CC}	V

NOTE 31: The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.

crystal oscillator, XT2 oscillator (see Note 32)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
X_{CIN}	Integrated input capacitance	V_{CC} = 2.2 V/3 V		2		pF
X_{COUT}	Integrated output capacitance	V_{CC} = 2.2 V/3 V		2		pF
X_{INL}	Input levels at XIN, XOUT	V_{CC} = 2.2 V/3 V	V_{SS}		$0.2 \times V_{CC}$	V
X_{INH}		V_{CC} = 2.2 V/3 V	$0.8 \times V_{CC}$		V_{CC}	V

NOTE 32: The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.

USART0, USART1 (see Note 33)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{(\tau)}$	USART0/1: deglitch time	V_{CC} = 2.2 V	200	430	800	ns
		V_{CC} = 3 V	150	280	500	

NOTE 33: The signal applied to the USART0/1 receive signal/terminal (URXD0/1) should meet the timing requirements of $t_{(t)}$ to ensure that the URXS flip-flop is set. The URXS flip-flop is set with negative pulses meeting the minimum-timing condition of $t_{(t)}$. The operating conditions to set the flag must be met independently from this timing constraint. The deglitch circuitry is active only on negative transitions on the URXD0/1 line.

rical characteristics over recommended operating free-air temperature (unless otherwise d) (continued)

ADC, power supply and input range conditions (see Note 34)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
	Analog supply voltage	AV_{CC} and DV_{CC} are connected together AV_{SS} and DV_{SS} are connected together $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.2		3.6	V
F+	Positive built-in reference voltage output	2_5 V = 1 for 2.5 V built-in reference 2_5 V = 0 for 1.5 V built-in reference $I_{V(REF+)} \le I_{(VREF+)max}$	3 V	2.4	2.5	2.6	V
			2.2 V/3 V	1.44	1.5	1.56	
F+	Load current out of V_{REF+} terminal		2.2 V	0.01		–0.5	mA
			3 V			–1	
	Load-current regulation V_{REF+} terminal	$I_{V(REF)+}$ = 500 µA +/– 100 µA Analog input voltage ~0.75 V; 2_5 V = 0	2.2 V			±2	LSB
			3 V			±2	
REF)+ †		$I_{V(REF)+}$ = 500 µA ± 100 µA Analog input voltage ~1.25 V; 2_5 V = 1	3 V			±2	LSB
VREF) +‡	Load current regulation V_{REF+} terminal	$I_{V(REF)+}$ =100 µA → 900 µA, VCC=3 V, ax ~0.5 x V_{REF+} Error of conversion result ≤ 1 LSB	C_{VREF+}=5 µF			20	ns
EF+	Positive external reference voltage input	$V_{eREF+} > V_{eREF-}/V_{eREF-}$ (see Note 35)		1.4		V_{AVCC}	V
EF– /VeREF–	Negative external reference voltage input	$V_{eREF+} > V_{eREF-}/V_{eREF-}$ (see Note 36)		0		1.2	V
REF+ – EF–/VeREF–)	Differential external reference voltage input	$V_{eREF+} > V_{eREF-}/V_{eREF-}$ (see Note 37)		1.4		V_{AVCC}	V
6.x/Ax)	Analog input voltage range (see Note 38)	All P6.0/A0 to P6.7/A7 terminals. Analog inputs selected in ADC12MCTLx register and P6Sel.x=1 $0 \le x \le 7$; $V_{(AVSS)} \le V_{P6.x/Ax} \le V_{(AVCC)}$		0		V_{AVCC}	V
DC12	Operating supply current into AV_{CC} terminal (see Note 39)	$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 1, REFON = 0 SHT0=0, SHT1=0, ADC12DIV=0	2.2 V		0.65	1.3	mA
			3 V		0.8	1.6	
EF+	Operating supply current into AV_{CC} terminal (see Note 40)	$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 0, REFON = 1, 2_5V = 1	3 V		0.5	0.8	mA
EF+	Operating supply current (see Note 40)	$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 0, REFON = 1, 2_5V = 0	2.2 V		0.5	0.8	mA
			3 V		0.5	0.8	

ot production tested, limits characterized
ot production tested, limits verified by design

TES: 34. The leakage current is defined in the leakage current table with P6.x/Ax parameter.
35. The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
36. The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
37. The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
38. The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
39. The internal reference supply current is not included in current consumption parameter I_{ADC12}.
40. The internal reference current is supplied via terminal AV_{CC}. Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.

lectrical characteristics over recommended operating free-air temperature (unless otherwise oted) (continued)

2-bit ADC, built-in reference (see Note 41)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
V_{eREF+}	Static input current (see Note 42)	$0V \le V_{eREF+} \le V_{AVCC}$	2.2 V/3 V			±1	µA
$I_{VREF-/VeREF-}$	Static input current (see Note 42)	$0V \le V_{eREF-} \le V_{AVCC}$	2.2 V/3 V			±1	µA
C_{VREF+}	Capacitance at pin V_{REF+} (see Note 43)	REFON =1, $0 mA \le I_{VREF+} \le I_{V(REF)+(max)}$	2.2 V/3 V	5	10		µF
C_i ‡	Input capacitance (see Note 44)	Only one terminal can be selected at one time, P6.x/Ax	2.2 V			40	pF
Z_i‡	Input MUX ON resistance(see Note 44)	$0V \le V_{Ax} \le V_{AVCC}$	3 V			2000	Ω
T_{REF+}†	Temperature coefficient of built-in reference	$I_{V(REF)+}$ is a constant in the range of $0 mA \le I_{V(REF)+} \le 1 mA$	2.2 V/3 V			±100	ppm/°C

† Not production tested, limits characterized
‡ Not production tested, limits verified by design

NOTES: 41. The voltage source on V_{eREF+} and $V_{REF-/VeREF-}$) needs to have low dynamic impedance for 12-bit accuracy to allow the charge to settle for this accuracy (See Figures 12 and 13).
42. The external reference is used during conversion to charge and discharge the capacitance array. The dynamic impedance should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
43. The internal buffer operational amplifier and the accuracy specifications require an external capacitor.
44. The input capacitance is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy. All INL and DNL tests uses two capacitors between pins V(REF+) and AVSS and V(REF–)/V(eREF–) and AVSS: 10 µF tantalum and 100 nF ceramic.

trical characteristics over recommended operating free-air temperature (unless otherwise d) (continued)

it ADC, timing parameters

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
F(ON)†	Settle time of internal reference voltage (see Figure 15 and Note 45)	$I_{V(REF)+}$ = 0.5 mA, $C_{V(REF)+}$ = 10 µF, V_{REF+} = 1.5 V, V_{AVCC} = 2.2 V				17	ms
C12OSC)		ADC12DIV=0 [f(ADC12CLK) =f(ADC12OSC)]	2.2 V	3.7		6.3	MHz
			3 V				
NVERT	Conversion time	$AV_{CC(min)} \le V_{AVCC} \le AV_{CC(max)}$, $C_{VREF+} \ge 5$ µF, Internal oscillator, f_{OSC} = 3.7 MHz to 6.3 MHz	2.2 V/ 3 V	2.06		3.51	µs
	Conversion time	$A_{VCC(min)} \le V_{AVCC} \le A_{VCC(max)}$, External $f_{ADC12(CLK)}$ from ACLK or MCLK or SMCLK: ADC12SSEL ≠ 0			13×ADC12DIV× $1/f_{ADC12(CLK)}$		µs
C12ON‡	Settle time of the ADC	$A_{VCC(min)} \le V_{AVCC} \le A_{VCC(max)}$ (see Note 46)				100	ns
mple‡	Sampling time	$V_{AVCC(min)} \le V_{AVCC} \le V_{AVCC(max)}$ $R_{i(source)}$ = 400 Ω, Z_i = 1000 Ω, C_i = 30 pF $\tau = [R_{i(source)} x + Z_i] \times C_i$ (see Note 47)	3 V	1220			ns
			2.2 V	1400			

ot production tested, limits characterized
ot production tested, limits verified by design

TES: 45. The condition is that the error in a conversion started after $t_{REF(ON)}$ is less than ±0.5 LSB. The settling time depends on the external capacitive load.

46. The condition is that the error in a conversion started after $t_{ADC12ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.

47. Ten Tau (τ) are needed to get an error of less than ±0.5 LSB. t_{Sample} = 10 x (Ri + Zi) x Ci+ 800 ns

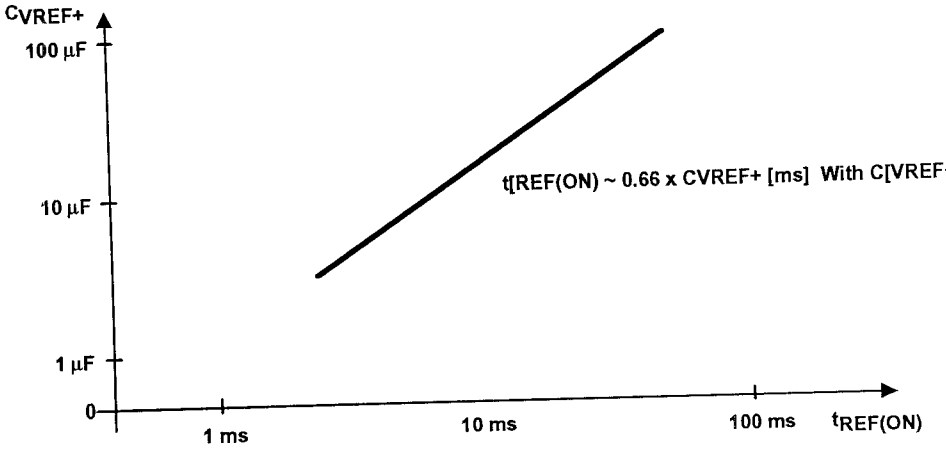


Figure 15. Typical Settling Time of Internal Reference $t_{REF(ON)}$ vs External Capacitor on V_{REF+}

ectrical characteristics over recommended operating free-air temperature (unless otherwise oted) (continued)

2-bit ADC, linearity parameters

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$E_{(I)}$	Integral linearity error	1.4 V ≤ (VeREF+ – VREF–/VeREF–) min ≤ 1.6 V	2.2 V/3 V			±2	LSB
		1.6 V < [V(eREF+) – V(REF–)/V(eREF–)] min ≤ [V(AVCC)]				±1.7	
E_D	Differential linearity error	($V_{eREF+} - V_{REF-}/V_{eREF-}$)min ≤ ($V_{eREF+} - V_{REF-}/V_{eREF-}$), C(VREF+) = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V/3 V			±1	LSB
E_O	Offset error†	($V_{eREF+} - V_{REF-}/V_{eREF-}$)min ≤ ($V_{eREF+} - V_{REF-}/V_{eREF-}$), Internal impedance of source R_i < 100 Ω, C(VREF+) = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±2	±4	LSB
E_G	Gain error†	($V_{eREF+} - V_{REF-}/V_{eREF-}$)min ≤ ($V_{eREF+} - V_{REF-}/V_{eREF-}$), C(VREF+) = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±1.1	±2	LSB
E_T	Total unadjusted error†	($V_{eREF+} - V_{REF-}/V_{eREF-}$)min ≤ ($V_{eREF+} - V_{REF-}/V_{eREF-}$), C(VREF+) = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±2	±5	LSB

† Not production tested, limits characterized

National Semiconductor

August 2000

LM139/LM239/LM339/LM2901/LM3302 Low Power Low Offset Voltage Quad Comparators

General Description

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic— where the low power drain of the LM339 is a distinct advantage over standard comparators.

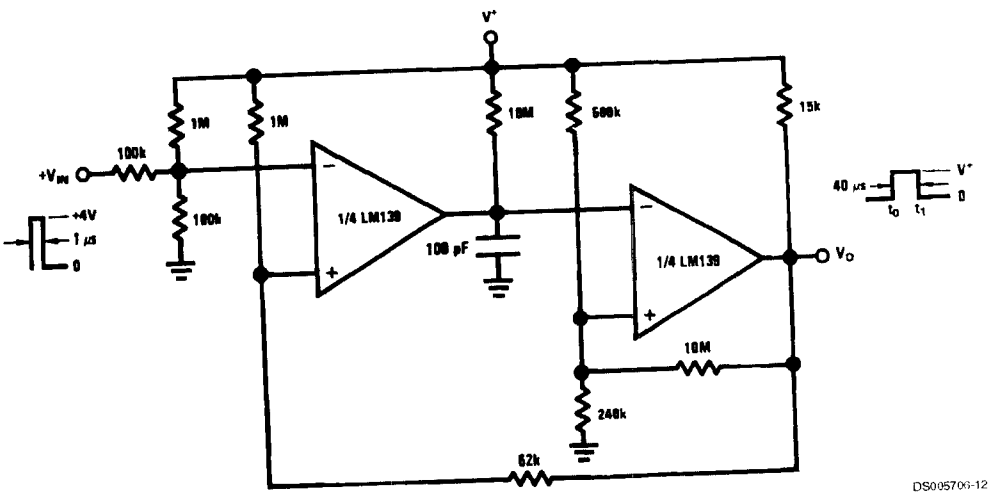
Features

- Wide supply voltage range
- LM139/139A Series 2 to 36 V_{DC} or ±1 to ±18 V_{DC}
- LM2901: 2 to 36 V_{DC} or ±1 to ±18 V_{DC}
- LM3302: 2 to 28 V_{DC} or ±1 to ±14 V_{DC}
- Very low supply current drain (0.8 mA) — independent of supply voltage
- Low input biasing current: 25 nA
- Low input offset current: ±5 nA
- Offset voltage: ±3 mV
- Input common-mode voltage range includes GND
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage: 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Advantages

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

One-Shot Multivibrator with Input Lock Out



DS005706-12

Absolute Maximum Ratings (Note 10)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LM139/LM239/LM339 LM139A/LM239A/LM339A LM2901	LM3302
Supply Voltage, V^+	36 V_{DC} or ±18 V_{DC}	28 V_{DC} or ±14 V_{DC}
Differential Input Voltage (Note 8)	36 V_{DC}	28 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}	−0.3 V_{DC} to +28 V_{DC}
Input Current (V_{IN}<−0.3 V_{DC}), (Note 3)	50 mA	50 mA
Power Dissipation (Note 1)		1050 mW
Molded DIP	1050 mW	
Cavity DIP	1190 mW	
Small Outline Package	760 mW	
Output Short-Circuit to GND, (Note 2)	Continuous	Continuous
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C
Operating Temperature Range		−40°C to +85°C
LM339/LM339A	0°C to +70°C	
LM239/LM239A	−25°C to +85°C	
LM2901	−40°C to +85°C	
LM139/LM139A	−55°C to +125°C	
Soldering Information		
Dual-In-Line Package		260°C
Soldering (10 seconds)	260°C	
Small Outline Package		215°C
Vapor Phase (60 seconds)	215°C	220°C
Infrared (15 seconds)	220°C	
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.		
ESD rating (1.5 kΩ in series with 100 pF)	600V	600V

Electrical Characteristics

(V^+=5 V_{DC}, T_A = 25°C, unless otherwise stated)

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)		1.0	2.0		1.0	2.0		2.0	5.0	mV_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, (Note 5), V_{CM}=0V		25	100		25	250		25	100	nA_{DC}
Input Offset Current	$I_{IN(+)}-I_{IN(-)}$, V_{CM}=0V		3.0	25		5.0	50		3.0	25	nA_{DC}
Input Common-Mode Voltage Range	V^+=30 V_{DC} (LM3302, V^+=28 V_{DC}) (Note 6)	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	V_{DC}
Supply Current	R_L=∞ on all Comparators,		0.8	2.0		0.8	2.0		0.8	2.0	mA_{DC}
	R_L=∞, V^+=36V, (LM3302, V^+=28 V_{DC})					1.0	2.5		1.0	2.5	mA_{DC}
Voltage Gain	R_L≥15 kΩ, V^+=15 V_{DC} V_o= 1 V_{DC} to 11 V_{DC}	50	200		50	200		50	200		V/mV
Large Signal Response Time	V_{IN}=TTL Logic Swing, V_{REF}= 1.4 V_{DC}, V_{RL}=5 V_{DC}, R_L=5.1 kΩ		300			300			300		ns
Response Time	V_{RL}=5 V_{DC}, R_L=5.1 kΩ,		1.3			1.3			1.3		µs

trical Characteristics (Continued)

V_{DC}, T_A = 25°C, unless otherwise stated)

arameter	Conditions	LM139A			LM239A, LM339A			LM139			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
ink Current	$V_{IN(-)}$=1 V_{DC}, $V_{IN(+)}$=0, V_O≤1.5 V_{DC}	6.0	16		6.0	16		6.0	16		mA_{DC}
on Voltage	$V_{IN(-)}$=1 V_{DC}, $V_{IN(+)}$=0, I_{SINK}≤4 mA		250	400		250	400		250	400	mV_{DC}
Leakage nt	$V_{IN(+)}$=1 V_{DC}, $V_{IN(-)}$=0, V_O=5 V_{DC}		0.1			0.1			0.1		nA_{DC}

ctrical Characteristics

V_{DC}, T_A = 25°C, unless otherwise stated)

Parameter	Conditions	LM239, LM339			LM2901			LM3302			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Offset Voltage	(Note 9)		2.0	5.0		2.0	7.0		3	20	mV_{DC}
Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, (Note 5), V_{CM}=0V		25	250		25	250		25	500	nA_{DC}
Offset Current	$I_{IN(+)}$−$I_{IN(-)}$, V_{CM}=0V		5.0	50		5	50		3	100	nA_{DC}
Common-Mode age Range	V^+=30 V_{DC} (LM3302, V^+=28 V_{DC}) (Note 6)	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	V_{DC}
y Current	R_L=∞ on all Comparators, R_L=∞, V^+=36V, (LM3302, V^+=28 V_{DC})		0.8 1.0	2.0 2.5		0.8 1.0	2.0 2.5		0.8 1.0	2.0 2.5	mA_{DC} mA_{DC}
ge Gain	R_L≥15 kΩ, V^+=15 V_{DC} V_o= 1 V_{DC} to 11 V_{DC}	50	200		25	100		2	30		V/mV
e Signal sponse Time	V_{IN}=TTL Logic Swing, V_{REF}= 1.4 V_{DC}, V_{RL}=5 V_{DC}, R_L=5.1 kΩ,		300			300			300		ns
onse Time	V_{RL}=5 V_{DC}, R_L=5.1 kΩ, (Note 7)		1.3			1.3			1.3		µs
ut Sink Current	$V_{IN(-)}$=1 V_{DC}, $V_{IN(+)}$=0, V_O≤1.5 V_{DC}	6.0	16		6.0	16		6.0	16		mA_{DC}
ration Voltage	$V_{IN(-)}$=1 V_{DC}, $V_{IN(+)}$=0, I_{SINK}≤4 mA		250	400		250	400		250	500	mV_{DC}
put Leakage urrent	$V_{IN(+)}$=1 V_{DC}, $V_{IN(-)}$=0, V_O=5 V_{DC}		0.1			0.1			0.1		nA_{DC}

Electrical Characteristics

V^+ = 5.0 V_{DC}, (Note 4))

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
ut Offset Voltage	(Note 9)			4.0			4.0			9.0	mV_{DC}
ut Offset Current	$I_{IN(+)}$−$I_{IN(-)}$, V_{CM}=0V			100			150			100	nA_{DC}
ut Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, V_{CM}=0V (Note 5)			300			400			300	nA_{DC}
put Common-Mode oltage Range	V^+=30 V_{DC} (LM3302, V^+=28 V_{DC}) (Note 6)	0		V^+−2.0	0		V^+−2.0	0		V^+−2.0	V_{DC}
aturation Voltage	$V_{IN(-)}$=1 V_{DC}, $V_{IN(+)}$=0,			700			700			700	mV_{DC}

Electrical Characteristics (Continued)

(V^+ = 5.0 V_{DC}, (Note 4))

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Leakage Current	$V_{IN(+)}$=1 V_{DC}, $V_{IN(-)}$=0, V_O=30 V_{DC}, (LM3302, V_O=28 V_{DC})			1.0			1.0			1.0	μA_{DC}
Differential Input Voltage	Keep all V_{IN}'s≥0 V_{DC} (or V^-, if used), (Note 8)			36			36			36	V_{DC}

Electrical Characteristics

(V^+ = 5.0 V_{DC}, (Note 4))

Parameter	Conditions	LM239, LM339			LM2901			LM3302			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)			9.0		9	15			40	mV_{DC}
Input Offset Current	$I_{IN(+)}$–$I_{IN(-)}$, V_{CM}=0V			150		50	200			300	nA_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, V_{CM}=0V (Note 5)			400		200	500			1000	nA_{DC}
Input Common-Mode Voltage Range	V^+=30 V_{DC} (LM3302, V^+=28 V_{DC}) (Note 6)			V^+–2.0	0		V^+–2.0	0		V^+–2.0	V_{DC}
Saturation Voltage	$V_{IN(-)}$=1 V_{DC}, $V_{IN(+)}$=0, I_{SINK}≤4 mA			700		400	700			700	mV_{DC}
Output Leakage Current	$V_{IN(+)}$=1 V_{DC}, $V_{IN(-)}$=0, V_O=30 V_{DC}, (LM3302, V_O=28 V_{DC})			1.0			1.0			1.0	μA_{DC}
Differential Input Voltage	Keep all V_{IN}'s≥0 V_{DC} (or V^-, if used), (Note 8)			36			36			28	V_{DC}

Note 1: For operating at high temperatures, the LM339/LM339A, LM2901, LM3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 95°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM239 and LM139 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small (P_D≤100 mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V_{DC} (at 25°)C.

Note 4: These specifications are limited to −55°C≤T_A≤+125°C, for the LM139/LM139A. With the LM239/LM239A, all temperature specifications are limited to −25°C≤T_A≤+85°C, the LM339/LM339A temperature specifications are limited to 0°C≤T_A≤+70°C, and the LM2901, LM3302 temperature range is −40°C≤T_A≤+85°C.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+ −1.5V at 25°C, but either or both inputs can go to +30 V_{DC} without damage (25V for LM3302), independent of the magnitude of V^+.

Note 7: The response time specified is a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

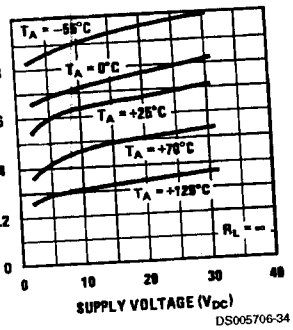
Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3 V_{DC} (or 0.3 V_{DC}below the magnitude of the negative power supply, if used) (at 25°C).

Note 9: At output switch point, V_O=1.4 V_{DC}, R_S=0Ω with V^+ from 5 V_{DC} to 30 V_{DC}; and over the full input common-mode range (0 V_{DC} to V^+ −1.5 V_{DC}), at 25°C. For LM3302, V^+ from 5 V_{DC} to 28 V_{DC}.

Note 10: Refer to RETS139AX for LM139A military specifications and to RETS139X for LM139 military specifications.

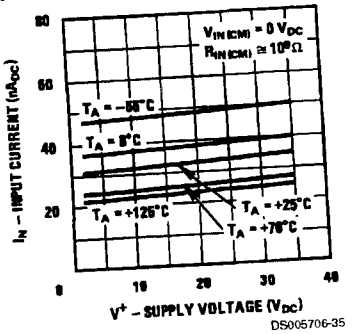
cal Performance Characteristics LM139/LM239/LM339, LM139A/LM239A/LM339A, LM3302

Current



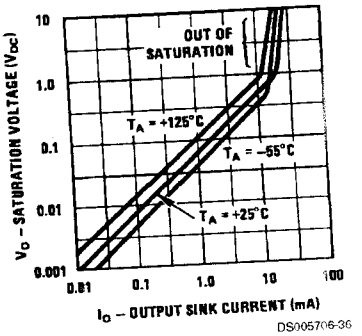
DS005706-34

Input Current



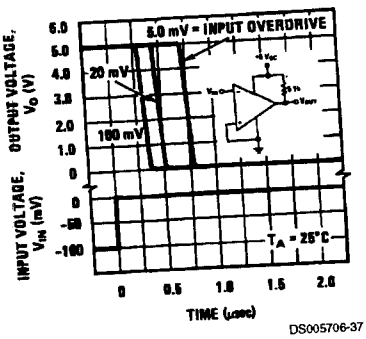
DS005706-35

Output Saturation Voltage



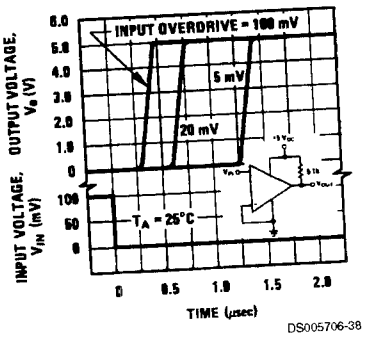
DS005706-36

onse Time for Various Overdrives—Negative sition



DS005706-37

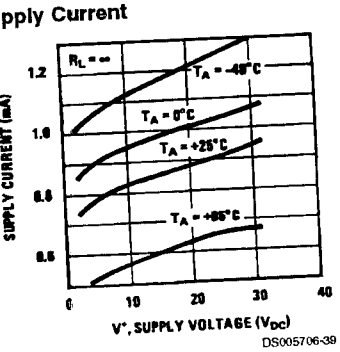
Response Time for Various Input Overdrives—Positive Transition



DS005706-38

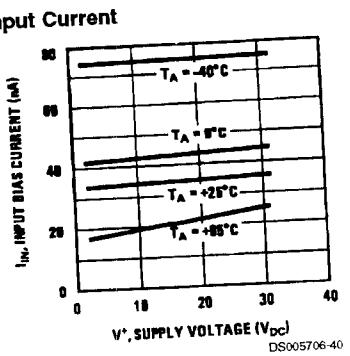
ypical Performance Characteristics LM2901

pply Current



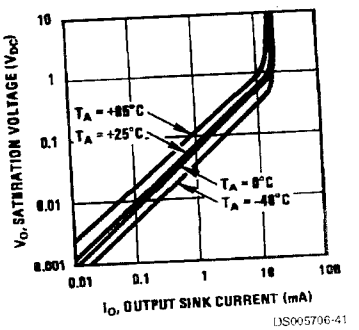
DS005706-39

Input Current



DS005706-40

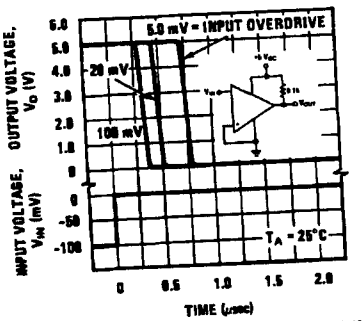
Output Saturation Voltage



DS005706-41

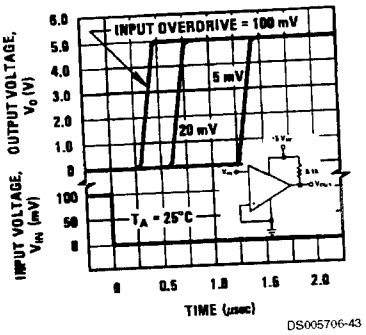
Typical Performance Characteristics LM2901 (Continued)

Response Time for Various Input Overdrives—Negative Transition



DS005706-42

Response Time for Various Input Overdrives-Positive Transition



DS005706-43

Application Hints

The LM139 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing this input resistors to < 10 kΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be tied to the negative supply.

The bias network of the LM139 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 V_{DC} to 30 V_{DC}.

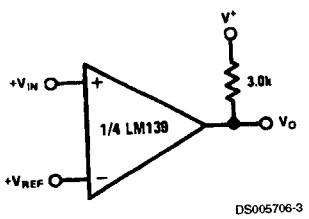
It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in the applications section.

The output of the LM139 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM139A package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω R_{SAT} of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.

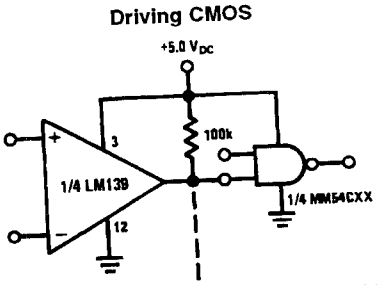
Typical Applications (V^+ = 5.0 V_{DC})

Basic Comparator



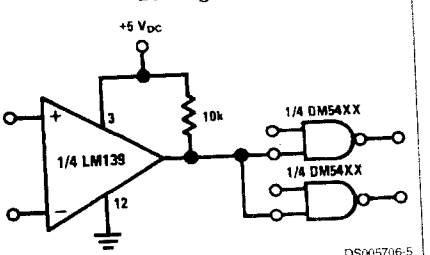
DS005706-3

Driving CMOS



DS005706-4

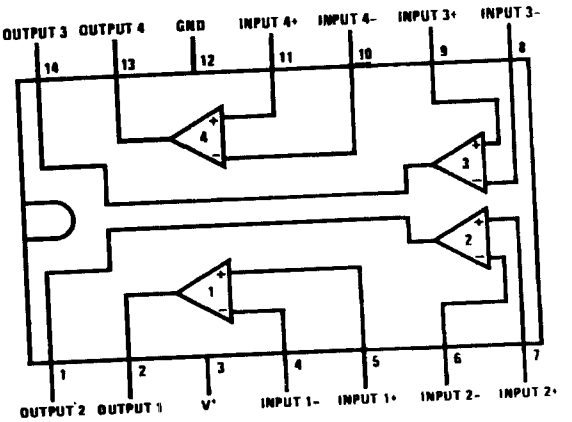
Driving TTL



DS005706-5

Connection Diagrams

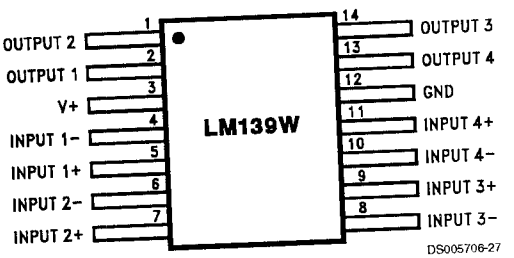
Dual-In-Line Package



TOP VIEW

DS005706-2

Order Number LM139J, LM139J/883 (Note 11), **LM139AJ, LM139AJ/883** (Note 12), **LM239J, LM239AJ, LM339J**
See NS Package Number J14A
Order Number LM339AM, LM339AMX, LM339M, LM339MX or LM2901M
See NS Package Number M14A
Order Number LM339N, LM339AN, LM2901N or LM3302N
See NS Package Number N14A



DS005706-27

Order Number LM139AW/883 or LM139W/883 (Note 11)
See NS Package Number W14B,
LM139AWGRQMLV (Note 13)
See NS Package Number WG14A

Note 11: Available per JM38510/11201

Note 12: Available per SMD# 5962-8873901

Note 13: See STD Mil Dwg 5962R96738 for Radiation Tolerant Device

SFH600

TRIOS® Phototransistor Optocoupler

TURES

- **gh Current Transfer Ratios**
- **FH600-0, 40 to 80%**
- **FH600-1, 63 to 125%**
- **FH600-2, 100 to 200%**
- **FH600-3, 160 to 320%**
- **olation Test Voltage (1.0 s), 5300 V_{RMS}**
- **$_{CEsat}$ 0.25 (≤0.4) V, I_F=10 mA, I_C=2.5 mA**
- **gh Quality Premium Device**
- **ong Term Stability**
- **torage Temperature, –55° to +150°C**
- **eld Effect Stable by TRIOS (TRansparent n Shield)**
- **nderwriters Lab File #E52744**
- **VDE 0884 Available with Option 1**

SCRIPTION

SFH600 is an optocoupler with a GaAs LED emit- which is optically coupled with a silicon planar pho- nsistor detector. The component is packaged in a tic plug-in case, 20 AB DIN 41866.

coupler transmits signals between two electri- y isolated circuits. The potential difference ween the circuits to be coupled is not allowed to eed the maximum permissible insulating voltage.

ximum Ratings

itter

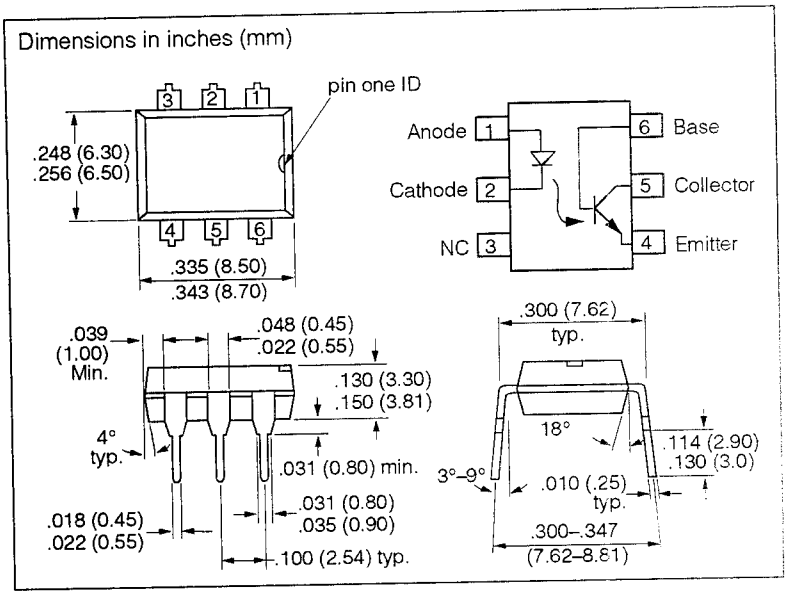
verse Voltage ..... 6.0 V
Forward Current ..... 60 mA
ge Forward Current (t_p=10 µs) ..... 2.5 A
al Power Dissipation ..... 100 mW

tector

llector-Emitter Voltage ..... 70 V
itter-Base Voltage ..... 7.0 V
llector Currentt ..... 50 mA
llector Current (t=1 ms) ..... 100 mA
wer Dissipation ..... 150 mW

ckage

lation Test Voltage (between emitter and detector referred to climate DIN 40046, part 2, Nov. 74) (t=1.0 s) ..... 5300 V_{RMS}
eepage ..... ≥7.0 mm
earance ..... ≥7.0 mm
lation Thickness between Emitter & tector ..... ≥0.4 mm
mparative Tracking Index per DIN IEC 112/VDE0303, part 1 175
lation Resistance
V_{IO}=500 V, T_A=25°C ..... ≥10^{12} Ω
V_{IO}=500 V, T_A=100°C ..... ≥10^{11} Ω
orage Temperature Range ..... –55°C to +150°C
bient Temperature Range ..... –55°C to +100°C



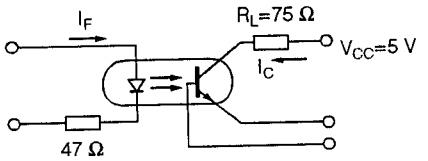
Characteristics (T_A=25°C)

	Symbol		Unit	Condition
Emitter				
Forward Voltage	V_F	1.25 (≤1.65)	V	I_F=60 mA
Breakdown Voltage	V_{BR}	≥6.0		I_R=10 µA
Reverse Current	I_R	0.01 (≤10)	µA	V_R=6.0 V
Capacitance	C_O	25	pF	V_F=0 V f=1.0 MHz
Thermal Resistance	R_{THJamb}	750	K/W	—
Detector				
Capacitance Collector-Emitter Collector-Base Emitter-Base	 C_{CE} C_{CB} C_{EB}	 5.2 6.5 9.5	pF	f=1.0 MHz V_{CE}=5.0 V V_{CB}=5.0 V V_{EB}=5.0 V
Thermal Resistance	R_{THJamb}	500	K/W	—
Package				
Saturation Voltage, Collector-Emitter	V_{CEsat}	0.25 (≤0.4)	V	I_F=10 mA, I_C=2.5 mA
Coupling Capacitance	C_{IO}	0.6	pF	V_{IO}=0 f=1.0 MHz

1. Current Transfer Ratio and Collector-emitter Leakage Current ash Number

ameter	Dash No.				Unit	Condition
	-0	-1	-2	-3		
at V_{CE}=5.0 V	40-80	63-125	100-200	160-320	%	I_F=10 mA
at V_{CE}=5.0 V	30 (>13)	45 (>22)	70 (>34)	90 (>56)		I_F=1.0 mA
ector-Emitter kage Current O)	2.0 (≤35)	2.0 (≤35)	2.0 (≤35)	5.0 (≤70)	nA	V_{CE}=10 V

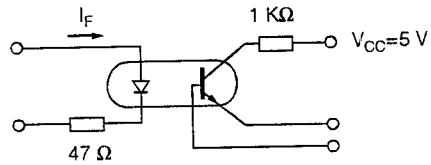
re 1. Linear Operation (without saturation)



10 mA, V_{CC}=5.0 V, T_A=25°C, Typical

ad Resistance	R_L	75	Ω
rn-On Time	t_{ON}	3.2	µs
se Time	t_R	2.0	
rn-Off Time	t_{OFF}	3.0	
ll Time	t_f	2.5	
ut-off Frequency	F_{CO}	250	kHz

ure 2. Switching Operation (with saturation)



ble 2. Typical

arameter		Dash No.			Unit
		-0 (I_F=20 mA)	-1 and -2 (I_F=10 mA)	-3 (I_F=5.0 mA)	
urn-On Time	t_{ON}	3.7	4.5	5.8	µs
ise Time	t_R	2.5	3.0	4.0	
urn-Off Time	t_{OFF}	19	21	24	
all Time	t_F	11	12	14	
	V_{CESAT}	0.25 (≤0.4)			V

Figure 3. Current Transfer Ratio versus Diode Current (T_A=–25°C, V_{CE}=5.0 V)
I_C/I_F=f (I_F)

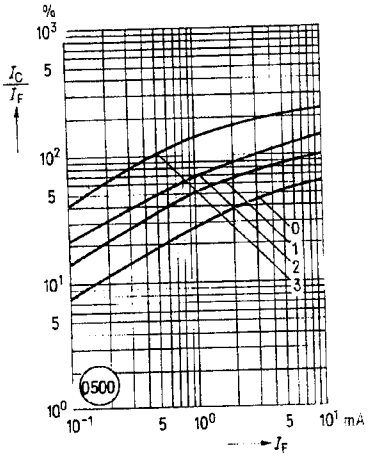


Figure 4. Current Transfer Ratio versus Diode Current (T_A=0°C, V_{CE}=5.0 V)
I_C/I_F=f (I_F)

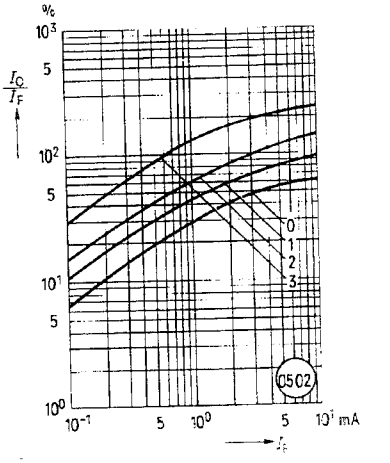
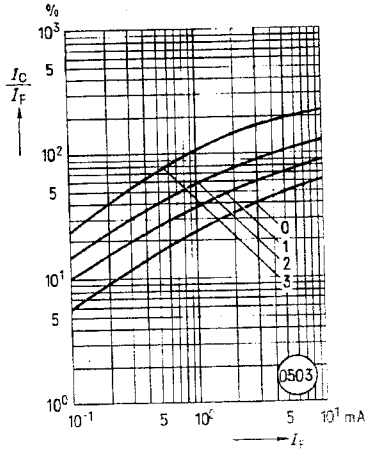
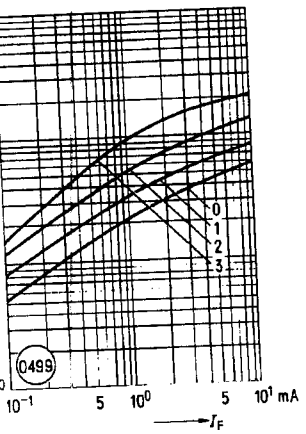


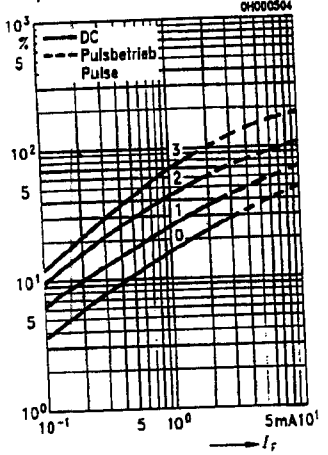
Figure 5. Current Transfer Ratio versus Diode Current (T_A=25°C, V_{CE}=5.0 V)
I_C/I_F=f (I_F)



6. Current Transfer Ratio versus Current (T_A=50°C, V_{CE}=5.0 V) (I_F)



re 7. Current Transfer Ratio versus e Current (T_A=75°C, V_{CE}=5.0 V) =f (I_F)



ure 8. Current Transfer Ratio rsus Temperature (I_F=10 mA, E=5.0 V) I_C/I_F=f(T)

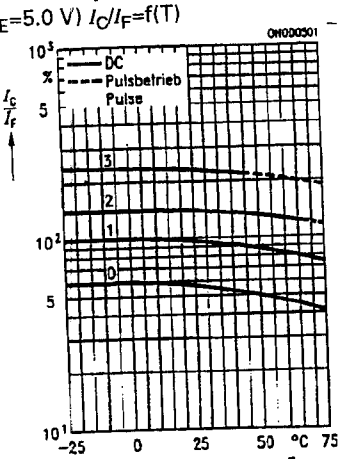


Figure 9. Transistor Characteristics (HFE =550) SFH600-2, -3 I_C=f(V_{CE}) (T_A=25°C, I_F=0)

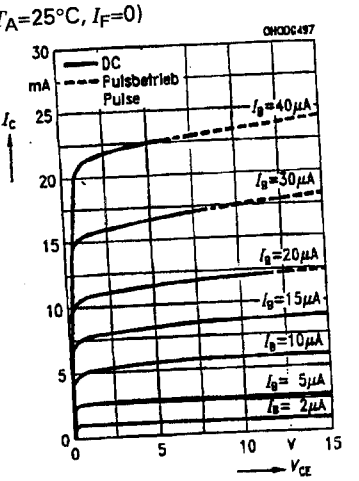


Figure 10. Output Characteristics SFH600-2, -3 (T_A=25°C) I_C=f(V_{CE})

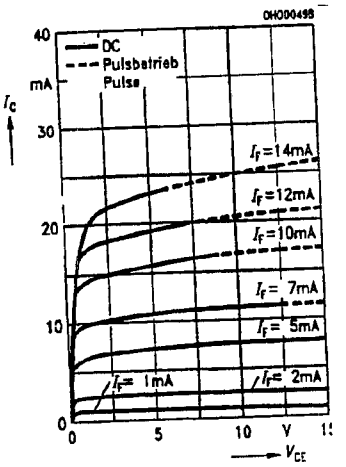


Figure 11. Forward Voltage V_F=f (I_F)

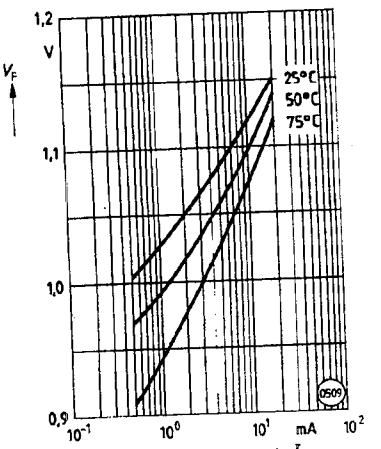


Figure 12. Collector Emitter Off-state Current I_{CEO}=f (V, T) (T_A=25°C, I_F=0)

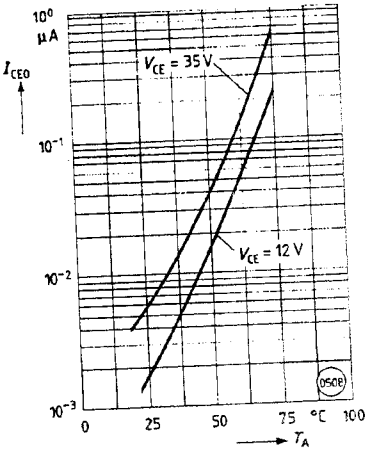


Figure 13. Saturation Voltage versus Collector Current and Modulation Depth SFH600-0 V_{CEsat}=f (I_C) (T_A=25°C)

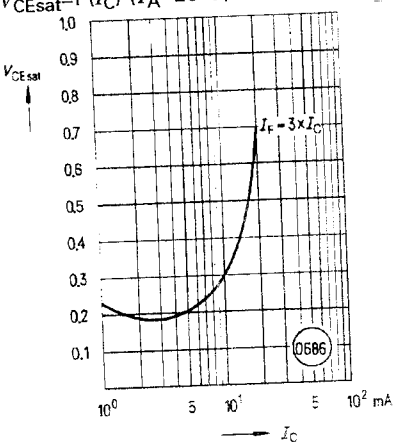


Figure 14. Saturation Voltage versus Collector Current and Modulation Depth SFH600-1 V_{CEsat}=f (I_C) (T_A=25°C)

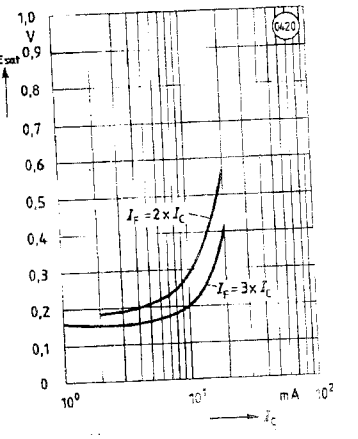


Figure 15. Saturation Voltage versus Collector Current and Modulation with SFH600-2 V_{CEsat}=f (I_C) (T_A=25°C)

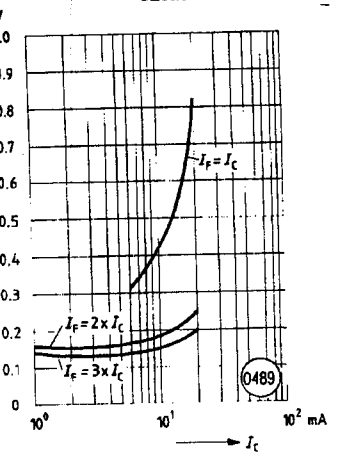


Figure 16. Saturation Voltage versus Collector Current and Modulation with SFH600-3 V_{CEsat}=f (I_C) (T_A=25°C)

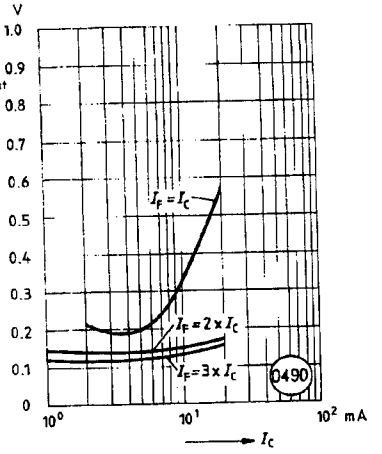


Figure 17. Permissible Pulse Load D=parameter, T_A=25°C, I_F=f (t_p)

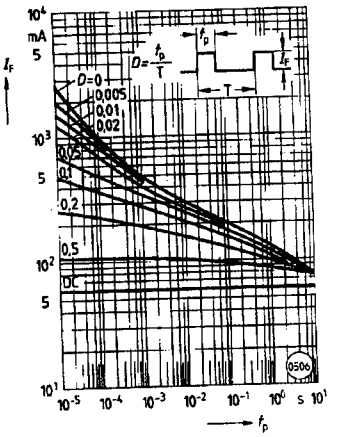


Figure 18. Permissible Power Dissipation for Transistor and Diode P_{tot}=f (T_A)

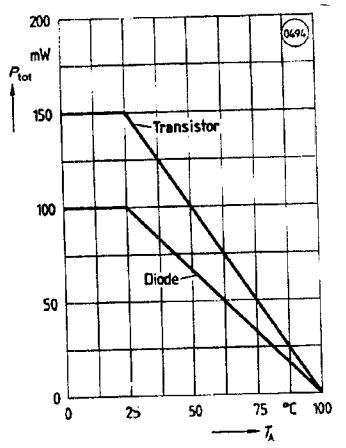


Figure 19. Permissible Forward Current Diode P_{tot}=f (T_A)

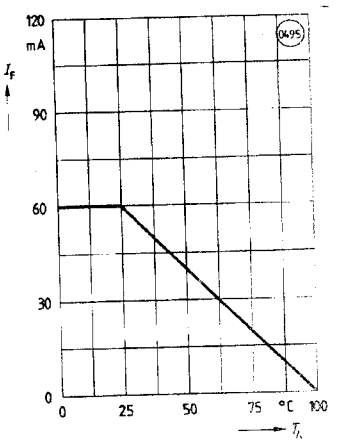
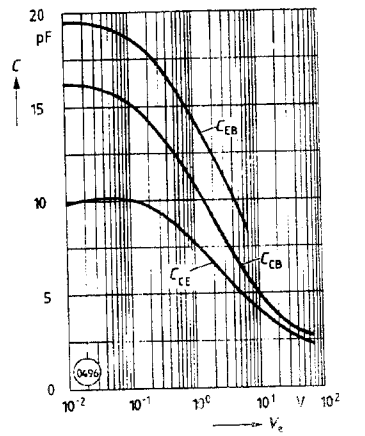


Figure 20. Transistor Capacitance C=f(V_O) (T_A=25°C, f=1.0 MHz)



22; Rev 6; 10/01

MAXIM

Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

General Description

MAX481, MAX483, MAX485, MAX487–MAX491, and X1487 are low-power transceivers for RS-485 and RS- communication. Each part contains one driver and one eiver. The MAX483, MAX487, MAX488, and MAX489 ure reduced slew-rate drivers that minimize EMI and uce reflections caused by improperly terminated cables, s allowing error-free data transmission up to 250kbps. driver slew rates of the MAX481, MAX485, MAX490, X491, and MAX1487 are not limited, allowing them to smit up to 2.5Mbps.

ese transceivers draw between 120µA and 500µA of pply current when unloaded or fully loaded with disabled vers. Additionally, the MAX481, MAX483, and MAX487 ve a low-current shutdown mode in which they consume y 0.1µA. All parts operate from a single 5V supply.

vers are short-circuit current limited and are protected ainst excessive power dissipation by thermal shutdown cuitry that places the driver outputs into a high-imped- ce state. The receiver input has a fail-safe feature that arantees a logic-high output if the input is open circuit.

e MAX487 and MAX1487 feature quarter-unit-load ceiver input impedance, allowing up to 128 MAX487/ AX1487 transceivers on the bus. Full-duplex communi- tions are obtained using the MAX488–MAX491, while e MAX481, MAX483, MAX485, MAX487, and MAX1487 e designed for half-duplex applications.

Applications

Low-Power RS-485 Transceivers

Low-Power RS-422 Transceivers

Level Translators

Transceivers for EMI-Sensitive Applications

Industrial-Control Local Area Networks

Features

- **In µMAX Package: Smallest 8-Pin SO**
- **Slew-Rate Limited for Error-Free Data Transmission (MAX483/487/488/489)**
- **0.1µALow-Current Shutdown Mode (MAX481/483/487)**
- **Low Quiescent Current:**
  120µA (MAX483/487/488/489)
  230µA (MAX1487)
  300µA (MAX481/485/490/491)
- **-7V to +12V Common-Mode Input Voltage Range**
- **Three-State Outputs**
- **30ns Propagation Delays, 5ns Skew (MAX481/485/490/491/1487)**
- **Full-Duplex and Half-Duplex Versions Available**
- **Operate from a Single 5V Supply**
- **Allows up to 128 Transceivers on the Bus (MAX487/MAX1487)**
- **Current-Limiting and Thermal Shutdown for Driver Overload Protection**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX481CPA	0°C to +70°C	8 Plastic DIP
MAX481CSA	0°C to +70°C	8 SO
MAX481CUA	0°C to +70°C	8 µMAX
MAX481C/D	0°C to +70°C	Dice*

Ordering Information continued at end of data sheet.

**Contact factory for dice specifications.*

Selection Table

PART NUMBER	HALF/FULL DUPLEX	DATA RATE (Mbps)	SLEW-RATE LIMITED	LOW-POWER SHUTDOWN	RECEIVER/ DRIVER ENABLE	QUIESCENT CURRENT (µA)	NUMBER OF TRANSMITTERS ON BUS	PIN COUNT
MAX481	Half	2.5	No	Yes	Yes	300	32	8
MAX483	Half	0.25	Yes	Yes	Yes	120	32	8
MAX485	Half	2.5	No	No	Yes	300	32	8
MAX487	Half	0.25	Yes	Yes	Yes	120	128	8
MAX488	Full	0.25	Yes	No	No	120	32	8
MAX489	Full	0.25	Yes	No	Yes	120	32	14
MAX490	Full	2.5	No	No	No	300	32	8
MAX491	Full	2.5	No	No	Yes	300	32	14
MAX1487	Half	2.5	No	No	Yes	230	128	8

ow-Power, Slew-Rate-Limited
S-485/RS-422 Transceivers

SOLUTE MAXIMUM RATINGS

y Voltage (Vcc) 12V
ol Input Voltage (RE, DE) ..... -0.5V to (Vcc + 0.5V)
Input Voltage (DI) ..... -0.5V to (Vcc + 0.5V)
Output Voltage (A, B) ..... -8V to +12.5V
iver Input Voltage (A, B) ..... -8V to +12.5V
iver Output Voltage (RO) ..... -0.5V to (Vcc +0.5V)
nuous Power Dissipation (TA = +70°C)
in Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
Pin Plastic DIP (derate 10.00mW/°C above +70°C) ..800mW
in SO (derate 5.88mW/°C above +70°C) 471mW
14-Pin SO (derate 8.33mW/°C above +70°C) 667mW
8-Pin µMAX (derate 4.1mW/°C above +70°C) 830mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW
14-Pin CERDIP (derate 9.09mW/°C above +70°C) 727mW
Operating Temperature Ranges
MAX4_ _C_ _/MAX1487C_ A ..... 0°C to +70°C
MAX4_ _E_ _/MAX1487E_ A ..... -40°C to +85°C
MAX4_ _MJ_/MAX1487MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

ses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional ation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to lute maximum rating conditions for extended periods may affect device reliability.

C ELECTRICAL CHARACTERISTICS

c = 5V ±5%, TA = TMIN to TMAX, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ferential Driver Output (no load)	VOD1					5	V
ferential Driver Output th load)	VOD2	R = 50Ω (RS-422)		2			V
		R = 27Ω (RS-485), Figure 4		1.5		5	
hange in Magnitude of Driver fferential Output Voltage for omplementary Output States	ΔVOD	R = 27Ω or 50Ω, Figure 4				0.2	V
river Common-Mode Output oltage	VOC	R = 27Ω or 50Ω, Figure 4				3	V
hange in Magnitude of Driver ommon-Mode Output Voltage or Complementary Output States	ΔVOD	R = 27Ω or 50Ω, Figure 4				0.2	V
nput High Voltage	VIH	DE, DI, RE		2.0			V
nput Low Voltage	VIL	DE, DI, RE				0.8	V
nput Current	IIN1	DE, DI, RE				±2	µA
nput Current (A, B)	IIN2	DE = 0V; VCC = 0V or 5.25V, all devices except MAX487/MAX1487	VIN = 12V			1.0	mA
			VIN = -7V			-0.8	
		MAX487/MAX1487, DE = 0V, VCC = 0V or 5.25V	VIN = 12V			0.25	mA
			VIN = -7V			-0.2	
Receiver Differential Threshold Voltage	VTH	-7V ≤ VCM ≤ 12V		-0.2		0.2	V
Receiver Input Hysteresis	ΔVTH	VCM = 0V			70		mV
Receiver Output High Voltage	VOH	IO = -4mA, VID = 200mV		3.5			V
Receiver Output Low Voltage	VOL	IO = 4mA, VID = -200mV				0.4	V
Three-State (high impedance) Output Current at Receiver	IOZR	0.4V ≤ VO ≤ 2.4V				±1	µA
Receiver Input Resistance	RIN	-7V ≤ VCM ≤ 12V, all devices except MAX487/MAX1487		12			kΩ
		-7V ≤ VCM ≤ 12V, MAX487/MAX1487		48			kΩ

ELECTRICAL CHARACTERISTICS (continued)

(VCC = 5V ±5%, TA = TMIN to TMAX, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
o-Load Supply Current (lote 3)	ICC	MAX488/MAX489, DE, DI, $\overline{RE}$ = 0V or VCC				120	250	µA
		MAX490/MAX491, DE, DI, $\overline{RE}$ = 0V or VCC				300	500	
		MAX481/MAX485, $\overline{RE}$ = 0V or VCC	DE = VCC			500	900	
			DE = 0V			300	500	
		MAX1487, $\overline{RE}$ = 0V or VCC	DE = VCC			300	500	
			DE = 0V			230	400	
		MAX483/MAX487, $\overline{RE}$ = 0V or VCC	DE = 5V	MAX483		350	650	
				MAX487		250	400	
			DE = 0V			120	250	
upply Current in Shutdown	ISHDN	MAX481/483/487, DE = 0V, $\overline{RE}$ = VCC				0.1	10	µA
river Short-Circuit Current, O = High	IOSD1	-7V ≤ VO ≤12V (Note 4)			35		250	mA
river Short-Circuit Current, O = Low	IOSD2	-7V ≤ VO ≤12V (Note 4)			35		250	mA
eceiver Short-Circuit Current	IOSR	0V ≤ VO ≤ VCC			7		95	mA

WITCHING CHARACTERISTICS—MAX481/MAX485, MAX490/MAX491, MAX1487

(CC = 5V ±5%, TA = TMIN to TMAX, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
river Input to Output	tPLH	Figures 6 and 8, RDIFF = 54Ω, CL1 = CL2 = 100pF		10	30	60	ns
	tPHL			10	30	60	
river Output Skew to Output	tSKEW	Figures 6 and 8, RDIFF = 54Ω, CL1 = CL2 = 100pF			5	10	ns
Driver Rise or Fall Time	tR, tF	Figures 6 and 8, RDIFF = 54Ω, CL1 = CL2 = 100pF	MAX481, MAX485, MAX1487	3	15	40	ns
			MAX490C/E, MAX491C/E	5	15	25	
			MAX490M, MAX491M	3	15	40	
Driver Enable to Output High	tZH	Figures 7 and 9, CL = 100pF, S2 closed			40	70	ns
Driver Enable to Output Low	tZL	Figures 7 and 9, CL = 100pF, S1 closed			40	70	ns
Driver Disable Time from Low	tLZ	Figures 7 and 9, CL = 15pF, S1 closed			40	70	ns
Driver Disable Time from High	tHZ	Figures 7 and 9, CL = 15pF, S2 closed			40	70	ns
Receiver Input to Output	tPLH, tPHL	Figures 6 and 10, RDIFF = 54Ω, CL1 = CL2 = 100pF	MAX481, MAX485, MAX1487	20	90	200	ns
			MAX490C/E, MAX491C/E	20	90	150	
			MAX490M, MAX491M	20	90	200	
| tPLH - tPHL | Differential Receiver Skew	tSKD	Figures 6 and 10, RDIFF = 54Ω, CL1 = CL2 = 100pF			13		ns
Receiver Enable to Output Low	tZL	Figures 5 and 11, CRL = 15pF, S1 closed			20	50	ns
Receiver Enable to Output High	tZH	Figures 5 and 11, CRL = 15pF, S2 closed			20	50	ns
Receiver Disable Time from Low	tLZ	Figures 5 and 11, CRL = 15pF, S1 closed			20	50	ns
Receiver Disable Time from High	tHZ	Figures 5 and 11, CRL = 15pF, S2 closed			20	50	ns
Maximum Data Rate	fMAX			2.5			Mbps
Time to Shutdown	tSHDN	MAX481 (Note 5)		50	200	600	ns

ow-Power, Slew-Rate-Limited S-485/RS-422 Transceivers

WITCHING CHARACTERISTICS—MAX481/MAX485, MAX490/MAX491, MAX1487 (continued)

c = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
iver Enable from Shutdown to utput High (MAX481)	$t_{ZH(SHDN)}$	Figures 7 and 9, C_L = 100pF, S2 closed		40	100	ns
iver Enable from Shutdown to utput Low (MAX481)	$t_{ZL(SHDN)}$	Figures 7 and 9, C_L = 100pF, S1 closed		40	100	ns
eceiver Enable from Shutdown Output High (MAX481)	$t_{ZH(SHDN)}$	Figures 5 and 11, C_L = 15pF, S2 closed, A - B = 2V		300	1000	ns
eceiver Enable from Shutdown Output Low (MAX481)	$t_{ZL(SHDN)}$	Figures 5 and 11, C_L = 15pF, S1 closed, B - A = 2V		300	1000	ns

WITCHING CHARACTERISTICS—MAX483, MAX487/MAX488/MAX489

CC = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output	t_{PLH}	Figures 6 and 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250	800	2000	ns
	t_{PHL}		250	800	2000	
Driver Output Skew to Output	t_{SKEW}	Figures 6 and 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		100	800	ns
Driver Rise or Fall Time	t_R, t_F	Figures 6 and 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250		2000	ns
Driver Enable to Output High	t_{ZH}	Figures 7 and 9, C_L = 100pF, S2 closed	250		2000	ns
Driver Enable to Output Low	t_{ZL}	Figures 7 and 9, C_L = 100pF, S1 closed	250		2000	ns
Driver Disable Time from Low	t_{LZ}	Figures 7 and 9, C_L = 15pF, S1 closed	300		3000	ns
Driver Disable Time from High	t_{HZ}	Figures 7 and 9, C_L = 15pF, S2 closed	300		3000	ns
Receiver Input to Output	t_{PLH}	Figures 6 and 10, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250		2000	ns
	t_{PHL}		250		2000	
| t_{PLH} - t_{PHL} | Differential Receiver Skew	t_{SKD}	Figures 6 and 10, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		100		ns
Receiver Enable to Output Low	t_{ZL}	Figures 5 and 11, C_{RL} = 15pF, S1 closed		20	50	ns
Receiver Enable to Output High	t_{ZH}	Figures 5 and 11, C_{RL} = 15pF, S2 closed		20	50	ns
Receiver Disable Time from Low	t_{LZ}	Figures 5 and 11, C_{RL} = 15pF, S1 closed		20	50	ns
Receiver Disable Time from High	t_{HZ}	Figures 5 and 11, C_{RL} = 15pF, S2 closed		20	50	ns
Maximum Data Rate	f_{MAX}	t_{PLH}, t_{PHL} < 50% of data period	250			kbps
Time to Shutdown	t_{SHDN}	MAX483/MAX487 (Note 5)	50	200	600	ns
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	MAX483/MAX487, Figures 7 and 9, C_L = 100pF, S2 closed			2000	ns
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	MAX483/MAX487, Figures 7 and 9, C_L = 100pF, S1 closed			2000	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	MAX483/MAX487, Figures 5 and 11, C_L = 15pF, S2 closed			2500	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	MAX483/MAX487, Figures 5 and 11, C_L = 15pF, S1 closed			2500	ns

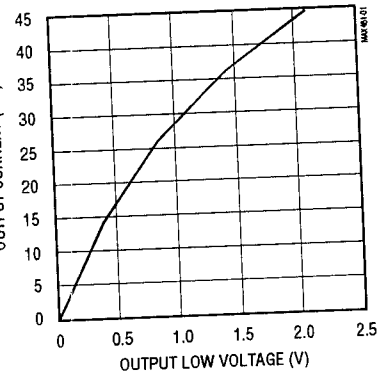
TES FOR ELECTRICAL/SWITCHING CHARACTERISTICS

1: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
2: All typical specifications are given for V_{CC} = 5V and T_A = +25°C.
3: Supply current specification is valid for loaded transmitters when DE = 0V.
4: Applies to peak current. See *Typical Operating Characteristics.*
5: The MAX481/MAX483/MAX487 are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 50ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 600ns, the parts are guaranteed to have entered shutdown. See *Low-Power Shutdown Mode* section.

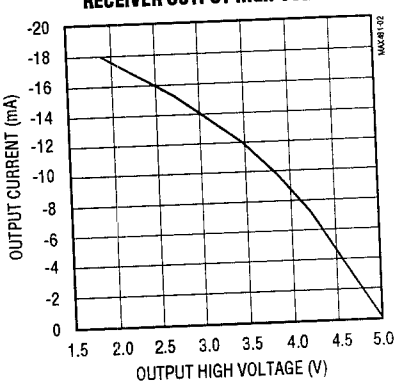
Typical Operating Characteristics

C = 5V, T_A = +25°C, unless otherwise noted.)

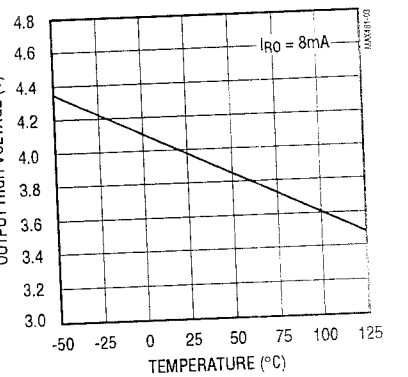
OUTPUT CURRENT vs. RECEIVER OUTPUT LOW VOLTAGE



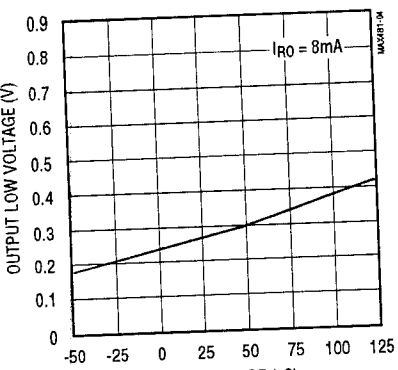
OUTPUT CURRENT vs. RECEIVER OUTPUT HIGH VOLTAGE



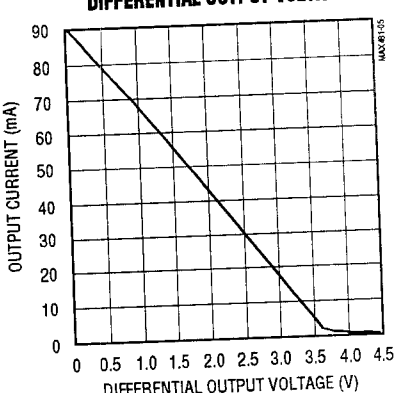
RECEIVER OUTPUT HIGH VOLTAGE vs. TEMPERATURE



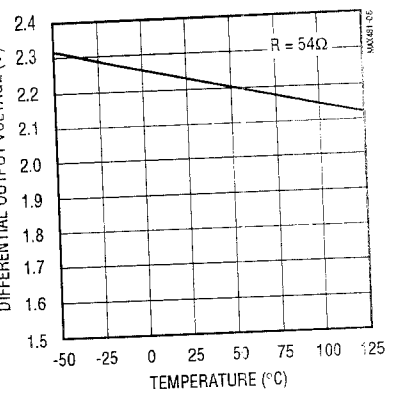
RECEIVER OUTPUT LOW VOLTAGE vs. TEMPERATURE



DRIVER OUTPUT CURRENT vs. DIFFERENTIAL OUTPUT VOLTAGE



DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE

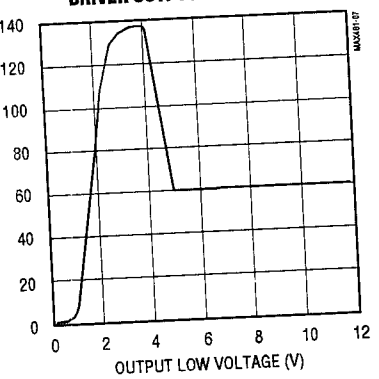


ow-Power, Slew-Rate-Limited
S-485/RS-422 Transceivers

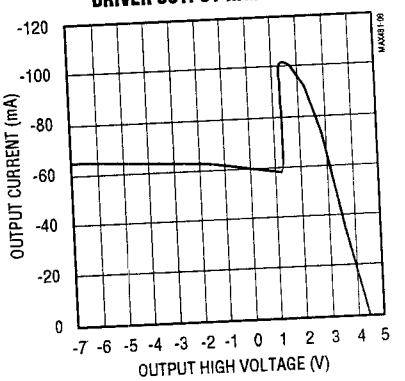
Typical Operating Characteristics (continued)

= 5V, T_A = +25°C, unless otherwise noted.)

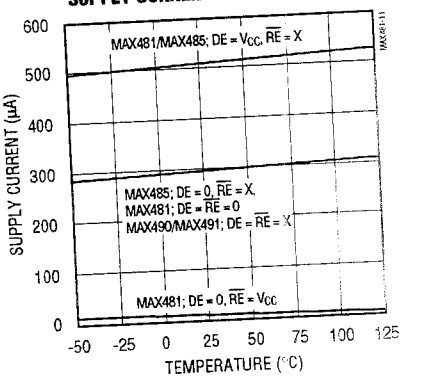
OUTPUT CURRENT vs. DRIVER OUTPUT LOW VOLTAGE



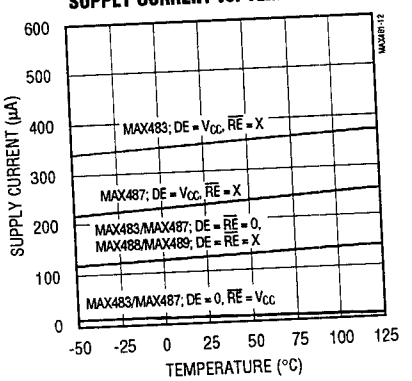
OUTPUT CURRENT vs. DRIVER OUTPUT HIGH VOLTAGE



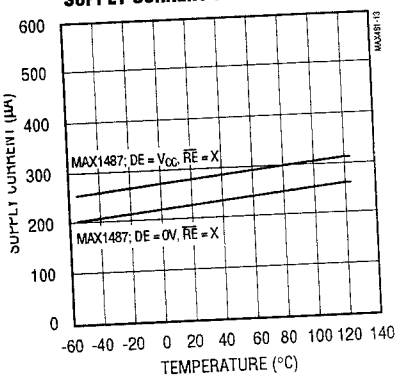
MAX481/MAX485/MAX490/MAX491 SUPPLY CURRENT vs. TEMPERATURE



MAX483/MAX487–MAX489 SUPPLY CURRENT vs. TEMPERATURE



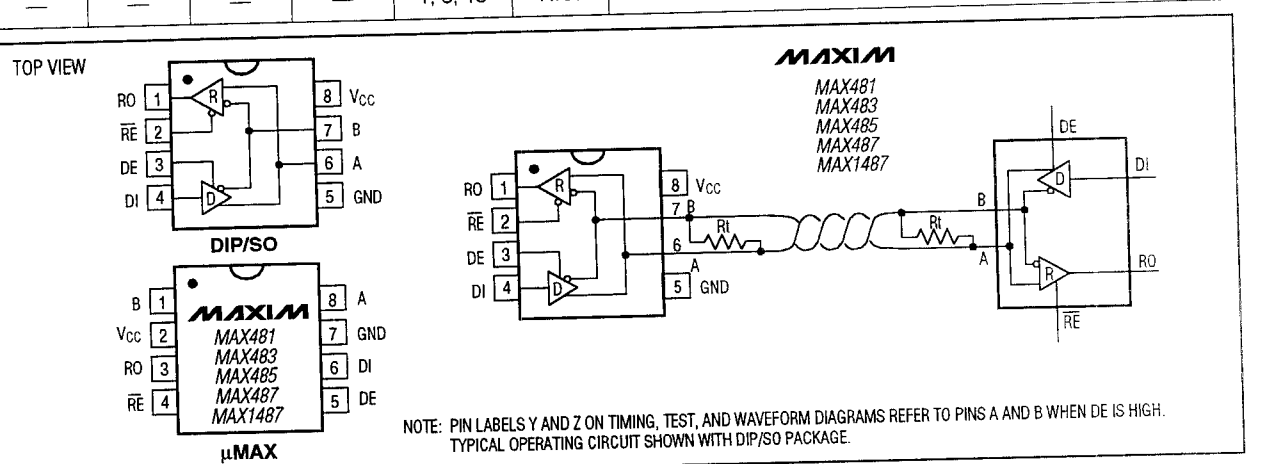
MAX1487 SUPPLY CURRENT vs. TEMPERATURE



Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

Pin Description

PIN					NAME	FUNCTION
AX481/MAX483/ AX485/MAX487/ MAX1487		MAX488/ MAX490		MAX489/ MAX491		
P/SO	µMAX	DIP/SO	µMAX	DIP/SO		
1	3	2	4	2	RO	Receiver Output: If A > B by 200mV, RO will be high; If A < B by 200mV, RO will be low.
2	4	—	—	3	$\overline{RE}$	Receiver Output Enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high.
3	5	—	—	4	DE	Driver Output Enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low. If the driver outputs are enabled, the parts function as line drivers. While they are high impedance, they function as line receivers if $\overline{RE}$ is low.
4	6	3	5	5	DI	Driver Input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
5	7	4	6	6, 7	GND	Ground
—	—	5	7	9	Y	Noninverting Driver Output
—	—	6	8	10	Z	Inverting Driver Output
6	8	—	—	—	A	Noninverting Receiver Input and Noninverting Driver Output
—	—	8	2	12	A	Noninverting Receiver Input
7	1	—	—	—	B	Inverting Receiver Input and Inverting Driver Output
—	—	7	1	11	B	Inverting Receiver Input
8	2	1	3	14	Vcc	Positive Supply: 4.75V ≤ Vcc ≤ 5.25V
—	—	—	—	1, 8, 13	N.C.	No Connect—not internally connected



NOTE: PIN LABELS Y AND Z ON TIMING, TEST, AND WAVEFORM DIAGRAMS REFER TO PINS A AND B WHEN DE IS HIGH. TYPICAL OPERATING CIRCUIT SHOWN WITH DIP/SO PACKAGE.

Figure 1. MAX481/MAX483/MAX485/MAX487/MAX1487 Pin Configuration and Typical Operating Circuit

ow-Power, Slew-Rate-Limited
S-485/RS-422 Transceivers

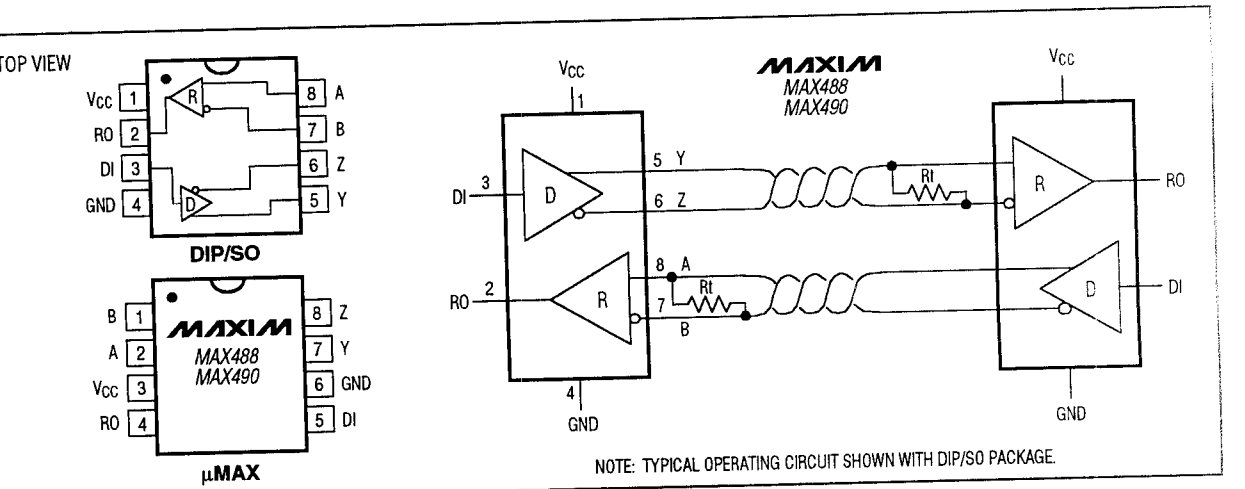


Figure 2. MAX488/MAX490 Pin Configuration and Typical Operating Circuit

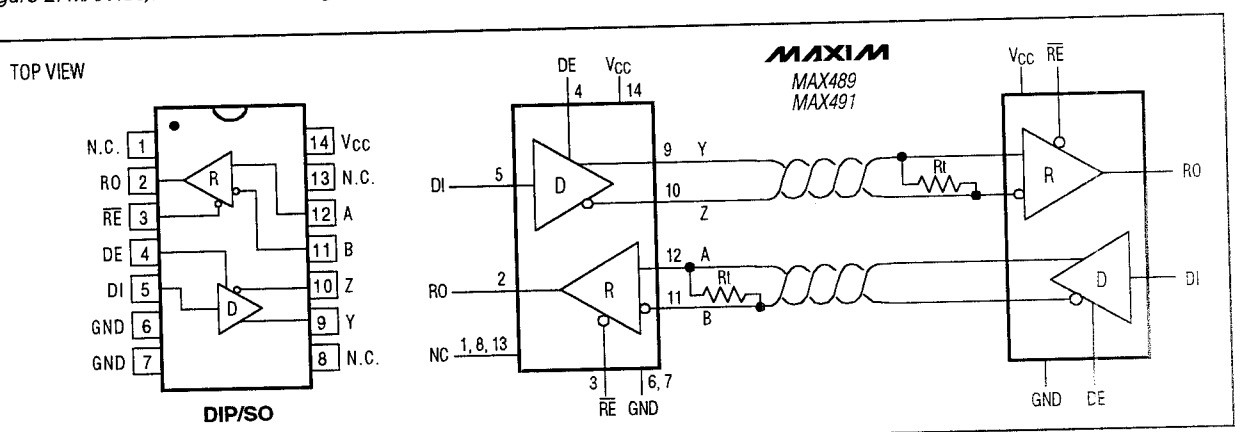


Figure 3. MAX489/MAX491 Pin Configuration and Typical Operating Circuit

Applications Information

The MAX481/MAX483/MAX485/MAX487–MAX491 and MAX1487 are low-power transceivers for RS-485 and RS-422 communications. The MAX481, MAX485, MAX490, MAX491, and MAX1487 can transmit and receive at data rates up to 2.5Mbps, while the MAX483, MAX487, MAX488, and MAX489 are specified for data rates up to 250kbps. The MAX488–MAX491 are full-duplex transceivers while the MAX481, MAX483, MAX485, MAX487, and MAX1487 are half-duplex. In addition, Driver Enable (DE) and Receiver Enable (RE) pins are included on the MAX481, MAX483, MAX485, MAX487, MAX489, MAX491, and MAX1487. When disabled, the driver and receiver outputs are high impedance.

MAX487/MAX1487: 128 Transceivers on the Bus

The 48kΩ, 1/4-unit-load receiver input impedance of the MAX487 and MAX1487 allows up to 128 transceivers on a bus, compared to the 1-unit load (12kΩ input impedance) of standard RS-485 drivers (32 transceivers maximum). Any combination of MAX487/MAX1487 and other RS-485 transceivers with a total of 32 unit loads or less can be put on the bus. The MAX481/MAX483/MAX485 and MAX488–MAX491 have standard 12kΩ Receiver Input impedance.

23; Rev 10; 8/01

MAXIM

+5V-Powered, Multichannel RS-232 Drivers/Receivers

General Description

MAX220–MAX249 family of line drivers/receivers is ided for all EIA/TIA-232E and V.28/V.24 communica- interfaces, particularly applications where ±12V is available.

se parts are especially useful in battery-powered sys- s, since their low-power shutdown mode reduces ver dissipation to less than 5µW. The MAX225, X233, MAX235, and MAX245/MAX246/MAX247 use external components and are recommended for appli- ons where printed circuit board space is critical.

Applications

Portable Computers

Low-Power Modems

Interface Translation

Battery-Powered RS-232 Systems

Multidrop RS-232 Networks

Features

Superior to Bipolar

- ♦ **Operate from Single +5V Power Supply (+5V and +12V—MAX231/MAX239)**
- ♦ **Low-Power Receive Mode in Shutdown (MAX223/MAX242)**
- ♦ **Meet All EIA/TIA-232E and V.28 Specifications**
- ♦ **Multiple Drivers and Receivers**
- ♦ **3-State Driver and Receiver Outputs**
- ♦ **Open-Line Detection (MAX243)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX220CPE	0°C to +70°C	16 Plastic DIP
MAX220CSE	0°C to +70°C	16 Narrow SO
MAX220CWE	0°C to +70°C	16 Wide SO
MAX220C/D	0°C to +70°C	Dice*
MAX220EPE	-40°C to +85°C	16 Plastic DIP
MAX220ESE	-40°C to +85°C	16 Narrow SO
MAX220EWE	-40°C to +85°C	16 Wide SO
MAX220EJE	-40°C to +85°C	16 CERDIP
MAX220MJE	-55°C to +125°C	16 CERDIP

Ordering Information continued at end of data sheet.

**Contact factory for dice specifications.*

Selection Table

rt umber	Power Supply (V)	No. of RS-232 Drivers/Rx	No. of Ext. Caps	Nominal Cap. Value (µF)	SHDN & Three-State	Rx Active in SHDN	Data Rate (kbps)	Features
AX220	+5	2/2	4	0.1	No	—	120	Ultra-low-power, industry-standard pinout
AX222	+5	2/2	4	0.1	Yes	—	200	Low-power shutdown
AX223 (MAX213)	+5	4/5	4	1.0 (0.1)	Yes	✔	120	MAX241 and receivers active in shutdown
AX225	+5	5/5	0	—	Yes	✔	120	Available in SO
AX230 (MAX200)	+5	5/0	4	1.0 (0.1)	Yes	—	120	5 drivers with shutdown
AX231 (MAX201)	+5 and +7.5 to +13.2	2/2	2	1.0 (0.1)	No	—	120	Standard +5/+12V or battery supplies; same functions as MAX232
AX232 (MAX202)	+5	2/2	4	1.0 (0.1)	No	—	120 (64)	Industry standard
AX232A	+5	2/2	4	0.1	No	—	200	Higher slew rate, small caps
AX233 (MAX203)	+5	2/2	0	—	No	—	120	No external caps
AX233A	+5	2/2	0	—	No	—	200	No external caps, high slew rate
AX234 (MAX204)	+5	4/0	4	1.0 (0.1)	No	—	120	Replaces 1488
AX235 (MAX205)	+5	5/5	0	—	Yes	—	120	No external caps
AX236 (MAX206)	+5	4/3	4	1.0 (0.1)	Yes	—	120	Shutdown, three state
AX237 (MAX207)	+5	5/3	4	1.0 (0.1)	No	—	120	Complements IBM PC serial port
AX238 (MAX208)	+5	4/4	4	1.0 (0.1)	No	—	120	Replaces 1488 and 1489
AX239 (MAX209)	+5 and +7.5 to +13.2	3/5	2	1.0 (0.1)	No	—	120	Standard +5/+12V or battery supplies; single-package solution for IBM PC serial port
AX240	+5	5/5	4	1.0	Yes	—	120	DIP or flatpack package
AX241 (MAX211)	+5	4/5	4	1.0 (0.1)	Yes	—	120	Complete IBM PC serial port
AX242	+5	2/2	4	0.1	Yes	✔	200	Separate shutdown and enable
AX243	+5	2/2	4	0.1	No	—	200	Open-line detection simplifies cabling
AX244	+5	8/10	4	1.0	No	—	120	High slew rate
AX245	+5	8/10	0	—	Yes	✔	120	High slew rate, int. caps, two shutdown modes
AX246	+5	8/10	0	—	Yes	✔	120	High slew rate, int. caps, three shutdown modes
AX247	+5	8/9	0	—	Yes	✔	120	High slew rate, int. caps, nine operating modes
AX248	+5	8/8	4	1.0	Yes	✔	120	High slew rate, selective half-chip enables
AX249	+5	6/10	4	1.0	Yes	✔	120	Available in quad flatpack package

5V-Powered, Multichannel RS-232 rivers/Receivers

SOLUTE MAXIMUM RATINGS—MAX220/222/232A/233A/242/243

oly Voltage (Vcc) .....-0.3V to +6V
t Voltages
.....-0.3V to (Vcc - 0.3V)
(Except MAX220) .....±30V
(MAX220).....±25V
UT (Except MAX220) (Note 1) .....±15V
UT (MAX220).....±13.2V
put Voltages
UT.....±15V
UT.....-0.3V to (Vcc + 0.3V)
er/Receiver Output Short Circuited to GND.....Continuous
ntinuous Power Dissipation (T_A = +70°C)
-Pin Plastic DIP (derate 10.53mW/°C above +70°C)....842mW
-Pin Plastic DIP (derate 11.11mW/°C above +70°C)....889mW
20-Pin Plastic DIP (derate 8.00mW/°C above +70°C) ..440mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) ...696mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C).....762mW
18-Pin Wide SO (derate 9.52mW/°C above +70°C).....762mW
20-Pin Wide SO (derate 10.00mW/°C above +70°C)....800mW
20-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C).....800mW
18-Pin CERDIP (derate 10.53mW/°C above +70°C).....842mW
Operating Temperature Ranges
MAX2_ _AC_ _, MAX2_ _C_ _.....0°C to +70°C
MAX2_ _AE_ _, MAX2_ _E_ _ .....-40°C to +85°C
MAX2_ _AM_ _, MAX2_ _M_ _.....-55°C to +125°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) ....+300°C

te 1: Input voltage measured with T_{OUT} in high-impedance state, $\overline{SHDN}$ or V_{CC} = 0V.

te 2: For the MAX220, V+ and V- can have a maximum magnitude of 7V, but their absolute difference cannot exceed 13V.

esses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional eration of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to solute maximum rating conditions for extended periods may affect device reliability.

LECTRICAL CHARACTERISTICS—MAX220/222/232A/233A/242/243

(CC = +5V ±10%, C1–C4 = 0.1µF, MAX220, C1 = 0.047µF, C2–C4 = 0.33µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RS-232 TRANSMITTERS						
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to GND		±5	±8		V
nput Logic Threshold Low				1.4	0.8	V
nput Logic Threshold High	All devices except MAX220		2	1.4		V
	MAX220: Vcc = 5.0V		2.4			
Logic Pull-Up/Input Current	All except MAX220, normal operation			5	40	µA
	$\overline{SHDN}$ = 0V, MAX222/242, shutdown, MAX220			±0.01	±1	
Output Leakage Current	Vcc = 5.5V, $\overline{SHDN}$ = 0V, V_{OUT} = ±15V, MAX222/242			±0.01	±10	µA
	Vcc = $\overline{SHDN}$ = 0V, V_{OUT} = ±15V			±0.01	±10	
Data Rate				200	116	kb/s
Transmitter Output Resistance	Vcc = V+ = V- = 0V, V_{OUT} = ±2V		300	10M		Ω
Output Short-Circuit Current	V_{OUT} = 0V			±7	±22	mA
RS-232 RECEIVERS						
RS-232 Input Voltage Operating Range					±30	V
RS-232 Input Threshold Low	Vcc = 5V	All except MAX243 $R2_{IN}$	0.8	1.3		V
		MAX243 $R2_{IN}$ (Note 2)	-3			
RS-232 Input Threshold High	Vcc = 5V	All except MAX243 $R2_{IN}$		1.8	2.4	V
		MAX243 $R2_{IN}$ (Note 2)		-0.5	-0.1	
RS-232 Input Hysteresis	All except MAX243, Vcc = 5V, no hysteresis in shdn.		0.2	0.5	1	V
	MAX243			1		
RS-232 Input Resistance			3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 3.2mA			0.2	0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1.0mA		3.5	Vcc - 0.2		V
TTL/CMOS Output Short-Circuit Current	Sourcing V_{OUT} = GND		-2	-10		mA
	Shrinking V_{OUT} = Vcc		10	30		

ECTRICAL CHARACTERISTICS—MAX220/222/232A/233A/242/243 (continued)

: = +5V ±10%, C1–C4 = 0.1µF, MAX220, C1 = 0.047µF, C2–C4 = 0.33µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
L/CMOS Output Leakage Current	$\overline{SHDN}$ = V_{CC} or $\overline{EN}$ = V_{CC} ($\overline{SHDN}$ = 0V for MAX222), 0V ≤ V_{OUT} ≤ V_{CC}			±0.05	±10	µA
T Input Threshold Low	MAX242			1.4	0.8	V
T Input Threshold High	MAX242		2.0	1.4		V
perating Supply Voltage			4.5		5.5	V
cc Supply Current ($\overline{SHDN}$ = V_{CC}), gures 5, 6, 11, 19	No load	MAX220		0.5	2	mA
		MAX222/232A/233A/242/243		4	10	
	3kΩ load both inputs	MAX220		12		
		MAX222/232A/233A/242/243		15		
hutdown Supply Current	MAX222/242	T_A = +25°C		0.1	10	µA
		T_A = 0°C to +70°C		2	50	
		T_A = -40°C to +85°C		2	50	
		T_A = -55°C to +125°C		35	100	
HDN Input Leakage Current	MAX222/242				±1	µA
HDN Threshold Low	MAX222/242			1.4	0.8	V
HDN Threshold High	MAX222/242		2.0	1.4		V
Transition Slew Rate	C_L = 50pF to 2500pF, R_L = 3kΩ to 7kΩ, V_{CC} = 5V, T_A = +25°C, measured from +3V to -3V or -3V to +3V	MAX222/232A/233A/242/243	6	12	30	V/µs
		MAX220	1.5	3	30	
Transmitter Propagation Delay TLL to RS-232 (normal operation), Figure 1	t_{PHLT}	MAX222/232A/233A/242/243		1.3	3.5	µs
		MAX220		4	10	
	t_{PLHT}	MAX222/232A/233A/242/243		1.5	3.5	
		MAX220		5	10	
Receiver Propagation Delay RS-232 to TLL (normal operation), Figure 2	t_{PHLR}	MAX222/232A/233A/242/243		0.5	1	µs
		MAX220		0.6	3	
	t_{PLHR}	MAX222/232A/233A/242/243		0.6	1	
		MAX220		0.8	3	
Receiver Propagation Delay RS-232 to TLL (shutdown), Figure 2	t_{PHLS}	MAX242		0.5	10	µs
	t_{PLHS}	MAX242		2.5	10	
Receiver-Output Enable Time, Figure 3	t_{ER}	MAX242		125	500	ns
Receiver-Output Disable Time, Figure 3	t_{DR}	MAX242		160	500	ns
Transmitter-Output Enable Time ($\overline{SHDN}$ goes high), Figure 4	t_{ET}	MAX222/242, 0.1µF caps (includes charge-pump start-up)		250		µs
Transmitter-Output Disable Time ($\overline{SHDN}$ goes low), Figure 4	t_{DT}	MAX222/242, 0.1µF caps		600		ns
Transmitter + to - Propagation Delay Difference (normal operation)	t_{PHLT} - t_{PLHT}	MAX222/232A/233A/242/243		300		ns
		MAX220		2000		
Receiver + to - Propagation Delay Difference (normal operation)	t_{PHLR} - t_{PLHR}	MAX222/232A/233A/242/243		100		ns
		MAX220		225		

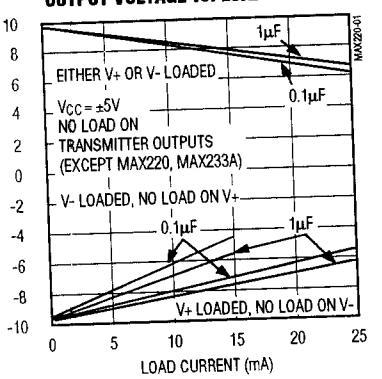
Note 3: MAX243 $R2_{OUT}$ is guaranteed to be low when $R2_{IN}$ is ≥ 0V or is floating.

5V-Powered, Multichannel RS-232 rivers/Receivers

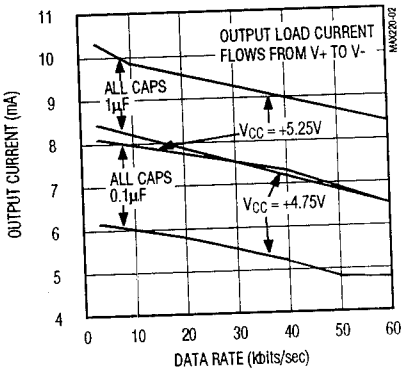
Typical Operating Characteristics

MAX220/MAX222/MAX232A/MAX233A/MAX242/MAX243

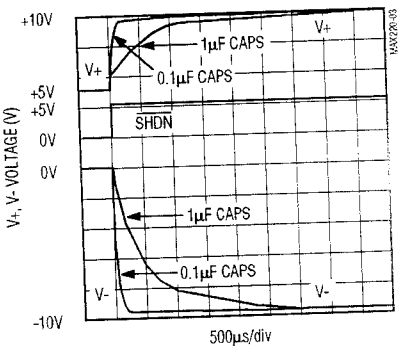
OUTPUT VOLTAGE vs. LOAD CURRENT



AVAILABLE OUTPUT CURRENT vs. DATA RATE



MAX222/MAX242 ON-TIME EXITING SHUTDOWN



+5V-Powered, Multichannel RS-232 Drivers/Receivers

BSOLUTE MAXIMUM RATINGS—MAX223/MAX230–MAX241

.....-0.3V to +6V
.....(VCC - 0.3V) to +14V
.....+0.3V to -14V
.....
ut Voltages
N .....-0.3V to (VCC + 0.3V)
N.....±30V
put Voltages
OUT .....(V+ + 0.3V) to (V- - 0.3V)
OUT.....-0.3V to (VCC + 0.3V)
ort-Circuit Duration, TOUT .....Continuous
ntinuous Power Dissipation (TA = +70°C)
4-Pin Plastic DIP (derate 10.00mW/°C above +70°C)....800mW
6-Pin Plastic DIP (derate 10.53mW/°C above +70°C)....842mW
0-Pin Plastic DIP (derate 11.11mW/°C above +70°C)....889mW
4-Pin Narrow Plastic DIP
(derate 13.33mW/°C above +70°C) 1.07W
4-Pin Plastic DIP (derate 9.09mW/°C above +70°C).....500mW
6-Pin Wide SO (derate 9.52mW/°C above +70°C).....762mW
20-Pin Wide SO (derate 10 00mW/°C above +70°C).....800mW
24-Pin Wide SO (derate 11.76mW/°C above +70°C).....941mW
28-Pin Wide SO (derate 12.50mW/°C above +70°C) 1W
44-Pin Plastic FP (derate 11.11mW/°C above +70°C) 889mW
14-Pin CERDIP (derate 9.09mW/°C above +70°C).....727mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C).....800mW
20-Pin CERDIP (derate 11.11mW/°C above +70°C).....889mW
24-Pin Narrow CERDIP
(derate 12.50mW/°C above +70°C) 1W
24-Pin Sidebraze (derate 20.0mW/°C above +70°C).....1.6W
28-Pin SSOP (derate 9.52mW/°C above +70°C).....762mW
Operating Temperature Ranges
MAX2 _ _ C _ _.....0°C to +70°C
MAX2 _ _ E _ _.....-40°C to +85°C
MAX2 _ _ M _ _.....-55°C to +125°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

esses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional eration of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to solute maximum rating conditions for extended periods may affect device reliability.

LECTRICAL CHARACTERISTICS—MAX223/MAX230–MAX241

IAX223/230/232/234/236/237/238/240/241, VCC = +5V ±10; MAX233/MAX235, VCC = 5V ±5%, C1–C4 = 1.0µF; MAX231/MAX239, CC = 5V ±10%; V+ = 7.5V to 13.2V; TA = TMIN to TMAX; unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to ground		±5.0	±7.3		V
VCC Power-Supply Current	No load, TA = +25°C	MAX232/233		5	10	mA
		MAX223/230/234–238/240/241		7	15	
		MAX231/239		0.4	1	
V+ Power-Supply Current		MAX231		1.8	5	mA
		MAX239		5	15	
Shutdown Supply Current	TA = +25°C	MAX223		15	50	µA
		MAX230/235/236/240/241		1	10	
Input Logic Threshold Low	TIN; EN, $\overline{SHDN}$ (MAX233); $\overline{EN}$, SHDN (MAX230/235–241)				0.8	V
Input Logic Threshold High	TIN		2.0			V
	EN, $\overline{SHDN}$ (MAX223); $\overline{EN}$, SHDN (MAX230/235/236/240/241)		2.4			
Logic Pull-Up Current	TIN = 0V			1.5	200	µA
Receiver Input Voltage Operating Range			-30		30	V

5V-Powered, Multichannel RS-232 rivers/Receivers

ECTRICAL CHARACTERISTICS—MAX223/MAX230–MAX241 (continued)

X223/230/232/234/236/237/238/240/241, V_{CC} = +5V ±10; MAX233/MAX235, V_{CC} = 5V ±5%, C1–C4 = 1.0µF; MAX231/MAX239, = 5V ±10%; V+ = 7.5V to 13.2V; $T_A = T_{MIN}$ to T_{MAX}; unless otherwise noted.)

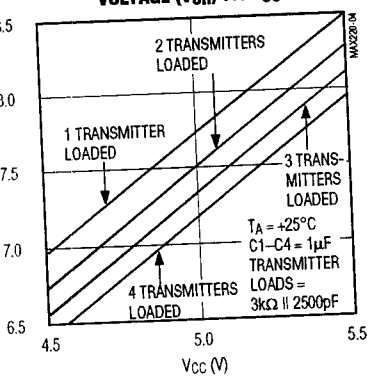
PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
-232 Input Threshold Low	T_A = +25°C, V_{CC} = 5V	Normal operation $\overline{SHDN}$ = 5V (MAX223) SHDN = 0V (MAX235/236/240/241)		0.8	1.2		V
		Shutdown (MAX223) $\overline{SHDN}$ = 0V, EN = 5V ($R4_{IN}$, $R5_{IN}$)		0.6	1.5		
S-232 Input Threshold High	T_A = +25°C, V_{CC} = 5V	Normal operation $\overline{SHDN}$ = 5V (MAX223) SHDN = 0V (MAX235/236/240/241)			1.7	2.4	V
		Shutdown (MAX223) $\overline{SHDN}$ = 0V, EN = 5V ($R4_{IN}$, $R5_{IN}$)			1.5	2.4	
S-232 Input Hysteresis	V_{CC} = 5V, no hysteresis in shutdown			0.2	0.5	1.0	V
S-232 Input Resistance	T_A = +25°C, V_{CC} = 5V			3	5	7	kΩ
TL/CMOS Output Voltage Low	I_{OUT} = 1.6mA (MAX231/232/233, I_{OUT} = 3.2mA)					0.4	V
TL/CMOS Output Voltage High	I_{OUT} = -1mA			3.5	V_{CC} - 0.4		V
TL/CMOS Output Leakage Current	0V ≤ R_{OUT} ≤ V_{CC}; EN = 0V (MAX223); $\overline{EN}$ = V_{CC} (MAX235–241)				0.05	±10	µA
Receiver Output Enable Time	Normal operation	MAX223			600		ns
		MAX235/236/239/240/241			400		
Receiver Output Disable Time	Normal operation	MAX223			900		ns
		MAX235/236/239/240/241			250		
Propagation Delay	RS-232 IN to TTL/CMOS OUT, C_L = 150pF	Normal operation			0.5	10	µs
		$\overline{SHDN}$ = 0V (MAX223)	t_{PHLS}		4	40	
			t_{PLHS}		6	40	
Transition Region Slew Rate	MAX223/MAX230/MAX234–241, T_A = +25°C, V_{CC} = 5V, R_L = 3kΩ to 7kΩ, C_L = 50pF to 2500pF, measured from +3V to -3V or -3V to +3V			3	5.1	30	V/µs
	MAX231/MAX232/MAX233, T_A = +25°C, V_{CC} = 5V, R_L = 3kΩ to 7kΩ, C_L = 50pF to 2500pF, measured from +3V to -3V or -3V to +3V				4	30	
Transmitter Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V			300			Ω
Transmitter Output Short-Circuit Current					±10		mA

+5V-Powered, Multichannel RS-232 Drivers/Receivers

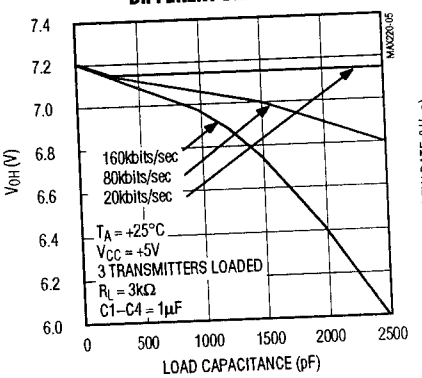
Typical Operating Characteristics

MAX223/MAX230–MAX241

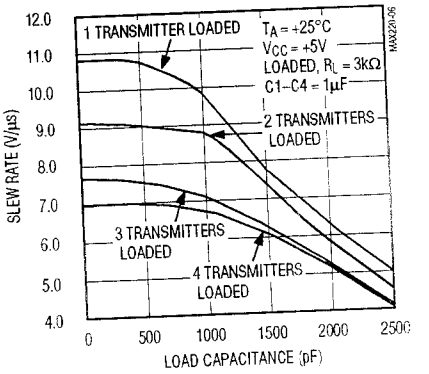
TRANSMITTER OUTPUT VOLTAGE (V_{OH}) vs. V_{CC}



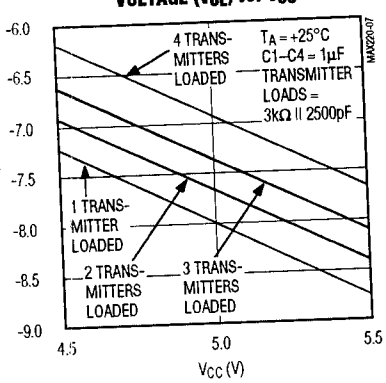
TRANSMITTER OUTPUT VOLTAGE (V_{OH}) vs. LOAD CAPACITANCE AT DIFFERENT DATA RATES



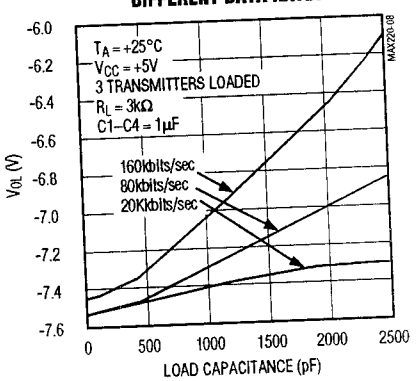
TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



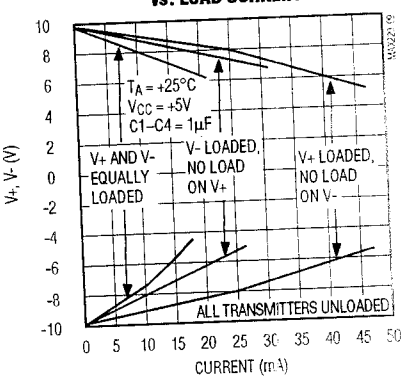
TRANSMITTER OUTPUT VOLTAGE (V_{OL}) vs. V_{CC}



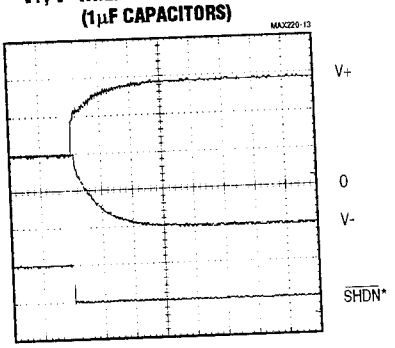
TRANSMITTER OUTPUT VOLTAGE (V_{OL}) vs. LOAD CAPACITANCE AT DIFFERENT DATA RATES



TRANSMITTER OUTPUT VOLTAGE (V+, V-) vs. LOAD CURRENT



V+, V- WHEN EXITING SHUTDOWN (1µF CAPACITORS)



*SHUTDOWN POLARITY IS REVERSED

5V-Powered, Multichannel RS-232 rivers/Receivers

Detailed Description

MAX220–MAX249 contain four sections: dual rge-pump DC-DC voltage converters, RS-232 dri-, RS-232 receivers, and receiver and transmitter ble control inputs.

Dual Charge-Pump Voltage Converter

MAX220–MAX249 have two internal charge-pumps convert +5V to ±10V (unloaded) for RS-232 driver ration. The first converter uses capacitor C1 to dou-the +5V input to +10V on C3 at the V+ output. The ond converter uses capacitor C2 to invert +10V to V on C4 at the V- output.

mall amount of power may be drawn from the +10V -) and -10V (V-) outputs to power external circuitry e the *Typical Operating Characteristics* section), cept on the MAX225 and MAX245–MAX247, where se pins are not available. V+ and V- are not regulated, the output voltage drops with increasing load current. not load V+ and V- to a point that violates the mini-um ±5V EIA/TIA-232E driver output voltage when urcing current from V+ and V- to external circuitry.

hen using the shutdown feature in the MAX222, AX225, MAX230, MAX235, MAX236, MAX240, AX241, and MAX245–MAX249, avoid using V+ and V- power external circuitry. When these parts are shut own, V- falls to 0V, and V+ falls to +5V. For applica-ns where a +10V external supply is applied to the V+ n (instead of using the internal charge pump to gen-ate +10V), the C1 capacitor must not be installed and e $\overline{SHDN}$ pin must be tied to V_{CC}. This is because V+ internally connected to V_{CC} in shutdown mode.

RS-232 Drivers

he typical driver output voltage swing is ±8V when aded with a nominal 5kΩ RS-232 receiver and V_{CC} = 5V. Output swing is guaranteed to meet the EIA/TIA-32E and V.28 specification, which calls for ±5V mini-um driver output levels under worst-case conditions. hese include a minimum 3kΩ load, V_{CC} = +4.5V, and naximum operating temperature. Unloaded driver out-ut voltage ranges from (V+ -1.3V) to (V- +0.5V).

nput thresholds are both TTL and CMOS compatible. he inputs of unused drivers can be left unconnected ince 400kΩ input pull-up resistors to V_{CC} are built in except for the MAX220). The pull-up resistors force the outputs of unused drivers low because all drivers invert. The internal input pull-up resistors typically source 12µA, except in shutdown mode where the pull-ups are dis-abled. Driver outputs turn off and enter a high-imped-ance state—where leakage current is typically microamperes (maximum 25µA)—when in shutdown mode, in three-state mode, or when device power is removed. Outputs can be driven to ±15V. The power-supply current typically drops to 8µA in shutdown mode. The MAX220 does not have pull-up resistors to force the outputs of the unused drivers low. Connect unused inputs to GND or V_{CC}.

The MAX239 has a receiver three-state control line, and the MAX223, MAX225, MAX235, MAX236, MAX240, and MAX241 have both a receiver three-state control line and a low-power shutdown control. Table 2 shows the effects of the shutdown control and receiver three-state control on the receiver outputs.

The receiver TTL/CMOS outputs are in a high-impedance, three-state mode whenever the three-state enable line is high (for the MAX225/MAX235/MAX236/MAX239–MAX241), and are also high-impedance whenever the shutdown control line is high.

When in low-power shutdown mode, the driver outputs are turned off and their leakage current is less than 1µA with the driver output pulled to ground. The driver output leakage remains less than 1µA, even if the transmitter output is backdriven between 0V and (V_{CC} + 6V). Below -0.5V, the transmitter is diode clamped to ground with 1kΩ series impedance. The transmitter is also zener clamped to approximately V_{CC} + 6V, with a series impedance of 1kΩ.

The driver output slew rate is limited to less than 30V/µs as required by the EIA/TIA-232E and V.28 specifications. Typical slew rates are 24V/µs unloaded and 10V/µs loaded with 3Ω and 2500pF.

RS-232 Receivers

EIA/TIA-232E and V.28 specifications define a voltage level greater than 3V as a logic 0, so all receivers invert. Input thresholds are set at 0.8V and 2.4V, so receivers respond to TTL level inputs as well as EIA/TIA-232E and V.28 levels.

The receiver inputs withstand an input overvoltage up to ±25V and provide input terminating resistors with

Table 2. Three-State Control of Receivers

PART	SHDN	$\overline{SHDN}$	EN	$\overline{EN}$(R)	RECEIVERS
MAX223	—	Low High High	X Low High	—	High Impedance Active High Impedance
MAX225	—	—	—	Low High	High Impedance Active
MAX235 MAX236 MAX240	Low Low High	—	—	Low High X	High Impedance Active High Impedance

nal 5kΩ values. The receivers implement Type 1 pretation of the fault conditions of V.28 and IA-232E.

receiver input hysteresis is typically 0.5V with a anteed minimum of 0.2V. This produces clear out- transitions with slow-moving input signals, even moderate amounts of noise and ringing. The iver propagation delay is typically 600ns and is pendent of input swing direction.

Low-Power Receive Mode

low-power receive-mode feature of the MAX223, X242, and MAX245–MAX249 puts the IC into shut- n mode but still allows it to receive information. This portant for applications where systems are periodi- y awakened to look for activity. Using low-power ive mode, the system can still receive a signal that activate it on command and prepare it for communi- on at faster data rates. This operation conserves tem power.

Negative Threshold—MAX243

MAX243 is pin compatible with the MAX232A, differ- only in that RS-232 cable fault protection is removed one of the two receiver inputs. This means that control s such as CTS and RTS can either be driven or left ating without interrupting communication. Different oles are not needed to interface with different pieces of uipment.

e input threshold of the receiver without cable fault otection is -0.8V rather than +1.4V. Its output goes sitive only if the input is connected to a control line t is actively driven negative. If not driven, it defaults the 0 or "OK to send" state. Normally, the MAX243's er receiver (+1.4V threshold) is used for the data line D or RD), while the negative threshold receiver is con- cted to the control line (DTR, DTS, CTS, RTS, etc.).

her members of the RS-232 family implement the tional cable fault protection as specified by EIA/TIA- 2E specifications. This means a receiver output goes gh whenever its input is driven negative, left floating, shorted to ground. The high output tells the serial mmunications IC to stop sending data. To avoid this, e control lines must either be driven or connected th jumpers to an appropriate positive voltage level.

Shutdown—MAX222–MAX242

On the MAX222, MAX235, MAX236, MAX240, and MAX241, all receivers are disabled during shutdown. On the MAX223 and MAX242, two receivers continue to operate in a reduced power mode when the chip is in shutdown. Under these conditions, the propagation delay increases to about 2.5µs for a high-to-low input transition. When in shutdown, the receiver acts as a CMOS inverter with no hysteresis. The MAX223 and MAX242 also have a receiver output enable input ($\overline{EN}$ for the MAX242 and EN for the MAX223) that allows receiver output control independent of $\overline{SHDN}$ (SHDN for MAX241). With all other devices, $\overline{SHDN}$ (SHDN for MAX241) also disables the receiver outputs.

The MAX225 provides five transmitters and five receivers, while the MAX245 provides ten receivers and eight transmitters. Both devices have separate receiver and transmitter-enable controls. The charge pumps turn off and the devices shut down when a logic high is applied to the ENT input. In this state, the supply current drops to less than 25µA and the receivers continue to operate in a low-power receive mode. Driver outputs enter a high-impedance state (three-state mode). On the MAX225, all five receivers are controlled by the $\overline{ENR}$ input. On the MAX245, eight of the receiver outputs are controlled by the $\overline{ENR}$ input, while the remaining two receivers (RA5 and RB5) are always active. RA1–RA4 and RB1–RB4 are put in a three-state mode when $\overline{ENR}$ is a logic high.

Receiver and Transmitter Enable Control Inputs

The MAX225 and MAX245–MAX249 feature transmitter and receiver enable controls.

The receivers have three modes of operation: full-speed receive (normal active), three-state (disabled), and low-power receive (enabled receivers continue to function at lower data rates). The receiver enable inputs control the full-speed receive and three-state modes. The transmitters have two modes of operation: full-speed transmit (normal active) and three-state (disabled). The transmitter enable inputs also control the shutdown mode. The device enters shutdown mode when all transmitters are disabled. Enabled receivers function in the low-power receive mode when in shutdown.

5V-Powered, Multichannel RS-232 Drivers/Receivers

es 1a–1d define the control states. The MAX244 no control pins and is not included in these tables.

MAX246 has ten receivers and eight drivers with control pins, each controlling one side of the ce. A logic high at the A-side control input ($\overline{ENA}$) ses the four A-side receivers and drivers to go into ree-state mode. Similarly, the B-side control input $\overline{B}$) causes the four B-side drivers and receivers to nto a three-state mode. As in the MAX245, one A- and one B-side receiver (RA5 and RB5) remain ve at all times. The entire device is put into shut- n mode when both the A and B sides are disabled $\overline{A}$ = $\overline{ENB}$ = +5V).

MAX247 provides nine receivers and eight drivers four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver ble inputs each control four receiver outputs. The $\overline{TA}$ and $\overline{ENTB}$ transmitter enable inputs each control drivers. The ninth receiver (RB5) is always active. device enters shutdown mode with a logic high on n $\overline{ENTA}$ and $\overline{ENTB}$.

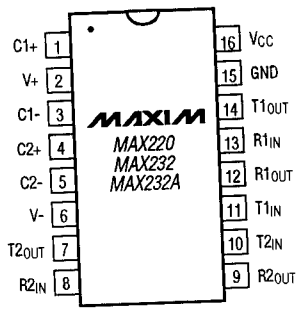
MAX248 provides eight receivers and eight drivers n four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver able inputs each control four receiver outputs. The $\overline{TA}$ and $\overline{ENTB}$ transmitter enable inputs control four vers each. This part does not have an always-active eiver. The device enters shutdown mode and trans- ters go into a three-state mode with a logic high on h $\overline{ENTA}$ and $\overline{ENTB}$.

The MAX249 provides ten receivers and six drivers with four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver enable inputs each control five receiver outputs. The $\overline{ENTA}$ and $\overline{ENTB}$ transmitter enable inputs control three drivers each. There is no always-active receiver. The device enters shutdown mode and transmitters go into a three-state mode with a logic high on both $\overline{ENTA}$ and $\overline{ENTB}$. In shutdown mode, active receivers operate in a low-power receive mode at data rates up to 20kbits/sec.

Applications Information

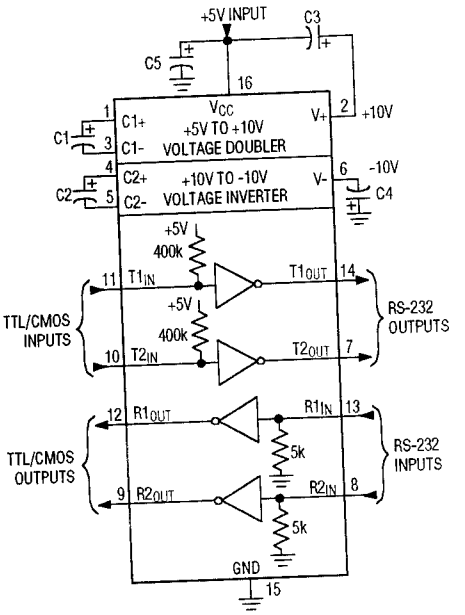
Figures 5 through 25 show pin configurations and typical operating circuits. In applications that are sensitive to power-supply noise, V_{CC} should be decoupled to ground with a capacitor of the same value as C1 and C2 connected as close as possible to the device.

TOP VIEW



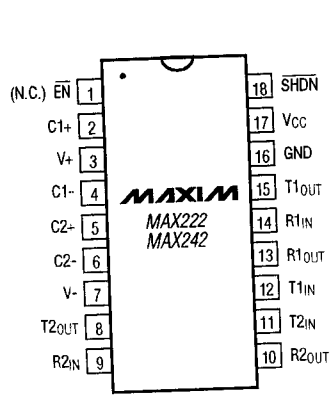
DIP/SO

CAPACITANCE (µF)					
DEVICE	C1	C2	C3	C4	C5
MAX220	4.7	4.7	10	10	4.7
MAX232	1.0	1.0	1.0	1.0	1.0
MAX232A	0.1	0.1	0.1	0.1	0.1

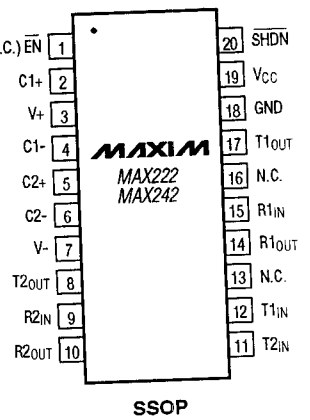


gure 5. MAX220/MAX232/MAX232A Pin Configuration and Typical Operating Circuit

TOP VIEW



DIP/SO



SSOP

( ) ARE FOR MAX222 ONLY.
PIN NUMBERS IN TYPICAL OPERATING CIRCUIT ARE FOR DIP/SO PACKAGES ONLY.

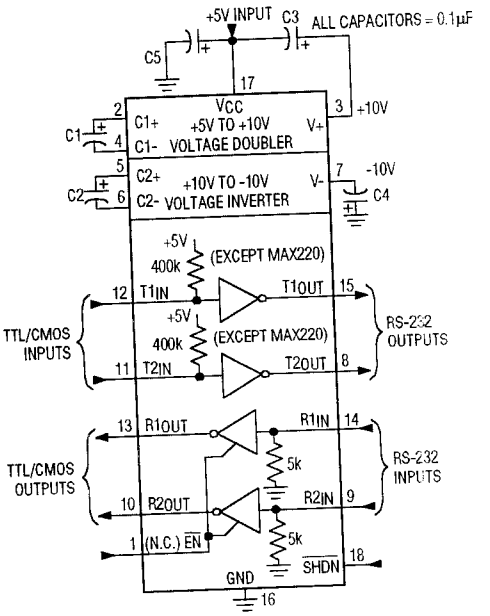


Figure 6. MAX222/MAX242 Pin Configurations and Typical Operating Circuit