AUTOMATIC VEHICLE GUIDING

PROJECT REPORT

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IN PARTIAL FULFILMENT OF THE REQUIREMENTS
FOR THE AWARD OF THE DEGREE OF
BACHELOR OF ENGINEERING IN
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Department of Electronics and Communication Engineering
KUMARAGURU COLLEGE OF TECHNOLGY
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Department of Electronics and Communication Engineering

CERTIFICATE

This is to certify that this project entitled

AUTOMATIC VEHICLE GUIDING

has been submitted by

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In partial fulfillment of the requirements for the award of degree of

Bachelor of Engineering in Electronics and Communication Engineering branch of **BHARATHIAR UNIVERSITY, Coimbatore**.
during the Academic year 2003-2004.

(Internal Guide) | **(Head of the Department)**

Certified that the candidate was examined by us in the Project Work Viva-Voice Examination held on ____________________.

University Register Number ____________________.

Examiner) | **(External Examiner)**

ACKNOWLEDGEMENT

We would like to express sincere and heartfelt gratitude to all those who have assisted us in the successful completion of the project.

We are greatly indebted to our project guide Prof.Muthuraman Ramasamy, Head of Electronics and Communication Department who has been instrumental in providing us all guidance and encouragement and has been a very part of all our lows and highs. He has also pepped up our spirits in our cruise during the various stages of this project.

We acknowledge the assistance offered by our Principal Dr.Padmanabhan, .M.E., Ph.D., for providing all the amenities to do this project.

We have great pleasure in extending our gratitude to other Teaching staffs and lab assistants, Department of Electronics and Communication Engineering for their support in this project.

We thank all our friends and well-wishers for all their kind help extended directly or indirectly towards the completion of this project

Automatic Vehicle Guiding

Contents

SYNOPSIS

In any Industry, transport of raw materials, finished products and waste materials is an important task. Many vehicles will be used for this purpose. Manual operation and unregulated use of the vehicles give room for potential misuse. Therefore, it would be advantageous if there was a system to monitor and guide the vehicles in the industrial environment. In this world where wireless communication is tremendous, our project provides a simple way of movement of vehicle from one place to another on its own without any need for wire.

One way of locating the vehicle is through GPS. But in small industries, the cost of leasing transponders in satellites is prohibitive. Therefore our project provides a cost effective alternative.

This project effectively satisfies the need for a cost effective way of implementing automatic vehicle guiding in Industries

1. INTRODUCTION

Technology has progressed as never before in the past five years. Automation has crept into every aspect of life. In industries there is need to decrease the complexities involved in transportation and reduce the need for labor. In this world where wireless communication is tremendous, we in our project provide simple way of movement of vehicle from one place to another on its own without any need for wire.

1.1.PROJECT OVERVIEW

The project is implemented by first finding the position of the vehicle using matrix scanning. This is visualized on the screen and then the point is got to which the vehicle is to be moved. The respective relay contact of the vehicle is closed for the movement to the specified point. It involves the movement of the vehicle from one point to another manually with the help of direction keys in the keyboard of the pc. Here the path of movement is also traced with the help of the software visual basic.

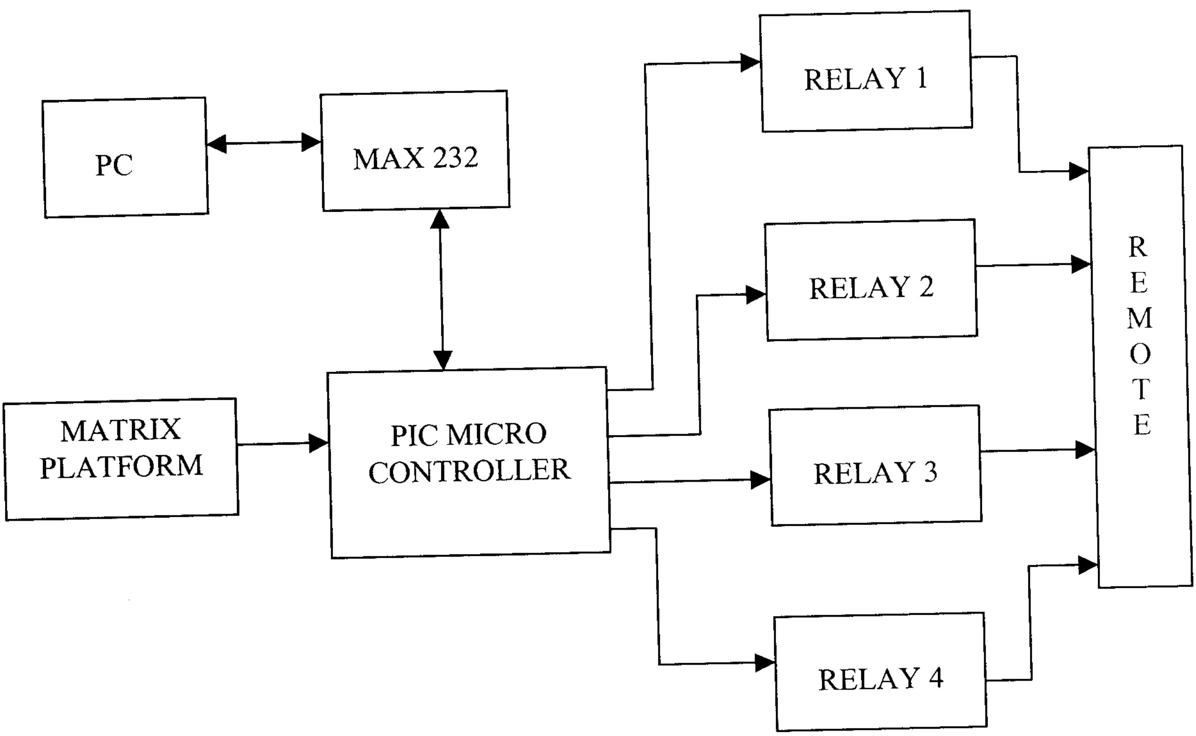
A microcontroller is used to get the data from the board to the pc and vice versa. A chip called Max Rs 232 is used for the serial communication between the pc and the microcontroller. The relay for the movement of the vehicle is controlled by the signal from the microcontroller. The speed of the movement of the vehicle can be varied depending upon the area of working.

2.HARDWARE DESCRIPTION

The hardware of the automatic vehicle guiding system has the following major components:

- Power supply
- PIC 16F877 A
- MAX RS-232
- Matrix Board Scanner
- Personal Computer
- Relays

2.1.1.BLOCK DIAGRAM



Description:

The block diagram consists of the following parts.

- Power supply
- Microcontroller
- Max Rs 232
- Matrix board scanner
- Personal Computer
- Relays.

2.1.2.Power Supply:

A supply of 5 volts and 12 volts is used for the functioning of the microcontroller and the Max Rs 232 chip (serial communication protocol). This is done with the help of 7805 and 7812.

2.1.3.Microcontroller:

A PIC microcontroller consists of powerful CPU tightly coupled with memory (RAM, ROM or EPROM), various I/O features such as serial ports, parallel ports, timer/ counters, Interrupt controller, Data acquisition Interfaces – analog to Digital Converter(ADC), Digital to Analog Converter(DAC), everything integrated onto single Silicon Chip. In our project it is used to get the scanned signal from the matrix board and transmit it to the pc and also to get it back. It is also used to supply the signals to the relay of the vehicle for its control.

2.1.4.Matrix board scanner:

This consists of wooden board of size 4 x 4, which is divided into an 8 x 8 matrix, reed switch is kept at each intersection point which is used to give information about the placement of the vehicle. The data transmission is done using a bidirectional latch.

2.1.5.Max Rs 232:

This is the serial data transfer protocol, which is used as communication interface between the pc and the microcontroller as the signal from the pc and microcontroller is understandable directly by the microcontroller and the pc respectively.

2.1.6.Personal Computer:

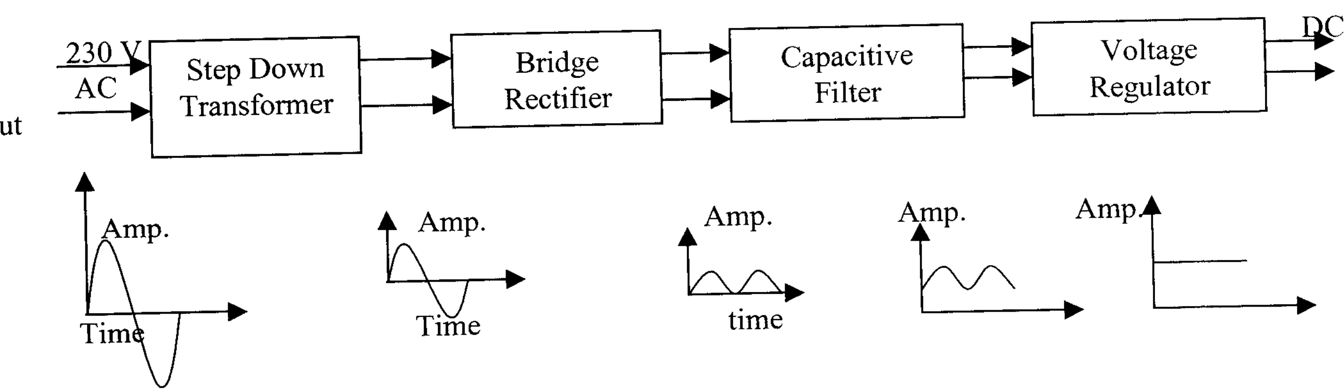
An ordinary computer that is used for visualizing the movement of the vehicle using the software visual basic is sufficient. All manipulation of data is done in the pc only. The respective control signal is given to the microcontroller through the Max Rs 232 interface from the pc only.

A detailed description of the parts in the block diagram is given in the following pages.

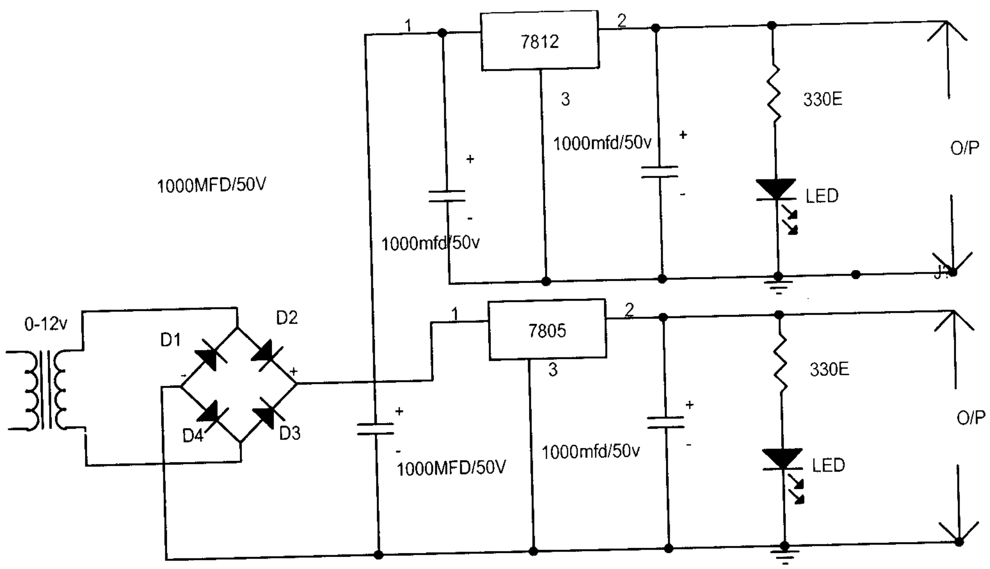
2.2.POWER SUPPLY UNIT:

All electronic devices work only with low D.C. voltage, so we need power supply unit to provide the appropriate voltage supply. The unit consists of a Transformer, Rectifier, filter and regulator. A.C. voltage typically 230 V rms is connected to a transformer which steps down the AC voltage to the desired level. A diode rectifier then provides full wave rectified voltage that is initially filtered by simple capacitor filter to produce a DC voltage. This resulting DC voltage usually has some ripples or AC voltage variations. A regulator circuit can use this DC input to provide regulated output voltage.

POWER SUPPLY – BLOCK DIAGRAM



POWER SUPPLY-CIRCUIT DIAGRAM



2.2.1.TRANSFORMER:

A transformer is a static piece of which electric power in one circuit is transformed into electric power of the same frequency in another circuit. In our project, we use step down transformer to provide the necessary supply for the electronic circuits. We have used the 15-0-15 centre tapped transformer.

2.2.2.RECTIFIER:

A full wave bridge rectifier is used for rectifying operation. It uses four diodes in bridge configuration. From the basic bridge configuration we see that two diodes (say D2 and D3) re conducting while the other two diodes (D1 and D4) are in 'OFF' state during one half of the cycle. During the other half of the cycle, the vice versa happens. Thus the polarity cross the load is the same.

2.2.3.FILTER:

The filter circuit used here is the capacitor filter circuit where a capacitor is connected to the rectifier output, and DC is obtained across it. The filtered waveform is essentially DC voltage with negligible ripples, which is ultimately fed to the load.

2.2.4.REGULATOR:

The output voltage from the capacitor is more filtered and finally regulated. The voltage regulator is a device, which maintains the output voltage constant irrespective of the change in supply variations, load variations, and temperature changes. Here we use two fixed voltage regulators namely LM 7812, L 7805 and LM 7912. The IC 7812 is +12V regulator, IC 7912 is -12V regulator and IC 7805 is +5V regulator.

2.3.PIC 16F877 A

2.3.1.INTRODUCTION:

PIC 16F877 A is a 40 pin enhanced flash microcontroller.It has inbuilt peripheral devices.It is an 8 bit microcontroller with 8KB flash program memory.It has a lot of special features.These are listed below.

2.3.2.FEATURES:

High-Performance RISC CPU

- Only 35 single word instructions to learn
- All instructions are single cycle (1µs) except for program branches
- Operating speed: DC - 20MHz clock input
- 8 k Bytes Flash Program Memory
- 368 Byte RAM Data Memory
- 256 Byte EEPROM Data Memory
- In-circuit serial programming

Peripheral Features

- Two 8-bit timer/counter(TMR0,TMR2) with 8-bit programmable prescalar
- One 16 bit timer/counter(TMR1)
- Two Capture, Compare, PWM module
- 10-bit, 8-channel Analog-to-Digital converter
- Synchronous Serial Port (SSP) with SPI (Master mode) and I2C (Master/Slave)
- Universal Synchronous Asynchronous Receiver

Transmitter with 9-bit address detection

- Two Analog Comparators
- Watchdog Timer (WDT) with separate RC oscillator

Special Microcontroller Features

- 100,000 erase/write cycle Enhanced FLASH program memory
- 1,000,000 erase/write cycle Data EEPROM memory typical
- Power saving SLEEP mode
- Programmable code protection
- Selectable Oscillator Options
- Self-reprogrammable under software control

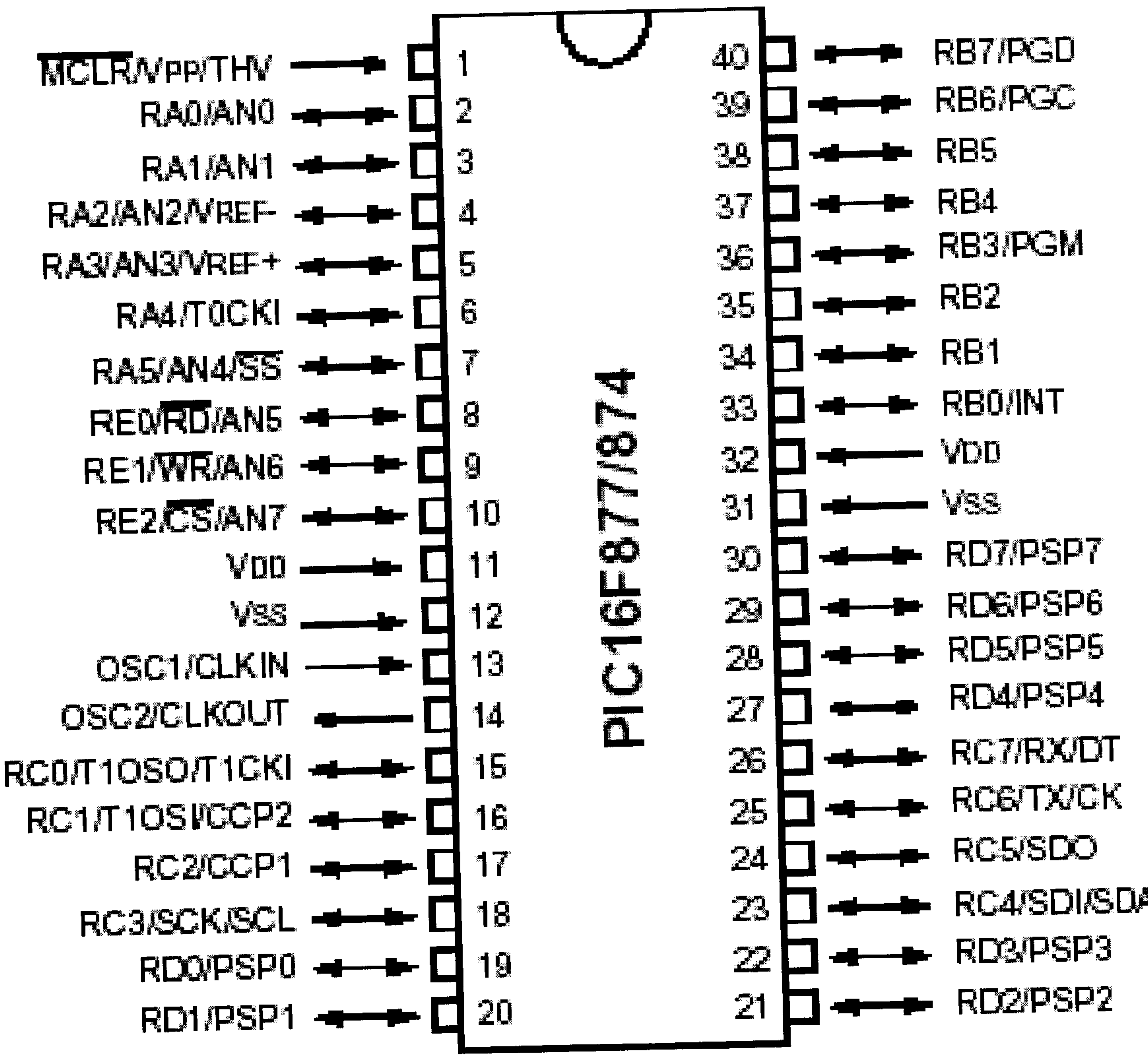
CMOS Technology

- Low power, high speed CMOS FLASH technology
- Fully Static Design
- Low Power Consumption

I/O and Packages

- 33 I/O pins with individual direction control
- 40-pin DIP

2.3.3.PIN LAYOUT

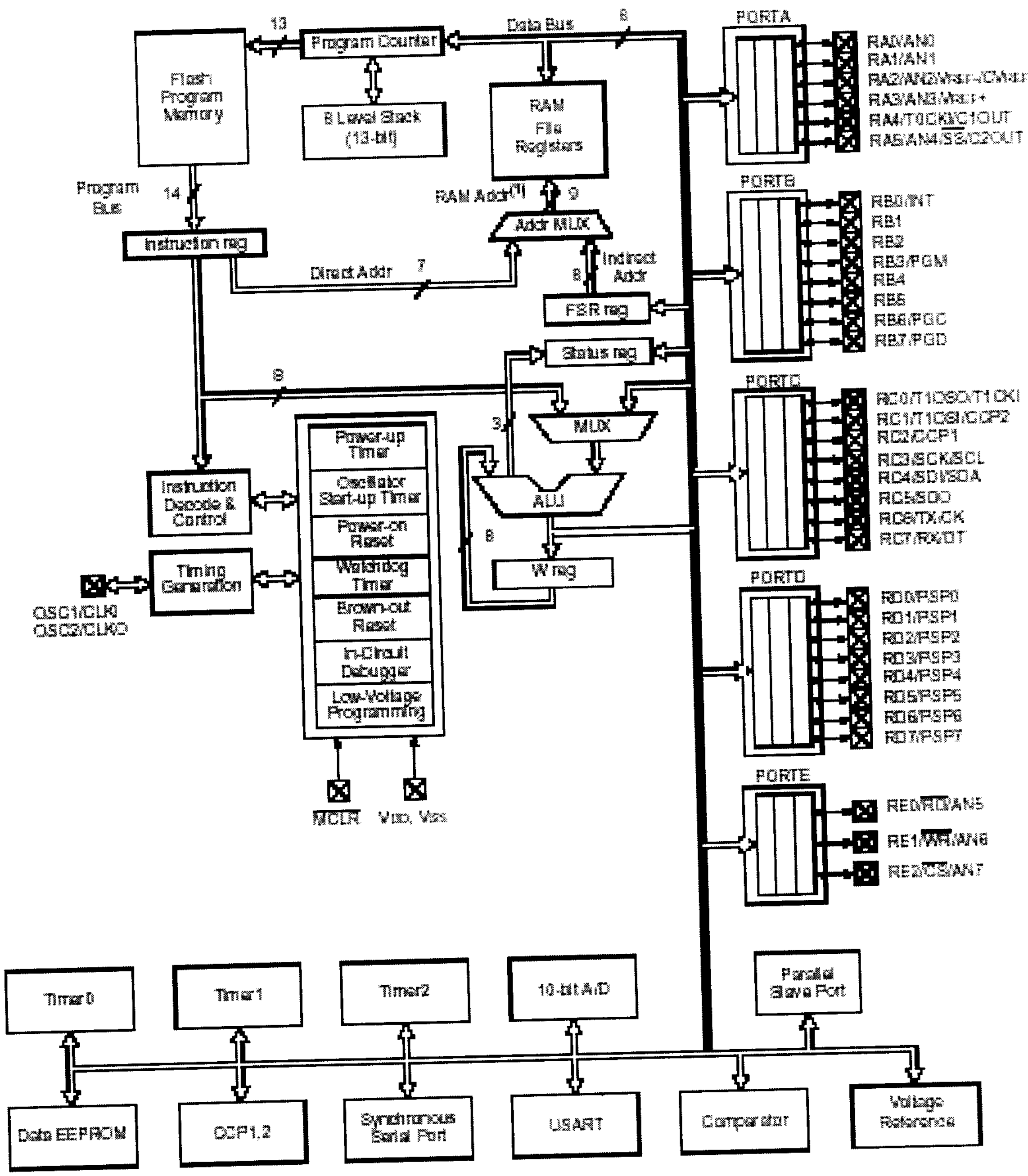


2.3.4.PIN DESCRIPTION

Pin Number	Description
1	MCLR/Vpp - Master clear input (active low)
2	RA0/AN0 - Port A
3	RA1/AN1 - Port A
4	RA2/AN2/Vref/CVref - Port A
5	RA3/AN3/Vref - Port A
6	RA4/TOCK1/C1OUT - Port A
7	RA5/AN4/SS/C2OUT - Port A
8	RE0/RD/AN5 - Port E
9	RE1/WR/AN6 - Port E
10	RE2/CS/AN7 - Port E
11	Vdd - Positive Power Supply
12	Vss - Ground
13	OSC1/CLKIN - Oscillator
14	OSC2/CLKOUT - Oscillator
15	RC0/T1OSO/T1CKI - Port C
16	RC1/T1OSI/CCP2 - Port C
17	RC2/CCP1 - Port C
18	RC3/SCK/SCL - Port C
19	RD0/PSP0 - Port D
20	RD1/PSP1 - Port D
21	RD2/PSP2 - Port D
22	RD3/PSP3 - Port D
23	RC4/SDI/SDO - Port C
24	RC5/SDO - Port C
25	RC6/TX/CK - Port C
26	RC7/RX/DT - Port C
27	RD4/PSP4 - Port D

28	RD5/PSP5 - Port D
29	RD6/PSP6 - Port D
30	RD7/PSP7 - Port D
31	Vss - Ground
32	Vdd - Positive Power Supply
33	RB0/INT - Port B
34	RB1 - Port B
35	RB2 - Port B
36	RB3/PGM - Port B
37	RB4 - Port B
38	RB5 - Port B
39	RB6/PGC - Port B
40	RB7/PGD - Port B

2.3.5.ARCHITECTURE



2.4.MAX RS-232

The Max Rs 232 line drivers/receivers is intended for all EIA/TIA -232E and V.28/V.24 communication interfaces, particularly applications where +-12V is not viable. These parts are especially useful in battery powered systems, since their low power shutdown mode reduces power dissipation to less then 5 microwatt. The Max 225, Max 233 Max 235 and Max 245/ Max 246/ Max 247 use no external components and are recommended for applications where printed circuit board space is critical.

2.4.1. SUPERIORITY COMPARED TO BIPOLAR:

- Operates from Single +5V Power Supply and +12V(Max 231/ Max 239)
- Low Power Receive Mode in Shutdown (Max 223/ Max 242)
- Meet all EIA/TIA- 232E and V.28 Specifications
- Multiple Drivers and Receivers
- 3- State Drivers and Receiver Outputs
- Open-Line Detection (Max 243)

2.4.2. APPLICATIONS:

- Portable Computers
- Low-Power Modems
- Interface Translation
- Battery-Powered RS-232 Systems
- Multidrop RS-232 Networks
- Industry Standard

2.4.3.DETAILED DESCRIPTION:

The MAX 220- MAX 249 contain four sections: dual charge pump DC-DC voltage converters, RS-232 drivers, RS-232 receivers and receiver and transmitter enable control inputs.

Dual Charge- Pump Voltage Converter:

The MAX 220- MAX 249 have two internal charge pumps that convert +5V to +- 10V (unloaded) for RS-232 driver operation. The first converter uses Capacitor C1 to double the +5V input to +10V on C3 at the V+ output. Second converter uses the capacitor C2 to invert the +10V to -10V on C4 at the V- output.

Small amount of power may be drawn from the +10V (V+) and -10V (V-) outputs to power external circuitry. V+ and V- are not regulated, so the output voltage drops with increasing load current. Do not load V+ and V- to point that violates the minimum+-5V EIA/TIA -232E driver output voltage when sourcing current fro V+ and V- to external circuitry.

RS-232 Drivers:

The typical driver voltage swing is +-8V when loaded with nominal 5k RS-232 receiver and VCC=+5V. Output swing is guaranteed to meet the EIA/TIA -232E and V.28 specification, which calls for +-5V minimum driver output levels under worst-case conditions. These include minimum 3k load, VCC=+4.5V, and maximum operating temperature. Unloaded driver output voltage ranges from (V+ -1.3V) to (V- +0.5V). Input thresholds are both TTL and CMOS compatible. The inputs of unused drivers can be left unconnected since 400k input pull up resistors to VCC are built in (except for the MAX 220). The pull-up resistors force the outputs of unused drivers low because all drivers invert. The internal input pull-up resistors typically source 12 microA, except in shutdown mode where the pull-ups are disabled.

Driver outputs turn off and enter high impedance state – where leakage current is typically microamperes (maximum 25 microamperes) –when in shut down mode, in three state mode, or when device power is removed. Outputs can be driven to +-15V. The power supply current typically drops to 8 microA in shutdown mode. The driver output slew rate is limited to less then 30V/micro s as required by the EIA/TIA -232E and V.28 specifications. Typical slew rates are 24V/micro s unloaded and 10V/micro s loaded with 3k and 2500pF.

RS-232 Receivers:

EIA/TIA -232E and V.28 specifications define voltage level greater than 3V as logic 0, so all receivers invert. Input thresholds are set at 0.8V and 2.4V, so receivers respond to TTL level inputs as well as EIA/TIA -232E and V.28 levels. The receiver inputs withstand an input over voltage up to +-25V and provide input terminating resistors with nominal 5k values. The receivers implement Type 1 interpretation of the fault conditions of EIA/TIA -232E and V.28 standards. The receiver input hysteresis is typically 0.5V with a guaranteed minimum of 0.2V. This produces clear output transitions with slow-moving input signals, even with moderate mounts of noise and ringing. The receiver propagation delay is typically 600ns and is independent of input swing direction.

2.5.MATRIX SCANNING

2.5.1.MATRIX SCANNER BOARD:

The board that we have considered for scanning is card board of size 4 x 4 feet. The board is then divided into 8 x 8 matrix. Reed switch is placed at each node with the help of glue, the output of which gives an approximate position of the vehicle. As a side wall reeper is given all the four sides. All the circuit connections are given in the board itself. A scanned output is given to the microcontroller.

2.5.2.BIDIRECTIONAL LATCH:

A magnet is placed at the bottom of the vehicle so that the reed switch gives information about the position. Here we use 74LS373 BIDIRECTIONAL LATCH which can both transmit and receive data. In the matrix board, we have 8 inputs, in the latch we make all the inputs one and transmit it, which is received using a latch at the bottom. The output is one if there is no vehicle and zero in the presence of the vehicle. Each and every node is checked for the presence of the vehicle using co-ordinates and the exact position is found.

2.6.PERSONAL COMPUTER

In our project we use the pc to get data and manipulate it, as it provides user friendly way to visualize the working of the project. The software we have used is Visual Basic.

2.6.1 INTRODUCTION:

In the earlier days of programming, the language BASIC (Beginners All Purpose Symbolic Instruction Code) was very small, simple, easy to learn and a gateway to learn other complicated programming languages like PASCAL,C,etc. But when the fourth generation languages originated, BASIC evolved as Visual Basic, which is a Windows programming language with the capability of competing with any other Windows programming language. One can learn VB quickly as well as develop any application.

2.6.2 FEATURES:

- Fastest and easiest way to create applications
- Provides tools to simplify rapid application development
- Provides pre-built objects helpful to form graphical user interface
- Enables system to react in real time during coding
- Multiple projects can be loaded to the environment
- Break points can be toggled with a mouse click
- Bookmarks can be placed for quick location

2.6.3 DESCRIPTION:

In our project the pc manipulates the scanned signal to find out the position, then provides signal for vehicle navigation, the initiation for the movement (i.e.) to trigger the motor and for the different direction is done through RF data communication.

The position of the vehicle is seen in the monitor, in which the matrix is seen. Only the node at which there is a vehicle is highlighted and the other nodes are not highlighted.

The movement of the vehicle is also seen in the screen (i.e.) in the matrix board. When the vehicle is moving, all nodes through which it passes are highlighted in the same sequence. In case of an obstruction, the next node is not highlighted till the obstruction is removes manually.

The movement of the vehicle is also made user friendly by making the movement with the help of direction keys in the keyboard, as described below.

- Up arrow – Forward Motion
- Down arrow – Backward motion
- Left arrow – Left motion
- Right arrow – Right Motion

3.CIRCUIT DESCRIPTION

3.1.PRINCIPLE:

The scanned data from the board is given to the microcontroller, which transfers the data to the pc through the serial port. Every control for the movement of the vehicle is generated from the pc. The relay switches are controlled for the navigation, which can be visualized in the pc using VB.

3.2.DETAILED DESCRIPTION:

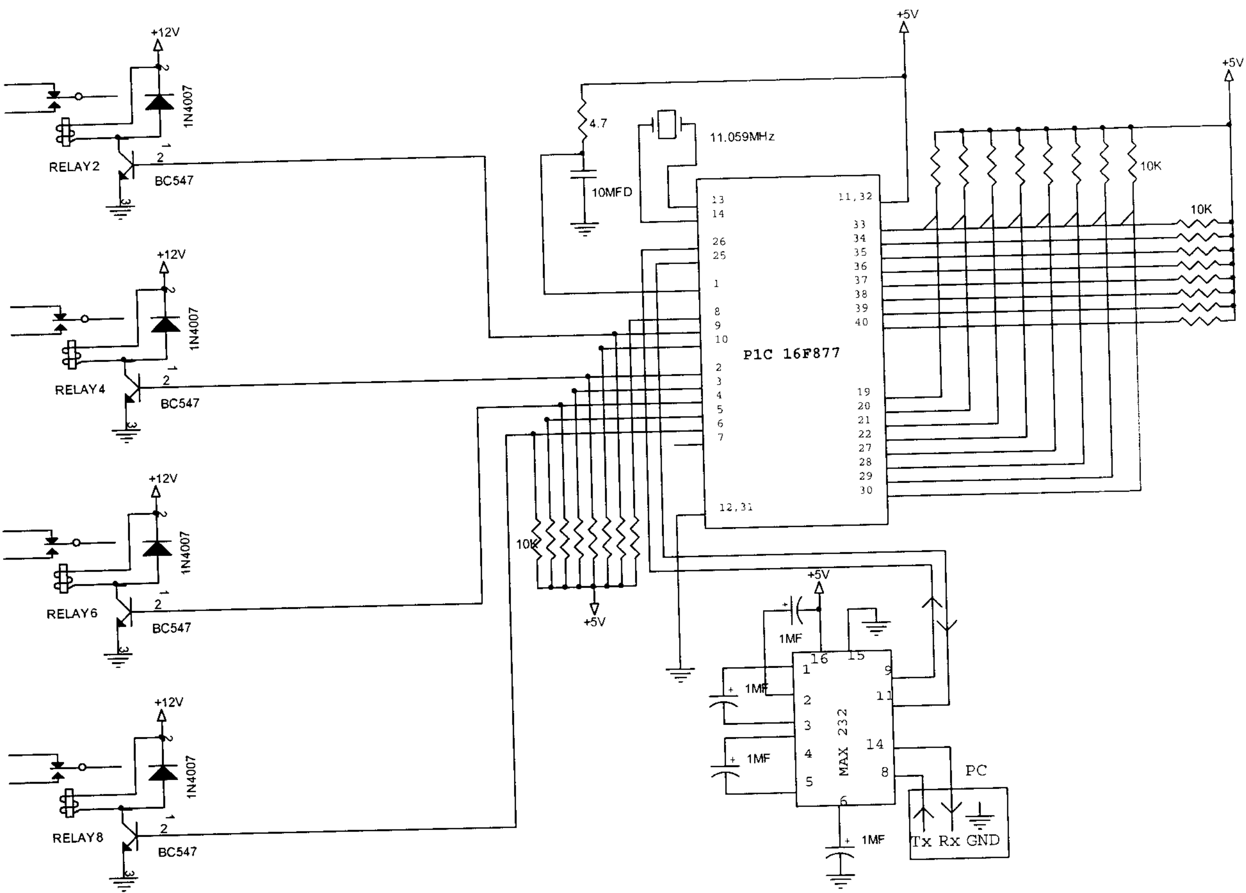
The cardboard is divided into an 8 x 8 matrix, and then each node is numbered fro 1 to 64. Magnetic reed switches are placed at the joints. Magnet is placed at the bottom of the vehicle so that when it comes over the reed switch, the switch gets closed and data is given to the microcontroller. The node number gives the data. Then this data is to be transmitted serially.

In the pc, the position is plotted using visual basic. Now we have the position of the vehicle. The desired place to which the vehicle is to be moved is entered (i.e.) the co-ordinate of the destination. Now the vehicle traces to the specified position.

The data from the scanner is continuously got, so that the movement of the vehicle is continuously traces in the VB screen. The movement can also be made manually using keyboard arrow keys.

The VB and the microcontroller are interfaced using the Activex control. The data transmission between the pc and the microcontroller are as given above.

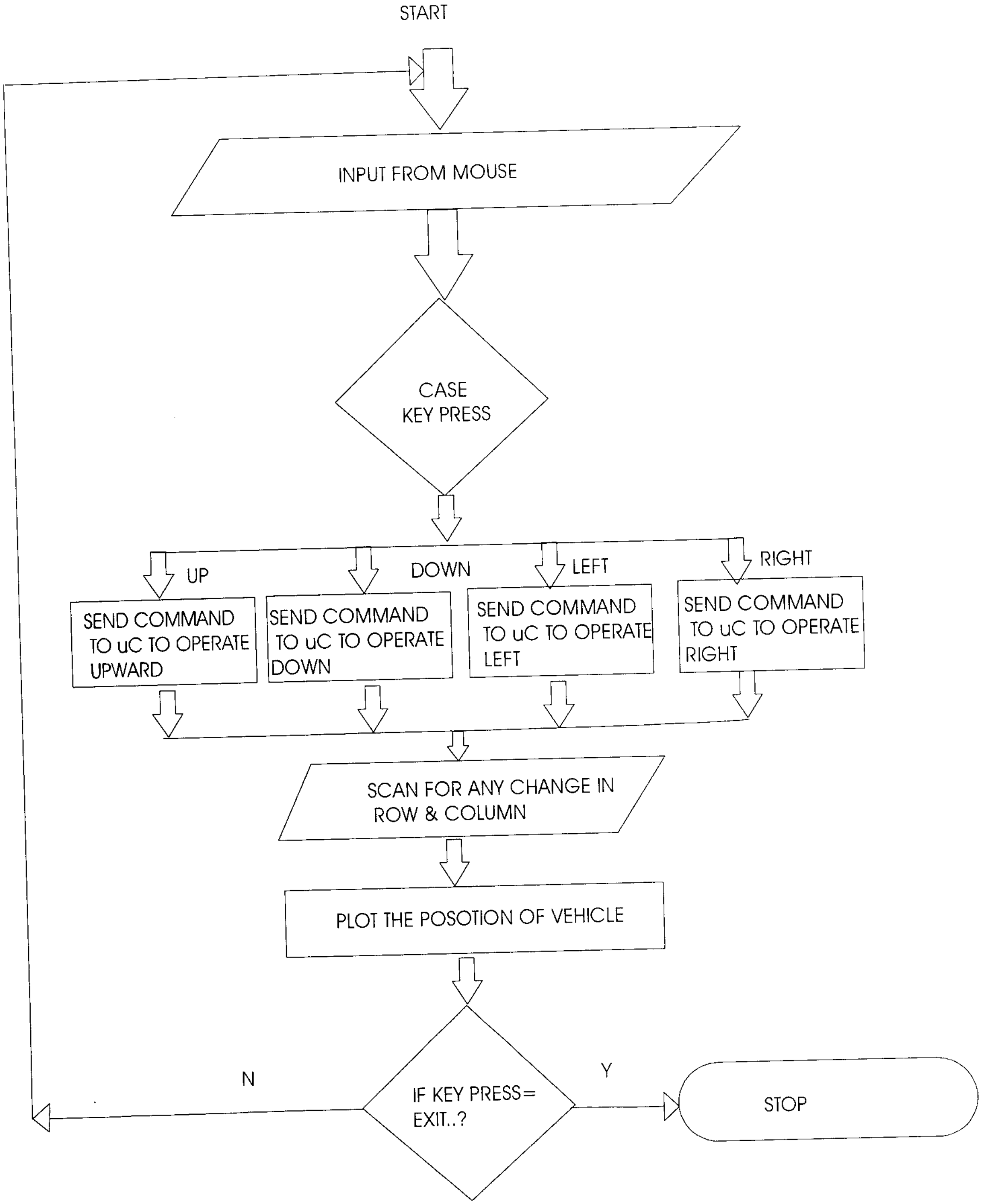
3.3.CIRCUIT DIAGRAM



SOFTWARE DESCRIPTION

The primary and substantial contribution for this project comes from the software that runs in the microcontroller and the computer.The program written for the microcontroller controls the data acquisition from the platform.The VB program running in the PC is involved in the display of vehicular position and in issuing control signals for vehicle movement.

FLOWCHART


START
INPUT FROM MOUSE
CASE
KEY PRESS
UP
DOWN
LEFT
RIGHT
SEND COMMAND
TO uC TO OPERATE
UPWARD
SEND COMMAND
TO uC TO OPERATE
DOWN
SEND COMMAND
TO uC TO OPERATE
LEFT
SEND COMMAND
TO uC TO OPERATE
RIGHT
SCAN FOR ANY CHANGE IN
ROW & COLUMN
PLOT THE POSOTION OF VEHICLE
N
Y
IF KEY PRESS=
EXIT..?
STOP

CONCLUSION

In this information age, there is a conscious effort to improve every process. It is imperitive, especially in industries to utilize technology to a greater extent to make their operation more efficient. Our project has given a thrust towards this goal by implementing automatic vehicle tracking and control.

The Automatic Vehicle Guiding system eliminates the need for a very costly satellite based tracking system. It uses simple tools and achieves the required purpose with high degree of accuracy.

The primary objectives of this project were to build a low cost and high performance vehicle guiding system. All these goals envisaged at the beginning of the project were successfully fulfilled. We sincerely hope that this small thrust will evolve into a widespread alternative in the industrial world.

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Appendix

PIC16F87XA

28/40-Pin Enhanced FLASH Microcontrollers

Devices Included in this Data Sheet:

- PIC16F873A
- PIC16F874A
- PIC16F876A
- PIC16F877A

High Performance RISC CPU:

- Only 35 single word instructions to learn
- All single cycle instructions except for program branches, which are two-cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle
- Up to 8K x 14 words of FLASH Program Memory,
  Up to 368 x 8 bytes of Data Memory (RAM),
  Up to 256 x 8 bytes of EEPROM Data Memory
- Pinout compatible to other 28-pin or 40/44-pin PIC16CXXX and PIC16FXXX microcontrollers

Peripheral Features:

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler, can be incremented during SLEEP via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules
  - Capture is 16-bit, max. resolution is 12.5 ns
  - Compare is 16-bit, max. resolution is 200 ns
  - PWM max. resolution is 10-bit
- Synchronous Serial Port (SSP) with SPI™ (Master mode) and I^{2}C™ (Master/Slave)
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with 9-bit address detection
- Parallel Slave Port (PSP) 8-bits wide, with external $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ controls (40/44-pin only)
- Brown-out detection circuitry for Brown-out Reset (BOR)

Analog Features:

- 10-bit, up to 8 channel Analog-to-Digital Converter (A/D)
- Brown-out Reset (BOR)
- Analog Comparator module with:
  - Two analog comparators
  - Programmable on-chip voltage reference (V_{REF}) module
  - Programmable input multiplexing from device inputs and internal voltage reference
  - Comparator outputs are externally accessible

Special Microcontroller Features:

- 100,000 erase/write cycle Enhanced FLASH program memory typical
- 1,000,000 erase/write cycle Data EEPROM memory typical
- Data EEPROM Retention > 40 years
- Self-reprogrammable under software control
- In-Circuit Serial Programming™ (ICSP™) via two pins
- Single supply 5V In-Circuit Serial Programming
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving SLEEP mode
- Selectable oscillator options
- In-Circuit Debug (ICD) via two pins

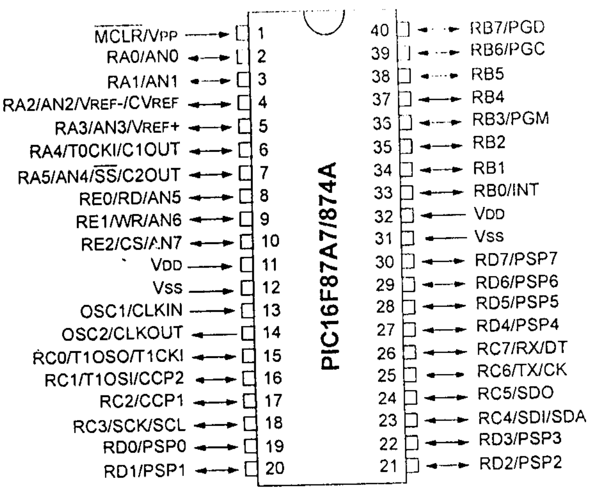
CMOS Technology:

- Low power, high speed FLASH/EEPROM technology
- Fully static design
- Wide operating voltage range (2.0V to 5.5V)
- Commercial and Industrial temperature ranges
- Low power consumption

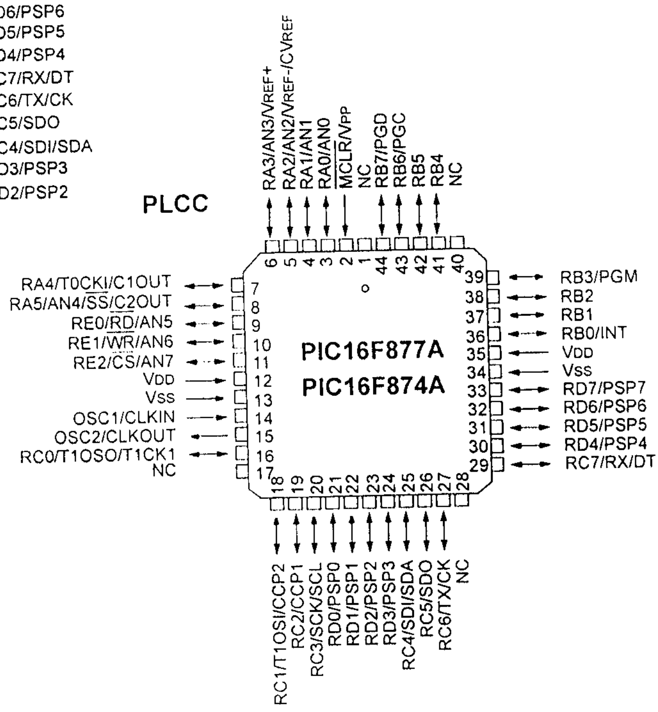
Device	Program Memory		Data SRAM (Bytes)	EEPROM (Bytes)	I/O	10-bit A/D (ch)	CCP (PWM)	MSSP		USART	Timers 8/16-bit	Comparators
	Bytes	# Single Word Instructions						SPI	Master I^{2}C			
PIC16F873A	7.2K	4096	192	128	22	5	2	Yes	Yes	Yes	2/1	2
PIC16F874A	7.2K	4096	192	128	33	8	2	Yes	Yes	Yes	2/1	2
PIC16F876A	14.3K	8192	368	256	22	5	2	Yes	Yes	Yes	2/1	2
PIC16F877A	14.3K	8192	368	256	33	8	2	Yes	Yes	Yes	2/1	2

Pin Diagram

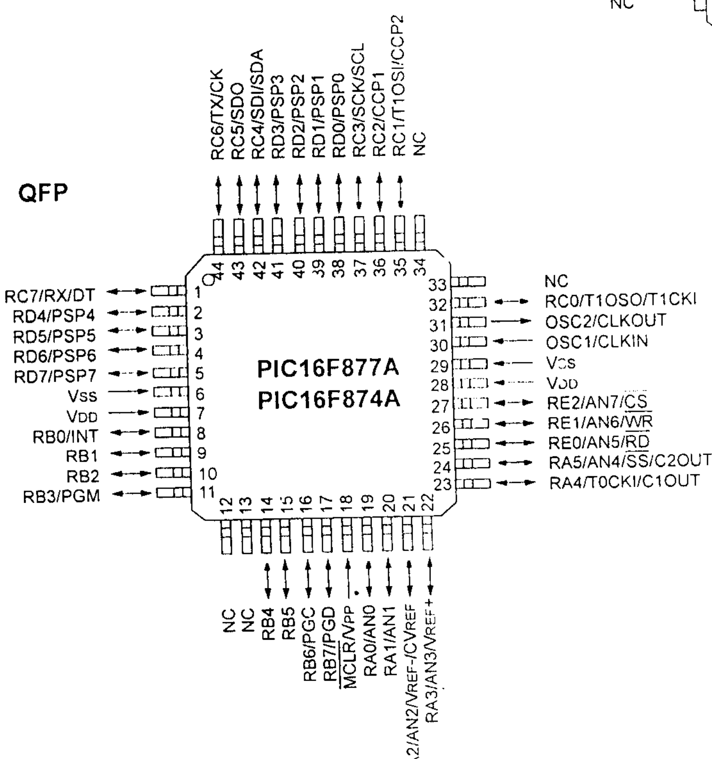
PDIP (40 pin)



PLCC



QFP



1.0 DEVICE OVERVIEW

This document contains device specific information about the following devices:

- PIC16F873A
- PIC16F874A
- PIC16F876A
- PIC16F877A

PIC16F873A/876A devices are available only in 28-pin packages, while PIC16F874A/877A devices are available in 40-pin and 44-pin packages. All devices in the PIC16F87XA family share common architecture, with the following differences:

- the PIC16F873A and PIC16F876A have one-half of the total on-chip memory of the PIC16F874A and PIC16F877A
- the 28-pin devices have three I/O ports, while the 40/44-pin devices have five
- the 28-pin devices have 14 interrupts, while the 40/44-pin devices have 15
- the 28-pin devices have five A/D input channels, while the 40/44-pin devices have eight
- the Parallel Slave Port is implemented only on the 40/44-pin devices

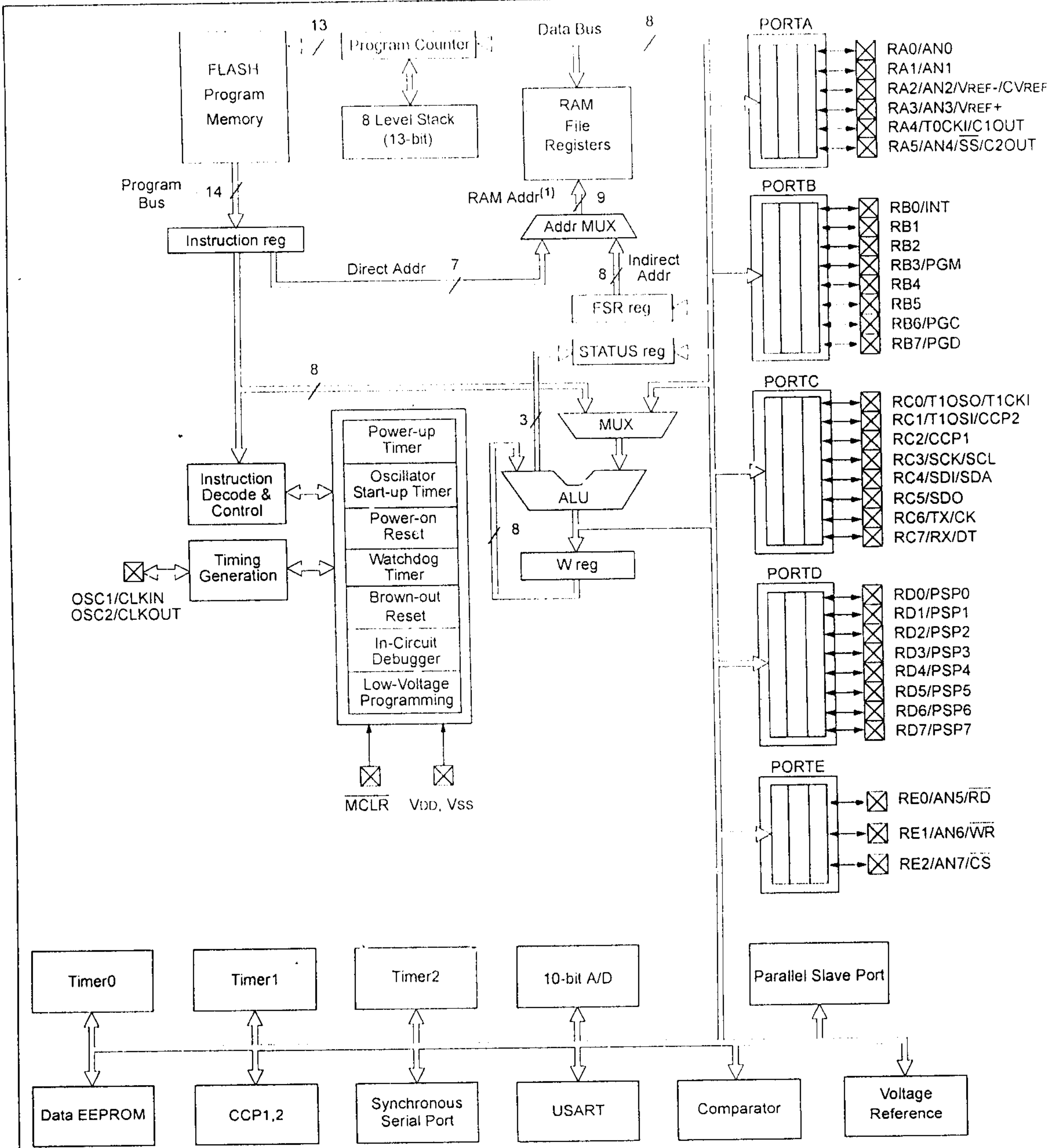
The available features are summarized in Table 1-1. Block diagrams of the PIC16F873A/876A and PIC16F874A/877A devices are provided in Figure 1-1 and Figure 1-2, respectively. The pinouts for these device families are listed in Table 1-2 and Table 1-3.

Additional information may be found in the PICmicro™ Mid-Range Reference Manual (DS33023), which may be obtained from your local Microchip Sales Representative or downloaded from the Microchip website. The Reference Manual should be considered a complementary document to this data sheet, and is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

TABLE 1-1: PIC16F87XA DEVICE FEATURES

Key Features	PIC16F873A	PIC16F874A	PIC16F876A	PIC16F877A
Operating Frequency	DC - 20 MHz	DC - 20 MHz	DC - 20 MHz	DC - 20 MHz
RESETS (and Delays)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)
FLASH Program Memory (14-bit words)	4K	4K	8K	8K
Data Memory (bytes)	192	192	368	368
EEPROM Data Memory (bytes)	128	128	256	256
Interrupts	14	15	14	15
I/O Ports	Ports A,B,C	Ports A,B,C,D,E	Ports A,B,C	Ports A,B,C,D,E
Timers	3	3	3	3
Capture/Compare/PWM modules	2	2	2	2
Serial Communications	MSSP, USART	MSSP, USART	MSSP, USART	MSSP, USART
Parallel Communications	—	PSP	—	PSP
10-bit Analog-to-Digital Module	5 input channels	8 input channels	5 input channels	8 input channels
Analog Comparators	2	2	2	2
Instruction Set	35 Instructions	35 Instructions	35 Instructions	35 Instructions
Packages	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin MLF	40-pin PDIP 44-pin PLCC 44-pin QFP	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin MLF	40-pin PDIP 44-pin PLCC 44-pin QFP

FIGURE 1-2: PIC16F874A/877A BLOCK DIAGRAM



Device	Program FLASH	Data Memory	Data EEPROM
PIC16F874A	4K words	192 Bytes	128 Bytes
PIC16F877A	8K words	368 Bytes	256 Bytes

Note 1: Higher order bits are from the STATUS register.

TABLE 1-3: PIC16F874A/877A PINOUT DESCRIPTION

Pin Name	DIP Pin#	PLCC Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKI	13	14	30	I	ST/CMOS(4)	Oscillator crystal or external clock input.
OSC1						Oscillator crystal input or external clock source input. ST buffer when configured in RC mode. Otherwise CMOS.
CLKI						External clock source input. Always associated with pin function OSC1 (see OSC1/CLKI, OSC2/CLKO pins).
OSC2/CLKOUT	14	15	31	O	—	Oscillator crystal or clock output.
OSC2						Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO						In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	1	2	18	I/P	ST	Master Clear (input) or programming voltage (output).
$\overline{MCLR}$						Master Clear (Reset) input. This pin is an active low RESET to the device.
VPP						Programming voltage input.
						PORTA is a bi-directional I/O port.
RA0/AN0	2	3	19		TTL	
RA0				I/O		Digital I/O.
AN0				I		Analog input 0.
RA1/AN1	3	4	20		TTL	
RA1				I/O		Digital I/O.
AN1				I		Analog input 1.
RA2/AN2/VREF-/CVREF	4	5	21		TTL	
RA2				I/O		Digital I/O.
AN2				I		Analog input 2.
VREF-				I		A/D reference voltage (Low) input.
CVREF				O		Comparator VREF output.
RA3/AN3/VREF+	5	6	22		TTL	
RA3				I/O		Digital I/O.
AN3				I		Analog input 3.
VREF+				I		A/D reference voltage (High) input.
RA4/T0CKI/C1OUT	6	7	23		ST	
RA4				I/O		Digital I/O – Open drain when configured as output.
T0CKI				I		Timer0 external clock input.
C1OUT				O		Comparator 1 output.
RA5/$\overline{SS}$/AN4/C2OUT	7	8	24		TTL	
RA5				I/O		Digital I/O.
$\overline{SS}$				I		SPI slave select input.
AN4				I		Analog input 4.
C2OUT				O		Comparator 2 output.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).
4: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

TABLE 1-3: PIC16F874A/877A PINOUT DESCRIPTION (CONTINUED)

Pin Name	DIP Pin#	PLCC Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
						PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs
RB0/INT	33	36	8		TTL/ST(1)	
RB0				I/O		Digital I/O.
INT				I		External interrupt.
RB1	34	37	9	I/O	TTL	Digital I/O.
RB2	35	38	10	I/O	TTL	Digital I/O.
RB3/PGM	36	39	11		TTL	
RB3				I/O		Digital I/O.
PGM				I/O		Low voltage ICSP programming enable pin.
RB4	37	41	14	I/O	TTL	Digital I/O.
RB5	38	42	15	I/O	TTL	Digital I/O.
RB6/PGC	39	43	16		TTL/ST(2)	
RB6				I/O		Digital I/O.
PGC				I/O		In-Circuit Debugger and ICSP programming clock.
RB7/PGD	40	44	17		TTL/ST(2)	
RB7				I/O		Digital I/O.
PGD				I/O		In-Circuit Debugger and ICSP programming data.
						PORTC is a bi-directional I/O port.
RC0/T1OSO/T1CKI	15	16	32		ST	
RC0				I/O		Digital I/O.
T1OSO				O		Timer1 oscillator output.
T1CKI				I		Timer1 external clock input.
RC1/T1OSI/CCP2	16	18	35		ST	
RC1				I/O		Digital I/O.
T1OSI				I		Timer1 oscillator input.
CCP2				I/O		Capture2 input, Compare2 output, PWM2 output.
RC2/CCP1	17	19	36		ST	
RC2				I/O		Digital I/O.
CCP1				I/O		Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL	18	20	37		ST	
RC3				I/O		Digital I/O.
SCK				I/O		Synchronous serial clock input/output for SPI mode.
SCL				I/O		Synchronous serial clock input/output for I²C mode.
RC4/SDI/SDA	23	25	42		ST	
RC4				I/O		Digital I/O.
SDI				I		SPI data in.
SDA				I/O		I²C data I/O.
RC5/SDO	24	26	43		ST	
RC5				I/O		Digital I/O.
SDO				O		SPI data out.
RC6/TX/CK	25	27	44		ST	
RC6				I/O		Digital I/O.
TX				O		USART asynchronous transmit.
CK				I/O		USART 1 synchronous clock.
RC7/RX/DT	26	29	1		ST	
RC7				I/O		Digital I/O.
RX				I		USART asynchronous receive.
DT				I/O		USART synchronous data.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

FIGURE 2-3: PIC16F876A/877A REGISTER FILE MAP

Bank 0	File Address	Bank 1	File Address	Bank 2	File Address	Bank 3	File Address
Indirect addr.(*)	00h	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h		105h		185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
PORTC	07h	TRISC	87h		107h		187h
PORTD(1)	08h	TRISD(1)	88h		108h		188h
PORTE(1)	09h	TRISE(1)	89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	EEDATA	10Ch	EECON1	18Ch
PIR2	0Dh	PIE2	8Dh	EEADR	10Dh	EECON2	18Dh
TMR1L	0Eh	PCON	8Eh	EEDATH	10Eh	Reserved(2)	18Eh
TMR1H	0Fh		8Fh	EEADRH	10Fh	Reserved(2)	18Fh
T1CON	10h		90h	General Purpose Register 16 Bytes	110h–11Fh	General Purpose Register 16 Bytes	190h–19Fh
TMR2	11h	SSPCON2	91h				
T2CON	12h	PR2	92h				
SSPBUF	13h	SSPADD	93h				
SSPCON	14h	SSPSTAT	94h				
CCPR1L	15h		95h				
CCPR1H	16h		96h				
CCP1CON	17h		97h				
RCSTA	18h	TXSTA	98h				
TXREG	19h	SPBRG	99h				
RCREG	1Ah		9Ah				
CCPR2L	1Bh		9Bh				
CCPR2H	1Ch	CMCON	9Ch				
CCP2CON	1Dh	CVRCON	9Dh				
ADRESH	1Eh	ADRESL	9Eh				
ADCON0	1Fh	ADCON1	9Fh				
General Purpose Register 96 Bytes	20h–7Fh	General Purpose Register 80 Bytes	A0h–EFh	General Purpose Register 80 Bytes	120h–16Fh	General Purpose Register 80 Bytes	1A0h–1EFh
		accesses 70h-7Fh	F0h–FFh	accesses 70h-7Fh	170h–17Fh	accesses 70h - 7Fh	1F0h–1FFh

▒ Unimplemented data memory locations, read as '0'.

* Not a physical register.

Note 1: These registers are not implemented on the PIC16F876A.

2: These registers are reserved, maintain these registers clear.

2.2.2.2 OPTION_REG Register

The OPTION_REG Register is a readable and writable register, which contains various control bits to configure the TMR0 prescaler/WDT postscaler (single assignable register known also as the prescaler), the External INT Interrupt, TMR0 and the weak pull-ups on PORTB.

Note:	To achieve a 1:1 prescaler assignment for the TMR0 register, assign the prescaler to the Watchdog Timer.

REGISTER 2-2: OPTION_REG REGISTER (ADDRESS 81h, 181h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

bit 7 **RBPU**: PORTB Pull-up Enable bit
1 = PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled by individual port latch values

bit 6 **INTEDG**: Interrupt Edge Select bit
1 = Interrupt on rising edge of RB0/INT pin
0 = Interrupt on falling edge of RB0/INT pin

bit 5 **T0CS**: TMR0 Clock Source Select bit
1 = Transition on RA4/T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4 **T0SE**: TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA4/T0CKI pin
0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3 **PSA**: Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS2:PS0**: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Note:	When using low voltage ICSP programming (LVP) and the pull-ups on PORTB are enabled, bit 3 in the TRISB register must be cleared to disable the pull-up on RB3 and ensure the proper operation of the device

.2.2.3 INTCON Register

The INTCON Register is a readable and writable register, which contains various enable and flag bits for the TMR0 register overflow, RB Port change and External RB0/INT pin interrupts.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-3: INTCON REGISTER (ADDRESS 0Bh, 8Bh, 10Bh, 18Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF
bit 7							bit 0

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all unmasked interrupts
0 = Disables all interrupts

bit 6 **PEIE**: Peripheral Interrupt Enable bit
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5 **TMR0IE**: TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4 **INTE**: RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt

bit 3 **RBIE**: RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2 **TMR0IF**: TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1 **INTF**: RB0/INT External Interrupt Flag bit
1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur

bit 0 **RBIF**: RB Port Change Interrupt Flag bit
1 = At least one of the RB7:RB4 pins changed state; a mismatch condition will continue to set the bit. Reading PORTB will end the mismatch condition and allow the bit to be cleared (must be cleared in software).
0 = None of the RB7:RB4 pins have changed state

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

2.2.2.1 STATUS Register

The STATUS register contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are not writable, therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect the Z, C or DC bits from the STATUS register. For other instructions not affecting any status bits, see the "Instruction Set Summary."

Note:	The C and DC bits operate as a $\overline{\text{borrow}}$ and $\overline{\text{digit borrow}}$ bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

REGISTER 2-1: STATUS REGISTER (ADDRESS 03h, 83h, 103h, 183h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C
bit 7							bit 0

bit 7 **IRP:** Register Bank Select bit (used for indirect addressing)
1 = Bank 2, 3 (100h - 1FFh)
0 = Bank 0, 1 (00h - FFh)

bit 6-5 **RP1:RP0**: Register Bank Select bits (used for direct addressing)
11 = Bank 3 (180h - 1FFh)
10 = Bank 2 (100h - 17Fh)
01 = Bank 1 (80h - FFh)
00 = Bank 0 (00h - 7Fh)
Each bank is 128 bytes

bit 4 **$\overline{\text{TO}}$**: Time-out bit
1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3 **$\overline{\text{PD}}$**: Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2 **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC**: Digit carry/$\overline{\text{borrow}}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)
(for $\overline{\text{borrow}}$, the polarity is reversed)
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result

bit 0 **C**: Carry/$\overline{\text{borrow}}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note: For $\overline{\text{borrow}}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high, or low order bit of the source register.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

TABLE 4-1: PORTA FUNCTIONS

Name	Bit#	Buffer	Function
RA0/AN0	bit0	TTL	Input/output or analog input.
RA1/AN1	bit1	TTL	Input/output or analog input.
RA2/AN2/VREF-/CVREF	bit2	TTL	Input/output or analog input or VREF- or CVREF.
RA3/AN3/VREF+	bit3	TTL	Input/output or analog input or VREF+.
RA4/T0CKI/C1OUT	bit4	ST	Input/output or external clock input for Timer0 or comparator output. Output is open drain type.
RA5/$\overline{SS}$/AN4/C2OUT	bit5	TTL	Input/output or slave select input for synchronous serial port or analog input or comparator output.

Legend: TTL = TTL input, ST = Schmitt Trigger input

TABLE 4-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
05h	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--0x 0000	--0u 0000
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111
9Ch	CMCON	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0111	0000 0111
9Dh	CVRCON	CVREN	CVROE	CVRR	—	CVR3	CVR2	CVR1	CVR0	000- 0000	000- 0000
9Fh	ADCON1	ADFM	ADCS2	—	—	PCFG3	PCFG2	PCFG1	PCFG0	--0- 0000	--0- 0000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

Note: When using the SSP module in SPI Slave mode and $\overline{SS}$ enabled, the A/D converter must be set to one of the following modes, where PCFG3:PCFG0 = `0100`, `0101`, `011x`, `1101`, `1110`, `1111`.

TABLE 4-3: PORTB FUNCTIONS

Name	Bit#	Buffer	Function
RB0/INT	bit0	TTL/ST(1)	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3/PGM(3)	bit3	TTL	Input/output pin or programming pin in LVP mode. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB6/PGC	bit6	TTL/ST(2)	Input/output pin (with interrupt-on-change) or In-Circuit Debugger pin. Internal software programmable weak pull-up. Serial programming clock.
RB7/PGD	bit7	TTL/ST(2)	Input/output pin (with interrupt-on-change) or In-Circuit Debugger pin. Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode or In-Circuit Debugger.
3: Low Voltage ICSP Programming (LVP) is enabled by default, which disables the RB3 I/O function. LVP must be disabled to enable RB3 as an I/O pin and allow maximum compatibility to the other 28-pin and 40-pin mid-range devices.

TABLE 4-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
06h, 106h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
86h, 186h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
81h, 181h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

TABLE 4-5: PORTC FUNCTIONS

Name	Bit#	Buffer Type	Function
RC0/T1OSO/T1CKI	bit0	ST	Input/output port pin or Timer1 oscillator output/Timer1 clock input.
RC1/T1OSI/CCP2	bit1	ST	Input/output port pin or Timer1 oscillator input or Capture2 input/ Compare2 output/PWM2 output.
RC2/CCP1	bit2	ST	Input/output port pin or Capture1 input/Compare1 output/ PWM1 output.
RC3/SCK/SCL	bit3	ST	RC3 can also be the synchronous serial clock for both SPI and I^2C modes.
RC4/SDI/SDA	bit4	ST	RC4 can also be the SPI Data In (SPI mode) or Data I/O (I^2C mode).
RC5/SDO	bit5	ST	Input/output port pin or Synchronous Serial Port data output.
RC6/TX/CK	bit6	ST	Input/output port pin or USART Asynchronous Transmit or Synchronous Clock.
RC7/RX/DT	bit7	ST	Input/output port pin or USART Asynchronous Receive or Synchronous Data.

Legend: ST = Schmitt Trigger input

TABLE 4-6: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
07h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111

Legend: x = unknown, u = unchanged

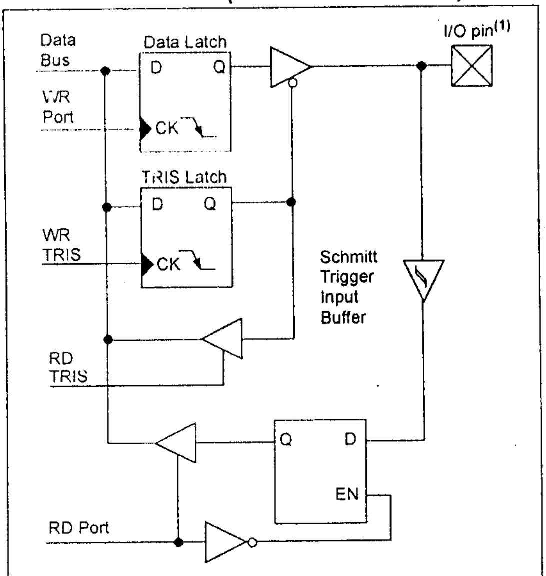
.4 PORTD and TRISD Registers

Note:	PORTD and TRISD are not implemented on the 28-pin devices.

ORTD is an 8-bit port with Schmitt Trigger input buff-
s. Each pin is individually configureable as an input or
itput.

ORTD can be configured as an 8-bit wide micropro-
essor port (parallel slave port) by setting control bit
SPMODE (TRISE<4>). In this mode, the input buffers
re TTL.

FIGURE 4-8: PORTD BLOCK DIAGRAM (IN I/O PORT MODE)



Note 1: I/O pins have protection diodes to VDD and Vss.

ABLE 4-7: PORTD FUNCTIONS

Name	Bit#	Buffer Type	Function
RD0/PSP0	bit0	ST/TTL(1)	Input/output port pin or parallel slave port bit0.
RD1/PSP1	bit1	ST/TTL(1)	Input/output port pin or parallel slave port bit1.
RD2/PSP2	bit2	ST/TTL(1)	Input/output port pin or parallel slave port bit2.
RD3/PSP3	bit3	ST/TTL(1)	Input/output port pin or parallel slave port bit3.
RD4/PSP4	bit4	ST/TTL(1)	Input/output port pin or parallel slave port bit4.
RD5/PSP5	bit5	ST/TTL(1)	Input/output port pin or parallel slave port bit5.
RD6/PSP6	bit6	ST/TTL(1)	Input/output port pin or parallel slave port bit6.
RD7/PSP7	bit7	ST/TTL(1)	Input/output port pin or parallel slave port bit7.

Legend: ST = Schmitt Trigger input, TTL = TTL input
Note 1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffers when in Parallel Slave Port mode.

ABLE 4-8: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
08h	PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx xxxx	uuuu uuuu
88h	TRISD	PORTD Data Direction Register								1111 1111	1111 1111
89h	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Data Direction Bits			0000 -111	0000 -111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTD.

+5V-Powered, Multichannel RS-232 Drivers/Receivers

ABSOLUTE MAXIMUM RATINGS—MAX220/222/232A/233A/242/243

Supply Voltage (V_{CC}) ....-0.3V to +6V
Input Voltages
T_{IN}...-0.3V to (V_{CC} - 0.3V)
R_{IN} (Except MAX220) ....±30V
R_{IN} (MAX220)..±25V
T_{OUT} (Except MAX220) (Note 1) ....±15V
T_{OUT} (MAX220)...±13.2V
Output Voltages
T_{OUT}...±15V
R_{OUT}..-0.3V to (V_{CC} + 0.3V)
Driver/Receiver Output Short Circuited to GND.........Continuous
Continuous Power Dissipation (T_A = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C)....842mW
18-Pin Plastic DIP (derate 11.11mW/°C above +70°C)....889mW
20-Pin Plastic DIP (derate 8.00mW/°C above +70°C) ..440mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) ...696mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C)......762mW
18-Pin Wide SO (derate 9.52mW/°C above +70°C)......762mW
20-Pin Wide SO (derate 10.00mW/°C above +70°C)....800mW
20-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C).....800mW
18-Pin CERDIP (derate 10.53mW/°C above +70°C).....842mW
Operating Temperature Ranges
MAX2_ _AC_ _, MAX2_ _C_ _ ....0°C to +70°C
MAX2_ _AE_ _, MAX2_ _E_ _ ....-40°C to +85°C
MAX2_ _AM_ _, MAX2_ _M_ _.........................-55°C to +125°C
Storage Temperature Range ....-65°C to +160°C
Lead Temperature (soldering, 10sec) ....+300°C

Note 1: Input voltage measured with T_{OUT} in high-impedance state, $\overline{SHDN}$ or V_{CC} = 0V.
Note 2: For the MAX220, V+ and V- can have a maximum magnitude of 7V, but their absolute difference cannot exceed 13V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX220/222/232A/233A/242/243

(V_{CC} = +5V ±10%, C1–C4 = 0.1μF, MAX220, C1 = 0.047μF, C2–C4 = 0.33μF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RS-232 TRANSMITTERS						
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to GND		±5	±8		V
Input Logic Threshold Low				1.4	0.8	V
Input Logic Threshold High	All devices except MAX220		2	1.4		V
	MAX220: V_{CC} = 5.0V		2.4			
Logic Pull-Up/Input Current	All except MAX220, normal operation			5	40	μA
	$\overline{SHDN}$ = 0V, MAX222/242, shutdown, MAX220			±0.01	±1	
Output Leakage Current	V_{CC} = 5.5V, $\overline{SHDN}$ = 0V, V_{OUT} = ±15V, MAX222/242			±0.01	±10	μA
	V_{CC} = $\overline{SHDN}$ = 0V, V_{OUT} = ±15V			±0.01	±10	
Data Rate				200	116	kb/s
Transmitter Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V		300	10M		Ω
Output Short-Circuit Current	V_{OUT} = 0V		±7	±22		mA
RS-232 RECEIVERS						
RS-232 Input Voltage Operating Range					±30	V
RS-232 Input Threshold Low	V_{CC} = 5V	All except MAX243 $R2_{IN}$	0.8	1.3		V
		MAX243 $R2_{IN}$ (Note 2)	-3			
RS-232 Input Threshold High	V_{CC} = 5V	All except MAX243 $R2_{IN}$		1.8	2.4	V
		MAX243 $R2_{IN}$ (Note 2)		-0.5	-0.1	
RS-232 Input Hysteresis	All except MAX243, V_{CC} = 5V, no hysteresis in shdn.		0.2	0.5	1	V
	MAX243			1		
RS-232 Input Resistance			3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 3.2mA			0.2	0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1.0mA		3.5	V_{CC} - 0.2		V
TTL/CMOS Output Short-Circuit Current	Sourcing V_{OUT} = GND		-2	-10		mA
	Shrinking V_{OUT} = V_{CC}		10	30		

ELECTRICAL CHARACTERISTICS—MAX220/222/232A/233A/242/243 (continued)

(V_{CC} = +5V ±10%, C1–C4 = 0.1µF, MAX220, C1 = 0.047µF, C2–C4 = 0.33µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TTL/CMOS Output Leakage Current	$\overline{SHDN}$ = V_{CC} or EN = V_{CC} ($\overline{SHDN}$ = 0V for MAX222), 0V ≤ V_{OUT} ≤ V_{CC}			±0.05	±10	µA
$\overline{EN}$ Input Threshold Low	MAX242			1.4	0.8	V
$\overline{EN}$ Input Threshold High	MAX242		2.0	1.4		V
Operating Supply Voltage			4.5		5.5	V
V_{CC} Supply Current ($\overline{SHDN}$ = V_{CC}), Figures 5, 6, 11, 19	No load	MAX220		0.5	2	mA
		MAX222/232A/233A/242/243		4	10	
	3kΩ load both inputs	MAX220		12		
		MAX222/232A/233A/242/243		15		
Shutdown Supply Current	MAX222/242	T_A = +25°C		0.1	10	µA
		T_A = 0°C to +70°C		2	50	
		T_A = -40°C to +85°C		2	50	
		T_A = -55°C to +125°C		35	100	
$\overline{SHDN}$ Input Leakage Current	MAX222/242				±1	µA
$\overline{SHDN}$ Threshold Low	MAX222/242			1.4	0.8	V
$\overline{SHDN}$ Threshold High	MAX222/242		2.0	1.4		V
Transition Slew Rate	C_L = 50pF to 2500pF, R_L = 3kΩ to 7kΩ, V_{CC} = 5V, T_A = +25°C, measured from +3V to -3V or -3V to +3V	MAX222/232A/233A/242/243	6	12	30	V/µs
		MAX220	1.5	3	30	
Transmitter Propagation Delay TLL to RS-232 (normal operation), Figure 1	t_{PHLT}	MAX222/232A/233A/242/243		1.3	3.5	µs
		MAX220		4	10	
	t_{PLHT}	MAX222/232A/233A/242/243		1.5	3.5	
		MAX220		5	10	
Receiver Propagation Delay RS-232 to TLL (normal operation), Figure 2	t_{PHLR}	MAX222/232A/233A/242/243		0.5	1	µs
		MAX220		0.6	3	
	t_{PLHR}	MAX222/232A/233A/242/243		0.6	1	
		MAX220		0.8	3	
Receiver Propagation Delay RS-232 to TLL (shutdown), Figure 2	t_{PHLS}	MAX242		0.5	10	µs
	t_{PLHS}	MAX242		2.5	10	
Receiver-Output Enable Time, Figure 3	t_{ER}	MAX242		125	500	ns
Receiver-Output Disable Time, Figure 3	t_{DR}	MAX242		160	500	ns
Transmitter-Output Enable Time ($\overline{SHDN}$ goes high), Figure 4	t_{ET}	MAX222/242, 0.1µF caps (includes charge-pump start-up)		250		µs
Transmitter-Output Disable Time ($\overline{SHDN}$ goes low), Figure 4	t_{DT}	MAX222/242, 0.1µF caps		600		ns
Transmitter + to - Propagation Delay Difference (normal operation)	t_{PHLT} - t_{PLHT}	MAX222/232A/233A/242/243		300		ns
		MAX220		2000		
Receiver + to - Propagation Delay Difference (normal operation)	t_{PHLR} - t_{PLHR}	MAX222/232A/233A/242/243		100		ns
		MAX220		225		

Note 3: MAX243 $R2_{OUT}$ is guaranteed to be low when $R2_{IN}$ is ≥ 0V or is floating.