THREE – PHASE SINE WAVE INVERTER USING ZVS AND EMBEDDED CONTROLLER FOR MODERN INDUSTRIAL DRIVES

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BONAFIDE CERTIFICATE

Certified that this project report titled **THREE PHASE SINE WAVE INVERTER USING ZVS AND EMBEDDED CONTROLLER FOR MODERN INDUSTRIAL DRIVES** is the bonafide work of Ms. **T.NITHYA** who carried out the research under my supervision. Certified further, that to the best of my knowledge the work reported herein does not form part of any other report or dissertation on the basis of which a degree or award was conferred on an earlier occasion on this or any other candidate.

PROJECT GUIDE

HEAD OF THE DEPARTMENT

The candidate with University Register No: 71203415009 was examined by us in the project viva – voce examination held on 23.6.05

INTERNAL EXAMINER

EXTERNAL EXAMINER 23/6/05

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CHAPTER – 1

INTRODUCTION

This project presents a new approach to device switching. It is easily shown that maximum device stresses and switching losses occur when switching OFF a stiff dc bus. In the concept presented here, the dc bus is made to oscillate at a high frequency so that the bus voltage passes through periodic zero crossings, thus setting up ideal switching conditions for all devices and moderately sized reactive elements.

IGBT is a newly developed element in the area of power electronics. This device combines into it the advantages of both MOSFET and BJT. So an IGBT has high input impedance like a MOSFET and low-on-state power loss as in a BJT. IGBT is free from second breakdown problem present in BJT. It is constructed in the same manner as a power MOSFET. But there is a major difference in the substrate. The n+ layer substrate at the drain in the power MOSFET is now substituted in the IGBT by a p+ layer substrate called collector. Like power MOSFET, an IGBT has also thousands of basic structure cells connected appropriately on a single chip of silicon.

The output characteristics of an IGBT show the plot of collector current versus collector – emitter voltages for various values of gate – emitter voltages. In the forward direction, the shape of the output characteristics is similar to that of BJT. But here the controlling parameter is gate – emitter voltage because IGBT is voltage controlled device.

the transfer characteristic of an IGBT is a plot of collector current versus gate – emitter voltage. This characteristic is identical to that of power MOSFET. IGBTs are widely used in medium power applications such as dc and ac motor drives, UPS systems, power supplies and drives for solenoids, relays and contactors. Though IGBTs are more expensive than BJTs, yet they are becoming popular because of, Lower gate – drive requirements, Lower switching losses. IGBT converters are more efficient with less size as well as cost, as compared to converters based on BJTs. Recently, IGBT inverter induction – motor drives using high switching frequency are finding favor where audio – noise is objectionable. In most applications, IGBTs will eventually push out BJTs.

1.1.OUTLINE OF PROJECT REPORT

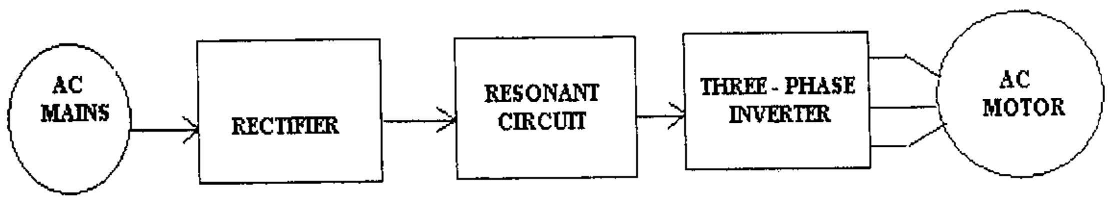


Fig: 1.1. Block diagram

There are three main blocks in the block diagram shown above. One is the power supply. The other is the resonant circuit and the third one is the three-phase inverter circuit. The power supply may be either single phase or three- phase. Rectifier is used to convert A.C to D.C. Resonant circuit consists of L and C component. The input voltage is made to oscillate by means of an LC resonance. So that the input voltage remains zero for a finite duration and hence during that period the status of the switches are changed, resulting in zero – voltage switching. Three phase inverter circuit consists of three legs, one for each phase. The output of each leg depends only on Vs and the switch status. AC motor load or RL load can be used. The switching sequence of IGBT is controlled by means of PIC microcontroller – Peripheral Interface Controller. The circuit is simulated and the output results are obtained using sim power system toolbox of MATLAB simulink.

CHAPTER – 2

PROJECT DESCRIPTION

2.1. HARD SWITCHING TOPOLOGY

Today, the power converter topology of choice for AC output applications is the HARD SWITCHING dc/ac voltage source inverter shown in fig. 2.1. The AC output voltage is synthesized using a pulse width modulated (PWM) switching waveform, which has controlled amplitude low – frequency 'fundamental' component, and high – frequency modulation components. The modulation components of the current are filtered by the low pass characteristic of typical inductive power electronic loads.

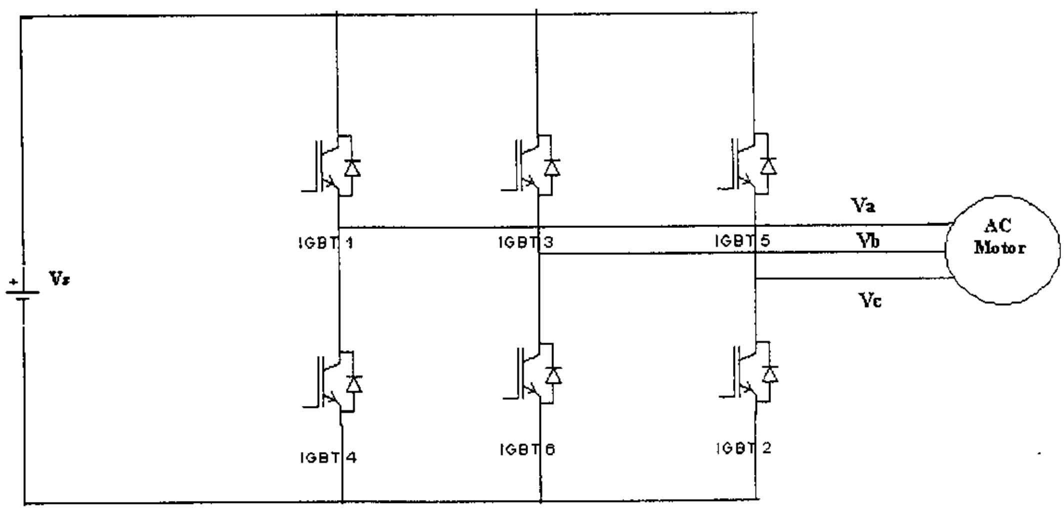


Fig: 2.1. Conventional Voltage Source Inverter

A key factor in reducing the size of reactive components used for filtering and energy storage, improving transient performance and meeting stringent harmonic specifications is the switching frequency of the inverter. Although the IGBTs switch rapidly, switching losses occur due to the transient existence of both voltage across, and current in the device. These stresses require significant device derating for switching frequencies in excess of 5 – 6 KHZ, thus increasing system cost. In addition IGBT losses are further increased at turn – ON by the charge stored in the complementary switch's anti – parallel diode and at turn – OFF by the energy trapped in the parasitic inductance of the IGBT package and device interconnections.

Another issue is the transient on the inverter output voltage caused by IGBT switching, resulting in dv/dt's in excess of 5 – 10,000 volts/µs. Impressing such high dv/dt across motor loads can cause severe problems and result in transient voltages of twice the nominal value across motor windings, which can cause winding insulation breakdown. Also associated with the high switching speed is the broadband electro magnetic interference (EMI) that is generated on the inverter output. It is really very difficult to suppress this EMI. In applications such as uninterruptible ac power supplies and AC motor drives, three phase inverters are commonly used to supply three phase loads. It is possible to supply a three phase load by means of three separate single phase inverters, where each inverter produces an output displaced by 120° with respect to each other. Though this arrangement may be preferable under certain conditions, it requires either a three phase output transformer or separate access to each of the three phases of the load.

The most frequently used three phase inverter circuit consists of three legs, one for each phase, as shown in fig. 2.1. Each inverter leg is similar to the one used for single phase inverter. Therefore, the output of each leg depends only on V_d and the switch status; the output voltage is independent of the output load current since one of the two switches in a leg is always on at any instant. The objective in pulse width modulated three-phase inverter is to shape and control the three phase output voltages in magnitude and frequency with an essentially constant input voltage V_d. To obtain balanced three phase output voltages in a three phase PWM inverter, the triangular voltage waveform is compared with three sinusoidal control voltages that are 120° out of phase.

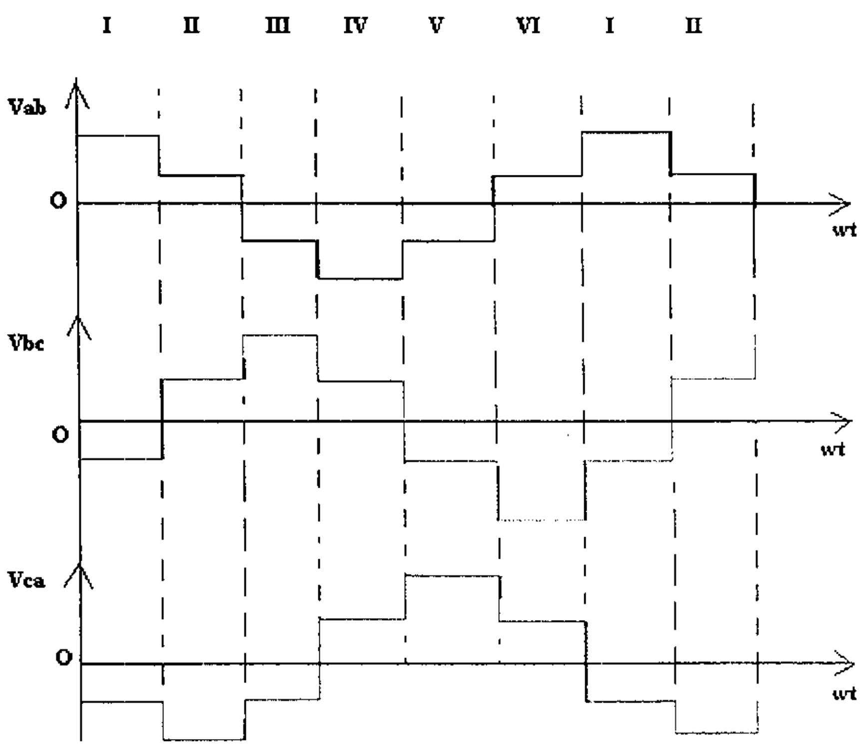


Fig: 2.2.Voltage waveforms for 120°mode 3 – phase VSI

For the 120° mode VSI, each thyristor conducts for 120° of a cycle. It requires six steps, each of 60° duration, for completing one cycle of the output AC voltage. During each step, only two thyristors conduct for this inverter.

2.2. SOFT SWITCHING TECHNIQUES

One technique that has demonstrated promise in obtaining improved system performance is soft switching. Soft switching converters constrain the switching of power devices to time intervals when the voltage across the device, or the current through it is nearly zero. This significantly reduces the device switching losses and hence allows higher switching frequencies and wider control bandwidths, while simultaneously lowering dv/dt and electromagnetic interference (EMI) problems.

The use of soft switching in dc/dc converters and induction heating for industrial applications is fairly common and widespread. Soft switching in dc/dc converters is fairly simple to realize, because at any given operating point, power flow is unidirectional, the switching frequency is fixed, and modulation is at zero frequency, i.e. dc. The task of realizing soft switching in dc/ac inverters is considerably more complex. This is primarily because unlike most dc/dc converters, inverters require bi-directional power flow between the dc bus and the ac output, and typically have two distinct operating frequencies, one associated with modulation and the other with the fundamental output frequency. Further, soft switching operation is required over a much wider range of load conditions.

Soft switching inverters are generally classified into two distinct categories: resonant link and resonant pole inverters. Resonant link inverters tend to use one set of resonant components per inverter, and achieve low loss switching of all its power semiconductors using a common zero voltage (or current) crossing point. Known configurations include the passively clamped and actively clamped resonant dc link inverters, and various forms of quasi-resonant dc link inverters. Resonant pole inverters, on the other hand, tend to use one set of reactive L-C components per inverter phase. Known forms include the basic resonant pole inverter, the auxiliary resonant commutated pole inverter and various forms of resonant snubber circuits.

While soft switching circuits can be of both the zero voltage or zero current switching types, and often include both types, this paper will focus on configurations which realize a voltage source inverter function and primarily use zero voltage switching of the main devices.

In all the pulse width modulated dc to dc and dc to ac converter topologies, the controllable switches are operated in a switch mode where they are required to turn ON and turn OFF the entire load current during each switching. In this switch mode operation, the switches are subjected to high switching stresses and high switching power loss that increases linearly with the switching frequency of the PWM. Another significant drawback of the switch mode operation is the EMI produced due to large di/dt and dv/dt caused by a switch mode operation. These shortcomings of switch mode converters are exacerbated if the switching frequency is increased in order to reduce the converter size and weight and hence to increase the power density. Therefore, to realize high switching frequencies in converters, the aforementioned shortcomings are minimized if each switch in a converter changes its status when the voltage across it and/or the current through it is zero at the switching instant. Since most of these topologies require some form of LC resonance, these are broadly classified as “resonant converters”.

The average value of the switching loss is proportional to the switching frequency, limits how high the switching frequency can be pushed without significantly degrading the system efficiency. With the availability of fast switches, the present limit seems to be up to approximately 500 KHz with a reasonable energy efficiency. Another significant disadvantage of the switch mode operation is that it results in large di/dt and dv/dt due to fast switching transitions required to keep the switching losses in the switch as low as possible. Diodes with poor reverse recovery characteristics significantly add to this phenomenon, which produces EMI. Switch mode inductive current switching results in switching loci in the V – I plane as shown in the fig 2.3.

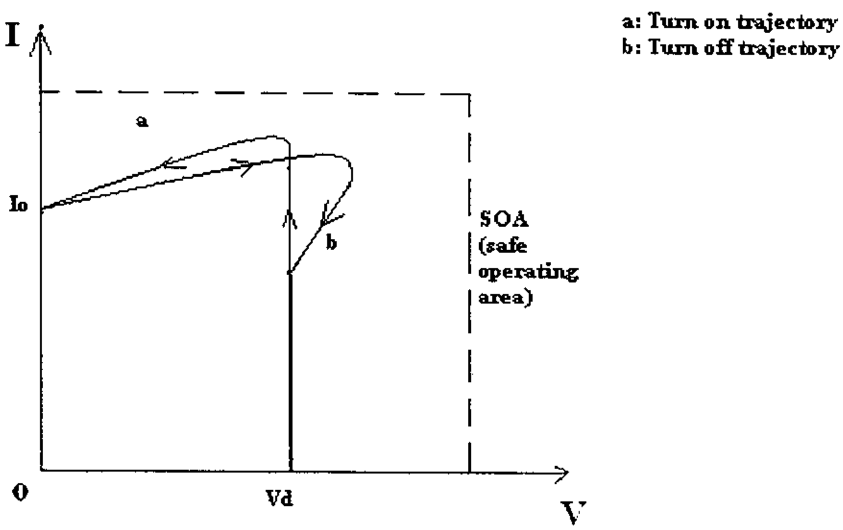


Fig: 2.3.Switch mode inductive current switching.

Because a large switch voltage and a large switch current occur simultaneously, the switch must be capable of withstanding high switching stresses, with a safe operating area (SOA) as shown by the dashed lines. This requirement to be able to withstand such large stresses results in undesirable design compromises in other characteristics of the power semiconductor devices. The switching frequencies can be increased to such high values only if the problems of switch stresses, switching losses, and the EMI associated with the switch mode converter can be overcome. The switch stresses can be reduced by connecting simple dissipative snubber circuits in series and parallel with the switches in the switch mode converter. However these dissipative snubbers shift the switching power loss from the switch to the snubber circuit and therefore do not provide a reduction in the overall switching power loss.

The switching loci that result in reduced switch stresses are shown in fig 2.4.

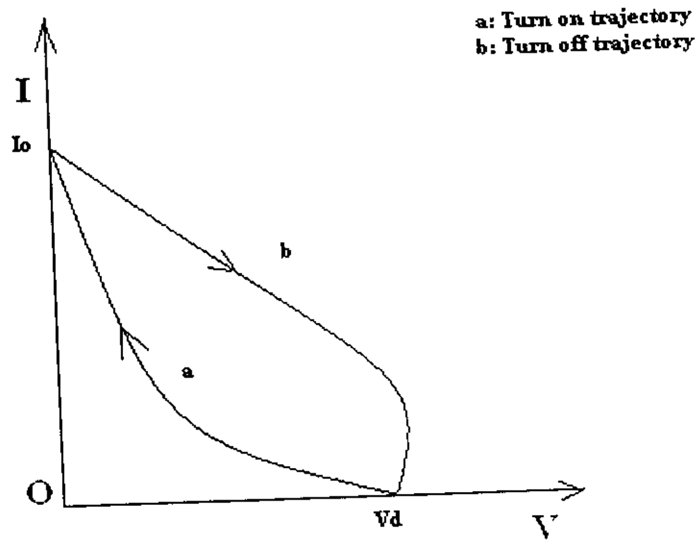


Fig: 2.4. Switching loci with snubbers.

In contrast to dissipative snubbers in switch mode converters, the combination of proper converter topologies and switching strategies can overcome the problems of switching stresses, switching power losses, and the EMI by turning ON and turning OFF each of the converter switches when either the switch voltage or the switch current is zero. Ideally, both the switch voltage and current should be zero when the switching transition occurs. If both the turn ON and turn OFF switching occur under a zero voltage and/or a zero current condition, then the switching loci are shown in fig: 2.5, where the switching loci in the switch mode are shown by dashed curves for comparison purposes. Such switching loci, without dissipative snubbers, reduce switch stresses, switching power losses, and the EMI.

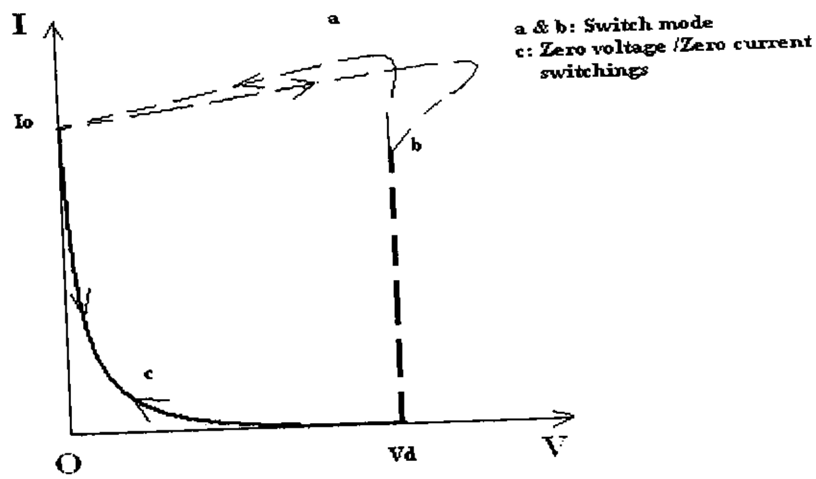


Fig: 2.5. Zero voltage/Zero current switching loci.

2.3. CLASSIFICATION OF RESONANT CONVERTERS

The resonant converters are defined here as the combination of converter topologies and switching strategies that result in zero voltage and/or zero current switching. One way to categorize these converters is as follows:

1. Load resonant converters.
2. Resonant switch converters.
3. Resonant dc link converters.
4. High frequency link integral half cycle converters.

These classifications are explained further.

1. Load resonant converters: These converters consist of an LC resonant tank circuit. Oscillating voltage and current, due to LC resonance in the tank are applied to the load, and the converter switches can be switched at zero voltage and /or zero current. Either a series LC or a parallel LC circuit can be used. In these converter circuits, the power flow to the load is controlled by the resonant tank impedance which in turn is controlled by the switching frequency, in comparison to the resonant frequency of the tank. These dc to dc and dc to ac converters can be sub classified as follows.

1. Voltage source series resonant converters.
    a. Series loaded resonant converters.
    b. Parallel loaded resonant converters.
    c. Hybrid resonant converters.
2. Current source parallel resonant converters.
3. Class E and Subclass E resonant converters.

2. Resonant switch converters: In certain switch mode converter topologies, and LC resonance can be utilized primarily to shape the switch voltage and current to provide zero voltage and/or zero current switching. In such resonant switch converters, during one switching frequency time period, there are resonant as well as non-resonant operating intervals. Therefore these converters in the literature have also been termed Quasi resonant converters. They can be sub classified as follows.

1. Resonant switch dc-to-dc converters.
    a. Zero current switching converters.
    b. Zero voltage switching converters.
2. Zero voltage switching, clamped voltage converters.

3. Resonant dc link converters: In the conventional switch mode PWM dc to ac inverters, the input voltage to the inverter is a fixed magnitude dc, and the sinusoidal output is obtained by switch mode PWM switching. However, in the resonant dc link converters the input voltage is made to oscillate around input voltage by means of an LC resonance so that the input voltage remains zero for a finite duration during which the status of the inverter switches can be changed, thus resulting in zero voltage switchings.

4. High frequency link integral half cycle converters: If the input to a single phase or three phase inverter is a high frequency sinusoidal ac, then by using bi-directional switches it is possible to synthesize a low frequency ac of adjustable magnitude and frequency or an adjustable magnitude dc, where the switches are turned ON and OFF at the zero crossings of the input voltage.

2.4.COMPARISON OF HARD AND SOFT SWITCHING TECHNIQUES

The high speed switching that occurs in power converter designs leads to more electromagnetic energy being radiated at levels that can easily exceed the maximum allowable limits. Therefore utilization of "Soft Switching" (ZVS) helps to successfully meet international standards.

"Soft Switching" is relatively a new technique which uses circuit resonance to ensure that power semiconductor devices switch at a zero voltage level. This reduces the stress on the part, and also greatly reduces the high frequency energy that would otherwise be radiated as RF noise.

Traditional high frequency switch mode supplies, which rely on generating an AC waveform in the range of 100 KHz to 200 KHz to drive the main power transformer, have used power transistors to "hard switch" the unregulated input voltage at this rate. This means that a transistor turning on will have the whole raw input voltage, typically in the range of 350 V, across it as it changes state. During the actual switching interval (less than 0.5μsec) there is a finite period as the transistor begins to conduct where the voltage begins to fall at the same time as current begins to flow. This simultaneous presence of voltage across the transistor and current through it means that, during this period, power is being dissipated within the device. A similar event occurs as the transistor turns off, with the full current flowing through it as shown in fig. 2.6.

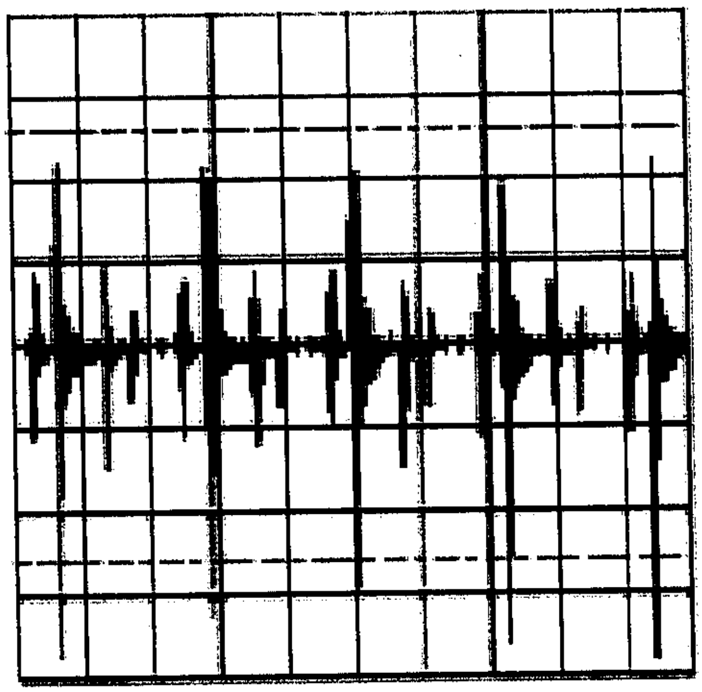


Fig.2.6. "Hard Switching" topology power loss waveform. (Showing high instantaneous peak power loss during each switching cycle).

Designers that use a hard switching topology are in a no – win situation when they try to reduce wasted power. As the switching period is reduced through the use of improved driving circuitry, the faster rise and fall times generate more high frequency energy that is radiated and conducted out of the unit as unacceptable radio frequency interference (RFI). If the rise and fall times are intentionally slowed to reduce the radio frequency interference the power losses in the transistor increase proportionally increasing the thermal stress on the part, thus reducing its life span. In this way, hard switching topology is a compromise between electrical efficiency reduction and noise trade offs.

More recently, new power conversion topologies have been developed which dramatically reduce the power dissipated by the main power transistors during the switching interval, while at the same time merely eliminating much of the generated radio frequency energy, or high frequency noise. The most common technique employed has been a constant frequency resonant switching scheme, which ensures that the actual energy being dissipated by the active device is reduced to nearly zero. This method commonly called "zero voltage switching – ZVS or Soft Switching" uses a capacitor and an inductor as a resonant circuit. This resonant circuit and an appropriate switching sequence allows the voltage across each transistor to swing to zero before the device turns ON and current flows. Likewise, at turn OFF, the voltage differential across the transistor swings to zero before its driven to a non – conducting state.

With this scheme, current is only flowing through the transistors when they are fully on, and doing useful work transferring energy to the output of the supply. The power dissipation within the transistor that would normally occur during the switching interval has effectively been eliminated as shown in fig. 2.7.

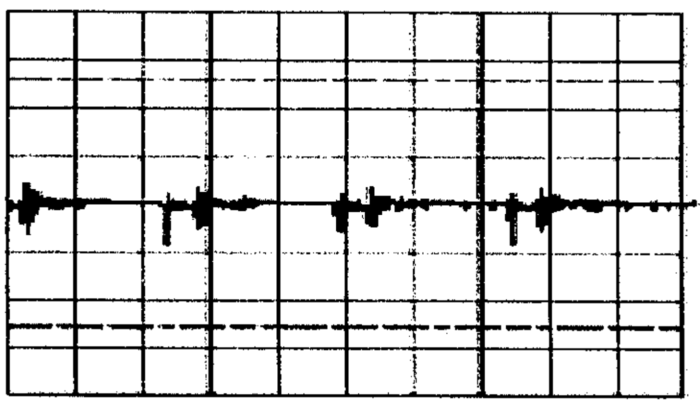


Fig. 2.7. "Soft Switching" topology power loss waveform (Showing instantaneous peak power loss to be reduced to less than one – quarter level in "hard – switching" version).

Unwanted high frequency voltage and current transients during the switching period – the culprits that supply much of the RF noise radiated and conducted out of the power supply are also dramatically reduced at its source, enhancing filtering at the input and output of the unit ensures that the unit is well within the noise limits set by international standards. With soft switching techniques, reduction in wasted power will often improve the frequency. Reducing the power loss here lowers their junction temperature giving increased thermal operating margins and has a longer life and significantly generates less electrical noise, achieves greater frequency and higher immunity to the effects of other equipment operating near by.

2.5. RESONANT DC LINK INVERTER (ZVS)

One of the earliest and most mature of a large number of soft switching inverter topologies that have been proposed is the resonant dc link (RDCL) inverter. The basic version of the resonant dc link inverter is shown in fig. 2.8.

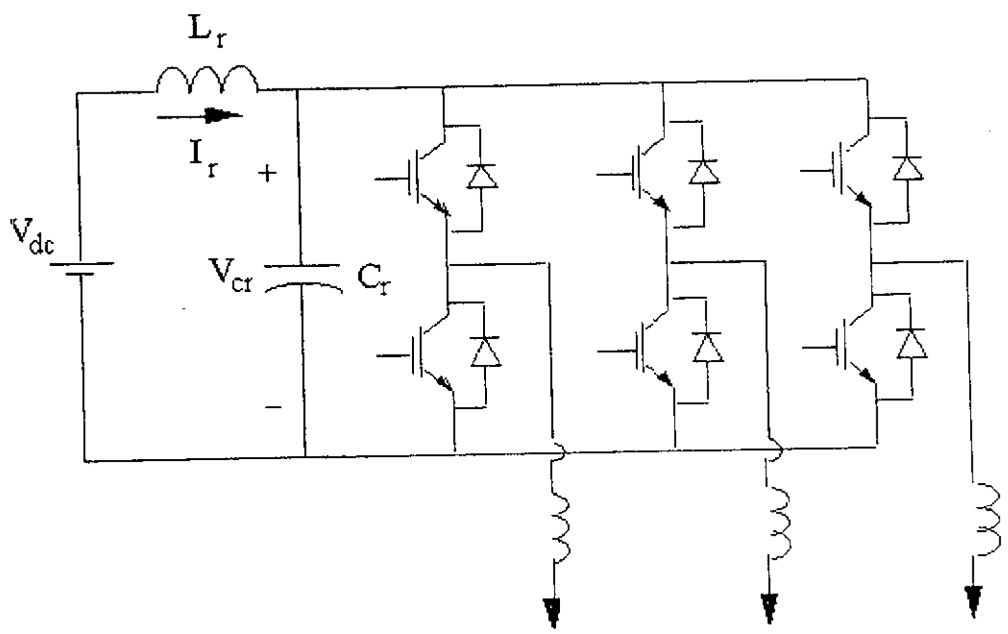


Fig. 2.8. Resonant DC Link Inverter (RDCLI).

In the RDCLI, the voltage across the resonant capacitor is also impressed across the six power devices. This voltage has an average or dc value which is equal to the dc bus, V_{dc}, and an oscillating or resonant component. The combined voltage is referred to as the resonant link. The resonant link is 'excited' and maintains resonance through appropriate control of the inverter switches such that the resonating dc bus voltage periodically reaches zero volts. Switching of the devices is synchronized to the link zero crossings to obtain the desired low switching loss.

The main inverter devices are allowed to change state at the link voltage zero crossings. This forces the inverter output to consist of an integral number of resonant link voltage pulses, a significantly different strategy from the pulse width modulation used in conventional hard switching inverters. The desired low frequency output voltage now has to be synthesized using discrete pulse modulation (DPM). Typical low voltage synthesis is shown in fig. 2.9.

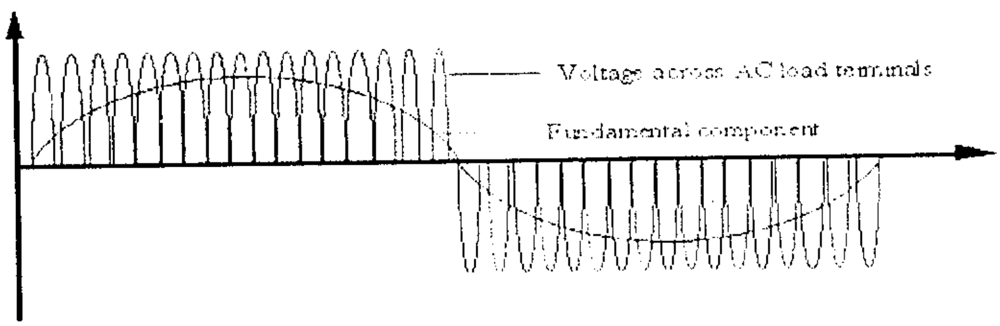


Fig. 2.9. Typical line – to – line voltage synthesis using DPM

In order to simplify the analysis of a RDCLI, and since the resonant frequency is much higher than the fundamental frequency of the synthesized waveform, an equivalent circuit of the system during each resonant pulse is shown in fig. 2.10. Note here that the load current I_x, is assumed to be constant during resonant pulse duration.

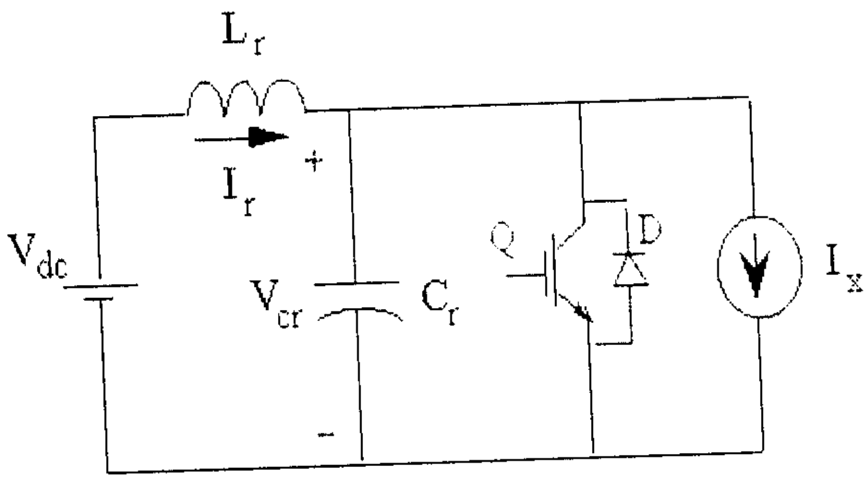


Fig. 2.10. Simplified circuit of RDCLI

If the switch Q is turned off, applying Vdc to the circuit results in a resonant cycle and the capacitor voltage Vcr is given by,

$$Vcr\ (t) = Vdc\ (1 - \cos\ \ t) \qquad (2.1)$$

Where, is the resonant frequency of the LC circuit. When t = 2p, the capacitor voltage goes back to zero setting up a zero voltage switching condition for the switch Q. When the switch is turned on, the inductor current will ramp up in a linear fashion. Sufficient energy has to be stored in Lr before the switch is turned off to ensure that the capacitor voltage with return to zero. Typical waveforms with zero load current are shown in fig. 2.11.

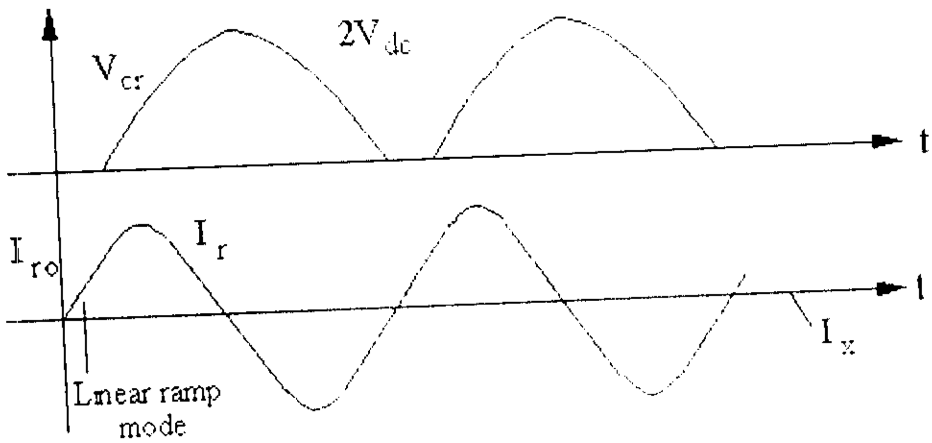


Fig. 2.11. Typical waveforms of the RDCLI with $I_x = 0$

The value of the current I_x depends on the individual phase currents and the switching functions of the six-inverter devices. Here the I_x can change significantly from a switching cycle to the next depending on the switching strategy. However, during the resonant cycle itself, I_x remains fairly constant since the inverter states are preserved. In order to ensure ZVS, the inverter actively controls the current ($I_r - I_x$) to ensure that the resonant cycle is controlled in a deadbeat fashion and is independent of the value of I_x. As devices are switched, the LC resonant circuit excitation initial condition is changed. This can result in high peak voltage stresses. Typically, the main devices voltage stress in a RDCLI is $2V_{dc}$. Consequently, the resonant dc link circuit is always used with a means to limit the peak voltage stress across the device. Two possible variations include the passively clamped and the actively clamped resonant dc link inverters.

For the resonant dc link inverter, one resonant circuit is used to provide soft switching for the entire inverter. As the name resonant dc link hints, it is the DC link which is forced to oscillate. This means that the resonance circuit is located on the DC link side and not on the load side of the converter. This is very useful, especially for three phase converters since otherwise, one resonant circuit for each half bridge would be required. The idea of the resonant DC link inverter is that the switch state of the inverter only should be changed at or close to zero link voltage. The resonant circuit is formed by the resonant inductor Lr and the resonant capacitor Cr. Since the DC link capacitor has a much higher capacitance than Cr, it does not affect the resonance behaviour. In other words, the DC link capacitor can be regarded as a constant voltage source.

Assume that a resonant cycle starts at a capacitor voltage equal to twice the DC link voltage V_{dc}. Due to the resonant properties of this circuit the capacitor voltage decreases towards zero. When the voltage across Cr passes the level of the DC link voltage the inductor current is close to its minimum value. When the capacitor voltage reaches zero, it will be clamped to this level due to the fact that the load current freewheels through the freewheeling diodes, at least if the resonant inductor current is lower than the load current which is the case if no switching is performed. As soon as the inductor current reaches the level of the load current, the capacitor voltage starts up to ramp up. When the voltage across Cr passes the level of the DC link voltage the inductor current is at its maximum value. For the case where the output current is not changed, the capacitor voltage reaches the starting point of the analysis, which equals twice the DC link voltage.

The normalized resonant waveforms for the case of changing output current are shown in fig. 2.12. From fig. 2.12, first, when the output current is decreased due to a change of the inverter switch state, the resonant DC link voltage resonates to a peak value higher than twice the DC link voltage Vdc. Second, when the output current is increased, the zero voltage interval is prolonged and the resonant capacitor voltage increases with a moderate derivative, to a peak value close to twice the DC link voltage V_{dc}.

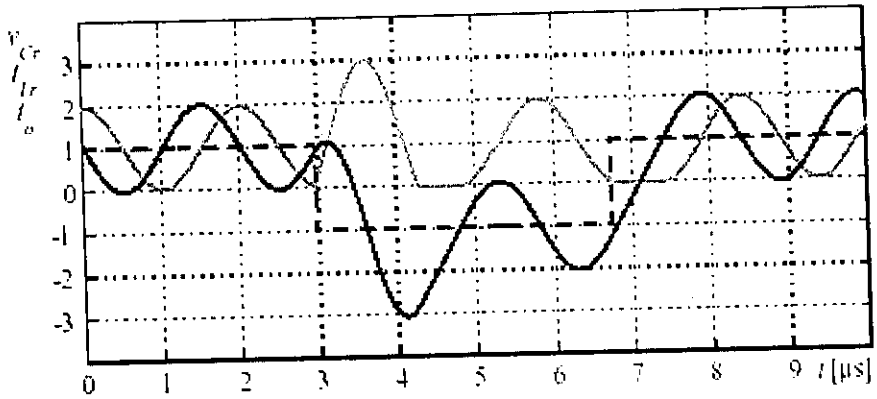


Fig. 2.12. Normalized inductor current (black) and resonant link voltage (grey) for a resonant DC link inverter. The current fed to the inverter is also shown (dashed).

In the first case, there is excess energy stored in the resonant inductor due to the previously high current through Lr, corresponding to the load current. This energy must decrease to meet the new output current, which implies that the energy must be transferred to the resonant capacitor Cr. This excess energy thus results in a high voltage across the capacitor. By increasing the capacitance and decreasing the inductance, the peak capacitor voltage is decreased. However, the same action increases the magnitude of the resonant current through Lr.

In the second case, a too small amount of energy is stored in the inductor, which results in a prolonged zero voltage interval. The length of the zero voltage interval is determined by the time needed for the inductor current to reach the same level as the inverter current. When the inductor current reaches the level of the inverter current, the resonant capacitor is being charged, since the inductor current continues to rise. Since the capacitor charging current is low and controlled by the inductor in this case, the voltage is increasing with a moderate derivative. The capacitor voltage only reaches about twice the DC link voltage, which is due to the fact the voltage rise interval starts at zero voltage with zero charging current.

If the resonant frequency of the DC link is much higher than the switching frequency the oscillation might be damped which means that after some resonance cycles, zero voltage will not be reached. This damping is due to losses of the passive components. One way to cope with this problem is to maintain the zero voltage interval somewhat longer by short-circuiting the resonant capacitor with the converter switches. This forces storage of more energy in the resonant inductor, which in turn results in higher capacitor peak voltage.

However, the zero voltage switching resonant DC link inverter has some fundamental problems such as zero crossing failure, inverter phase current ripple due to integral cycle switching and capacitor voltage overshoot. To overcome all these problems simultaneously, a clamp circuit is being used. A clamp circuit assures that the maximum capacitor voltage is limited to a certain level by an external circuit. Two methods of clamping are proposed in literature, active and passive clamping. Active clamping is being incorporated. Active clamping circuit utilizes one IGBT and two thyristors to provide clamp action.

Here, the resonant DC link voltage is limited to a level determined by the voltage across the capacitor. When the voltage across the capacitor equals the supply voltage, the IGBT starts to conduct. Thus, the resonant link voltage is clamped to this value. During the clamping action, the capacitor is charged, implying that the clamping voltage will increase if no precautions are made. To solve this problem the controllable part of IGBT has to be operated during the off clamping intervals of the resonant cycle. If this is done appropriately the clamping voltage can be controlled to be almost constant.

2.6. RESONANT DC LINK INVERTER WITH ACTIVE VOLTAGE CLAMPING

The resonant circuit consists of three auxiliary switches, one resonant inductor and one resonant capacitor. The auxiliary switches are controlled at certain instant to obtain the resonant between inductor and capacitor. Thus the DC link voltage and current reaches temporarily and the main switches of the inverter get ZVS and ZCS condition. The equivalent circuit is shown in fig. 2.13.

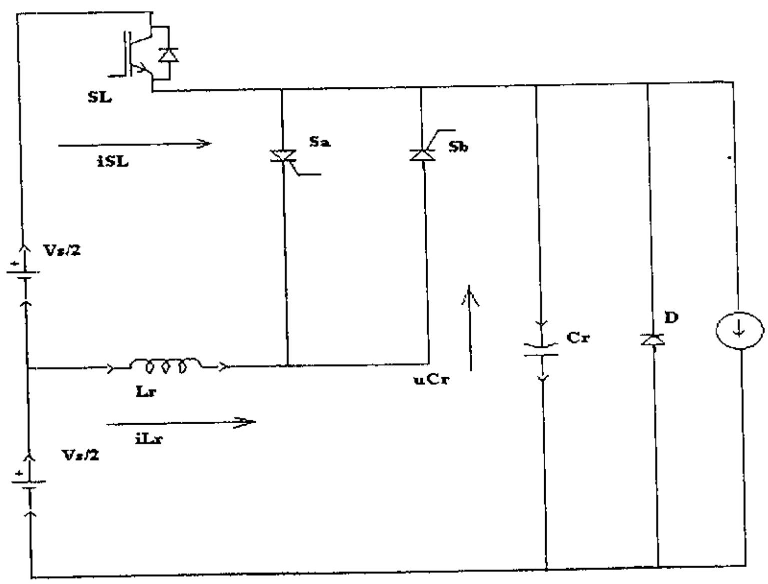


Fig. 2.13. Equivalent Circuit

Since the resonant procedure is very short, the load current is assumed to be constant. The corresponding waveforms of gate signal of auxiliary switches, resonant capacitor voltage (u_{cr}), inductor current (i_{lr}) and current of switch s_L (i_{SL}) is illustrated in fig. 2.14. The dc link voltage reduce to zero and then rise to dc supply voltage again is called one zero voltage transition process. The operation of the circuit can be divided into six modes, as shown in fig. 2.15.

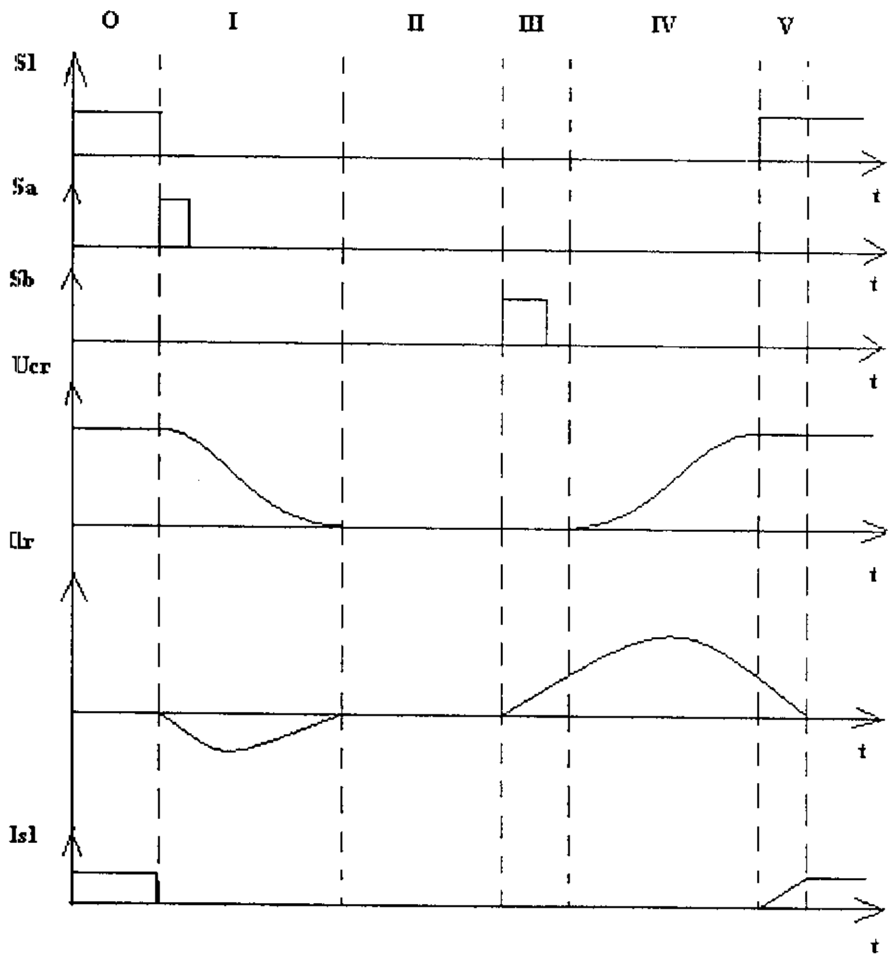
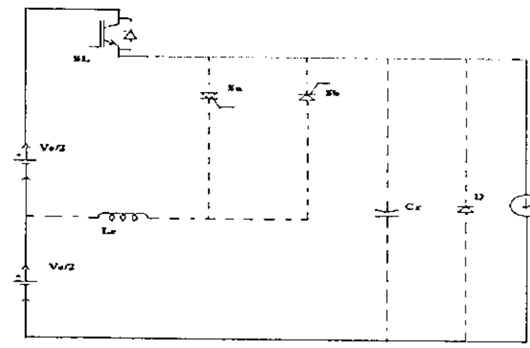


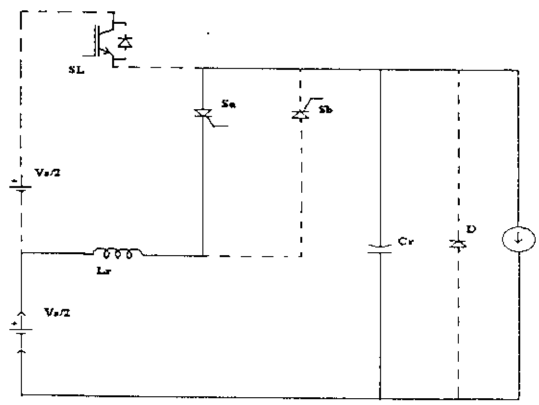
Fig. 2.14. Waveforms of Equivalent circuit

MODE 0, ENERGY STORAGE INTERVAL:

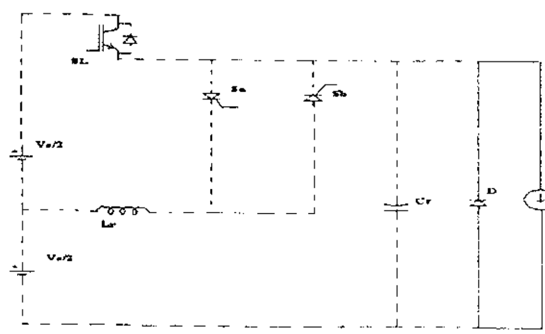
Its operation is the same as conventional inverter. Current flows from dc power supply through S_L to the load. The voltage across the capacitor Cr is u_{cr} and is equal to the supply voltage, Vs. The auxiliary switches S_a and S_b are in OFF state. An energy storage interval is needed in order to store resonant energy in the inductor Lr to ensure that the resonant link voltage do decrease down to zero, during the ramp down interval. The energy storage interval starts with turn OFF of S_b.



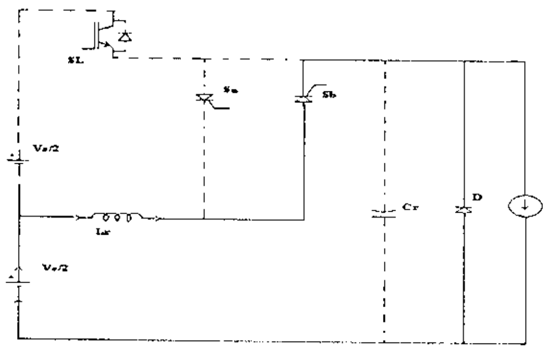
MODE 0



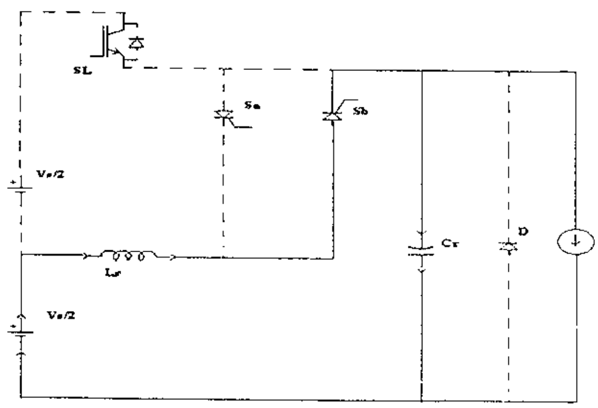
MODE 1



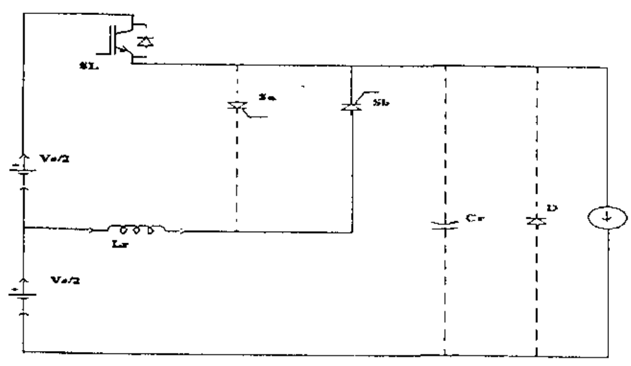
MODE 2



MODE 3



MODE 4



MODE 5

Fig. 2.15. Operation modes of the Equivalent circuit

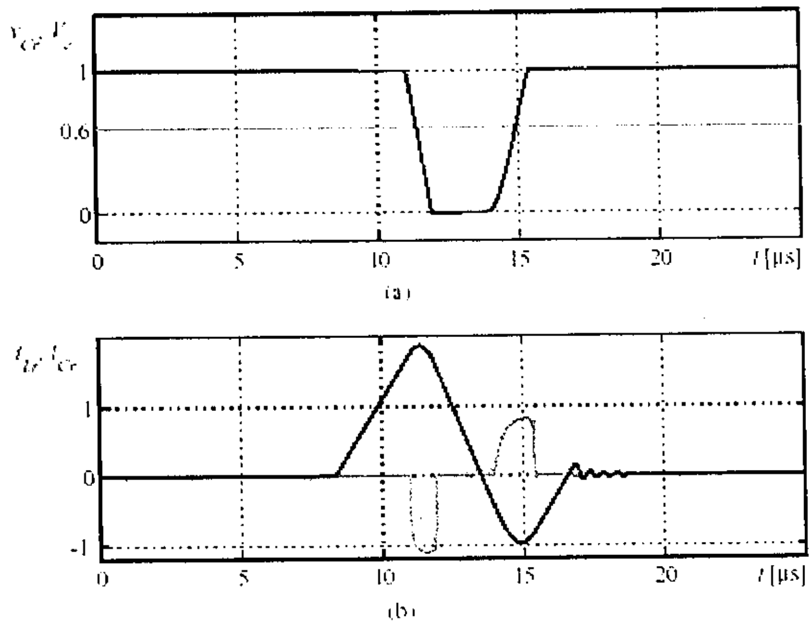


Fig. 17. (a) Resonant link voltage u_{cr} (black) and energy storage capacitor voltage (grey), and (b) Resonant inductor current i_{Lr} (black) and Resonant capacitor current i_{Cr} (grey)

MODE 1, RESONANT LINK VOLTAGE RAMP DOWN INTERVAL:

The thyristor, S_a is fired and IGBT S_L is turned OFF at the same time. Capacitor Cr resonates with inductor Lr. The voltage across the capacitor Cr is decreased. i_{Lr} is zero at the same time. Then the thyristor, S_a is self turned OFF. The resonant link voltage ramp down interval is initiated by turning off the IGBT S_L, forcing a discharge of the resonant link capacitor Cr. The system of differential equations valid for this mode is given below:

$$u_{Cr} - Lr\,(di_{Lr}/dt) = 0 \qquad (2.2)$$

$$i_{Cr} = Cr\,(du_{Cr}/dt) \qquad (2.3)$$

$$i_{Lr} + i_{Cr} + i_{o1} = 0 \qquad (2.4)$$

The characteristic angular frequency ${}_r$ is given by,

$${}_r = 1/(Lr.Cr)^{1/2} \qquad (2.5)$$

MODE 2, ZERO VOLTAGE INTERVAL:

None of the auxiliary switches is fired and the voltage of dc link, u_{Cr} is zero. The main switches of the inverter can be either turned ON or turned OFF under ZVS condition during the interval. Load current flows through the freewheeling diode, D. During the zero voltage interval the resonant link voltage is clamped to zero, first by the inverter freewheeling diodes and then by inverter switches. This implies,

$$u_{Cr}(t) = 0 \qquad (2.6)$$

Which means that the differential equation for this mode is given by,

$$Lr\,(di_{Lr}/dt) = 0 \qquad (2.7)$$

MODE 3, RESONANT LINK VOLTAGE RAMP UP INTERVAL:

As the main switches have turned ON or turned OFF, thyristor S_b is fired and i_{Lr} starts to build up linearly in the auxiliary branch. The current in the freewheeling diode D begins to fall linearly. The load current is slowly diverted from the freewheeling diodes to the resonant branch. But u_{Cr} is still equal to zero. As i_{Lr} equals the load current Io and the current through the diode becomes zero. Thus the freewheeling diode turns off under zero current condition. The system of differential equations valid for the resonant link voltage ramp up interval is given below.

$$u_{Cr} - Lr\,(di_{Lr}/dt) = 0 \qquad (2.8)$$

$$i_{Cr} = Cr\,(du_{Cr}/dt) \qquad (2.9)$$

$$i_{Lr} + i_{Cr} + i_{o2} = 0 \qquad (2.10)$$

MODE 4 and MODE 5, ENERGY RECOVERY INTERVALS:

i_{Lr} is increased continuously from Io and u_{Cr} is increased from zero when the freewheeling diode D is turned OFF. When u_{Cr} = Vs, IGBT S_L is fired and $i_{Lr} = i_o$ again. During the resonant energy recovery interval, the excess energy stored in the resonant inductor Lr, is transferred back to the supply via the resonant link series diode. Furthermore, this also implies that the resonant link voltage is clamped to the DC link voltage level. During the energy recovery interval the resonant link series IGBT S_L is turned ON, to be able to support the current fed to the inverter during the OFF resonance period. The differential equation valid for this mode is thus written

$$Vs - Lr\,(di_{Lr}/dt) = 0 \qquad (2.11)$$

The excess resonant energy is fully restored when

$$i_{Lr}\,(t_5) = 0 \qquad (2.12)$$

For this circuit, either the series IGBT or diode of the resonant link, i.e., S_L or Ds, is conducting the current drawn by the inverter during the OFF resonance interval. This also means that the resonant link voltage u_{Cr} is clamped to the DC link voltage level Vs. Consequently no oscillations are observed during the OFF resonance interval, i.e., in between the resonant cycles. When the dc link voltage is equal to the supply voltage, auxiliary switch S_L is turned ON. i_{Lr} is decreased linear from Io to zero at t_5 and the thyristor S_b is self turned OFF. Then go back to mode 0 again. The operation principle of the other procedure is the same as conventional inverter. Hence the oscillatory output voltage of the resonant circuit is given to three phase inverter circuit. At the zero voltage and zero current conditions the IGBTs are triggered sequentially.

As shown in fig. 2.1, in three phase inverter circuit each IGBT conducts for 120° of a cycle. The IGBT pair in each arm is 1,4; 3,6; 5,2. Here 1 conducts for 120° and for the next 60°, neither 1 nor 4 conducts. Now 4 is turned on at 180° and it further conducts for 120° i.e. from 180° to 300°. This means that for 60° interval from 120° to 180°, series connected IGBTs do not conduct. At 300°, 4 is turned OFF, then 60° interval elapses before 1 is turned ON again at 360°. 3 is turned ON at 120°. Now 3 conducts for 120°, then 60° interval elapses during which neither 3 or 6 conducts. The process continues. The sequence of firing the six IGBTs is 6,1; 1,2; 2,3; 3,4; 4,5; 5,6; 6,1. During each step, only two IGBTs conduct for this inverter – one from the upper group and one from the lower group. Hence here the motor is energized by having two switches closed in sequence at one time. In this inverter, there is a 60° interval between the turning OFF of 1 and turning on of 4. During this 60° interval, 1 can be commutated safely. In general, this angular interval of 60° exists between the turning OFF of one device and turning ON of the complementary device in the same leg. This 60° period provides sufficient time for the outgoing IGBT to regain forward blocking capability.

Each arm of the bridge normally contains an inverse parallel-connected diode. These diodes, which are called the return current or feedback diodes, must be provided to allow for an alternate path for the inductive motor current that continues to flow when the main power device is turned OFF. The line-to-line voltages are given as Va, Vb, and Vc. The embedded controller used for controlling the switching of IGBTs is PIC microcontroller. The IGBTs of the inverter are switched in sequence under ZVS, ZCS and 120° switch mode conditions using embedded controller. The output line-to-line voltage of the inverter is fed to the three-phase induction motor.

2.7. ANALYSIS AND DESIGN CONSIDERATIONS

For the resonant dc link inverter with active voltage clamping investigated here, only two parameter values are possible to use as design parameters, Lr and Cr. This means that the design constraints on the duration of the zero voltage interval and the maximum resonant link voltage derivative together determines the resonant link passive components. If Vs is applied to the system, for loss less Lr and Cr, Vo will be given by,

$$Vo\ (t) = Vs\ (1\text{-}\cos\ \ t) \qquad (2.13)$$

Where is the resonant frequency. At t = 2 ∏, Vo will return to zero volts, thus setting up desired loss less switching condition. To accomplish the objective of ZVS, it is necessary to monitor ($i_{Lr} - I_o$) to ascertain that sufficient excess energy is stored in L to ensure that Vo returns to zero. Active control of the current ($i_{Lr} - I_o$) ensures that each resonant cycle starts with the same initial conditions.

$$= (L.C)^{-1/2} \qquad (2.14)$$

$$f = 1/\,(2\Pi\,(L.C)^{-1/2}) \qquad (2.15)$$

$$Vc\ (t) = Vs + e^{-\alpha t}\,[-Vs.\cos\ \ t + \ \ L.\ Im.\sin\ \ t] \qquad (2.16)$$

$$\text{Where, } Im = i_{L\phi} - I_o \qquad (2.17)$$

Here the value of capacitor is taken to be $10e^{-6}$F and the switching frequency is 2 KHz. Hence by using the above mentioned formulae the value of inductor is calculated to be $5e^{-4}$H. The input voltage is kept as Vs/2 = 250V. Hence, Vs = 500V. Nominal output line to line voltage is 460 Vrms. Nominal output frequency is 50 Hz. The load used is three phase induction motor. The rotor type is squirrel cage and the machine is asynchronous type. The simulated results for line-to-line voltages, motor speed and motor torque are given in simulation results. The simulation is done in MATLAB using sim power system toolbox.

2.8. COMPONENT CHARACTERISTICS

IGBTs

The IGBT was introduced to be a compromise between the bipolar junction transistor (BJT) and the metal oxide semiconductor field effect transistor (MOSFET). However, the IGBT has become more than just a compromise, due to its high ruggedness, moderate voltage drop and fairly high switching speed. Actually, in many modern designs it is the only reasonable device choice. The main reasons for its popularity is the high blocking voltage, up to 6KV, its moderate driving requirements and its limited need for protective devices, i.e. snubbers.

BASIC DOPING STRUCTURE

The IGBT is a three terminal semiconductor device. The terminal named emitter is common to both input and output. The device is controlled by applying a voltage between the gate and emitter terminals. The output current flows between the collector and emitter terminals. The gate emitter region is split into thousands of cells. In fig.18. the vertical cross section of a NPT – IGBT and also of a PT – IGBT are shown. The only structural difference between these two, is that the PT device has an additional doping layer, termed buffer. The n^+ buffer layer between the p^+ drain contact and the n^- drift layer is not essential for the operation of the IGBT, and some IGBTs are made without it. They are termed as non – punch – through, NPT – IGBTs, whereas those with this buffer layer are termed punch – through, PT – IGBTs. The reason for dividing the gate – emitter structure into cells, is to keep the channel resistance low by increasing its cross – sectional area and decreasing its length. Further on, the emitter metallisation extends over the body region, which is done to short circuit the body – emitter junction. This is used to reduce the risk of entering latch up.

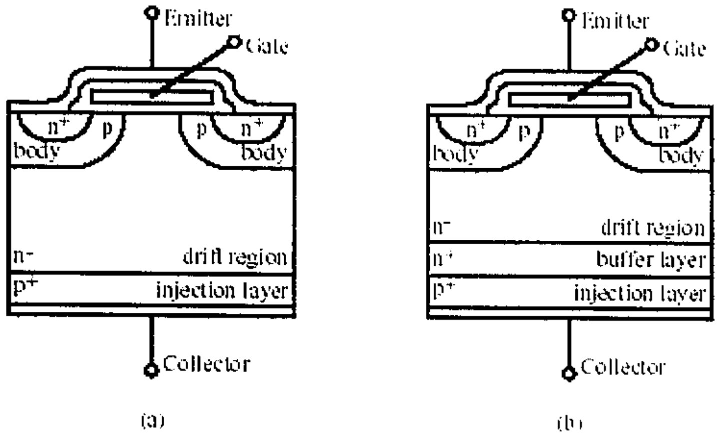


Fig. 2.17. Principal doping structure for (a) NPT – IGBT (b) PT – IGBT

STEADY STATE OPERATION

From fig. 2.17 it is seen that the doping structure of an IGBT looks similar to the one of a MOSFET. For the NPT device the only difference is the presence of a heavily doped injection layer at the IGBT collector metallisation. The reason for having this layer is that holes should be injected into the drift region to obtain conductivity modulation when the device operates in the conduction state. The lack of conductivity modulation is the main drawback of the MOSFET, being a majority carrier device. In the on state, similar to the MOSFET, a channel is created in the body region underneath the gate oxide, connecting the n – doped emitter and drift regions. The channel supports an electron current, flowing from the emitter into the drift region. The negative charge of the electrons attracts holes from the injection layer, which in turn causes conductivity modulation of the drift region. When the IGBT operates in the forward blocking state, the drift region supports the voltage. Similar to the power diode case, a depletion region is formed in the drift region. For a NPT device, this is also true for the reverse blocking state, i.e. when the IGBT is blocking a collector – emitter voltage of reverse polarity. However, the PT – IGBT can not block a collector – emitter voltage of negative polarity, since the injection – buffer junction should support the voltage in this case. Both these regions are highly, doped, resulting in a high electric field strength even at low blocking voltages. Consequently, avalanche breakdown will occur for low reverse blocking voltage. This is the reason why the PT – IGBT is often termed asymmetric. In fig. 2.18. the current – voltage characteristics of a typical IGBT is shown. The output characteristic of an IGBT shows the collector current, i_c, as a function of the collector – emitter voltage V_{CE}, for different gate – emitter voltages V_{GE} . The transfer characteristic shows the collector current as a function of the gate – emitter voltage, when the IGBT is in the active region. The transfer characteristics is thus mainly interesting for the switching transients, since otherwise the device should operate in the on – state or off – state regions.

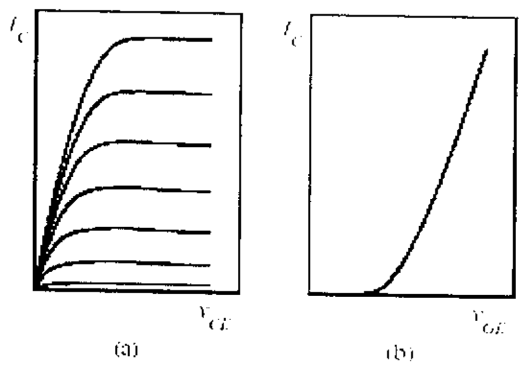


Fig. 2.18. (a) Output characteristic for low collector – emitter voltages
(b) Transfer characteristic

Since this is a voltage source inverter, the load is a current source, i.e. inductive. Fig. 20. shows typical collector current and collector – emitter voltage for a IGBT, when used in step down converter. The collector current and collector – emitter voltage is expressed in p.u., where the normalization values are selected as the rated maximum continuous collector current, I_c, and maximum collector – emitter voltage that can be sustained across the device, V_{CE}.

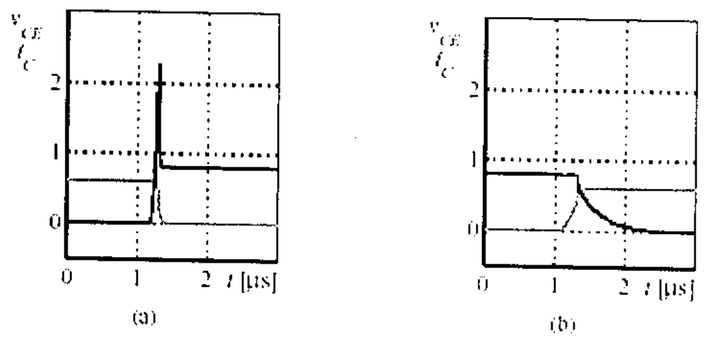


Fig. 2.19. Time – signals showing normalized IGBT current (black) and voltage (grey) at (a) turn – ON and (b) turn – OFF of the IGBT in the step down converter

Fig.2.19 shows typical switching waveforms for an IGBT operating at inductively clamped load. At **turn – ON** of the IGBT, the gate – emitter voltage V_{GE} must first reach its threshold level, $V_{GE\ (th)}$, before the collector current starts to increase. The time needed to do this is termed the turn – on delay time $\mathbf{t_{d\ (on)}}$. The gate – emitter threshold voltage is seen in the transfer characteristic of fig. 2.18 as a sharp bend where the collector current becomes non – zero. Since the IGBT has a capacitive input, the gate resistor determines the delay time. Also note that the internal capacitance is varying due to depletion layer thickness, i.e. collector – emitter voltage. The gate – collector capacitance is the most affected. After the turn on delay time, the gate – emitter voltage continues to increase and the collector current starts to increase. The collector current time derivative is determined by the transfer characteristics, shown in fig. 2.18. which implies that it is determined by the size of the gate resistor. The duration of this current rise interval is termed current rise time $\mathbf{t_{ri}}$. Following the current rise interval, the voltage fall interval commences. The duration of this interval is termed voltage fall time $\mathbf{t_{fv}}$. The voltage fall interval can be subdivided into two portions. The first part is similar to the voltage fall of a MOSFET. The second part has considerably lower fall rate mainly due to conductivity modulation lag.

IGBT **turn – OFF** also starts with a delay time, $t_{d\ (off)}$, due to the fact that the gate – emitter voltage has to decrease to the level determined by the transfer characteristic before the collector -- emitter voltage starts to increase. During the voltage rise time t_{rv} the collector – emitter voltage increases and the gate – emitter voltage is constant. When the collector – emitter voltage has reached the level of the dc link voltage the free wheeling diode becomes forward biased. Hence the IGBT collector current starts to decrease. The collector current fall rate is also determined by the gate – emitter voltage through the transfer characteristic, i.e. the fall rate is essentially determined by the gate resistor value. When the gate – emitter voltage has decreased to its threshold level $V_{GE\ (th)}$, the channel in the body region is removed, corresponding to that the MOSFET part of the IGBT is turned off. This part of the collector current fall is termed t_{fi}.

INDUCTIVE ELEMENTS

A resonant inverter has at least one inductive element being a part of the oscillatory circuit. Inductive elements consist of one or several copper wire windings which in most cases are wound up on an iron core. Magnetic components for power electronic applications, such as inductors and transformers, are often designed only for the intended application, due to the fact that it is impossible to maintain a storage of the wide variety of components needed. This means that for most power electronic applications, inductor design is a natural part of the development, since almost every power electronic circuit contains this kind of components. The frequency spectra of interest for power electronics range from 50 Hz to several MHz. There are mainly three types of core materials used to cover this frequency spectra. For the low frequency region, (50 Hz – 10KHz) alloys of iron are used. For the mid frequency region, (1 KHz – 100 KHz) cores made iron powder are used. For the upper frequency region, (30 KHz – 10 MHz) soft ferrite cores are used.

CAPACITORS

Two types of capacitors used in power electronic circuits are non – polarized metallised film polypropylene capacitor and the polarized wet aluminium electrolytic capacitor. Non polarized capacitors are used in output filters and for applications with high capacitor voltage time derivative, like commutation circuits. Polarized capacitors are used when a high capacitance is needed for dc link capacitors. Metallised film polypropylene capacitors have a thin plastic film to support the metal layer of the electrodes. The plastic used for the film can be polyester. If the plastic film has electrodes on both sides it is referred to as double metallised film. The dielectric consists of polypropylene film. To avoid air pockets resulting in a locally high electric field strength, the polypropylene film should be somewhat porous to be able to absorb oil. Wet aluminium electrolytic capacitors contains of fluid, the electrolyte, between the aluminium electrodes. The electrolyte is absorbed by paper in between the aluminium electrodes, in order to avoid air pockets. Since the electrolyte is conductive, the aluminium electrodes are electrically close together, only separated by the dielectric of the capacitor. The dielectric constitutes of a thin aluminium oxide layer on the positive electrode.

CHAPTER – 3

CONCLUSION

3.1. SIMULATION RESULTS

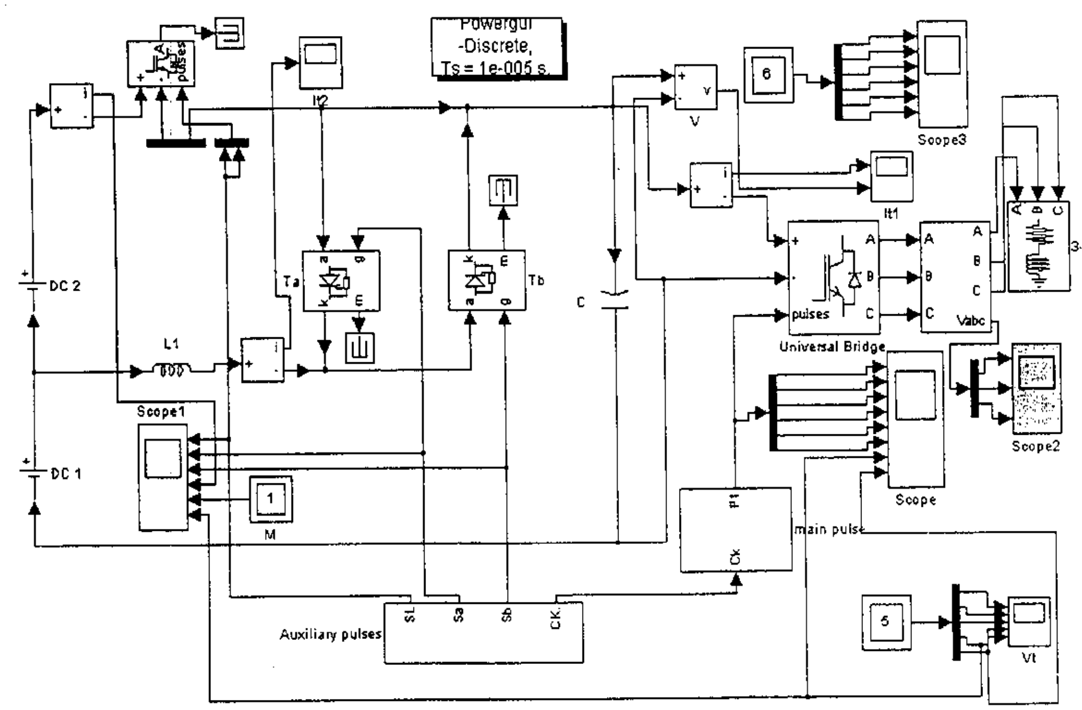


Fig. 3.1. Three phase sine wave inverter using ZVS along with active voltage clamping

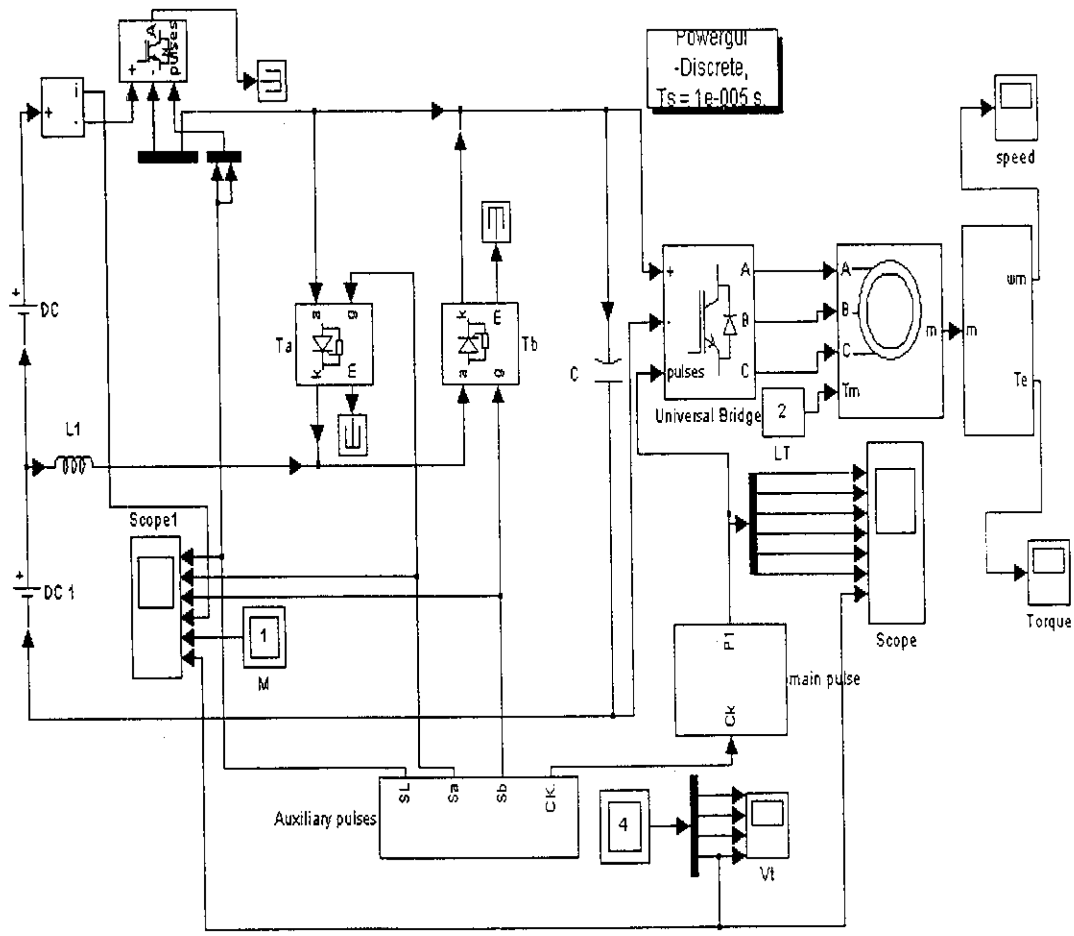


Fig.3.2. Three phase sine wave inverter with ZVS along with active voltage clamping with Induction Motor load

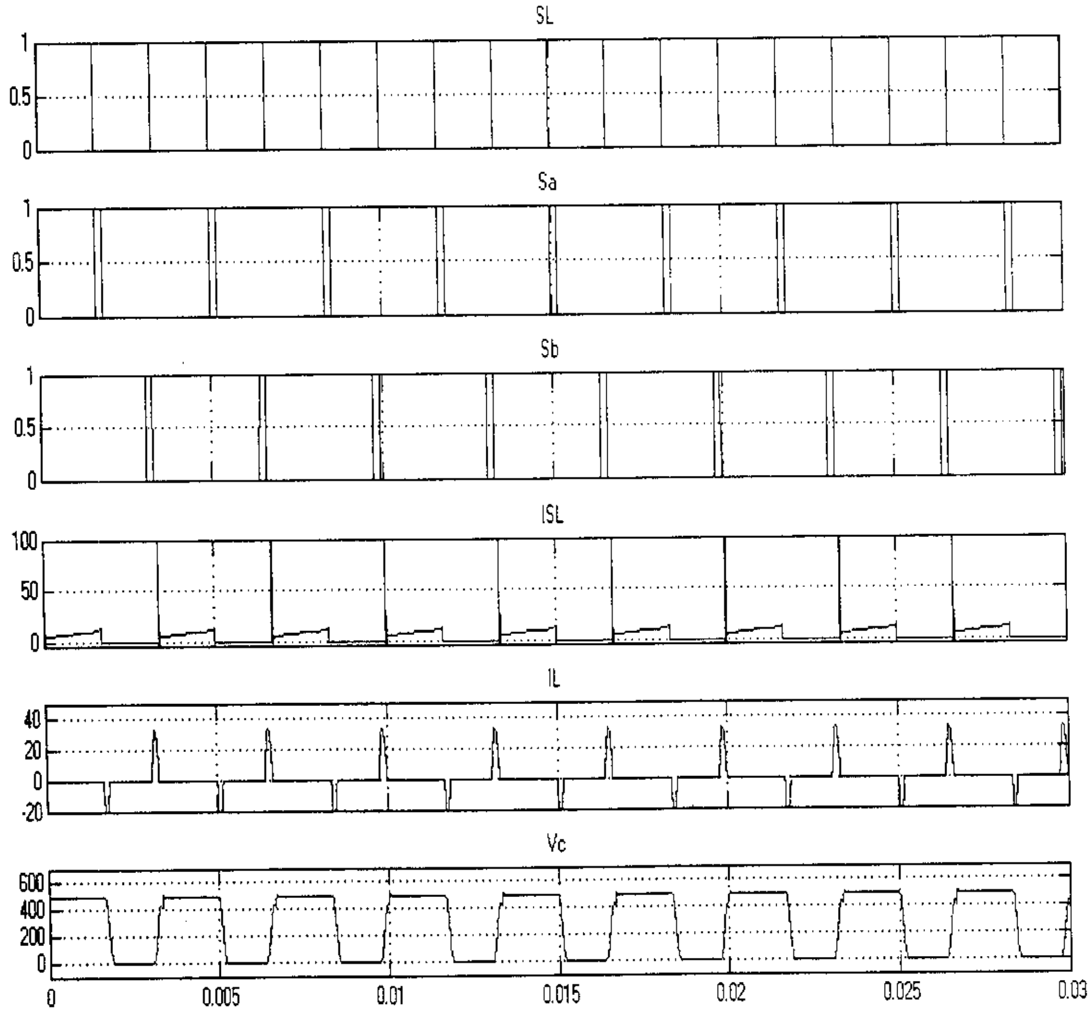


Fig. 3.3. Waveforms representing the operation of resonant circuit

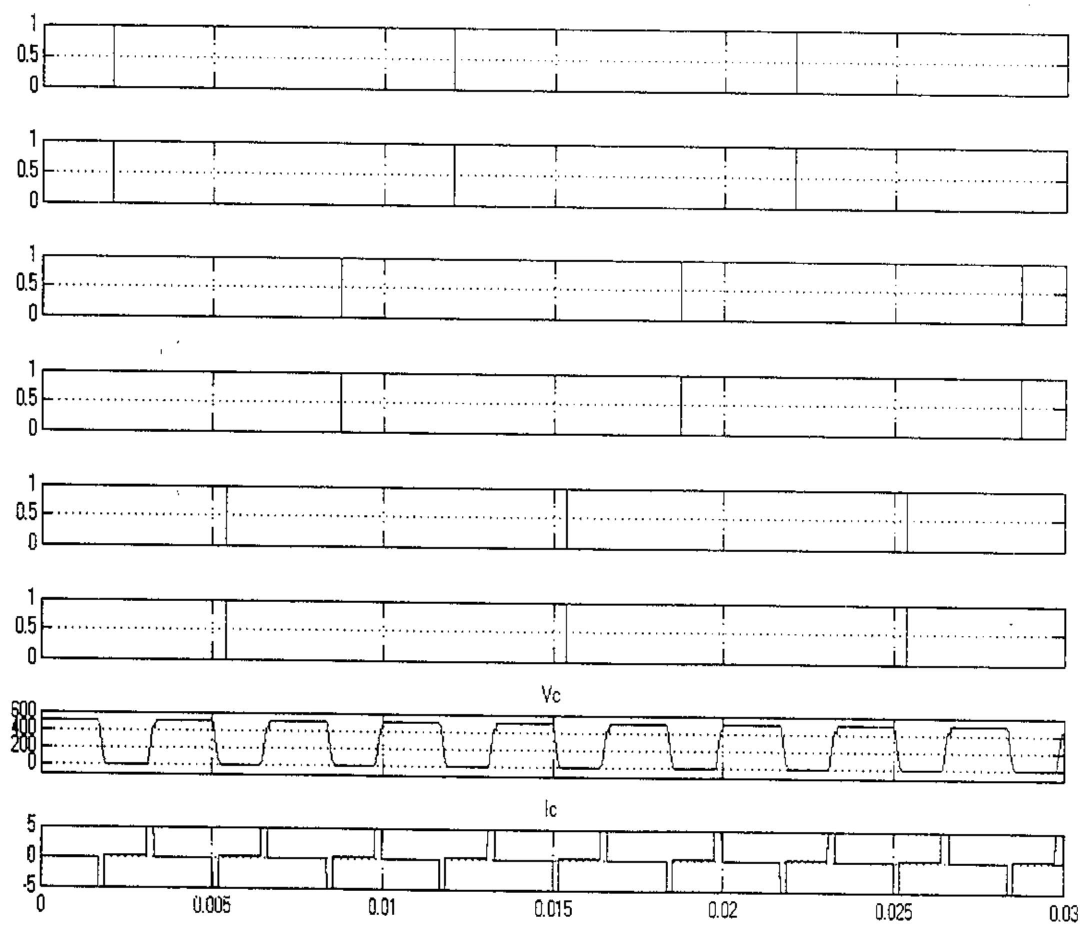


Fig. 3.4. Waveforms that indicate that all IGBTs are triggered under ZVS & ZCS condition

Fig. 3.5. Waveforms of device voltages using ZVS along with active voltage clamping

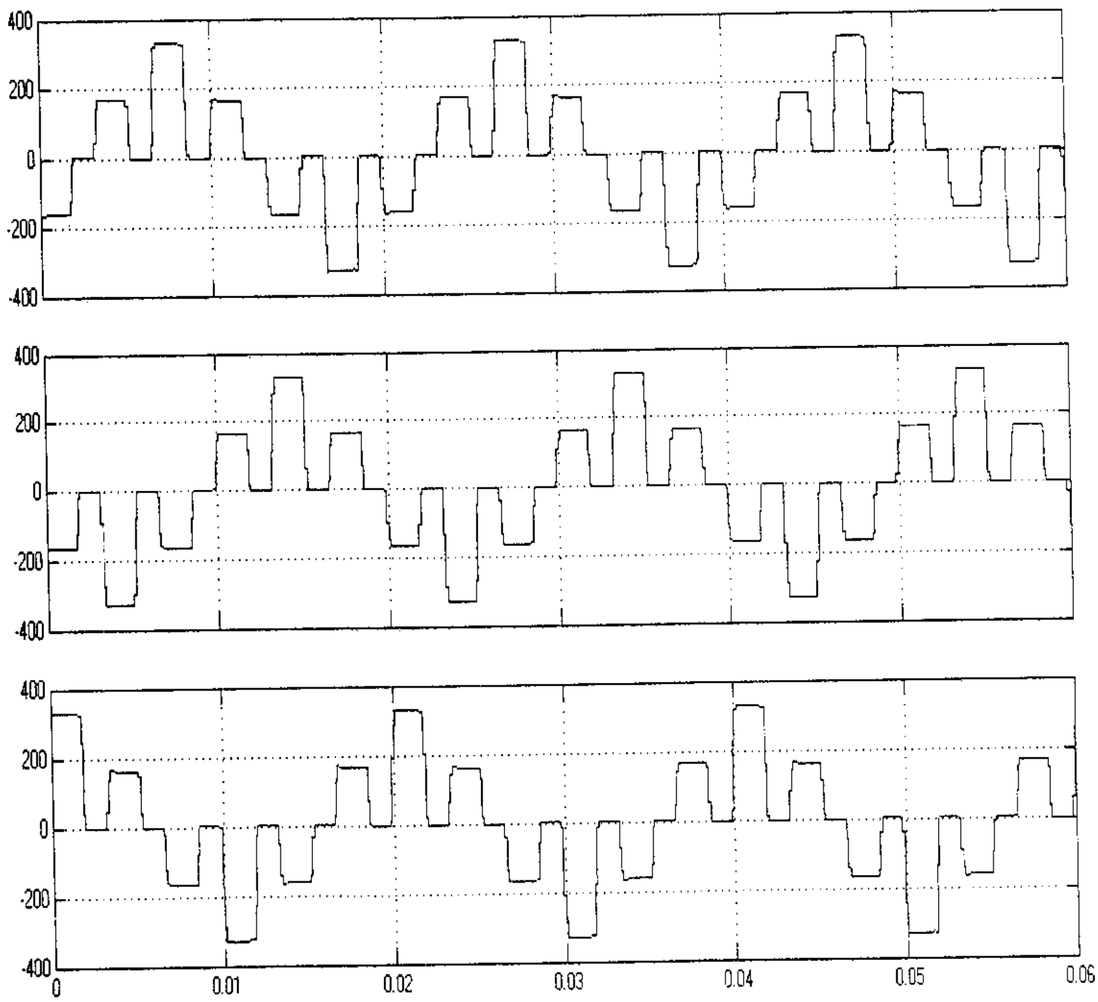


Fig. 3.6. Waveforms of output line-to-line voltages using ZVS along with active voltage clamping

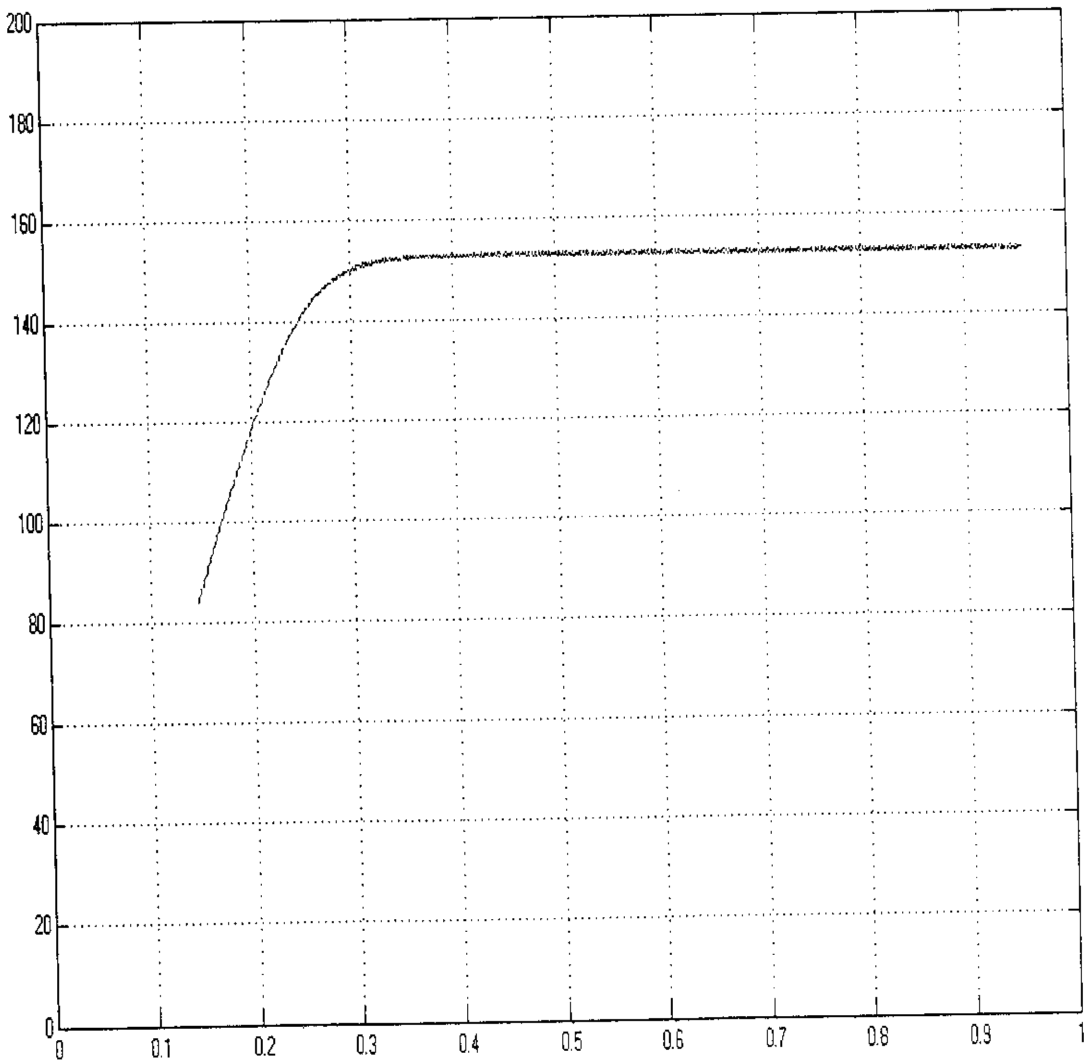


Fig. 3.7. Waveform representing the speed of induction motor

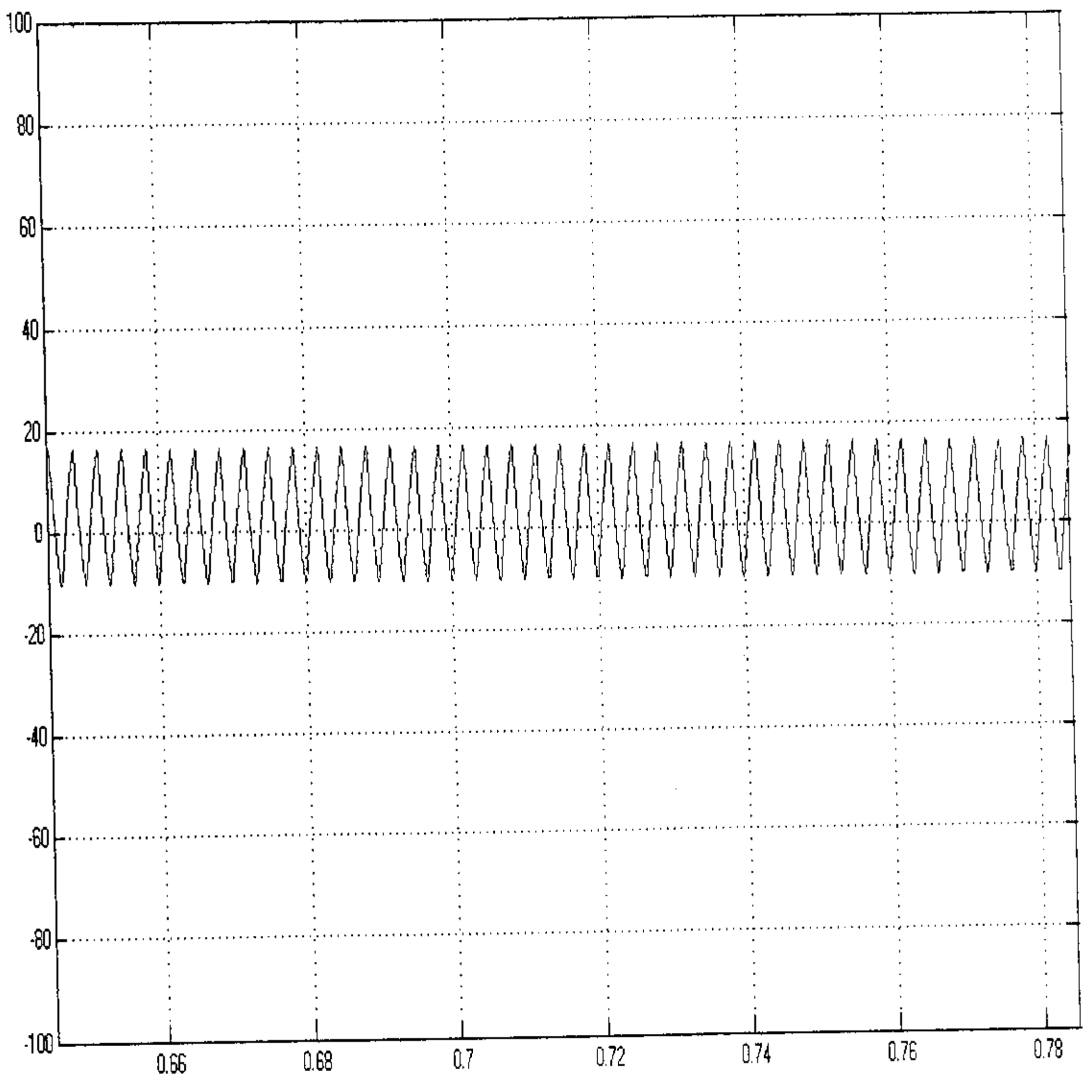


Fig. 3.8. Waveform representing the torque of induction motor

3.2. ADVANTAGES

The advantages of resonant DC link inverter are,

- Minimum number of power devices
- Elimination of switching losses
- Elimination of switching stresses
- Elimination of snubbers
- High switching frequency
- Low harmonics on AC line side
- Minimal cooling requirement
- High efficiency
- High reliability
- Low Electromagnetic interference (EMI)

3.3. APPLICATIONS

Switch mode DC to AC inverters are used in, **adjustable speed ac motor drives and uninterruptible ac power supplies** where the objective is to produce a sinusoidal AC output whose magnitude and frequency can both be controlled. The resonant DC link inverters are also used for **Electric Vehicle application.** The electric vehicles utilize hard switching inverters to drive their motors. This type of inverter suffers from high switching losses, high switching stresses and EMI problems. To solve these problems soft switching resonant DC link inverters have been proposed.

3.4. CONCLUSION

Advances in soft switching converters have set new benchmarks in performance and cost in power converter technology, and have shown promise in overcoming the limitations of conventional hard switching technology. Resonant dc link inverters have been realized at power ratings of 200 KVA in single modules. The use of zero voltage switching with IGBT power devices demonstrates of some aggressive benchmarks when compared with conventional technology. These include:

- 100% power device utilization
- Low EMI
- Enhanced robustness
- High power densities
- High switching frequencies
- High efficiencies

One of the main advantages of soft switching is the improved power device utilization due to the reduction in the turn – on and turn – off energy loss. As a result, the power device can be operated at higher switching frequencies while being subjected to the losses as in hard switching applications. Alternatively, the power device utilization can be improved by reducing the switching frequency and increasing the forward current while maintaining the total losses to be the same. One of the important benefits that accrue from the use of zero voltage switching inverter circuits is the low dv/dt that a capacitive snubber yields. The other aspect of soft switching converters that has received much attention is the possibility of realizing low conducted EMI levels, as compared with their hard switching counterparts. This topology exhibits unique operating characteristics which enhance its usefulness in an industrial environment.

3.5. APPENDICES

MICROCONTROLLER – PROGRAM

```
#include<pic.h>
static bit SL  @((unsigned)&PORTB*8+7);
static bit SA  @((unsigned)&PORTB*8+6);
static bit CLK @((unsigned)&PORTB*8+5);
static bit SB  @((unsigned)&PORTB*8+4);
static bit PG1 @((unsigned)&PORTB*8+0);
static bit PG2 @((unsigned)&PORTB*8+1);
static bit PG3 @((unsigned)&PORTB*8+2);
static bit OP1 @((unsigned)&PORTE*8+0);
static bit OP2 @((unsigned)&PORTE*8+1);
static bit OP3 @((unsigned)&PORTE*8+2);
static bit OP4 @((unsigned)&PORTA*8+1);
static bit OP5 @((unsigned)&PORTA*8+2);
static bit OP6 @((unsigned)&PORTA*8+3);
bit sld,k,j,l,m,v;
unsigned int a,b,c,d,x,y,n,ja,o;
void interrupt timer1(void)
{
 if(TMR1IF==1)
 {
  n++;
  if(n==6)
  {
   n=0;
   a++;x++;
   b++;y++;
   c++;o++;
   d++;ja++;
   if(a==16)
   {
    a=0;
    sld=SL=!SL;
    if(sld==0)
    {
```

```
j=l=1;
   SA=1;
   x=y=0;
  }
 }
 if(a==2) SA=0;
 if(j==1 && x==4)
 {
  x=0;
  j=0;
  CLK=1;
 }
 if(x==2) CLK=0;

 if(l==1 && y==14)
 {
  y=0;
  l=0;
  SB=1;
 }
 if(y==2)  SB=0;

 if(b==100)
 {
  b=0;
  PG1=!PG1;
  m=1;
  ja=0;
 }
 if(m==1 && ja==66)
 {
  m=0;
  PG2=PG1;
  v=1;
  o=0;
 }
 if(v==1 && o==66)
 {
  v=0;
  PG3=PG2;
 }
 }
 TMR1IF=0;
 TMR1L=0x98;
 TMR1H=0xff;
}
```

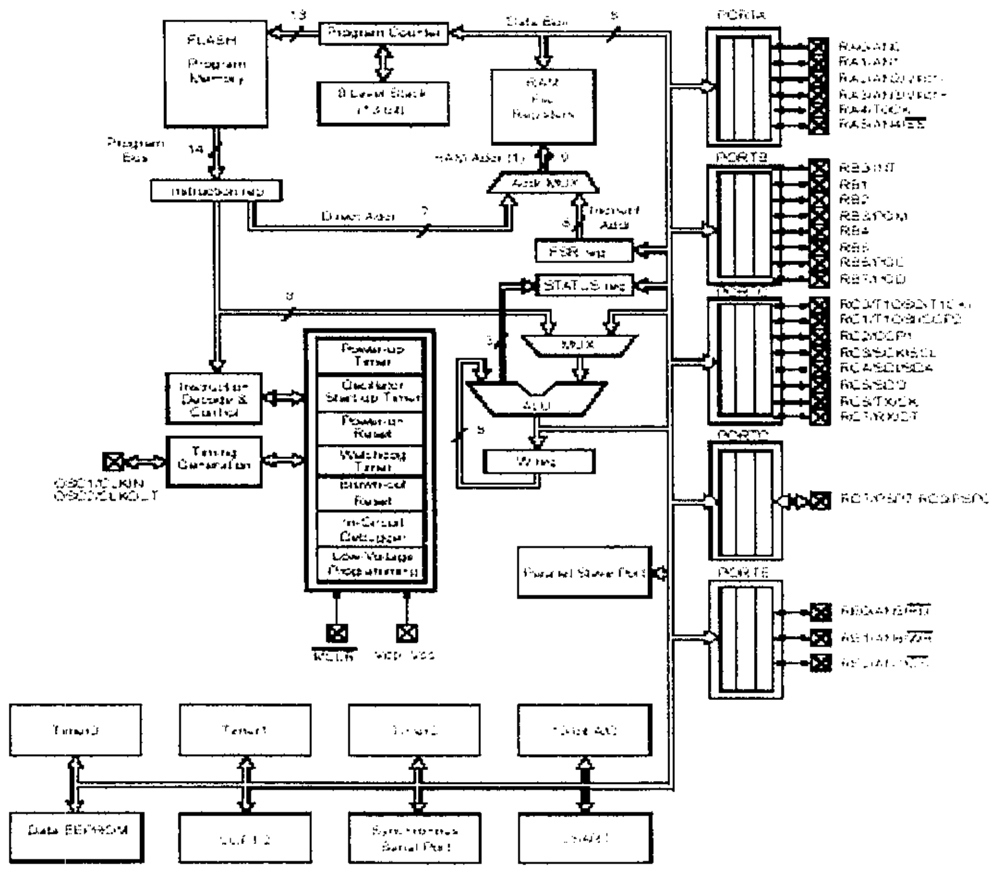
```
}
main()
{
 ADCON1=0x06;
 TRISE=0x00;
 TRISA=0x00;
 PORTB=0x00;
 TRISB=0x00;
 GIE=1;
 PEIE=1;
 TMR1IE=1;
 TMR1L=0x98;
 TMR1H=0xff;
 TMR1ON=1;
 SL=1;
 a=b=c=d=0;
 x=y=o=ja=0;
 while(1)
 {
  if(PG1==1 && CLK==1)
  {
   OP1=1;
   OP2=0;
  }
  else if(PG1==0 && CLK==1)
  {
   OP1=0;
   OP2=1;
  }
  if(PG2==1 && CLK==1)
  {
   OP3=1;
   OP4=0;
  }
  else if(PG2==0 && CLK==1)
  {
   OP3=0;
   OP4=1;
  }

  if(PG3==1 && CLK==1)
  {
   OP6=1;
   OP5=0;
  }
  else if(PG3==0 && CLK==1)
```

```
 {
 OP6=0;
 OP5=1;
 }
 }
}
```

PIC16F87X

FIGURE 1-2: PIC16F874 AND PIC16F877 BLOCK DIAGRAM

Device	Program FLASH	Data Memory	Data EEPROM
PIC16F874	4K	192 Bytes	128 Bytes
PIC16F877	8K	368 Bytes	256 Bytes



Note 1: Higher order bits are from the STATUS register.

TABLE 1-2: PIC16F874 AND PIC16F877 PINOUT DESCRIPTION

Pin Name	DIP Pin#	PLCC Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	13	14	30	I	ST/CMOS(4)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	14	15	31	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR/VPP/THV	1	2	18	I/P	ST	Master clear (reset) input or programming voltage input or high voltage test mode control. This pin is an active low reset to the device.
						PORTA is a bi-directional I/O port.
RA0/AN0	2	3	19	I/O	TTL	RA0 can also be analog input0
RA1/AN1	3	4	20	I/O	TTL	RA1 can also be analog input1
RA2/AN2/VREF-	4	5	21	I/O	TTL	RA2 can also be analog input2 or negative analog reference voltage
RA3/AN3/VREF+	5	6	22	I/O	TTL	RA3 can also be analog input3 or positive analog reference voltage
RA4/T0CKI	6	7	23	I/O	ST	RA4 can also be the clock input to the Timer0 timer/counter. Output is open drain type.
RA5/SS/AN4	7	8	24	I/O	TTL	RA5 can also be analog input4 or the slave select for the synchronous serial port.
						PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	33	36	8	I/O	TTL/ST(1)	RB0 can also be the external interrupt pin.
RB1	34	37	9	I/O	TTL	
RB2	35	38	10	I/O	TTL	
RB3/PGM	36	39	11	I/O	TTL	RB3 can also be the low voltage programming input
RB4	37	41	14	I/O	TTL	Interrupt on change pin.
RB5	38	42	15	I/O	TTL	Interrupt on change pin.
RB6/PGC	39	43	16	I/O	TTL/ST(2)	Interrupt on change pin or In-Circuit Debugger pin. Serial programming clock.
RB7/PGD	40	44	17	I/O	TTL/ST(2)	Interrupt on change pin or In-Circuit Debugger pin. Serial programming data.
						PORTC is a bi-directional I/O port.
RC0/T1OSO/T1CKI	15	16	32	I/O	ST	RC0 can also be the Timer1 oscillator output or a Timer1 clock input.
RC1/T1OSI/CCP2	16	18	35	I/O	ST	RC1 can also be the Timer1 oscillator input or Capture2 input/Compare2 output/PWM2 output.
RC2/CCP1	17	19	36	I/O	ST	RC2 can also be the Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL	18	20	37	I/O	ST	RC3 can also be the synchronous serial clock input/output for both SPI and I2C modes.
RC4/SDI/SDA	23	25	42	I/O	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I2C mode).
RC5/SDO	24	26	43	I/O	ST	RC5 can also be the SPI Data Out (SPI mode).
RC6/TX/CK	25	27	44	I/O	ST	RC6 can also be the USART Asynchronous Transmit or Synchronous Clock.
RC7/RX/DT	26	29	1	I/O	ST	RC7 can also be the USART Asynchronous Receive or Synchronous Data.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.
2: This buffer is a Schmitt Trigger input when used in serial programming mode.
3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).
4: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

PIN DIAGRAM

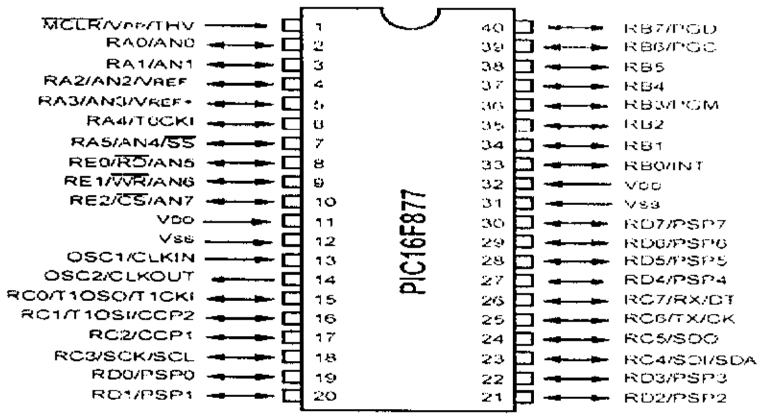


TABLE 1-2: PIC16F874 AND PIC16F877 PINOUT DESCRIPTION (CONTINUED)

Pin Name	DIP Pin#	PLCC Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
						PORTD is a bi-directional I/O port or parallel slave port when interfacing to a microprocessor bus.
RD0/PSP0	19	21	38	I/O	ST/TTL(3)	
RD1/PSP1	20	22	39	I/O	ST/TTL(3)	
RD2/PSP2	21	23	40	I/O	ST/TTL(3)	
RD3/PSP3	22	24	41	I/O	ST/TTL(3)	
RD4/PSP4	27	30	2	I/O	ST/TTL(3)	
RD5/PSP5	28	31	3	I/O	ST/TTL(3)	
RD6/PSP6	29	32	4	I/O	ST/TTL(3)	
RD7/PSP7	30	33	5	I/O	ST/TTL(3)	
						PORTE is a bi-directional I/O port.
RE0/RD/AN5	8	9	25	I/O	ST/TTL(3)	RE0 can also be read control for the parallel slave port, or analog input5.
RE1/WR/AN6	9	10	26	I/O	ST/TTL(3)	RE1 can also be write control for the parallel slave port, or analog input6.
RE2/CS/AN7	10	11	27	I/O	ST/TTL(3)	RE2 can also be select control for the parallel slave port, or analog input7.
VSS	12,31	13,34	6,29	P	—	Ground reference for logic and I/O pins.
VDD	11,32	12,35	7,28	P	—	Positive supply for logic and I/O pins.
NC	—	1,17,28, 40	12,13, 33,34		—	These pins are not internally connected. These pins should be left unconnected.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).
4: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

PIC16F87X

TABLE 13-2: PIC16CXXX INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode MSb			LSb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	lfff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1(2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1(2)	01	11bb	bfff	ffff		3
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	$\overline{TO}$,$\overline{PD}$	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into standby mode	1	00	0000	0110	0011	$\overline{TO}$,$\overline{PD}$	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3. If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

3.6. REFERENCES

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