AUTOMATIC SYNCHRONISATION

A PROJECT REPORT

Submitted by

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In partial fulfillment for the award of the degree

of

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in

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Under the guidance of

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The report of the project work submitted by the above students in partial fulfillment for the award of Bachelor of Engineering degree in Electrical & Electronics Engineering of Anna University were evaluated and confirmed to be report of the work done by the above students and then evaluated.

(EXTERNAL EXAMINER)

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SYNOPSIS

SYNOPSIS

This project is a modern equipment which is meant for synchronization of alternator and EB supply. It checks the conditions for synchronization using micro controller and electronic devices.

Nowadays in industries and power stations synchronization is done manually by using the existing methods. This requires analog meters and other devices. Also these existing methods are time consuming process and gives only approximate results.

In this project, we set a new trend in the process of synchronization. . micro controller plays a major role in checking the conditions that should be satisfied before synchronization process. Conditions to be satisfied by the two alternators are that they must have the same voltage, frequency and phase sequence. Circuits for checking these three conditions are designed, fabricated and checked. After checking, the outputs can be seen visually. This project gives the accurate result and helps to obtaining the exact point of synchronization.

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LIST OF SYMBOLS

SYMBOL	DESCRIPTION
V_i	DC input voltage
V_o	DC output voltage
V_{CC}	Supply voltage
INT	Interrupt
PSW	Program status word
SFR	Special function register
SBUF	Serial data buffer
ACC	Accumulator
SP	Stack pointer
ZCD	Zero crossing detector

CHAPTER -1

INTRODUCTION

INTRODUCTION

Synchronization of alternator

The operation of connecting one alternator in parallel with another alternator or with common bus bar is known as parallel operation or synchronization of alternators.

1.1 NEED FOR SYNCHRONIZATION

1.1.1 Reliability of supply

When two alternators are connected in parallel in case one of the alternator fails the other alternator keeps supplying the load so the continuity of supply to the load is not affected and the system is reliable.

1.1.2 Better utility of machines

In case maximum demand of the power station decreases, some machines may be put off making better use of other machines..

1.1.3 Easy maintenance and repairs

It is easy to attend repairs and maintenance work on anyone of the machine without affecting the supply to the load when the alternators are

1.1.4 Usage of older machines

Due to aging the capacity of the machine decreases. Because of that we cannot simply throw away them away. In order to meet the load we have to synchronize these older machines with new ones or bus bars.

1.1.5 Decrease in reserve capacity

By synchronizing to or more alternators the reserve capacity of the system is reduced and thereby capital cost is reduced.

1.1.6 Easy to meet new load

When there is an increase of load on the system it can be met by connecting alternators in parallel without any additional equipment.

Because of the above advantages we go for synchronizing process. For that purpose we need a device which synchronizes the alternators accurately.

1.2 CONDITIONS FOR SYNCHRONIZATION

For proper synchronization of alternators the following three conditions must be satisfied before they put into the synchronization process.

- The terminal voltage of the incoming alternator must be same as the Voltage of the other alternator or bus bar.
- Frequency of generated voltage of one alternator should be equal to frequency of other alternator or bus bar.
- Phase sequence of existing alternator and incoming alternator must be identical.

1.3 EXISTING METHODS

1.3.1 Dark lamp method

First the field excitation of the alternator is so adjusted such that the voltmeter reading V2 should be equal to v1. now the terminal voltages are same. Phase sequences are identical if the three lamps flicker in clockwise direction. If not the terminal voltages are changed properly.

Speed of the incoming alternator is so adjusted such that the flickering of lamps are slow. It is preferable the flickering is one dark period per second.. now the two frequencies are almost same. The synchronizing switch is closed. When the three are in dark period the alternator A2 is said to be synchronized with bus bar. Now the alternator is ready to share the common load. Since the synchronizing switch is closed, when the three lamps are in dark period this method is known as **Dark Lamp Method**

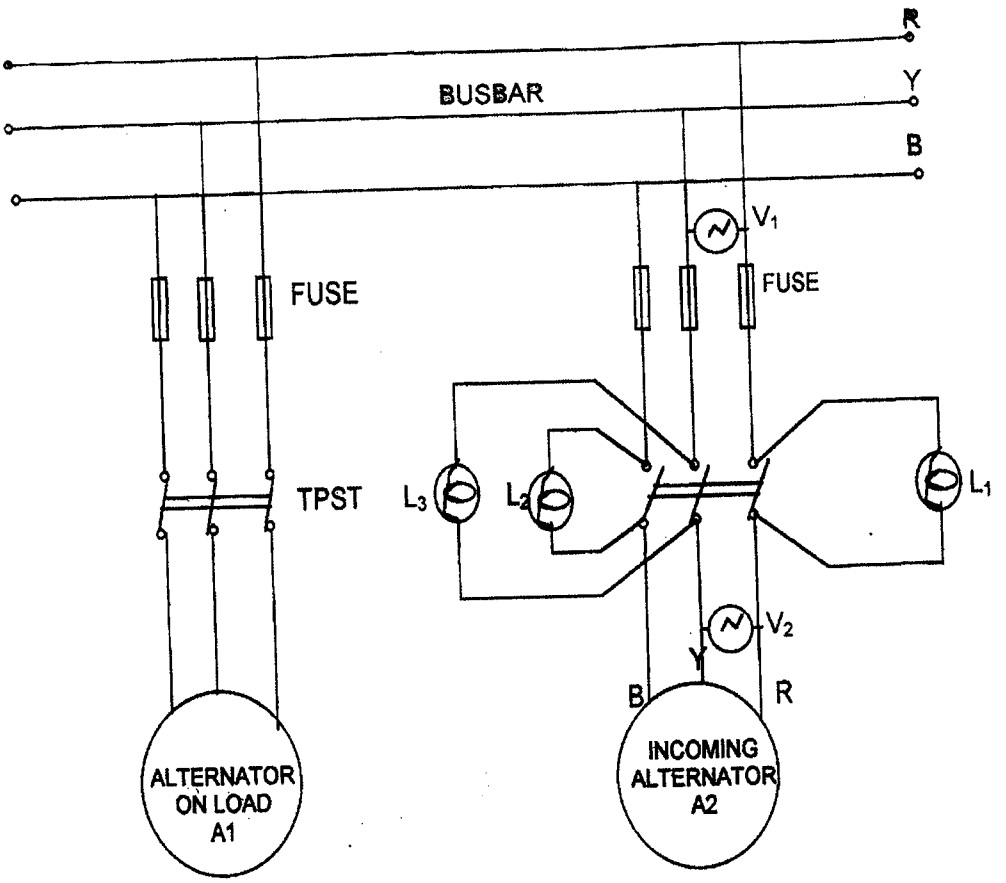


FIG. 1.1. DARK LAMP METHOD

1.3.2 Bright and dark lamp method

Circuit is connected as shown . first the field excitation of the alternators are so adjusted such that the voltmeter using reading V2 should be equal to V1. now the terminal voltages are same.

Phase sequence of the incoming alternator is identified by using sequence indicator. The speed of the incoming alternator is so adjusted such that the frequency must be same as that of the bus bar frequency. It is adjusted by using three lamps i.e. the lamp L1 is in dark period, the lamp L2 and L3 are in maximum brightness. The synchronizing switches are closed under this condition. Now the alternator "2" is said to be synchronized with bus bar.

Since the synchronizing switch is closed when the two lamps are in bright period and one lamp is in dark period. So this method is known as **'Bright And Dark Lamp Method'**

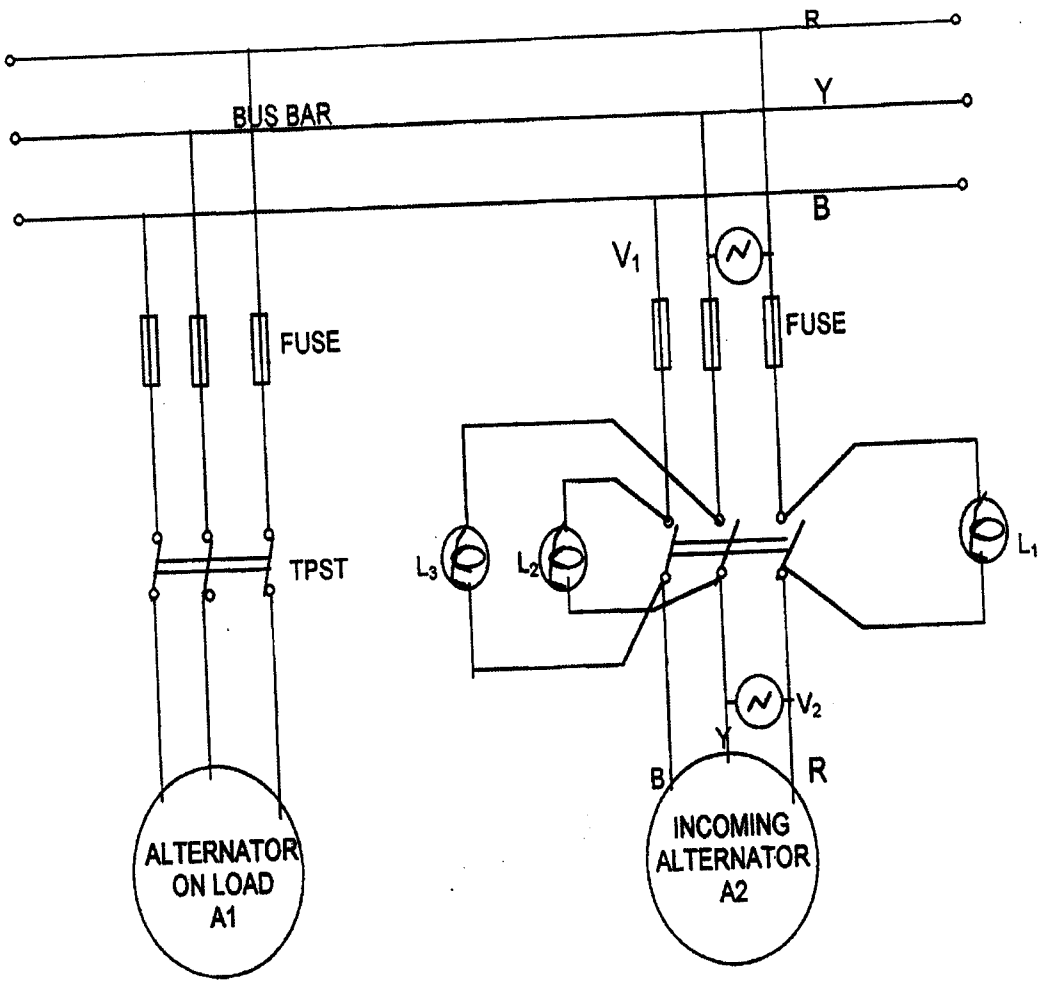


FIG. 1.2. DARK AND BRIGHT LAMP METHOD

1.3.3 Synchroscope method

In this method the given alternator is synchronized to the bus bar by synchroscope. In this method of synchronizing the connection diagram is as shown.. he terminal voltage of the incoming alternator is so adjusted such that the readings of voltmeter v2 is equal to v1.The phase sequence of the incoming alternator and bus bar is identified by using phase sequence indicator.

Condition two is verified by using synchroscope. It consists of a fixed coil stator and a rotating coil rotor. Stator is supplied from bus bar and the rotor is supplied from incoming alternator as shown in fig. If the frequencies of the bus bar and incoming alternator is not same then the rotor of the synchroscope will rotate. A pointer rotates in clockwise direction, then it means the speed of the incoming alternator is fast. If the pointer rotates in anti-clockwise direction then it means speed of the alternator is too slow. The speed of the incoming alternator is so adjusted such that the pointer will not rotate in either direction. The synchronizing switch is closed position. Now A2 is said to be synchronized with bus bar.

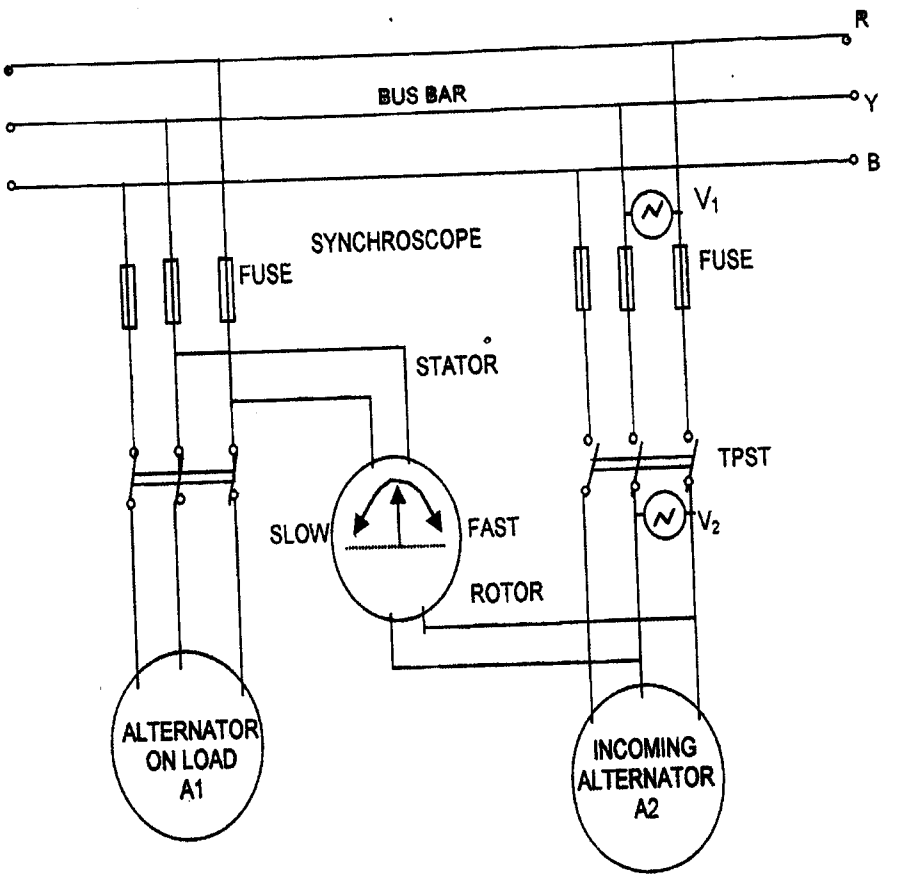


FIG. 1.3. SYNCHROSCOPE METHOD

1.4 ADVANTAGES OF ELECTRONIC SYNCHRONIZATION

By using existing methods for synchronizing process, we have to face certain difficulties and it will give only approximate results. So we go for electronic synchronizer whose advantages are discussed below.

1.4.1 No need for meters

If we use electronic synchronizer for synchronizing purpose there is no need for meters i.e voltmeters and frequency meters. Without these meters we can check terminal voltages of two alternators.

1.4.2 Accuracy

This project gives accurate results than the existing methods. It senses very small variation in voltages in the range of 0 to 2V. Also it detects very small variation in frequencies in the range of 0 to 1 Hz.

1.4.3 Lower cost

Cost involved in the design and maintenance o the electronic synchronizer is very less when compared to other existing methods of synchronization .

1.4.4 Compact in size

The size of the electronic synchronizer is very small and it is portable. It occupies very small space when compared to other methods .

1.4.5 Less power consumption

The power required for the control circuits and checking circuits are very low. It does not require any high wattage lamps an in the case of dark and bright lamp methods. It needs only 12V dc supply for control circuits.

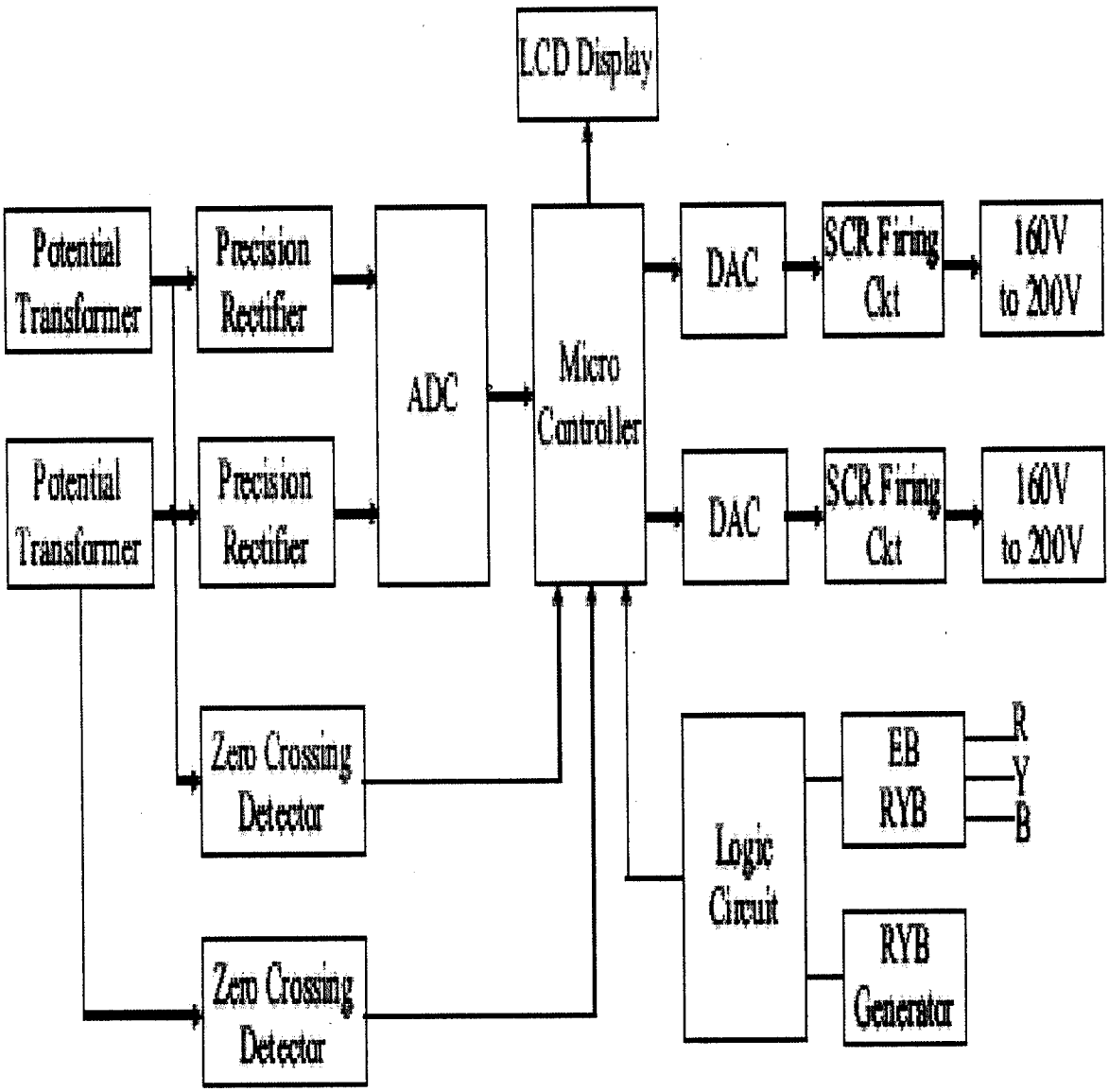
1.4.6 Easily Understandable

Electronics synchronizer gives visual signal to the operator when after satisfying condition. From this we can know which condition is not satisfied.

CHAPTER -2

BLOCK DIAGRAM & MODULES

FIGURE 2.1 Block diagram



2.1 BLOCK DIAGRAM

The general block diagram is shown in the figure 2.1 .The figure shows the layout of the control circuit.

Control circuits check the conditions to be satisfied before synchronization. The necessary conditions are

- Terminal voltages should be same.
- Frequency of both alternator and the EB supply should be same
- Phase sequence should be same.

Once the above mentioned conditions are checked ,the alternator is ready to be synchronized with the EB supply. once the alternators are connected in parallel , they supply a common load. The LCD display gives the indication for the process of synchronization.

The potential transformer is used to step down the AC supply voltage to the level needed for the operation of the electronic components. There are two potential transformers used in this circuit. One is used for stepping down the voltage from the AC supply of the EB mains and the other is used for stepping down the voltage from the alternator. The precision rectifier is used for converting the AC voltage into DC voltage as the electronic components needed a regulated DC power supply. The purpose of using the precision rectifier is that the losses in the case of precision rectifiers is small when

The zero crossing detector is used to measure the frequency of both EB supply and the alternator output voltage. The A/D converter changes analog voltage into digital signal. The digital signal is fed to the micro controller. The logic circuit is used for checking the phase sequence of both the alternator and the EB supply.

The LCD display which is interfaced with the micro controller displays the voltage ,frequency of both the alternator and the EB supply. The micro controller compares the voltage, frequency and phase sequence . the micro controller adjusts the DAC voltage accordingly such that both the voltages and frequencies get synchronized. If there is a difference of voltage , the field voltage of the alternator is varied automatically until both the voltages remains same. If there is a difference in frequency the field voltage of the motor is varied automatically until both the frequencies match each other.

2.2 MODULES OF THE PROJECT

Our project is divided into three modules. These three modules checks the different conditions that are to be satisfied before synchronization process. These three modules are listed below.

- voltage comparison circuit.
- Frequency comparison circuit
- phase sequence detection circuit.

Brief operation and performance of each and every module is described below.

2.2.1 Voltage comparison circuit

The AC voltage of the both alternator and EB supply is stepped down by using potential transformer and it is rectified to DC voltage using precision rectifier . The precision rectifier output is a DC voltage. A/D converter changes the analog input into digital signal. The digital output is fed to the micro controller. The micro controller compares the voltages of both the alternator and the EB supply. If there is a difference in voltage then the micro controller varies the firing angle of the SCR by varying the DAC voltage .

If there is a difference in voltage the field voltage of the alternator is adjusted by varying the firing angle of the SCR..The output of the alternator

is given as the input ,so a feed back path is formed. Any change in the field voltage will affect the output voltage. The micro controller compares both the voltages always. The output of the alternator increases with the increase in the field voltage of the alternator. The loop is executed as long as the two voltages become equal. The advantage of using precision rectifier is the drop is very less when compared to the diode rectifier

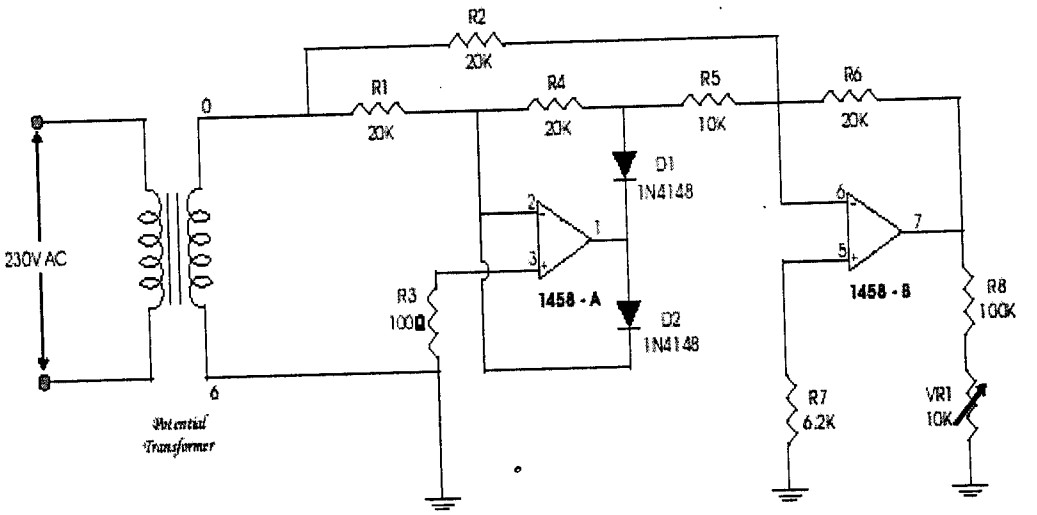


FIGURE 2.2 Voltage measuring circuit

2.2.2 Frequency comparison circuit

The frequency measurement circuit is shown in the figure 2.3. The AC voltage is stepped down using potential transformer. The output of the potential transformer is given to op-amp LM 741. The comparator is connected to the transistor BC547. When the input sine wave of the inverting terminal crosses 0v from negative to positive cycle, the output

When the sine wave crosses the zero from +ve to –ve half cycle, the output wave form is suddenly shifted to the high state from the ground state. Thus the zero crossing detector generates square wave for the given sine wave.

The micro controller compares the two frequencies. If there is any difference of frequency ,the micro controller varies the field voltage of the motor. If the field voltage of the motor increases then the speed of the motor decreases. Consequently the frequency of the alternator supply also decreases.

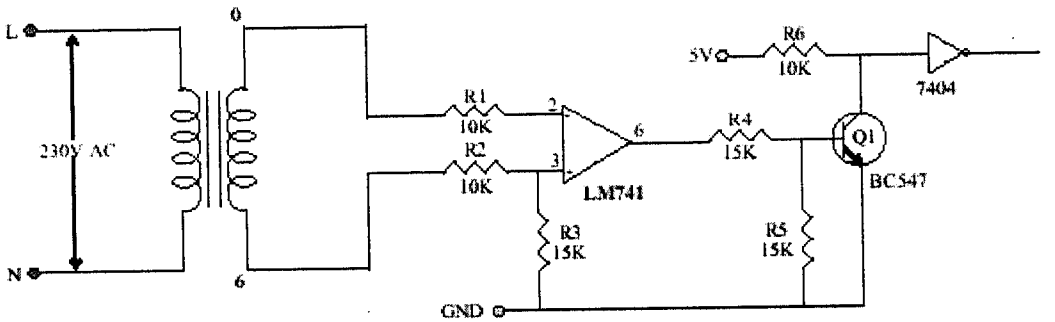


FIGURE 2.3 Frequency measuring circuit

2.2.3 PHASE SEQUENCE DETECTION

In a three phase supply system the order in which the three phases namely R,Y,B attain their maximum value is called the phase sequence.

If the sequence is R-Y-B, it is called correct sequence or if the sequence is called incorrect phase sequence. Usually the phase sequence of

meter. In this type there would be friction due to the moving system and heating due to the resistance of coils. This in turn would lead to wrong results. Also the method of phase sequence meter is costlier. Nowadays logic circuits have been used to find the phase sequence. The disadvantages in the previous methods have been overcome in this method . More over the operation of logic circuit is very faster when compared to the older methods.

The correct phase sequence is R,Y,B sequence . The phases R and Y are compared .In this case the phase R must come before Y if the phase sequence is proper. Similarly Y and B are compared .If the phase Y comes before B then the phase sequence is proper. Now if both the sequences are correct ,then the phase sequence is R,Y,B. otherwise the phase sequence is improper. If the phase sequence of both the alternator and the generator are matched, then the condition for synchronization is satisfied.

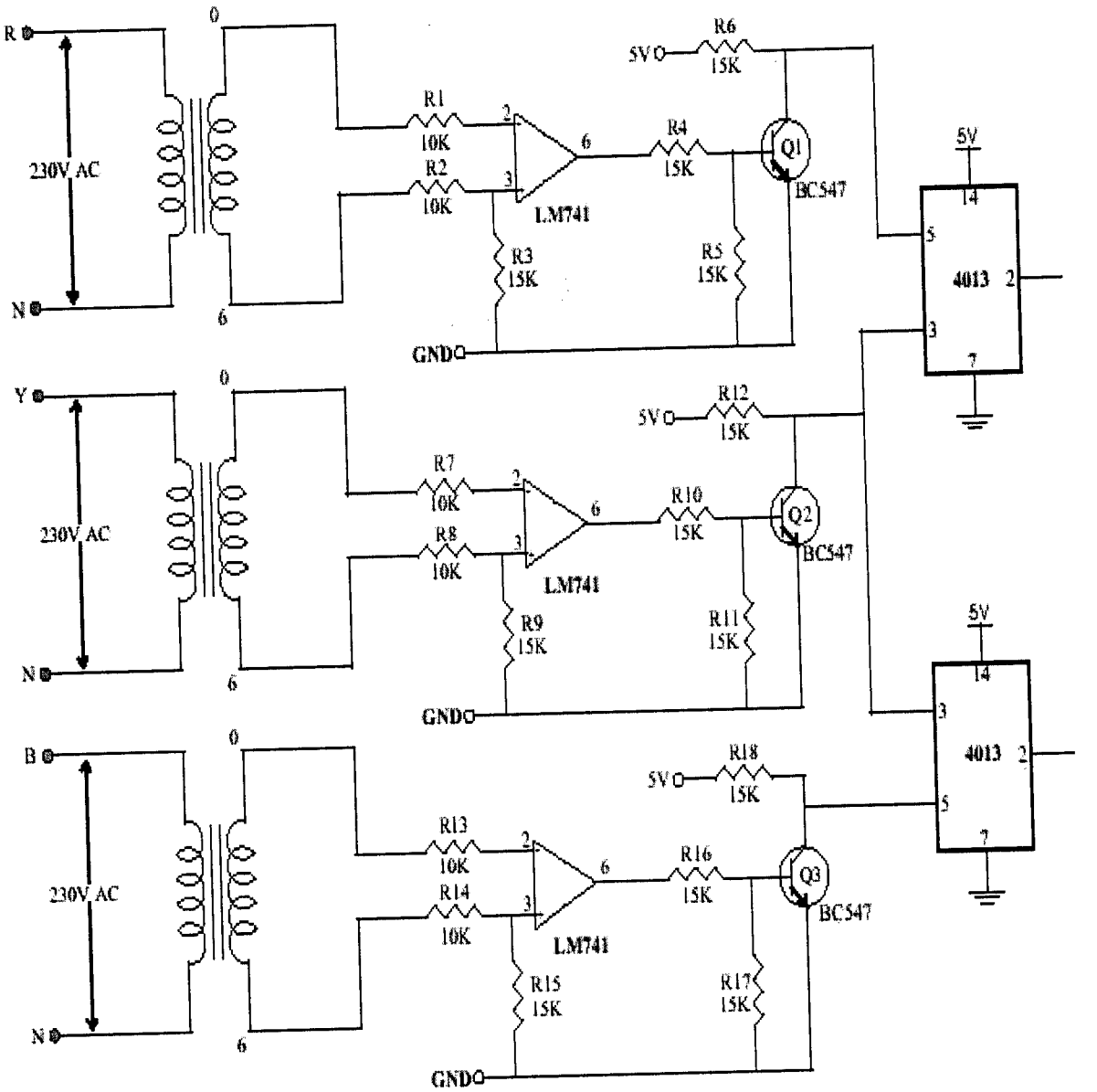


FIGURE 2.4 Phase sequence detection circuit

CHAPTER - 3

HARDWARE DESCRIPTION

3.1 POWER SUPPLY

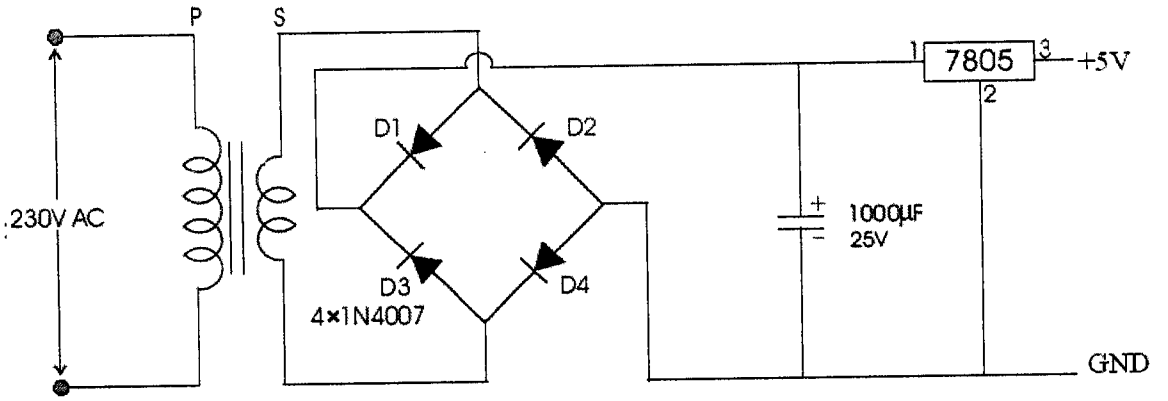


FIGURE 3.1 Power supply

The present chapter introduces the operation of power supply circuits built using filters, rectifiers, and then voltage regulators. Starting with an ac voltage, a steady dc voltage is obtained by rectifying the ac voltage, then filtering to a dc level, and finally, regulating to obtain a desired fixed dc voltage. The regulation is usually obtained from an IC voltage regulator unit, which takes a dc voltage and provides a somewhat lower dc voltage, which remains the same even if the input dc voltage varies, or the output load connected to the dc voltage changes.

3.2 BLOCK DIAGRAM

A block diagram containing the parts of a typical power supply and the voltage at various points in the unit is shown in fig . The ac voltage, typically 120V RMS, is connected to a transformer, which steps that ac

provides a full-wave rectified voltage that is initially filtered by a simple capacitor filter to produce a dc voltage. This resulting dc voltage usually has some ripple or ac voltage variation. A regulator circuit can use this dc input to provide a dc voltage that not only has much less ripple voltage but also remains the same dc value even if the input dc voltage varies somewhat, or the load connected to the output dc voltage changes. This voltage regulation is usually obtained using one of a number of popular voltage regulator IC units.

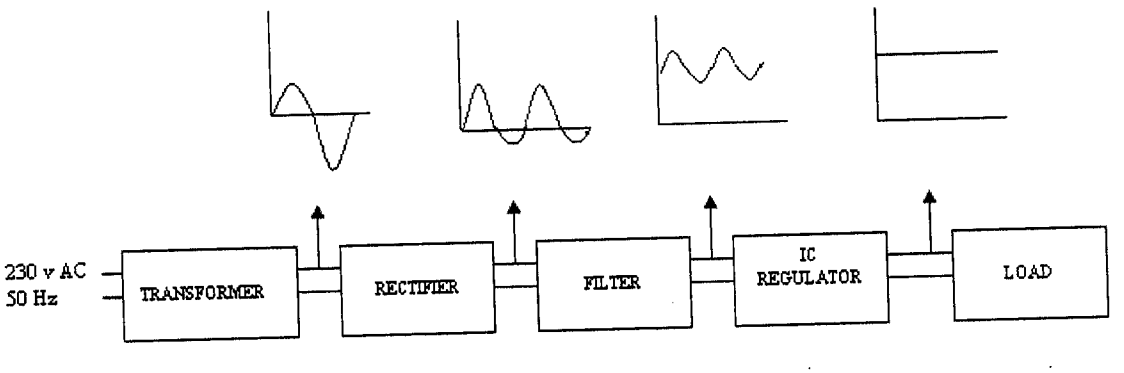


FIGURE 3.2 Block Diagram

3.3 IC VOLTAGE REGULATORS

Voltage regulators comprise a class of widely used ICs. Regulator IC units contain the circuitry for reference source, comparator amplifier, control device, and overload protection all in a single IC. Although the internal construction of the IC is somewhat different from that described for discrete

provide regulation of either a fixed positive voltage, a fixed negative voltage, or an adjustably set voltage.

A power supply can be built using a transformer connected to the ac supply line to step the ac voltage to a desired amplitude, then rectifying that ac voltage, filtering with a capacitor and RC filter, if desired, and finally regulating the dc voltage using an IC regulator. The regulators can be selected for operation with load currents from hundreds of milli amperes to tens of amperes, corresponding to power ratings from milliwatts to tens of watts.

3.3.1 THREE-TERMINAL VOLTAGE REGULATORS

Figure shows the basic connection of a three-terminal voltage regulator IC to a load. The fixed voltage regulator has an unregulated dc input voltage, Vi, applied to one input terminal, a regulated output dc voltage, Vo, from a second terminal with the third terminal connected to ground. For a selected regulator, IC device specifications list a voltage range over which the input voltage can vary to maintain a regulated output voltage over a range of load current. The specifications also list the amount of output voltage change resulting from a change in load current(load regulation) or in input voltage (line regulation).

3.3.2 FIXED POSITIVE VOLTAGE REGULATORS

The series 78 regulators provide fixed regulated voltages from 5 to

regulation with output from this unit of +12V dc. An unregulated input voltage Vi is filtered by capacitor C1 and connected to the IC's OUT terminal provides a regulated +12V which is filtered by capacitor C2(mostly for any high- frequency noise). The third IC terminal is connected to ground(GND). While the input voltage may vary over some permissible voltage range., and the output load may vary over some acceptable range, the output voltage remains constant within specified voltage variation limits. These limitations are spelled out in the manufacturer's specification sheets. A table of positive voltage regulated ICs provided in table .

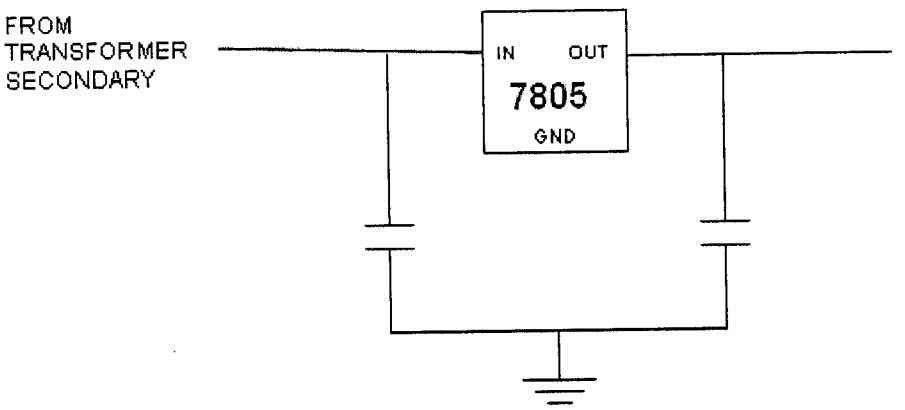


FIGURE 3.3 Positive voltage regulator

TABLE 1 POSITIVE VOLTAGE REGULATORS IN 7800 SERIES

IC PART	OUTPUT VOLTAGE (V)	MINIMUM Vi(v)
7805	+5	7.3
7806	+6	8.3
7808	+8	10.5
7810	+10	12.5
7812	+12	14.6
7815	+15	17.7
7818	+18	21.0
7824	+24	27.1

3.4 TRANSFORMER

A transformer is a static (or stationary) piece of which electric power in one circuit is transformed into electric power of the same frequency in another circuit. It can raise or lower the voltage in a circuit but with a corresponding decrease or increase in current. It works with the principle of mutual induction. In our project we are using step down transformer for providing a necessary supply for the electronic circuits. In our project we are using a (0-12)V transformer.

3.5 RECTIFIER

The DC level obtained from a sinusoidal input can be improved 100% using a process called full-wave rectification. It uses 4 diodes in a bridge configuration. From the basic bridge configuration we see that two diodes(say D2&D3) are conducting while the other two diodes(D1&D4) are in "off" state during the period t=0 to T/2. Accordingly for the negative of the input the conducting diodes are D1&D4. Thus the polarity across the load is the same.

3.6 FILTER

The filter circuit used here is the capacitor filter circuit where a capacitor is connected at the rectifier output, and a DC is obtained across it. The filtered waveform is essentially a DC voltage with negligible ripples,

3.7 RELAYS

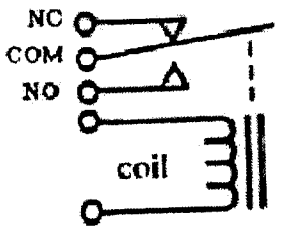


Figure 1

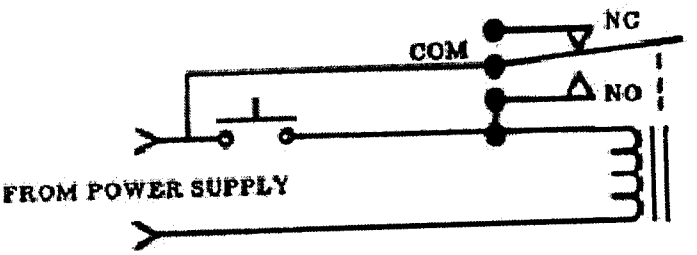


Figure 2

FIGURE 3.4 Relay

Early digital logic circuits employ relays to perform all of the required functions. A relay is constructed from three very basic components: an electromagnet, a switch, and a spring. But where most switches are activated by pushing a button or throwing a lever, the switch (or switches) in a relay change state when voltage is applied to the coil of the electromagnet. The voltage causes the iron core to become magnetized, which then pulls the metal switch contacts into position.

And when the voltage is removed, the spring takes over and pulls the contacts back. Most relays contain at least two switches, though some have as many as four or more, offering a wide range of possible circuit combinations .Since drawing a realistic picture of an electronic component is not always the most efficient way to convey a circuit, electronic engineers instead use a schematic diagram. Most schematic representations are really pretty close to what an equivalent picture might look like, and a relay is shown both ways for you to compare. Figure shows the schematic for a single-pole (one switch) double-throw relay. The term double-throw means

possible contacts: normally open, or normally closed. That is, when the relay is at rest with no voltage applied to its coil, the common contact is connected to the normally closed contact. And when the relay is activated, the common will be connected to the normally open one instead.

3.8 ZERO CROSSING DETECTORS

The detector circuit is to analyze the state of input of the sine wave at any instant. The basic comparator circuit can be modified as zero crossing detector. Here we have adopted the general purpose op-amp (IC741).

Op_amps have five basic terminals that is , two input terminals, one output terminal, two power supply terminals. The significance of other terminal varies with the type of op_amp. The general purpose op_amp has eight pins. Pin 2 is called the inverting input terminal andpin 3 is non inverting input terminal, pin 6 is the output terminal and pins 7 and 4 are the supply terminals labeled as v+ and v- respectively. Terminals 1 and 5 are used for DC offset. The pin 8 marked NC indicates no connection. The v+ and v- power supply terminal s are connected to two DC voltage sources . v+ is connected to the positive terminal of one source and v- is connected to the negative terminal of other source. The power supply voltage range from about 5V to 22V. The common terminal of v+ and v- pin is connected to the reference or ground

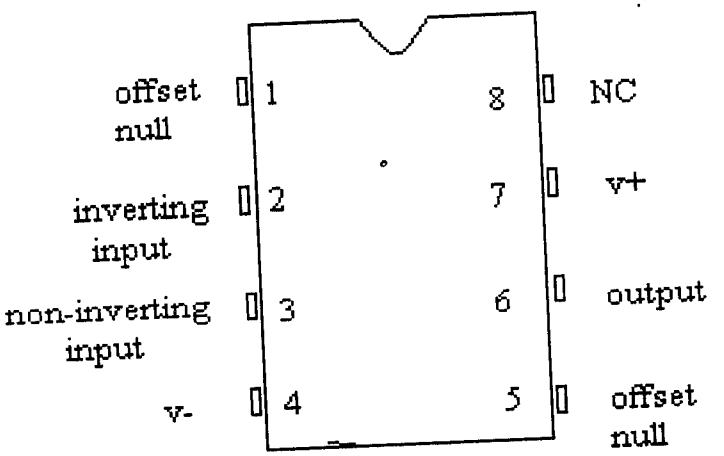


FIGURE 3.5 Pin Diagram.

3.8.1 ZERO CROSSING DETECTION

The input supply is Stepped down to six volt and is given to the inverting terminal of the op-amp through a resistance of 1k. The non inverting terminal is connected to the found of the supply. The v+ pin is connected to the ground of the controller supply. The output is taken from the pin 6 through a resistance of 220Ω and is fed to the input port of the controller. This is the extension of basic comparator with vref being to set to zero.

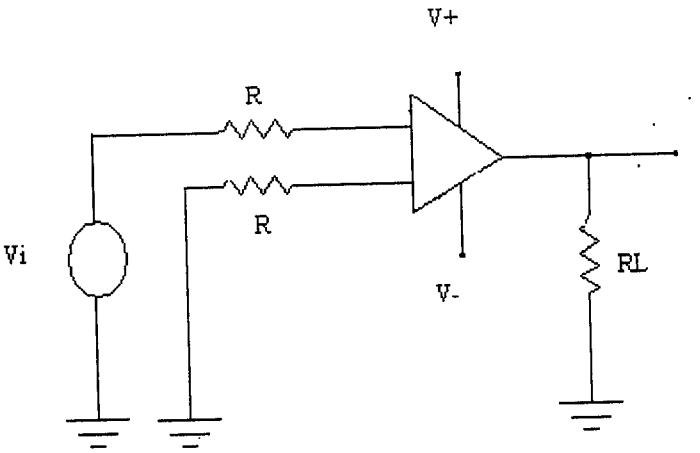
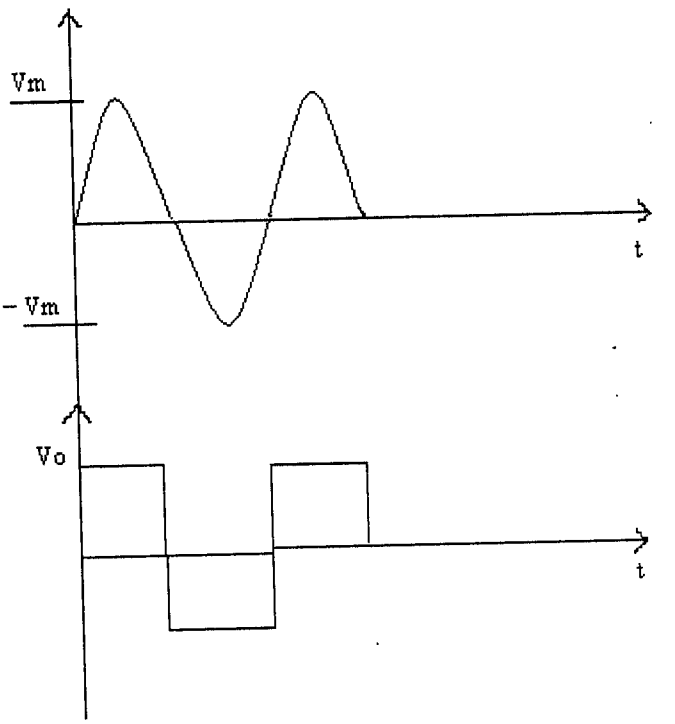


FIGURE 3.6 Zero crossing detector



When the input sine wave of the inverting terminal crosses 0v from negative to positive cycle, the output waveform of zero crossing detector shifts from +Vsat value to ground state. When the sine wave crosses the zero from +ve to –ve half cycle, the output wave form is suddenly shifted to the high state from the ground state. Thus the zero crossing detector generates square wave for the given sine wave. So this circuit is called sine to square wave generator.

3.9 FULL-WAVE PRECISION RECTIFIER

An absolute-value circuit, or full-wave precision rectifier, can be implemented by summing the output of a half-wave rectifier and its input with the proper phase and amplitude relations. Such a circuit in its basic form is shown in figure. This circuit will be the starting point for a number of other absolute-value circuits, which have evolved from this basic form.

In this circuit, A1 is an inverting rectifier similar to the figure. The output from A1 is added to the original input signal in A2 (a summing mixer) with the signal amplitude and phase relations shown. Negative alterations of Ein feeds A2 through 20-kΩ resistor, and E1 feed A2 through a 10-kΩ resistor. The net effect of this scaling is that, for equal amplitudes of Ein and E1, E1will provide twice as much current into the summing point. This fact is used to advantage here, as the negative alteration of E1 produces twice the input current of that caused by the positive alternation of Ein. This causes a current of precisely half the amplitude, which E1 alone would generate due to the subtraction of Ein. It is the equivalent of having E1 feed

through a 20-kΩ input receiver and having Ein non-existent during this half cycle, and it results in a positive going output at A2. During negative alterations of Ein, E1 is absent and Ein produces the alternate positive output swing that, in summation, produces the desired full-wave rectified response. As before, operation with the opposite output polarity is possible by reversing D1 and D2.

The general –purpose dual-741 type indicated can be replaced with higher-speed units or FET types, as appropriate. The relation-ships between resistors for proper circuit operation are noted in the illustration, and may be satisfied best by a single network. Note that resistor R6 can be used as an overall gain trim, or for scaling to net gains of (n) other than unity, as is shown by the equations. If impedance is raised, FET input units, such as the 3240, TL082, etc., are effective. With high impedances, low-leakage diodes are suggested.

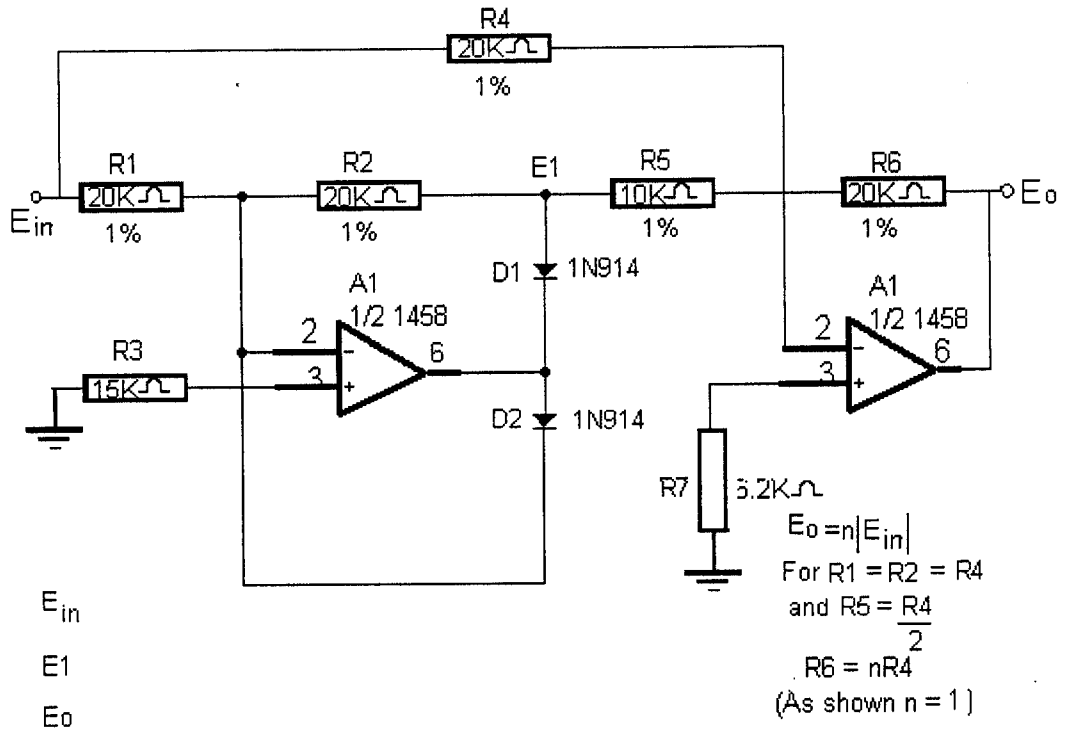


FIGURE 3.8 Precision rectifier.

3.10 ARCHITECTURE OF 8255

From the internal block diagram of the 8255A, you can see that the device has 24 input/output lines. Port A can be used as an 8 bit input port or as an 8 bit output port. Likewise, port B can be used as an 8 bit input port or as an 8 bit output port. Port C can be used as an 8-bit input or output port, two 4 bit ports or to produce handshake signals for ports A and B. Along the left side ports or to produce handshake signals for ports A and B. Along the left side of the diagram you see the signals lines used to connect the device to the system buses. Eight data lines allow you to write data bytes to a port or the control register and to read bytes from a port or the status register under the control of the register. The internal addresses for the device are:

port A-00, port B-01, port C-10, control register-11. Asserting the input of the address decoder circuitry to select the device when it is addressed.

The RESET input of the 8255A is connected to the system RESET line so that when the system is reset all of the port lines are initialized as input lines this is done to prevent destruction of circuitry connected to port lines. If port lines were initialized as outputs after a power up or reset the port might try to input into the output of a device connected to the port. The possible argument between the outputs might destroy one or both of them. Therefore all of the programmable port devices initialize their port lines as inputs when reset.

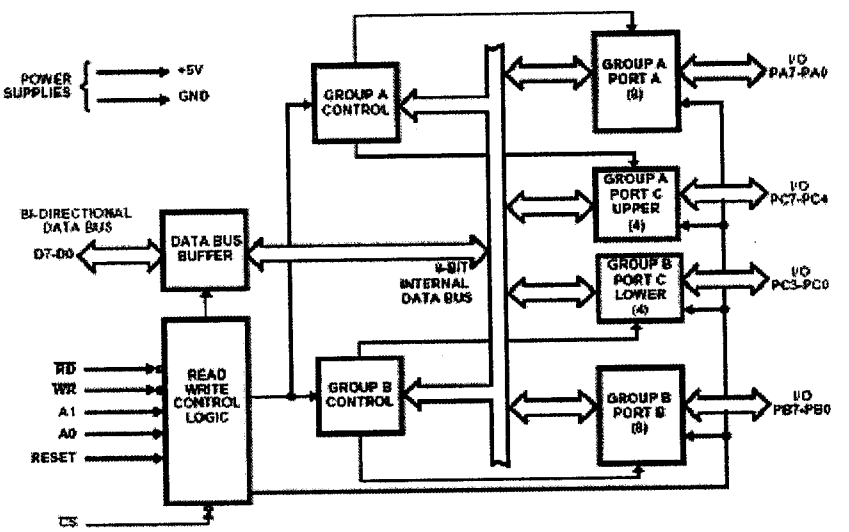


FIGURE 3.9. Functional diagram

3.10.1 MODES AND INITIALIZATION:

- Modes in which the ports of the 8255 A can be initialized.
- Programming the 8255A

The MSB of the control word tells the 8255A which control word you are sending it. You use the bit set\reset control word format when you want to set or reset the output on a pin or port C or when you want to enable the interrupt output signals for handshake data transfers. The MSB is 0 for this control word. Both control words are sent to the control register address for the 8255 A. as usual making up a control word consists of figuring out what to put in the 8 boxes one at a time.

Suppose that you want to output a 1 to (set) bit 2 of port C, which was initialized as an output with the mode set control word above. To set or reset a port C output pin you use 1 in the bit set\reset control word as shown. Take bit D7 a 0 to identify this a bit set\reset control and put a 1 in bit D0to specify that you want to set a bit of port C. bits D3, D2, D1 are used to tell the 8255 A which bit you want to act on.

3.10.2 TIMING OF THE 8255A operations:

To be able to interface the 8255A PPI devices, the system designer must have an understanding of timings associated with it's various operations. In this section we shall discuss the timings of read\write operations for data transfer between the peripherals devices and 8255A.

- Mode 0 data transfer
- Mode 1 data transfer
- Mode 2 data transfer

Read\write operations:

The read and write timing of the 8255A. These timings are relatively easy to understand and therefore not collaborated further.

Mode 0 data transfer:

The timings of data transfer from upto any of the ports in mode0. The μp reads data from a port by executing an IM instruction. The port specified in this instruction must select the 8255A and chip set A0 & A1. The RD input from the bus to the addressed port on to the data output lines after TRD time units, the data input to the port is placed on the data bus. The tie units prior to RD are going low. The data outputs are tristated after a delay of tdf from the raising edges of RD.

The timing for data output operation is similar to the read timings. The WR in/out controls data transfer from the bus to the output port. Upon completion of the write operation indicated by WR going high the output is available at the accessed port after a maximum delay of t wb.

Mode 1 data transfer

The mode 1 data transfer timing, data transfer in this mode begins with the input device asserting the strobe STB. The fact that the input device has activated to the external circuitry by setting the IBF output high. Input data from this device is latched at the trailing edge of the strobe. After the

device has removed the strobe, the INTR output goes high. The CPU will respond some time latter by executing an input instruction to read the data from the relevant port.

The INTR output of A go low on the falling of the RD input. The IBF output goes low after RD input gets inactive. That completes 1 byte of data transfer from the device of the CPU using strobe input. Notice that as the 8255A latch the input it does not matter how long it takes the CPU to respond to the interrupt.

- The output data transfer begins with CPU writing a byte of data to an output port. The strobe output timing after the CPU has completed the write operation as indicated by the WR input going high the OBF output goes low.

Mode 2 Data transfer:

This is known as the strobed bi-directional bus input/output mode. Only port A can operate in this mode. PC3-PC2 serve as control signals for data transfer in this mode. When in this mode 2 port A can be used for receiving and transmitting data to a peripheral device. The devices can strobe into the port using the STB input. The 8255 A can strobe data to the device using OBF output. The different control signals associated with mode 2 operations.

In addition to their use in basic input/output mode, individual bits of port C can be controlled directly by the CPU. Using this bit set\reset feature the CPU can send a command to the 8255A for setting\reseting any one of

the 8 bits of port C. here it is assumed that the bit which is being affected this way corresponds to an output pin on the 8255A.

As an e.g. it is possible to connect 8 LED's one to each output pin of port C and then selectively turn them ON or OFF. An another e.g. port C outputs can be used to control relays. Individual relays can then be turned ON/OFF using bit set/reset command. It may be noted that bit set corresponds to setting a bit to 0 (low) and reset to setting a bit to 1(high).

3.10.3 DATA TRANSFER:

The data is transferred from 8255A to the PC bus when it is selected through 74LS245 from PC bus and store the input in the RAM.

Table 3.2. Basic operation of 8255

A1	A0	RD	WR	CS	INPUT OPERATION (READ)
0	0	0	1	0	Port A → Data Bus
0	1	0	1	0	Port B → Data Bus
1	0	0	1	0	Port C → Data Bus
1	1	0	1	0	Control Word → Data Bus
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	Data Bus → Port A
0	1	1	0	0	Data Bus → Port B
1	0	1	0	0	Data Bus → Port C
1	1	1	0	0	Data Bus → Control
					DISABLE FUNCTION
X	X	X	X	1	Data Bus → Three-State

3.11 ADC 0808/0809

The ADC 0809 has one type of 8-bit ADC, which can very easily be interfaced with any of the microprocessors. This type of converter changes the analog voltage input V in to an 8-bit digital output (D7-D0). The conversion process is initiated by a pulse applied to the ADC's START conversion terminal. The completion of conversion takes an amount of time depending upon the method of conversion time can be as large as 100ms for some ADC.

The features of ADC 0808/0809:

- High speed
- High accuracy
- Minimal temperature dependence
- Excellent long term accuracy and repeatability
- Consume minimal power

This ADC 0808/0809 does not contain the sample-and-hold circuit. If a sample-and-hold circuit is required, it could be connected before the multiplexes. The input states for the address lines to select any particular channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

3.12 DAC CHIP 0800

The DAC 0800 series are monolithic 8 bit high speed current output digital to analog converter (DAC) featuring typical setting time of 100ns.

reference current range is possible. The DAC 0800 series also features high compliance complementary current outputs to allow differential output voltages of 20V peak to peak with simple resistor loads. The reference to full scale current matching of better ±1LSB eliminates the need for full scale trims in most applications while the nonlinearities of better than ±0.1% over temperature minimizes system error accumulations.

The noise immune inputs of the DAC0800 series will accept TTL levels with the logic threshold pin, V_{lc} grounded. Simple adjustments of the Vlc potential will allow direct interface to all logic families. The performance and characteristics of the device are essentially unchanged over the full ±4.5V to ±18V power supply range; power dissipation is only 33mW with ±5V supplies and is independent of the logic input states.

Features:

- Fast setting output current 100ns
- Full scale error ±1 LSB
- Nonlinearity over temperature ±0.1%
- Full scale current drift ±10ppm/°C
- High output compliance ±10V to +18V
- Complementary current outputs
- Interface directly with TL, CMOS, PMOS, and others
- 2 quadrant wide range multiplying capability
- Wide power supply range ±4.5V to ±18V
- Low power consumption 33mW to ±5V

3.13 D-TYPE FLIP FLOP

The CD4013B dual D-type flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement mode transistors. Each flip-flop has independent data, set, reset, and clock inputs and "Q" and "Q" outputs. These devices can be used for shift register applications, and by connecting "Q" output to the data input, for counter and toggle applications. The logic level present at the "D" input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line respectively

3.13.1 Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 VDD (typ.)
- Low power TTL: fan out of 2 driving 74L

3.13.2 Applications

- Automotive
- Data terminals
- Instrumentation

TABLE 3.3 Truth Table for D-Type flip flop

CL (Note 1)	D	R	S	Q	$\overline{Q}$
⎽▔	0	0	0	0	1
⎽▔	1	0	0	1	0
▔⎽	X	0	0	Q	$\overline{Q}$
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

X — don't care case

CHAPTER – 4

MICRO CONTROLLER DETAILS

4.1 INTRODUCTION

The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K bytes of Flash programmable and erasable read only memory (PEROM). The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard MCS-51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer.

The AT89C51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power-down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

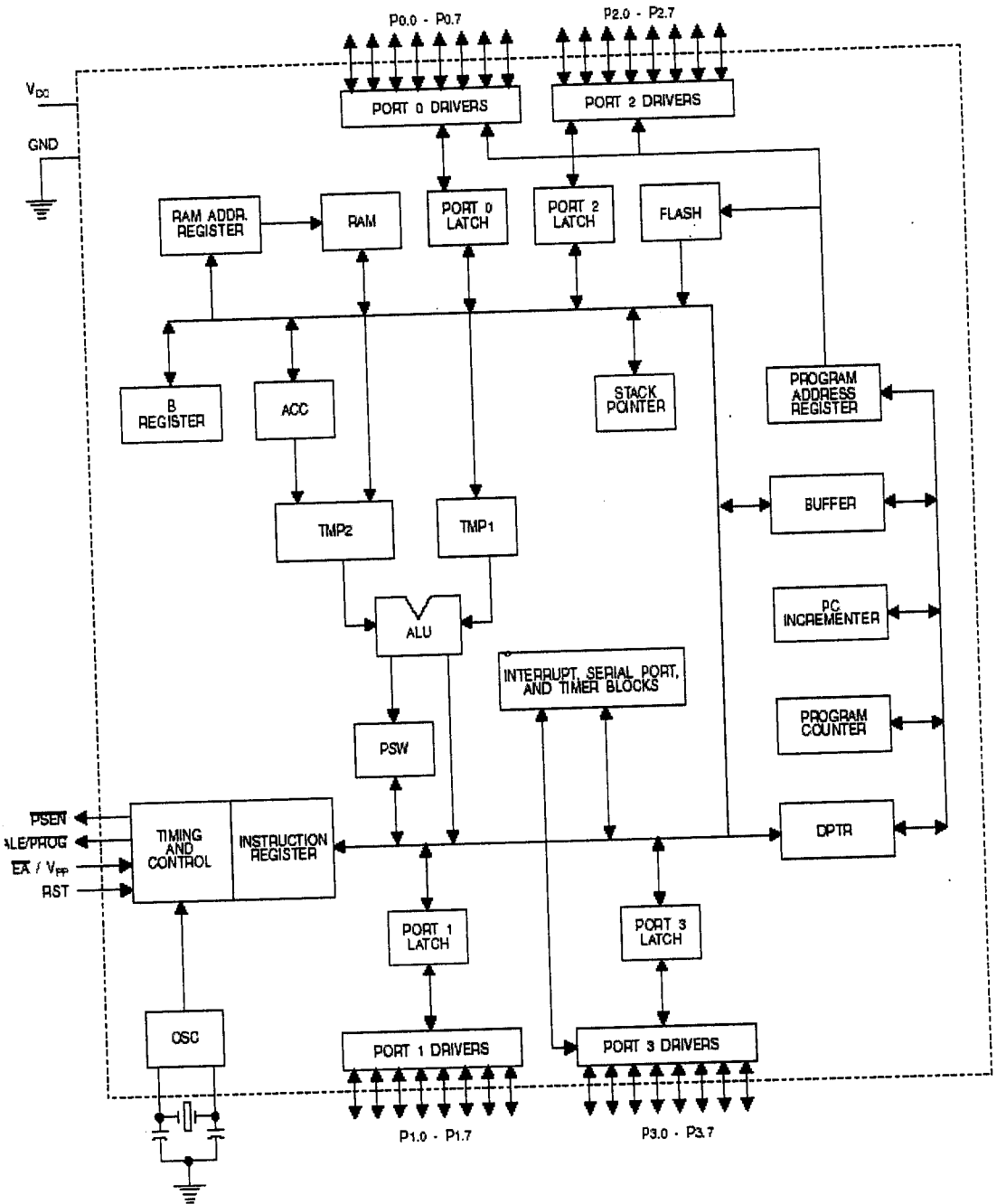
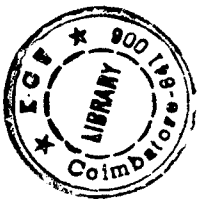


FIGURE.4.1 Block Diagram

4.2 FEATURES



- 80C51 based architecture
- 4-Kbytes of on-chip Reprogrammable Flash
- Memory
- 128 x 8 RAM
- Two 16-bit Timer/Counters
- Full duplex serial channel
- Boolean processor
- Four 8-bit I/O ports, 32 I/O lines
- Memory addressing capability
- 64K ROM and 64K RAM
- Program memory lock
- Lock bits (3)
- Power save modes:
- Idle and power-down
- Six interrupt sources
- Most instructions execute in 0.3 ms
- CMOS and TTL compatible
- Maximum speed: 40 MHz @ Vcc = 5V

FIGURE 4.2 Pin diagram of 89C51

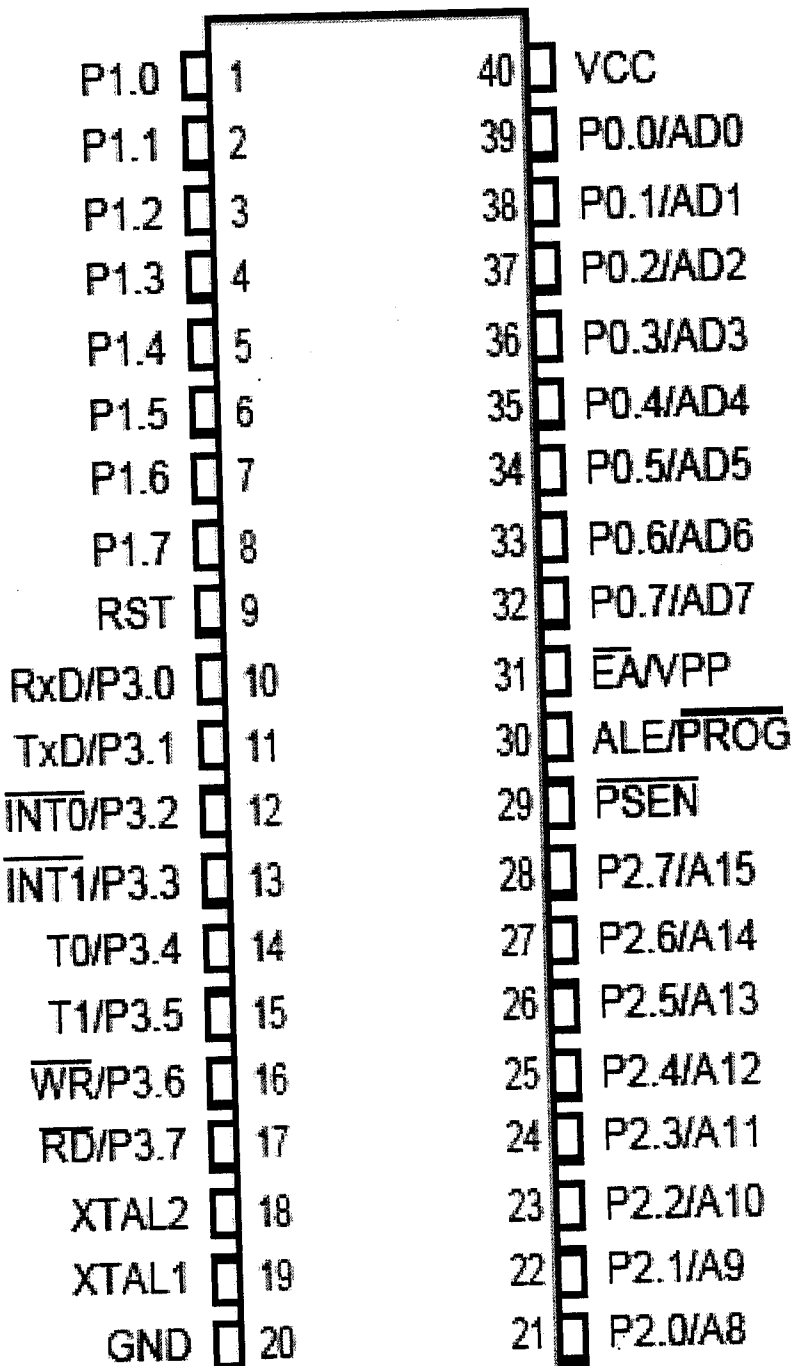


TABLE 4.1 Pin description of 89C51

Symbol	PDIP	PLCC	PQFP	I/O	Name and Function
ALE/$\overline{PROG}$	30	33	27	I/O	**Address Latch Enable:** Output pulse for latching the low byte of the address during an address to the external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the Program Pulse input ($\overline{PROG}$) during Flash programming.
$\overline{EA}$/V_{PP}	31	35	29	I	**External Access enable:** $\overline{EA}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H to FFFFH. If $\overline{EA}$ is held high, the device executes from internal program memory unless the program counter contains an address greater than 0FFFH. This also receives the 12V programming enable voltage (V_{PP}) during Flash programming.
P0.0-P0.7	39-32	43-36	37-30	I/O	**Port 0:** Port 0 is an 8-bit open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pullups when emitting 1s. Port 0 also receives the code bytes during programmable memory programming and outputs the code bytes during program verification. External pullups are required during program verification.
P1.0-P1.7	1-8	2-9	40-44 1-3	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 pins that have 1s written to them are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pullups. (See DC Characteristics: I_{IL}) The Port 1 output buffers can sink/source four TTL inputs. Port 1 also receives the low-order address byte during Flash programming and verification.
P2.0-P2.7	21-28	24-31	18-25	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pullups. Port 2 pins that have 1s written to them are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pullups. (See DC Characteristics: I_{IL}) Port 2 emits the high order address byte during fetches from external program memory and during accesses to external data memory that used 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ Ri [i = 0, 1]), Port 2 emits the contents of the P2 Special Function Register. Port 2 also receives the high-order bits and some control signals during Flash programming and verification. P2.6 and P2.7 are the control signals while the chip programs and erases.

Symbol	PDIP	PLCC	PQFP	I/O	Name and Function
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with inter pullups. Port 3 pins that have 1s written to them are pulled h by the internal pullups and can be used as inputs. As inpu Port 3 pins that are externally pulled low will source curr because of the internal pullups. (See DC Characteristics: I Port 3 also serves the special features of the IS89C51, as lis below:
	10	11	5	I	**RxD (P3.0):** Serial input port.
	11	13	7	O	**TxD (P3.1):** Serial output port.
	12	14	8	I	**$\overline{\text{INT0}}$ (P3.2):** External interrupt 0.
	13	15	9	I	**$\overline{\text{INT1}}$ (P3.3):** External interrupt 1.
	14	16	10	I	**T0 (P3.4):** Timer 0 external input.
	15	17	11	I	**T1 (P3.5):** Timer 1 external input.
	16	18	12	O	**$\overline{\text{WR}}$ (P3.6):** External data memory write strobe.
	17	19	13	O	**$\overline{\text{RD}}$ (P3.7):** External data memory read strobe.
$\overline{\text{PSEN}}$	29	32	26	O	**Program Store Enable:** The read strobe to external prog memory. When the device is executing code from the exte program memory, $\overline{\text{PSEN}}$ is activated twice each machine c except that two $\overline{\text{PSEN}}$ activations are skipped during e access to external data memory. $\overline{\text{PSEN}}$ is not activated du fetches from internal program memory.
RST	9	10	4	I	**Reset:** A high on this pin for two machine cycles while oscillator is running, resets the device. An internal MOS res to GND permits a power-on reset using only an exte capacitor connected to Vcc.
XTAL 1	19	21	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and in to the internal clock generator circuits.
XTAL 2	18	20	14	O	**Crystal 2:** Output from the inverting oscillator amplifier.
GND	20	22	16	I	**Ground:** 0V reference.
Vcc	40	44	38	I	**Power Supply:** This is the power supply voltage for opera

4.3 MEMORY

The IS89C51 has separate address spaces for program and data memory. The program and data memory can be up to 64K bytes long. The lower 4K program memory can reside on-chip. Figure 5 shows a map of the IS89C51program and data memory. The IS89C51 has 128 bytes of on-chip RAM, plus numbers of special unction registers. The lower 128 bytes can be accessed either by direct addressing or by indirect addressing. The lower 128 bytes of RAM can be divided into three
segments as listed below .

1.Register Banks 0-3:

Locations 00H through 1FH (32bytes). The device after reset defaults to register bank0. To use the other register banks, the user must select them in software. Each register bank contains eight 1-byte registers R0-R7. Reset initializes the stack point to location 07H, and is incremented once to start from 08H, which is the first register of the second register bank.

2. Bit Addressable Area:

16 bytes have been assigned for this segment 20H-2FH. Each one of the 128 bits of this segment can be directly addressed (0-7FH). Each of the 16 bytes in this segment can also be addressed as a byte.

3. Scratch Pad Area:

30H-7FH are available to the user as data RAM. However, if the data pointer has been initialized to this area, enough bytes should be left aside to

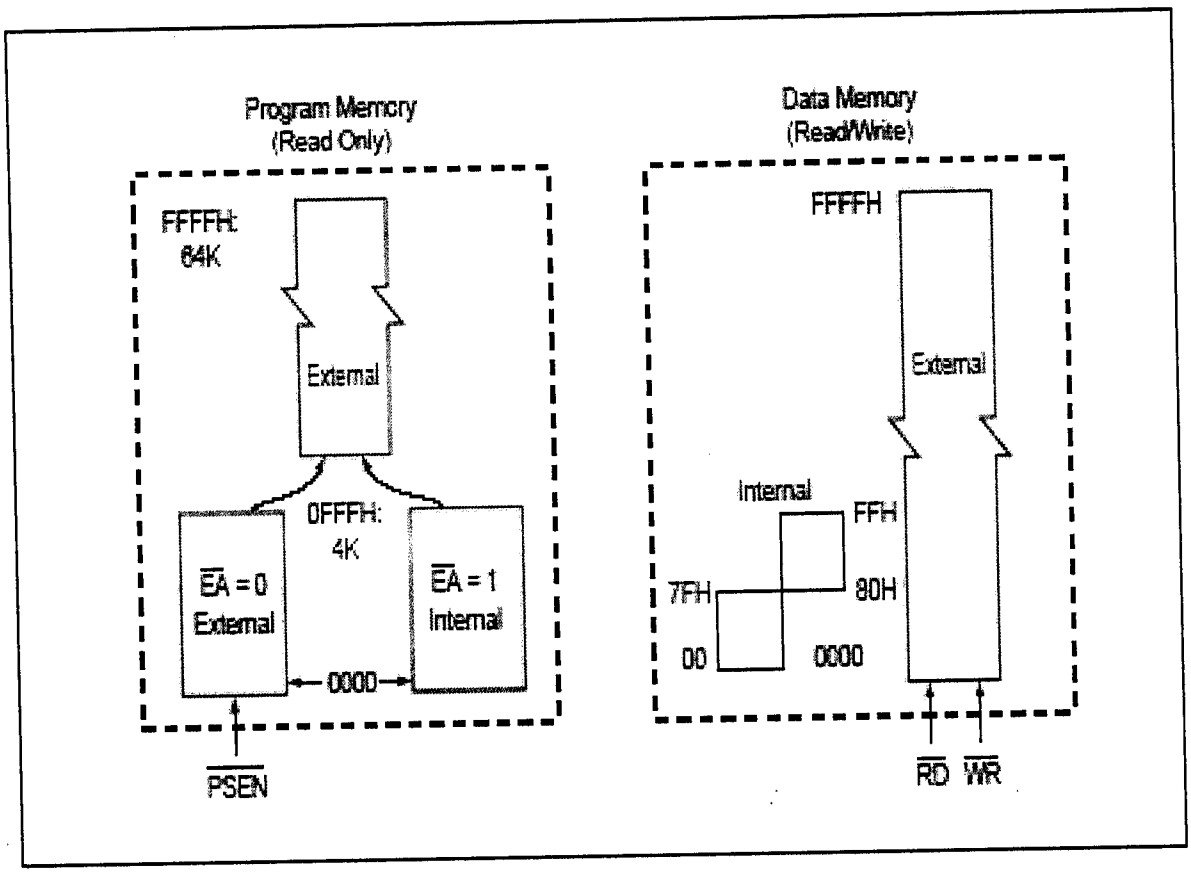


FIGURE 4.3 Programming and data memory structure

4.4 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFR's) are located in upper 128 Bytes direct addressing area. The SFR Memory Map shows that. Not all of the addresses are occupied. Unoccupied addresses are not implemented on the chip. Read accesses to these addresses in general return random data, and write accesses have no effect. User software should not write 1's to these

unimplemented locations, since they may be used in future microcontrollers to invoke new features. In that case, the reset or inactive values of the new bits will always be 0, and their active values will be 1.

4.4.1 Accumulator (ACC)

ACC is the Accumulator register. The mnemonics for Accumulator-specific instructions, however, refer to the Accumulator simply as A.

4.4.2 B Register (B)

The B register is used during multiply and divide operations. For other instructions it can be treated as another scratch pad register.

4.4.3 Program Status Word (PSW).

The PSW register contains program status information.

4.4.4 Stack Pointer (SP)

The Stack Pointer Register is eight bits wide. It is incremented before data is stored during PUSH and CALL executions. While the stack may reside anywhere in on chip RAM, the Stack Pointer is initialized to 07H after a reset. This causes the stack to begin at location 08H.

4.4.5 Data Pointer (DPTR)

The Data Pointer consists of a high byte (DPH) and a low byte (DPL). Its function is to hold a 16-bit address. It may be manipulated as a 16-bit register or as two independent 8-bit registers.

4.4.6 Ports 0 To 3

P0, P1, P2, and P3 are the SFR latches of Ports 0, 1, 2, and 3 respectively.

4.4.7 Serial Data Buffer (SBUF)

The Serial Data Buffer is actually two separate registers, a transmit buffer and a receive buffer register. When data is moved to SBUF, it goes to the transmit buffer, where it is held for serial transmission. (Moving a byte to SBUF initiates the transmission.) When data is moved from SBUF, it comes from the receive buffer.

4.4.8 Timer Registers

Register pairs (TH0, TL0) and (TH1, TL1) are the 16-bit Counter registers for Timer/Counters 0 and 1, respectively.

4.4.9 Control Registers

Special Function Registers IP, IE, TMOD, TCON, SCON, and PCON contain control and status bits for the interrupt system, the Timer/Counters, and the serial port. They are described in later sections of this chapter.

4.5 TIMER/COUNTERS

The IS89C51 has two 16-bit Timer/Counter registers: Timer 0 and Timer 1. All two can be configured to operate either as Timers or event Counters. As a Timer, the register is incremented every machine cycle. Thus, the register counts machine cycles. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

Thus, the register counts machine cycles. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12
of the oscillator frequency .As a Counter, the register is incremented in response to a
1-to-0 transition at its corresponding external input pin, T0 nd T1. The external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected .Since two machine cycles (24 oscillator periods) are required
to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but it should be held for at least one full machine cycle to ensure that a given level is sampled at least once before it changes. In addition to the Timer or Counter functions, Timer 0 and Timer 1 have four operating modes: 13-bit timer, 16-bit timer,8-bit auto reload timer.

4.5.1 Timer 0 and Timer 1

The Timer or Counter function is selected by control bits C/T in the Special Function Regiser TMOD. These two Timer/Counters have four operating modes, which areselected by bit pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both Timer/Counters, but Mode 3 is different. The four modes are described in the following sections.

4.5.2 Mode 0:

Both Timers in Mode 0 are 8-bit Counters with a divide-by-32

this mode, the Timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the Timer interrupt flag TF1. The counted input is enabled to the Timer when TR1 = 1 and either GATE = 0 or INT1 = 1. Setting GATE = 1 allows the Timer to be controlled by external input INT1, to facilitate pulse width measurements. TR1 is a control bit in the Special Function Register TCON. Gate is in TMOD. The 13-bit register consists of all eight bits of TH1 and the lower five bits of TL1. The upper three bits of TL1 are indeterminate and should be ignored. Setting the run flag (TR1) does not clear the registers. Mode 0 operation is the same for Timer 0 as for Timer 1, except that TR0, TF0 and INT0 replace the corresponding Timer 1 signals in Figure 8. There are two different GATE bits, one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).

4.5.3 Mode 1:

Mode 1 is the same as Mode 0, except that the Timer register is run with all 16 bits. The clock is applied to the combined high and low timer registers (TL1/TH1). As clock pulses are received, the timer counts up: 0000H, 0001H, 0002H, etc. An overflow occurs on the FFFFH-to-0000H overflow flag. The timer continues to count. The overflow flag is the TF1 bit in TCON that is read or written by software.

4.5.4 Mode 2:

Mode 2 configures the Timer register as an 8-bit Counter (TL1) with automatic eload, as shown in Figure 10. Overflow from TL1 not only sets TF1, but also reloads TL1 with the contents of TH1, which is preset by software. The reload leaves the TH1 unchanged. Mode 2 operation is the

4.5.5 Mode 3:

Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0. Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. The logic for Mode 3 on Timer 0 is shown in Figure 11. TL0 uses the Timer 0 control bits: C/T, GATE, TR0, INT0, and TF0. TH0 is locked into a timer function (counting machine cycles) and over the use of TR1 and TF1 from Timer 1. Thus, TH0 now controls the Timer 1 interrupt. Mode 3 is for applications requiring an extra 8-bit timer or counter. With Timer 0 in Mode 3, the IS89C51 can appear to have three Timer/Counters. When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3. In this case, Timer 1 can still be used by the serial port as a baud rate generator or in any application not requiring an interrupt.

4.6 SERIAL INTERFACE

The Serial port is full duplex, which means it can transmit and receive simultaneously. It is also receive-buffered, which means it can begin receiving a second byte before a previously received byte has been read from the receive register. (However, if the first byte still has not been read when reception of the second byte is complete, one of the bytes will be lost.) The serial port receive and transmit registers are both accessed at Special Function Register SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register. The serial port can operate in the following four modes:

4.6.1 Mode 0:

Serial data enters and exits through RXD. TXD outputs the shift clock. Eight data bits are transmitted/received, with the LSB first. The baud rate is fixed at 1/12 the oscillator frequency (see Figure 12).

4.6.2 Mode 1:

Ten bits are transmitted (through TXD) or received (through RXD): a start bit (0), eight data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in Special Function Register SCON. The baud rate is variable.

4.6.3 Mode 2:

Eleven bits are transmitted (through TXD) or received (through RXD): a start bit (0), eight data bits (LSB first), a programmable ninth data bit, and a stop bit (1). On transmit, the ninth data bit (TB8 in SCON) can be assigned the value of 0 or 1. Or, for example, the parity bit (P, in the PSW) can be moved into TB8. On receive, the ninth data bit goes into RB8 in Special Function Register SCON, while the stop bit is ignored. The baud rate is programmable to either 1/32 or1/64 the oscillator frequency.

4.6.4 Mode 3:

Eleven bits are transmitted (through TXD) or received (through RXD): a start bit (0), eight data bits (LSB first), a programmable ninth data bit, and a stop bit (1). In fact, Mode 3 is the same as Mode 2 in all respects except the baud rate, which is variable in Mode 3. In all four modes, transmission is initiated by any instruction that uses SBUF as a destination

CHAPTER - 5

CONCLUSION

CONCLUSION

In this project we have made to obtain the conditions for synchronization. The conditions for synchronizations are checked and the parameters are adjusted automatically. until the conditions for synchronization are reached. The motor field voltage and armature voltage are adjusted to control the frequency and alternator terminal voltage .if the conditions are satisfied then they can be synchronized .This project can be further enhanced by making them to synchronize after obtaining the point of synchronization. This can be further enhanced by interfacing with the computer and the monitoring of the parameters such as voltage ,frequency can be done. As a result of this synchronizing can be done easily

CHAPTER – 6

APPENDICES

6.1 APPENDIX I

November 1994

National Semiconductor

LM741 Operational Amplifier

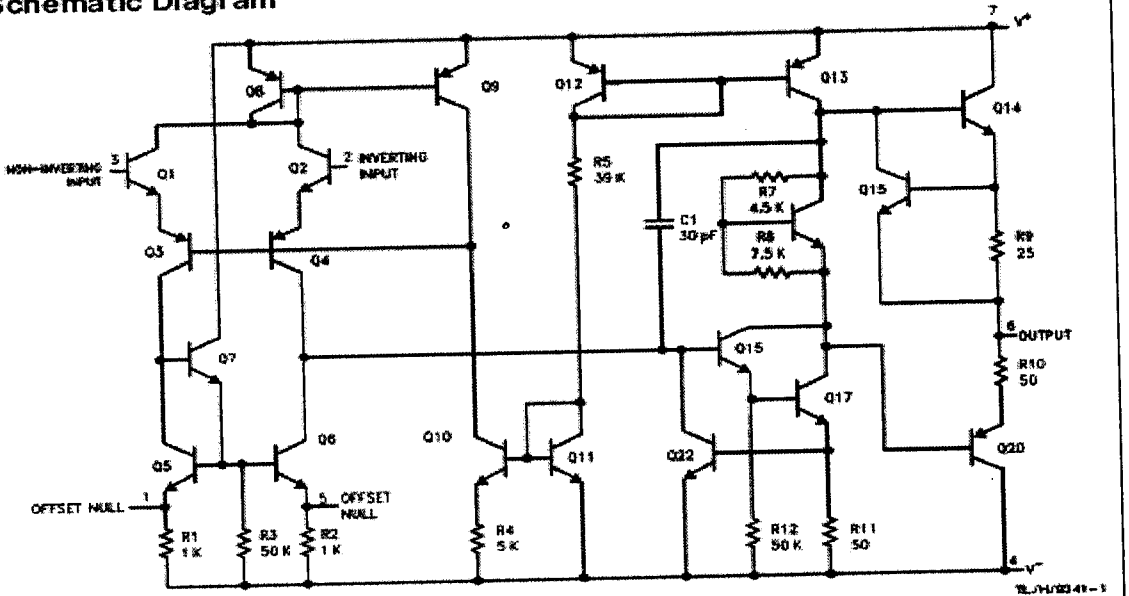
General Description

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

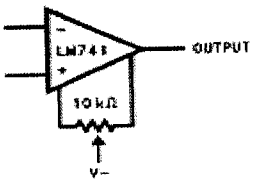
The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

The LM741C/LM741E are identical to the LM741/LM741A except that the LM741C/LM741E have their performance guaranteed over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

Schematic Diagram



Offset Nulling Circuit



TL/H/9341–7

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Note 5)	LM741A	LM741E	LM741	LM741C
Supply Voltage	±22V	±22V	±22V	±18V
Power Dissipation (Note 1)	500 mW	500 mW	500 mW	500 mW
Differential Input Voltage	±30V	±30V	±30V	±30V
Input Voltage (Note 2)	±15V	±15V	±15V	±15V
Output Short Circuit Duration	Continuous	Continuous	Continuous	Continuous
Operating Temperature Range	−55°C to +125°C	0°C to +70°C	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Junction Temperature	150°C	100°C	150°C	100°C
Soldering Information				
N-Package (10 seconds)	260°C	260°C	260°C	260°C
J- or H-Package (10 seconds)	300°C	300°C	300°C	300°C
M-Package				
Vapor Phase (60 seconds)	215°C	215°C	215°C	215°C
Infrared (15 seconds)	215°C	215°C	215°C	215°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 6)	400V	400V	400V	400V

Electrical Characteristics (Note 3)

Parameter	Conditions	LM741A/LM741E			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$ $R_S \le 10k\Omega$ $R_S \le 50\Omega$		0.8	3.0		1.0	5.0		2.0	6.0	mV mV
	$T_{AMIN} \le T_A \le T_{AMAX}$ $R_S \le 50\Omega$ $R_S \le 10k\Omega$			4.0			6.0			7.5	mV mV
Average Input Offset Voltage Drift				15							µV/°C
Input Offset Voltage Adjustment Range	$T_A = 25°C$, $V_S = \pm 20V$	±10				±15			±15		mV
Input Offset Current	$T_A = 25°C$		3.0	30		20	200		20	200	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			70		85	500			300	nA
Average Input Offset Current Drift				0.5							nA/°C
Input Bias Current	$T_A = 25°C$		30	80		80	500		80	500	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			0.210			1.5			0.8	µA
Input Resistance	$T_A = 25°C$, $V_S = \pm 20V$	1.0	6.0		0.3	2.0		0.3	2.0		MΩ
	$T_{AMIN} \le T_A \le T_{AMAX}$, $V_S = \pm 20V$	0.5									MΩ
Input Voltage Range	$T_A = 25°C$							±12	±13		V
	$T_{AMIN} \le T_A \le T_{AMAX}$				±12	±13					V
Large Signal Voltage Gain	$T_A = 25°C$, $R_L \ge 2k\Omega$ $V_S = \pm 20V$, $V_O = \pm 15V$ $V_S = \pm 15V$, $V_O = \pm 10V$	50			50	200		20	200		V/mV V/mV
	$T_{AMIN} \le T_A \le T_{AMAX}$, $R_L \ge 2k\Omega$, $V_S = \pm 20V$, $V_O = \pm 15V$ $V_S = \pm 15V$, $V_O = \pm 10V$ $V_S = \pm 5V$, $V_O = \pm 2V$	32 10			25			15			V/mV V/mV V/mV

Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	LM741A/LM741E			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage Swing	$V_S = \pm 20V$ $R_L \geq 10\ k\Omega$ $R_L \geq 2\ k\Omega$	±16 ±15									V V
	$V_S = \pm 15V$ $R_L \geq 10\ k\Omega$ $R_L \geq 2\ k\Omega$				±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
Output Short Circuit Current	$T_A = 25°C$ $T_{AMIN} \leq T_A \leq T_{AMAX}$	10 10	25	35 40		25			25		mA mA
Common-Mode Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$ $R_S \leq 10\ k\Omega$, $V_{CM} = \pm 12V$ $R_S \leq 50\Omega$, $V_{CM} = \pm 12V$	80	95		70	90		70	90		dB dB
Supply Voltage Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$ $V_S = \pm 20V$ to $V_S = \pm 5V$ $R_S \leq 50\Omega$ $R_S \leq 10\ k\Omega$	86	96		77	96		77	96		dB dB
Transient Response Rise Time Overshoot	$T_A = 25°C$, Unity Gain		0.25 6.0	0.8 20		0.3 5			0.3 5		µs %
Bandwidth (Note 4)	$T_A = 25°C$	0.437	1.5								MHz
Slew Rate	$T_A = 25°C$, Unity Gain	0.3	0.7			0.5			0.5		V/µs
Supply Current	$T_A = 25°C$					1.7	2.8		1.7	2.8	mA
Power Consumption	$T_A = 25°C$ $V_S = \pm 20V$ $V_S = \pm 15V$		80	150		50	85		50	85	mW mW
LM741A	$V_S = \pm 20V$ $T_A = T_{AMIN}$ $T_A = T_{AMAX}$			165 135							mW mW
LM741E	$V_S = \pm 20V$ $T_A = T_{AMIN}$ $T_A = T_{AMAX}$			150 150							mW mW
LM741	$V_S = \pm 15V$ $T_A = T_{AMIN}$ $T_A = T_{AMAX}$					60 45	100 75				mW mW

Note 1: For operation at elevated temperatures, these devices must be derated based on thermal resistance and T_j max. (listed under "Absolute Maximum Ratings"). $T_j = T_A + (\theta_{jA} P_D)$.

Thermal Resistance	Cerdip (J)	DIP (N)	HO8 (H)	SO-8 (M)
θ_{jA} (Junction to Ambient)	100°C/W	100°C/W	170°C/W	195°C/W
θ_{jC} (Junction to Case)	N/A	N/A	25°C/W	N/A

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Unless otherwise specified, these specifications apply for $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to $0°C \leq T_A \leq +70°C$.

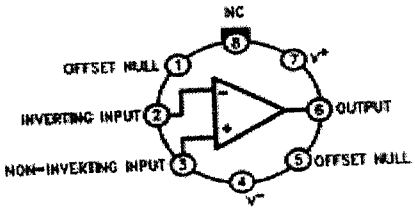
Note 4: Calculated value from: BW (MHz) = 0.35/Rise Time(µs).

Note 5: For military specifications see RETS741X for LM741 and RETS741AX for LM741A.

Note 6: Human body model, 1.5 kΩ in series with 100 pF.

Connection Diagrams

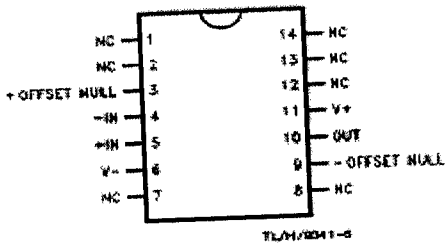
Metal Can Package



TL/H/9341–2

Order Number LM741H, LM741H/883*, LM741AH/883 or LM741CH
See NS Package Number H08C

Ceramic Dual-In-Line Package

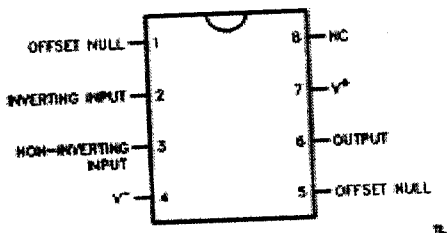


TL/H/9341–6

Order Number LM741J-14/883*, LM741AJ-14/883**
See NS Package Number J14A

*also available per JM38510/10101
**also available per JM38510/10102

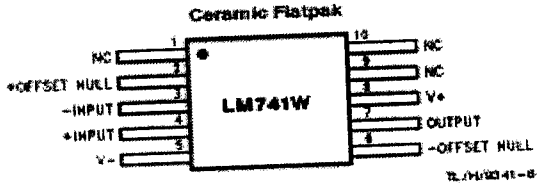
Dual-In-Line or S.O. Package



TL/H/9341–3

Order Number LM741J, LM741J/883, LM741CM, LM741CN or LM741EN
See NS Package Number J08A, M08A or N08E

Ceramic Flatpak



TL/H/9341–8

Order Number LM741W/883
See NS Package Number W10A

*LM741H is available per JM38510/10101

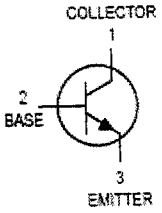
MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Order this document
by BC546/D

Amplifier Transistors

NPN Silicon

BC546, B
BC547, A, B, C
BC548, A, B, C



CASE 29–04, STYLE 17
TO–92 (TO–226AA)

MAXIMUM RATINGS

Rating	Symbol	BC 546	BC 547	BC 548	Unit
Collector–Emitter Voltage	V_{CEO}	65	45	30	Vdc
Collector–Base Voltage	V_{CBO}	80	50	30	Vdc
Emitter–Base Voltage	V_{EBO}	6.0			Vdc
Collector Current — Continuous	I_C	100			mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0			mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12			Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Breakdown Voltage (I_C = 1.0 mA, I_B = 0)	BC546 BC547 BC548	$V_{(BR)CEO}$	65 45 30	— — —	— — —	V
Collector–Base Breakdown Voltage (I_C = 100 µAdc)	BC546 BC547 BC548	$V_{(BR)CBO}$	80 50 30	— — —	— — —	V
Emitter–Base Breakdown Voltage (I_E = 10 µA, I_C = 0)	BC546 BC547 BC548	$V_{(BR)EBO}$	6.0 6.0 6.0	— — —	— — —	V
Collector Cutoff Current (V_{CE} = 70 V, V_{BE} = 0) (V_{CE} = 50 V, V_{BE} = 0) (V_{CE} = 35 V, V_{BE} = 0) (V_{CE} = 30 V, T_A = 125°C)	 BC546 BC547 BC548 BC546/547/548	I_{CES}	 — — — —	 0.2 0.2 0.2 —	 15 15 15 4.0	 nA µA

BC546, B BC547, A, B, C BC548, A, B, C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS						
DC Current Gain		h_{FE}				—
(I_C = 10 μA, V_{CE} = 5.0 V)	BC547A/548A		—	90	—	
	BC546B/547B/548B		—	150	—	
	BC548C		—	270	—	
(I_C = 2.0 mA, V_{CE} = 5.0 V)	BC546		110	—	450	
	BC547		110	—	800	
	BC548		110	—	800	
	BC547A/548A		110	180	220	
	BC546B/547B/548B		200	290	450	
	BC547C/BC548C		420	520	800	
(I_C = 100 mA, V_{CE} = 5.0 V)	BC547A/548A		—	120	—	
	BC546B/547B/548B		—	180	—	
	BC548C		—	300	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$				V
(I_C = 10 mA, I_B = 0.5 mA)			—	0.09	0.25	
(I_C = 100 mA, I_B = 5.0 mA)			—	0.2	0.6	
(I_C = 10 mA, I_B = See Note 1)			—	0.3	0.6	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$	—	0.7	—	V
(I_C = 10 mA, I_B = 0.5 mA)						
Base–Emitter On Voltage		$V_{BE(on)}$				V
(I_C = 2.0 mA, V_{CE} = 5.0 V)			0.55	—	0.7	
(I_C = 10 mA, V_{CE} = 5.0 V)			—	—	0.77	
SMALL–SIGNAL CHARACTERISTICS						
Current–Gain — Bandwidth Product		f_T				MHz
(I_C = 10 mA, V_{CE} = 5.0 V, f = 100 MHz)	BC546		150	300	—	
	BC547		150	300	—	
	BC548		150	300	—	
Output Capacitance		C_{obo}	—	1.7	4.5	pF
(V_{CB} = 10 V, I_C = 0, f = 1.0 MHz)						
Input Capacitance		C_{ibo}	—	10	—	pF
(V_{EB} = 0.5 V, I_C = 0, f = 1.0 MHz)						
Small–Signal Current Gain		h_{fe}				—
(I_C = 2.0 mA, V_{CE} = 5.0 V, f = 1.0 kHz)	BC546		125	—	500	
	BC547/548		125	—	900	
	BC547A/548A		125	220	260	
	BC546B/547B/548B		240	330	500	
	BC547C/548C		450	800	900	
Noise Figure		NF				dB
(I_C = 0.2 mA, V_{CE} = 5.0 V, R_S = 2 kΩ,						
f = 1.0 kHz, Δf = 200 Hz)	BC546		—	2.0	10	
	BC547		—	2.0	10	
	BC548		—	2.0	10	

Note 1: I_B is value for which I_C = 11 mA at V_{CE} = 1.0 V.

FAIRCHILD SEMICONDUCTOR™

October 1987
Revised March 2002

CD4013BC
Dual D-Type Flip-Flop

General Description

The CD4013B dual D-type flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement mode transistors. Each flip-flop has independent data, set, reset, and clock inputs and "Q" and "$\overline{Q}$" outputs. These devices can be used for shift register applications, and by connecting "$\overline{Q}$" output to the data input, for counter and toggle applications. The logic level present at the "D" input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line respectively.

Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{DD} (typ.)
- Low power TTL: fan out of 2 driving 74L
  compatibility: or 1 driving 74LS

Applications

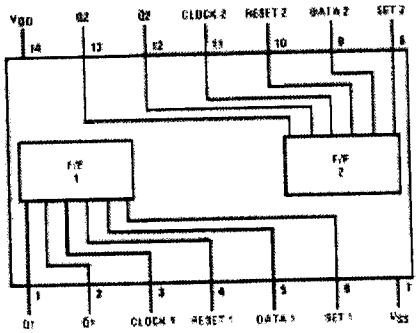
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial electronics
- Remote metering
- Computers

Ordering Code:

Order Number	Package Number	Package Description
CD4013BCM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4013BCSJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4013BCN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



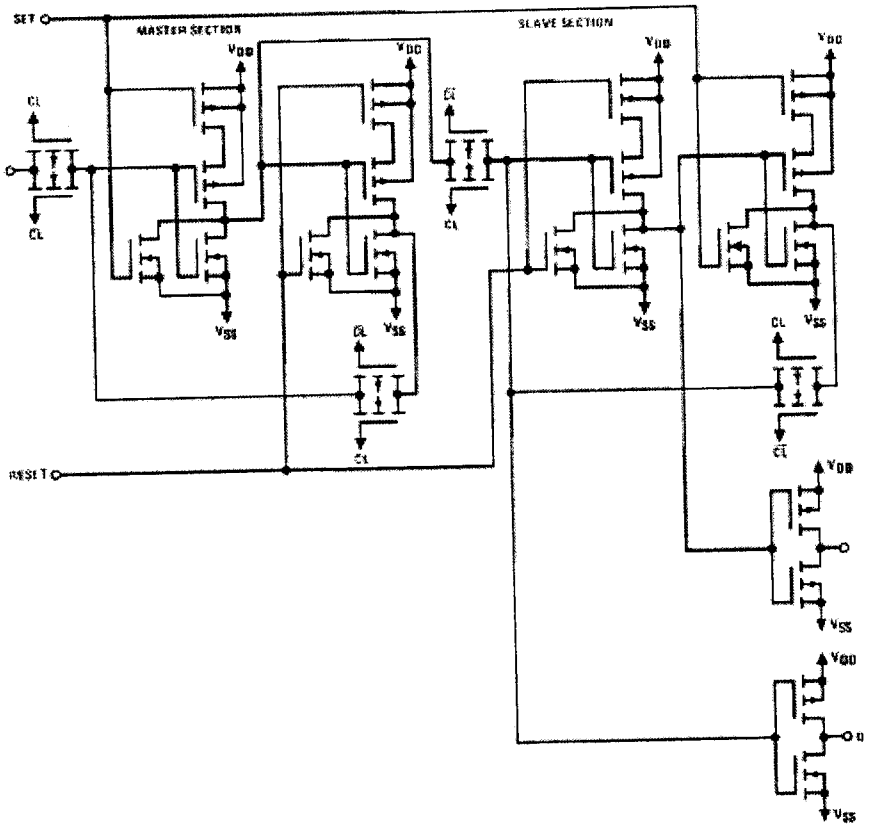
Top View

Truth Table

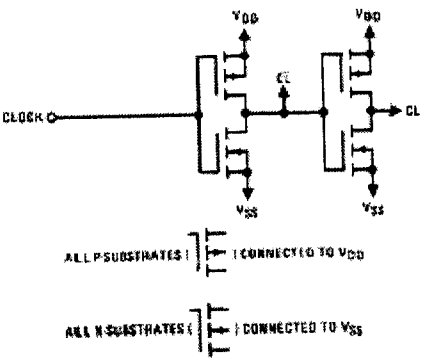
CL (Note 1)	D	R	S	Q	$\overline{Q}$
↓	0	0	0	0	1
↓	1	0	0	1	0
↓	X	0	0	Q	$\overline{Q}$
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

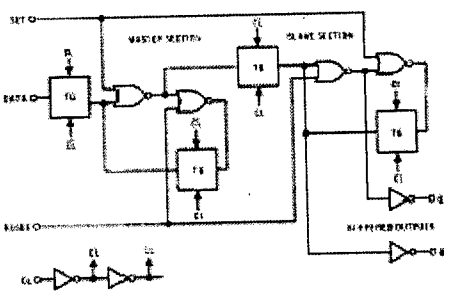
No Change
X = Don't Care Case
Note 1: Level Change

Schematic Diagrams



Logic Diagram





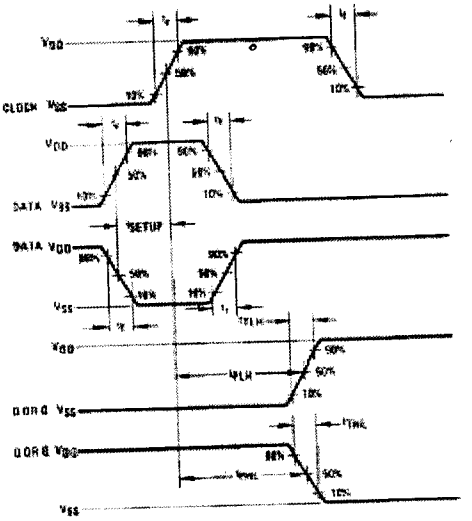
AC Electrical Characteristics (Note 5)

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CLOCK OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		200	350	ns
		$V_{DD} = 10V$		80	160	
		$V_{DD} = 15V$		65	120	
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	
		$V_{DD} = 15V$		40	80	
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		40	80	
		$V_{DD} = 15V$		32	65	
t_{RCL}, t_{FCL}	Maximum Clock Rise and Fall Time	$V_{DD} = 5V$			15	µs
		$V_{DD} = 10V$			10	
		$V_{DD} = 15V$			5	
t_{SU}	Minimum Set-Up Time	$V_{DD} = 5V$		20	40	ns
		$V_{DD} = 10V$		15	30	
		$V_{DD} = 15V$		12	25	
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	2.5	5		MHz
		$V_{DD} = 10V$	6.2	12.5		
		$V_{DD} = 15V$	7.6	15.5		
SET AND RESET OPERATION						
$t_{PHL(R)}$, $t_{PLH(S)}$	Propagation Delay Time	$V_{DD} = 5V$		150	300	ns
		$V_{DD} = 10V$		65	130	
		$V_{DD} = 15V$		45	90	
$t_{WH(R)}$, $t_{WH(S)}$	Minimum Set and Reset Pulse Width	$V_{DD} = 5V$		90	180	ns
		$V_{DD} = 10V$		40	80	
		$V_{DD} = 15V$		25	50	
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF

Note 6: AC Parameters are guaranteed by DC correlated testing.

Switching Time Waveforms



Absolute Maximum Ratings (Note 2)

(Note 3)

DC Supply Voltage (V_{DD})	−0.5 V_{DC} to +18 V_{DC}
Input Voltage (V_{IN})	−0.5 V_{DC} to V_{DD} +0.5 V_{DC}
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 3)

DC Supply Voltage (V_{DD})	+3 V_{DC} to +15 V_{DC}
Input Voltage (V_{IN})	0 V_{DC} to V_{DD} V_{DC}
Operating Temperature Range (T_A)	−55°C to +125°C

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 3: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		1.0			1.0		30	µA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		2.0			2.0		60	
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		4.0			4.0		120	
V_{OL}	LOW Level Output Voltage	|I_O| < 1.0 µA								V
		V_{DD} = 5V		0.05			0.05		0.05	
		V_{DD} = 10V		0.05			0.05		0.05	
		V_{DD} = 15V		0.05			0.05		0.05	
V_{OH}	HIGH Level Output Voltage	|I_O| < 1.0 µA								V
		V_{DD} = 5V	4.95		4.95			4.95		
		V_{DD} = 10V	9.95		9.95			9.95		
		V_{DD} = 15V	14.95		14.95			14.95		
V_{IL}	LOW Level Input Voltage	|I_O| < 1.0 µA								V
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	
V_{IH}	HIGH Level Input Voltage	|I_O| < 1.0 µA								V
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		
I_{OL}	LOW Level Output Current (Note 4)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		
I_{OH}	HIGH Level Output Current (Note 4)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	µA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	

Note 4: I_{OH} and I_{OL} are measured one output at a time.

6.2 APPENDIX II

CODING

```
/thie is the working program for frequency measurement
#include <reg51.h>
#include<math.h>
void htd_ex();
void display1();
void del(unsigned int);
void display();
void adc0();
void adc1();
void delay(unsigned int);
void htd(unsigned int);
void read(unsigned char);
void write(unsigned char);
void lcd_dis(unsigned char *,unsigned char,unsigned char);
void lcd_init();
pdata unsigned char ch0 _at_ 0x08;
pdata unsigned char ch1 _at_ 0x09;
pdata unsigned char soc_dat _at_ 0x10;
pdata unsigned char porta _at_ 0x18;
pdata unsigned char portb _at_ 0x19;
pdata unsigned char portc _at_ 0x1a;
pdata unsigned char cwr  _at_ 0x1b;
unsigned char
```

```
float m,n;
sbit input1=P1^0;
sbit input2=P1^1;
sbit phase1=P1^2;
sbit phase2=P1^3;
sbit phase3=P1^4;
sbit phase4=P1^5;
sbit relay=P1^6;
bit z,y;

 unsigned long tenlk1,onelk1;
 unsigned int k,tenlk,onelk,ten_th,ten_th1,thou,thou1,hund1;

 unsigned long reg1,count,count2,reg2;
 unsigned int k,high;
 unsigned char i,j,low;

main()
{
 relay=0;
 lcd_init();
 read(0x01);
 lcd_dis("SYNCHRONISATION ",16,0x80);
 lcd_dis("OF EB &GENERATOR",16,0xc0);
 delay(65000);
 delay(65000);
```

```
delay(65000);
TMOD=0x11;
EA=1;
ET0=1;
ET1=1;
read(0x01);
lcd_dis("V1:000   V2:000 ",16,0x80);
lcd_dis("DAC:000        ",16,0xc0);
P2=0x90;
dac=0x90;
portb=0x90;
lcd_dis("V1:000   V2:000 ",16,0x80);
lcd_dis("DAC:000        ",16,0xc0);
ag:
 adc0();
 adc1();
 htd(temp1);
 read(0x83);
 display();
 htd(temp2);
 read(0x8C);
 display();
 if(temp1-5>temp2)
 {
  P2=P2+1;
  htd(P2);
```

```
display();
if(P2>=0xbf)  P2=0xbf;
del(65000);
del(65000);
goto ag;
}
else if(temp1+5<temp2)
{
P2=P2-1;
htd(P2);
read(0xC4);
display();
if(P2<=0x80)  P2=0x80;
del(65000);
del(65000);
goto ag;
}
del(65000);
del(65000);
del(65000);
lcd_dis("    VOLTAGE     ",16,0x80);
lcd_dis("SYNCHRONIZATION ",16,0xc0);
del(65000);
del(65000);
lcd_dis("     OVER      ",16,0x80);
lcd_dis("               ",16,0xc0);
```

```
del(65000);
del(65000);
del(65000);
del(65000);
portb=0x90;
lcd_dis("F1:000   F2:000 ",16,0x80);
lcd_dis("DAC:000        ",16,0xc0);
ag1:
 TH0=0x00;
 TL0=0x00;
 while(input1==0);
 while(input1==1);
 while(input1==0);
 TR0=1;
 while(input1==1);
 while(input1==0);
 TR0=0;
 high=TH0;
 low=TH0;
 high=high<<8;
 high=high+low;
 reg1=count;
 reg1=reg1*65535;
 reg1=reg1+high;
 TH0=0x00;
 TL0=0x00;
```

```
htd(reg1);
read(0x83);
display();

htd(dac);
read(0xC4);
display();
del(65000);
TH1=0x00;
TL1=0x00;
while(input2==0);
while(input2==1);
while(input2==0);
TR1=1;
while(input2==1);
while(input2==0);
TR1=0;
high=TH1;
low=TH1;
high=high<<8;
high=high+low;
reg2=count2;
reg2=reg2*65535;
reg2=reg2+high;
TH1=0x00;
```

```
htd(reg2);
read(0x8c);
display();

del(65000);
if(reg1>reg2)
{
 dac=dac+1;
 if(dac>=0xbf)  dac=0xbf;
 htd(dac);
 read(0xC4);
 display();
 portb=dac;
 count=0;
 count2=0;
 goto ag1;
 }
 if(reg1<reg2)
 {
  dac=dac-1;
  if(dac<=0x80)  dac=0x80;
  htd(dac);
  read(0xC4);
  display();
  portb=dac;
```

```
goto ag1;
}
count=0;
count2=0;
del(65000);
del(65000);
lcd_dis("  FREQUENCY   ",16,0x80);
lcd_dis("SYNCHRONIZATION ",16,0xc0);
del(65000);
del(65000);
lcd_dis("    OVER     ",16,0x80);
lcd_dis("             ",16,0xc0);
del(65000);
del(65000);
del(65000);
del(65000);
ph:
lcd_dis("    PHASE     ",16,0x80);
lcd_dis("SYNCHRONIZATION ",16,0xc0);
if(phase1==0 && phase2==0 && phase3==0 && phase4==0)  relay=1;
else
{
relay=0;
goto ph;
}
```

```
del(65000);
del(65000);
lcd_dis("     OVER     ",16,0x80);
lcd_dis("              ",16,0xc0);
del(65000);
del(65000);
del(65000);
read(0x01);
lcd_dis("SYNCHRONISATION ",16,0x80);
lcd_dis("OF EB &GENERATOR",16,0xc0);
while(1);
}
void timer0(void) interrupt 1
{
TR0=0;
count++;
TR0=1;
}
void timer1(void) interrupt 3
{
TR1=0;
count2++;
TR1=1;
}
void htd(unsigned int hex_val)
```

```
hund_r=hex_val%100;
ten=hund_r/10;
one=hund_r%10;
}
void delay(unsigned int b)// the only delay routine, which is user variable &
is decided by the values given in the brackets
{
 do b-=1;
 while (b!=0);
 }
 void del(unsigned int num)
 {
  while(num--);
  }
  void lcd_init()
  {
   cwr=0x80;
   read(0x38);
   read(0x06);
   read(0x0c);
   }
   void read(unsigned char y)
   {
    porta=y;
    portc=0x04;
```

```
delay(125);
}
void write(unsigned char y)
{
 porta=y;
 portc=0x05;
 delay(125);
 portc=0x01;
 delay(125);
 }
 void lcd_dis(unsigned char *dis,unsigned char rr,unsigned char lcd)
 {
  unsigned char w;
  read(lcd);
  for (w=0;w<rr;w++) {write(dis[w]);}
  }
  void adc0()
  {
   x=ch0;
   delay(255);
   temp1=soc_dat;
   }
   void adc1()
   {
    x=ch1;
```

```
}
void display()
{
 write(hund+0x30);
 write(ten+0x30);
 write(one+0x30);
 }
 void htd_ex()
 {
                        tenlk=reg1/1000000;
                        tenlk1=reg1%1000000;
                        onelk=tenlk1/100000;
                        onelk1=tenlk1%100000;
                        ten_th=onelk1/10000;
                        ten_th1=onelk1%10000;
                        thou=ten_th1/1000;
                        thou1=ten_th1%1000;
                        hund=thou1/100;
                        hund1=thou1%100;
                        ten=hund1/10;
                        one=hund1%10;
   }
   void display1()
    {
                         read(0xc0);
                         write(tenlk+0x30);
```

```
write(ten_th+0x30);
write(thou+0x30);
write(hund+0x30);
write(ten+0x30);
write(one+0x30);
}
```

CHAPTER – 7

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