AUTOMATIC TRACKING SYSTEM FOR SOLAR PANEL

A PROJECT REPORT

Submitted by

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in partial fulfillment for the award of the degree

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in

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Under the guidance of
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BONAFIDE CERTIFICATE

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Branch : **Electrical & Electronics Engineering**

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(INTERNAL EXAMINER)

(EXTERNAL EXAMINER)

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ABSTRACT

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The nature is ready to relieve its underlying secrets provided, the proper keys are used for the respective locks. Sun, the ultimate source of energy, from the beginning of mankind still serves as a key for solving the problem of energy crisis. The solar energy which if properly utilized, can serve as a huge reservoir of energy.

The solar panels that are available in the market at present are static and hence the maximum energy can be tapped only at noon that is the time at which the panel and the sun are perpendicular. The project "AUTOMATIC TRACKING SYSTEM FOR SOLAR PANEL" aims to utilise solar energy to the maximum extend. The solar tracking system that we have created using micro controller is automatic in its movement with respect to suns rays. The LDR that are mounted on the panel at both ends act as a potential divider and performs the conversion of light into appropriate voltage signals, which aids the automatic movement of panel.

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CHAPTER 1: INTRODUCTION

INTRODUCTION

OBJECTIVE :

To design and implement an automatic tracking system so as to tap solar energy efficiently.

1.1 INTRODUCTION TO SOLAR POWER :

The sun is the most prominent feature in our solar system. It is the largest object and contains approximately 98% of the total solar system mass. The sun's outer visible layer is called the photosphere and has a temperature of 6,000°C (11,000°F).

Solar energy is created deep within the core of the sun. It is here that the temperature (15,000,000°C; 27,000,000°F) and pressure (340 billion times Earth's air pressure at sea level) is so intense that nuclear reactions take place. Energy generated in the sun's core takes a million years to reach its surface. Every second 700 million tones of hydrogen are converted into helium ashes. The sun appears to have been active for 4.6 billion years and has enough fuel to go on for another 5 billion years or so. At the end of its life, the sun will start to fuse helium into heavier elements and begin to swell up; ultimately growing so large that it will swallow the Earth.

1.2 EXISTING MODEL:

The existing model used to tap solar energy is an open loop system. The amount of voltage obtained by this system is substantially less during mornings and evenings when compared to the voltage obtained at noons. Hence the efficiency of this system is low for the major part of the day.

An innovation to this system was made using GPS (Global Positioning System) technology. A GPS system receives data from a satellite and accordingly positions the system towards the sun. Even though the efficiency of this system is very high, the cost of the system proved to be a constraint among large numbers.

1.3 AUTOMATIC TRACKING SYSTEM:

Solar energy being the natural source of energy has to be utilized efficiently. So tracking system has to be employed. The main disadvantage with the GPS system is that it is very costly. To overcome that difficulty we have employed tracking using sensing circuits. In this project the intensities of the sun's radiation is sensed and according to that signals are passed to the driver circuitry which controls the solar panels rotation. As a result efficient and perfect tracking is obtained.

1.4 ORGANISATION OF THE THESIS:

The thesis is organized in such a way to provide a clear picture of our project "AUTOMATIC TRACKING SYSTEM FOR SOLAR PANEL". The explanation of the thesis begins with the solar energy generation and its usage explained in chapter 1 followed by chapter 2 which gives a detailed explanation on various system components used. The detailed hardware configurations are explained in chapter 3.The algorithm and working is explained in chapter 4 followed by a comparative study and results in chapter 5.

CHAPTER 2 : SYSTEM COMPONENTS

CHAPTER 2
SYSTEM COMPONENTS

2.1 INTRODUCTION:

Automatic tracking system for solar panel consists of components like voltage regulators, Control circuitry, sensing circuitry, driver circuitry and a storage device for storing electricity produced from the panel. Control circuitry is the main part of the system with which proper control signals are sent according to which the panel tracks. Control circuitry consists of the following components. They are

1. Micro controllers – For programming purpose.
2. ADC – For converting the analog Voltage input to a digital Value
3. Programmable peripheral interface – For interfacing the output To display unit (LCD).

Sensing circuitry is used to sense the position of the panel and gives signals to the control circuitry. They are

1. LDRs - Placed at both the ends of the panel which Senses the sun light. The resistance of LDR Decreases with increase in sunlight.
2. Micro switches - These switches are used as keys. These are Used as limits beyond which the panel can't rotate or move.

For tracking the suns path the panel has to rotate. This is possible with the help of driver circuitry. This has

1. Relay - Used to give supply to the DC motor based on the Signals from the microcontroller that is either to make the motor to rotate forward or reverse
2. DC motor - The DC motor used is in this project is of permanent Magnet type. The panel requires low RPM which is Obtained by gear reduction method. The holding Torque for DC motor is higher than Stepper motor.

2.2 BLOCK DIAGRAM:

The basic block diagram is given below

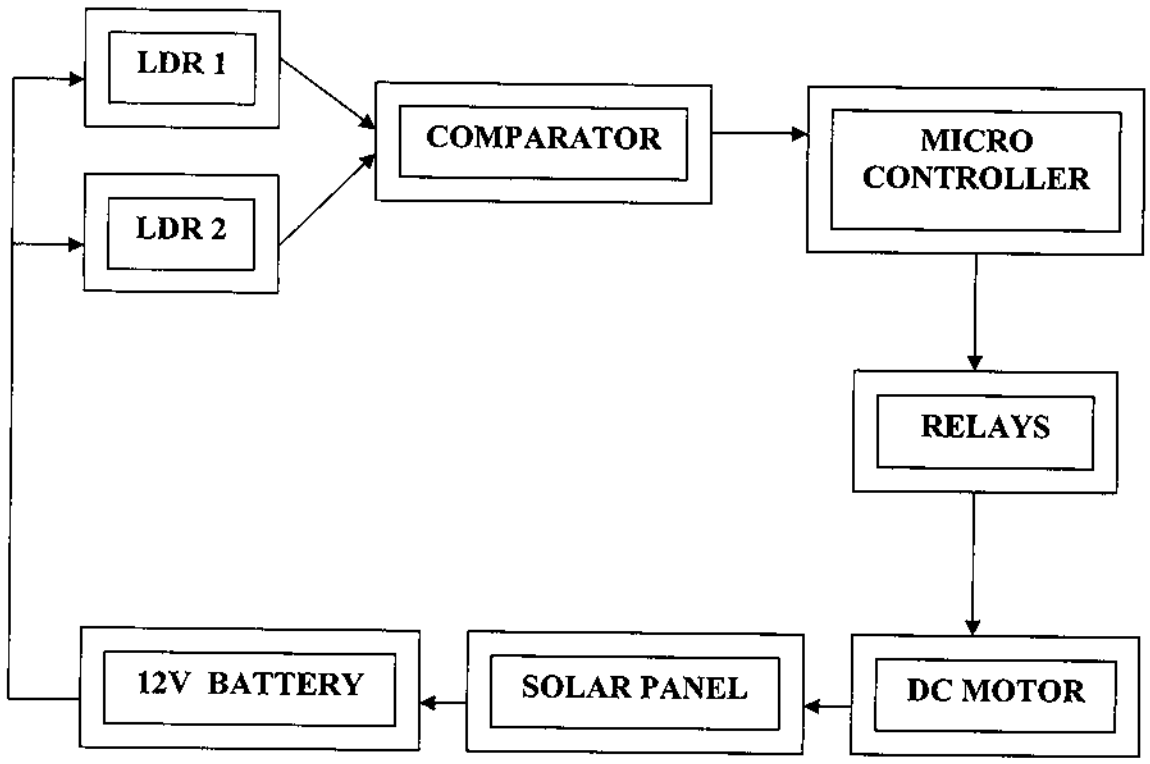
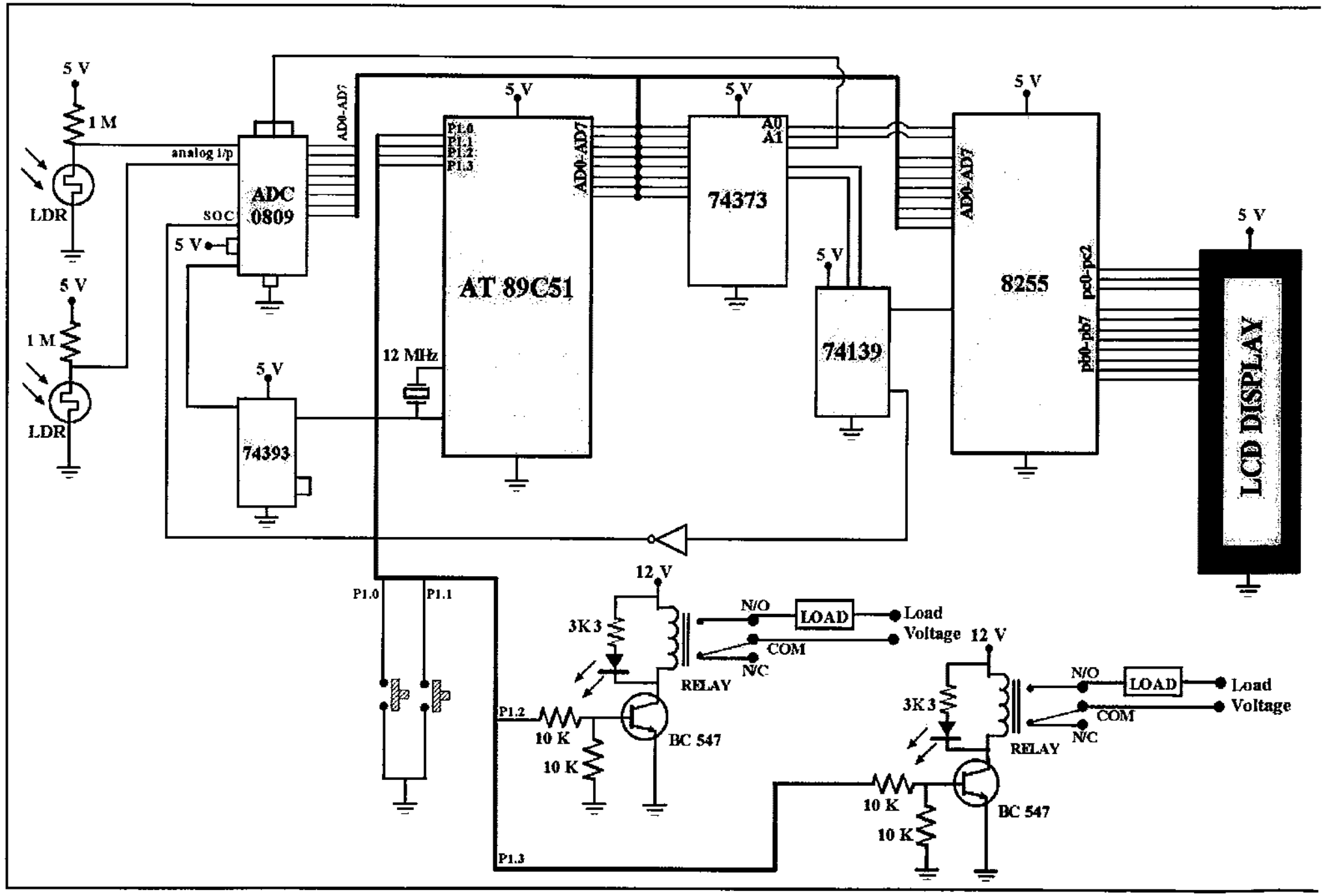


Fig 2.2 Block diagram of automatic solar tracking system

SEQUENCE OF OPERATION:

The LDR placed at both ends of the solar panel detects the intensities of light at both the ends. The two different values of intensities are then fed to the comparator for comparison. This value is then given to a micro controller which in turn decides the direction of rotation of motor. The rotation of panel is done with the help of a driver circuit. The output of the panel is stored with the help of a battery. The power from the battery is used as supply to the various components in the hardware circuit.


5 V
1 M
LDR
analog i/p
ADC 0809
SOC
AD0-AD7
AT 89C51
P1.0
P1.1
P1.2
P1.3
12 MHz
74373
A0
A1
74139
74393
8255
pa0-pa7
pb0-pb7
pc0-pc2
LCD DISPLAY
12 V
3K3
RELAY
N/O
COM
N/C
LOAD
Load
Voltage
10 K
BC 547

CHAPTER 3: HARDWARE IMPLEMENTATION

CHAPTER 3
HARDWARE IMPLEMENTATION

3.1 IC VOLTAGE REGULATORS:

Voltage regulators comprise a class of widely used ICs. Regulator IC units contain the circuitry for reference source, comparator amplifier, control device, and overload protection all in a single IC. Although the internal construction of the IC is somewhat different from that described for discrete voltage regulator circuits, the external operation is much the same. IC units provide regulation of either a fixed positive voltage, a fixed negative voltage, or an adjustably set voltage.

A power supply can be built using a transformer connected to the ac supply line to step the ac voltage to desired amplitude, then rectifying that ac voltage, filtering with a capacitor and RC filter, if desired, and finally regulating the dc voltage using an IC regulator. The regulators can be selected for operation with load currents from hundreds of milli amperes to tens of amperes, corresponding to power ratings from milli watts to tens of watts.

3.2 SENSING CIRCUIT:

Sensing circuits mainly consists of two components .They is

1. Micro switches.
2. LDR (Light Dependent Resistor)

3.2.1 LDR :

The LDR placed at both the ends of the solar panel is used to detect the different intensities of light at either ends of the solar panel, one to sense

the intensity of light in the east direction and the other in the west direction. The internal working of the LDR is given below.

The LDR light dependent resistor is varying resistance with light intensity. This will be mostly linear to the light intensity. During the darkness the resistance of LDR shoots up to Mega ohm ranges. When LDR is illuminated by means of the sunlight, the resistance of LDR suddenly decreases (below 10 kilo ohm).

The resistance is converted into differential voltage, then the voltage is amplified and given to the comparator. The comparator compares the light intensity with the required level and it will produce output depends on the intensity.

3.2.2 MICRO SWITCHES :

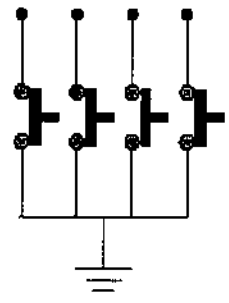


Fig 3.2.2 Micro Switches

Micro switches are placed at either ends of housing which consists of the motor and the solar panel. These switches help to limit the movement of the solar panel. The switch is normally in the OFF state. As the panel touches the limit switch, the limit switch goes to ON state and simultaneously a signal is generated at the ports of the micro controller.

3.3 CONTROL UNIT :

Control unit is the most important part of any hardware circuitry. This mainly consists of the following. They are

1. Analog to Digital converter,
2. Microcontroller,
3. Programmable Peripheral Interface,
4. Decoder and
5. Latch.

The whole control circuitry is shown below.

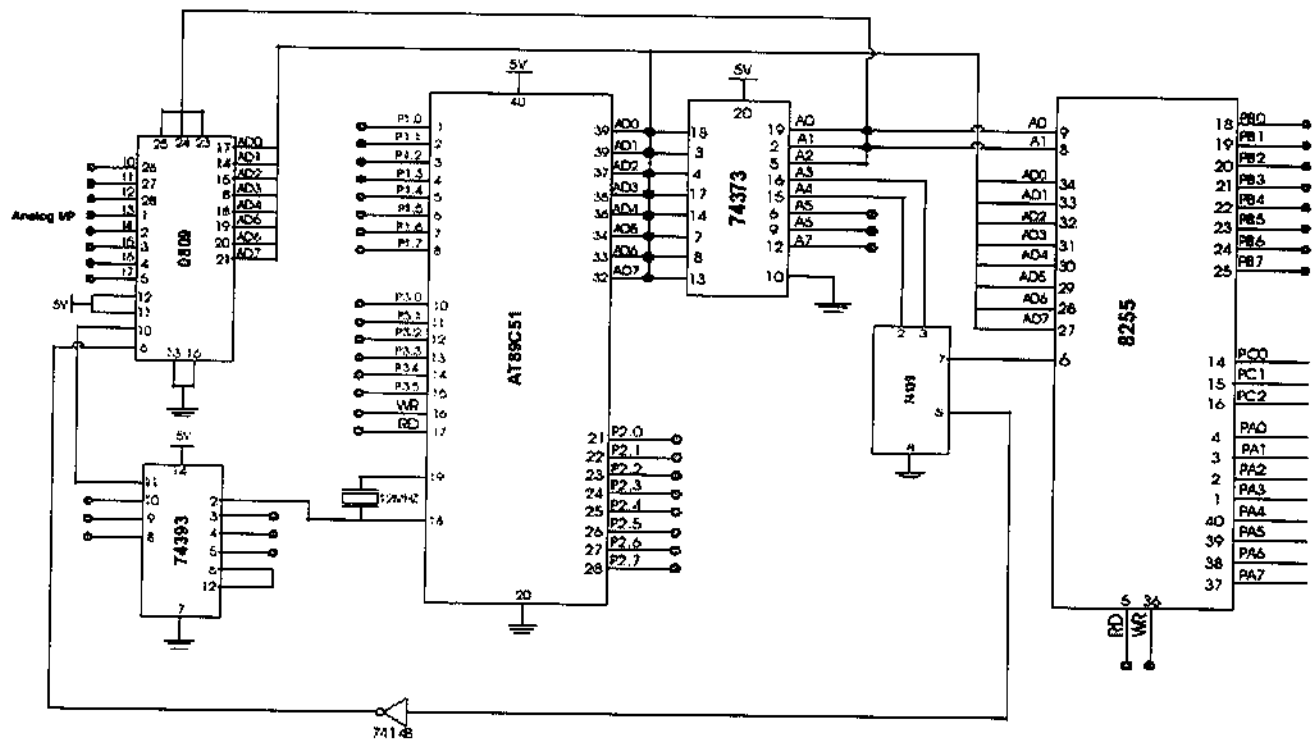


Fig 3.3 Control Circuitry

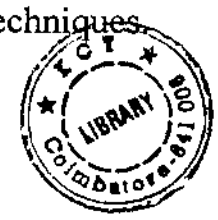
3.3.1 ANALOG TO DIGITAL CONVERTER :

In our project, the two LDR' s which are placed at both ends of the solar panel detects the intensities of light and are converted to equivalent digital signals before it is given to a micro controller for further processing. The method of conversion of the voltage signal from analog to digital is explained below.

The ADC 0809 has an eight bit resolution. It works with a supply voltage of 5V and has a conversion time of about 100 micro seconds. It operates at a wide range of clock frequencies (10Khz - 1280Khz) and temperatures.

The ADC 0808/0809 is an 8-bit analog to digital converter with 8-channel inbuilt Multiplexer. It is the monolithic CMOS device manufactured by the National semiconductors. It uses the principle of successive approximation technique for the conversion process. The 8-channel Multiplexer can directly access any of the 8-single-ended analog signals. The converter features a high impedance chopper stabilized capacitor and a successive approximation register (SAR) . It is free from external zero and full-scale adjustments. Easy interfacing to microprocessors or micro controllers are provided by the latched and decoded multiplexes address inputs and latched TTL TIR-STATE outputs. The design of the ADC 0808/0809 has been optimized by incorporating the most desirable aspects of several ADC techniques.

The 0808/0809 ADC offers following advantages.



- High speed,
- High accuracy
- Minimal temperature dependence
- Excellent long term accuracy and repeatability
- Consume minimal power

The heart of this ADC is the successive approximation register (SAR). On receipt of the 1st CLK at start of the SC cycle, the SAR outputs a high on its MSB. The DAC and the amplifier convert this to an analog voltage and apply to one of the inputs of the comparator, the comparator will go low to indicate to the SAR to turn OFF that bit because it is too large. If the output voltage from DAC is less than he input voltage, the comparator output will be high to indicate to the SAR to keep that bit ON. On receipt of the next pulse, the SAR will turn ON the next MSB to DAC. Based on the answer, it produces from the comparator; the SAR will keep or RESET the bit. The SAR proceeds in this manner down to the LSB, adding each bit to the total in turn and using the signal from the comparator to decide whether to keep that bit in the result or not. Only 8-CLK pulses are needed to do the actual conversion signal to indicate the completion of the process. The EOC signal is used to strobe the binary result into some latches where it can be read by a microcomputer.

SAMPLE & HOLD CIRCUIT:

This ADC 0808/0809 does not contain the sample-and-hold circuit. If a sample-and-hold circuit is required, it could be connected before the multiplexes. The pin configuration of the ADC 0808/0809 where as the figure is its timing diagram. The input states for the address lines to select any particular channel. The address latched into the decoder on the low-to-high transition of the address latch enable signal.

NEED FOR SAMPLE AND HOLD CIRCUIT :

As discussed, the ADC takes finite time, called the conversion time, to give a digital output to corresponding analog input value. If the analog input signals are not stable during conversion time, the digital output will not be the true representation of its analog value. This may lead to error

in digital converted data. This error will be some function of the highest frequency and uncertainty in time. In order to overcome this problem, the sample and hold (S/H) circuit is used. This increases the system band width (BW) without change in the accuracy.

The sample and hold circuit has two modes;

Sample mode

Hold mode

In the sample mode, the output follows the input with unity gain. Whereas in the hold mode, it retains the last value of the sample when the switch was opened.

The basic sample and hold circuit consists of a switch and a capacitor. When the switch is closed, the capacitor is charged to the instantaneous value of the input signal voltage and when it is opened, it holds the voltage. This process of charging and holding the voltage assumes very high value of load impedance. If the load impedance is not high, then the charge on the capacitor will, start leaking through the low value of the load impedance and the held voltage will never be constant.

The ideal waveform of the simplest sample and hold circuit. If the time constant RC is very small, the capacitor C will be charged to the sample value very rapidly. Hence during the sample interval, the sample voltage very closely follows the input voltage and during the hold interval, the capacitor holds the sampled value. There are many types of deviations from the ideal situation. The important specifications worth mentioning for the selection of switches are

Aperture time; and

Acquisition Time.

3.3.2 MICROCONTROLLER :

The digitalized signals from the ADC is fed to port 0 (pin 39 - pin 32). The output is taken through port 1 (P1.2 - P1.3) and given to the driver circuit. The two digitalized signals are compared with each other in order to decide the direction of rotation of solar panel. A tolerance value of +5 (0000 0101) or -5 (1111 1011) is maintained. The differential digitalized voltage is then calculated and compared with the tolerance value. If the differential value is greater than the tolerance value then a signal is generated at the output port which activates the relay and in turn drives the motor and the panel. If the differential digitalized value is lesser than or equal to the tolerance value, no signal is generated and hence motor will not rotate. Port 1.0 and Port 1.1 are connected to two limit switches. The sun rises in the east and sets in the west. After sunset, the panel is supposed to come to the east direction in order to perform tracking for the next day. Hence the micro controller is programmed in such a way that once the panel touches the limit switch in the west direction, it returns to the east direction without tracking. The internal working of micro controller is explained below.

A Micro controller consists of a powerful CPU tightly coupled with memory RAM, ROM or EPROM), various I / O features such as Serial ports, Parallel Ports, Timer/Counters, Interrupt Controller, Data Acquisition interfaces-Analog to Digital Converter (ADC), Digital to Analog Converter (DAC), everything integrated onto a single Silicon Chip.

Any microcomputer system requires memory to store a sequence of instructions making up a program, parallel port or serial port for communicating with an external system, timer / counter for control purposes like generating time delays, Baud rate for the serial port, apart from the controlling unit called the **Central Processing Unit.**

ADVANTAGES OF MICROCONTROLLERS:

1. If a system is developed with a microprocessor, the designer has to go for external memory such as RAM, ROM or EPROM and peripherals and hence the size of the PCB will be large enough to hold all the required peripherals. But, the micro controller has got all these peripheral facilities on a single chip so development of a similar system with a micro controller reduces PCB size and cost of the design.

One of the major differences between a micro controller and a microprocessor is that a controller often deals with bits , not bytes as in the real world application, for example switch contacts can only be open or close , indicators should be lit or dark and motors can be either turned on or off and so forth.

FEATURES OF AT89C51

SERIES: 89C51 Family

TECHNOLOGY: CMOS

The major Features of 8-bit Micro controller **ATMEL 89C51**

- 8 Bit CPU optimized for control applications
- Extensive Boolean processing (Single - bit Logic) Capabilities.
- On - Chip Flash Program Memory
- On - Chip Data RAM
- Bi-directional and Individually Addressable I/O Lines
- Multiple 16-Bit Timer/Counters
- Full Duplex UART
- Multiple Source / Vector / Priority Interrupt Structure
- On - Chip Oscillator and Clock circuitry.

- On - Chip EEPROM
- SPI Serial Bus Interface
- Watch Dog Timer

POWER MODES OF ATMEL 89C51 MICROCONTROLLER:

To exploit the power savings available in CMOS circuitry. Atmel 's Flash micro controllers have two software-invited reduced power modes. They are,

IDLE MODE:

The CPU is turned off while the RAM and other on - chip peripherals continue operating. Inn this mode current draw is reduced to about 15 percent of the current drawn when the device is fully active.

POWER DOWN MODE:

All on-chip activities are suspended while the on – chip RAM continues to hold its data. In this mode, the device typically draws less than 15 Micro Amps and can be as low as 0.6 Micro Amps

POWER ON RESET:

When power is turned on, the circuit holds the RST pin high for an amount of time that depends on the capacitor value and the rate at which it charges.

To ensure a valid reset, the RST pin must be held high long enough to allow the oscillator to start up plus two machine cycles. On power up, Vcc should rise within approximately 10ms. The oscillator start-up time depends on the oscillator frequency. For a 10 MHz crystal, the start-up time is typically 1ms.With the given circuit, reducing Vcc quickly to 0

causes the RST pin voltage to momentarily fall below 0V. However, this voltage is internally limited and will not harm the device.

MEMORY ORGANISATION

FLASH ROM:

4-kilo byte ROM is available in the Micro controller. It can be erased and reprogrammed. If the available memory is not enough for your program, you can interface the external ROM with this IC, it has 16 address lines, so maximum of (2^16) i.e. 64 bytes of ROM can be interfaced with this Micro controller. Both internal and external ROM cannot be used simultaneously.

For external accessing of ROM, A pin is provided in Micro controller itself is i.e. pin no.31 EA should be high to use internal ROM, low to use external ROM

RAM:

Internal 256 bytes of RAM are available for user. These 256 bytes of RAM can be used along with the external RAM. Externally you can connect 64-kilo bytes of RAM with micro controller. In internal RAM first 128 bytes of RAM is available for user and the remaining 128 bytes are used as special function registers (SFR). These SFR's are used as control registers for timer, serial port etc.

INPUT/ OUTPUT PORTS:

There are four I/O ports available in AT89C51. They are port 0, port 1, port 2, and port 3. All these ports are eight bit ports. All these ports can be controlled as eight-bit port or it can be controlled individually. One of the main feature of this micro controller is it can control the port pins individually. In 89C51 port 1 is available for users Port 3 is combined

with interrupts. This can be used as interrupts (or) I/O ports, ports 2 & port 0 is combined with address bus & data bus. This Micro controller is working in a speed of maximum of 24MHz. Program memory can only be read. There can be up to 64K bytes of directly addressable program memory. The read strobe for external program memory is the Program Store Enable Signal (PSEN) Data memory occupies a separate address space from program memory. Up to 64K bytes of external memory can be directly addressed in the external data memory space. The CPU generates read and write signals, RD and WR, during external data memory accesses. External program memory and external data memory can be combined by a applying the RD and PSEN signals to the inputs of AND gate and using the output of the fate as the read strobe to the external program/data memory.

All these port lines are available with internal pull-ups except port 0. If we want to use port 0 as I/O port we have to use pull up resistors.

This Micro controller is working in a speed of maximum of 24MHz. This micro controller is available with inbuilt oscillator; just we have to connect the crystal to its terminal.

All Atmel Flash micro controllers have separate address spaces for program and data memory. The logical separation of program and data memory allows the data memory to be accessed by 8 bit addresses . Which can be more quickly stored and manipulated by an 8 bit CPU Nevertheless 16 Bit data memory addresses can also be generated through the DPTR register.

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PROGRAM MEMORY:

Fig 3.3.2 shows the map of the lower part of the program memory, after reset, the CPU begins execution from location 0000h. As shown in Fig each interrupt is assigned a fixed location in program memory. The interrupt causes the CPU to jump to that location, where it executes the service routine. External Interrupt 0 for example, is assigned to location 0003h.

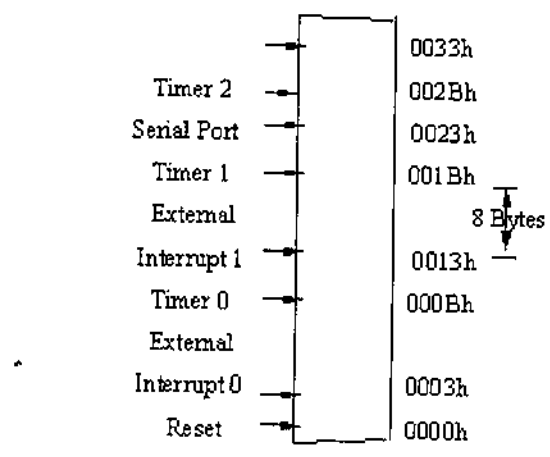


Fig 3.3.2 Program memory

If external Interrupt 0 is used, its service routine must begin at location 0003h. The interrupt service locations are spaced at 8 byte intervals 0003h for External interrupt 0, 000Bh for Timer 0, 0013h for External interrupt 1,001Bh for Timer1, and so on. If an Interrupt service routine is short enough (as is often the case in control applications) it can reside entirely within that 8-byte interval. Longer service routines can use a jump instruction to skip over subsequent interrupt locations. If other

interrupts are in use. The lowest addresses of program memory can be either in the on-chip Flash or in an external memory. To make this selection, strap the External Access (EA) pin to either Vcc or GND. For example, in the AT89C51 with 4K bytes of on-chip Flash, if the EA pin is strapped to Vcc, program fetches to addresses 0000h through 0FFFh are directed to internal Flash. Program fetches to addresses 1000h through FFFFh are directed to external memory.

DATA MEMORY:

The Internal Data memory is dived into three blocks namely,

- The lower 128 Bytes of Internal RAM.
- The Upper 128 Bytes of Internal RAM.
- Special Function Register.

Internal Data memory Addresses are always 1 byte wide, which implies an address space of only 256 bytes. However, the addressing modes for internal RAM can in fact accommodate 384 bytes. Direct addresses higher than 7Fh access one memory space, and indirect addresses higher than 7Fh access a different Memory Space.

The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word (PSW) Select, which register bank, is in use. This architecture allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

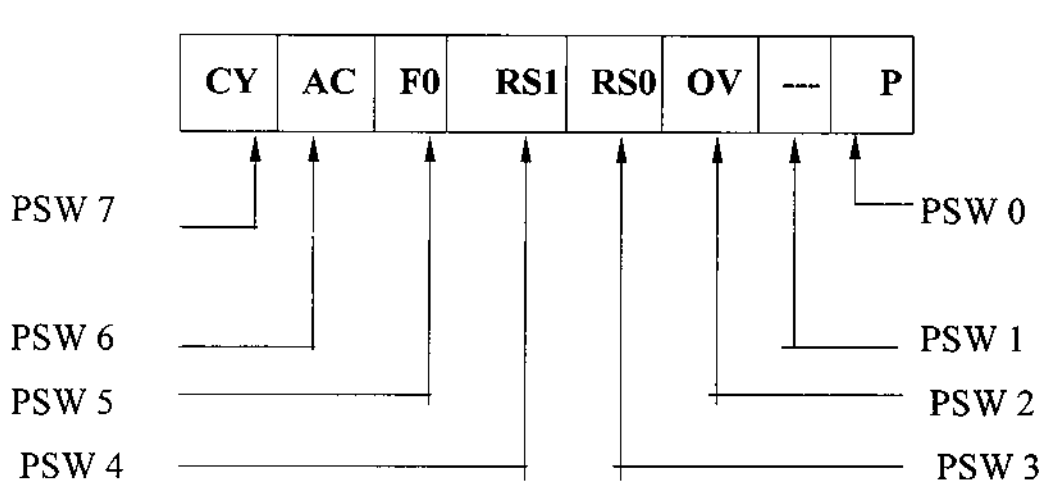
The next 16-bytes above the register banks form a block of bit addressable memory space. The micro controller instruction set includes a wide selection of single - bit instructions and this instruction can directly address the 128 bytes in this area. These bit addresses are 00h through 7Fh. either direct or indirect addressing can access all of the bytes in

lower 128 bytes. Indirect addressing can only access the upper 128. The upper 128 bytes of RAM are only in the devices with 256 bytes of RAM. The Special Function Register includes Ports latches, timers, peripheral controls etc., direct addressing can only access these register. In general, all Atmel micro controllers have the same SFR's at the same addresses in SFR space as the

AT89C51 and other compatible micro controllers. However, upgrades to the AT89C51 have additional SFR's. Sixteen addresses in SFR space are both byte and bit Addressable. The bit Addressable SFR's are those whose address ends in 000B. The bit addresses in this area are 80h through FFh.

PROGRAM STATUS WORD:

Program Status Word Register in Atmel Flash Micro controller:



PSW 0:

Parity of Accumulator Set By Hardware To 1 if it contains an Odd number of 1s, Otherwise it is reset to 0.

PSW1:

User Definable Flag

PSW2:

Overflow Flag Set By Arithmetic Operations

PSW3:

Register Bank Select

PSW4:

Register Bank Select

PSW5:

General Purpose Flag.

PSW6:

Auxiliary Carry Flag Receives Carry Out from

Bit 1 of Addition Operands

PSW7:

Carry Flag Receives Carry Out From Bit 1 of ALU Operands.

The Program Status Word contains Status bits that reflect the current state of the CPU. The PSW shown if Fig resides in SFR space. The PSW contains the Carry Bit, The auxiliary Carry (For BCD Operations) the two - register bank select bits, the Overflow flag, a Parity bit and two user Definable status Flags.

The Carry Bit, in addition to serving as a Carry bit in arithmetic operations also serves the as the "Accumulator" for a number of Boolean Operations .The bits RS0 and RS1 select one of the four register banks. A number of instructions register to these RAM locations as R0 through R7.The status of the RS0 and RS1 bits at execution time determines which of the four banks is selected.

The Parity bit reflect the Number of 1s in the Accumulator .P=1 if the Accumulator contains an even number of 1s, and P=0 if the Accumulator contains an even number of 1s. Thus, the number of 1s in the

Accumulator plus P is always even. Two bits in the PSW are uncommitted and can be used as general-purpose status flags.

INTERRUPTS :

The AT89C51 provides 5 interrupt sources:

Two External interrupts, two-timer interrupts and a serial port interrupts. The External Interrupts INT0 and INT1 can each either level activated or transition - activated, depending on bits IT0 and IT1 in Register TCON. The Flags that actually generate these interrupts are the IE0 and IE1 bits in TCON. When the service routine is vectored to hardware clears the flag that generated an external interrupt only if the interrupt WA transition - activated. If the interrupt was level - activated, then the external requesting source (rather than the on-chip hardware) controls the requested flag.

Tf0 and Tf1 generate the Timer 0 and Timer 1 Interrupts, which are set by a rollover in their respective Timer/Counter Register (except for Timer 0 in Mode 3). When a timer interrupt is generated, the on-chip hardware clears the flag that generated it when the service routine is vectored to. The logical OR of RI and TI generate the Serial Port Interrupt. Neither of these flag is cleared by hardware when the service routine is vectored to. In fact, the service routine normally must determine whether RI or TI generated the interrupt and the bit must be cleared in software.

In the Serial Port Interrupt is generated by the logical OR of RI and TI. Neither of these flag is cleared by hardware when the service routine is vectored to. In fact, the service routine normally must determine whether RI to TI generated the interrupt and the bit must be cleared in software.

IE: Interrupt Enable Register

EA	-	ET2	ES	ET1	EX1	ET0	EX0

Enable bit = 1 enabled the interrupt

Enable bit = 0 disables it.

OSCILLATOR AND CLOCK CIRCUIT:

XTAL1 and XTAL2 are the input and output respectively of an inverting amplifier which is intended for use as a crystal oscillator in the pierce configuration, in the frequency range of 1.2 MHz to 12 MHz. XTAL2 also the input to the internal clock generator.

To drive the chip with an internal oscillator, one would ground XTAL1 and XTAL2. Since the input to the clock generator is divide by two flip flops there are no requirements on the duty cycle of the external oscillator signal. However, minimum high and low times must be observed.

The clock generator divides the oscillator frequency by 2 and provides a tow phase clock signal to the chip. The phase 1 signal is active during the first half to each clock period and the phase 2 signals are active during the second half of each clock period.

CPU TIMING:

A machine cycle consists of 6 states. Each stare is divided into a phase / half, during which the phase 1 clock is active and phase 2 half. Arithmetic and Logical operations take place during phase1 and internal register - to register transfer take place during phase 2.

3.3.3 PROGRAMMABLE PERIPHERAL INTERFACE :

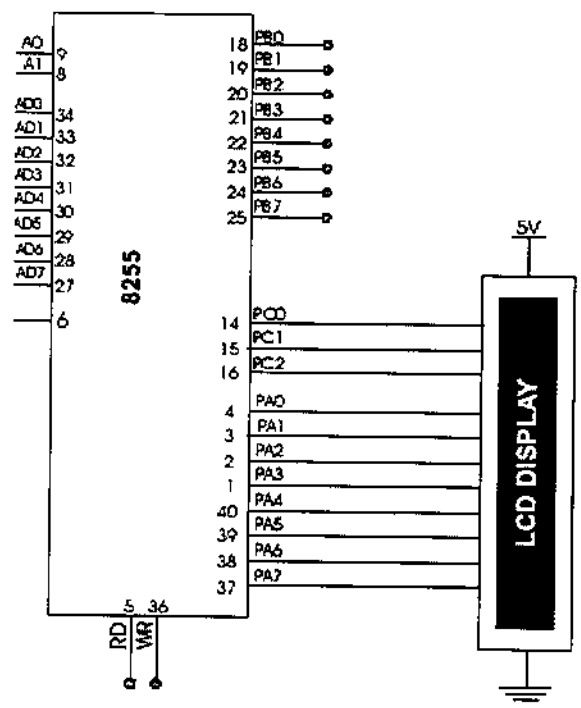


Fig 3.3.3 Programmable Peripheral Interface

The digitalized digital data from ADC is sent to the port A of programmable peripheral interface and the output is obtained at port B and lower part of port C (PC0 - PC3). This output is then given to the LCD display as shown in the above figure 3.3.3.

The 8255 is a widely used programmable parallel I/O device. It can be programmed to transfer data under various conditions from simple I/O to interrupt I/O. The 8255 has 24 I/O pins that can be grouped primarily in two 8 bit parallel ports : A & B with the remaining 8 bits as port C. The 8 bits of port C can be used as individual bits or be grouped into two 4 bit ports : C upper and C lower. The functions of 8255 can be classified into two modes :

1. Bit set / Reset (BSR)
2. I / O Mode.

The BSR mode is used to set or reset the bits in port C. The I/O mode is further divided into 3 modes :

1.Mode 0,

2.Mode 1 and

3.Mode 2

In mode 0 , all ports function as simple I/O ports.

Mode 1 is a handshake mode, whereby ports A &/or B use bits from port C as handshake signals.

In mode 2, port A can be setup for bi-directional data transfer using handshake signals from port C and port B can be setup either in mode 0 or mode 1.

3.3.4 DECODER LS 74139

It is a 2x4 decoder with 2 binary weighted inputs (B, A or A1, A0)and one active low enable input. When it is enable, one of the 4 output signals corresponding to the decimal equivalent of the input goes active low. When it is not enabled all output signals remain high.

3.3.5 LATCH LS 74373

It is a 4 bit latch, each pair of bits is controlled by high enable input E. It also has complementary outputs (Q and Q'). The information at D input is transferred to Q output when E is high and Q follows D input as long as E is high. When E goes low D input is latched at the output and remains latched until E goes high again.

3.4 LCD DISPLAY :

The intensities of the LDR' s placed in the east direction and west direction are displayed along with the battery voltage.

Liquid crystal displays (LCD's) have materials which combine the properties of both liquids and crystals. Rather than having a melting point, they have a temperature range within which the molecules are almost as mobile as they would be in a liquid, but are grouped together in an ordered form similar to a crystal.

An LCD consists of two glass panels, with the liquid crystal material sand witched in between them. The inner surface of the glass plates are coated with transparent electrodes which define the character, symbols or patterns to be displayed polymeric layers are present in between the electrodes and the liquid crystal, which makes the liquid crystal molecules to maintain a defined orientation angle. One each polarisers are pasted outside the two glass panels. These polarisers would rotate the light rays passing through them to a definite angle, in a particular direction.

When the LCD is in the off state, light rays are rotated by the two polarisers and the liquid crystal, such that the light rays come out of the LCD without any orientation, and hence the LCD appears transparent.

When sufficient voltage is applied to the electrodes, the liquid crystal molecules would be aligned in a specific direction. The light rays passing through the LCD would be rotated by the polarisers, which would result in activating / highlighting the desired characters. The LCD's are lightweight with only a few millimeters thickness. Since the LCD's consume less power, they are compatible with low power electronic circuits, and can be powered for long durations.

The LCD's don't generate light and so light is needed to read the display. By using backlighting, reading is possible in the dark. The LCD's have

long life and a wide operating temperature range. Changing the display size or the layout size is relatively simple which makes the LCD's more customer friendly.

The LCD's used exclusively in watches, calculators and measuring instruments are the simple seven-segment displays, having a limited amount of numeric data. The recent advances in technology have resulted in better legibility, more information displaying capability and a wider temperature range. These have resulted in the LCD's being extensively used in telecommunications and entertainment electronics. The LCD's have even started replacing the cathode ray tubes (CRTs) used for the display of text and graphics, and also in small TV applications.

3.5 DRIVER CIRCUIT:

The supply to the driver circuit is given by means of a battery which is charged by the electrical energy obtained from the solar panel. Hence no external supply is required. The driver circuit consists of the following components. They are

1. Relay Control
2. DC Motor

3.5.1 RELAY CONTROL :

The supply from the battery is given to the NO (Normally Open) terminal which drives the motor. The input signal to the relays is obtained from the output ports of the micro controller (P1.2 - P1.3) which is used to energize the relay. Based on the signal from the micro controller, the relay operates the motor in the forward or reverse direction.

Relays are electromechanical devices. In this circuit transistor BC547 is used as a switch. The control signal is given to the base terminal of the

transistor. The collector is attached to the relay coil. There are two types of relays.

1. Normally closed
2. Normally opened

We are using normally opened type relay. When the controller output from the micro controller is high the transistor will be in the ON state, so relay is energized. When the controller output from the micro controller is low the transistor will be in the OFF state, so relay is de-energized the valve will open. When the relay is de-energized the valve will close. So according to the controller output the valve will open or close and thus level is maintained.

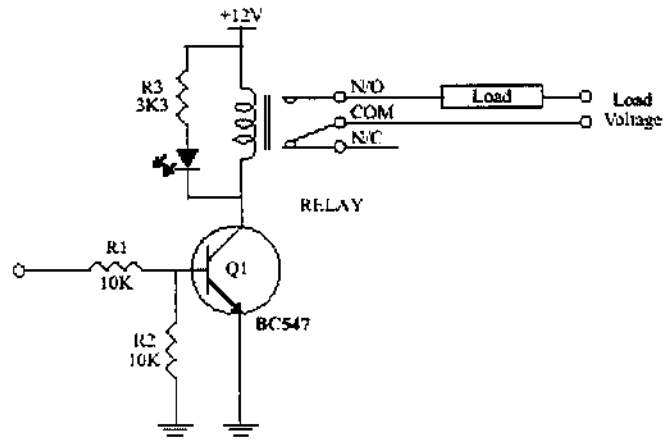


Fig 3.5.1 Relay circuit

3.5.2 DC MOTOR:

The drive along with the relay consists of a permanent magnet DC motor. The supply to the DC motor is given through the relay. The direction of rotation of shaft is either in the forward or reverse direction. For forward rotation of the motor the supply from the relay is given to the positive and negative terminals of the motor respectively. If the supply is reversed the motor rotates in reverse direction. The forward or the reverse movement of the motor helps to rotate the solar panel in the west or the east direction respectively. The DC drive has an inbuilt gear which reduces the produced RPM to 30 rpm . The following are the specifications for the permanent magnet DC motor

Rated Voltage (DC) : 12 V.

Rated Amps (DC) : 1.5 A.

Rated Power (DC) : 18 W.

Rated Speed : 30 rpm.

The permanent magnet is an important excitation source commonly employed for imparting energy to magnetic circuits used in rotating machines and other types of electron mechanical devices. There are three classes of permanent magnetic materials used for permanent magnet DC motors(PMDC). They are Alnico, ceramics and rare earth materials. Alnico magnets are used in motors upto 200KW while ceramic magnets are most economical in fractional KW motors. The rare earth magnetic materials are very costly, but are the most economic choice in various small motors. The latest addition is neodymium-iron boron. At room temperature, it has highest energy products of all commonly available magnets. The high permeance and coercivity allow marked reduction in motor frame size for the same output compared to motors using ceramic magnets. For very high temperature applications alnico or rare earth

cobalt magnets must be used. A number of new permanent magnetic materials - ceramics and rare earth magnetic materials have become available commercially. These materials have high residual flux as well as high coercivity. Smaller fractional and sub fractional HVDC motors are now constructed with permanent magnet poles. As no field windings are needed, so no field current and continuous field loss. As a result PMDC motors are smaller in size than the corresponding rated field wound type motors, this fact partially off-sets the high cost of permanent magnets. These motors offer shunt type characteristic and can only be armature controlled. The risk of permanent magnetism getting destroyed by armature reaction (at starting/reversing or heavy over-loads) has been greatly reduced by the new PM materials.

MECHANICAL MODELLING :

The panel is mounted on the DC motor by using a suitable gear arrangement. In order to rotate the panel this rpm produced is very high. Hence in order to reduce the rpm gear reduction technique is employed.

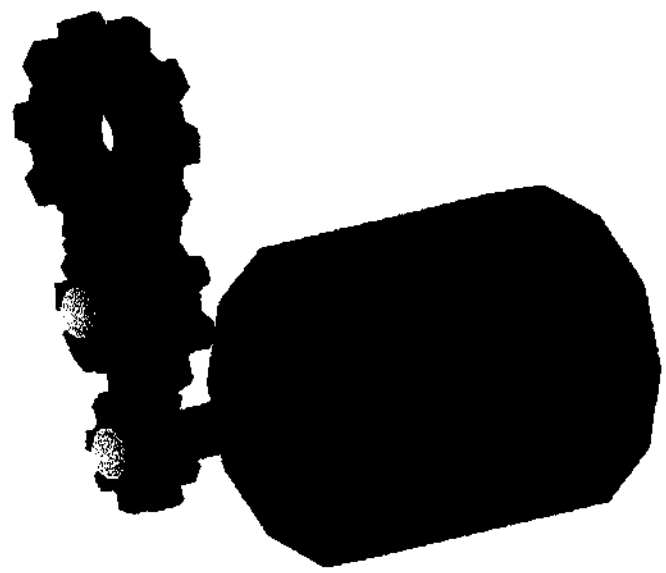


Fig 3.5.2 Mechanical model

In the above fig 3.5.2, Blue colored cylinder represents the DC motor , Blue colored Pinion represents the gear which has 20 teeth's , Red colored pinion represents the gear with 54 teeth's and Green colored pinion represents the gear with 72 teeth's . Speed reduction is done using the following calculation

Reduced speed = present shaft speed/Gear ratio.

Gear ratio = Greater teethed gear/smaller teethed gear.

Now the shaft speed of the DC motor is 30 rpm. First it is reduced by a gear ratio of 54/20. then that reduced speed is further reduced by a gear ratio of 72/20 to 3 rpm approximately

That is

Gear ratio 1 = 54/20 = 2.7

Reduced speed = 30/2.7 = 11.11 rpm

Gear ratio 2 = 72/20 = 3.6

Final speed required for rotating solar panel = 11.11/3.6 = 3.08 rpm

Thus the speed is reduced to $1/10^{th}$ of the shaft speed.

SOLAR PANEL :

The solar panel which we have used in our project is manufactured by BHEL, India and it has an array of 72 cells (8 rows and 9 columns). The cells used in the solar panel are photo voltaic cells.

These cells are made from silicon which is abundantly available on the earth's surface. Photovoltaic cells have the unique property of converting light energy into electrical energy. A glass covering is placed above the cells. Glass has the unique property of refraction that is it allows the sun's rays to pass through it but prevents it from getting reflected. The glass covering also acts as a protective shield to the photo voltaic cells. The electrical energy produced is stored with the help of a battery. Following are the specifications of solar panel.

Rated voltage	=	20V (max).
Rated power	=	12W (max).
Rated current	=	0.6A.

BATTERY :

The main source of power for our project is obtained from a 12V DC rechargeable battery. The electrical energy obtained from the solar panel is used to charge the battery. The battery is used to supply voltages to the various components like relay, micro controller, DC motor and to a fan type load which is used as an application. The supply to the micro controller is regulated using an IC 7805 regulator.

CHAPTER 4: ALGORITHM AND OPERATION

CHAPTER 4

ALGORITHM AND OPERATION

Automatic tracking system for solar panel consists of one main program and four sub routines. They are

1. Read - Used to read data from the sensing circuit
2. Write - Used to write the data into the micro controller
3. Control - To check whether the values lie with in the limits and further operation is carried
4. Display - The values like east LDR intensity, west LDR intensity and battery voltage are displayed in LCD

ALGORITHM FOR MAIN PROGRAM:

Step 1: Start.

Step 2: Initialize relay 1 and relay 2 to zero.

Step 3: Call the subprogram, read.

Step 4: Call the subprogram, write.

Step 5: Call the subprogram, control.

Step 5: Call the subprogram, display.

Step 6: Stop.

ALGORITHM FOR SUBPROGRAMS

READ :

Step 1: Initialize port b.

Step 2: Initialize port c = 0x04 and give a delay .

Step 3: Initialize port c = 0x00 and give a delay.

Step 4: Return to main program.

WRITE :

Step 1: Initialize port b.

Step 2: Initialize port c = 0x05 and give a delay .

Step 3: Initialize port c = 0x01 and give a delay.

Step 4: Return to main program.

CONTROL :

Step 1: The values data_adc0 and data_adc1 are compared. If data_adc0 > data_adc1 calculate error. If not goto step 3

Step 2: If this error > 5 and key1 = =1 set relay 1 = 1 and relay 2 = 0 else both the relays are set to zero. Goto step 6

Step 3: If data_adc0 < data_adc1 calculate error.

Step 4: If this error > 5 and key2 = = 1 set both the relays to 1 else set both the relays to zero. Goto step 6

Step 5: When key 2 is pressed the relay 1 is set to 1 and relay 2 to zero

Step 6: Return to main program.

DISPLAY :

Step 1: Display the values of east intensity, west intensity and battery voltage in LCD through programmable peripheral interface.

Step 2: Return to main program.

OPERATION:

The operation of automatic tracking system for solar panel is as follows. Two LDR's are kept at opposite ends of the panel such that one facing towards east and other towards west. Two limit switches are oppositely placed at the end of the base plate beyond which the panel can't rotate. The intensity of the LDR's decreases with increase in sunlight. Hence the panel rotates where the intensity of the LDR is less. An error of +5% or -5% is maintained between the LDR values. These analog values are then given to ADC 0809 at I/P port. ADC converts these analog values into their respective digital equivalents. The digital equivalent obtained is an eight bit data. This eight bit data is then fed to the micro controller (AT89C51) through port 0 (pin 39 - pin 32). The output is taken through port 1 (P1.2 - P1.3) and given to the driver circuit. The two digitalized signals are compared with each other in order to decide the direction of rotation of solar panel. A tolerance value of +5 (0000 0101) or -5 (1111 1011) is maintained. The differential digitalized voltage is then calculated and compared with the tolerance value. If the differential value is greater than the tolerance value then a signal is generated at the output port which activates the relay and in turn drives the motor and the panel. If the differential digitalized value is lesser than or equal to the tolerance value, no signal is generated and hence motor will not rotate. Port 1.0 and Port 1.1 are connected to two limit switches. The sun rises in the east and sets in the west. After sunset, the panel is supposed to come to the east direction in order to perform tracking for the next day. Hence the micro controller is programmed in such a way that once the panel touches the limit switch in the west direction, it returns to the east direction without tracking. The supply to the motor is given by means of a relay. The direction of rotation of the motor either forward or reverse is also decided by the signals given to the relays. The power obtained from the panel is

stored in a battery from which the power is fed to driver circuit, application and various system components in the hardware circuitry like micro controller, ADC, decoder, LCD, programmable peripheral interface etc.

CHAPTER 5: RESULTS AND COMPARISON

CHAPTER 5

RESULTS AND COMPARISON

By employing the automatic tracking system for solar panel the following results are obtained.

1. Solar panel output - 12W, 19.5V
2. Battery voltage - 12V, 5A
3. DC motor rating - 12V, 18W, 1.5A

The output voltage of solar panel is kept almost same from morning to evening with the help of tracking. The output voltage is stored in a battery from which the supply is given to the permanent magnet DC motor, relay unit and to the various system components through voltage regulators. Hence, our project does not need any external power supply for various components present in the hardware circuitry.

To prove that our project is more effective than the conventional static solar panels a comparative study has been made by measuring voltages from morning sunrise to sunset for every two hours and the results are tabulated as follows.

TABLE 5.1 COMPARATIVE STUDIES

TIME (Hrs)	WITH TRACKING (V)	WITHOUT TRACKING (V)
6.30	12.5	12.5
8.30	19.25	18.85
10.30	18.87	18.34
12.30	18.8	18.31
14.30	19.61	17.6
16.30	18.8	17.3
18.30	15.3	12.05

A graph is drawn by taking time along x-axis and voltage along y-axis for the readings tabulated above. The variations are shown graphically in the form of chart below.

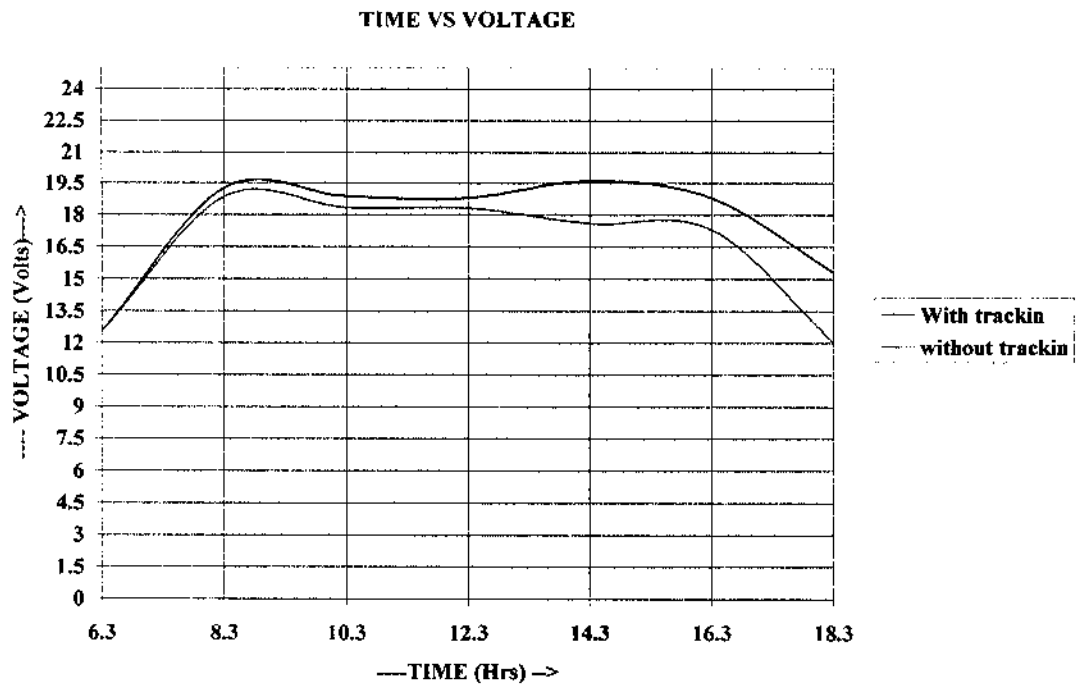


Fig .5.1

CHAPTER 6: CONCLUSION

CHAPTER 6
CONCLUSION

6.1 GENERAL :

A micro controller based automatic tracking system for solar panel has been designed and tested successfully in areas which receive adequate suns rays throughout the year. The main advantage of our project is that no external power supply is required. The conventional models which are being used in the market today are static in nature and because of this the efficiency depends upon the fall of rays .The project we have developed is working based on the LDR sensed directions and there by it increases the efficiency of the solar tracking system. As we have used LDRs in our project, it is very sensitive to variations of light .The existing system consists of GPS system which is costly and cannot be used by majority of the population. The system implemented by us is much cheaper when compared with GPS system and at the same time efficient

6.2 FUTURE ENHANCEMENT :

The working model is a prototype of the DC solar water pump. The working model can also be further extended to fields such as street lighting, emergency lamps etc.

6.3 EPILOGUE :

The project Automatic Tracking System For Solar Panel is a new opening in the field of solar energy utilization. The project is developed taking into consideration the future developments that will take place in the forth coming days. But at any point of time and technology the main aim of the project is to use sun's rays effectively and efficiently for the human welfare.

APPENDIX

APPENDIX

PROGRAM :

```
# include <reg51.h>
void control( );
void all_disp( );
void display( );
void htd (unsigned int);
void adc0( );
void adc1( );
void adc2( );
void lcd_init( );
void lcd_dis (unsigned char*,unsigned char);
void delay (unsigned int);
void read (unsigned char);
void write (unsigned char);
sbit relay1 = P1^0;
sbit relay2 = P1^1;
sbit key1 = P1^2;
sbit key2 = P1^3;
pdata unsigned char ch0 _at_ 0x08;
pdata unsigned char ch1 _at_ 0x09;
pdata unsigned char ch2 _at_ 0x0a;
pdata unsigned char soc _at_ 0x10;
pdata unsigned char porta _at_ 0x18;
pdata unsigned char portb _at_ 0x19;
pdata unsigned char portc _at_ 0x1a;
pdata unsigned char cwr _at_ 0x1b;
unsigned char data_adc0,data_adc1,data_adc2,err;
unsigned char tenthous,thous,hund,ten,one,hund_r;
unsigned int tenthous_r,thous_r;
main( )
{
 relay1 = 0;
 relay2 = 0;
 lcd_init( );
 read (0x80);
 lcd_dis(" SOLAR TRACKING ",16);
 read (0xc0);
 lcd_dis("    SYSTEM    ",16);
 delay (65000);
 delay (65000);
 delay (20000);
```

```
while ( key1)
{
 relay1 = 1;
 relay2 = 0;
}
relay1 = 0;
relay2 = 0;
read (0x01);
while (1)
{
 all_disp( );
 adc1( );
 htd (data_adc1);
 read (0x83);
 display( );
 adc0( );
 htd (data_adc0);
 read (0x8a);
 display( );
 adc2 ( );
 htd (data_adc2);
 read (0xCc);
 display( );
 if (data_adc0>240 && data_adc1>240)
 {
  while (key1)
  {
   relay1 = 1;
   relay2 = 0;
  }
  relay1 = 0;
  relay2 = 0;
 }
 control( );
 delay (25000);
}
}
void control( )
{
 if (data_adc0>data_adc1)
 {
 err = data_adc0 - data_adc1;
 if (err>5 &&  key1= =1)
```

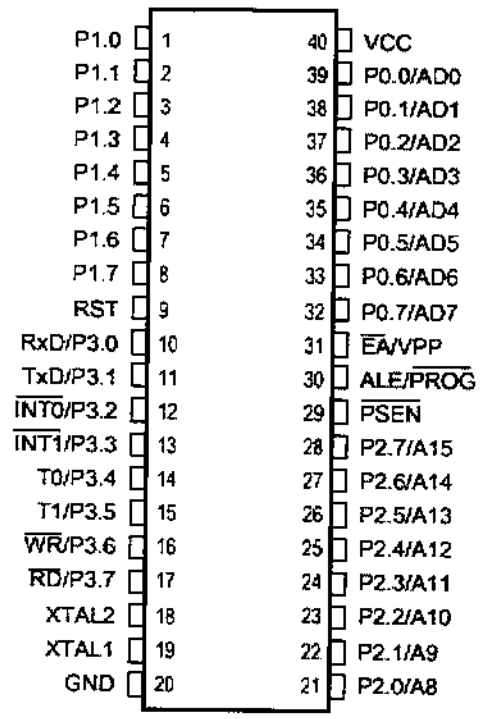
```
{
 relay1 = 1;
 relay2 = 0;
}
else
{
 relay1 = 0;
 relay2 = 0;
}
}
else if (data_adc0<data_adc1)
{
err = data_adc1- data_adc0;
if (err>5 && key2= =1)
{
 relay2 = 1;
 delay (50000);
 delay (25000);
 relay1= 1;
}
else
{
 relay1 = 0;
 relay2 = 0;
}
}
if(key2= =0)
{
 while ( key1)
 {
  relay1 = 1;
  relay2 = 0;
 }
 relay1 = 0;
 relay2 = 0;
}}
void all_disp( )
{
 read (0x80);
 lcd_dis (" E :",3);
 read (0x87);
 lcd_dis (" W :",3);
 read (0xc0);
```

```
 lcd_dis (" Battery Volt:",12);
}
void display( )
{
 write (hund+0x30);
 write (ten+0x30);
 write (one+0x30);
}
void htd(unsigned int air)
{
 hund = air/100;
 hund_r = air%100;
 ten = hund_r/10;
 one = hund_r%10;
}
void adc0( )
{
 unsigned char x;
 x = ch0;
 delay (30);
 data_adc0 = soc;
}
void adc1( )
{
 unsigned char x;
 x = ch1;
 delay (30);
 data_adc1 = soc;
}
void adc2( )
{
 unsigned char x;
 x = ch2;
 delay (30);
 data_adc2 = soc;
}
void lcd_init( )
{
 cwr = 0x80;
 read (0x38);
 read (0x06);
 read (0x0c);
}
```

```
void lcd_dis(unsigned char *mess,unsigned char n)
{
 unsigned char i;
 for(i=0;i<n;i++)
 {
  write (mess[i]);
 }}
void read(unsigned char i)
{
 portb = i;
 portc = 0x04;
 delay (125);
 portc = 0x00;
 delay (125);
}
void write(unsigned char i)
{
 portb = i;
 portc = 0x05;
 delay (125);
 portc = 0x01;
 delay (125);
}
void delay(unsigned int s)
{
 while (s--);
}
```

MICROCONTROLLER :

ATMEL 89C51
PIN DIAGRAM



BLOCK DIAGRAM

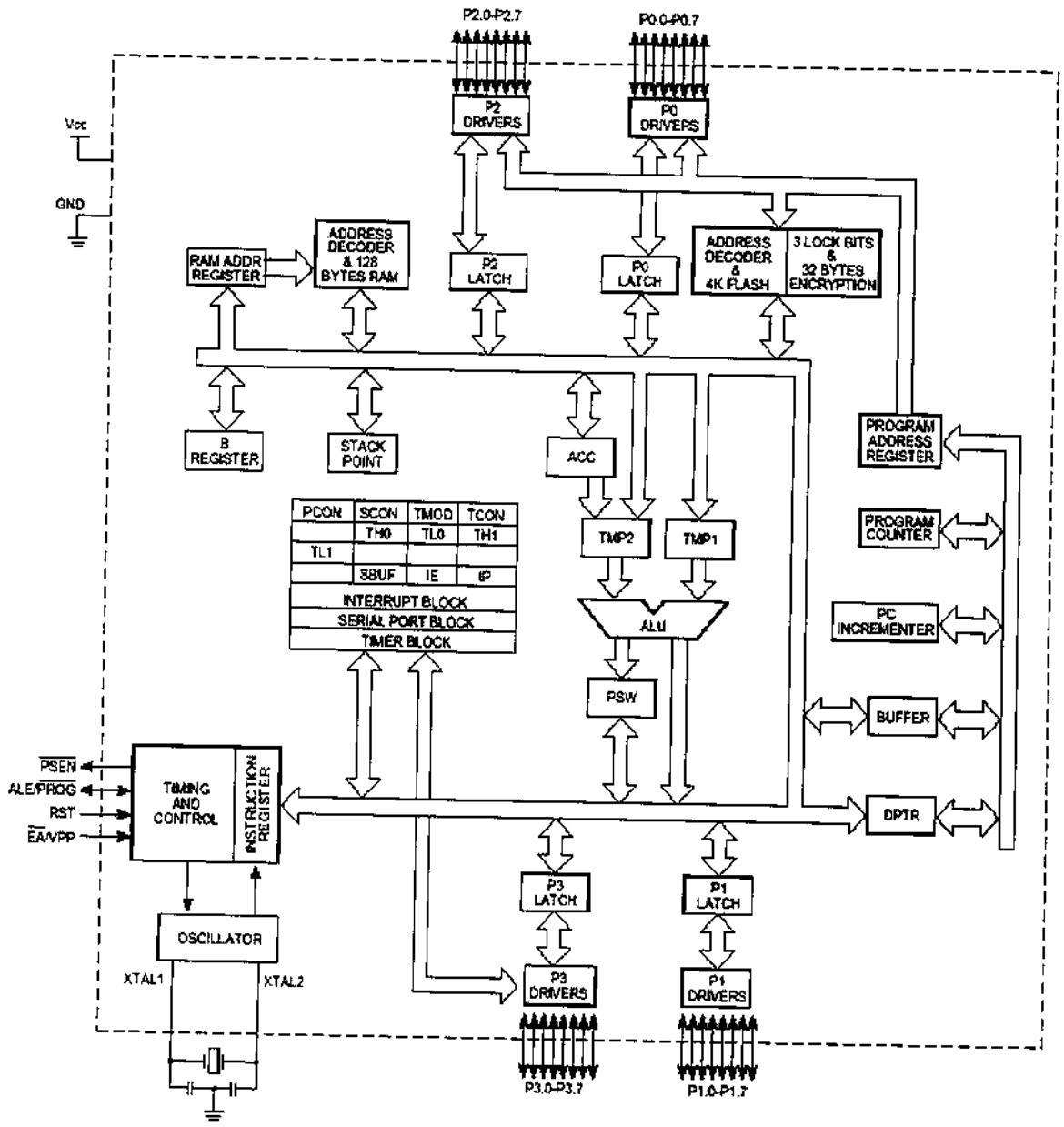


Table 1. Detailed Pin Description

Symbol	PDIP	PLCC	PQFP	I/O	Name and Function
ALE/$\overline{PROG}$	30	33	27	I/O	**Address Latch Enable:** Output pulse for latching the low byte of the address during an address to the external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the Program Pulse input ($\overline{PROG}$) during Flash programming.
$\overline{EA}$/V_{PP}	31	35	29	I	**External Access enable:** $\overline{EA}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H to FFFFH. If $\overline{EA}$ is held high, the device executes from internal program memory unless the program counter contains an address greater than 0FFFH. This also receives the 12V programming enable voltage (V_{PP}) during Flash programming.
P0.0-P0.7	39-32	43-36	37-30	I/O	**Port 0:** Port 0 is an 8-bit open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pullups when emitting 1s. Port 0 also receives the code bytes during programmable memory programming and outputs the code bytes during program verification. External pullups are required during program verification.
P1.0-P1.7	1-8	2-9	40-44 1-3	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 pins that have 1s written to them are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pullups. (See DC Characteristics: I_{IL}). The Port 1 output buffers can sink/source four TTL inputs. Port 1 also receives the low-order address byte during Flash programming and verification.
P2.0-P2.7	21-28	24-31	18-25	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pullups. Port 2 pins that have 1s written to them are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pullups. (See DC Characteristics: I_{IL}). Port 2 emits the high order address byte during fetches from external program memory and during accesses to external data memory that used 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ Ri [i = 0, 1]), Port 2 emits the contents of the P2 Special Function Register. Port 2 also receives the high-order bits and some control signals during Flash programming and verification. P2.6 and P2.7 are the control signals while the chip programs and erases.

Symbol	PDIP	PLCC	PQFP	I/O	Name and Function
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pullups. Port 3 pins that have 1s written to them are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pullups. (See DC Characteristics: I_{IL}).
					Port 3 also serves the special features of the IS89C51, as listed below:
	10	11	5	I	**RxD (P3.0):** Serial input port.
	11	13	7	O	**TxD (P3.1):** Serial output port.
	12	14	8	I	**$\overline{INT0}$ (P3.2):** External interrupt 0.
	13	15	9	I	**$\overline{INT1}$ (P3.3):** External interrupt 1.
	14	16	10	I	**T0 (P3.4):** Timer 0 external input.
	15	17	11	I	**T1 (P3.5):** Timer 1 external input.
	16	18	12	O	**$\overline{WR}$ (P3.6):** External data memory write strobe.
	17	19	13	O	**$\overline{RD}$ (P3.7):** External data memory read strobe.
$\overline{PSEN}$	29	32	26	O	**Program Store Enable:** The read strobe to external program memory. When the device is executing code from the external program memory, $\overline{PSEN}$ is activated twice each machine cycle except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.
RST	9	10	4	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal MOS resistor to GND permits a power-on reset using only an external capacitor connected to Vcc.
XTAL 1	19	21	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL 2	18	20	14	O	**Crystal 2:** Output from the inverting oscillator amplifier.
GND	20	22	16	I	**Ground:** 0V reference.
Vcc	40	44	38	I	**Power Supply:** This is the power supply voltage for operation.

FLASH PROGRAMMING AND VERIFICATION CHARACTERISTICS AND WAVEFORMS

Table 14. Flash Programming and Verification Characteristics[1]

Symbol	Parameter	Min	Max	Unit
V_{PP}	Programming Supply Voltage	11.5	12.5	V
$1/t_{CLCL}$	Oscillator Frequency	3.5	12	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	48	—	t_{CLCL}
t_{GHAX}	Address Hold after $\overline{PROG}$	48	—	t_{CLCL}
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	48	—	t_{CLCL}
t_{GHDX}	Data Hold after $\overline{PROG}$	48	—	t_{CLCL}
t_{EHSH}	COND ENABLE to V_{PPH}	48	—	t_{CLCL}
t_{SHGL}	V_{PPH} Setup to $\overline{PROG}$ Low	10	—	µs
t_{GHSL}	V_{PPH} Hold after $\overline{PROG}$	10	—	µs
t_{GLGH}	$\overline{PROG}$ Pulse Width	120	—	µs
t_{GHGL}	$\overline{PROG}$ High to $\overline{PROG}$ Low	10	—	µs
t_{AVQV}	Address to Data Valid	—	48	t_{CLCL}
t_{ELQV}	COND ENABLE to Data Valid	—	48	t_{CLCL}
t_{EHQZ}	Data Float after COND DISABLE	—	48	t_{CLCL}
t_{GLGHE}	Erase $\overline{PROG}$ Pulse Width	200	—	ms
t_{ELPL}	COND DISABLE to Power Low	0	—	ns
t_{PLPH}	Power Off Time	10	—	µs
t_{PHEH}	Power On to V_{PPL}	10	—	ms
t_{EHVH}	V_{PPL} to COND ENABLE	0	—	ns

Notes:
1. T_A = 21°C to 27°C, Vcc = 5.0V ± 10%.
2. COND ENABLE and COND DISABLE are generated and depend on the control signals on pins P2.6, P2.7, P3.6 and P3.7. The signals set the device in to and out of different processing conditions, such as programming condition, erasing condition, and verify condition.

AC CHARACTERISTICS

(Over Operating Range; GND = 0V; C_L for Port 0, ALE and $\overline{PSEN}$ Outputs = 100 pF; C_L for Other Outputs = 80 pF)

EXTERNAL MEMORY CHARACTERISTICS

Symbol	Parameter	24 MHz Clock Min	24 MHz Clock Max	40 MHz Clock Min	40 MHz Clock Max	Variable Oscillator (3.5 - 40 MHz) Min	Variable Oscillator (3.5 - 40 MHz) Max	Unit
1/t_{CLCL}	Oscillator frequency	—	—	—	—	3.5	40	MHz
t_{LHLL}	ALE pulse width	68	—	35	—	2t_{CLCL}–15	—	ns
t_{AVLL}	Address valid to ALE low	26	—	10	—	t_{CLCL}–15	—	ns
t_{LLAX}	Address hold after ALE low	31	—	15	—	t_{CLCL}–10	—	ns
t_{LLIV}	ALE low to valid instr in	—	147	—	80	—	4t_{CLCL}–20	ns
t_{LLPL}	ALE low to $\overline{PSEN}$ low	31	—	15	—	t_{CLCL}–10	—	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	110	—	60	—	3t_{CLCL}–15	—	ns
t_{PLIV}	$\overline{PSEN}$ low to valid instr in	—	105	—	55	—	3t_{CLCL}–20	ns
t_{PXIX}	Input instr hold after $\overline{PSEN}$	0	—	0	—	0	—	ns
t_{PXIZ}	Input instr float after $\overline{PSEN}$	—	37	—	20	—	t_{CLCL}–5	ns
t_{AVIV}	Address to valid instr in	—	188	—	105	—	5t_{CLCL}–20	ns
t_{PLAZ}	$\overline{PSEN}$ low to address float	—	10	—	10	—	10	ns
t_{RLRH}	$\overline{RD}$ pulse width	230	—	130	—	6t_{CLCL}–20	—	ns
t_{WLWH}	$\overline{WR}$ pulse width	230	—	130	—	6t_{CLCL}–20	—	ns
t_{RLDV}	$\overline{RD}$ low to valid data in	—	157	—	90	—	4t_{CLCL}–10	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	—	0	—	0	—	ns
t_{RHDZ}	Data float after $\overline{RD}$	—	78	—	45	—	2t_{CLCL}–5	ns
t_{LLDV}	ALE low to valid data in	—	282	—	165	—	7t_{CLCL}–10	ns
t_{AVDV}	Address to valid data in	—	323	—	190	—	8t_{CLCL}–10	ns
t_{LLWL}	ALE low to $\overline{RD}$ or $\overline{WR}$ low	105	145	55	95	3t_{CLCL}–20	3t_{CLCL}+20	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ low	146	—	80	—	4t_{CLCL}–20	—	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	26	—	10	—	t_{CLCL}–15	—	ns
t_{WHQX}	Data hold after $\overline{WR}$	31	—	15	—	t_{CLCL}–10	—	ns
t_{RLAZ}	$\overline{RD}$ low to address float	—	0	—	0	—	0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ high to ALE high	26	57	10	40	t_{CLCL}–15	t_{CLCL}+15	ns

DC CHARACTERISTICS

(Over Operating Range; GND = 0V)

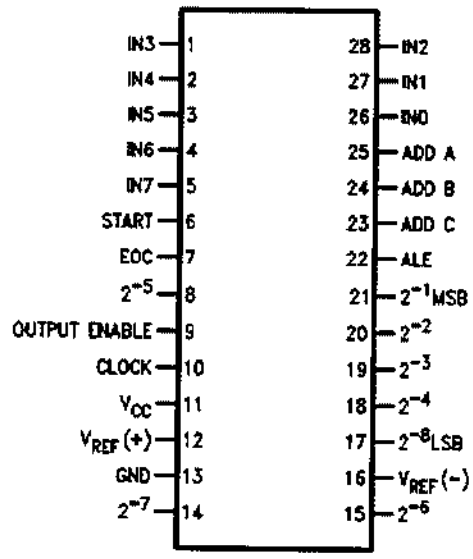
Symbol	Parameter	Test conditions	Min	Max	Unit
V_{IL}	Input low voltage (All except $\overline{EA}$)		–0.5	0.2Vcc – 0.1	V
V_{IL1}	Input low voltage ($\overline{EA}$)		–0.5	0.2Vcc – 0.3	V
V_{IH}	Input high voltage (All except XTAL 1, RST)		0.2Vcc + 0.9	Vcc + 0.5	V
V_{IH1}	Input high voltage (XTAL 1)		0.7Vcc	Vcc + 0.5	V
V_{SCH+}	RST positive schmitt-trigger threshold voltage		0.7Vcc	Vcc + 0.5	V
V_{SCH-}	RST negative schmitt-trigger threshold voltage		0	0.2Vcc	V
V_{OL}[1]	Output low voltage (Ports 1, 2, 3)	Iol = 100 µA	—	0.3	V
		I_{OL} = 1.6 mA	—	0.45	V
		I_{OL} = 3.5 mA	—	1.0	V
V_{OL1}[1]	Output low voltage (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 200 µA	—	0.3	V
		I_{OL} = 3.2 mA	—	0.45	V
		I_{OL} = 7.0 mA	—	1.0	V
V_{OH}	Output high voltage (Ports 1, 2, 3, ALE, $\overline{PSEN}$)	I_{OH} = –10 µA Vcc = 4.5V-5.5V	0.9Vcc	—	V
		I_{OL} = –25 µA	0.75Vcc	—	V
		I_{OL} = –60 µA	2.4	—	V
V_{OH1}	Output high voltage (Port 0, ALE, $\overline{PSEN}$)	I_{OH} = –80 µA Vcc = 4.5V-5.5V	0.9Vcc	—	V
		I_{OH} = –300 µA	0.75Vcc	—	V
		I_{OH} = –800 µA	2.4	—	V
I_{IL}	Logical 0 input current (Ports 1, 2, 3)	V_{IN} = 0.45V	—	–80	µA
I_{LI}	Input leakage current (Port 0)	0.45V < V_{IN} < Vcc	–10	+10	µA
I_{TL}	Logical 1-to-0 transition current (Ports 1, 2, 3)	V_{IN} = 2.0V	—	–650	µA
R_{RST}	RST pulldown resister		50	300	KΩ

Note:

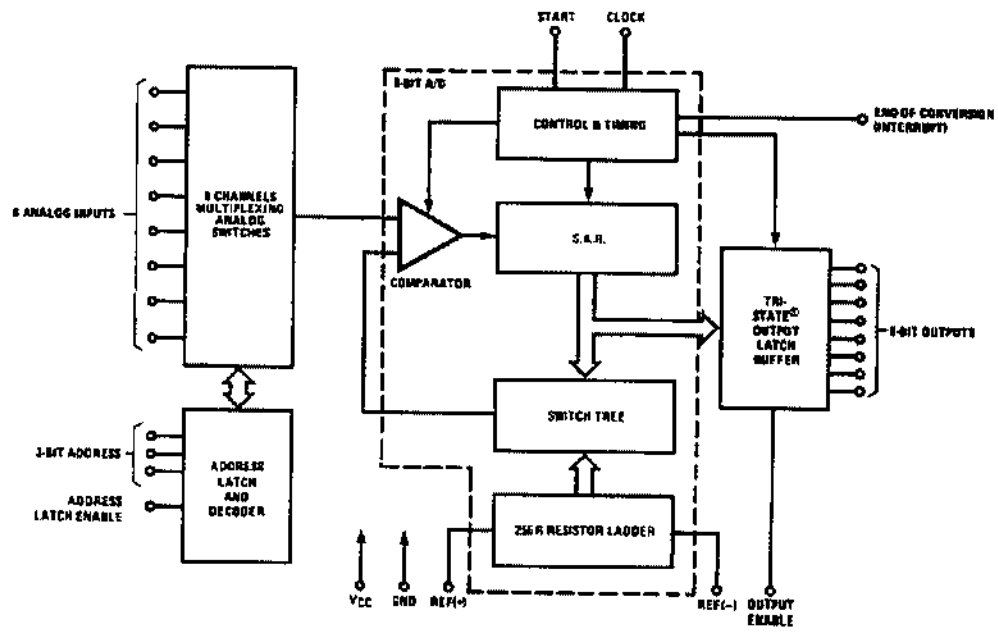
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port
   Port 0: 26 mA
   Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification.

ANALOG TO DIGITAL CONVERTER :

ADC 0809
PIN DIAGRAM



BLOCK DIAGRAM



Electrical Characteristics

Converter Specifications: V_{CC}=5 V_{DC}=V_{REF+}, $V_{REF(-)}$=GND, T_{MIN}≤T_A≤T_{MAX} and f_{CLK}=640 kHz unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	ADC0808					
	Total Unadjusted Error	25°C			±½	LSB
	(Note 5)	T_{MIN} to T_{MAX}			±¾	LSB
	ADC0809					
	Total Unadjusted Error	0°C to 70°C			±1	LSB
	(Note 5)	T_{MIN} to T_{MAX}			±1¼	LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	2.5		kΩ
	Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.10		V_{CC}+0.10	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	V_{CC}+0.1	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder		V_{CC}/2-0.1	V_{CC}/2	V_{CC}/2+0.1	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V
I_{IN}	Comparator Input Current	f_c=640 kHz, (Note 6)	−2	±0.5	2	µA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV, 4.75≤V_{CC}≤5.25V, −40°C≤T_A≤+85°C unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
$I_{OFF(+)}$	OFF Channel Leakage Current	V_{CC}=5V, V_{IN}=5V,				
		T_A=25°C		10	200	nA
		T_{MIN} to T_{MAX}			1.0	µA
$I_{OFF(-)}$	OFF Channel Leakage Current	V_{CC}=5V, V_{IN}=0,				
		T_A=25°C	−200	−10		nA
		T_{MIN} to T_{MAX}	−1.0			µA
CONTROL INPUTS						
$V_{IN(1)}$	Logical "1" Input Voltage		V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	V_{IN}=15V			1.0	µA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	V_{IN}=0	−1.0			µA
I_{CC}	Supply Current	f_{CLK}=640 kHz		0.3	3.0	mA

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV, $4.75 \le V_{CC} \le 5.25V$, $-40^{\circ}C \le T_A \le +85^{\circ}C$ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 4.75V I_{OUT} = −360µA I_{OUT} = −10µA		 2.4 4.5		 V(min) V(min)
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O=1.6 mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	I_O=1.2 mA			0.45	V
I_{OUT}	TRI-STATE Output Current	V_O=5V V_O=0	 −3		3	µA µA

Electrical Characteristics

Timing Specifications $V_{CC}=V_{REF(+)}=5V$, $V_{REF(-)}=GND$, $t_r=t_f=20$ ns and $T_A=25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	(*Figure 5*)		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	(*Figure 5*)		100	200	ns
t_S	Minimum Address Set-Up Time	(*Figure 5*)		25	50	ns
t_H	Minimum Address Hold Time	(*Figure 5*)		25	50	ns
t_D	Analog MUX Delay Time From ALE	R_S=0Ω (*Figure 5*)		1	2.5	µs
t_{1H}, t_{H0}	OE Control to Q Logic State	C_L=50 pF, R_L=10k (*Figure 6*)		125	250	ns
t_{1H}, t_{0H}	OE Control to Hi-Z	C_L=10 pF, R_L=10k (*Figure 6*)		125	250	ns
t_C	Conversion Time	f_C=640 kHz, (*Figure 5*) (Note 7)	90	100	116	µs
f_C	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	(*Figure 5*)	0		8+2 µS	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE Output Capacitance	At TRI-STATE Outputs		10	15	pF

Functional Description

Multiplexer. The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. *Table 1* shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE 1.

SELECTED ANALOG CHANNEL	ADDRESS LINE		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach (*Figure 1*) was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +½ LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0808, ADC0809, the approximation technique is extended to 8 bits using the 256R network.

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0808 as measured using the procedures outlined in AN-179.

Functional Description (Continued)

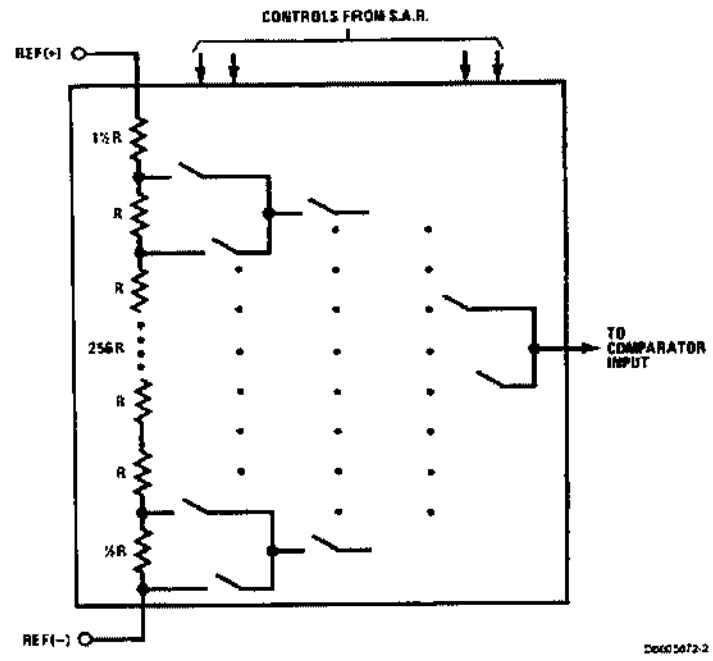


FIGURE 1. Resistor Ladder and Switch Tree

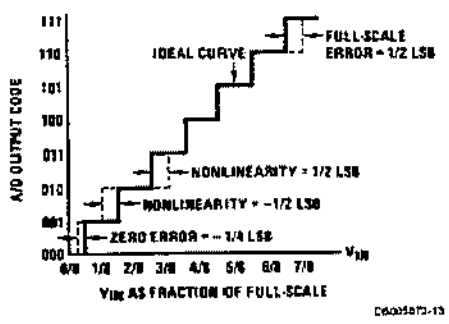


FIGURE 2. 3-Bit A/D Transfer Curve

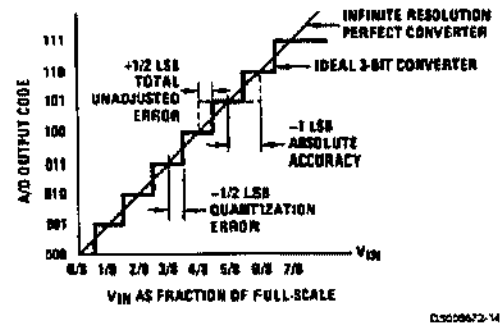


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

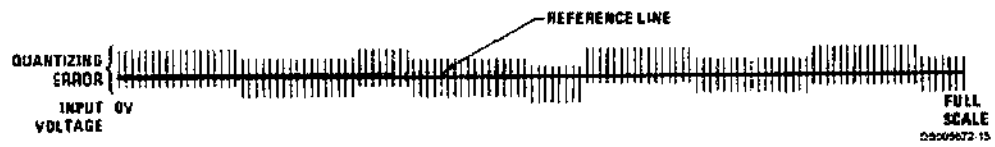
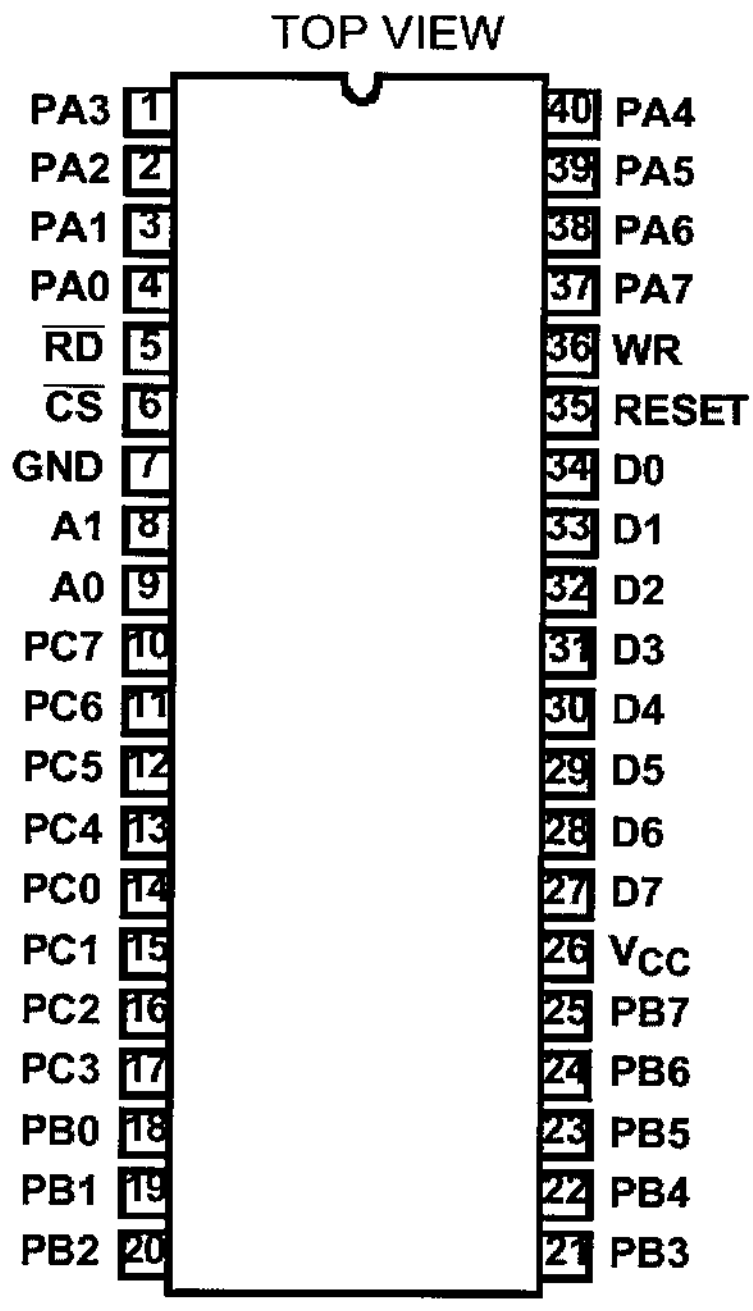


FIGURE 4. Typical Error Curve

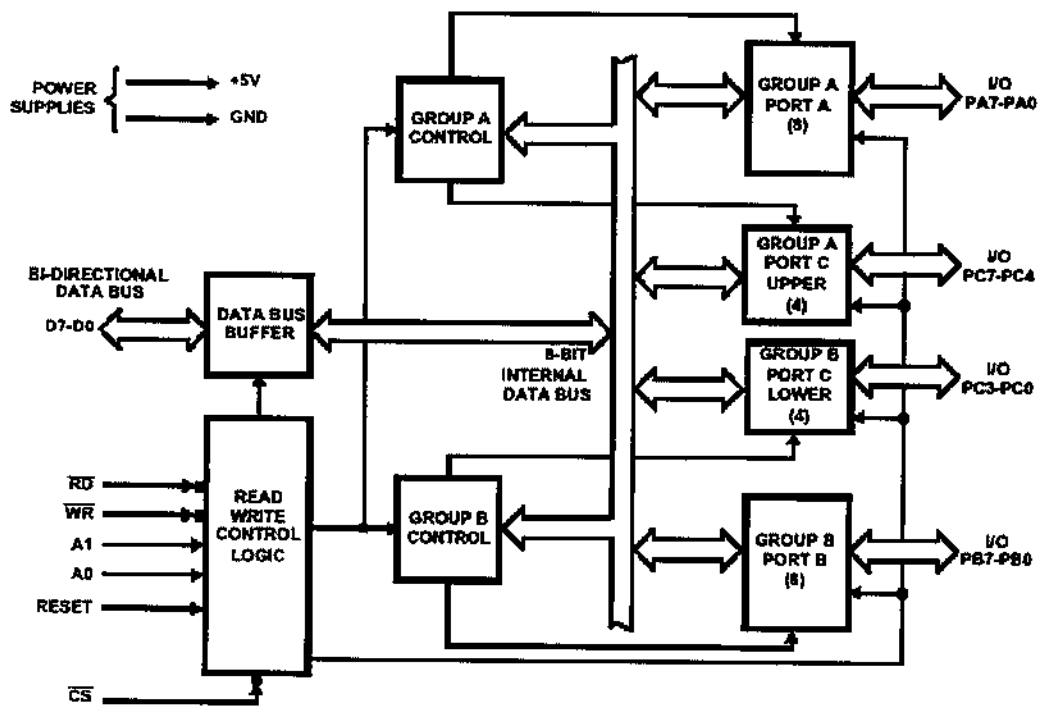
82C55A (DIP)


TOP VIEW
PA3 1
PA2 2
PA1 3
PA0 4
RD 5
CS 6
GND 7
A1 8
A0 9
PC7 10
PC6 11
PC5 12
PC4 13
PC0 14
PC1 15
PC2 16
PC3 17
PB0 18
PB1 19
PB2 20
40 PA4
39 PA5
38 PA6
37 PA7
36 WR
35 RESET
34 D0
33 D1
32 D2
31 D3
30 D4
29 D5
28 D6
27 D7
26 VCC
25 PB7
24 PB6
23 PB5
22 PB4
21 PB3

Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	26		V_{CC}: The +5V power supply pin. A 0.1µF capacitor between pins 26 and 7 is recommended for decoupling.
GND	7		GROUND
D0-D7	27-34	I/O	DATA BUS: The Data Bus lines are bidirectional three-state pins connected to the system data bus.
RESET	35	I	RESET: A high on this input clears the control register and all ports (A, B, C) are set to the input mode with the "Bus Hold" circuitry turned on.
$\overline{CS}$	6	I	CHIP SELECT: Chip select is an active low input used to enable the 82C55A onto the Data Bus for CPU communications.
$\overline{RD}$	5	I	READ: Read is an active low input control signal used by the CPU to read status information or data via the data bus.
$\overline{WR}$	36	I	WRITE: Write is an active low input control signal used by the CPU to load control words and data into the 82C55A.
A0-A1	8, 9	I	ADDRESS: These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the control word register. A0 and A1 are normally connected to the least significant bits of the Address Bus A0, A1.
PA0-PA7	1-4, 37-40	I/O	PORT A: 8-bit input and output port. Both bus hold high and bus hold low circuitry are present on this port.
PB0-PB7	18-25	I/O	PORT B: 8-bit input and output port. Bus hold high circuitry is present on this port.
PC0-PC7	10-17	I/O	PORT C: 8-bit input and output port. Bus hold circuitry is present on this port.

Functional Diagram



Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND-0.5V to V_{CC}+0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Voltage Range . . . . . +4.5V to 5.5V
Operating Temperature Range
C82C55A . . . . . 0°C to 70°C
I82C55A . . . . . -40°C to 85°C
M82C55A . . . . . -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA}	θ_{JC}
CERDIP Package	50°C/W	10°C/W
CLCC Package	65°C/W	14°C/W
PDIP Package	50°C/W	N/A
PLCC Package	46°C/W	N/A

Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Junction Temperature
CDIP Package . . . . . 175°C
PDIP Package . . . . . 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(PLCC Lead Tips Only)

Die Characteristics

Gate Count . . . . . 1000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air

Electrical Specifications

V_{CC} = 5.0V ±10%; T_A = 0°C to +70°C (C82C55A);
T_A = -40°C to +85°C (I82C55A);
T_A = -55°C to +125°C (M82C55A)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.0 2.2	-	V	I82C55A, C82C55A, M82C55A
V_{IL}	Logical Zero Input Voltage	-	0.8	V	
V_{OH}	Logical One Output Voltage	3.0 V_{CC} -0.4	-	V	I_{OH} = -2.5mA, I_{OH} = -100µA
V_{OL}	Logical Zero Output Voltage	-	0.4	V	I_{OL} +2.5mA
I_I	Input Leakage Current	-1.0	+1.0	µA	V_{IN} = V_{CC} or GND, DIP Pins: 5, 6, 8, 9, 35, 36
IO	I/O Pin Leakage Current	-10	+10	µA	VO = V_{CC} or GND DIP Pins: 27 - 34
IBHH	Bus Hold High Current	-50	-400	µA	VO = 3.0V. Ports A, B, C
IBHL	Bus Hold Low Current	50	400	µA	VO = 1.0V. Port A ONLY
IDAR	Darlington Drive Current	-2.5	Note 2, 4	mA	Ports A, B, C. Test Condition 3
ICCSB	Standby Power Supply Current	-	10	µA	V_{CC} = 5.5V, V_{IN} = V_{CC} or GND. Output Open
ICCOP	Operating Power Supply Current	-	1	mA/MHz	T_A = +25°C, V_{CC} = 5.0V, Typical (See Note 3)

NOTES:

2. No internal current limiting exists on Port Outputs. A resistor must be added externally to limit the current.
3. ICCOP = 1mA/MHz of Peripheral Read/Write cycle time. (Example: 1.0µs I/O Read/Write cycle time = 1mA).
4. Tested as V_{OH} at -2.5mA.

Capacitance T_A = 25°C

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
CIN	Input Capacitance	10	pF	FREQ = 1MHz, All Measurements are referenced to device GND
CI/O	I/O Capacitance	20	pF	

AC Electrical Specifications V_{CC} = +5V± 10%, GND = 0V; T_A = -55°C to +125°C (M82C55A) (M82C55A-5);
T_A = -40°C to +85°C (I82C55A) (I82C55A-5);
T_A = 0°C to +70°C (C82C55A) (C82C55A-5)

SYMBOL	PARAMETER	82C55A-5		82C55A		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
READ TIMING							
(1) tAR	Address Stable Before $\overline{RD}$	0	-	0	-	ns	
(2) tRA	Address Stable After $\overline{RD}$	0	-	0	-	ns	
(3) tRR	$\overline{RD}$ Pulse Width	250	-	150	-	ns	
(4) tRD	Data Valid From $\overline{RD}$	-	200	-	120	ns	1
(5) tDF	Data Float After $\overline{RD}$	10	75	10	75	ns	2
(6) tRV	Time Between $\overline{RD}$s and/or $\overline{WR}$s	300	-	300	-	ns	
WRITE TIMING							
(7) tAW	Address Stable Before $\overline{WR}$	0	-	0	-	ns	
(8) tWA	Address Stable After $\overline{WR}$	20	-	20	-	ns	
(9) tWW	$\overline{WR}$ Pulse Width	100	-	100	-	ns	
(10) tDW	Data Valid to $\overline{WR}$ High	100	-	100	-	ns	
(11) tWD	Data Valid After $\overline{WR}$ High	30	-	30	-	ns	
OTHER TIMING							
(12) tWB	$\overline{WR}$ = 1 to Output	-	350	-	350	ns	1
(13) tIR	Peripheral Data Before $\overline{RD}$	0	-	0	-	ns	
(14) tHR	Peripheral Data After $\overline{RD}$	0	-	0	-	ns	
(15) tAK	ACK Pulse Width	200	-	200	-	ns	
(16) tST	STB Pulse Width	100	-	100	-	ns	
(17) tPS	Peripheral Data Before STB High	20	-	20	-	ns	
(18) tPH	Peripheral Data After STB High	50	-	50	-	ns	
(19) tAD	ACK = 0 to Output	-	175	-	175	ns	1
(20) tKD	ACK = 1 to Output Float	20	250	20	250	ns	2
(21) tWOB	$\overline{WR}$ = 1 to OBF = 0	-	150	-	150	ns	1
(22) tAOB	ACK = 0 to OBF = 1	-	150	-	150	ns	1
(23) tSIB	STB = 0 to IBF = 1	-	150	-	150	ns	1
(24) tRIB	$\overline{RD}$ = 1 to IBF = 0	-	150	-	150	ns	1
(25) tRIT	$\overline{RD}$ = 0 to INTR = 0	-	200	-	200	ns	1
(26) tSIT	STB = 1 to INTR = 1	-	150	-	150	ns	1
(27) tAIT	ACK = 1 to INTR = 1	-	150	-	150	ns	1
(28) tWIT	$\overline{WR}$ = 0 to INTR = 0	-	200	-	200	ns	1
(29) tRES	Reset Pulse Width	500	-	500	-	ns	1, (Note)

NOTE: Period of initial Reset pulse after power-on must be at least 50μsec. Subsequent Reset pulses may be 500ns minimum.

VOLTAGE REGULATORS :

Positive Voltage Regulators in 7800 series

IC Part	Output Voltage (V)	Minimum Vi (V)
7805	+5	7.3
7806	+6	8.3
7808	+8	10.5
7810	+10	12.5
7812	+12	14.6
7815	+15	17.7
7818	+18	21.0
7824	+24	27.1

Electrical Characteristics LM78XXC (Note 2)

0°C ≤ T_J ≤ 125°C unless otherwise noted.

Output Voltage				5V			12V			15V			Units
Input Voltage (unless otherwise noted)				10V			19V			23V			
Symbol	Parameter	Conditions		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_O	Output Voltage	Tj = 25°C, 5 mA ≤ I_O ≤ 1A		4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
		P_D ≤ 15W, 5 mA ≤ I_O ≤ 1A		4.75		5.25	11.4		12.6	14.25		15.75	V
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(7.5 ≤ V_{IN} ≤ 20)			(14.5 ≤ V_{IN} ≤ 27)			(17.5 ≤ V_{IN} ≤ 30)			V
ΔV_O	Line Regulation	I_O = 500 mA	Tj = 25°C		3	50		4	120		4	150	mV
			ΔV_{IN}	(7 ≤ V_{IN} ≤ 25)			14.5 ≤ V_{IN} ≤ 30)			(17.5 ≤ V_{IN} ≤ 30)			V
			0°C ≤ Tj ≤ +125°C			50			120			150	mV
			ΔV_{IN}	(8 ≤ V_{IN} ≤ 20)			(15 ≤ V_{IN} ≤ 27)			(18.5 ≤ V_{IN} ≤ 30)			V
		I_O ≤ 1A	Tj = 25°C			50			120			150	mV
			ΔV_{IN}	(7.5 ≤ V_{IN} ≤ 20)			(14.6 ≤ V_{IN} ≤ 27)			(17.7 ≤ V_{IN} ≤ 30)			V
			0°C ≤ Tj ≤ +125°C			25			60			75	mV
			ΔV_{IN}	(8 ≤ V_{IN} ≤ 12)			(16 ≤ V_{IN} ≤ 22)			(20 ≤ V_{IN} ≤ 26)			V
ΔV_O	Load Regulation	Tj = 25°C	5 mA ≤ I_O ≤ 1.5A		10	50		12	120		12	150	mV
			250 mA ≤ I_O ≤ 750 mA			25			60			75	mV
		5 mA ≤ I_O ≤ 1A, 0°C ≤ Tj ≤ +125°C				50			120			150	mV
I_Q	Quiescent Current	I_O ≤ 1A	Tj = 25°C			8			8			8	mA
			0°C ≤ Tj ≤ +125°C			8.5			8.5			8.5	mA
ΔI_Q	Quiescent Current Change	5 mA ≤ I_O ≤ 1A				0.5			0.5			0.5	mA
		Tj = 25°C, I_O ≤ 1A				1.0			1.0			1.0	mA
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(7.5 ≤ V_{IN} ≤ 20)			(14.8 ≤ V_{IN}≤ 27)			(17.9 ≤ V_{IN} ≤ 30)			V
		I_O ≤ 500 mA, 0°C ≤ Tj ≤ +125°C				1.0			1.0			1.0	mA
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(7 ≤ V_{IN} ≤ 25)			(14.5 ≤ V_{IN}≤ 30)			(17.5 ≤ V_{IN} ≤ 30)			V
V_N	Output Noise Voltage	T_A =25°C, 10 Hz ≤ f ≤ 100 kHz			40			75			90		µV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz	I_O ≤ 1A, Tj = 25°C or	62	80		55	72		54	70		dB
			I_O ≤ 500 mA 0°C ≤ Tj ≤ +125°C	62			55			54			dB
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(8 ≤ V_{IN} ≤ 18)			(15 ≤ V_{IN} ≤ 25)			(18.5 ≤ V_{IN} ≤ 28.5)			V
R_O	Dropout Voltage	Tj = 25°C, I_{OUT} = 1A			2.0			2.0			2.0		V
	Output Resistance	f = 1 kHz			8			18			19		mΩ

Electrical Characteristics LM78XXC (Note 2) (Continued)

$0°C \le T_J \le 125°C$ unless otherwise noted.

Output Voltage			5V			12V			15V			Units
Input Voltage (unless otherwise noted)			10V			19V			23V			
Symbol	Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Short-Circuit Current	$T_J = 25°C$		2.1			1.5			1.2		A
	Peak Output Current	$T_J = 25°C$		2.4			2.4			2.4		A
	Average TC of V_{OUT}	$0°C \le T_J \le +125°C$, $I_O = 5$ mA		0.6			1.5			1.8		mV/°C
V_{IN}	Input Voltage Required to Maintain Line Regulation	$T_J = 25°C$, $I_O \le 1A$		7.5		14.6			17.7			V

Note 1: Thermal resistance of the TO-3 package (K, KC) is typically 4°C/W junction to case and 35°C/W case to ambient. Thermal resistance of the TO-220 package

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REFERENCES

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