SINGLE PHASE HIGH FREQUENCY RESONANT INVERTER

A PROJECT REPORT

Submitted by

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in

ELECTRICAL AND ELECTRONICS ENGINEERING

Under the guidance of

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BONAFIDE CERTIFICATE

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ABSTRACT

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In the conventional DC/AC converters, the controllable switches are operated in a switch mode and are required to turn on and off the entire load current during each switching. This results in the switches being subject to high switching stresses and switches losses. The switching losses can be minimized if each switch changes its status from on to off or vice versa when the voltage across it and/or current through it is zero at the switching instant. This is accomplished using a **Resonant Inverter**.

In the project entitled "SINGLE PHASE HIGH FREQUENCY RESONANT INVERTER" the concept of Resonant DC Link Inverter (RDCLI) is proposed and realized with the addition of an inductor and a capacitor to a conventional voltage source inverter circuit. In order to increase the power density of the inverter, high frequency operation is preferred.

This project deals with the design and implementation of constant high frequency resonant DC link inverter (RDCLI) for industrial and domestic appliances. The entire circuit is modeled and simulated using MATLAB/SIMULINK and implemented in hardware.

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INTRODUCTION

1.1 EXISTING SYSTEM

Advances in the semiconductor technology have led to the use of switched mode power supplies in the last two decades. Because of their higher efficiency, small size and weight, relatively low cost and step-up/step-down ability, they are fast replacing the linear mode supplies (Mohan et al 1995). PWM converters are widely used for obtaining controllable DC voltage from a fixed DC.

1.2 LIMITATIONS OF THE EXISTING SYSTEM

Today, the power converter topology of choice for ac output applications is the 'hard switching' dc/ac voltage source inverter. The ac output voltage is synthesized using a pulse width modulated (PWM) switching waveform, which has a controlled amplitude low-frequency 'fundamental' component, and high-frequency modulation components. . The modulation components of the current are filtered by the low pass characteristic of typical inductive power electronic loads.

In PWM converters, the controllable switches are operated in a switch mode where they are required to turn on and turn off the entire load current during each switching. In this switch mode operation, the switches are subjected to high switching stresses and high switching power loss that increases linearly with the switching frequency of the PWM. The power

density is and important selection of an inverter for industrial, telecommunication and aerospace applications.

1.3 PROPOSED SYSTEM

The power density can be improved by increasing the switching frequency. A key factor in reducing the size of reactive components used for filtering and energy storage, improving transient performance and meeting stringent harmonic specifications is the switching frequency of the inverter. Although switching rapidly occurs, switching losses occur during device turn-on and turn-off due to the transient existence of both voltage across, and current in the device. These stresses require significant device derating for switching frequencies in excess of 5 - 6 kHz, thus increasing system cost. So at higher frequencies, conventional PWM switched mode converters unsuitable because of high switching losses, high switching stresses, reduced reliability, Electromagnetic Interference (EMI) and acoustic noise (Mohan et al 1995). The presence of leakage inductance and junction capacitance in the semiconductor devices cause the power devices to inductively turn-off and capacitively turn-on. When a semiconductor devices switches off an inductive load, voltage spikes induced by sharp di/dt across leakage inductance produce increased voltage stress and noise. Most switching converters owing to the rapid switching of voltage and current produce EMI.

1.4 PROJECT OVERVIEW

To improve switching conditions for semiconductor devices in power processing circuits, two resonant techniques were proposed. The first is the zero current switching technique. By incorporating an LC circuit, the current

waveform of the switching device is forced to oscillate in a quasi-sinusoidal manner, creating zero-current switching conditions during both turn-on and turn-off. By simply replacing the power switches in PWM converters with the resonant switch, family of zero current switched (ZCS) resonant DC link inverters (RDCLI) has been derived. This new family of circuits can be viewed as a hybrid of PWM and resonant converters. RDCLIs utilize the principle of inductive or capacitive energy storage and transfer in a manner similar to PWM converters and their circuit topologies also resemble those of PWM converters. However an LC tank circuit is always present near the power switch and is used not only to shape the current and voltage waveforms of the power switch, but also to store and transfer energy from the input to the output in a manner similar to the conventional resonant inverters.

The second resonant technique is zero voltage switching technique. By using an LC resonant network, the voltage waveform of the switching device can be shaped into a quasi-sine wave such that zero voltage condition is created for the switch to turn on and turn off without incurring only switching loss. This technique eliminates the turn on loss associated with the parasitic output capacitance of the power switch.

The recent advances in modern power semiconductor device technologies have led to high utilization of power converters in a large number of applications and have opened up a host of new converter topologies for many new applications. The most visible gain in industrial and commercial products is occurring in the area of power inverters, which convert a dc voltage into a single or polyphase ac voltage at a desired

amplitude and frequency. Technology advances in these areas have arisen primarily from improvements in semiconductor power devices.

High frequency power can be found widespread applications in such as motor drives induction heating, fluorescent lighting. By operating the power system at high frequency, the system can be made compact because of the large reduction in the size and weight of the transformers, reactors, capacitors and circuit breakers. Use of high frequency also speeds up system response and offers high quality power. Moreover newly developed materials such as amorphous metal and low dielectric loss materials can be used much effectively than in the conventional 50/60 Hz power system. It is important to select a proper frequency; frequencies ranging from 400 Hz to 12 KHz can be found most interesting applications both today and in the near future. The high frequency power can find many applications both in industrial and commercial utilization such as ultra speed motors, induction heating and fluorescent lighting.

PROJECT DESCRIPTION AND METHODOLOGIES

CHAPTER 2

PROJECT DESCRIPTION AND METHODOLOGIES

To avoid the switching loss in the inverter a new topology has been proposed, where a resonant circuit is introduced in-between the dc input voltage and the inverter. It has been realized with the addition of only one small inductor and capacitor to a conventional voltage source inverter circuit. The resonant converter is capable of switching at the high frequency. It is extremely important to realize that if the switching environment could be modified to ensure zero switching losses. Zero switching losses could be obtained by holding the dc bus voltage at zero volts for the duration of the switching transient. An elegant method for attaining the desired objective is to make the dc bus oscillatory, ensuring that the voltage remains at zero for sufficient time to allow lossless switching to take place.

2.1 RESONANT DC LINK INVERTER

The basic version of the resonant dc link inverter is shown in Fig. 2.1

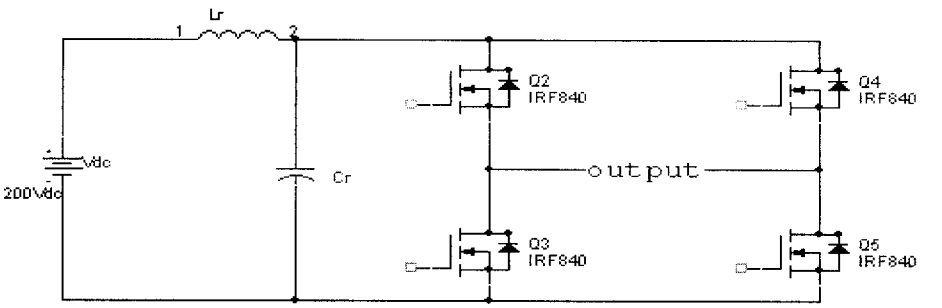


Fig. 2.1 Resonant DC Link Inverter (RDCLI)

In the RDCLI, the voltage across the resonant capacitor is also impressed across the six power devices. This voltage has an average or dc value which is equal to the dc bus, V_{dc}, and an oscillating or resonant component. The combined voltage is referred to as the resonant link. The resonant link is 'excited' and maintains resonance through appropriate control of the inverter switches such that the resonating dc bus voltage periodically reaches zero volts. Switching of the devices is synchronized to the link zero crossings to obtain the desired low switching loss.

The main inverter devices are only allowed to change state at the link voltage zero crossings. This force the inverter output to consist of an integral number of resonant link voltage pulses, a significantly different strategy from the pulse width modulation used in conventional hard switching inverters. The desired low frequency output voltage now has to be synthesized using discrete resonant pulses, using a discrete pulse modulation (DPM) strategy. Typical low voltage synthesis is shown in Fig.2.2

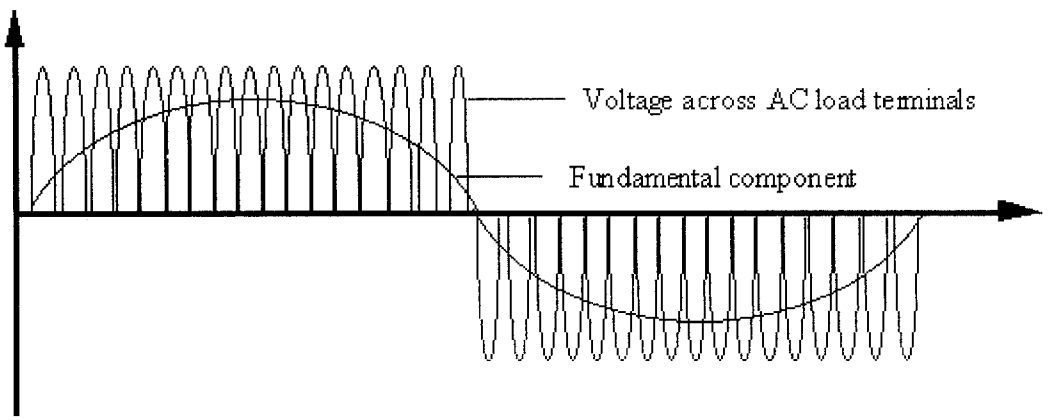


Fig. 2.2 Typical line-to-line voltage synthesis using DPM

In order to simplify the analysis of a RDCLI and since the resonant frequency is much higher than the fundamental frequency of the synthesized waveform, an equivalent circuit of the system during each resonant pulse is shown in Fig. 2.3. Note here that the load current I_x, is assumed to be constant during resonant pulse duration.

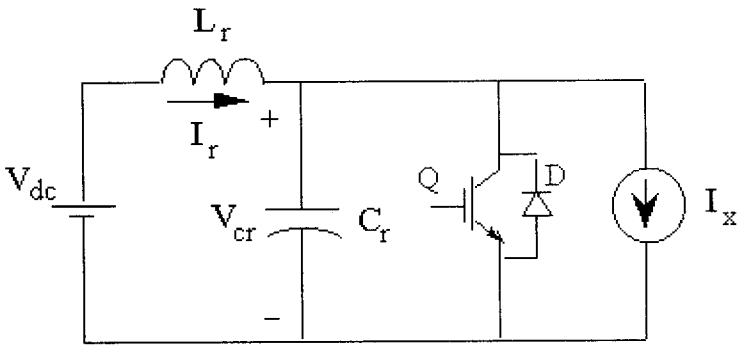


Fig. 2.3 Equivalent circuit of the RDCLI during each resonant pulse]

If the switch Q is turned off, applying V_{dc} to the circuit results in a resonant cycle and the capacitor voltage V_{cr} is given by,

$$V_{cr}(t) = V_{dc}\,(1-\cos\omega t)$$

where ω is the resonant frequency of the LC circuit. When $\omega t=2\Pi$, the capacitor voltage goes back to zero setting up a zero voltage switching condition for the switch Q. When the switch is turned on, the inductor current will ramp up in a linear fashion. Sufficient energy has to be stored in L_r before the switch is turned off to ensure that the capacitor voltage will return to zero. Typical waveforms with zero load current are shown in Fig. 2.4.

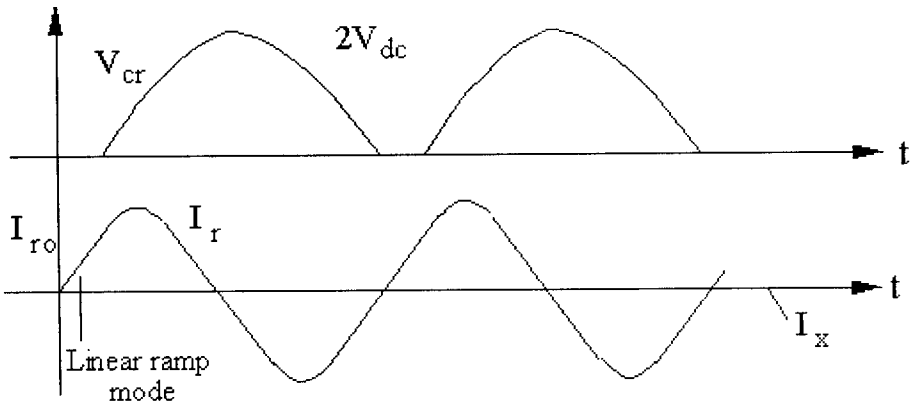


Fig. 2.4 Typical waveforms of the RDCLI with Ix=0

The value of the current I_x depends on the individual phase currents and the switching functions of the six inverter devices. Note here that I_x can change significantly from a switching cycle to the next depending on the switching strategy. However, during the resonant cycle itself, I_x remains fairly constant since the inverter states are preserved. In order to ensure ZVS, the inverter actively controls the current (I_r-I_x) to ensure that the resonant cycle starts with the same initial conditions. Hence, the resonant cycle is controlled in a dead beat fashion and is independent of the value of I_x.

2.2 SIMULATION

2.2.1 NEED FOR SIMULATION

New designs of power electronics systems are the norm due to new applications and the lack of standardization in specifications is because of

varying customer demands. Accurate simulation is necessary to minimize costly repetitions of designs and bread boarding and, hence, reduce the overall cost and the concept-to-production time.

There are many benefits of simulation in the design process, some of which are listed here

- Simulation is well suited for educational purposes. It is an efficient way for designer to learn how a circuit and its control work.

- Simulation may give a comprehensive and an impressive documentation of system performance that gives a competitive edge to a company using the simulation.

- It is normally much cheaper to do a thorough analysis than to build the actual circuit in which component stresses are measured. A simulation can discover possible problems and determine optimal parameters, increasing the possibility of getting the prototype "right the first time". Simulation can be used to optimize the performance objective by letting the simulation search over a large number of variables.

- New circuit concepts and parameter variations (including tolerances on components) are easily tested. Changes in the circuit topology are implemented at no cost. There is no need for components to be available on short notice.

- In the initial phase of a study, parasitic effects such as start capacitances and leakage inductances are best omitted. They are important and must be considered, but they often cause confusion until the fundamental principles of a concept are understood. In a physical circuit, it is not possible to remove the stray capacitance and leakage inductances in order to get down to the fundamental behavior of the system.

- Simulated waveforms at different places in the circuit are easily monitored with out the hindrance of measurement noise (and other noise sources). As switching frequencies increases, the problem of laboratory measurements becomes increasingly difficult. Thus, simulations may become more accurate than measurement.

- Destructive tests that cannot be done in the laboratory, either because of safety or because of the costs involved, can easily be simulated. Responses to faults and abnormal conditions can also be thoroughly analyzed.

- Specification of components voltage and current ratings is difficult before the working principles of the circuit and the current and voltage waveforms are fully determined. In a simulation, component ratings are not needed.

- It is possible to simplify parts of circuits in order to focus on a specific portion of the circuit. This may not be possible in a laboratory setup.

- There may be a need to predict the interaction between several converters connected to the same distribution network. This will be almost impossible and certainly very expensive to do without simulation.

2.2.2 REQUIREMENTS FOR A SIMULATION

Simulation of power electronics and motion control systems poses many challenges to the simulation program and it user. These are discussed in the following subsections.

User friendly interface: A simulation program must have an easy to use interface for data entry and for output data processing.

Multilevel modeling capability: In simulating the motor drive example of the power electronics converters are described in the interconnection of circuit element models. On the other hand, the electrical machine and the load are best described by differential equations formulated in terms of state variables. Finally, the continuous and sampled data control systems are often represented in their functional form by transfer functions and/or logic statements that describe the behavior properties between their inputs and outputs. A good simulation program should allow these various locks to be easily implemented.

Accurate models: For a detailed analysis, a simulation program needs accurate models of all circuit elements, including transformers and transmission lines for utility related applications. Even if accurate models

are available, if it is difficult to know their parameter values. Parasitic inductances and capacitances are often difficult to estimate.

Robust switching operations: Switching actions due to solid state switches (diodes, thyristors, and transistors) must be appropriately handled. Depending on how the switches are modeled, their on-off transitions either represent an extreme nonlinearity or lead to a time-varying structure of the network.

Execution time: the simulation many need to cover a sufficiently large time span to observe the effect of slowly changing variables with large time constants. At the same time, the simulation often needs to precede with small a small time step in order to accurately represent rapidly changing variables with small time constants. A small time step is also required to represent switching times with good resolution in the presence of high switching frequencies. In such simulation, this leads to a large number of time steps. To keep the execution time within reasonable limits, an efficient equation solver with variables time steps is normally required.

Initial conditions: Unlike small-signal electronics, where the steady-state operating conditions are established by a DC bias analysis, there is no easy way to establish the steady-state operating conditions in a power electronics system. Often, an initial estimate of various state variables is provided by the user, and the time required to bring the system to its steady state may be substantial, depending on the accuracy of the initial estimates. Therefore, simulation programs for power electronics must allow user to set initial conditions.

2.2.3 SIMULATION SOFTWARES

The general software packages used to simulate the power electronics circuits are

- PSPICE
- ORCAD
- Lab view
- MATLAB
- Multisim

The software tool we have used to simulate the power circuit is MATLAB/SIMULINK 6.5.

2.2.4 MATLAB/SIMULINK

If we choose an equations solver, we must ourselves write the differential and algebraic equations to describe various circuit states, the logical expressions, and the controller that determine the circuit state. Then, these differential/algebraic equations are simultaneously solved as a function of time.

In the most basic form, we can solve these equations by programming in any one of the higher level languages such as FORTRAN, C or PASCAL. It is also possible to access libraries in any of these languages which consist of subroutines for specific applications such as to carry out integration or matrix inversion. However, it is far more convenient to use a package such as MATLAB or a host of other packages where many of these convenience

features are built in it. Each of these packages uses its own syntax and also excels in certain applications.

The program MATLAB can easily perform array and matrix manipulations, where for example y=a.*b results in y, which equals cell by cell multiplication of two arrays a and b. Similarly, to invert a matrix, all one needs to specify is y=inv(X). Powerful plotting routines are built in. MATLAB also features various libraries, called toolboxes, which can be used to solve particular classes' problems. For example, the neural network toolbox enables the simulation of an unlimited number of layers and interconnections. Neurons can be modeled with sigmoid, linear, limit, or competitive transfer functions. The toolbox contains functions for implementing a number of networks, including back propagation, Hopfield, and Widrow-hoff networks.

Simulink is another toolbox for graphical entry and simulation of nonlinear dynamic systems. It consists of a large number of building blocks that enables the simulation of control based systems. Some of the other features include seven integration routines and determination of equilibrium points.

MATLAB is widely used in industry. Also, such programs are used in the teaching of undergraduate courses in control systems and signal processing. Therefore, the students are usually familiar with MATLAB prior to taking power electronics courses. Even if this is not the case, it is possible to learn its use quickly, especially by means of examples.

The single phase simulations of the high frequency resonant inverter are shown in figures 2.5, 2.6, 2.7 below.

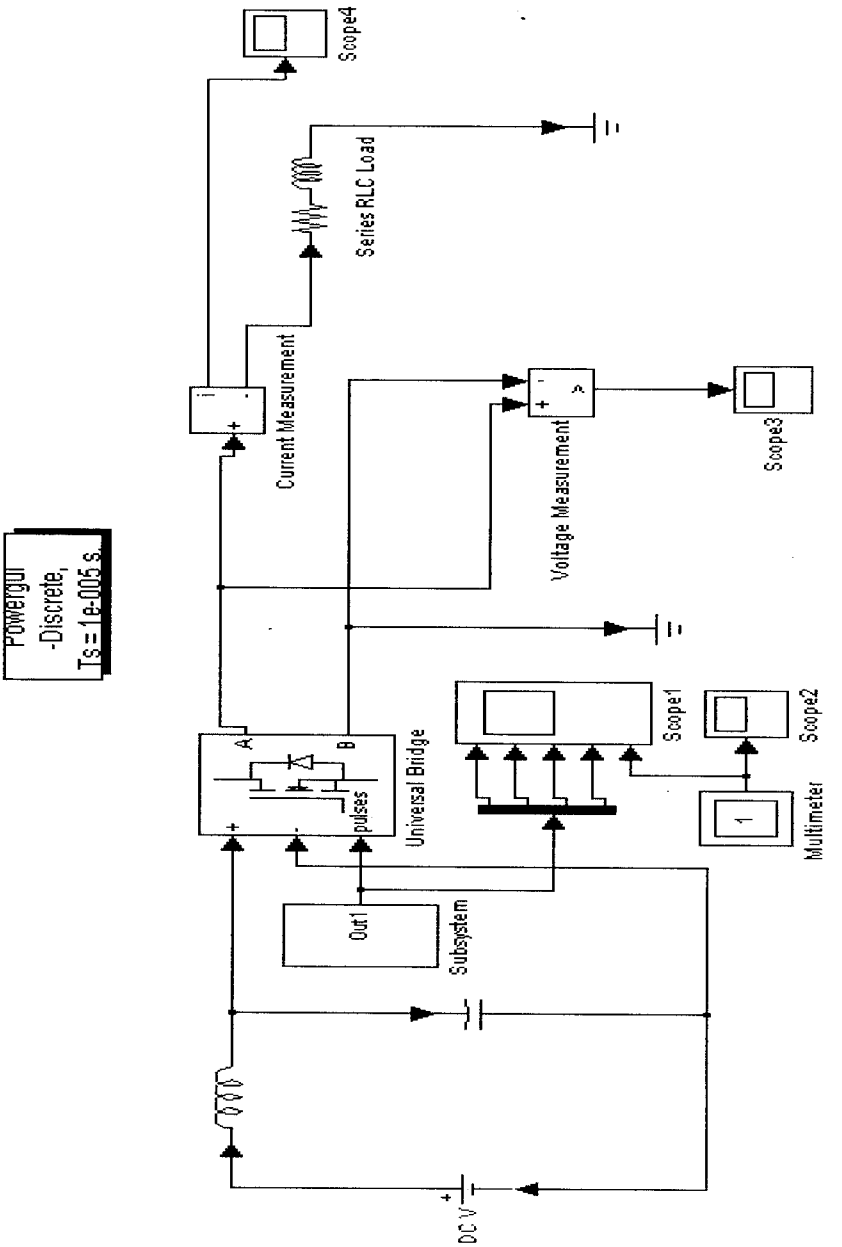


Fig. 2.5 Single Phase Simulation Model Circuit

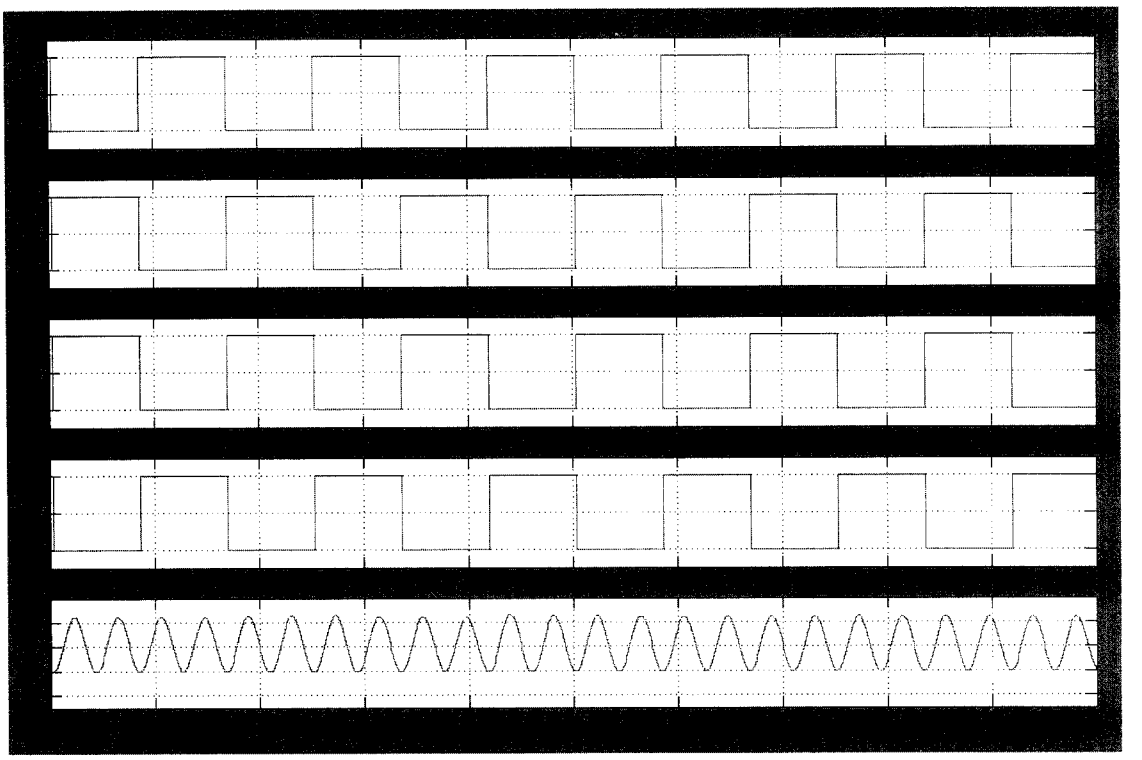


Fig 2.6 Gate pulse Signal waveform

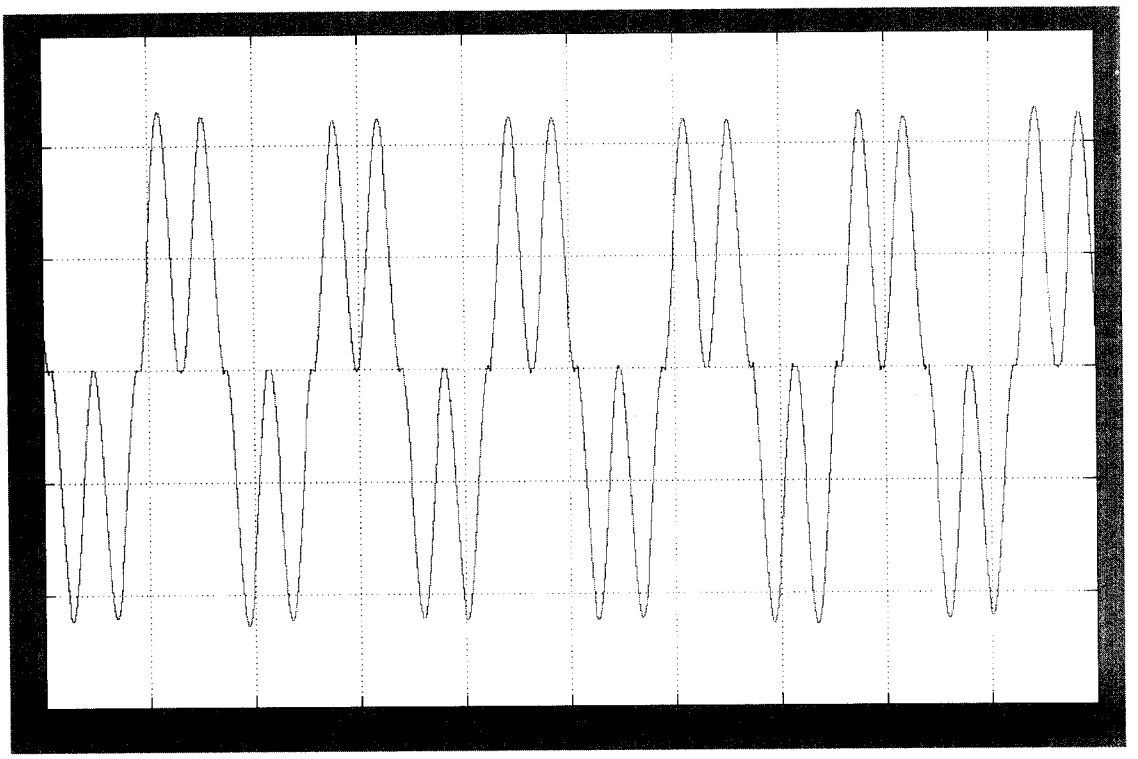


Fig 2.7 Single phase output waveform

The three phase simulations of the high frequency resonant inverter are shown in figures 2.8, 2.9 and 2.10 below. These simulations have not been implemented in hardware.

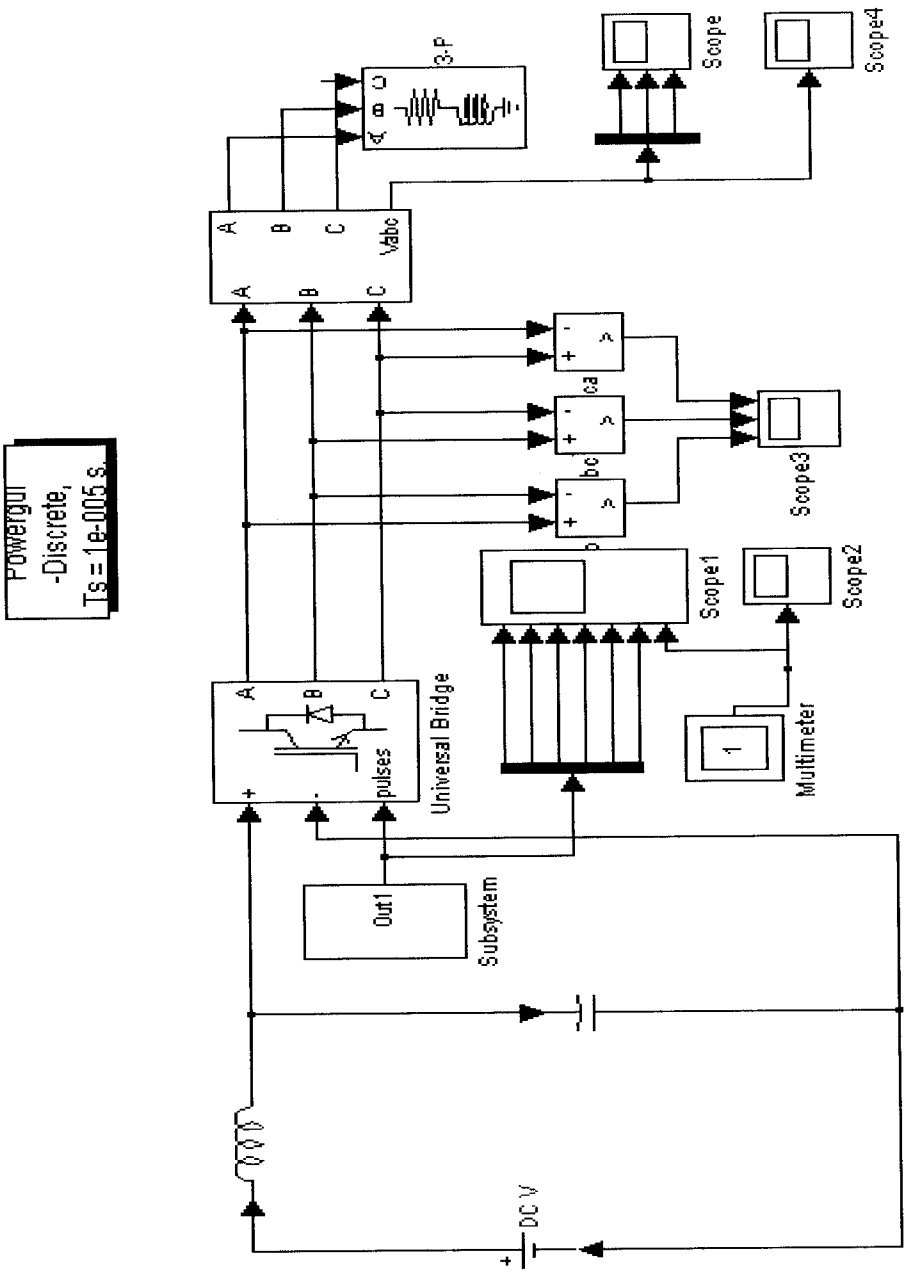


Fig. 2.8 Three Phase Simulation Model Circuit

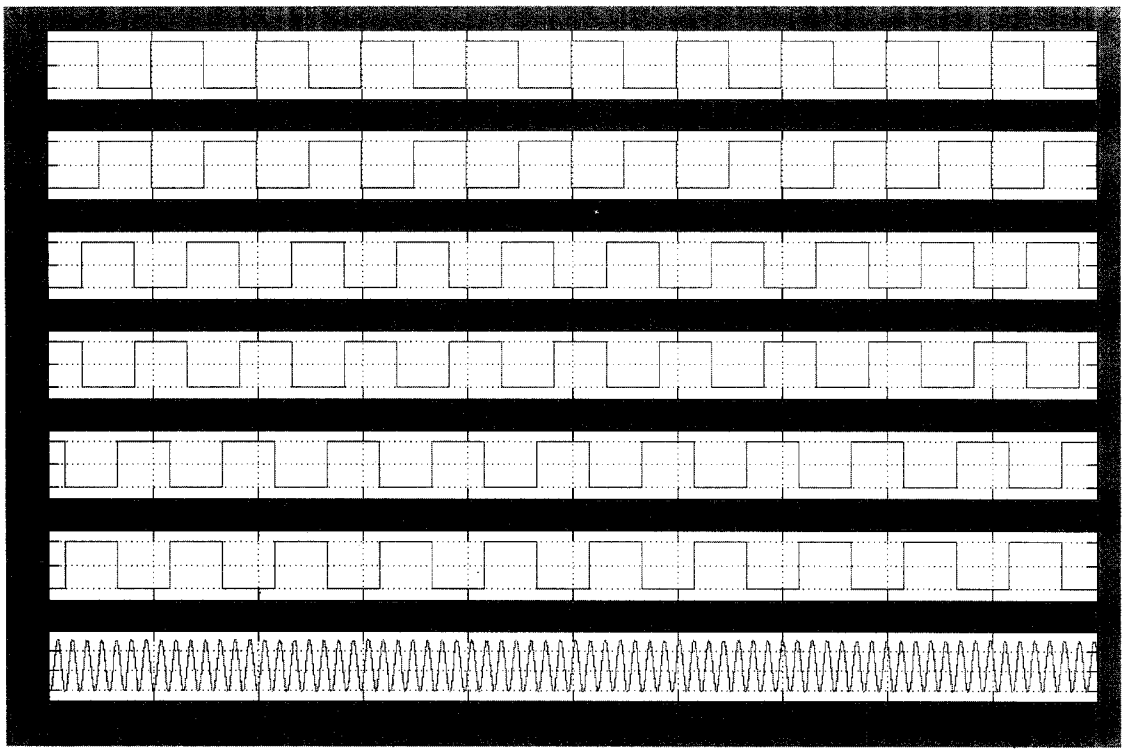


Fig 2.9 Gate pulse signal waveform

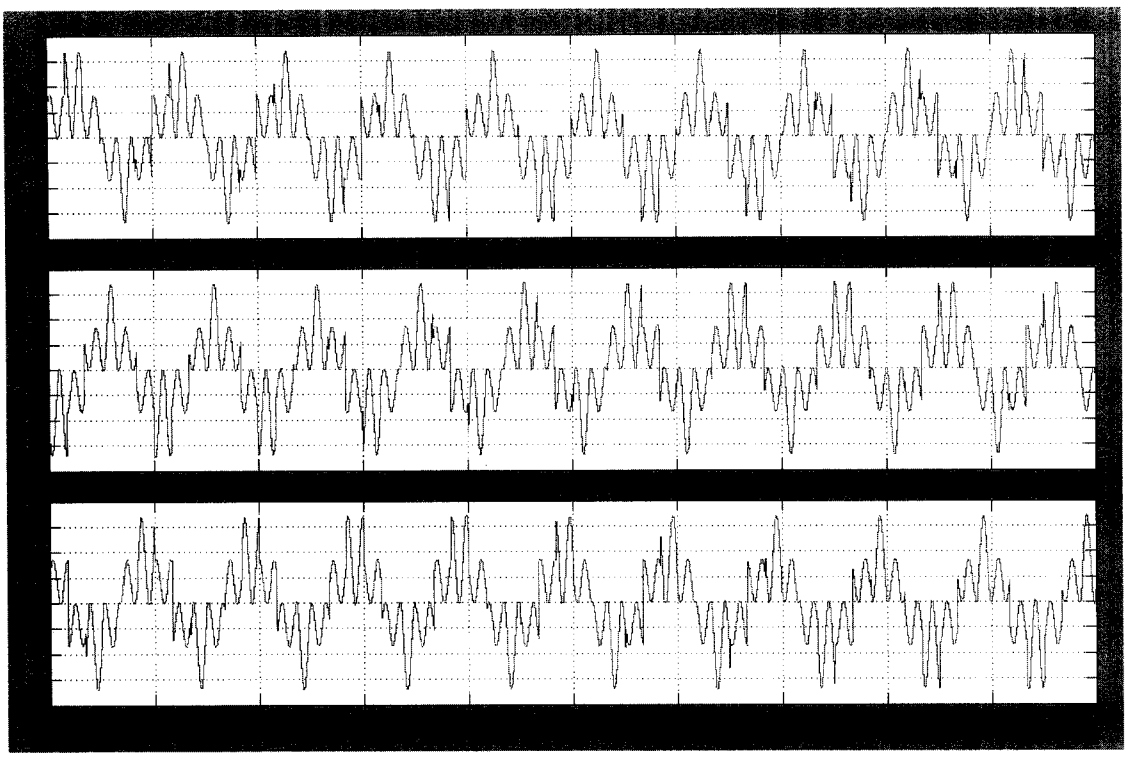


Fig 2.10 Three phase output waveform

2.3 BLOCK DIAGRAM

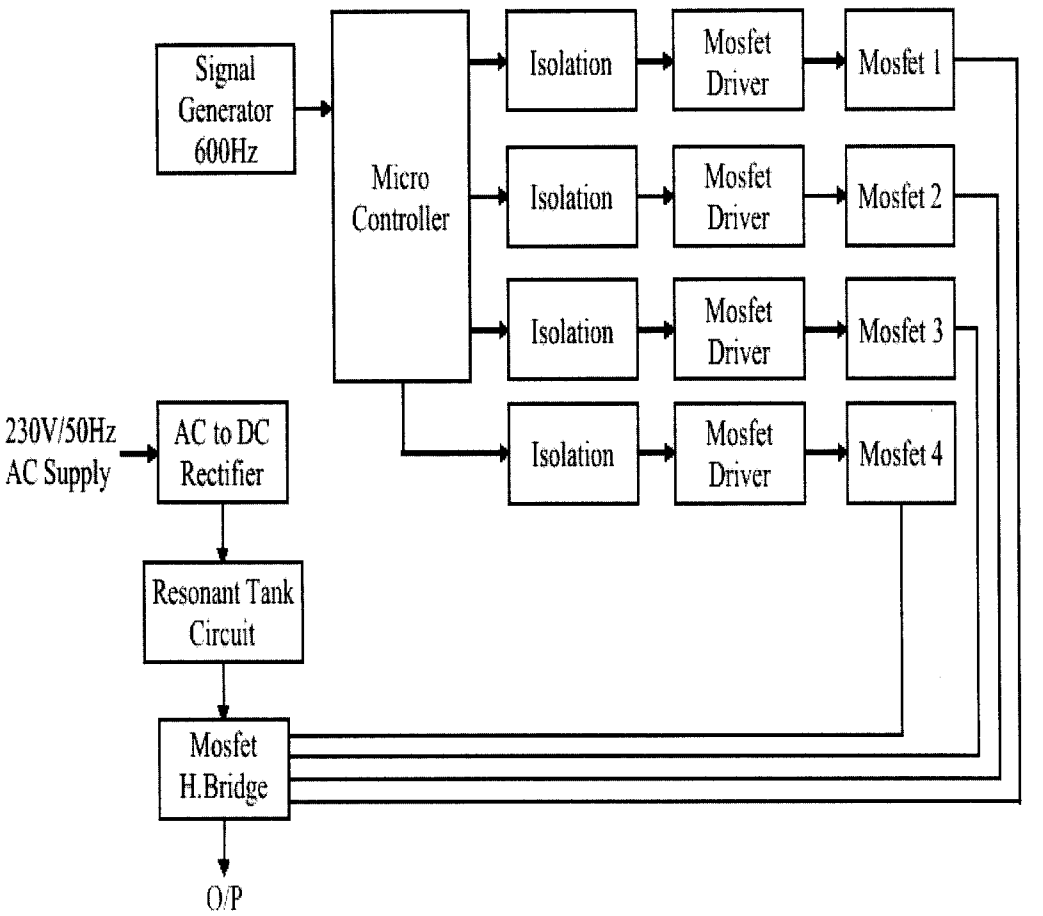


Fig. 2.11 Block Diagram

2.3.1 DESCRIPTION

The basic block diagram is shown in figure 2.11. The input supply to the module is 230V, 50Hz AC supply. This AC supply is rectified by a full wave rectifier. The rectified DC output is given to the designed resonance components: Inductor, L and Power Capacitor, C. This LC tank circuit is nothing but a parallel resonating circuit whose purpose is not only to shape the current and voltage waveforms of the power switch, but also to store and transfer energy from the input to the output under resonance condition. The MOSFET H-bridge inverter section is fed from the parallel resonance tank circuit. The MOSFET's are standard IRF840 series components which are used in the H-bridge section. The output of the inverter is taken across the mid of the H-bridge section.

In the MOSFET gate driver circuit, the variable frequency is achieved by means of IC4046 Voltage Controlled Oscillator (VCO). The Microcontroller 89C2051 is programmed in such way as to give suitable delay time to the MOSFET switching in order to avoid any cross conduction.

Safer and complete isolation to the MOSFET Driver circuit from the power inverter module is the most important criteria to be met in a high frequency switching operation. The isolation circuit consists of standard 6N135 optocouplers. The outputs of optocouplers are fed to IC7667 which is a dual monolithic high-speed driver which converts TTL signals into high current outputs at voltages upto 15V. This section produces the required gate current in order to drive the MOSFET's efficiently and effectively.

2.4 COMPONENT CHARACTERISTICS

2.4.1 POWER MOSFETs

The Power MOSFET symbol is shown in Fig. 2.12

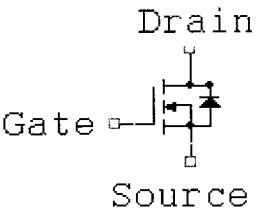


Fig. 2.12 MOSFET symbol

The power MOSFET is a voltage controlled device and requires only a small input current. In this device, the control signal is applied to a metal gate electrode that is separated from the semiconductor surface by an intervening insulator, typically silicon dioxide. The control signal required is essentially a bias voltage with no significant steady-state gate current flow in either the on-state or the off-state. Even during the switching of the deices between these states, the gate current is small at typical operating frequencies because it only serves to charge and discharge the input gate capacitance, the high input impedance is primary feature of the power MOSFET that greatly simplifies the gate drive circuitry and reduces the cost of the power-electronics.

The power MOSFET is a unipolar device. Current conduction occurs through transport of majority carriers in the drift region without the presence

of minority carrier injection required for bipolar transistor operation. In this device, during turn-off, no delays are observed as a result of storage or recombination of minority carriers. Their inherent switching speed is orders of magnitude faster than that for bipolar transistors. This feature is particularly attractive in circuits operating at high frequencies where switching power losses are dominant. The power MOSFET having operating frequencies are well above 100 KHz. The power MOSFETs switching timing is in order of 50-100 nanoseconds and can generate many kilowatts of power at frequencies to 500 KHz.

❖ SWITCHING CHARACTERISTICS

The switching characteristics of a power MOSFET are determined largely by the various capacitances inherent in its structure. These are shown in Fig.8. To turn the device on and off the capacitances have to be charged and discharged, the rate at which this can be achieved is dependent on the impedance and the current sinking/sourcing capability of the drive circuit. Since it is only the majority carriers that are involved in the conduction process, MOSFETs do not suffer from the same storage time problems which limit bipolar devices where minority carriers have to be removed during turn-off. For most applications therefore the switching times of the Power MOSFET are limited only by the drive circuit and can be very fast. Temperature has only a small effect on device capacitances therefore switching times are independent of temperature. The Internal Capacitances are shown in Fig. 2.13.

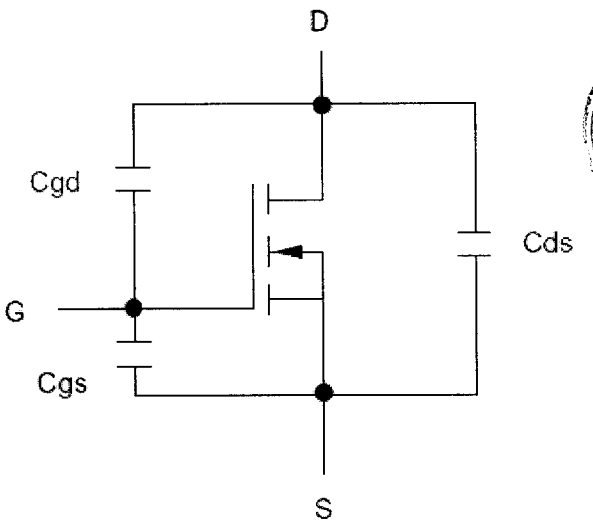


Fig.2.13 Internal Capacitances of Depletion MOSFET

In Fig.2.14 typical gate-source and drain-source voltages for a MOSFET switching current through a resistive load are shown. The gate source capacitance needs to be charged up to a threshold voltage of about 3 V before the MOSFET begins to turn on. The time constant for this is $C_{GS}(R_{DR}+R_G)$ and the time taken is called the turn-on delay time ($t_D(ON)$). As V_{GS} starts to exceed the threshold voltage the MOSFET begins to turn on and V_{DS} begins to fall. C_{GD} now needs to be discharged as well as C_{GS} being charged so the time constant is increased and the gradient of V_{GS} is reduced. As V_{DS} becomes less than V_{GS} the value of C_{GD} increases sharply since it is depletion dependent. A plateau thus occurs in the V_{GS} characteristic as the drive current goes into the charging of C_{GD}.

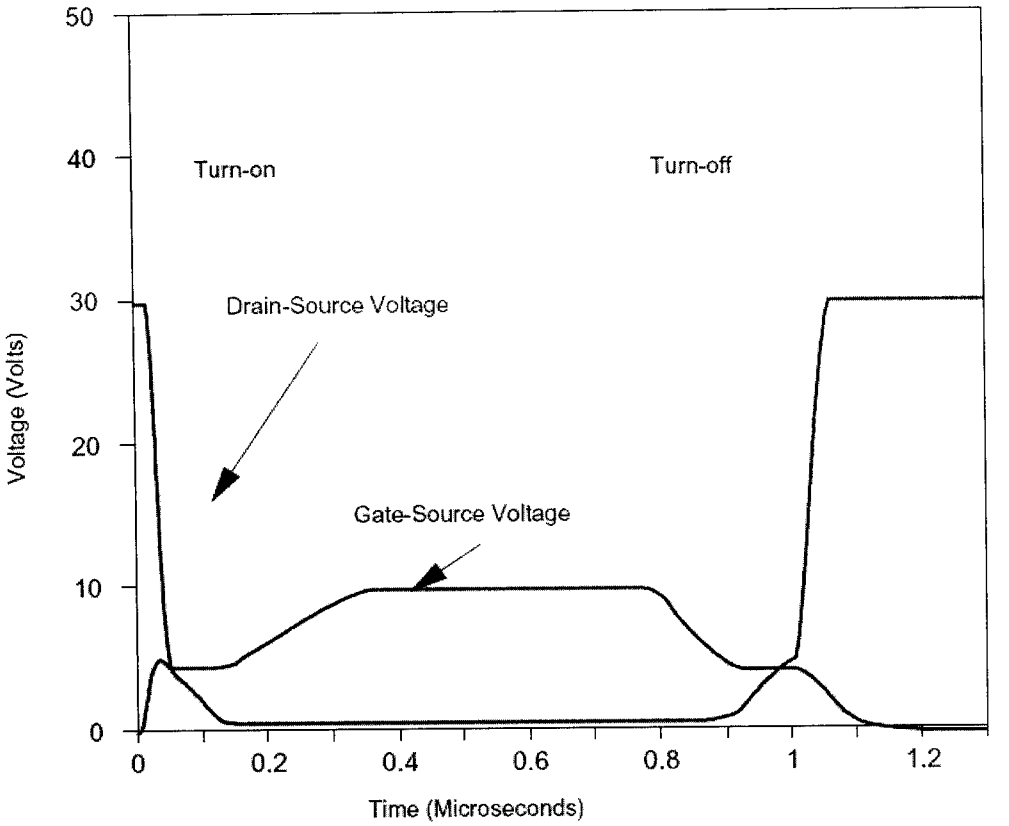


Fig.2.14 The switching waveforms for a MOSFET

When V_{DS} has collapsed V_{GS} continues to rise as overdrive is applied. Gate overdrive is necessary to reduce the on-resistance of the MOSFET and thereby keep power loss to a minimum. To turn the MOSFET off the overdrive has first to be removed. The charging path for C_{GD} and C_{DS} now contains the load resistor (R_L) and so the turn-off time will be generally longer than the turn-on time.

❖ MOSFET TURN-ON CHARACTERISTICS

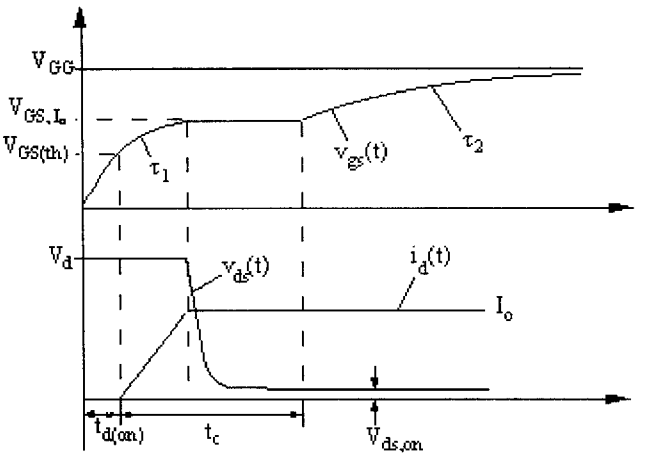


Fig.2.15 MOSFET turn-on characteristics

The turn-on behavior of the MOSFET is shown in Fig.2.15. As shown in this figure, the gate drive voltage changes in step function manner from 0 to V_{GG} which is above the threshold voltage $V_{GS}(th)$. During the turn on delay time t_d (on) the gate-source voltage V_{gs} rises from 0 to $V_{GS}(th)$ in fashion similar to an RC circuit. This is due to the resistance in the current path in addition to the equivalent input MOSFET capacitance (C_{gs} and C_{gd}). The rise time constant is given by $t1 = R_G (C_{gs} + C_{gd1})$. Beyond $V_{GS}(th)$, v_{gs} keeps rising as before and Ids starts increasing. Once the MOSFET is carrying the full load current I_o, the gate-source voltage becomes temporarily clamped at V_{gs},I_o. At this point, the gate current will flow through C_{gd} only. As a result, the drain-source voltage starts decreasing until it reaches the drop due to the on-state resistance. At this point, the gate-source voltage becomes unclamped and rises again to V_{GG} with a time constant of $t_2 = R_G (C_{gs} + C_{gd2})$. Note here that there are two values of C_{gd} due to the nonlinear nature of this capacitance.

❖ MOSFET turn-off characteristics

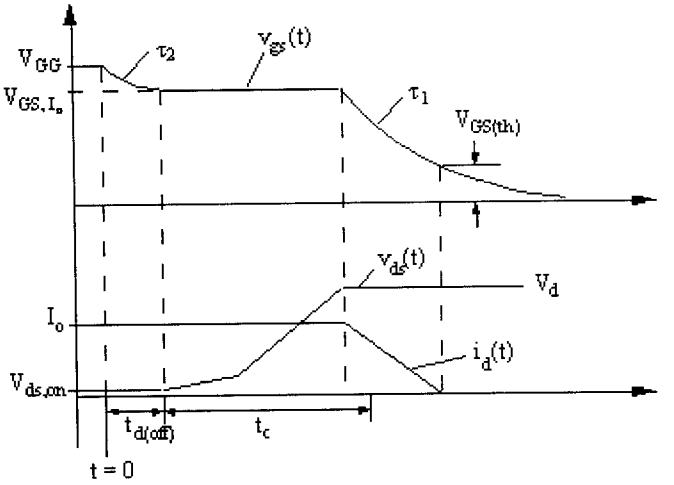


Fig.2.16 Turn-off characteristics of MOSFET

The turn-off of the MOSFET involves the inverse sequence of events that occurred during turn-on. This is shown in Fig.11. The turn-off process is initiated by applying a step gate voltage of -VGG.

❖ MOSFET PARAMETERS

On resistance, $R_{ds(on)}$.

This is the resistance between the source and drain terminals when the MOSFET is turned fully on.

Maximum drain current, $I_{d(max)}$.

This is the maximum current that the MOSFET can stand passing from drain to source. It is largely determined by the package and $R_{ds(on)}$.

Power dissipation, P_d.

This is the maximum power handling capability of the MOSFET, which depends largely on the type of package it is in.

Linear derating factor.

This is how much the maximum power dissipation parameter above must be reduced by per °C, as the temperature rises above 25°C.

Avalanche energy E_A

This is how much energy the MOSFET can withstand under avalanche conditions. Avalanche occurs when the maximum drain-to-source voltage is exceeded, and current rushes through the MOSFET. This does not cause permanent damage as long as the energy (power x time) in the avalanche does not exceed the maximum.

Peak diode recovery, dv/dt

This is how fast the intrinsic diode can go from the off state (reverse biased) to the on state (conducting). It depends on how much voltage was across it before it turned on. Hence the time taken, t = (reverse voltage / peak diode recovery).

Drain-to-Source Breakdown Voltage, V_{dss}.

This is the maximum voltage that can be placed from drain to source when the MOSFET is turned off.

Gate Threshold Voltage, $V_{GS(th)}$

This is the minimum voltage required between the gate and source terminals to turn the MOSFET on. It will need more than this to turn it fully on.

Forward transconductance, g_{fs}

As the gate-source voltage is increased, when the MOSFET is just starting to turn on, it has a fairly linear relationship between Vgs and drain current. This parameter is simply (Id / Vgs) in this linear section.

Input capacitance, C_{iss}

This is the lumped capacitance between the gate terminal and the source and drain terminals. The capacitance to the drain is the most important.

2.4.2 OPTO COUPLERS

An optocoupler is a combination of a light source and a photosensitive detector. In the optocoupler, or photon coupled pair, the coupling is achieved by light being generated on one side of a transparent insulating gap and being detected on the other side of the gap without an electrical connection between the two sides (except for a minor amount of coupling capacitance). In the optocouplers, the light is generated by an infrared light emitting diode, and the photo-detector is a silicon diode which drives an amplifier, e.g., transistor. The sensitivity of the silicon material peaks at the wavelength emitted by the LED, giving maximum signal coupling.

❖ OPTOCOUPLER 6N135

These high-speed optocouplers are designed for use in analog or digital interface applications that require high-voltage isolation between the input and output. Applications include line receivers that require high common-mode transient immunity and analog or logic circuits that require input-to-output electrical isolation. The 6N135 optocoupler each consists of a light-emitting diode and an integrated photon detector composed of a photodiode and an open-collector output transistor. Separate connections are provided for the photodiode bias and the transistor-collector output. This feature which reduces the transistor base-to-collector capacitance, results in speeds up to one hundred times that of a conventional phototransistor optocoupler. The 6N135 is designed for TTL/CMOS, TTL/LSTTL, and wide-band analog applications. The Optocoupler Schematic Diagram is shown in figure 2.17.

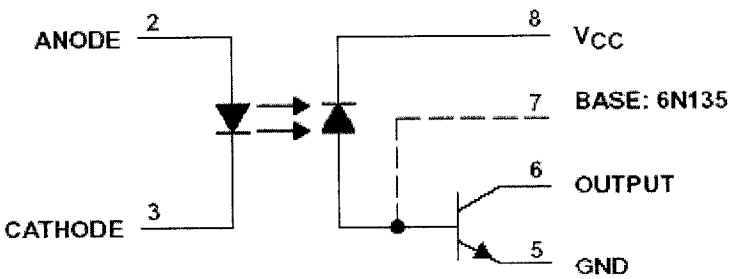


Fig.2.17 Optocoupler Schematic Diagram

The Optocoupler Pin Details are shown in figure 2.18.

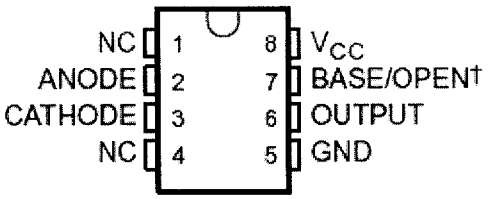


Fig.2.18 Optocoupler Pin Details

❖ DETAILED DESCRIPTION

The ICL7667 is a dual high-power CMOS inverter whose inputs respond to TTL levels while the outputs can swing as high as 15V. Its high output current enables it to rapidly charge and discharge the gate capacitance of power MOSFETs, minimizing the switching losses in switch mode power supplies. Since the output stage is CMOS, the output will swing to within milli volts of both ground and VCC without any external parts or extra power supplies as required by the DS0026/56 family. Although most specifications are at VCC = 15V, the propagation delays and specifications are almost independent of VCC. In addition to power MOS drivers, the ICL7667 is well suited for other applications such as bus, control signal, and clock drivers on large memory of microprocessor boards, where the load capacitance is large and low propagation delays are required. Other potential applications include peripheral power drivers and charge-pump voltage inverters.

❖ INPUT STAGE

The input stage is a large N-Channel FET with a P-channel constant-current source. This circuit has a threshold of about 1.5V, relatively independent of the VCC voltage. This means that the inputs will be directly compatible with TTL over the entire 4.5V - 15V VCC range. Being CMOS, the inputs draw less than 1mA of current over the entire input voltage range of ground to VCC. The quiescent current or no load supply current of the ICL7667 is affected by the input voltage, going to nearly zero when the inputs are at the 0 logic level and rising to 7mA maximum when both inputs are at the 1 logic level. A small amount of hysteresis, about 50mV to 100mV at the input, is generated by positive feedback around the second stage.

❖ OUTPUT STAGE

The ICL7667 output is a high-power CMOS inverter, swinging between ground and VCC. At VCC = 15V, the output impedance of the inverter is typically 7W. The high peak current capability of the ICL7667 enables it to drive a 1000pF load with a rise time of only 40ns. Because the output stage impedance is very low, up to 300mA will flow through the series N-Channel and P-channel output devices (from VCC to ground) during output transitions. This crossover current is responsible for a significant portion of the internal power dissipation of the ICL7667 at high frequencies. It can be minimized by keeping the rise and fall times of the input to the ICL7667 below 1ms.

2.5 DRIVER MODULE

2.5.1 REQUIREMENTS

The switching of a MOSFET involves the charging and discharging of the capacitance between the gate and source terminals. This capacitance is related to the size of the MOSFET chip used typically about 1-2 nF. A gate-source voltage of 6V is usually sufficient to turn a standard MOSFET fully on. However further increases in gate-to-source voltage are usually employed to reduce the MOSFETs on-resistance. Therefore for switching times of about 50 ns, applying a 10 V gate drive voltage to a MOSFET with a 2 nF gate-source capacitance would require the drive circuit to sink and source peak currents of about 0.5 A. However it is only necessary to carry this current during the switching intervals. The gate drive power requirements are given in equation

$$P_G = Q_G . V_{GS} . f$$

where QG is the peak gate charge, VGS is the peak gate source voltage and f is the switching frequency.

In circuits which use a bridge configuration, the gate terminals of the MOSFETs in the circuit need to float relative to each other. The gate drive circuitry then needs to incorporate some isolation. The impedance of the gate drive circuit should not be so large that there is a possibility of dv/dt turn on. dv/dt turn on can be caused by rapid changes of drain to source voltage. The charging current for the gate-drain capacitance CGD flows through the gate drive circuit. This charging current can cause a voltage drop across the gate drive impedance large enough to turn the MOSFET on.

The Driver Circuit is shown in figure 2.19.

SINGLE PHASE HIGH FREQUENCY INVERTER

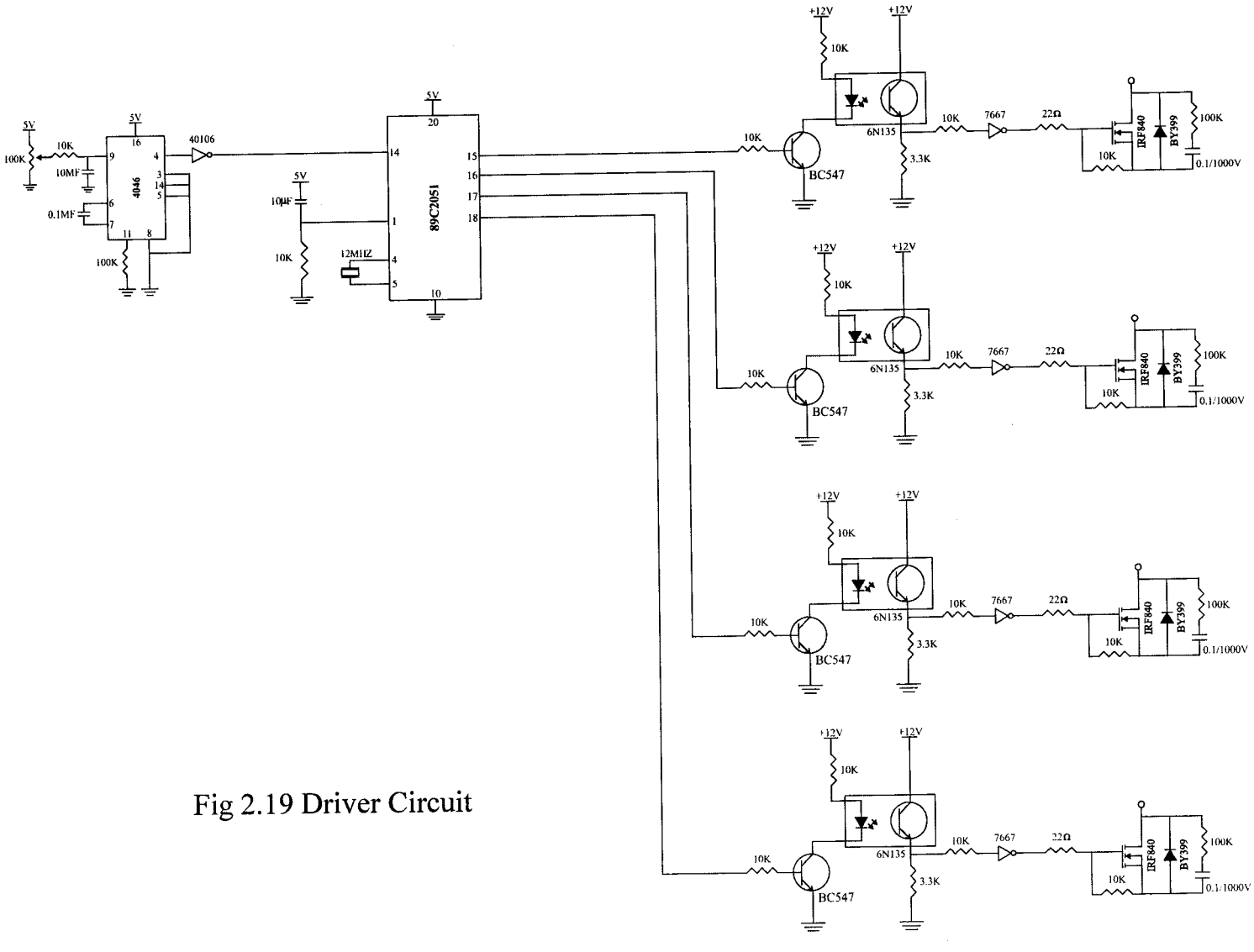


Fig 2.19 Driver Circuit

❖ VOLTAGE CONTROLLED OSCILLATOR

The voltage controlled oscillator IC 4046 produces a square wave output of frequency 600Hz which is used as the switching frequency f_s. Thus the switching frequency is variable and can be adjusted to produce desired switching frequency. The comparator input signal input and inhibit input are all grounded. The resistor and capacitor connection are done on respective pins. The V_{co} input is given at the 9^{th} pin. The V_{co} output is taken across the 4^{th} pin.

❖ PULSE GENERATING CIRCUIT

The microcontroller is a programmable logic device, designed with registers, flip-flops, and timing elements. The microcontroller has a set of instructions designed internally to manipulate data and communicate with the peripherals. This process of data manipulation and communication is designed by the logic design of the microcontroller. The prime use of microcontroller is to control the operation of a fixed program that is stored in ROM and that does not change over the time of the system.

The pulse generation program is developed in 89C2051 microcontroller assembly language. The control program is stored in EPROM. The heart of the 89C2051 is the circuitry that generates the clock pulses by which all internal operations are synchronized. Typically a quartz crystal and capacitors are employed. The crystal frequency is the basic

internal clock frequency of the microcontroller. The crystal oscillator used here is 12 MHz.

The port 1 is programmed as the input pin. When 1's are written to port 1 pin they are pulled high by internal pull-ups and can be used as inputs. As input port 1 pin they are externally being pulled low will be the source current because of internal pull-ups. The outputs are taken across the XTAL1, T1, WR, RD ports. The signals from these ports are used as gate pulses necessary to drive the MOSFETs.

The microcontroller is isolated from the power devices by using 6N135 optoisolators. The purpose of using optoisolators is to provide excellent protection for the controller from the high voltages developed in the inverter stage.

The inverter configuration is achieved by using a MOSFET H-Bridge. The MOSFET's used are standard N-channel power MOSFET's. The MOSFET's are provided with separate floating grounds from separate sources to avoid **'Cross Conduction'**.

2.6 POWER MODULE

2.6.1 CIRCUIT DIAGRAM

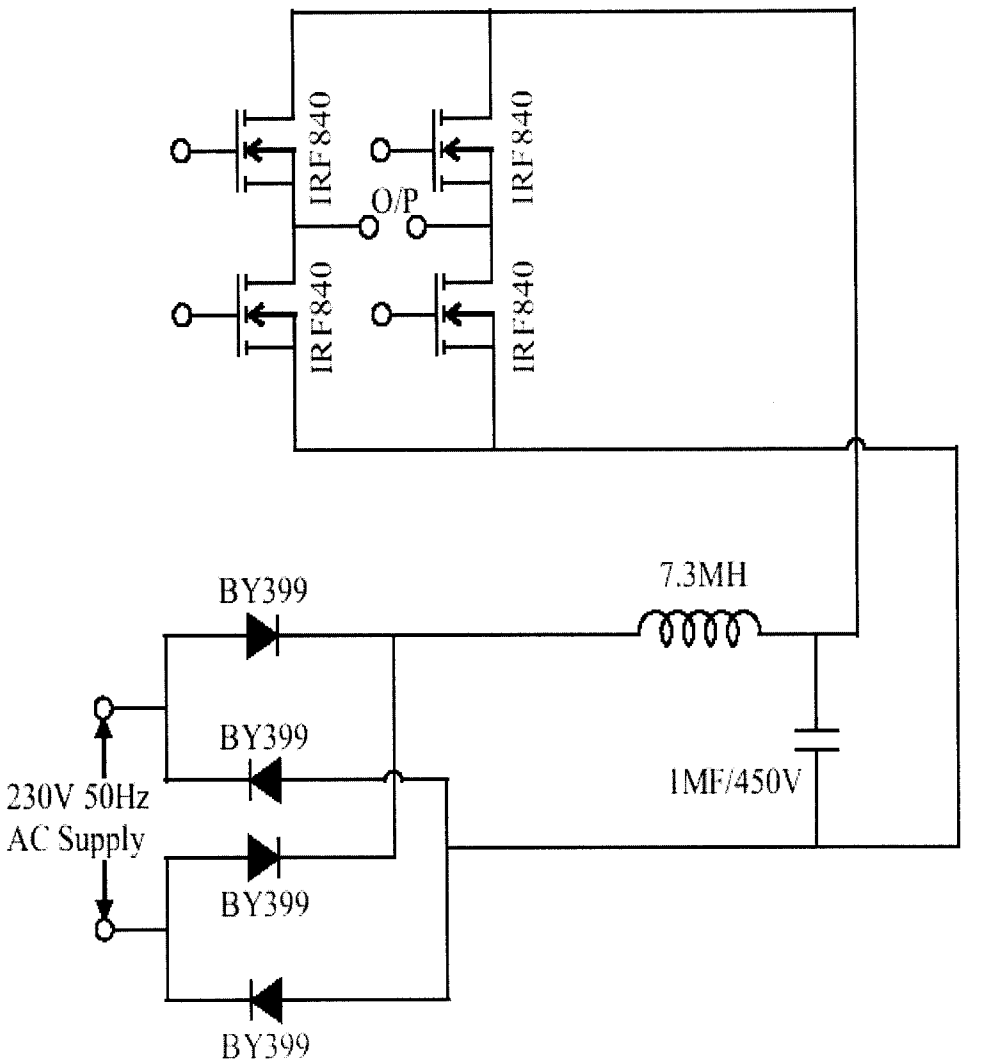


Fig.2.20 Power Module Circuit

2.6.2 MODULE CLASSIFICATION

High frequency resonant inverter consists of the following basic segments

- AC-DC Converter
- Resonant tank section
- Inverter section

❖ AC-DC CONVERTER

The 230V, 50Hz AC signal is rectified by the full wave bridge rectifier which consists of four 1N4007 diodes connected in bridge configuration. The positive and negative voltage regulators 7812 and also 7912 are used which provides both positive and negative regulated voltage levels. The output filtering capacitors of 100V/0.1μF are used suitably to smooth the rectified output of the rectifier.

❖ RESONANT TANK CIRCUIT

The inductance and capacitance forms the resonant tank circuit. The resonant tank circuit is used to achieve the soft switching. The rectified power signal is made to oscillate by using the resonant tank circuit. The switching of the MOSFETs are done in the zero crossing of the output of the resonant tank circuit.

❖ RESONANT TANK CIRCUIT DESIGN

Figure 2.21 is the resonance tank circuit. The above LC tank circuit is of parallel resonance tank configuration.

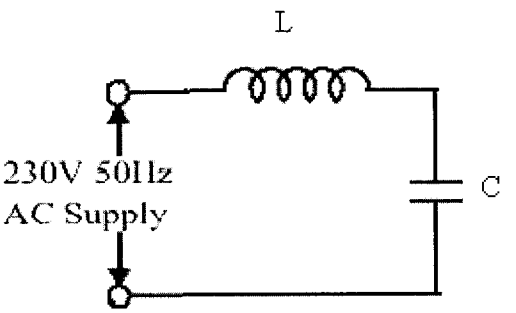


Fig.2.21 Resonant Tank Circuit

A condition of resonance will be experienced in a tank circuit when the reactances of the capacitor and inductor are equal to each other. Because inductive reactance increases with increasing frequency and capacitive reactance decreases with increasing frequency, there will only be one frequency where these two reactances will be equal.

In the above circuit, we have a 1μF capacitor and a 7.3mH inductor. Since we know the equations for determining the reactance of each at a given frequency, and we're looking for that point where the two reactances are equal to each other, we can set the two reactance formulae equal to each other and solve for frequency algebraically.

$X_L=2\pi fL$ $X_C=1/2\pi fC$

Setting the two equal to each other represents a condition of equal reactance.

$$2\pi fL=1/2\pi fC$$

Multiplying both sides by f eliminates the f term in the denominator of the fraction

$$2\pi f^2L=1/2\pi C$$

Dividing both sides by $2\pi L$ leaves f^2 by itself on the left-hand side of the equation

$$f^2=1/2\pi 2\pi LC$$

Taking the square root of both sides of the equation leaves f by itself on the left side

$$f=\sqrt{1} / \sqrt{(2\pi 2\pi LC)}$$

Simplifying,

$$\boxed{f=1/2\pi\sqrt{(LC)}}$$

This formula gives the resonant frequency of a tank circuit, given the values of inductance (L) in Henrys and capacitance (C) in Farads. Plugging in the values of L and C in our example circuit, we arrive at a resonant frequency of 1.862 kHz.

What happens at resonance is quite interesting. With capacitive and inductive reactances equal to each other, the total impedance increases to infinity, meaning that the tank circuit draws no current from the AC power source. We can calculate the individual impedances of the 1μF capacitor and

the 7.3mH inductor and work through the parallel impedance formula to demonstrate this mathematically:

$$X_L=2\pi fL$$

$$X_L=(2)(\pi)(1862.88\ Hz)(7.3\ mH)$$

$$X_L=85.44\ \Omega$$

$$X_C=1/2\pi fC$$

$$X_C=1/(2)(\pi)(1862.88\ Hz)(1\ \mu F)$$

$$X_C=85.44\ \Omega$$

Thus

$$X_L= X_C$$

Hence the resonance condition is achieved.

❖ INVERTER SECTION

The inverter configuration is achieved using a MOSFET H-Bridge. The MOSFETs used are N-Channel power MOSFETs. In the positive half cycle of the output MOSFETs 1 and 4 are turned on and in the negative half cycle of the output MOSFETs 2 and 3 are turned on. The required output frequency is generated using the proper gate signal. The circuit is configured in H-bridge connection. The gate section of each MOSFETs is switched at high frequency.

2.7 POWER SUPPLIES

Starting with an ac voltage, a steady dc voltage is obtained by rectifying the ac voltage, then filtering to a dc level, and finally, regulating to obtain a desired fixed dc voltage. The regulation is usually obtained from an IC voltage regulator unit, which takes a dc voltage and provides a somewhat lower dc voltage, which remains the same even if the input dc voltage varies, or the output load connected to the dc voltage changes.

A block diagram containing the parts of a typical power supply and the voltage at various points in the unit is shown in Fig 2.22. The ac voltage, typically 120 V RMS, is connected to a transformer, which steps that ac voltage down to the level for the desired dc output. A diode rectifier then provides a full-wave rectified voltage that is initially filtered by a simple capacitor filter to produce a dc voltage. This resulting dc voltage usually has some ripple or ac voltage variation. A regulator circuit can use this dc input to provide a dc voltage that not only has much less ripple voltage but also remains the same dc value even if the input dc voltage varies somewhat, or the load connected to the output dc voltage changes. This voltage regulation is usually obtained using one of a number of popular voltage regulator IC units.

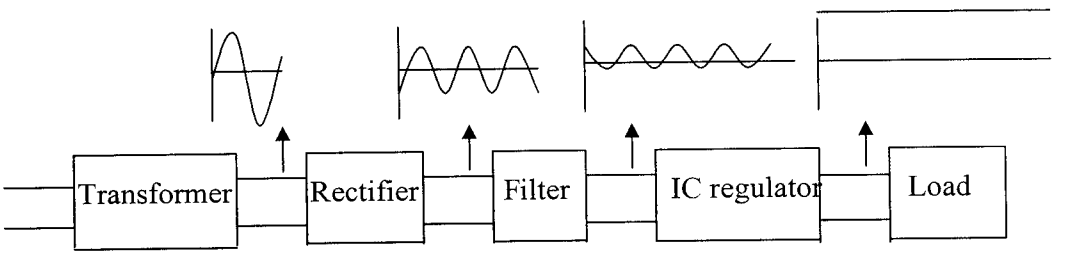


Fig 2.22 Regulated Power Supply Block

2.7.1 IC VOLTAGE REGULATOR

Voltage regulators comprise a class of widely used ICs. Regulator IC units contain the circuitry for reference source, comparator amplifier, control device, and overload protection all in a single IC. Although the internal construction of the IC is somewhat different from that described for discrete voltage regulator circuits, the external operation is much the same. IC units provide regulation of either a fixed positive voltage, a fixed negative voltage, or an adjustably set voltage.

A power supply can be built using a transformer connected to the ac supply line to step the ac voltage to desired amplitude, then rectifying that ac voltage, filtering with a capacitor and RC filter, if desired, and finally regulating the dc voltage using an IC regulator. The regulators can be selected for operation with load currents from hundreds of milli amperes to tens of amperes, corresponding to power ratings from mill watts to tens of watts.

❖ THREE-TERMINAL VOLTAGE REGULATORS

The fixed voltage regulator has an unregulated dc input voltage, Vi, applied to one input terminal, a regulated output dc voltage, Vo, from a second terminal, with the third terminal connected to ground. For a selected regulator, IC device specifications list a voltage range over which the input voltage can vary to maintain a regulated output voltage over a range of load current. The specifications also list the amount of output voltage change resulting from a change in load current (load regulation) or in input voltage (line regulation).

❖ FIXED POSITIVE VOLTAGE REGULATORS

The series 78 regulators provide fixed regulated voltages from 5 to 24 V. Figure 2.24 shows how one such IC, a 7812, is connected to provide voltage regulation with output from this unit of +12V dc. An unregulated input voltage Vi is filtered by capacitor C1 and connected to the IC's IN terminal. The IC's OUT terminal provides a regulated + 12V which is filtered by capacitor C2 (mostly for any high-frequency noise). The third IC terminal is connected to ground (GND). While the input voltage may vary over some permissible voltage range, and the output load may vary over some acceptable range, the output voltage remains constant within specified voltage variation limits. These limitations are spelled out in the manufacturer's specification sheets. A table of positive voltage regulated ICs of 7800 series are provided in Table 2.1.

IC Part	**Output Voltage (V)**	**Minimum Vi (V)**
7805	+5	7.3
7806	+6	8.3
7808	+8	10.5
7810	+10	12.5
7812	+12	14.6
7815	+15	17.7
7818	+18	21.0
7824	+24	27.1

Table 2.1 Positive Voltage Regulators

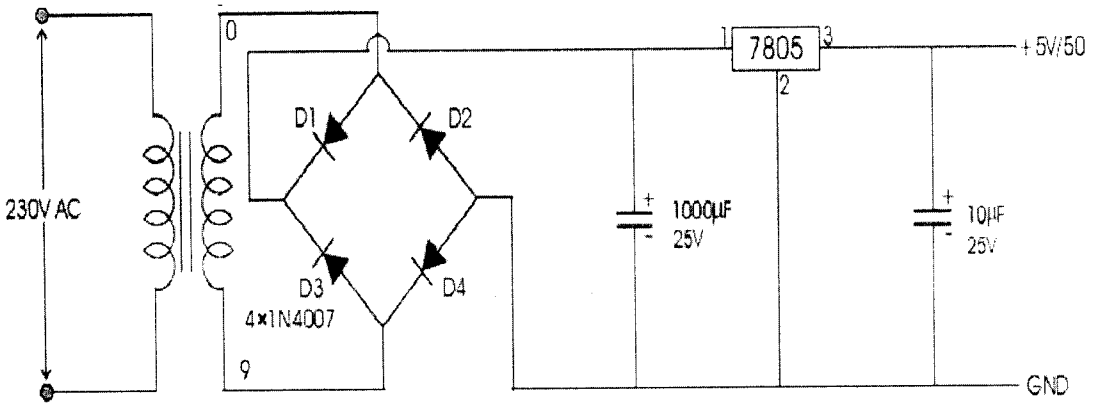


Fig 2.23 AC Rectifier Circuit (+5V)

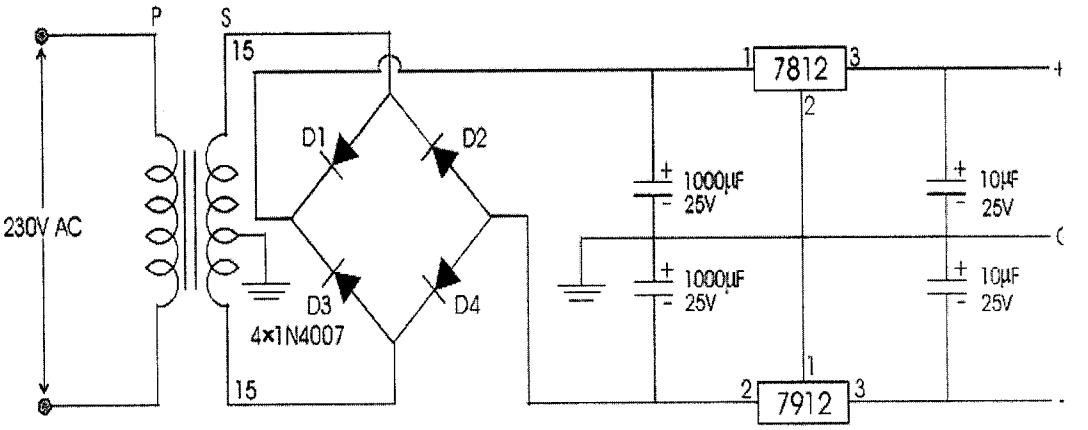


Fig 2.24 AC Rectifier Circuit (±12V)

2.8 TESTING

2.8.1 OUTPUT WAVEFORM

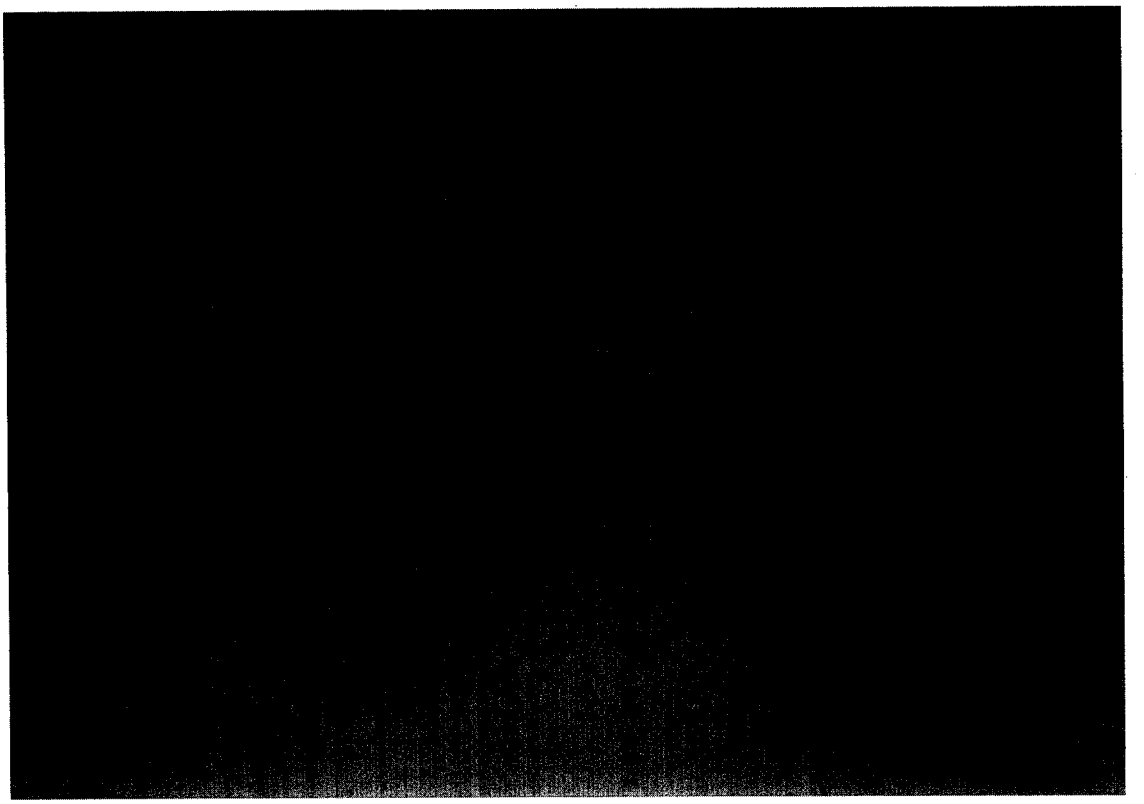


Fig 2.25 Resonant Waveform at 1.862 KHz

The above waveform has been observed in Tektronix Digital Scope Oscilloscope.

2.8.2 SYSTEM VALIDATION

The Resonant DC link inverter circuit has been simulated in MATLAB/SIMLINK 6.5 for the parameters considered in the design circuit. In the simulations, the waveforms of the gate pulses to the MOSFET switches are shown. The hardware has been implemented and the output waveform of the circuit is shown in digital CRO. The circuit output waveform agrees closely with simulated waveform.

The circuit output is tested with a Compact Fluorescent lamp (CFL). The CFL lamp is having many advantages on working under high frequency resonant conditions compared to conventional 50/60 Hz system.

They are:

- The illumination of the CFL is obtained at minimum operating voltages and flicker less operation is also obtained.

- Since diode reverse recovery current is high at high frequency operation, the CFL glows for the voltages below the normal operating voltage and hence quick, dynamic response is obtained.

- The harmonics in the bridge rectifier circuit of the CFL is reduced at high frequency operation.

CONCLUSION AND FUTURE ENHANCEMENTS

CHAPTER 3

CONCLUSION AND FUTURE ENHANCEMENTS

3.1 CONCLUSION

This project has been simulated using MATLAB. The simulation has been verified by hardware implementation. Using this hardware module, sinusoidal wave has been generated. The unique aspect of this project is that variable high frequency upto the range of 12 kHz has been generated successfully.

The power system appliances can operate even below their conventional voltage levels at higher frequencies. This has been tested with a Compact Fluorescent Lamp (CFL).

The conclusion drawn is that the variable high frequency power system module is able to provide many advantages to the utilization equipment over the conventional 50/60Hz power system.

3.2 FUTURE ENHANCEMENTS

This project can be enhanced using various techniques. The project can also be extended to a three phase system.

Energy and space saving, high performance by the use of the higher frequency to fluorescent lighting systems, amorphous metal cored transformers, DC power supplies and naturally commutated cycloconverters can be experimentally demonstrated.

In the future, more than 20 kHz, high power resonant inverters can be implemented depending on the requirements of the industry. Irrespective of the applications where size and space play an important role, the system can be upgraded and modifications can be incorporated in a flexible manner so as to reflect the new requirements.

APPENDICES

APPENDIX 1 – MICROCONTROLLER PROGRAM

```
#include<reg51.h>
void delay(unsigned int);
sbit input = P1^2;
sbit output1 = P1^3;
sbit output2 = P1^4;
sbit output3 = P1^5, output4 = P1^6;
main()
{
        output1=output2=0;
        while(1)
        {
                while(!input);
                output2=output4=0;
                delay(3);
                output1=output3=1;
                while(input);
                output1=output3=0;
                delay(3);
                output2=output4=1;
        }
}
void delay(unsigned int del)
{
        while(del--);
}
```

atures

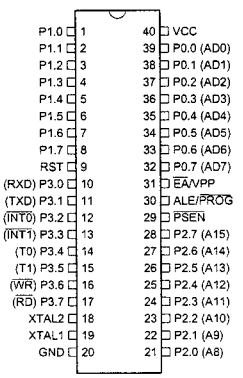
- mpatible with MCS-51™ Products
- Bytes of In-System Reprogrammable Flash Memory
- Endurance: 1,000 Write/Erase Cycles
- lly Static Operation: 0 Hz to 24 MHz
- ree-level Program Memory Lock
- 3 x 8-bit Internal RAM
- Programmable I/O Lines
- o 16-bit Timer/Counters
- x Interrupt Sources
- ogrammable Serial Channel
- w-power Idle and Power-down Modes

scription

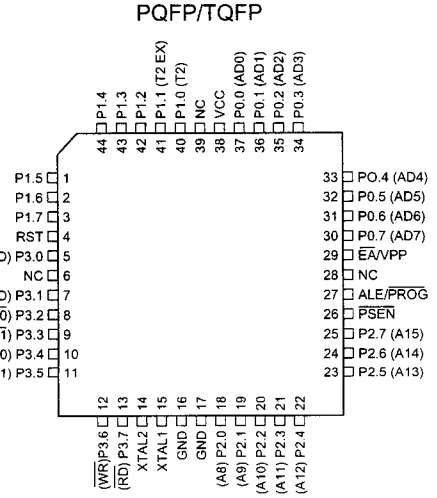
AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K s of Flash programmable and erasable read only memory (PEROM). The device anufactured using Atmel's high-density nonvolatile memory technology and is patible with the industry-standard MCS-51 instruction set and pinout. The on-chip h allows the program memory to be reprogrammed in-system or by a conven- al nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides ghly-flexible and cost-effective solution to many embedded control applications.

Configurations

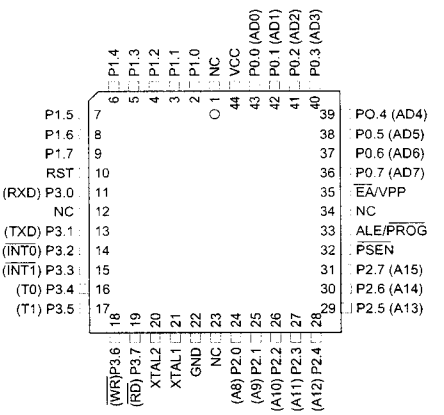
PDIP



PQFP/TQFP



PLCC



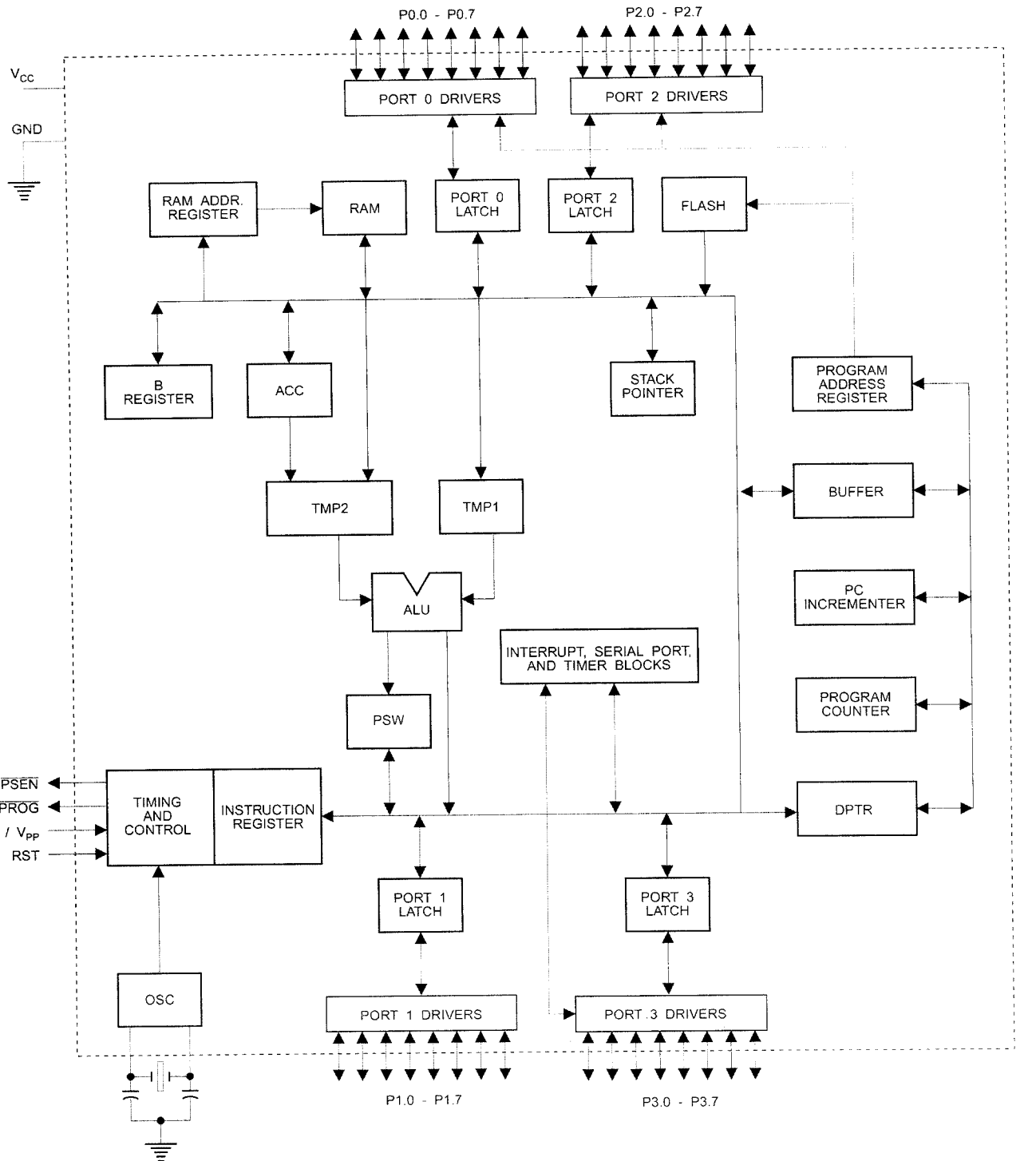
8-bit Microcontroller with 4K Bytes Flash

AT89C51

Not Recommended for New Designs. Use AT89S51.

Rev. 0265G–02/00

ck Diagram


P0.0 - P0.7
P2.0 - P2.7
V_{CC}
GND
PORT 0 DRIVERS
PORT 2 DRIVERS
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
BUFFER
TMP2
TMP1
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PROGRAM COUNTER
PSW
PSEN
PROG
/ V_{PP}
RST
TIMING AND CONTROL
INSTRUCTION REGISTER
DPTR
PORT 1 LATCH
PORT 3 LATCH
OSC
PORT 1 DRIVERS
PORT 3 DRIVERS
P1.0 - P1.7
P3.0 - P3.7

AT89C51 provides the following standard features: 4K s of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit r/counters, a five vector two-level interrupt architecture, l duplex serial port, on-chip oscillator and clock cir- y. In addition, the AT89C51 is designed with static logic peration down to zero frequency and supports two ware selectable power saving modes. The Idle Mode s the CPU while allowing the RAM, timer/counters, al port and interrupt system to continue functioning. The er-down Mode saves the RAM contents but freezes oscillator disabling all other chip functions until the next lware reset.

n Description

C

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und.

t 0

t 0 is an 8-bit open-drain bi-directional I/O port. As an out port, each pin can sink eight TTL inputs. When 1s written to port 0 pins, the pins can be used as high- edance inputs.

t 0 may also be configured to be the multiplexed low- er address/data bus during accesses to external pro- m and data memory. In this mode P0 has internal ups.

t 0 also receives the code bytes during Flash program- ng, and outputs the code bytes during program ification. External pullups are required during program ification.

rt 1

t 1 is an 8-bit bi-directional I/O port with internal pullups. e Port 1 output buffers can sink/source four TTL inputs. hen 1s are written to Port 1 pins they are pulled high by internal pullups and can be used as inputs. As inputs, t 1 pins that are externally being pulled low will source rrent (I_{IL}) because of the internal pullups.

rt 1 also receives the low-order address bytes during sh programming and verification.

rt 2

rt 2 is an 8-bit bi-directional I/O port with internal pullups. e Port 2 output buffers can sink/source four TTL inputs. hen 1s are written to Port 2 pins they are pulled high by internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and verification.

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE

se is skipped during each access to external Data nory.

esired, ALE operation can be disabled by setting bit 0 of R location 8EH. With the bit set, ALE is active only dur- a MOVX or MOVC instruction. Otherwise, the pin is kly pulled high. Setting the ALE-disable bit has no ct if the microcontroller is in external execution mode.

EN

gram Store Enable is the read strobe to external pro- m memory.

en the AT89C51 is executing code from external pro- m memory, $\overline{PSEN}$ is activated twice each machine e, except that two $\overline{PSEN}$ activations are skipped during h access to external data memory.

VPP

ernal Access Enable. $\overline{EA}$ must be strapped to GND in er to enable the device to fetch code from external pro- m memory locations starting at 0000H up to FFFFH. e, however, that if lock bit 1 is programmed, $\overline{EA}$ will be rnally latched on reset.

should be strapped to V_{CC} for internal program cutions.

s pin also receives the 12-volt programming enable volt- e (V_{PP}) during Flash programming, for parts that require volt V_{PP}.

AL1

ut to the inverting oscillator amplifier and input to the rnal clock operating circuit.

AL2

tput from the inverting oscillator amplifier.

scillator Characteristics

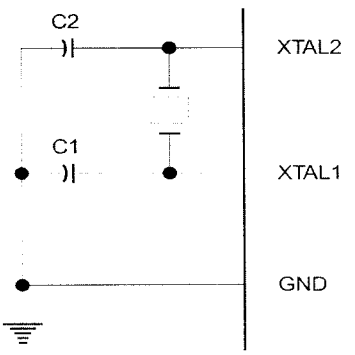
AL1 and XTAL2 are the input and output, respectively, an inverting amplifier which can be configured for use as on-chip oscillator, as shown in Figure 1. Either a quartz stal or ceramic resonator may be used. To drive the vice from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when idle is terminated by a hard ware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Figure 1. Oscillator Connections

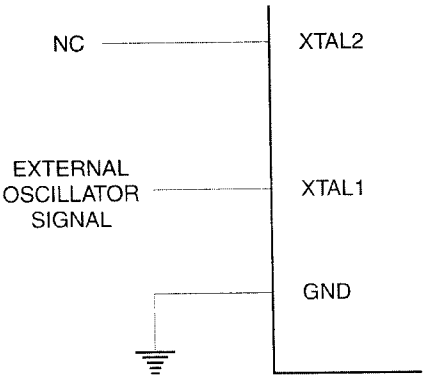


Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

atus of External Pins During Idle and Power-down Modes

ode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
le	Internal	1	1	Data	Data	Data	Data
le	External	1	1	Float	Data	Address	Data
ower-down	Internal	0	0	Data	Data	Data	Data
ower-down	External	0	0	Float	Data	Data	Data

ure 2. External Clock Drive Configuration



ower-down Mode

he power-down mode, the oscillator is stopped, and the truction that invokes power-down is the last instruction ecuted. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. The only exit from power-down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

ock Bit Protection Modes

	Program Lock Bits			
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash is disabled
3	P	P	U	Same as mode 2, also verify is disabled
4	P	P	P	Same as mode 3, also external execution is disabled

ogramming the Flash

AT89C51 is normally shipped with the on-chip Flash mory array in the erased state (that is, contents = FFH) ready to be programmed. The programming interface epts either a high-voltage (12-volt) or a low-voltage $_{C}$) program enable signal. The low-voltage program- g mode provides a convenient way to program the 9C51 inside the user's system, while the high-voltage gramming mode is compatible with conventional third- y Flash or EPROM programmers.

AT89C51 is shipped with either the high-voltage or -voltage programming mode enabled. The respective -side marking and device signature codes are listed in following table.

	V_{PP} = 12V	V_{PP} = 5V
p-side Mark	AT89C51 xxxx yyww	AT89C51 xxxx-5 yyww
gnature	(030H) = 1EH (031H) = 51H (032H) =F FH	(030H) = 1EH (031H) = 51H (032H) = 05H

AT89C51 code memory array is programmed byte-by- e in either programming mode. *To program any non- nk byte in the on-chip Flash Memory, the entire memory st be erased using the Chip Erase Mode.*

ogramming Algorithm: Before programming the 89C51, the address, data and control signals should be up according to the Flash programming mode table and ure 3 and Figure 4. To program the AT89C51, take the owing steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V for the high-voltage programming mode.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms.
6. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89C51 features $\overline{Data}$ Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The code array is written with all "1"s. The chip erase operation must be executed before the code memory can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H, 031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(030H) = 1EH indicates manufactured by Atmel
(031H) = 51H indicates 89C51
(032H) = FFH indicates 12V programming
(032H) = 05H indicates 5V programming

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

ash Programming Modes

ode		RST	PSEN	ALE/PROG	EA/V_{PP}	P2.6	P2.7	P3.6	P3.7
ite Code Data		H	L		H/12V	L	H	H	H
ad Code Data		H	L	H	H	L	L	H	H
ite Lock	Bit - 1	H	L		H/12V	H	H	H	H
	Bit - 2	H	L		H/12V	H	H	L	L
	Bit - 3	H	L		H/12V	H	L	H	L
ip Erase		H	L	(1)	H/12V	H	L	L	L
ead Signature Byte		H	L	H	H	L	L	L	L

e: 1. Chip Erase requires a 10 ms PROG pulse.

ure 3. Programming the Flash

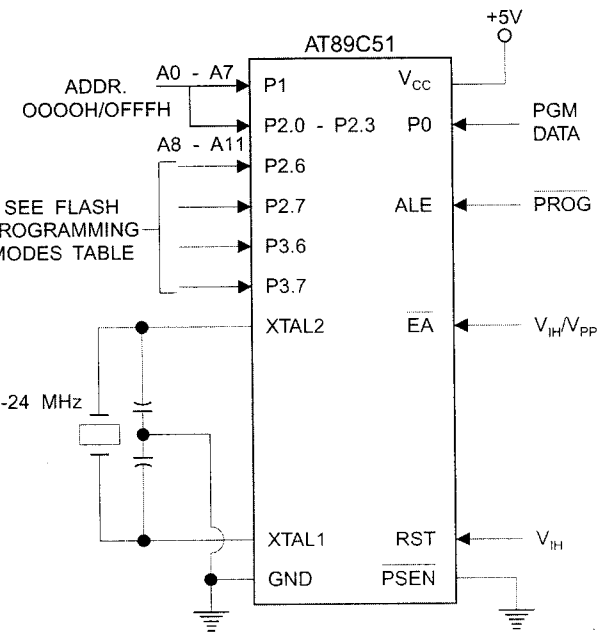
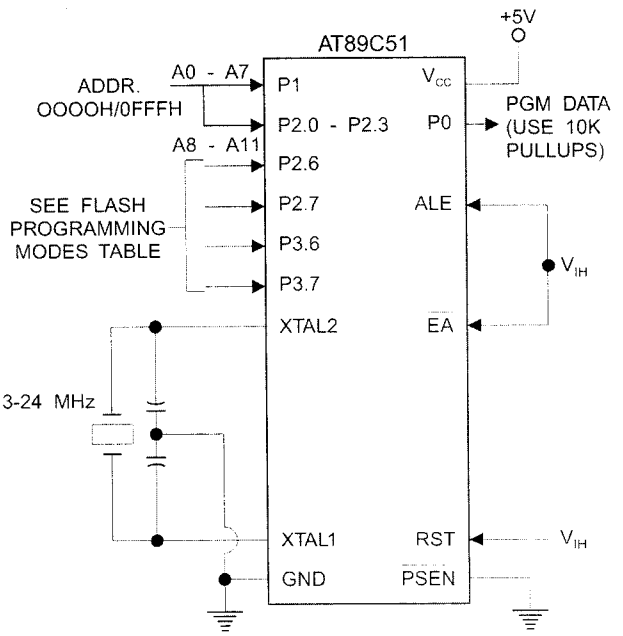


Figure 4. Verifying the Flash

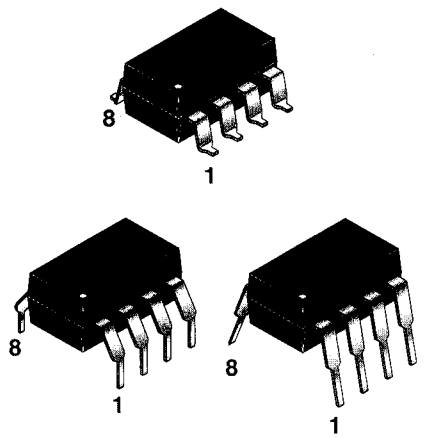


FAIRCHILD
SEMICONDUCTOR®

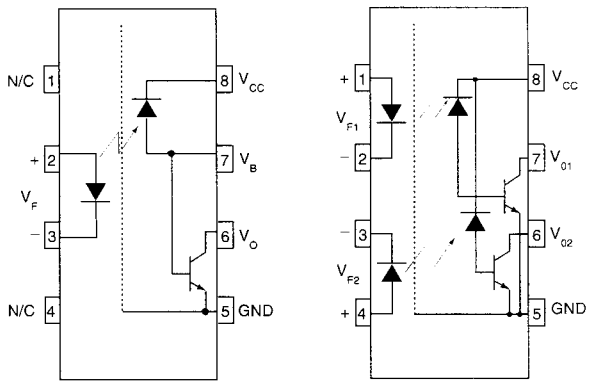
HIGH SPEED TRANSISTOR OPTOCOUPLERS

SINGLE-CHANNEL: 6N135 6N136 HCPL-2503 HCPL-4502
DUAL-CHANNEL: HCPL-2530 HCPL-2531

PACKAGE



SCHEMATIC



6N135, 6N136, HCPL-2503, HCPL-4502

HCPL-2530/HCPL-2531

Pin 7 is not connected in Part Number HCPL-4502

DESCRIPTION

The HCPL-4502/HCPL-2503, 6N135/6 and HCPL-2530/HCPL-2531 optocouplers consist of an AlGaAs LED optically coupled to a high speed photodetector transistor.

A separate connection for the bias of the photodiode improves the speed by several orders of magnitude over conventional phototransistor optocouplers by reducing the base-collector capacitance of the input transistor.

An internal noise shield provides superior common mode rejection of 10kV/μs. An improved package allows superior insulation permitting a 480 V working voltage compared to industry standard of 220 V.

FEATURES

- High speed-1 MBit/s
- Superior CMR-10 kV/μs
- Dual-Channel HCPL-2530/HCPL-2531
- Double working voltage-480V RMS
- CTR guaranteed 0-70°C
- U.L. recognized (File # E90700)

APPLICATIONS

- Line receivers
- Pulse transformer replacement
- Output interface to CMOS-LSTTL-TTL
- Wide bandwidth analog coupling

FAIRCHILD
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HIGH SPEED TRANSISTOR OPTOCOUPLERS

SINGLE-CHANNEL: 6N135 6N136 HCPL-2503 HCPL-4502
DUAL-CHANNEL: HCPL-2530 HCPL-2531

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Parameter		Symbol	Value	Units
Storage Temperature		T_{STG}	-55 to +125	°C
Operating Temperature		T_{OPR}	-55 to +100	°C
Lead Solder Temperature		T_{SOL}	260 for 10 sec	°C
EMITTER				
DC/Average Forward Input Current	Each Channel (Note 1)	I_F (avg)	25	mA
Peak Forward Input Current (50% duty cycle, 1 ms P.W.)	Each Channel (Note 2)	I_F (pk)	50	mA
Peak Transient Input Current - (≤1 µs P.W., 300 pps)	Each Channel	I_F (trans)	1.0	A
Reverse Input Voltage	Each Channel	V_R	5	V
Input Power Dissipation	(6N135/6N136 and HCPL-2503/4502) (HCPL-2530/2531) Each Channel (Note 3)	P_D	100 45	mW
DETECTOR				
Average Output Current	Each Channel	I_O (avg)	8	mA
Peak Output Current	Each Channel	I_O (pk)	16	mA
Emitter-Base Reverse Voltage	(6N135, 6N136 and HCPL-2503 only)	V_{EBR}	5	V
Supply Voltage		V_{CC}	-0.5 to 30	V
Output Voltage		V_O	-0.5 to 20	V
Base Current	(6N135, 6N136 and HCPL-2503 only)	I_B	5	mA
Output power dissipation	(6N135, 6N136, HCPL-2503, HCPL-4502) (Note 4)	P_D	100	mW
	(HCPL-2530, HCPL-2531) Each Channel		35	mW

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HIGH SPEED TRANSISTOR OPTOCOUPLERS

INGLE-CHANNEL: 6N135 6N136 HCPL-2503 HCPL-4502
)UAL-CHANNEL: HCPL-2530 HCPL-2531

ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C Unless otherwise specified)

NDIVIDUAL COMPONENT CHARACTERISTICS

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
EMITTER	(I_F = 16 mA, T_A =25°C)	V_F			1.45	1.7	V
nput Forward Voltage	(I_F = 16 mA)					1.8	
nput Reverse Breakdown Voltage	(I_R = 10 µA)	B_{VR}		5.0			V
Temperature coefficient of forward voltage	(I_F = 16 mA)	$(\Delta V_F/\Delta T_A)$			-1.6		mV/°C
DETECTOR							
Logic high output current	(I_F = 0 mA, V_O = V_{CC} = 5.5 V) (T_A =25°C)	I_{OH}	All		0.001	0.5	µA
	(I_F = 0 mA, V_O = V_{CC} = 15 V) (T_A =25°C)		6N135 6N136 HCPL-4502 HCPL-2503		0.005	1	
	(I_F = 0 mA, V_O = V_{CC} = 15 V)		All			50	
Logic low supply current	(I_F = 16 mA, V_O = Open) (V_{CC} = 15 V)	I_{CCL}	6N135 6N136 HCPL-4502 HCPL-2503		120	200	µA
	(I_{F1} = I_{F2} = 16 mA, V_O = Open) (V_{CC} = 15 V)		HCPL-2530 HCPL-2531		200	400	
Logic high supply current	(I_F = 0 mA, V_O = Open, V_{CC} = 15 V) (T_A =25°C)	I_{CCH}	6N135 6N136 HCPL-4502 HCPL-2503			1	µA
	(I_F = 0 mA, V_O = Open) (V_{CC} = 15 V)		6N135 6N136 HCPL-4502 HCPL-2503			2	
	(I_F = 0 mA, V_O = Open) (V_{CC} = 15 V)		HCPL-2530 HCPL-2531		0.02	4	

* All Typicals at T_A = 25°C

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HIGH SPEED TRANSISTOR OPTOCOUPLERS

SINGLE-CHANNEL: 6N135 6N136 HCPL-2503 HCPL-4502
DUAL-CHANNEL: HCPL-2530 HCPL-2531

TRANSFER CHARACTERISTICS (T_A = 0 to 70°C Unless otherwise specified)

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
COUPLED	(I_F = 16 mA, V_O = 0.4 V) (V_{CC} = 4.5 V, T_A =25°C)	CTR	6N135 HCPL-2530	7	18	50	%
			6N136 HCPL-4502 HCPL-2531	19	27	50	%
			HCPL-2503	12	27		%
Current transfer ratio (Note 5)	(I_F = 16 mA, V_{CC} = 4.5 V) V_{OL}=0.4V		6N135	5	21		%
	V_{OL}=0.5V		HCPL-2530				
	V_{OL}=0.4V		6N136 HCPL-4502	15	30		%
	V_{OL}=0.5V		HCPL-2531				
	V_{OL}=0.4V		HCPL-2503	9	30		%
Logic low output voltage output voltage	(I_F = 16 mA, I_O = 1.1 mA) (V_{CC} = 4.5 V, T_A =25°C)	V_{OL}	6N135		0.18	0.4	V
			HCPL-2530		0.18	0.5	
	(I_F = 16 mA, I_O = 3 mA) (V_{CC} = 4.5 V, T_A =25°C)		6N136 HCPL-2503		0.25	0.4	
			HCPL-2531		0.25	0.5	
	(I_F = 16 mA, I_O = 0.8 mA) (V_{CC} = 4.5 V)		6N135 HCPL-2530			0.5	
	(I_F = 16 mA, I_O = 2.4 mA) (V_{CC} = 4.5 V)		HCPL-4502 HCPL-2531			0.5	

** All Typicals at T_A = 25°C

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HIGH SPEED TRANSISTOR OPTOCOUPLERS

SINGLE-CHANNEL: 6N135 6N136 HCPL-2503 HCPL-4502
DUAL-CHANNEL: HCPL-2530 HCPL-2531

SWITCHING CHARACTERISTICS (T_A = 0 to 70°C unless otherwise specified., V_{CC} = 5 V)

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
Propagation delay time to logic low	T_A = 25°C, (R_L = 4.1 kΩ, I_F = 16 mA) (Note 6) (Fig. 7)	T_{PHL}	6N135 HCPL-2530		0.45	1.5	µs
	(R_L = 1.9 kΩ, I_F = 16 mA) (Note 7) (Fig. 7) T_A = 25°C		6N136 HCPL-4502 HCPL-2503 HCPL-2531		0.45	0.8	µs
	(R_L = 4.1 kΩ, I_F = 16 mA) (Note 6) (Fig. 7)		6N135 HCPL-2530			2.0	µs
	(R_L = 1.9 kΩ, I_F = 16 mA) (Note 7) (Fig. 7)		6N136 HCPL-4502 HCPL-2503 HCPL-2531			1.0	µs
Propagation delay time to logic high	T_A = 25°C, (R_L = 4.1 kΩ, I_F = 16 mA) (Note 6) (Fig. 7)	T_{PLH}	6N135 HCPL-2530		0.5	1.5	µs
	(R_L = 1.9 kΩ, I_F = 16 mA) (Note 7) (Fig. 7) T_A = 25°C		6N136 HCPL-4502 HCPL-2503 HCPL-2531		0.3	0.8	µs
	(R_L = 4.1 kΩ, I_F = 16 mA) (Note 6) (Fig. 7)		6N135 HCPL-2530			2.0	µs
	(R_L = 1.9 kΩ, I_F = 16 mA) (Note 7) (Fig. 7)		6N136 HCPL-4502 HCPL-2503 HCPL-2531			1.0	µs
Common mode transient immunity at logic high	(I_F = 0 mA, V_{CM} = 10 V_{P-P} R_L = 4.1 kΩ) (Note 8) (Fig. 8) T_A = 25°C	$\|CM_H\|$	6N135 HCPL-2530		10,000		V/µs
	(I_F = 0 mA, V_{CM} = 10 V_{P-P}) T_A = 25°C, (R_L = 1.9 kΩ) (Note 8) (Fig. 8)		6N136 HCPL-4502 HCPL-2503 HCPL-2531		10,000		V/µs
Common mode transient immunity at logic low	(I_F = 16 mA, V_{CM} = 10 V_{P-P} R_L = 4.1 kΩ) (Note 8) (Fig. 8) T_A = 25°C	$\|CM_L\|$	6N135 HCPL-2530		10,000		V/µs
	(I_F = 16 mA, V_{CM} = 10 V_{P-P}) (R_L = 1.9 kΩ) (Note 8) (Fig. 8)		6N136 HCPL-4502 HCPL-2503 HCPL-2531		10,000		V/µs

** All Typicals at T_A = 25°C

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HIGH SPEED TRANSISTOR OPTOCOUPLERS

SINGLE-CHANNEL: 6N135 6N136 HCPL-2503 HCPL-4502
DUAL-CHANNEL: HCPL-2530 HCPL-2531

ISOLATION CHARACTERISTICS (T_A = 0 to 70°C Unless otherwise specified)

Characteristics	Test Conditions	Symbol	Min	Typ**	Max	Unit
Input-output insulation leakage current	(Relative humidity = 45%) (T_A = 25°C, t = 5 s) (V_{I-O} = 3000 VDC) (Note 9)	I_{I-O}			1.0	µA
Withstand insulation test voltage	(RH ≤ 50%, T_A = 25°C) (Note 9) (t = 1 min.)	V_{ISO}	2500			V_{RMS}
Resistance (input to output)	(Note 9) (V_{I-O} = 500 VDC)	R_{I-O}		10^{12}		Ω
Capacitance (input to output)	(Note 9) (f = 1 MHz)	C_{I-O}		0.6		pF
DC Current gain	(I_O = 3 mA, V_O = 5 V)	HFE		150		
Input-Input Insulation leakage current	(RH ≤ 45%, V_{I-I} = 500 VDC) (Note 10) t = 5 s, (HCPL-2530/2531 only)	I_{I-I}		0.005		µA
Input-Input Resistance	(V_{I-I} = 500 VDC) (Note 10) (HCPL-2530/2531 only)	R_{I-I}		10^{11}		Ω
Input-Input Capacitance	(f = 1 MHz) (Note 10) (HCPL-2530/2531 only)	C_{I-I}		0.03		pF

Notes

1. Derate linearly above 70°C free-air temperature at a rate of 0.8 mA/°C.
2. Derate linearly above 70°C free-air temperature at a rate of 1.6 mA/°C.
3. Derate linearly above 70°C free-air temperature at a rate of 0.9 mW/°C.
4. Derate linearly above 70°C free-air temperature at a rate of 2.0 mW/°C.
5. Current Transfer Ratio is defined as a ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. The 4.1 kΩ load represents 1 LSTTL unit load of 0.36 mA and 6.1kΩ pull-up resistor.
7. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and 5.6 kΩ pull-up resistor.
8. Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse signal V_{CM}, to assure that the output will remain in a logic high state (i.e., V_O>2.0 V). Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a logic low state (i.e., V_O<0.8 V).
9. Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
10. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.

FAIRCHILD
SEMICONDUCTOR®

HIGH SPEED TRANSISTOR OPTOCOUPLERS

SINGLE-CHANNEL: 6N135 6N136 HCPL-2503 HCPL-4502
DUAL-CHANNEL: HCPL-2530 HCPL-2531

Fig. 1 Normalized CTR vs. Forward Current

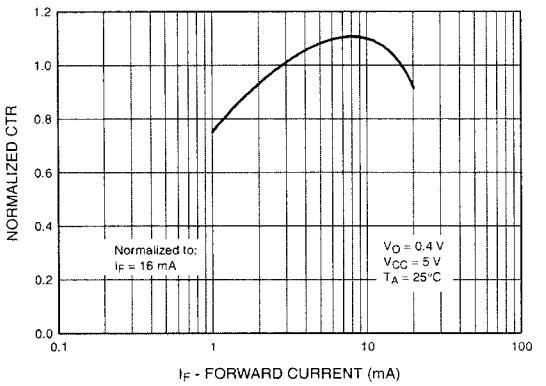


Fig. 2 Normalized CTR vs. Temperature

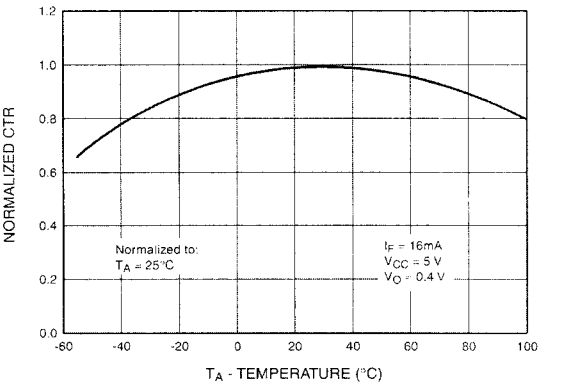


Fig. 3 Output Current vs. Output Voltage

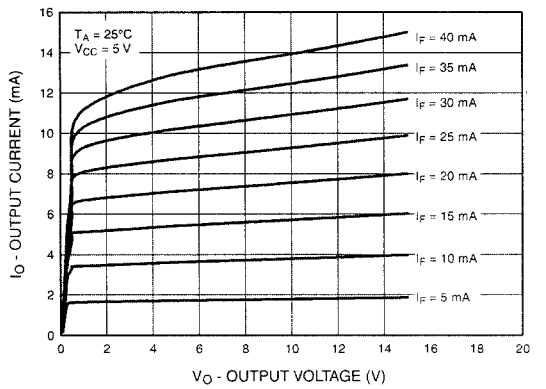


Fig. 4 Logic High Output Current vs. Temperature

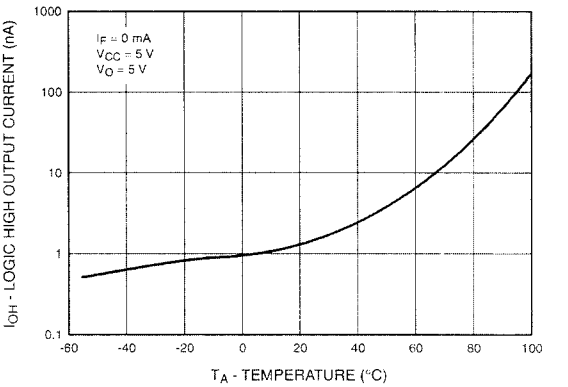


Fig. 5 Propagation Delay vs. Temperature

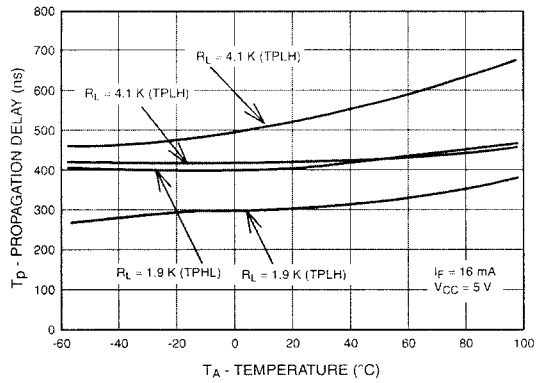
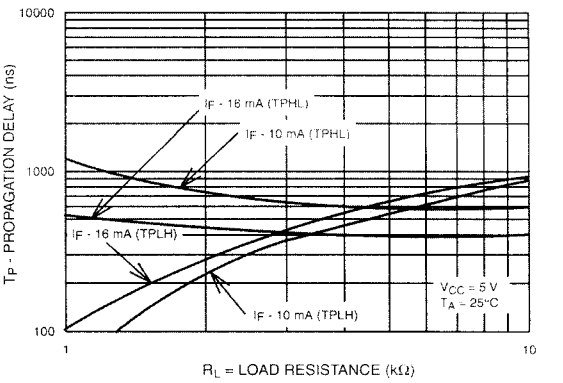


Fig. 6 Propagation Delay vs. Load Resistance

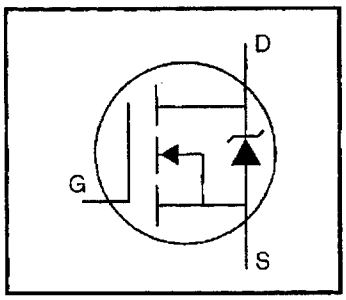


ternational
R Rectifier

IRF840

XFET® Power MOSFET

- ynamic dv/dt Rating
- epetitive Avalanche Rated
- ast Switching
- ase of Paralleling
- imple Drive Requirements



V_{DSS} = 500V

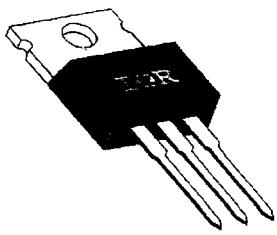
$R_{DS(on)}$ = 0.85Ω

I_D = 8.0A

scription

d Generation HEXFETs from International Rectifier provide the designer the best combination of fast switching, ruggedized device design, low esistance and cost-effectiveness.

TO-220 package is universally preferred for all commercial-industrial lications at power dissipation levels to approximately 50 watts. The low mal resistance and low package cost of the TO-220 contribute to its wide eptance throughout the industry.



TO-220AB

DATA

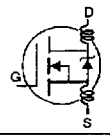
solute Maximum Ratings

	Parameter	Max.	Units
@ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10 V	8.0	A
@ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10 V	5.1	
	Pulsed Drain Current ①	32	
@ T_C = 25°C	Power Dissipation	125	W
	Linear Derating Factor	1.0	W/°C
S	Gate-to-Source Voltage	±20	V
S	Single Pulse Avalanche Energy ②	510	mJ
	Avalanche Current ①	8.0	A
R	Repetitive Avalanche Energy ①	13	mJ
dt	Peak Diode Recovery dv/dt ③	3.5	V/ns
TG	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

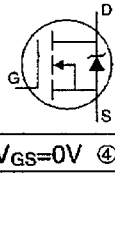
ermal Resistance

	Parameter	Min.	Typ.	Max.	Units
C	Junction-to-Case	—	—	1.0	°C/W
CS	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
A	Junction-to-Ambient	—	—	62	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	V_{GS}=0V, I_D= 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.78	—	V/°C	Reference to 25°C, I_D= 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.85	Ω	V_{GS}=10V, I_D=4.8A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS}=V_{GS}, I_D= 250μA
g_{fs}	Forward Transconductance	4.9	—	—	S	V_{DS}=50V, I_D=4.8A ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V_{DS}=500V, V_{GS}=0V
		—	—	250		V_{DS}=400V, V_{GS}=0V, T_J=125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS}=20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS}=-20V
Q_g	Total Gate Charge	—	—	63	nC	I_D=8.0A
Q_{gs}	Gate-to-Source Charge	—	—	9.3		V_{DS}=400V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	32		V_{GS}=10V See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	V_{DD}=250V
t_r	Rise Time	—	23	—		I_D=8.0A
$t_{d(off)}$	Turn-Off Delay Time	—	49	—		R_G=9.1Ω
t_f	Fall Time	—	20	—		R_D=31Ω See Figure 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1300	—	pF	V_{GS}=0V
C_{oss}	Output Capacitance	—	310	—		V_{DS}=25V
C_{rss}	Reverse Transfer Capacitance	—	120	—		f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	8.0	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	32		
V_{SD}	Diode Forward Voltage	—	—	2.0	V	T_J=25°C, I_S=8.0A, V_{GS}=0V ④
t_{rr}	Reverse Recovery Time	—	460	970	ns	T_J=25°C, I_F=8.0A
Q_{rr}	Reverse Recovery Charge	—	4.2	8.9	μC	di/dt=100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is neglegible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

② V_{DD}=50V, starting T_J=25°C, L=14mH R_G=25Ω, I_{AS}=8.0A (See Figure 12)

③ I_{SD}≤8.0A, di/dt≤100A/μs, V_{DD}≤$V_{(BR)DSS}$, T_J≤150°C

④ Pulse width ≤ 300 μs; duty cycle ≤2%.

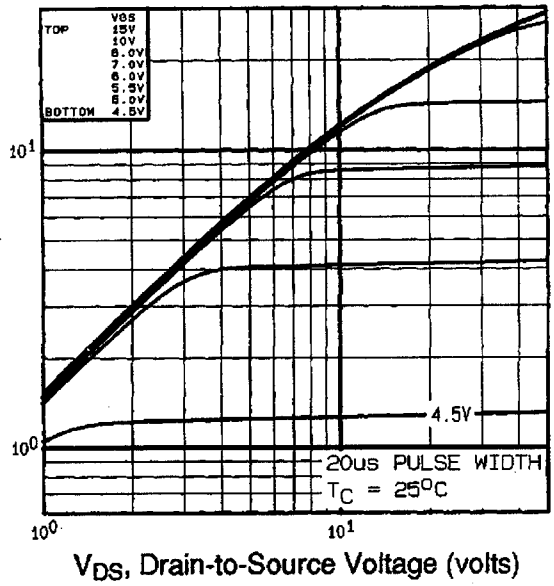


Fig 1. Typical Output Characteristics, T_C=25°C

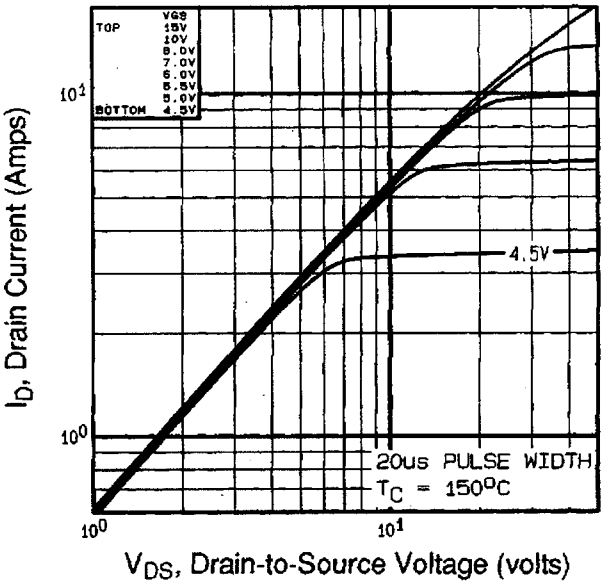


Fig 2. Typical Output Characteristics, T_C=150°C

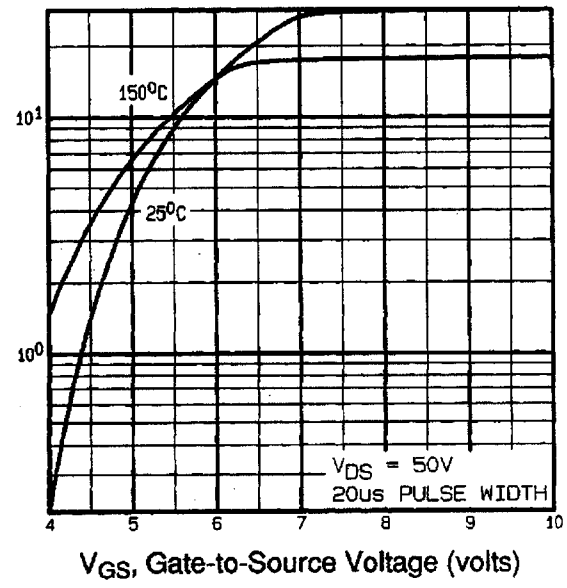


Fig 3. Typical Transfer Characteristics

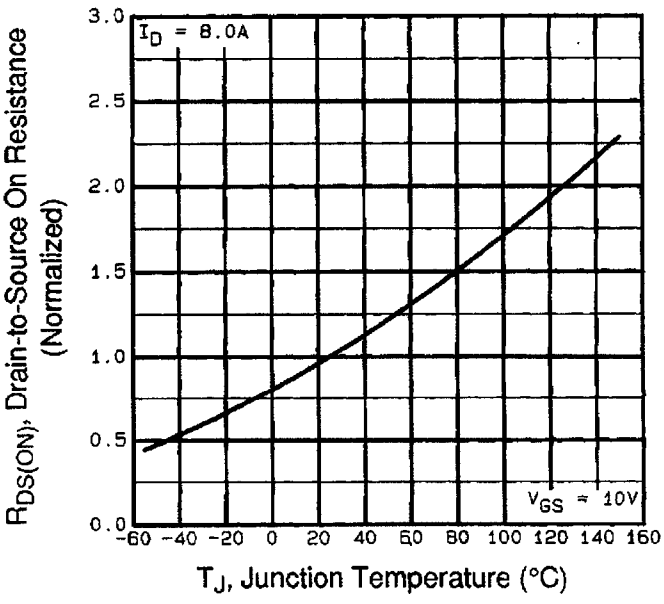


Fig 4. Normalized On-Resisance Vs. Temperature

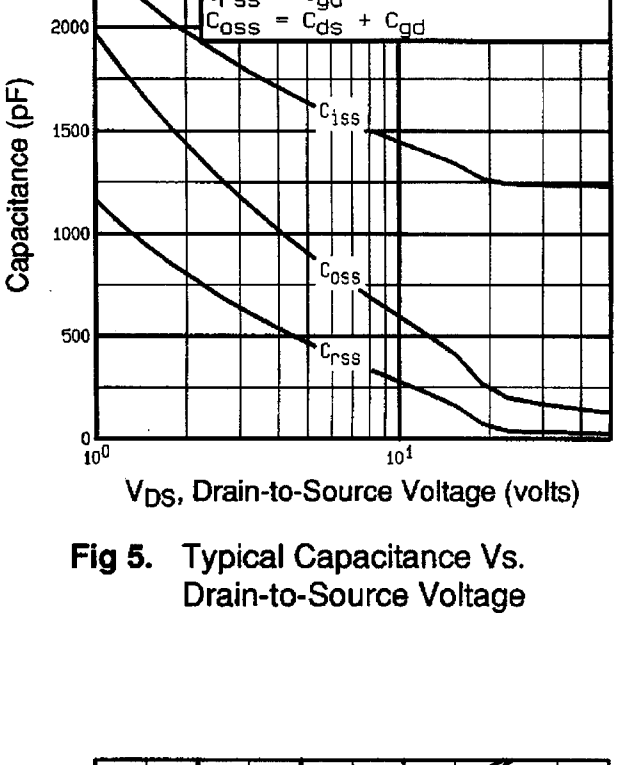


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

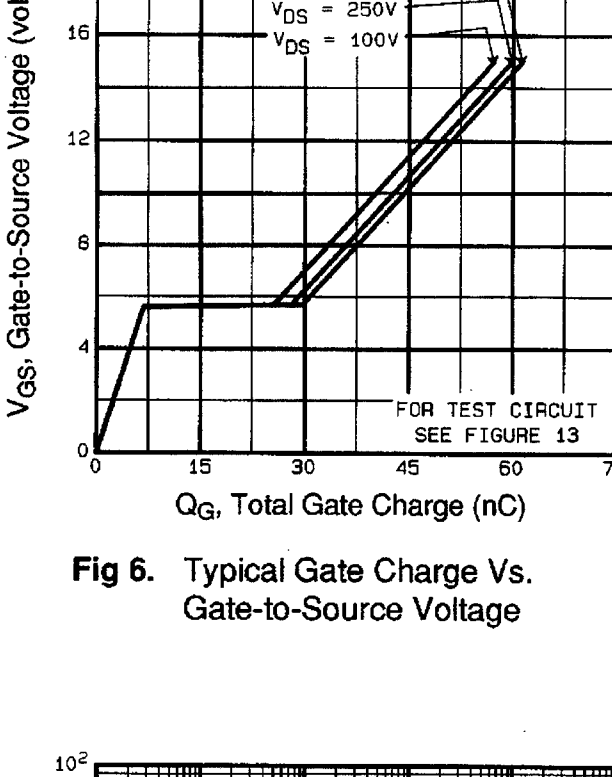


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

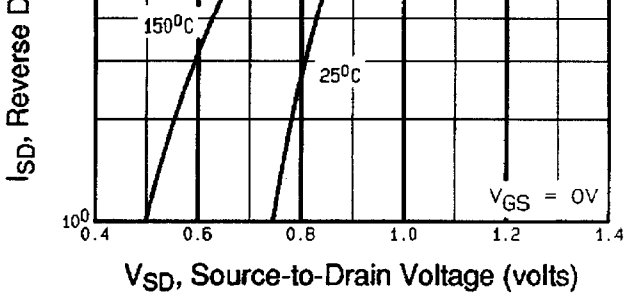


Fig 7. Typical Source-Drain Diode Forward Voltage

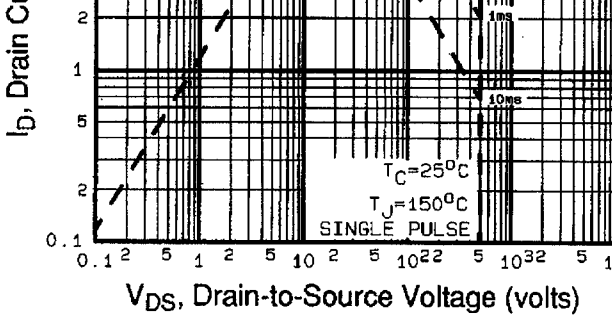


Fig 8. Maximum Safe Operating Area

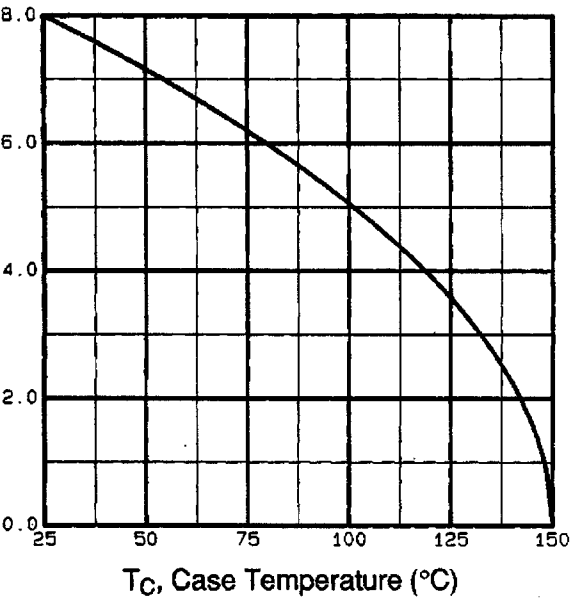


Fig 9. Maximum Drain Current Vs. Case Temperature

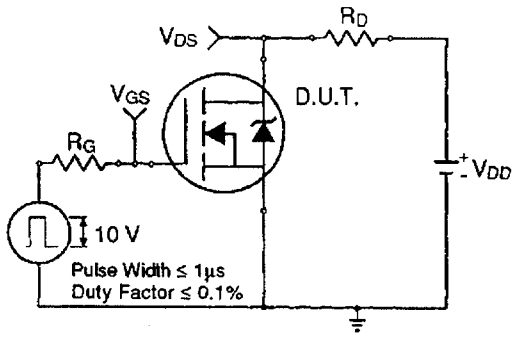


Fig 10a. Switching Time Test Circuit

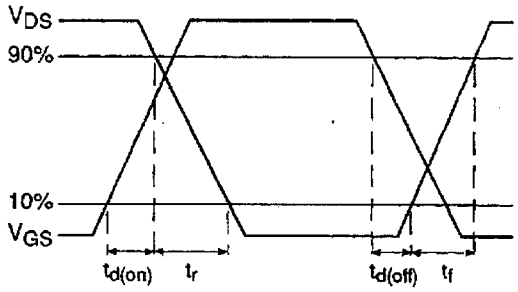


Fig 10b. Switching Time Waveforms

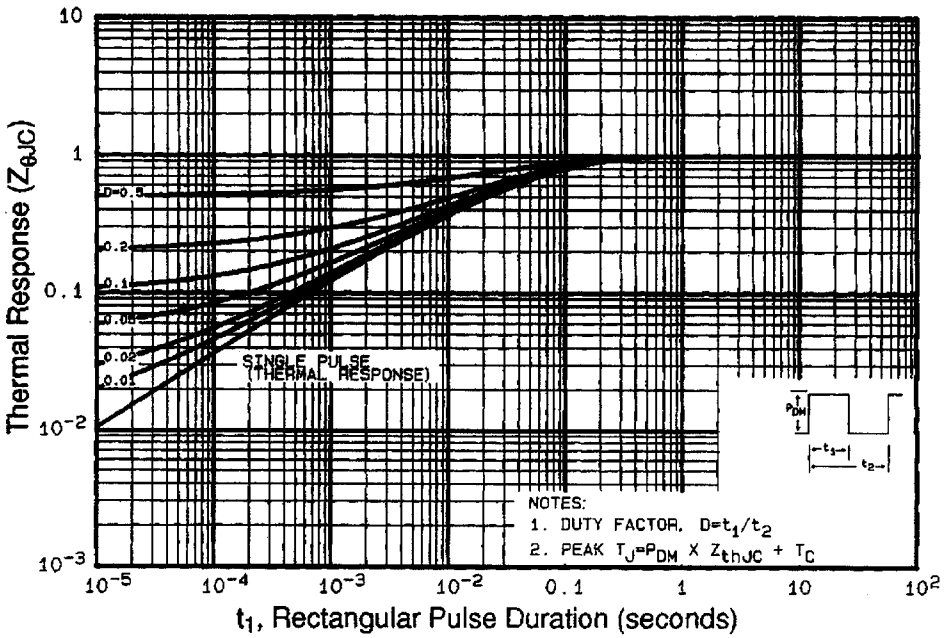


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

DATA

HARRIS SEMICONDUCTOR

ICL7667

April 1994

Dual Power MOSFET Driver

Features

- Fast Rise and Fall Times
  - 30ns with 1000pF Load
- Wide Supply Voltage Range
  - V_{CC} = 4.5V to 15V
- Low Power Consumption
  - 4mW with Inputs Low
  - 20mW with Inputs High
- TTL/CMOS Input Compatible Power Driver
  - R_{OUT} = 7Ω Typ
- Direct Interface with Common PWM Control ICs
- Pin Equivalent to DS0026/DS0056; TSC426

Typical Applications

- Switching Power Supplies
- DC/DC Converters
- Motor Controllers

Description

The ICL7667 is a dual monolithic high-speed driver designed to convert TTL level signals into high current outputs at voltages up to 15V. Its high speed and current output enable it to drive large capacitive loads with high slew rates and low propagation delays. With an output voltage swing only millivolts less than the supply voltage and a maximum supply voltage of 15V, the ICL7667 is well suited for driving power MOSFETs in high frequency switched-mode power converters. The ICL7667s high current outputs minimize power losses in the power MOSFETs by rapidly charging and discharging the gate capacitance. The ICL7667s input are TTL compatible and can be directly driven by common pulse-width modulation control ICs.

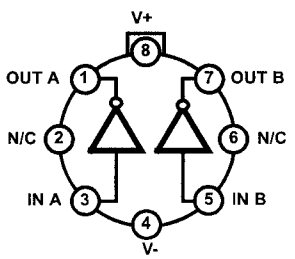
Order Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7667CBA	0°C to +70°C	8 Lead SOIC (N)
ICL7667CPA	0°C to +70°C	8 Lead Plastic DIP
ICL7667CJA	0°C to +70°C	8 Lead Ceramic DIP
ICL7667CTV	0°C to +70°C	8 Pin Metal Can
ICL7667MTV (Note 1)	-55°C to +125°C	8 Pin Metal Can
ICL7667MJA (Note 1)	-55°C to +125°C	8 Lead CerDIP

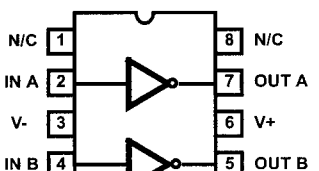
NOTE: 1. Add /883B to Part Number for 883B Processing

Pinouts

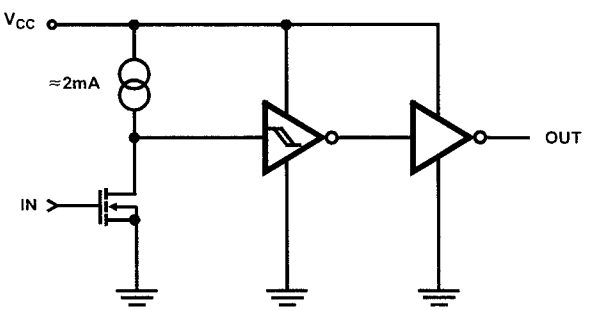
ICL7667 (CAN)
TOP VIEW



ICL7667 (PDIP, SOIC, CERDIP)
TOP VIEW



Functional Diagram



Specifications ICL7667

Absolute Maximum Ratings

Supply Voltage V+ to V- 15V
Input Voltage . . . . . V- -0.3V to V+ +0.3V
Package Dissipation, T_A +25°C 500mW

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
PDIP Package	150°C/W	-
SOIC Package	170°C/W	-
Metal Can Package	156°C/W	68°C/W
CerDIP Package	115°C/W	30°C/W

Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering 10s) . . . . . +300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Temperature Range

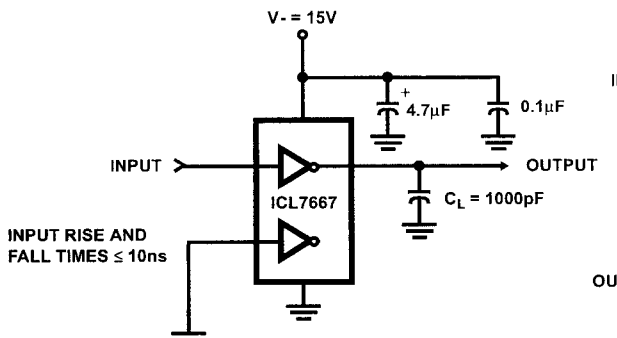
ICL7667C . . . . . 0°C to +70°C
ICL7667M . . . . . -55°C to +125°C

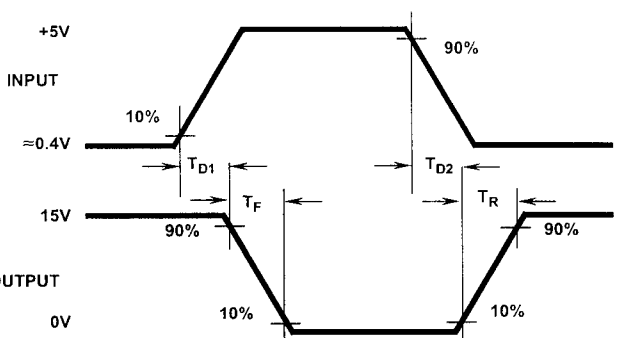
Electrical Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	ICL7667C, M T_A = +25°C MIN	TYP	MAX	ICL7667M -55°C ≤ T_A ≤ +125°C MIN	TYP	MAX	UNITS
DC SPECIFICATIONS									
Logic 1 Input Voltage	V_{IH}	V_{CC} = 4.5V	2.0	-	-	2.0	-	-	V
Logic 1 Input Voltage	V_{IH}	V_{CC} = 15V	2.0	-	-	2.0	-	-	V
Logic 0 Input Voltage	V_{IL}	V_{CC} = 4.5V	-	-	0.8	-	-	0.5	V
Logic 0 Input Voltage	V_{IL}	V_{CC} = 15V	-	-	0.8	-	-	0.5	V
Input Current	I_{IL}	V_{CC} = 15V, V_{IN} = 0V and 15V	-0.1	-	0.1	-0.1	-	0.1	µA
Output Voltage High	V_{OH}	V_{CC} = 4.5V and 15V	V_{CC} -0.05	V_{CC}	-	V_{CC} -0.1	V_{CC}	-	V
Output Voltage Low	V_{OL}	V_{CC} = 4.5V and 15V	-	0	0.05	-	-	0.1	V
Output Resistance	R_{OUT}	V_{IN} = V_{IL}, I_{OUT} = -10mA, V_{CC} = 15V	-	7	10	-	-	12	Ω
Output Resistance	R_{OUT}	V_{IN} = V_{IH}, I_{OUT} = 10mA, V_{CC} = 15V	-	8	12	-	-	13	Ω
Power Supply Current	I_{CC}	V_{CC} = 15V, V_{IN} = 3V both inputs	-	5	7	-	-	8	mA
Power Supply Current	I_{CC}	V_{CC} = 15V, V_{IN} = 0V both inputs	-	150	400	-	-	400	µA
SWITCHING SPECIFICATIONS									
Delay Time	T_{D2}	Figure 3	-	35	50	-	-	60	ns
Rise Time	T_R	Figure 3	-	20	30	-	-	40	ns
Fall Time	T_F	Figure 3	-	20	30	-	-	40	ns
Delay Time	T_{D1}	Figure 3	-	20	30	-	-	40	ns

NOTE: All typical values have been characterized but are not tested.

Test Circuits





Typical Performance Curves

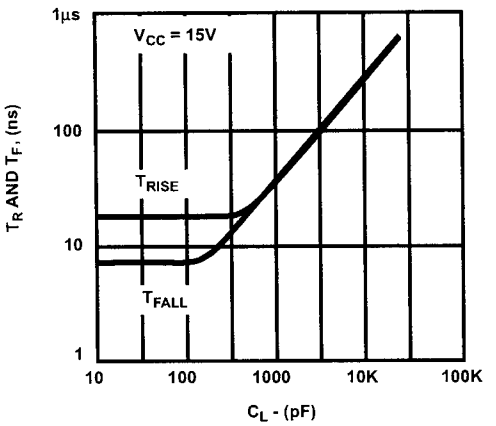


FIGURE 1. RISE AND FALL TIMES vs C_L

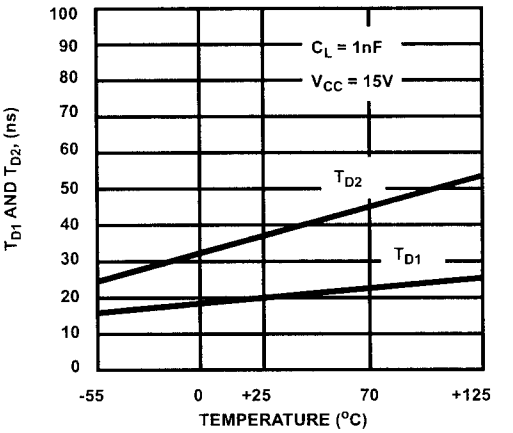


FIGURE 2. T_{D1}, T_{D2} vs TEMPERATURE

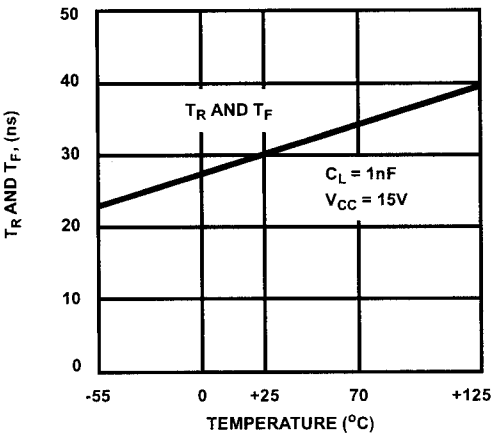


FIGURE 3. T_R, T_F vs TEMPERATURE

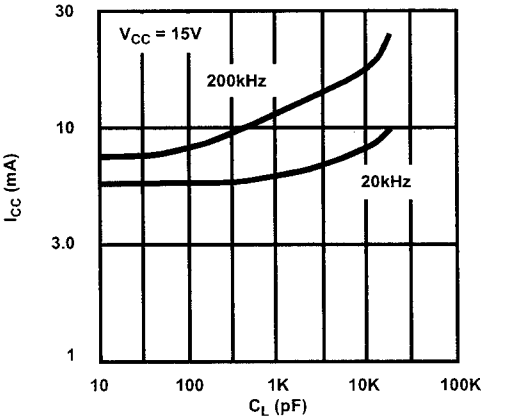


FIGURE 4. I_{CC} vs C_L

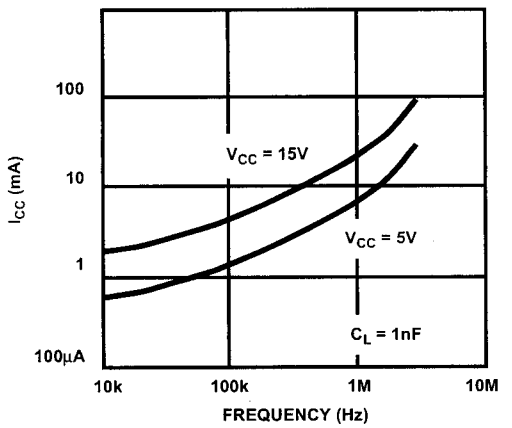


FIGURE 5. I_{CC} vs FREQUENCY

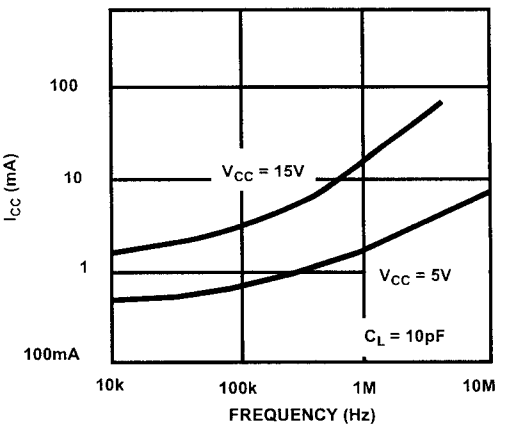


FIGURE 6. NO LOAD I_{CC} vs FREQUENCY

Typical Performance Curves (Continued)

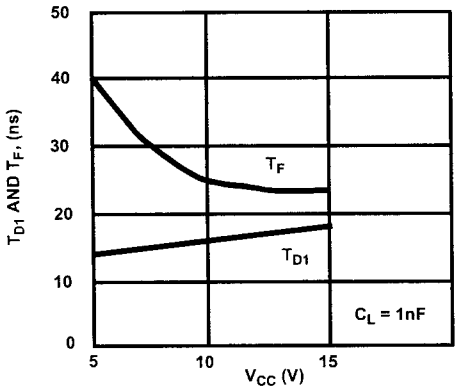


FIGURE 7. DELAY AND FALL TIMES vs V_{CC}

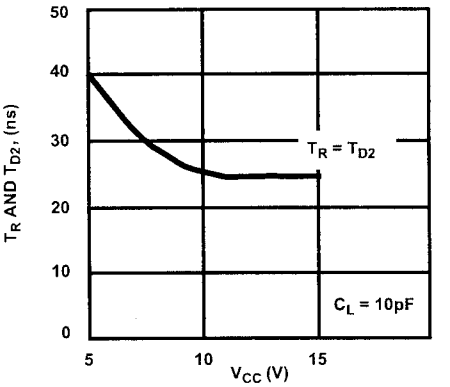


FIGURE 8. RISE TIME vs V_{CC}

Detailed Description

The ICL7667 is a dual high-power CMOS inverter whose inputs respond to TTL levels while the outputs can swing as high as 15V. Its high output current enables it to rapidly charge and discharge the gate capacitance of power MOSFETs, minimizing the switching losses in switchmode power supplies. Since the output stage is CMOS, the output will swing to within millivolts of both ground and V_{CC} without any external parts or extra power supplies as required by the DS0026/56 family. Although most specifications are at V_{CC} = 15V, the propagation delays and specifications are almost independent of V_{CC}.

In addition to power MOS drivers, the ICL7667 is well suited for other applications such as bus, control signal, and clock drivers on large memory of microprocessor boards, where the load capacitance is large and low propagation delays are required. Other potential applications include peripheral power drivers and charge-pump voltage inverters.

Input Stage

The input stage is a large N-channel FET with a P-channel constant-current source. This circuit has a threshold of about 1.5V, relatively independent of the VCC voltage. This means that the inputs will be directly compatible with TTL over the entire 4.5V - 15V V_{CC} range. Being CMOS, the inputs draw less than 1µA of current over the entire input voltage range of ground to V_{CC}. The quiescent current or no load supply current of the ICL7667 is affected by the input voltage, going to nearly zero when the inputs are at the 0 logic level and rising to 7mA maximum when both inputs are at the 1 logic level. A small amount of hysteresis, about 50mV to 100mV at the input, is generated by positive feedback around the second stage.

Output Stage

The ICL7667 output is a high-power CMOS inverter, swinging between ground and VCC. At V_{CC} = 15V, the output impedance of the inverter is typically 7Ω. The high peak current capability of the ICL7667 enables it to drive a 1000pF load with a rise time of only 40ns. Because the output stage impedance is very low, up to 300mA will flow through the series N-channel and P-channel output devices (from V_{CC} to ground) during output transitions. This crossover current is responsible for a significant portion of the internal power dissipation of the ICL7667 at high frequencies. It can be minimized by keeping the rise and fall times of the input to the ICL7667 below 1µs.

Application Notes

Although the ICL7667 is simply a dual level-shifting inverter, there are several areas to which careful attention must be paid.

Grounding

Since the input and the high current output current paths both include the ground pin, it is very important to minimize and common impedance in the ground return. Since the ICL7667 is an inverter, any common impedance will generate negative feedback, and will degrade the delay, rise and fall times. Use a ground plane if possible, or use separate ground returns for the input and output circuits. To minimize any common inductance in the ground return, separate the input and output circuit ground returns as close to the ICL7667 as is possible.

Bypassing

The rapid charging and discharging of the load capacitance requires very high current spikes from the power supplies. A parallel combination of capacitors that has a low impedance over a wide frequency range should be used. A 4.7µF tantalum capacitor in parallel with a low inductance 0.1µF capacitor is usually sufficient bypassing.

Output Damping

Ringing is a common problem in any circuit with very fast rise or fall times. Such ringing will be aggravated by long inductive lines with capacitive loads. Techniques to reduce ringing include:

1. Reduce inductance by making printed circuit board traces as short as possible.
2. Reduce inductance by using a ground plane or by closely coupling the output lines to their return paths.
3. Use a 10Ω to 30Ω resistor in series with the output of the ICL7667. Although this reduces ringing, it will also slightly increase the rise and fall times.
4. Use good bypassing techniques to prevent supply voltage ringing.

Power Dissipation

The power dissipation of the ICL7667 has three main components:

1. Input inverter current loss
2. Output stage crossover current loss
3. Output stage I^2R power loss

The sum of the above must stay within the specified limits for reliable operation.

As noted above, the input inverter current is input voltage dependent, with an I_{CC} of 0.1mA maximum with a logic 0 input and 6mA maximum with a logic 1 input.

The output stage crowbar current is the current that flows through the series N-channel and P-channel devices that form the output. This current, about 300mA, occurs only during output transitions. **Caution:** The inputs should never be allowed to remain between V_{IL} and V_{IH} since this could leave the output stage in a high current mode, rapidly leading to destruction of the device. If only one of the drivers is being used, be sure to tie the unused input to a ground. **NEVER** leave an input floating. The average supply current drawn by the output stage is frequency dependent, as can be seen in I_{CC} vs Frequency graph in the Typical Characteristics Graphs.

The output stage I^2R power dissipation is nothing more than the product of the output current times the voltage drop across the output device. In addition to the current drawn by any resistive load, there will be an output current due to the charging and discharging of the load capacitance. In most high frequency circuits the current used to charge and discharge capacitance dominates, and the power dissipation is approximately

$$P_{AC} = CV_{CC}{}^2f$$

where C = Load Capacitance, f = Frequency

In cases where the load is a power MOSFET and the gate drive requirement are described in terms of gate charge, the ICL7667 power dissipation will be

$$P_{AC} = Q_GV_{CC}f$$

where Q_G = Charge required to switch the gate, in Coulombs,
f = Frequency.

Power MOS Driver Circuits

Power MOS Driver Requirements

Because it has a very high peak current output, the ICL7667 the at driving the gate of power MOS devices. The high current output is important since it minimizes the time the power MOS device is in the linear region. Figure 9 is a typical curve of charge vs gate voltage for a power MOSFET. The flat region is caused by the Miller capacitance, where the drain-to-gate capacitance is multiplied by the voltage gain of the FET. This increase in capacitance occurs while the power MOSFET is in the linear region and is dissipating significant amounts of power. The very high current output of the ICL7667 is able to rapidly overcome this high capacitance and quickly turns the MOSFET fully on or off.

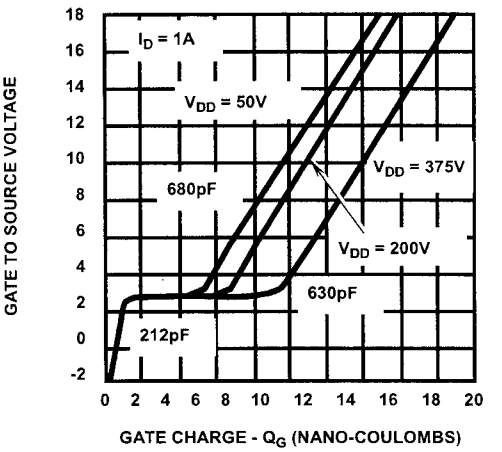


FIGURE 9. MOSFET GATE DYNAMIC CHARACTERISTICS

Direct Drive of MOSFETs

Figure 11 shows interfaces between the ICL7667 and typical switching regulator ICs. Note that unlike the DS0026, the ICL7667 does not need a dropping resistor and speedup capacitor between it and the regulator IC. The ICL7667, with its high slew rate and high voltage drive can directly drive the gate of the MOSFET. The SG1527 IC is the same as the SG1525 IC, except that the outputs are inverted. This inversion is needed since ICL7667 is an inverting buffer.

Transformer Coupled Drive of MOSFETs

Transformers are often used for isolation between the logic and control section and the power section of a switching regulator. The high output drive capability of the ICL7667 enables it to directly drive such transformers. Figure 11 shows a typical transformer coupled drive circuit. PWM ICs with either active high or active low output can be used in this circuit, since any inversion required can be obtained by reversing the windings on the secondaries.

Buffered Drivers for Multiple MOSFETs

In very high power applications which use a group of MOSFETs in parallel, the input capacitance may be very large and it can be difficult to charge and discharge quickly. Figure 13 shows a circuit which works very well with very large capacitance loads. When the input of the driver is zero, Q1 is held in conduction by the lower half of the ICL7667 and Q2 is clamped off by Q1. When the input goes positive, Q1 is turned off and a current pulse is applied to the gate of Q2 by the upper half of the ICL7667 through the transformer, T1. After about 20ns, T1 saturates and Q2 is held on by its own C_{GS} and the bootstrap circuit of C1, D1 and R1. This bootstrap circuit may not be needed at frequencies greater than 10kHz since the input capacitance of Q2 discharges slowly.

FAIRCHILD
SEMICONDUCTOR®

BC546/547/548/549/550

Switching and Applications

- High Voltage: BC546, V_{CEO}=65V
- Low Noise: BC549, BC550
- Complement to BC556 ... BC560

TO-92

1. Collector 2. Base 3. Emitter

NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings T_a=25°C unless otherwise noted

Symbol	Parameter		Value	Units
V_{CBO}	Collector-Base Voltage	: BC546	80	V
		: BC547/550	50	V
		: BC548/549	30	V
V_{CEO}	Collector-Emitter Voltage	: BC546	65	V
		: BC547/550	45	V
		: BC548/549	30	V
V_{EBO}	Emitter-Base Voltage	: BC546/547	6	V
		: BC548/549/550	5	V
I_C	Collector Current (DC)		100	mA
P_C	Collector Power Dissipation		500	mW
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C

Electrical Characteristics T_a=25°C unless otherwise noted

Symbol	Parameter		Test Condition	Min.	Typ.	Max.	Units
I_{CBO}	Collector Cut-off Current		V_{CB}=30V, I_E=0			15	nA
h_{FE}	DC Current Gain		V_{CE}=5V, I_C=2mA	110		800	
V_{CE} (sat)	Collector-Emitter Saturation Voltage		I_C=10mA, I_B=0.5mA		90	250	mV
			I_C=100mA, I_B=5mA		200	600	mV
V_{BE} (sat)	Base-Emitter Saturation Voltage		I_C=10mA, I_B=0.5mA		700		mV
			I_C=100mA, I_B=5mA		900		mV
V_{BE} (on)	Base-Emitter On Voltage		V_{CE}=5V, I_C=2mA	580	660	700	mV
			V_{CE}=5V, I_C=10mA			720	mV
f_T	Current Gain Bandwidth Product		V_{CE}=5V, I_C=10mA, f=100MHz		300		MHz
C_{ob}	Output Capacitance		V_{CB}=10V, I_E=0, f=1MHz		3.5	6	pF
C_{ib}	Input Capacitance		V_{EB}=0.5V, I_C=0, f=1MHz		9		pF
NF	Noise Figure	: BC546/547/548	V_{CE}=5V, I_C=200μA		2	10	dB
		: BC549/550	f=1KHz, R_G=2KΩ		1.2	4	dB
		: BC549	V_{CE}=5V, I_C=200μA		1.4	4	dB
		: BC550	R_G=2KΩ, f=30~15000MHz		1.4	3	dB

h_{FE} Classification

Classification	A	B	C
h_{FE}	110 ~ 220	200 ~ 450	420 ~ 800

Typical Characteristics

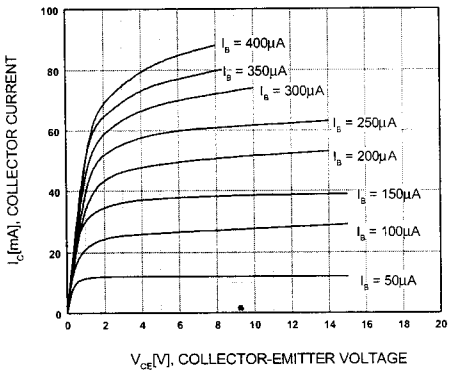


Figure 1. Static Characteristic

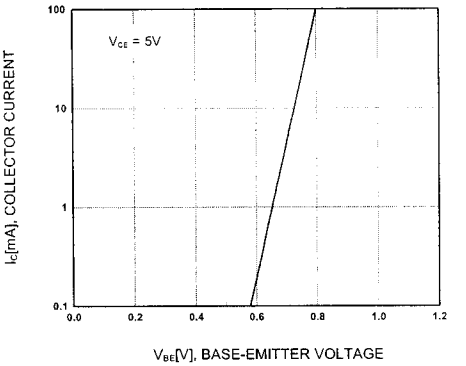


Figure 2. Transfer Characteristic

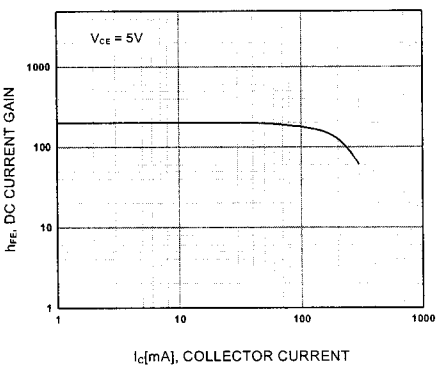


Figure 3. DC current Gain

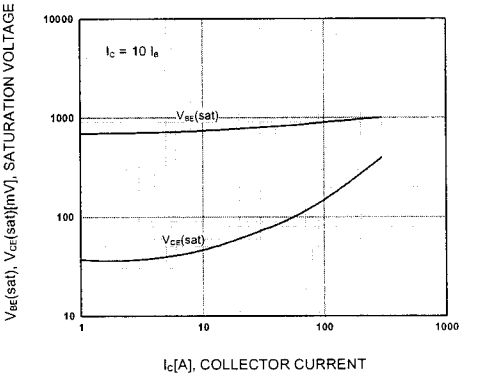


Figure 4. Base-Emitter Saturation Voltage Collector-Emitter Saturation Voltage

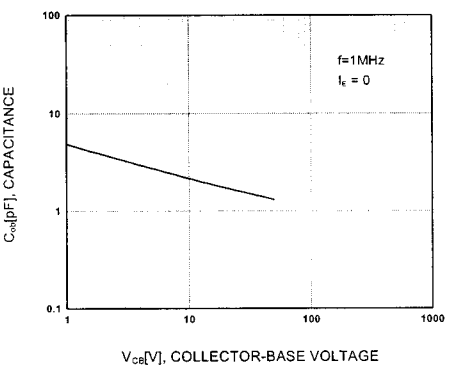


Figure 5. Output Capacitance

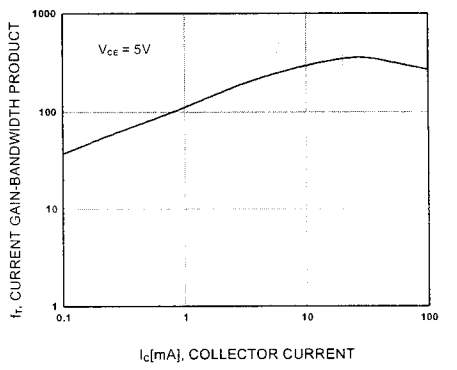


Figure 6. Current Gain Bandwidth Product

APPENDIX 3 - PHOTOGRAPH

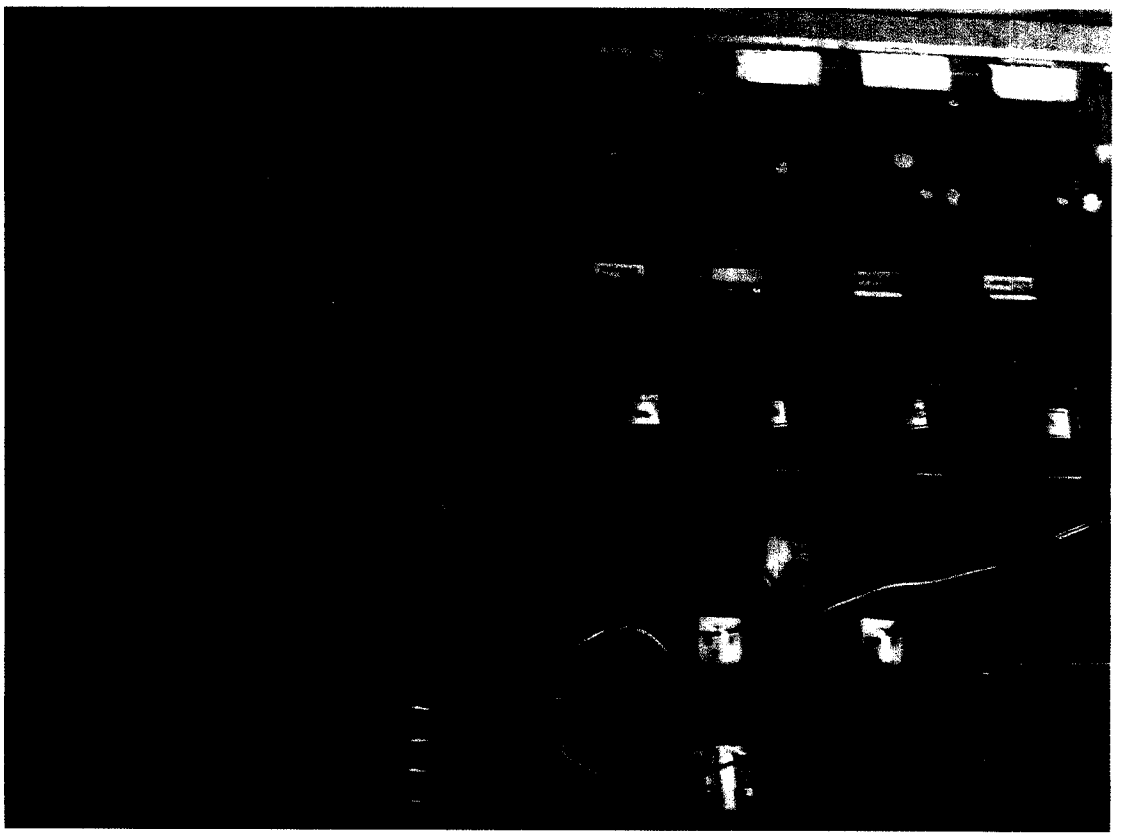


Fig A 3.1 Circuit Photograph-1

Fig A 3.2 Circuit Photograph-2