CRT CONTROLLED CHARACTER DISPLAY

PROJECT REPORT

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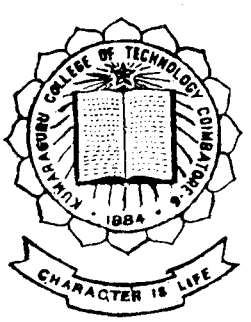

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PROJECT WORK

Register Number .....

This is to certify that the Project entitled

CRT CONTROLLED CHARACTER DISPLAY

has been submitted by

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Guide

Head of the Department

Submitted for the Viva-Voce examination held on.....

Internal Examiner

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DEDICATED TO MY

BELOVED PARENTS

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SYNOPSIS

The unit proposed here is a micro processer based CRT display terminal capable of supplying RS 232 or inverted TTL ASCII data. Designing such a terminal is possible with SSI chips but require a large number of IC's and system becomes bulky and difficult to trouble shoot. This can be over come by Micro Processor based terminal.

In this, data to be displayed are to be stored in the EPROM chip. With the help of Buffer and ROM, Micro Processor will process the data and send it to the CRT controller which is used in interface the system to the monitor. The width of dot and character are determined by the dot clock frequency. The 8 bit data from the character generator in the parallel form is convered to serial form by parallel input serial output shift register. The shift register is clocked at the dot clock rate and its output constitute the video input to the CRT.

The unit can be used as a teaching aid. It may be of interest to the deaf and hard of hearing. It is used in advertising purpose.

It is more flexible for future expansion and modification. It can be easily interfaced with any host computer. It can display the characters in TV screen with slight modification at the output.

CONTENTS

CONTENT

INTRODUCTION

CHAPTER-I

INTRODUCTION

Display of information will be required in a variety of applications involving calculating machines, computer systems, data retrieval systems, data communications systems and many other areas.

There are many types of display systems :

(i) CRT Displays (ii) LED Displays (iii) LCD Displays and so on. A CRT alphanumeric display is a recent development in display technique. Light emitting didode (LED) and Liquid Crystal Diode (LCD) displays are not used much commonly because the cost of LED is highand in the case of LCD, we need an external light and the ambient temperature of operation is limited. So CRT display is chosen almost always for large area displays owing to its merits of brightness, uniformity, low cost and high reliability.

Sometimes, in off-the-air television pictures, we see rows of alphanumeric message on tables-usually before news on forecast programmes. These message lines are obtained with a video chamera which is aimed upon messages that are written on paper on placards. But, when a microcomputer uses a TV as a peripheral display to write messages on the screen, the method of generating the video is entirely different (because no camera is

involved here), though the final video signal from the camera and that obtaine din the micro computer would be similar. The message words in the latter case are stored codes in digital memory chips corresponding to the alphanumeric characters it displays on the screen. Thus, the requirement is that of placing the 'digital words' in the form of several rows on the screen each row containing several characters.

In this project, we have developed a microprocessor based CRT display terminal. Normally designing a terminal with Integrated Circuits (MSI) will require large number of IC's and the system becomes complex and difficult to troubleshoot. But this can be overcome by a microprocessor based Terminal. Moreover, this type of system is more flexible for future expansion and modification. Also the system becomes more versatile and it can be easily interfaced with any host computer.

In our present work, the complete details for making an Add-on board which is interfaced to the microprocessor kit are given describing the elements of techniques, circuitry and application details so as to get a 20-line display of alphanumeric informatin on a T.V monitor on a solid state TV set with a modulator.

SYSTEM DESCRIPTION

CHAPTER - II

SYSTEM DESCRIPTION

2.1 CRT Basics

The image displayed on the CRT is built up by generating a series of lines across the face of the CRT. Usually the beam starts in the upper left hand corner of the display and simultaneously moves from left to right and from top to bottom to put a series of Zig Zag lines on the screen.

The simultaneously operating independent circuits control the vertical and horizontal movement of the beam. When the beam reaches the end of the line it is brought back to the beginning of the next line which is done much faster during which the electron beam is usually shut off. This action is referred to as "retrace".

When the beam finally reaches the bottom right hand of the screen it retraces vertically back to the top left hand corner. The time it takes for the beam to move from the top of the screen to the bottom and back again to the top is referred to as a "Frame".

The CRT itself can track a horizontal frequency between 15250 Hz and 16250 Hz or in other words, there can be 256

to 270 horizontal lines per vertical frame. The vertical frequency should be 50 Hz to ensure stability.

Scanning

In an interlaced system the line sets are not generated simultaneously. In a 50 Hz system first all the odd numbered lines are scanned (i.e) 1,3 ...625 then all the even numbered lines are scabbed (i.e) 0,2,4...624. Each set of lines usually contain different data. Interlacing provides data resolution. It also has some distinct disadvantages.

First of all, the circuitry needed to generate the extra half horizontal line per frame is quite complex when compared to a non interlaced design. Next the overall vertical refresh is half as that of a non interlaced display. As a result flicker may result when the CRT uses high speed Phosphors. The characters that are viewed on the screen are found by a series of dots that are shifted out of the controller where the electron beam moves across the face of the CRT. The circuit that creates this timing are referred to as the dot clock and character clock.

The character clock is equal to the dot clock divided by the number of dots used to form a character along the horizontal axis.

2.2 8275 Description

2.2.1 CRT Display Refreshing

The 8275 having been programmed for a specific screen format generates a series of DMA request signals, resulting in the transfer of a row of characters from display memory to the 8275 row buffers. The 8275 presents the character codes to an external character generator ROM by using outputs CC0-CC6. External dot timing logic is then used to transfer the parallel output data from the character generator ROM serially to the video input of the CRT. The character rows are displayed on the CRT one line at a time. Line count outputs LC0-LC3 are applied to the character generator ROM to perform the line selection function.

Proper CRT refreshing requires that certain 8275 parameters be programmed prior to the beginning of the display operation. The 8275 has two types of programming registers. The command registers (CREG) and the parameter registers (PREG). It also has a status register (SREG). The command registers may only be written into and the status registers only be read. The 8275 expects to receive a command followed by a sequence of 0 to 4 parameters depending on the command.

To establish the format of display the 8275 provides a number of user programmable display format parameters. Display formats having 1 to 80 characters per row, 1 to 64 rows per screen and 1 to 16 horizontal lines per row are available.

In addition to transferring from memory to the CRT screen the 8275 features cursor position control. The cursor position may be programmed via x and y cursor position registers to any character position on the display. The user may select from 4 cursor formats. Blinking and non blinking, underline and reverse video block cursors are available.

2.2.2. CRT Timing

The 8275 provides two timing outputs, HRTC and VRTC which are utilised in synchronising CRT horizontal and vertical oscillators to the 8275 refresher cycle. In addition whenever HRTC or VRTC is active, a third timing output, VSP (vieo supress) is there providing a blinking signal to the dot timing logic. The dot timing logic will normally inhibit a video output to the CRT during the time when VSP signal is true. An additional timing output LTEN is used to provide the ability to produce the video output high regardless of the state of VSP. This feature is used by the 8275 to place a cursor on the screen and control up to date functions.

2.2.3 Using the 8275 without DMA

The only real concern with using the 8275 in an interrupt-driven transfer mode is speed. Eighty characters must be loaded into the 8275 every 617 microseconds and the processor must also have time to perform all the other tasks that are required. To minimise overhead associated with loading the characters into the

8275, a special technique was employed. This technique involves setting a special transfer bit and executing a string of POP instructions. The string of POP instructions is used to rapidly move the data from memory into the 8275.

In this design the 8085's SOD line was used as the special transfer bit. In order to perform the transfer properly this special bit must do 2 things - 1) turn processor reads into $\overline{DACK}$ plus $\overline{WR}$ for the 8275; and 2) mask processor fetch cycles from the 8275, so that a fetch cycle does not write into the 8275, so that a fetch cycle does not write into the 8275. Conventional logic could have been used to implement this special function, but in this design a small bipolar programmable read only memory was used.

At first, it may seem strange that we are supplying a $\overline{DACK}$ when no DMA controller exists in the system. But as we know that all intel peripheral devices that have DMA lines actually use $\overline{DACK}$ as a chip select for the data, so when you want to write a command or read status, we assert $\overline{CS}$ and $\overline{WR}$ or $\overline{RD}$, but when we want to read or write data we assert $\overline{DACK}$ and $\overline{RD}$ or $\overline{WR}$. The peripheral divice does not know if a DMA controller is in the circuit or not. $\overline{DACK}$ and $\overline{CS}$ should not be asserted on the same time, since this combination yields an undefined result.

The POP technique actually compares quite favourably in terms of time to the DMA technique. One POP instruction transfers two bytes of data to the 8275 and takes 10 CPU clock

cycles to execute at a net transfer rate of 1 byte every five clock cycles. The DMA controller takes 4 clock cycles to transfer 1 bit but sometime is lost in synchronisation so the difference between two techniques is 1 clock cycle per byte maximum.

2.2.4 8275 - Programmable CRT Controller

Functional Description :

Data Bus Buffer :

This is a 3 state bidirectional 8 bit bufer which is used to interface 8275 to the system data bus. This functional block accepts inputs from the system control bus and generates control signals for overall device operation. it contains the command parameter and status register that stores various control formats for the device functional definition.

$\overline{RD}$ (READ)

A 'low' on this input informs the 8275 that the CPU is reading data or status information from the 8275.

$\overline{WR}$ (WRITE)

A 'low' on this input informs the 8275 that the CPU is writing data or control words to the 8275.

$\overline{CS}$ (CHIP SELECT)

A 'low' on this input selects the 8275. No reading or writing will occur unless the device is selected. When the CS is

high, the data Bus is in the float state and RD and WR will have no effect on the chip.

DRQ (DMA REQUEST)

A 'high' on this output informs the DMA controller that the 8275 desires a DMA transfer.

$\overline{\text{DACK}}$ (DMA ACKNOWLEDGE)

A 'low' on this input informs the 8275 that a DMA cycle is in progress.

IRQ (INTERRUPT REQUEST)

A 'high' on this output informs the CPU that the 8275 desires interrupt service.

CHARACTER COUNTER

A character Counter is programmable counter that is used to determine the number of characters to be displayed per row and the length of the horizontal retrace inteval. It is driven by the CCLK (Character Clock) input which should be a derivative of the external dot clock.

FIFO'S

These are two 16 character FIFO'S in the 8275. They are used to provide extra row buffer length in the transparent attribute modes.

BUFFER INPUT/OUTPUT CONTROLLERS

The Buffer input/output controllers decode the characters being placed in the row buffers. if the character is a character attribute, field attribute or special code, these controllers control the appropriate action.

SYSTEM OPERATION

The 8275 is programmable to a large number of different display formats. It provides raster timing, display row buffering, visual attribute decoding, cursor timing and light pen detection.

It is designed to interface with the 8257 DMA controller and standard character generator ROM's for dot matrix decoding. Dot level timing must be provided by external circuitry.

GENERAL SYSTEM'S OPERATIONAL DESCRIPTION

The 8275 provides a "window" into the micro computer system memory.

Display characters are retrieved from memory and displayed on a row by row basis. The 8275 has two row buffers. While one row buffer is being used for display, the other is being filed with the next row of characters to be displayed. The number of display characters per row and the number of charcter rows per frame are software programmable providing easy interface to most CRT displays.

The 8275 requests DMA to fill the row buffer that is not being used for display. DMA Burst length and spacing are programmable.

The 8275 displays character rows one line at a time.

The 8275 also controls raster timing. This is done by generating horizontal retrace (HRTC) and vertical retrace (VRTC) signals The timing of these signals are programmable.

The 8275 can generte a cursor. Cursor locations and formats are programmable.

The 8275 has a light pen input and registers. The light pen input is used to load the registers. Light pen registers can be read as command.

DISPLAY FORMAT

SCREEN FORMAT

The 8275 can be programmed to generate from 1 to 80 characters per row and from 1 to 64 rows per frame. The 8275 can also be programmed to blank alternate rows. In this mode the first row is displayed, the seocnd blanked the third displayed etc.

ROW FORMAT

The 8275 is designed to hold the line count stable while outputting the appropriate character codes during each horizontal sweep. The line count is incremented during horizontal retrace and the whole row of character codes are output again during the next sweep. This is continued until the whole character row is designed.

DOT FORMAT

Dot width and character width are dependant upon the external timing and control circuitary.

Dot level timing circuitary should be designed to accept the parallel output of the character generators and shift it out serially at the rate required by the CRT display.

Dot width is a function of dot clock frequency. Character width is a function of character generator width. Horizontal charcter spacing is a function of shift register length.

RASTER TIMING

The character counter is driven by the character clock input. It counts out the characters being displayed. It then causes the line counter to increment and it starts counting the horizontal retrace interval. This is constantly repeated.

The line counter is driven by the character counter. It is used to generate the line address outputs (LC0-3) for the character generator. After it counts all the lines in the character row, it increments the row counter and starts over again.

The row counter is an internal counter driven by the line counter. It controls the function of the row buffers and counts the number of character rows displayed.

After the row counter counts all the rows in a frame, it starts counting out the vertical retrace interval. The video suppression output (VSP) is active during horizontal and vertical retrace intervals. Dot level timing circuitry must synchronise these outputs with the video signal to the CRT display.

VISUAL ATTRIBUTES AND SPECIAL CODES

The characters processed by 8275 are 8 bit quantities. There are 2 types of visual attribute codes. They are character attributes and field attributes.

CHARACTER ATTRIBUTE CODES

Character attribute codes are codes that can be used to generate graphic symbols without the use of a character generator. This is accomplished by selectively the line attibute outputs (LA0-1), the video suppression output (VSP) and light

enable output. The dot level timing circuitry can be use these signals to generate the proper symbols.

Chracter attributes can be programmed to blink or be highlighted individually. Blinking is accomplished with the video suppression output (VSP). Blink frequency is equal to the screen refresh frequency divided by 32. Highlighting is accomplished by activating the highlight output (HGL T).

FIELD ATTRIBUTES

The field attributes are control codes which affect the visual characteristics for a field of characters. There are six field attributes.

1) BLINK:

Characters following the code, blink by activating the VSP. The blink frequency is equal to the screen refresh frequency divided by 32.

2) HIGHLIGHT:

Characters following the code are highlighted by activating the highlight output (HGL T).

3) REVERSE VIDEO:

Characters following the code appear with reverse video by activating the reverse video output.

4) UNDERLINE:

Characters following the code are underlined by activating the LTEN output.

5),6) GENERAL PURPOSE:

There are two additional 8275 outputs which act as general independently programmable field attributes. GPAO-1 are active high outputs.

FIELD FIND CHARACTER ATTRIBUTE INTERACTION

Character attribute symbols are affected by reverse video and general purpose field attribute. They are not affected by unerline, blink or highlihgt.

CURSOR TIMING:

The cursor location is determined by a cursor row register and a character position register which are located by commands to the controller. The cursor can be programmed to appear on the display as:

1) a blinking underline
2) a blinking reverse video block
3) a non blinking underline
4) a non blinking reverse video block

The cursor blinking frequency is equal to the screen refresh frequency divided by 16.

2.3. Prom (82S123) Decoding

The logic necessary to convert the 8275 into a non-DMA type of device was performed by a single small bipolar PROM. Besides turning certain processor READS into DACKS and WRITES forthe 8275. this 32 by 8 PROM decodes addresses for the system RAM, ROM as well as for the 8255 parallel 1/O port.

Any bipolar PROM that has a by eight configuration could function in this application. This particular device was chosen simply because it is the only "by eight" PROM available in a 16 pin package. The connection of the PROM is shown in detail in the figure and its truth table is also shown. Note that when a fetch cycle (M1) is not being performed, the state of the SOD line is the only thing that determines if memory needs will be written into the 8275's row buffer. This is done by pulling both DACK and WRITE low on the 8275.

Futures

Address accers time	= 35 sec max.
Power dessipation	= 1.3 mW/bit.
Fully TTL compatible.	

Applications

1. Sequential controller.
2. Random logic.

TRUTH TABLE FOR 82S123

NI	A12	A11	A10	SOD		8275 $\overline{RD}$	8275 $\overline{CS}$	8275 $\overline{DACK}$	8275 $\overline{WR}$	$\overline{6116}$	$\overline{2716}$
A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	1	1	1	1	1	1	0
0	0	0	0	1	1	1	1	1	1	1	1	0
0	0	0	1	0	1	1	1	1	1	1	1	0
0	0	0	1	1	1	1	1	1	1	1	1	0
0	0	1	0	0	1	1	1	1	1	1	1	0
0	0	1	0	1	1	1	1	1	1	1	0	1
0	0	1	1	0	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	0	1
0	1	0	0	0	1	1	1	1	1	1	0	1
0	1	0	0	1	1	1	1	0	1	0	1	1
0	1	0	1	0	1	1	1	0	1	0	1	1
0	1	0	1	1	1	1	0	0	1	1	1	1
0	1	1	0	0	1	1	0	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	1	1	1
0	1	1	1	0	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	0	1	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0
1	0	0	1	0	1	1	1	1	0	0	1	0
1	0	0	1	1	1	1	1	1	1	1	1	0
1	0	1	0	0	1	1	1	1	0	0	1	0
1	0	1	0	1	1	1	1	1	1	1	0	1
1	0	1	1	0	1	1	1	1	0	0	0	1
1	0	1	1	1	1	1	1	1	1	1	0	1
1	1	0	0	0	1	1	1	1	0	0	0	1
1	1	0	0	1	1	1	1	0	1	0	1	1
1	1	0	1	0	1	1	0	0	1	0	1	1
1	1	0	1	1	1	1	0	0	1	1	1	1
1	1	1	0	0	1	1	0	0	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1
1	1	1	1	0	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1

2.4. Chracter Generator

The character generator used in this terminal is a 2716 EPROM. The three low-order line count outputs (LC0-LC2) from the 8275 are connected to the three low order address lines of the character generator and the seven characer generator outputs (CC0-CC6) are connected to the A3-A9 of the character generator. The output from the character generator is loaded into a shift register and the serial output from the shift register is the video output of the termial.

Now let us assume that the letter E is to be displayed. The ASCII code for E is 45H. So 45H is presented to address lines A2-A9 of the character generator. The scan lines will now count each line from 0 to 7 to form the character. This same procedure is used to form all 128 possible characters.

It should be obvious tht "custom" character fonts could be made by just changing the bit pattern in the character generator PROM.

45H = 01000101

Address to PROM = 01000101 SL 2 SL1 SL0

= 228H - 22FH

CHARACTER GENERATOR OUTPUT

ROM ADDRESS	ROM HEX OUTPUT	BIT OUTPUT 0	1	2	3	4	5	6	7
228H	3E		*	*	*	*	*		
229H	02		*						
22AH	02		*						
22BH	0E		*	*	*				
22CH	02		*						
22DH	3E		*						
22EH	0C		*	*	*	*	*		

Bits 0, 6 and 7 are not used.

2.5. Description of 8085

The 8085 is the heart of the circuit. It is the LSI microprocessor chip. It needs only a single +5V supply for its working. It has a built in timing oscillator and works by connecting a crystal between its pin Numbers 1 and 2. The frequency upto which it can be worked is generally 6mHz, but we are making use of 3.127 MHz crystal.

In the 8085 chip, the low order byte of address bus is multiplexed with the data byte.

Therefore the lower order address byte has to seperate from the data byte to obtain the 16 line address bus and 8 line data bus. The 8212, latch 12 used for this purpose. The 8085 generates a positive pulse at pin 30 known as ALE (Address Latch Enable). Using this pulse, we latch the low order address lines in 8212.

Next the standard control bus consists of

a) Memory Read (bar) - MR.

b) Memory write (bar) - Mw.

c) Input part (bar) - IN.

d) Output part (bar) - OUT.

e) IN terrupt Acknowledge (bar) - INTA.

Memory Read (bar) means that memory's Read when this line goes low.

INTA is available from the 8085 chip itself. But MR, Mw, IN and OUT are not directly available. Instead there are only 3 lines from the 8085 chip namely 10/M, RD and WR. By using one 7400 and one 7404, we can seperate the 4 control lines MR,Mw, IN and OUT.

The 8085 chip has 40 pins, it is esential to clearly understand each pin is to be connected. Let us first account for the 40 pins.

High order address lines (OUT)	- 8 pins
Low order address and data (OUT)	- 8 pins
Address latch enable out	- 1 pin
+5V and ground line (IN)	- 2 pin
Crystal for oscillator (IN)	- 2 pin
INTERRUPT input pins (IN)	- 5 pins
Interrupt acknowledge pins (IN)	- 1 pin
HOld (DMA) IN	- 1 pin
Hold acknowledge (DMA OUT)	- 1 pin
Reset (input)	- 1 pin
Reset out	- 1 pin
Clock out	- 1 pin
10/M, RD and MR (OUT)	- 3 pin

Status lines (out)	- 2 pins
Ready (in)	- 1 pin
Serial date (IN)	- 1 pin
Serial data (OUT)	- 1 pin

Detail of 8085 :

S_0 and S_1 are status lines, which along with 10/M provides information regarding the nature of the Job, that the Cpu is executing.

0	0	1	- Memory write
0	1	0	- Memory read
1	0	1	- 1.0 write (OUT)
1	1	0	- 1.0 Read (IN)
0	1	1	- OP - code fetch
1	1	1	- interrupt acknowledge
*	X	X	- Hold
*	X	x	- Reset
*	0	0	- Halt

* = 3 state (high impedance)

x = Unspecified

READ (INPUT) : Should be high for normal memory Read/write opertion. If taken low, the Cpu will wait (normally tied to +5V).

RESET (INPUT) : Should be normally high. When taken low, the Cpu is Reset.

RESET (OUT) : Can be used as system reset.

CLOCK OUT : Has half the crystal frequency and can be used as the system clock.

SID (SERIAL INPUT DATA) : The data on this line is loaded into the accumulator D_7 whenever RIM (Reset interrupt mask) instructinis executed.

SOD (SERIAL OUTPUT DATA) : This is set or reset as specified by the SIM instruction

All Reset and interrupt lines are normally at 0 and when taken high, interrupt occurs.

Interrupt Priority Table

TRAP

RST 7.5

RST 6.5

RST 5.5

INTR.

(INTR INPUT) interrupt request is used as a general purpose interrupt. It is disabled by RESET and immediately after a interrupt is accepted. It is also enabled and disabled by software.

2.6 Display RAM: 6116

This [6116 - a 2K x 8 RAM memory] is used to store two set of 1024 words. This must be loaded with required messages using a microprocessor chip 8085. This form part of the total microprocessor memory and is addressable both by the microprocessor as well as the CRT controller. Only when one reads or writes a message word into this memory does the microprocessor select this RAM. At all other times the CRT controller only repeatedly reads its words sequentially to form rows with characters on the screen.

2.7 Address Buffer (8212)

In the 8085 chip the low & order byte of address bus is multiplexed with the date byte.

Therefore the low order address byte has to be seperated from the data byte to obtain the 16 line address bus and 8 line data bus. The 8212 address buffer is used for this purpose. The 8085 genertes a positive pulse at pin 30 known as ALE (Address Latch Enable) using this pulse. We latch the low order address lines in 8212.

The microprocessor data is connected to the data lines of the RAM Via address buffer 8212.

Since the data lines can be either in Read or Write mode a address buffer is needed for the data bus. Its direction control selects the direction according to Reading or Writing mode, while the enable line enables the buffer, if the microprocessor wants to Read/Write into the RAM.

2.8 Shift Register

This shift register shifts the data sent from the character generator in 8 bit parallel form into a sertal form. ie one bit after another so, this is called as parallel input serial output (PISO) shift register. The dot pattern comes out of the shift register one by one. This IC has in addition to the 8 bit parallel input and pair of output lines (Q and $\overline{Q}$) a load pin which loads the parallel data into the 8 bit shift register and a clock input pin which is the serial dot clock.

2.9 Counter: 74163

Like shift registers. Counters are composed primarily of flip flops with a samll amount of added combinational logic. The main control input of the counter is the count in line. When the counter is enabled, a pulse on count in line causes the transformation.

$z = z+1$, that is, it increments the count by one. Since the count in line triggers a single state change in the counter, it is also called the clock signal. A sequence of pulses on count in line makes the counter pass through a sequence of states and hence the counter effectively counts the number of pulses applied to its count in line. 74163 a synchronous counter is wired to dividethe clock by eight. So that each character slot occupies 8 dots. Its output is given to the CRT Controller Chip to tell it that the next character is on the way.

2.10 Hardware Description

The "heart" of the CRT terminal is the 8085 microprocessor. The 8084 initialises all devices in the system, loads the CRT controller, assembles the characters to be transmitted, decodes the incoming characters and determines where the character is to be placed on the screen.

The 8275 is used as the CRT controller in the system, and a 2716 is used as the character generator. To handle the high speed portion of the terminal the 8275 is surrounded by a small handful of TTL gates. The programme memory is contained in one 2716 EPROM and the data and screen memory use 6116 type RAM.

All decices in this system are memory mapped. A bipolar PROM is used to decode all of the addresses for the RAM, ROM and the 8275. The bipolar PROM also turns $\overline{\text{READS}}$ into $\overline{\text{DACKS}}$ and $\overline{\text{WRITES}}$ for the 8275. If this same terminal were designed using MCS-85 family of integrated chips additional port savings could have been realised.

Video RAM (6116) address lines are connected to microprocessor and CRT controller address lines via buffer, except when required by the micro-processor video RAM continuosly being addressed by the address lines A0-A9 of CRT controller. This words emerge one by one from memory chip and get latched by 74175.

The parallel input data from the EPROM is converted to serial data by parallel input serial output synchronous shift register. The Dot clock determines the width of dot and character and the output from the PISO gives the required video informatin for CRT.

SYSTEM OPERATION

CHAPTER - III

SYSTEM OPERTION

3.1 System Functioning

The 8085 CPU initialises each peripheral to the appropriate mode of opertion following system reset. When a character has been received, the 8085 decodes the character and takes appropriate action. While the 8085 is executing the above "foreground" programs it is being interrupted once every 617 microseconds by the 8275. This "background" program is used to load the row buffers on the 8275 is also interrupted once every frame time to read the status of 8275.

A special POP technique is used to rapidly move the contents of the display RAM into the 8275's row buffers. The characters are then synchronously transferred to the character code outputs CC0 - CC6. Connected to the character generator are address lines A3-A9. Line count outputs LCo-LC2 from the 8275 is applied to the character generator address lines A0-As. The 8275 displays character rows one line at a time. The line count outputs are used to determine which line of character selected by A3-A8 will be displayed. Following the transfer of the first line to the dot timing logic the line count is incremented and the second line of the charcter row is selected. The process continues until the last line of the row is transferred to the dot timing logic.

The dot timing logic latches the output of the character genertor ROM into a parallel in serial out synchronous shift register. The shift register is clocked at the dot clock rate (12.48 MHz) and its output constitutes the video input to the CRT.

ROUTINE TO LOAD 8275's ROW BUFFERS

Clock Cycles	Seq.	Source Statement	
10	1	PUSH PSW	Save A and Flags
10	2	PUSH H	Save H and L
10	3	PUSH D	Save D and E
10	4	LXI,0000H	Load Zero into H and L
10	5	DAD SP	Put stack pointer in H and L
4	6	XCHG	Put stack in D and E
16	7	LHLD	Get pointer
6	8	SPHL	Put current line into SP
7	9	MVI A,0000H	Set mask for SIM
4	10	SIN	Set special transfer bit
400	11	POP H	Do 40 POPS
4	12	RRC	Set up A
4	13	SIM	Go back 10 normal mode
10	14	LXI H,0000H	Zero H,L
10	15	DAD SP	Stack
4	16	XCHG	Put stack in H and L
6	17	SPHL	Restore Stack
10	18	LXI H,LAST	Put bottom in H and L
4	19	XCHG	Swap registers
4	20	MOV A,D	Put high of DEP in A
4	21	CMP H	See it same as H
7/10	22	JNZ KPTK	If not leave
4	23	MOV A.E	Put low order in A
4	24	CMP L	See it same as L
7/10	25	JNZ KPTK	If not leave
10	26	LXI H,TPDIS	H and L with top of screen return
16	27	KPTK:SHLD	Put back current address
7	28	MVI A,18H	Get mask Byte
4	29	SIM	Set interrupt mask
10	30	POP D	Get D and E
10	31	POP H	Get H and L
10	32	POP PSW	Get A and Flags
4	33	EI	Enable interrupts
10	34	RET	Go back

Total number of clock cycles = 650 (Worst case) with a 6.144 crystal total time to fill Row Buffer on 8275 = 650 x .325 = 211.25 microseconds.

3.2 System Timing

Each character is displayed on a 8 x 8 field and is formed by a 5 x 7 dot matrix. The 8275 allows the vertical retrace time to be only an integer multiple of the horizontal charcter line. This means that the total number of horizontal line in a frame equals 12 times the number of character lines plus the vertical retrace time, which is programmed to be either 1, 2, 3 or 4 character lines. Twentyfive display lines require 300 horizontal lines. So, if we wish to have a horizontal frequency in the neighbourhood of 15750 Hz we must choose two character lines for vertical retrace. This choice yields a net 300+ 24 = 324 horizontal lines per frame. So assuming a 50Hz frame the horizontal frequency must be = 50Hz x 324 = 16200 Hz. This value falls within our target specification of 15750 Hz with $\pm$ 500Hz variation (i.e) between 15250 Hz and 16250 Hz.

It is now known that the terminal is using 300 lines to display data and 24 horizontal lines to allow for vertical retrace and the horizontal frequency is 16200Hz. In this design 80 charcter can be displayed on a horizontal line and was empirically found that allowing 20 horizontal character lines for retrace gave the best results. So in reality there are 100 character lines. It should be noted that if too many character lines are used for retrace less time will be left to diaplay the character and the display will not "fill out" the screen. Conversely, if not enough character lines are allowed for retrace the display may "run off" the screen.

DESIGN OF DOT CLOCK

CHAPTER - IV

DESIGN OF DOT CLOCK

Method: 1

The number of lines per frame can be determined by the following equation.

$$L = (H \times Z) + V$$

H - number of horizontal lines per character = 12

Z - number of rows to be displayed = 25

V - number of horizontal lines during vertical retrace = 24

Therefore L = (25x12) + 24

L = 324 lines per frame

The DOT CLOCK is calculated from the equation given below.

DOT CLOCK (Hz) = (N+R) X D X L X F

N - number of displayed charactes per row = 80

R - number of retrace character time increments = 20

D - number of dots per character = 8

L - number of horizontal lines per frame = 324

F - the frame rate in Hz = 50

Therefore DOT CLOCK (Hz) = (80+20) x 8 x 324 x 50

DOT CLOCK = 12.96 mHz.

Method: II

The horizontal frequency is calculated as given below.

Horizontal frequency = frame rate mHz x Number of horizontal lines per frame

= 50 Hz x 324

= 16200 Hz.

Total time for one horizontal line = 1/16,200 Hz

= 61.7 micro seconds

Vertical retrace time = 61.7 micro seconds X 24 horizontal synch times

= 1.48 milliseconds.

One hundred Character times per complete horizontal line means that each charcter requires.

61.7 micro-seocnds/100 character times = 617 nanoseconds.

Therefore horizontal retrace time = 617 nsec x 20 retrace times

= 12.34 microseconds.

Now, the 617 nanosecond character clock period is known and the dot clock period is easy to calculate. Here each character is formed by placing 8 dots along the horizontal line.

Dot clock period = Character clock/8 dots

= 617 nsec/8

= 77.125 nanosec.

Therefore dot clock frequency = 1/77.125 nanosec.

DOT CLOCK FREQUENCY = 12.96 mHz.

SYSTEM SOFTWARE

PROGRAM TO BLANK DISPLAY RAM

0000	LXIH, 0800H	21,00,08
0003	MVI B,OFH	06,OF
0005	MVI C,FFH	OE,FF
0007	XYZ: LDA 20H	3A,20
0009	MOV M,A	77
000A	INX 4	23
000B	MOV A,B	78
000C	CMP H	BC
000D	JNZ XYZ	C2,07,00
0010	MOV A,C	79
0011	CMP L	BD
0012	JNZ XYZ	C2,07,00

PROGRAM TO MOVE ONE BLOCK OF MEMORY FROM 2716 TO DISPLAY RAM

0015	LXID OBE6H	11,E6,OB
0018	LXIH 0500H	21,00,05
001B	MVI C,15H	OE,15
001D	PQR: MOV A,M	7E
001E	STAX D	12
001F	DCR C	OD
0020	INX H	23
0021	INX D	13
0022	JNZ : PQR	C2, 1D,00

8275 INITIALIZATION

0025	LXI H,1001H	21,01,10
0028	MVI,M OOH	36,00
002A	DCX H	2B
002B	MVI M,4FH	36,4F
002D	MVI M,99H	36,99
002F	MVI M, FCH	36,FC
0031	MVI M, 39H	36,39
0033	INX H	23
0034	MVIM, 23	36,23

PROGRAM TO DISPLAY

0036	CALL:EI	FB
0037	LXI SP, OFD6H	31,D6,OF
003A	PUSH PSW	F5
003B	PUSH H	E5
003C	PUSH D	D5
003D	LXI H, 0000H	21,00,00
0040	DAD SP	39
0041	XCHG	EB
0042	LHLD,0800H	2A,00,08
0045	SPHL	F9
0046	ABC: MVI A, COH	3E, C0
0048	SIM	30
0049	POP H	E1
	POP H	E1
	.	
	. 40 times	
	.	
	POP H	

0071	RRC	OF
0072	SIM	30
0073	LXI,H,0000H	21,00,00
0074	DAD SP	39
0075	MOV A,D	7A
0076	CMP H	BC
0077	JNZ:ABC	C2,46,00
0078	MOV A,E	7B
0079	CMP L	BD
007A	JNZ:ABC	C2,46,00
007B	JMP:CALL	C3,36,00
007C	HALT	76
04FE	BLANK	20
04FF	BLANK	20
0500	W	57
0501	E	45
0502	L	4C
0503	C	43
0504	O	4F
0505	M	4D
0506	E	45
0507	BLANK	20
0508	T	54
0509	O	4F
050A	BLANK	20
050B	E	45
050C	BLANK	20
050D	C	43
050E	BLANK	20
050F	E	45
0510	BLANK	20
0511	D	44

0512	E	45
0513	P	50
0514	T	54
0515	BLANK	20
0516	BLANK	20
0517	BLANK	20

CONCLUSION

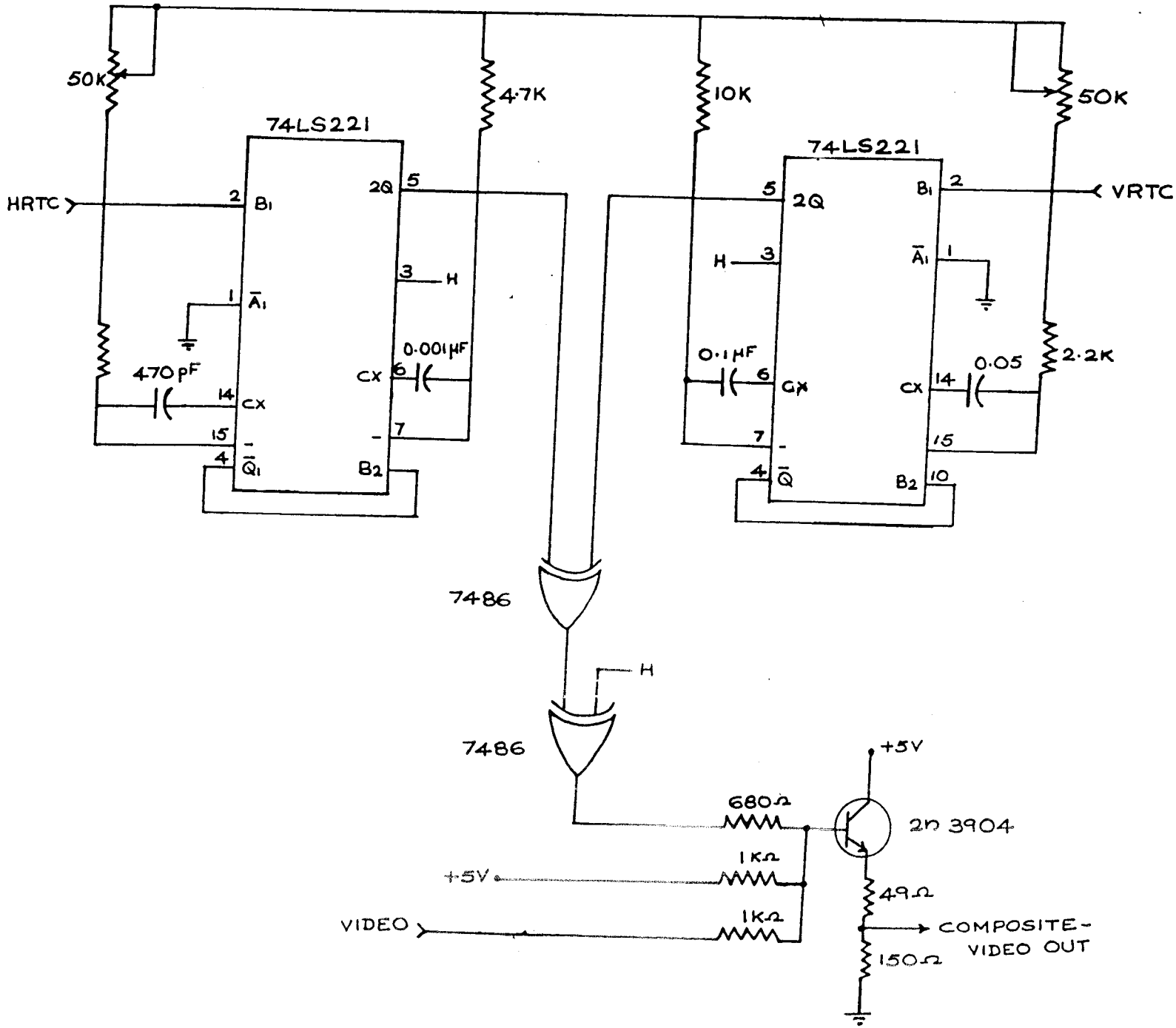
CHAPTER - VI

CONCLUSION

6.1 Composite Video

In this it was assumed that the monitor required a separate horizontal drive, vertical drive and video input. However many monitors require a Composite Video signal. The schematic shown in Fig.5.1 illustrates how to generate a Composite Video signal from the output of the 8275.

The dual shots are used to provide a small delay and proper horizontl and vertical pulse to the composite video monitor. The delay introduced in the vertical and horizontal timing is used to "center" the display. VR1 and VR2 control the amount of delay. 1C3 is used to mix the vertical and horizontal retrace and Q1 along with R1, R2 and R3 mix the video and the retrace signal and provide the DC levels.


50K
4.7K
10K
50K
74LS221
74LS221
HRTC
VRTC
2
B1
2Q
5
3
H
1
Ā1
0.001μF
470 pF
CX
6
14
15
7
4
Q̄1
B2
0.1μF
0.05
2.2K
H
Q̄
10
7486
7486
H
+5V
680Ω
2n 3904
1KΩ
+5V
49Ω
VIDEO
1KΩ
COMPOSITE-
VIDEO OUT
150Ω

6.2 Keyboard Interface

This design can be made more veasatile and dynamic by making use of a keyboard. The keyboard can be interfaced by using two parts of 8255 parallel 1/0 device.

When the system is initialized the contents of the keyboard RAM locations are set to zero. Once every frame which is 16.67 milliseconds the contents of the keyboard RAM is read and then rewritten with the contents of the current switch matrix. If a non zero value of one of the keyboard RAM locations is found to be the same as the corresponding current switch matrix, a valid key push is registered and action is taken. By operating the keyboard in this manner an automatic debounce time of 16.67 milliseconds is provided.

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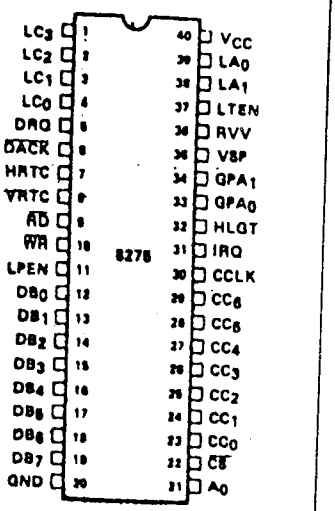
APPENDIX

8275
PROGRAMMABLE CRT CONTROLLER

- Programmable Screen and Character Format
- 8 Independent Visual Field Attributes
- 11 Visual Character Attributes (Graphic Capability)
- Cursor Control (4 Types)
- Light Pen Detection and Registers
- Fully MCS-80™ and MCS-85™ Compatible
- Dual Row Buffers
- Programmable DMA Burst Mode
- Single +5V Supply
- 40-Pin Package

PIN CONFIGURATION



BLOCK DIAGRAM

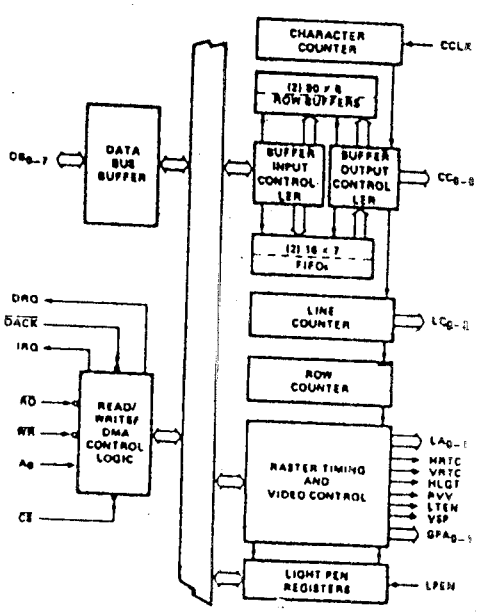


Table 1. Pin Descriptions

Symbol	Pin No.	Type	Name and Function
LC_3 LC_2 LC_1 LC_0	1 2 3 4	O	**LINE COUNT:** Output from the line counter which is used to address the character generator for the line positions on the screen.
DRQ	5	O	**DMA REQUEST:** Output signal to the 8257 DMA controller requesting a DMA cycle.
$\overline{DACK}$	6	I	**DMA ACKNOWLEDGE:** Input signal from the 8257H DMA controller acknowledging that the requested DMA cycle has been granted.
HRTC	7	O	**HORIZONTAL RETRACE:** Output signal which is active during the programmed horizontal retrace interval. During this period the VSP output is high and the LTEN output is low.
VRTC	8	O	**VERTICAL RETRACE:** Output signal which is active during the programmed vertical retrace interval. During this period the VSP output is high and the LTEN output is low.
$\overline{RD}$	9	I	**READ INPUT:** A control signal to read registers.
$\overline{WR}$	10	I	**WRITE INPUT:** A control signal to write commands into the control registers or write data into the row buffers during a DMA cycle.
LPEN	11	I	**LIGHT PEN:** Input signal from the CRT system signifying that a light pen signal has been detected.
DB_0 DB_1 DB_2 DB_3 DB_4 DB_5 DB_6 DB_7	12 13 14 15 16 17 18 19	I/O	**BI-DIRECTIONAL THREE-STATE DATA BUS LINES:** The outputs are enabled during a read of the C or P ports.
Ground	20		**GROUND.**
V_{CC}	40		**+5V POWER SUPPLY.**
LA_0 LA_1	39 38	O	**LINE ATTRIBUTE CODES:** These attribute codes have to be decoded externally by the dot timing logic to generate the horizontal and vertical line combinations for the graphic displays specified by the character attribute codes

Table 1. Pin Descriptions (Continued)

Symbol	Pin No.	Type	Name and Function
LTEN	37	O	**LIGHT ENABLE:** Output signal used to enable the video signal to the CRT. This output is active at the programmed underline cursor position, and at positions specified by attribute codes.
RVV	36	O	**REVERSE VIDEO:** Output signal used to indicate the CRT circuitry to reverse the video signal. This output is active at the cursor position if a reverse video block cursor is programmed or at the positions specified by the field attribute codes.
VSP	35	O	**VIDEO SUPPRESSION:** Output signal used to blank the video signal to the CRT. This output is active: • during the horizontal and vertical retrace intervals. • at the top and bottom lines of rows if underline is programmed to be number 8 or greater. • when an end of row or end of screen code is detected. • when a DMA underrun occurs. • at regular intervals ($1/16$ frame frequency for cursor, $1/32$ frame frequency for character and field attributes)—to create blinking displays as specified by cursor, character attribute, or field attribute programming.
GPA_1 GPA_0	34 33	O	**GENERAL PURPOSE ATTRIBUTE CODES:** Outputs which are enabled by the general purpose field attribute codes.
HLGT	32	O	**HIGHLIGHT:** Output signal used to intensify the display at particular positions on the screen as specified by the character attribute codes or field attribute codes.
IRQ	31	O	**INTERRUPT REQUEST.**
CCLK	30	I	**CHARACTER CLOCK (from Dot/Timing Logic).**
CC_6 CC_5 CC_4 CC_3 CC_2 CC_1 CC_0	29 28 27 26 25 24 23	O	**CHARACTER CODES:** Output from the row buffers used for character selection in the character generator.
CS	22	I	**CHIP SELECT:** The read and write are enabled by CS.
A_0	21	I	**PORT ADDRESS:** A high input on A_0 selects the "C" port or command registers and a low input selects the "P" port or parameter registers.

Field and Character Attribute Interaction

Character Attribute Symbols are affected by the Reverse Video (RVV) and General Purpose (GPA_{0-1}) field attributes. They are not affected by Underline, Blink or Highlight field attributes; however, these characteristics can be programmed *individually* for Character Attribute Symbols.

Cursor Timing

The cursor location is determined by a cursor row register and a character position register which are loaded by command to the controller. The cursor can be programmed to appear on the display as:

1) a blinking underline
2) a blinking reverse video block
3) a non-blinking underline
4) a non-blinking reverse video block

The cursor blinking frequency is equal to the screen refresh frequency divided by 16.

If a non-blinking reverse video *cursor* appears in a non-blinking reverse video *field*, the cursor will appear as a normal video block.

If a non-blinking underline *cursor* appears in a non-blinking underline *field*, the cursor will not be visible.

Light Pen Detection

A light pen consists of a micro switch and a tiny light sensor. When the light pen is pressed against the CRT screen, the micro switch enables the light sensor. When the raster sweep reaches the light sensor, it triggers the light pen output.

If the output of the light pen is presented to the 8275H LPEN input, the row and character position coordinates are stored in a pair of registers. These registers can be read on command. A bit in the status word is set, indicating that the light pen signal was detected. The LPEN input must be a 0 to 1 transition for proper operation.

NOTE:
Due to internal and external delays, the character position coordinate will be off by at least three character positions. This has to be corrected in software.

Device Programming

The 8275H has two programming registers, the Command Register (CREG) and the parameter register (PREG). It also has a Status Register (SREG). The Command Register can only be written into and the Status Registers can only be read from. They are addressed as follows:

A_0	Operation	Register
0	Read	PREG
0	Write	PREG
1	Read	SREG
1	Write	CREG

The 8275H expects to receive a command and a sequence of 0 to 4 parameters, depending on the command. If the proper number of parameter bytes are not received before another command is given, a status flag is set, indicating an improper command.

INSTRUCTION SET

The 8275H instruction set consists of 8 commands.

Command	No. of Parameter Bytes
Reset	4
Start Display	0
Stop Display	0
Read Light Pen	2
Load Cursor	2
Enable Interrupt	0
Disable Interrupt	0
Preset Counters	0

In addition, the status of the 8275H (SREG) can be read by the CPU at any time.

1.0 Reset Command

	Operation	A_0	Description	Data Bus MSB							LSB
Command	Write	1	Reset Command	0	0	0	0	0	0	0	0
Parameters	Write	0	Screen Comp Byte 1	S	H	H	H	H	H	H	H
	Write	0	Screen Comp Byte 2	V	V	R	R	R	R	R	R
	Write	0	Screen Comp Byte 3	U	U	U	U	L	L	L	L
	Write	0	Screen Comp Byte 4	M	F	C	C	Z	Z	Z	Z

Action—After the reset command is written, DMA requests stop, 8275H interrupts are disabled, and the VSP output is used to blank the screen. HRTC and VRTC continue to run. HRTC and VRTC timing are random on power-up.

As parameters are written, the screen composition is defined.

Parameter—S Spaced Rows

S	Functions
0	Normal Rows
1	Spaced Rows

Parameter—HHHHHHH
Horizontal Characters/Row

H	H	H	H	H	H	H	No. of Characters Per Row
0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	2
0	0	0	0	0	1	0	3
			.				.
			.				.
			.				.
1	0	0	1	1	1	1	80
1	0	1	0	0	0	0	Undefined
			.				.
			.				.
			.				.
1	1	1	1	1	1	1	Undefined

Parameter—VV Vertical Retrace Row Count

V	V	No. of Row Counts Per VRTC
0	0	1
0	1	2
1	0	3
1	1	4

Parameter—RRRRRR Vertical Rows/Frame

R	R	R	R	R	R	No. of Rows/Frame
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
			.			.
			.			.
			.			.
1	1	1	1	1	1	64

Parameter—UUUU Underline Placement

U	U	U	U	Line Number of Underline
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
		.		.
		.		.
		.		.
1	1	1	1	16

Parameter—LLLL
Number of Lines per Character Row

L	L	L	L	No. of Lines/Row
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
		.		.
		.		.
		.		.
1	1	1	1	16

Parameter—M Line Counter Mode

M	Line Counter Mode
0	Mode 0 (Non-Offset)
1	Mode 1 (Offset by 1 Count)

Parameter—F Field Attribute Mode

F	Field Attribute Mode
0	Transparent
1	Non-Transparent

Parameter—CC Cursor Format

C	C	Cursor Format
0	0	Blinking reverse video block
0	1	Blinking underline
1	0	Nonblinking reverse video block
1	1	Nonblinking underline

Parameter—ZZZZ Horizontal Retrace Count

Z	Z	Z	Z	No. of Character Counts Per HRTC
0	0	0	0	2
0	0	0	1	4
0	0	1	0	6
				.
				.
				.
1	1	1	1	32

NOTE:
uuuu MSB determines blanking of top and bottom lines (1 = blanked, 0 = not blanked).

SSS Burst Space Code

S	S	S	No. of Character Clocks Between DMA Requests
0	0	0	0
0	0	1	7
0	1	0	15
0	1	1	23
1	0	0	31
1	0	1	39
1	1	0	47
1	1	1	55

BB Burst Count Code

B	B	No. of DMA Cycles Per Burst
0	0	1
0	1	2
1	0	4
1	1	8

Action—8275H interrupts are enabled, DMA requests begin, video is enabled, Interrupt Enable and Video Enable status flags are set.

2.0 Start Display Command

	Operation	A_0	Description	Data Bus MSB							LSB
Command	Write	1	Start Display	0	0	1	S	S	S	B	B
No Parameters											

3.0 Stop Display Command

	Operation	A_0	Description	Data Bus MSB							LSB
Command	Write	1	Stop Display	0	1	0	0	0	0	0	0
No Parameters											

Action—Disables video, interrupts remain enabled, HRTC and VRTC continue to run, Video Enable status flag is reset, and the "Start Display" command must be given to re-enable the display.

4.0 Read Light Pen Command

	Operation	A_0	Description	Data Bus MSB							LSB
Command	Write	1	Read Light Pen	0	1	1	0	0	0	0	0
Parameters	Read	0	Char. Number	(Char. Position in Row)							
	Read	0	Row Number	(Row Number)							

Action—The 8275H is conditioned to supply the contents of the light pen position registers in the next two read cycles of the parameter register. Status flags are not affected.

NOTE:
Software correction of light pen position is required.

5.0 Load Cursor Position

	Operation	A_0	Description	Data Bus MSB							LSB
Command	Write	1	Load Cursor	1	0	0	0	0	0	0	0
Parameters	Write	0	Char. Number	(Char. Position in Row)							
	Write	0	Row Number	(Row Number)							

Action—The 8275H is conditioned to place the next two parameter bytes into the cursor position registers. Status flags not affected.

6.0 Enable Interrupt Command

	Operation	A_0	Description	Data Bus MSB							LSB
Command	Write	1	Enable Interrupt	1	0	1	0	0	0	0	0
No Parameters											

Action—The interrupt enable status flag is set and interrupts are enabled.

7.0 Disable Interrupt Command

	Operation	A_0	Description	Data Bus MSB							LSB
Command	Write	1	Disable Interrupt	1	1	0	0	0	0	0	0
No Parameters											

Action—Interrupts are disabled and the interrupt enable status flag is reset.

8.0 Preset Counters Command

	Operation	A_0	Description	Data Bus MSB							LSB
Command	Write	1	Preset Counters	1	1	1	0	0	0	0	0
No Parameters											

Action—The internal timing counters are preset, corresponding to a screen display position at the top left corner. Two character clocks are required for this operation. The counters will remain in this state until any other command is given.

- This command is useful for system debug and synchronization of clustered CRT displays on a single CPU. After this command, two additional clock cycles are required before the first character of the first row is put out.

STATUS FLAGS

	Operation	A_0	Description	Data Bus MSB							LSB
Command	Read	1	Status Word	0	IE	IR	LP	IC	VE	DU	FO

IE — (Interrupt Enable) Set or reset by command. It enables vertical retrace interrupt. It is automatically set by a "Start Display" command and reset with the "Reset" command.

IR — (Interrupt Request) This flag is set at the beginning of display of the last row of the frame if the interrupt enable flag is set. It is reset after a status read operation.

LP — This flag is set when the light pen input (LPEN) is activated and the light pen registers have been loaded. This flag is automatically reset after a status read.

IC — (Improper Command) This flag is set when a command parameter string is too long or too short. The flag is automatically reset after a status read.

VE — (Video Enable) This flag indicates that video operation of the CRT is enabled. This flag is set on a "Start Display" command, and reset on a "Stop Display" or "Reset" command.

DU — (DMA Underrun) This flag is set whenever a data underrun occurs during DMA transfers. Upon detection of DU, the DMA operation is stopped and the screen is blanked until after the vertical retrace interval. This flag is reset after a status read.

FO — (FIFO Overrun) This flag is set whenever the FIFO is overrun. It is reset on a status read.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C

Storage Temperature ..... −65°C to + 150°C

Voltage On Any Pin With Respect to Ground ..... −0.5V to + 7V

Power Dissipation ..... 1 Watt

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±5%

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5V	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to 0.45V
I_{CC}	V_{CC} Supply Current		160	mA	

CAPACITANCE T_A = 25°C, V_{CC} = GND = 0V

Symbol	Parameter	Min	Max	Units	Test Conditions
C_{IN}	Input Capacitance		10	pF	f_c = 1 MHz Unmeasured pins returned to V_{SS}
$C_{I/O}$	I/O Capacitance		20	pF	

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%, GND = 0V

Bus Parameters

READ CYCLE

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{AR}	Address Stable before READ	0		ns	
t_{RA}	Address Hold Time for READ	0		ns	
t_{RR}	READ Pulse Width	250		ns	
t_{RD}	Data Delay from READ		200	ns	C_L = 150 pF
t_{DF}	READ to Data Floating		100	ns	C_L = 150 pF

WRITE CYCLE

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{AW}	Address Stable before WRITE	0		ns	
t_{WA}	Address Hold Time for WRITE	0		ns	
t_{WW}	WRITE Pulse Width	250		ns	
t_{DW}	Data Setup Time for WRITE	150		ns	
t_{WD}	Data Hold Time for WRITE	0		ns	

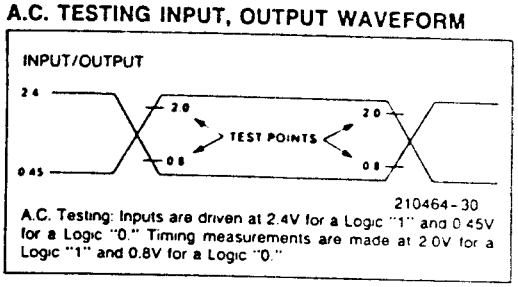
CLOCK TIMING

Symbol	Parameter	8275		8275-2		Units	Test Conditions
		Min	Max	Min	Max		
t_{CLK}	Clock Period	480		320		ns	
t_{KH}	Clock High	240		120		ns	
t_{KL}	Clock Low	160		120		ns	
t_{KR}	Clock Rise	5	30	5	30	ns	
t_{KF}	Clock Fall	5	30	5	30	ns	

OTHER TIMING

Symbol	Parameter	8275		8275-2		Units	Test Conditions
		Min	Max	Min	Max		
t_{CC}	Character Code Output Delay		150		150	ns	C_L = 50 pF
t_{HR}	Horizontal Retrace Output Delay		200		150	ns	C_L = 50 pF
t_{LC}	Line Count Output Delay		400		250	ns	C_L = 50 pF
t_{AT}	Control/Attribute Output Delay		275		250	ns	C_L = 50 pF
t_{VR}	Vertical Retrace Output Delay		275		250	ns	C_L = 50 pF
t_{RI}	IRQ ↓ from RD ↑		250		250	ns	C_L = 50 pF
t_{WQ}	DRQ ↑ from WR ↑		250		250	ns	C_L = 50 pF
t_{RQ}	DRQ ↓ from WR ↓		200		200	ns	C_L = 50 pF
t_{LR}	DACK ↓ to WR ↓	0		0		ns	
t_{RL}	WR ↑ to DACK ↑	0		0		ns	
t_{PR}	LPEN Rise		50		50	ns	
t_{PH}	LPEN Hold	100		100		ns	
t_{DI}	DACK Inactive Period	120				ns	

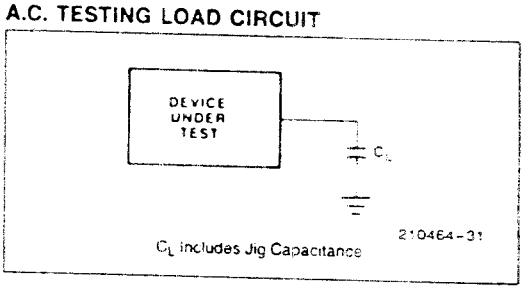
A.C. TESTING INPUT, OUTPUT WAVEFORM



210464-30

A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0." Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

A.C. TESTING LOAD CIRCUIT

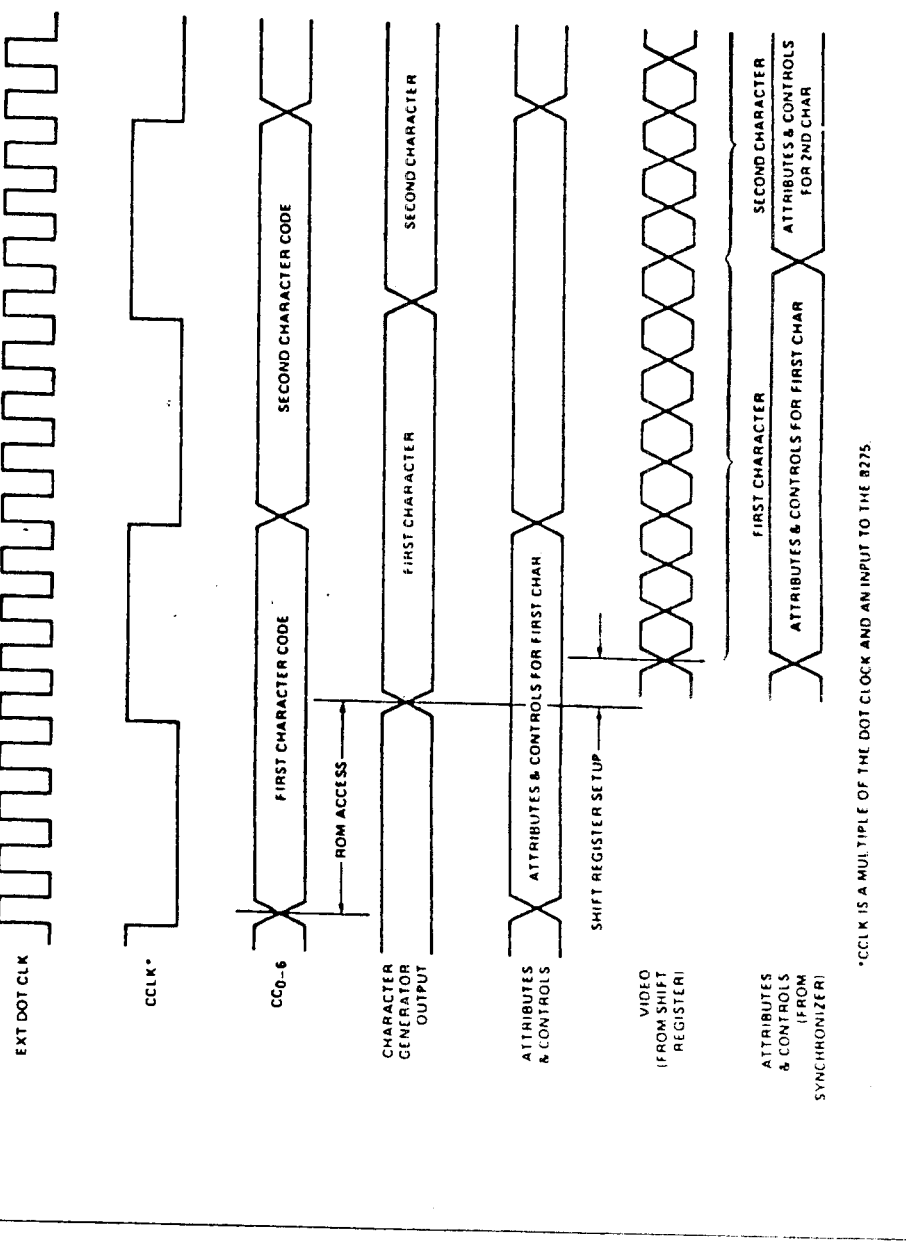


C_L includes Jig Capacitance

210464-31

WAVEFORMS

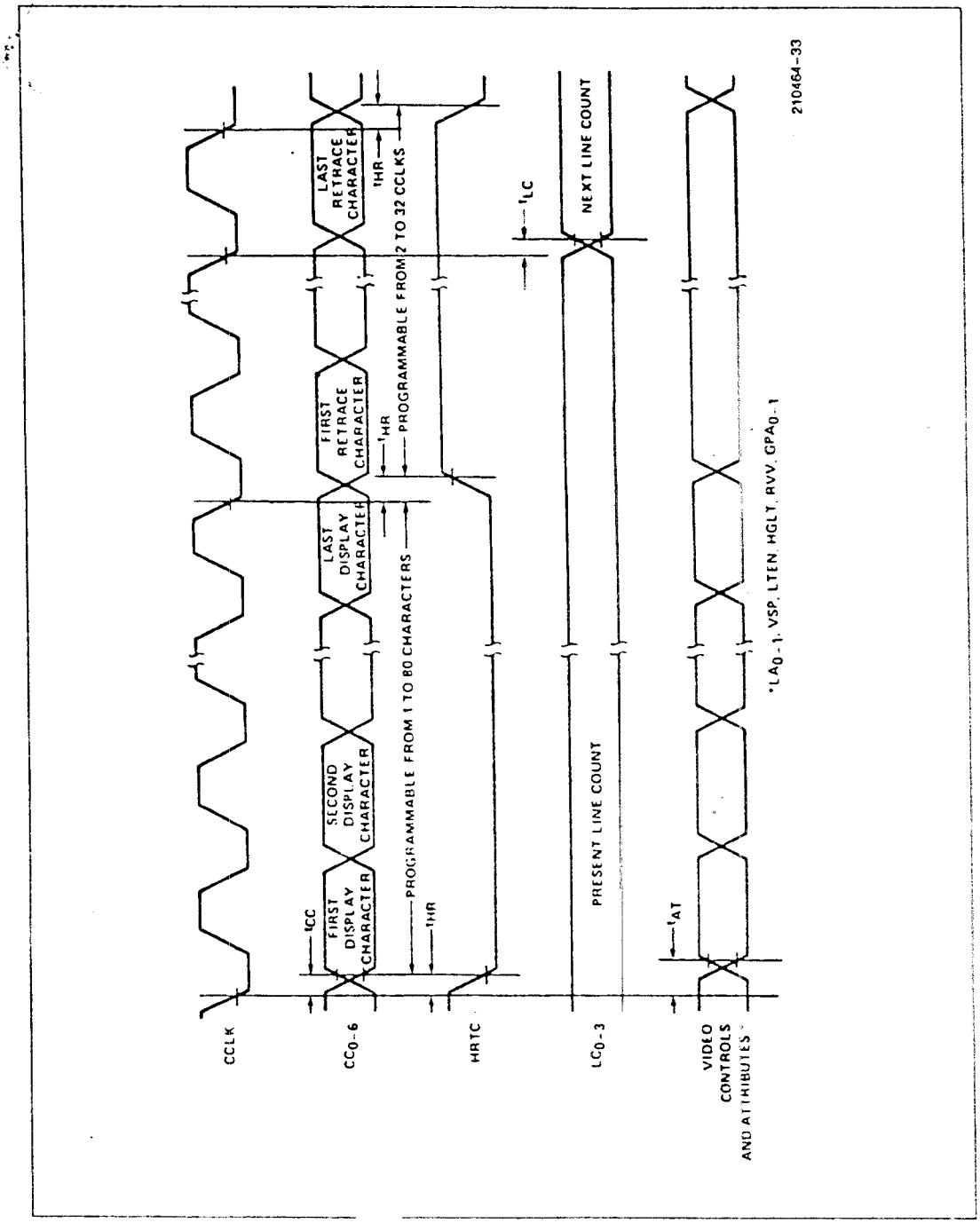
TYPICAL DOT LEVEL TIMING



*CCLK IS A MULTIPLE OF THE DOT CLOCK AND AN INPUT TO THE 8275.

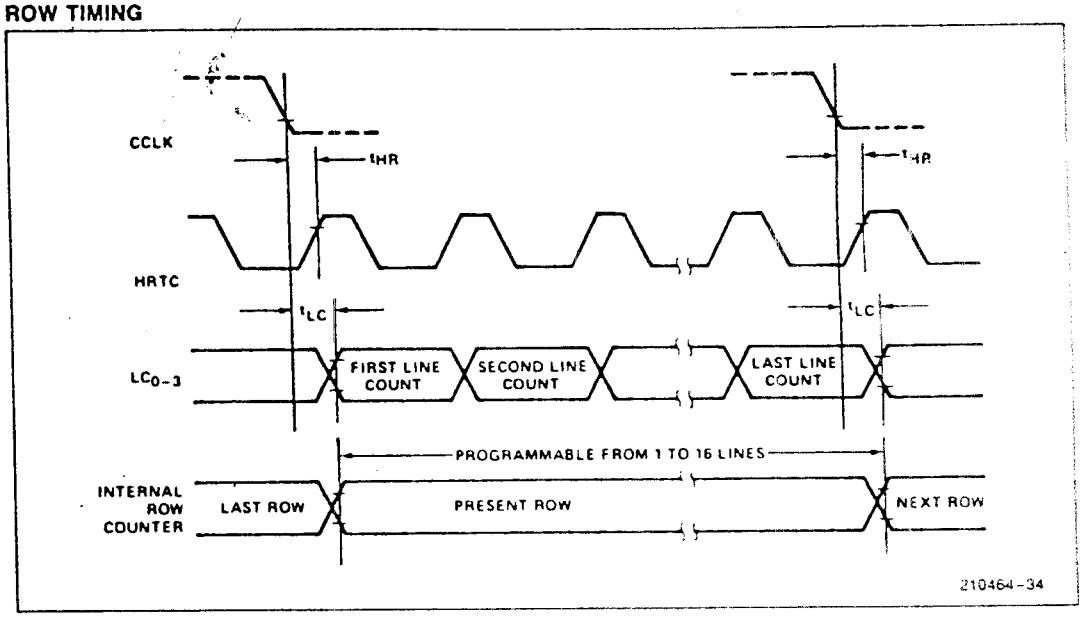
WAVEFORMS (Continued)

LINE TIMING

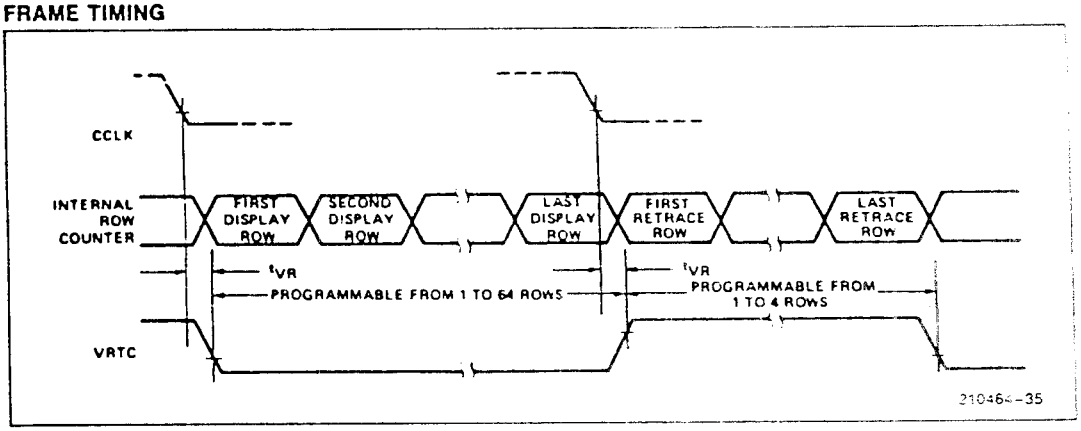


WAVEFORMS (Continued)

ROW TIMING

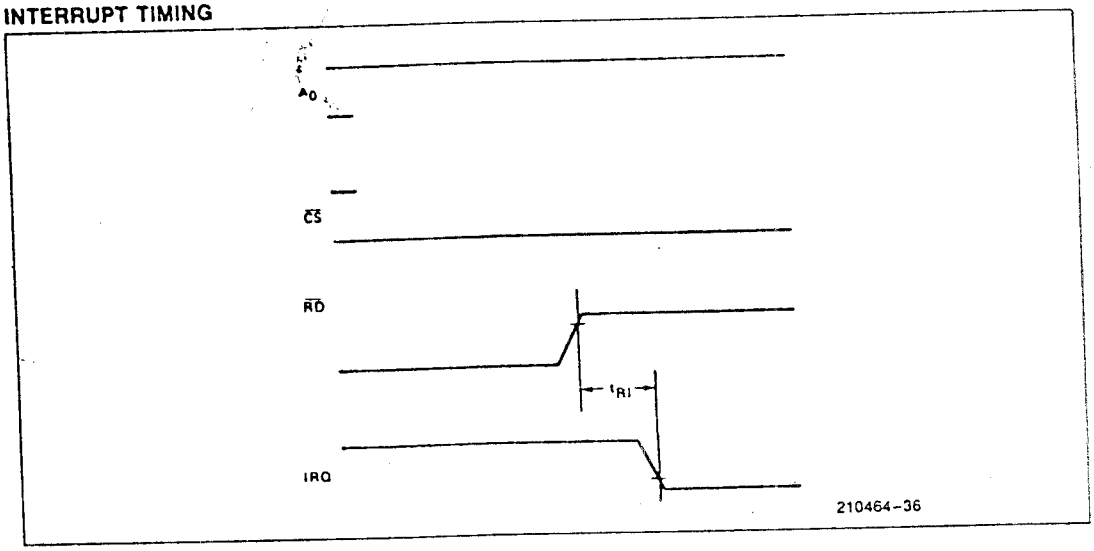


FRAME TIMING

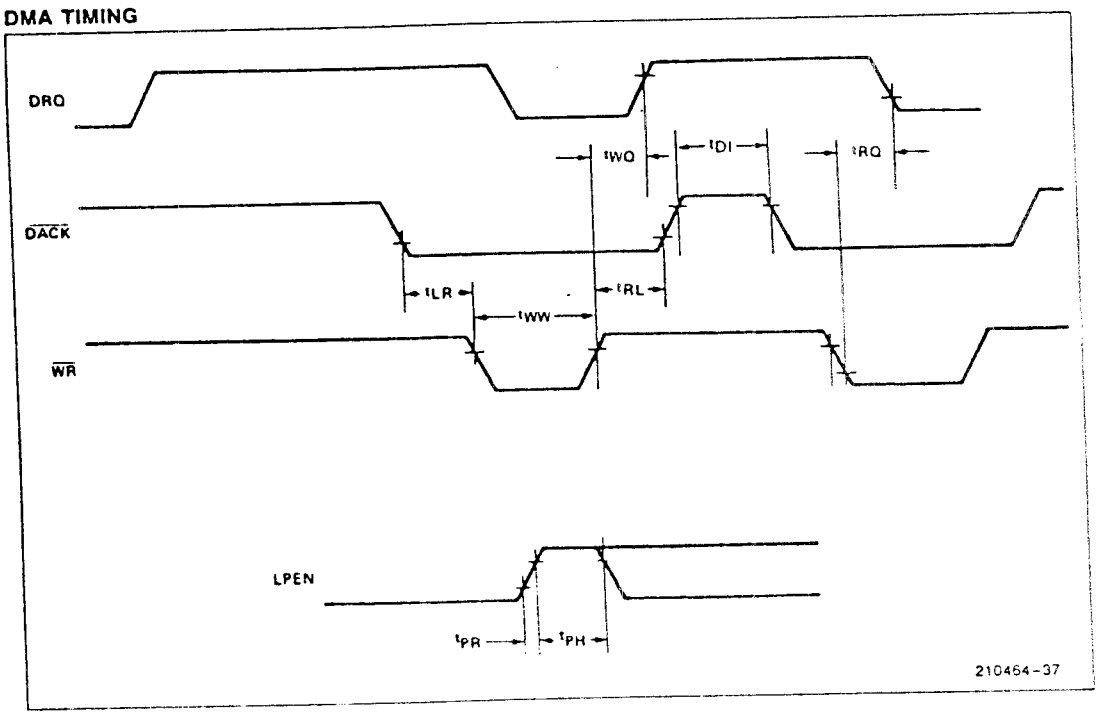


WAVEFORMS (Continued)

INTERRUPT TIMING

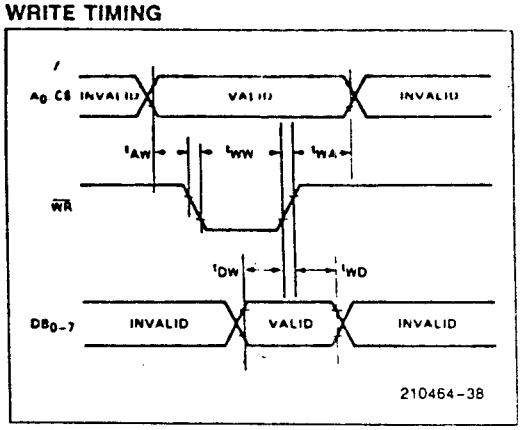


DMA TIMING

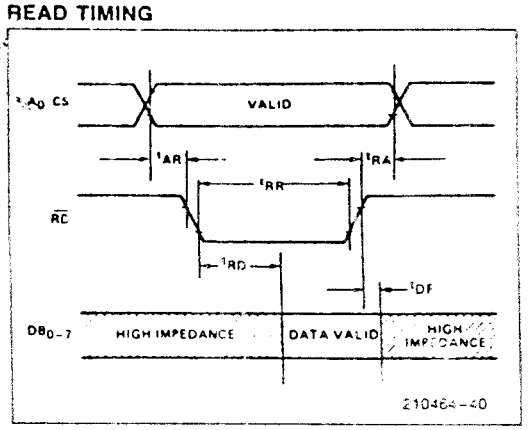


WAVEFORMS (Continued)

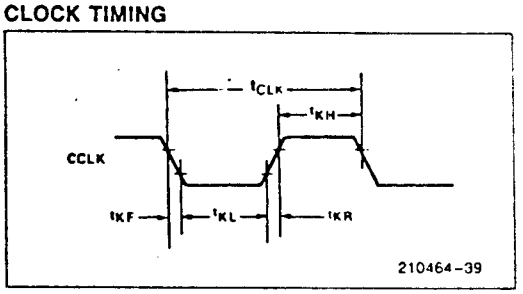
WRITE TIMING



READ TIMING



CLOCK TIMING



ROW 1	0800H	0801H 084FH
ROW 2	0850H	0851H 089FH
ROW 3	08A0H	08A1H 08EFH
ROW 4	08F0H	08F1H 093FH
ROW 5	0940H	0941H 098FH
ROW 6	0990H	0991H 090FH
ROW 7	09E0H	09E1H 0A2FH
ROW 8	0A30H	0A31H 0A7FH
ROW 9	0A80H	0A81H 0ACFH
ROW 10	0AD0H	0AD1H 0B1FH
ROW 11	0B20H	0B21H 0B6FH
ROW 12	0B70H	0B71H 0BBFH
ROW 13	0BC0H	0BC1H 0C0FH
ROW 14	0C10H	0C11H 0C5FH
ROW 15	0C60H	0C61H 0CAFH
ROW 16	0CB0H	0CB1H 0CFFH
ROW 17	0D00H	0D01H 0D4FH
ROW 18	0D50H	0D51H 0D9FH
ROW 19	0DA0H	0DA1H 0DEFH
ROW 20	0DF0H	0DF1H 0E3FH
ROW 21	0E40H	0E41H 0E8FH
ROW 22	0E90H	0E91H 0EDFH
ROW 23	0EE0H	0EE1H 0F2FH
ROW 24	0F30H	0F31H 0F7FH
ROW 25	0F80H	0F81H 0FCFH

After Initialization

ROW 2	0850H	0851H 089FH
ROW 3	08A0H	08A1H 08EFH
ROW 4	08F0H	08F1H 093FH
ROW 5	0940H	0941H 098FH
ROW 6	0990H	0991H 090FH
ROW 7	09E0H	09E1H 0A2FH
ROW 8	0A30H	0A31H 0A7FH
ROW 9	0A80H	0A81H 0ACFH
ROW 10	0AD0H	0AD1H 0B1FH
ROW 11	0B20H	0B21H 0B6FH
ROW 12	0B70H	0B71H 0BBFH
ROW 13	0BC0H	0BC1H 0C0FH
ROW 14	0C10H	0C11H 0C5FH
ROW 15	0C60H	0C61H 0CAFH
ROW 16	0CB0H	0CB1H 0CFFH
ROW 17	0D00H	0D01H 0D4FH
ROW 18	0D50H	0D51H 0D9FH
ROW 19	0DA0H	0DA1H 0DEFH
ROW 20	0DF0H	0DF1H 0E3FH
ROW 21	0E40H	0E41H 0E8FH
ROW 22	0E90H	0E91H 0EDFH
ROW 23	0EE0H	0EE1H 0F2FH
ROW 24	0F30H	0F31H 0F7FH
ROW 25	0F80H	0F81H 0FCFH
ROW 1	0800H	0801H 084FH

After 1 Scroll

ROW 3	08A0H	08A1H 08EFH
ROW 4	08F0H	08F1H 093FH
ROW 5	0940H	0941H 098FH
ROW 6	0990H	0991H 090FH
ROW 7	09E0H	09E1H 0A2FH
ROW 8	0A30H	0A31H 0A7FH
ROW 9	0A80H	0A81H 0ACFH
ROW 10	0AD0H	0AD1H 0B1FH
ROW 11	0B20H	0B21H 0B6FH
ROW 12	0B70H	0B71H 0BBFH
ROW 13	0BC0H	0BC1H 0C0FH
ROW 14	0C10H	0C11H 0C5FH
ROW 15	0C60H	0C61H 0CAFH
ROW 16	0CB0H	0CB1H 0CFFH
ROW 17	0D00H	0D01H 0D4FH
ROW 18	0D50H	0D51H 0D9FH
ROW 19	0DA0H	0DA1H 0DEFH
ROW 20	0DF0H	0DF1H 0E3FH
ROW 21	0E40H	0E41H 0E8FH
ROW 22	0E90H	0E91H 0EDFH
ROW 23	0EE0H	0EE1H 0F2FH
ROW 24	0F30H	0F31H 0F7FH
ROW 25	0F80H	0F81H 0FCFH
ROW 1	0800H	0801H 084FH
ROW 2	0850H	0851H 089FH

After 2 Scrolls

ROW 4	08F0H	08F1H 093FH
ROW 5	0940H	0941H 098FH
ROW 6	0990H	0991H 090FH
ROW 7	09E0H	09E1H 0A2FH
ROW 8	0A30H	0A31H 0A7FH
ROW 9	0A80H	0A81H 0ACFH
ROW 10	0AD0H	0AD1H 0B1FH
ROW 11	0B20H	0B21H 0B6FH
ROW 12	0B70H	0B71H 0BBFH
ROW 13	0BC0H	0BC1H 0C0FH
ROW 14	0C10H	0C11H 0C5FH
ROW 15	0C60H	0C61H 0CAFH
ROW 16	0CB0H	0CB1H 0CFFH
ROW 17	0D00H	0D01H 0D4FH
ROW 18	0D50H	0D51H 0D9FH
ROW 19	0DA0H	0DA1H 0DEFH
ROW 20	0DF0H	0DF1H 0E3FH
ROW 21	0E40H	0E41H 0E8FH
ROW 22	0E90H	0E91H 0EDFH
ROW 23	0EE0H	0EE1H 0F2FH
ROW 24	0F30H	0F31H 0F7FH
ROW 25	0F80H	0F81H 0FCFH
ROW 1	0800H	0801H 084FH
ROW 2	0850H	0851H 089FH
ROW 3	08A0H	08A1H 08EFH

After 3 Scrolls

Figure 6-4. Screen Memory During Scrolling

National Semiconductor

DM54S160/DM74S160, DM54S161/DM74S161, DM54S162/DM74S162, DM54S163/ DM74S163 Synchronous 4-Bit Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The S160 and S162 are 4-bit decade counters and the S161 and S163 are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable input.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages.

Features

- Synchronously programmable
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs
- Typical propagation time, clock to Q output 9 ns
- Typical clock frequency 70 MHz
- Typical power dissipation 475 mW

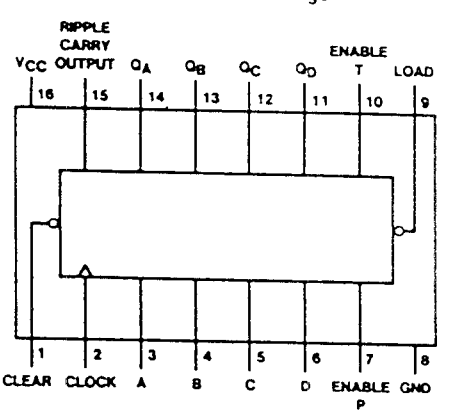
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6471-1

DM54S160 (J) DM74S160 (N)
DM54S161 (J) DM74S161 (N)
DM54S162 (J) DM74S162 (N)
DM54S163 (J) DM74S163 (N)

National Semiconductor

DM54S174/DM74S174, DM54S175/DM74S175 Hex/Quad D Flip-Flops with Clear

General Description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the quad (175) versions feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Features

- S174 contain six flip-flops with single-rail outputs.
- S175 contain four flip-flops with double-rail outputs.
- Buffered clock and direct clear inputs
- Individual data input to each flip-flop
- Applications include
  - Buffer/storage registers
  - Shift registers
  - Pattern generators
- Typical clock frequency 110 MHz
- Typical power dissipation per flip-flop 75 mW

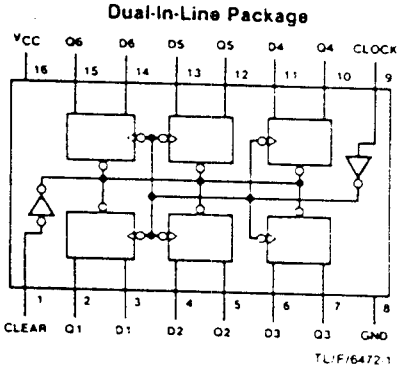
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

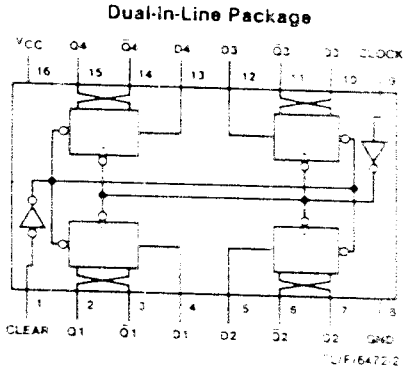
Connection Diagrams

Dual-In-Line Package



54S174 (J) 74S174 (N)

Dual-In-Line Package



54S175 (J) 74S175 (N)

Function Table (Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care
↑ = Transition from low to high level
Q_0 = The level of Q before the indicated steady-state input conditions were established.
† = S175 only

National Semiconductor

DM5410/DM7410 Triple 3-Input NAND Gates

General Description

This device contains three independent gates each of which performs the logic NAND function.

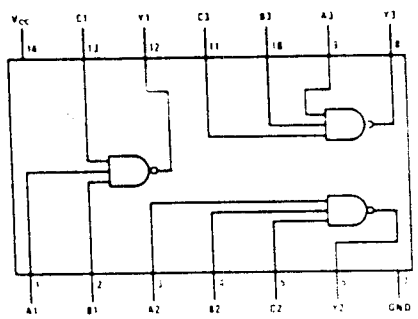
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6500-1

DM5410 (J) DM7410 (N)

Function Table

$Y = \overline{ABC}$

Inputs			Output
A	B	C	Y
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

National Semiconductor

DM5400/DM7400 Quad 2-Input NAND Gates

General Description

This device contains four independent gates each of which performs the logic NAND function.

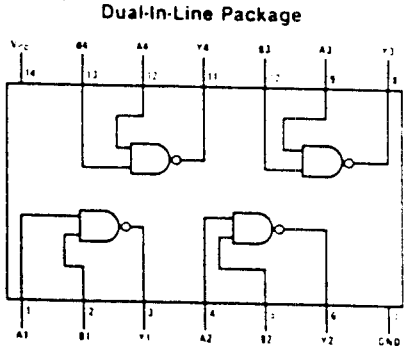
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6613-1

DM5400 (J) DM7400 (N)

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

National Semiconductor

DM5404/DM7404 Hex Inverting Gates

General Description

This device contains six independent gates each of which performs the logic INVERT function.

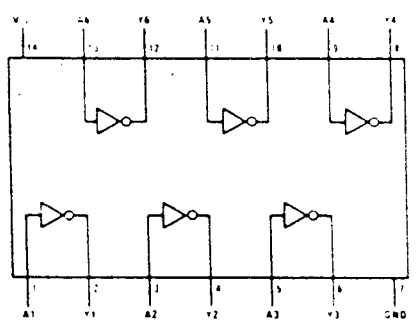
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6494-1

DM5404 (J) DM7404 (N)

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

National Semiconductor

DM54166/DM74166 8-Bit Parallel In/Serial Out Shift Registers

General Description

These parallel-in or serial-in, serial-out shift registers feature gated clock inputs and an overriding clear input. All inputs are buffered to lower the drive requirements to one normalized load, and input clamping diodes minimize switching transients to simplify system design. The load mode is established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input NOR gate, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free-running, and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

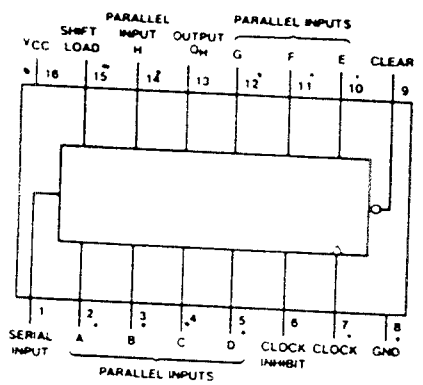
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6554-1

54166 (J) 74166 (N)

Function Table

Inputs							Internal Outputs		Output
Clear	Shift/Load	Clock Inhibit	Clock	Serial	Parallel A	Parallel H	Q_A	Q_B	Q_H
L	X	X	X	X	X		L	L	L
H	X	L	L	X	X		Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a	h	a	b	h
H	H	L	↑	H	X		H	Q_{An}	Q_{Gn}
H	H	↓	↑	L	X		L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X		Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)
X = Don't Care (any input, including transitions)
↑ = Transition from low to high level
a, ..., h = The level of steady state input at inputs A through H, respectively
Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, Q_H, respectively, before the indicated steady state input conditions were established
Q_{An}, Q_{Gn} = The level of Q_A, Q_G, respectively, before the most recent ↑ transition of the clock

National Semiconductor

DM5474/DM7474 Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs

General Description

This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is low or high without affecting the outputs as long as the data setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

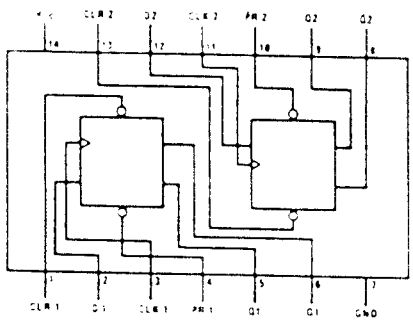
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6526-1

DM5474 (J) DM7474 (N)

Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = High Logic Level

X = Either Low or High Logic Level

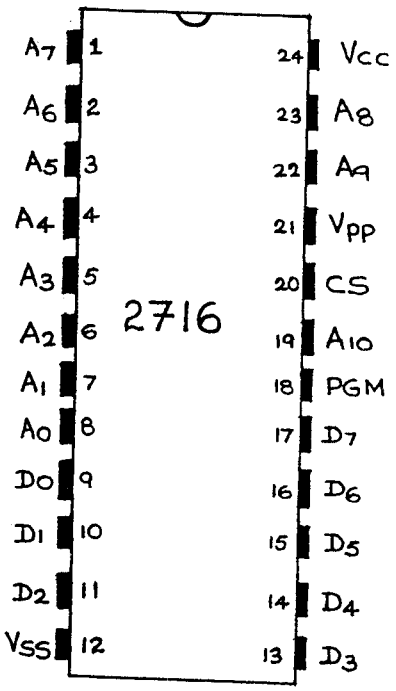
L = Low Logic Level

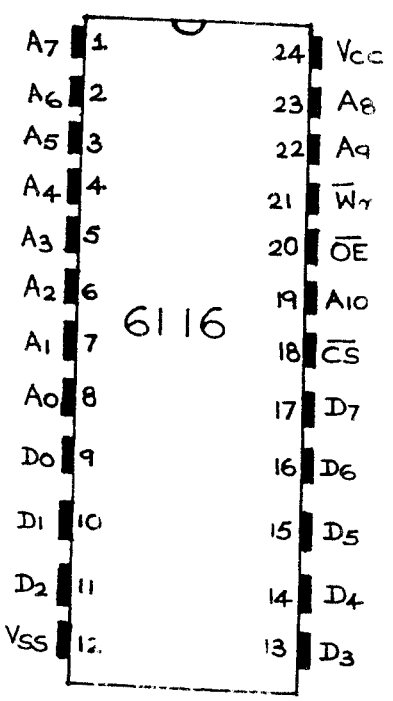
↑ = Positive-going transition of the clock

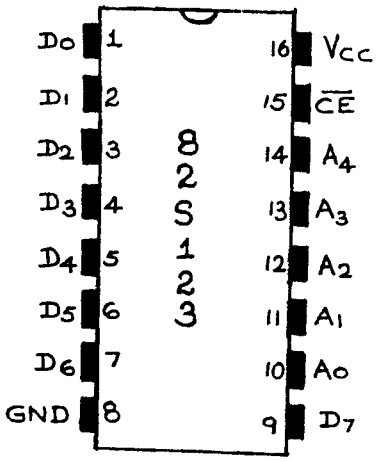
* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (high) level.

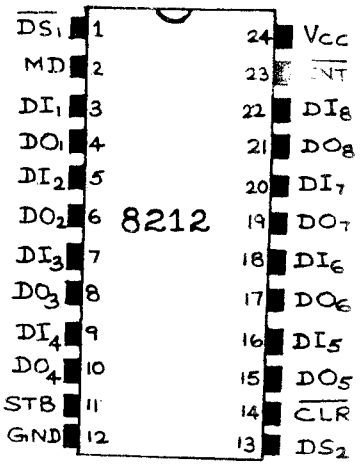
Q_0 = The output logic level of Q before the indicated input conditions were established.

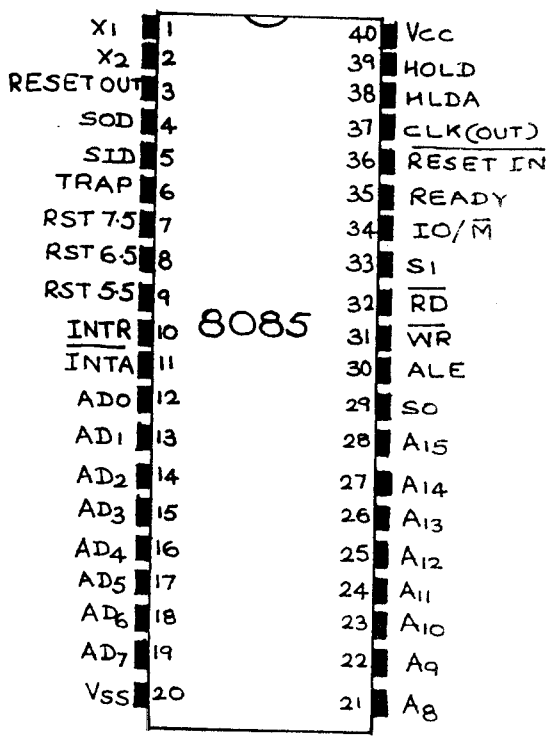
PIN CONFIGURATION

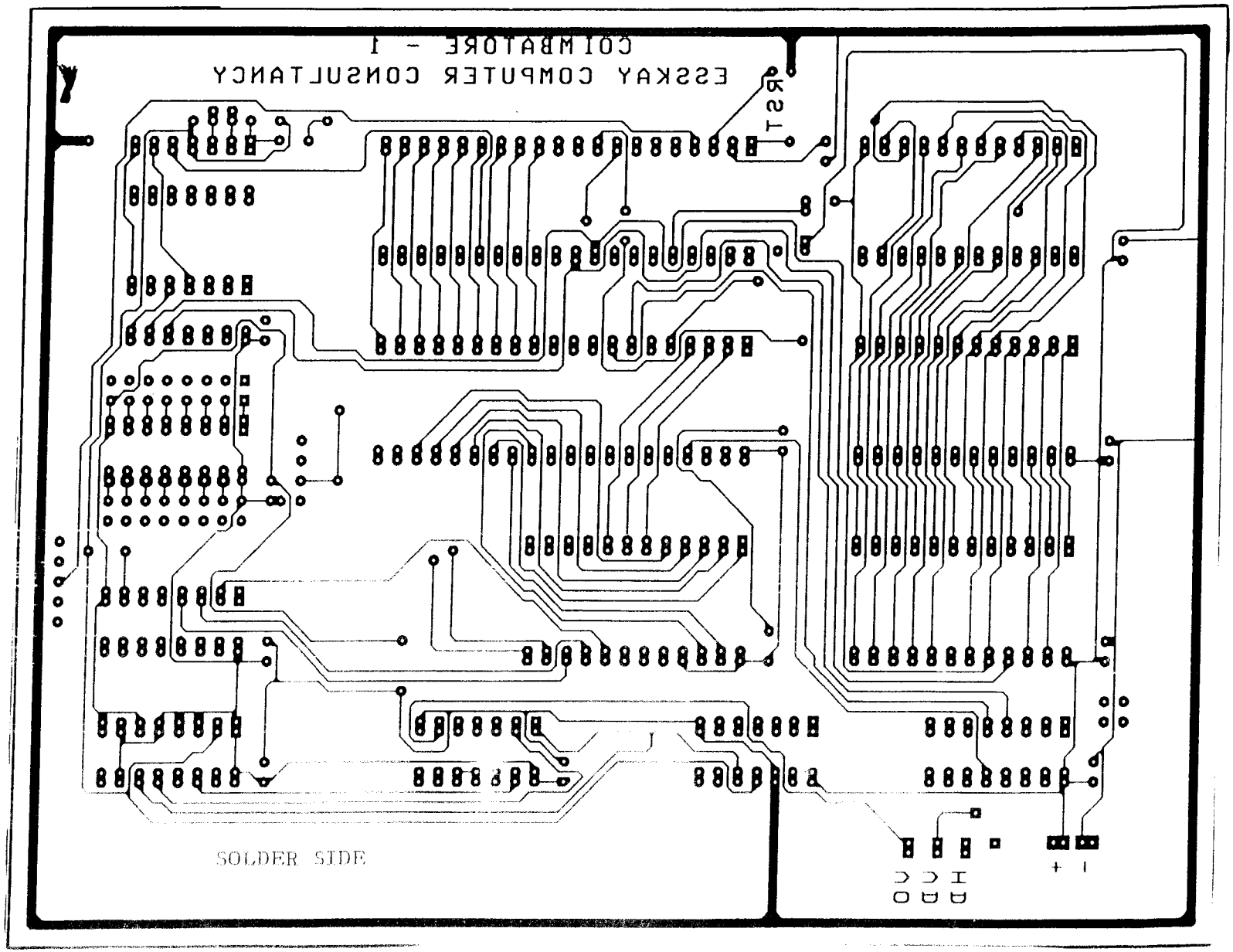


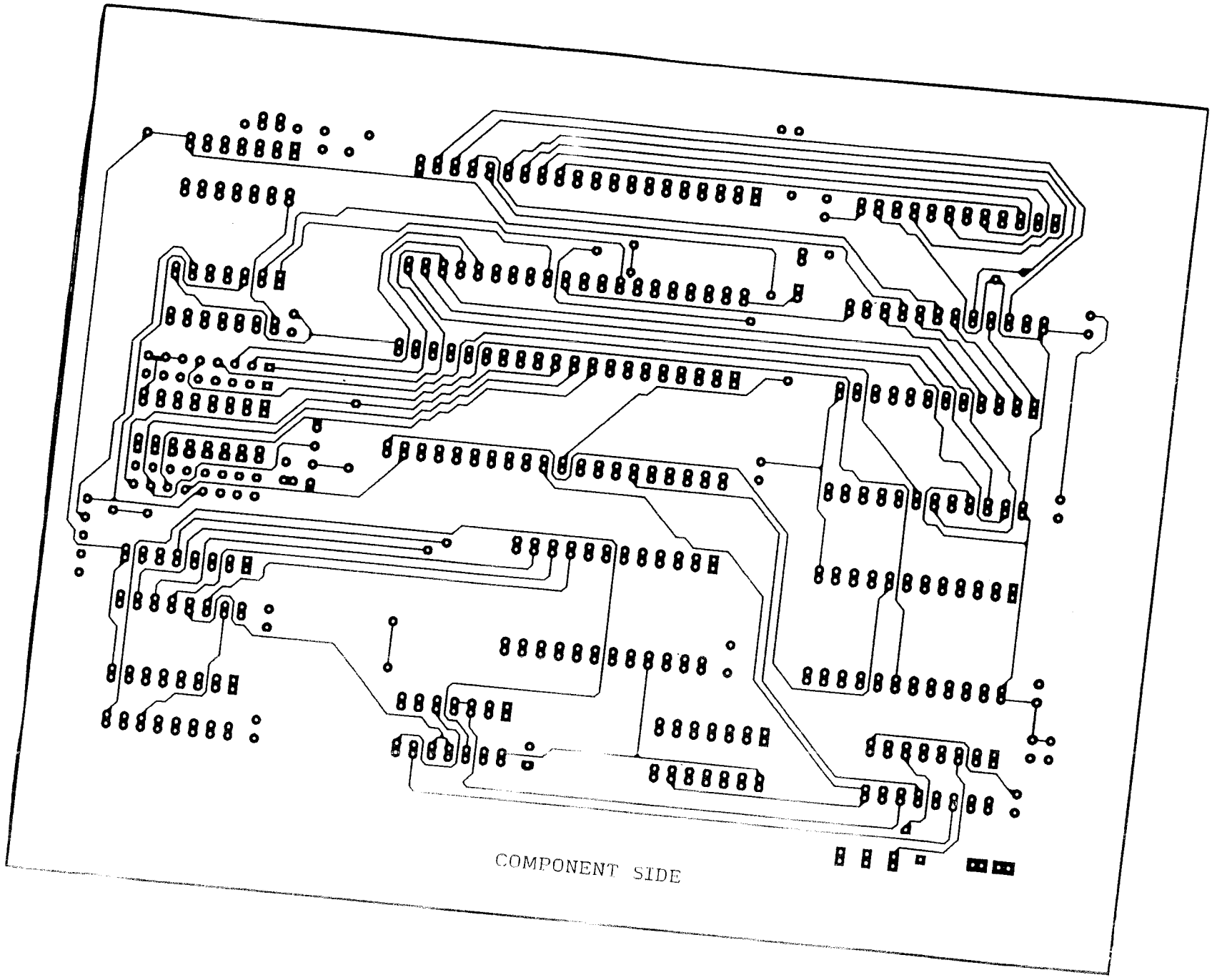



D0 1
D1 2
D2 3
D3 4
D4 5
D5 6
D6 7
GND 8
16 Vcc
15 CE
14 A4
13 A3
12 A2
11 A1
10 A0
9 D7
8
2
S
1
2
3


DS1 1
MD 2
DI1 3
DO1 4
DI2 5
DO2 6
DI3 7
DO3 8
DI4 9
DO4 10
STB 11
GND 12
24 Vcc
23 INT
22 DI8
21 DO8
20 DI7
19 DO7
18 DI6
17 DO6
16 DI5
15 DO5
14 CLR
13 DS2
8212


X1 1
X2 2
RESET OUT 3
SOD 4
SID 5
TRAP 6
RST 7.5 7
RST 6.5 8
RST 5.5 9
INTR 10
INTA 11
AD0 12
AD1 13
AD2 14
AD3 15
AD4 16
AD5 17
AD6 18
AD7 19
Vss 20
40 Vcc
39 HOLD
38 HLDA
37 CLK(OUT)
36 RESET IN
35 READY
34 IO/M
33 S1
32 RD
31 WR
30 ALE
29 S0
28 A15
27 A14
26 A13
25 A12
24 A11
23 A10
22 A9
21 A8
8085


COIMBATORE - 1
ESSKAY COMPUTER CONSULTANCY
RST
SOLDER SIDE
GND
VCC
+
-


COMPONENT SIDE