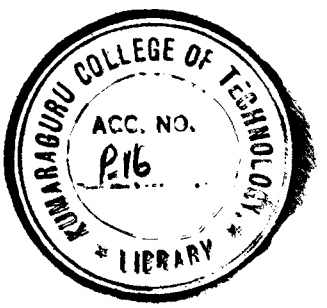
MICROPROCESSOR BASED LOAD SHEDDING AND RESTORATION



Project Work

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AUTHORS

SYNOPSIS

A disturbance on a power system can produce a severe generation load imbalance resulting in a rapid frequency fall. The possibility of such disturbance has led to increased interest in the application of load shedding schemes for regaining generation-load balance. This report explains a microprocessor based shedding and restoration scheme, by taking a typical example of a power system with three feeders. The microprocessor compares the system frequency with a reference frequency, produces control signals to shed feeders in stages. Restoration of feeders is based on improvement in the system frequency. LED indicators show the shed or restore signal generated by the processor. LED indicators are also used to indicate voltage signal failure.

CONTENTS

INTRODUCTION

The development of a load shedding and restoration system for a power system, is the subject matter of the work reported hereunder.

Tripping or re-connection of feeders for the purpose of load-shedding or restoration should take into account the system voltage, current and frequency. The measurement of these electrical quantities are normally done on analog basis. As an improvement over this, digital form of measurements were developed. Recently microprocessors are widely employed in instrumentation and control. In this project, a commercially available microprocessor trainer system has been utilised for measuring and controlling various quantities. This reduces the hardware requirements as the software capability of the microprocessor has been fully utilised.

MEASUREMENT OF VOLTAGE

The system voltage after rectification is fed to the microprocessor through an A/D convertor. The microprocessor selects the desired input by outputting an appropriate code to the multiplexer control lines of the A/D convertor. The analog signal is then converted into digital signal, which is then read by the microprocessor

MEASUREMENT OF CURRENT

The feeder current is fed to a load resistor. The voltage across the load resistor is proportional to this current. The measurement of this voltage will therefore be proportional to the current. This voltage is measured as above.

MEASUREMENT OF FREQUENCY

The period of the system voltage or current, the interval between two successive positive or negative transitions is measured with the help of the microprocessor to get the frequency.

MICROPROCESSOR BASED SYSTEM DESIGN

Since the advent of microprocessor in the year 1971, the usage of microprocessor has multiplied to an extent that a revolutionary development in the Electronic industry is presently observable. Microprocessor system design and implementation results in many benefits as discussed below.

The microprocessor is a "programmable logic device" and with reference to the field of computers, the term 'microprocessor' refers to the central processing unit of a small computer system. The microprocessor is an eelctronic integrated circuit of the LSI level. Although a microprocessor chip cannot function by itself, the addition of a few memories and I/O devices, make a typical computer system.

Microprocessors are not confined to digital computer applications alone. They are also used aso controllers, in numerically controlled machines.

MERITS OF MICROPROCESSOR BASED SYSTEM DESIGN:

Cost Savings in Hardware:

A microprocessor chip of LSI basis replaces several discrete logic gates resulting in reduction of cost as well as size of the system. Overall system design is simple .

Reliability:

As the number of components decreases, the probability of malfunctioning likewise decreases. This enhances the system performance.

Flexibility for changes:

To modify a system one has to merely reprogram the memory elements without redesigning the system. Hence system modification is achieved by merely changing the software without any modification of the hardware units.

Expandability:

Additional interfaces can be added to the system bus and the software can be suitably modified to cater system growth.

CRITERIA FOR THE CHOICE OF MICROPROCESSORS:

Given the system requirements, the choice of the microprocessor is based on the following considerations.

Nature of the task:

Whether computational or control oriented task is involved is decided first. The use of a computer oriented processor in a control application could lead to interface complexity.

Reliability:

For reliable performance in noisy environment, CMOS Processors will be better suited.

Processor loading:

The processor loading in the preliminary stage of the design should be about 50%. If the processor is loaded too little, it is better to consider a smaller and less complex chip which will consume less power.

Word size:

Larger word width means more capabilities but the complexity correspondingly increases, 4 bit processors are well suited for control applications while 8 bit processors are for general purpose applications.

Processing Speed:

Depending on the clock rate, number of cycles required to execute the given instructions, the processing capability would vary.

Power Dissipation;

For critical power systems, CMOS logic will be a better one.

Interrupt Capability:

It is an useful feature to be considered in the choice of the processor.

Input/Output Capabilities:

Programmable I/O lines will increase the system flexibility.

SOFTWARE LIFE CYCLE:

The development of software does not differ too much from hardware

design and development; and it is built by distinct stages of activity as in hardware system. The steps involved in the design of a microprocessor based system.

The various stages of development are:

* Understanding and Analysis of system functions/requirements;
* Software system design and algorithm development;
* Porgramming, coding and debugging;
* Software and combined software and hardware testing;
* Operation and maintenance.

Selection of a microprocessor is done on the basis of the points mentioned in previous section.

The selection of a particular microprocessor will strongly influence the software design. The matching of electrical characteristics and timings of IC's may create problems due to hardware design.

HARDWARE

The system voltage and current has been interfaced to the microprocessor through an analog to digital convertor. The detailed connection diagram is shown in Fig.1.

ANALOG-TO-DIGITAL CONVERSION:

The analog-to-digital converter employed is as 8 bit binary output, successive approximation type converter. The input to an A/D converter is obtained through an eight input analog multiplexer. The particular input channel being digitized by the A/D converter is determined by a 3 bit address signal for selecting the channels. These address signals are generated by the microprocessor. A schmitt trigger oscillator produces a 300kHZ clock for the A/D converter. An additional circuit is used to produce V_{cc} and V_{ref} of 5.12V for the A/D converter. With this reference voltage, the A/D converter will have 256 steps of 20mV each. This chip has a built in Sample and Hold circuit. The logic input for the Sample and Hold circuits is the "start conversion signal" given to the chip from the processor. The timing diagram for such a circuit is shown in Fig.2. ADC-0809-8bit microprocessor compatible ADC having the following salient features is used

* Resolution - 8 bits
* No missing codes
* Conversion time - 100 sec.
* Singal supply 5V(dc)
* 8 channel multiplexer with latch control logic

* Easy interface to all microprocessors
* '0-5' volt analog input voltage with single 5 Volt supply.
* Temperature ranges "-40° C to + 85°C" or "-55°C to + 125° C"
* Low power consumption (15mW)
* Operating ranges

V_{cc} : 4.5 V 6 V (dc)

MICROCOMPUTER

Microcomputer is the heart of the load shedding and restoration unit. It detects over-voltage and under-frequency conditions and gives signals to restore the system to normal operation. Microcomputer which is selected to serve this purpose is the SDA-85 system.

SDA-85 SYSTEM

The 8085 System Design Aid is a single Board Microcomputer, complete with a CPU, memory lines and Input/Output.

The 8085 System Design Aid is based on the industry standard 8085A, incorporating all the features required for it to function as a trainer and as prototype system in user applications. The features of the SDA-85 system is given in Appendix 2.

SOFTWARE

NOTATIONS:

fo - load restoration frequency

fi - trip reference frequency

I1,2,3- load on feeder groups 1,2 and 3, respectively

V - system voltage

INTRODUCTION

Since underfrequency condition is an effective indicator of the loss of balance between the power generation and the power delivered, underfrequency relays are widely used to sense this imbalance. Load shedding equipment typically incorporate a multistage underfrequency relay, which enables disconnection of loads in steps at preselected frequency values.

OPERATION LOGIC FOR LOAD SHEDDING

Tripping or disconnection of feeders for the purpose of load shedding should take into account several factors in addition to the system frequency. The operation used for load shedding in the present development work is detailed below.

FREQUENCY:

The amount by which the frequency falls below the normal value indicates extent of deficiency in generation or the extent of overloading. The common practice is to disconnect loads in three or four steps. In the present work, the feeders to be disconnected are put under three

groups 1. The group 1 is tripped as the frequency falls below a pre-selected threshold of f1. If the system frequency is still below fi the feeder group 2 is tripped and so on. The energy system may face temporary frequency dips on faults. To avoid disconnection of loads on such conditions, a time delay of 0.5 sec has been incorporated. A load tripping is carried out only if frequency remains below the selected threshold for this period.

VOLTAGE

A severe fault on the energy may also down the frequency because of the large currents. But this condition does call for disconnection of loads. Such faults invariably results in voltage dips whereas a generation-load imbalance does not. Thus tripping of loads on severe faults is prevented by monitoring the voltage in addition to frequency. Loads shall be tripped only if the underfrequency condition is not accompanied by the under-voltage conditon. Tripping of loads is blocked in the apparatus developed for voltages below 50% of the normal value.

CURRENT

If a feeder or a feeder-group is very lightly loaded, its disconnection is of little help in the regaining of generation-load balance. Such a feeder group is exempted from disconnection. To achieve this, the load shedding equipment monitors the feeder loads and in case the load in a feeder group is below 10% of the normal load then the removal of feeder group is prevented.

OPERATION LOGIC FOR LOAD RESTORATION

Tripped feeders should be restored as and when the generation deficiency is over and the normal system frequency is regained. The feeder brakers are closd when the frequency goes above a preset value fo. This restoration of feeders is done in the reverse order to that in which they are actually disconnected. To avoid unnecessary switchings, a delay of 0.5sec is provided for restoration like that of tripping.

TITLE LOAD SHEDDING AND RESTORATION

PROGRAM LISTING

MEMORY ADDRESS	LABEL	MNEMONICS	OP-CODE (HEX)	COMMENTS
				THIS PROGRAM IS WRITTEN TO RUNON SDA-85
	EQU	2001	ACVOL	ACTUAL VOLTAGE STORAGE AREA
	EQU	2004	ACFREQ	ACTUAL FREQUENCY STO-RAGE AREA
	EQU	2005	RAVOL	RATED VOLTAGE STORAGE AREA
	EQU	2006	SDREF	SHEDDING REFERENCE FREQUENCY STORAGE AREA
	EQU	2007	RSREF	RESTORATION REFERENCE FREQUENCY STORAGE AREA
	EQU	2008	CHECK	TO INDICATE THE STATE OF THE INDICATOR.
		MAIN PROGRAM		
1C00		MVI A, FF	3E FF	
1C02		STA CHECK:	32 08 20	CHECK FOR THE STATE OF THE INDICATORS
1C05		MVI A, 8A	3E 8A	CONTROL WORD
1C07		OUT 3B	D3 3B	TO CONTROL REGISTER PORT A-OUTPUT PORT, PORT B,C-INPUT PORTS
1C09		MVI E, 00	1E 00	

TITLE LOAD SHEDDING AND RESTORATION

PROGRAM LISTING

MEMORY ADDRESS	LABEL	MNEMONICS	OP-CODE (HEX)	COMMENTS
1C0B		MVI B, 0A	06 0A	
1C0D	BEGIN	MVI A, 00	3E 00	
1C0F		OUT 38	D3 38	PORT A
1C11		CALL ADC	CD 00 1D	SUBROUTINE TO MEASURE VOLTAGE
1C14		ADD E	83	
1C15		MOV E, A	5F	
1C16		DCR B	05	
1C17		JNZ BEGIN	C2 0D 1C	
1C1A		MOV L, A	6F	TOTAL VOLTAGE TO BE AVERAGED
1C1B		MVI, H, 00	26 00	
1C1D		MVI, C, 0A	0E 0A	
1C1F		CALL AVE	CD 60 1D	
1C22		STA ACVOL	32 01 20	
1C25		MVI, B, 0A	06 0A	
1C27		LXI H, 00	21 00	
1C29		LXI D, 00	11 00	
1C2B	MFREQ	CALL FREQ:	CD D0 1C	SUBROUTINE TO MEASURE FREQUENCY
1C2E		MOV E, A	5F	
1C2F		DAD D	19	
1C30		DCR B	05	
1C31		JNZ MFREQ	C2 2B 1C	

TITLE LOAD SHEDDING AND RESTORATION

PROGRAM LISTING

MEMORY ADDRESS	LABEL	MNEMONICS	OP-CODE (HEX)	COMMENTS
1C34		MVI C, 0A	0E 0A	
1C36		CALL AVE	CD 60 1D	
1C39		STA ACFREQ	32 04 20	
1C3C		LDA RAVDL	3A 05 20	
1C3C		LDA RAVOL	3A 05 20	
1C3F		RAR	1F	50% OF THE RATED VOLTAGE
1C40		MOV B, A	47	
1C41		LDA ACVOL	3A 01 20	
1C44		CMP B	B8	
1C45		JNC SHCHCK	D2 61 1C	
1C48		CALL UVIND:	CD 50 1E	SET U/V INDICATOR
1C4B		MVI C, 64	0E 64	
1C4D		CALL AVE	CD 60 1F	1% OF THE RATED VOLTAGE
1C50		MOV B, A	47	
1C51		LDA ACVOL	3A 01 20	
1C54		CMP B	B8	
1C55		JNC MEASR	D2 5B 1C	
1C58		CALL NVIND:	CD 60 1E	SET N/V INDICATOR
1C5B	MEASR	CALL DELAY1	CD 80 1F	GIVE 5 SECONDS DELAY
1C5E		JMP BEGIN	3E 0D1C	
1C61	SHCHCK	LDA SDREF	3A 06 20	
1C64		MOV B, A	47	

TITLE LOAD SHEDDING AND RESTORATION

PROGRAM LISTING

MEMORY ADDRESS	LABEL	MNEMONICS	OP-CODE (HEX)	COMMENTS
1C65		LDA ACFREQ	3A 04 20	
1C68		CMP B	B8	
1C69		JNC RESTR:	D2 90 1C	GO TO RESTORATION
1C6C	FEED 1	CALL COND1:	CD 50 1D	TEST FOR TRIP REQUIRE-MENTS OF FEEDER1
1C6F		CALL TRIP1:	CD 8D 1E	SET FEEDER1 INDICATOR
1C72		CALL DELAY1	CD 80 1F	
1C75		JMP BEGIN	3E 0D 1C	
1C78	FEED 2	CALL COND2:	CD A0 1F	TEST FOR TRIP REQUIRE-MENTS OF FEEDER2.
1C7B		CALL TRIP2:	CD 90 1E	SET FEEDER2 INDICATOR
1C7E		CALL DELAY1	CD 80 1F	
1C81		JMP BEGIN	3E 0D 1C	
1C84	FEED 3	CALL COND3:	CD 00 1E	TEST FOR TRIP REQUIRE-MENTS OF FEEDER 3
1C87		CALL TRIP3:	CD B0 1E	SET FEEDER 3 INDICATOR
1C8A		CALL DELAY1	CD 80 1F	
1C8D		JMP BEGIN	3E 0D 1C	
1C90	RESTR	LDA, RSREF	3A 07 20	
1C93		MOV, B, A	47	
1C94		LDA ACFREQ	3A 04 20	
1C97		CMP B	B8	
1C98		JNC REST1	D2 A4 1C	
1C9B		CALL NFIND:	CD 70 1E	SET N/F INDICATOR

TITLE LOAD SHEDDING AND RESTORATION

PROGRAM LISTING

MEMORY ADDRESS	LABEL	MNEMONICS	OP-CODE (HEX)	COMMENTS
1C9E		CALL DELAY1	CD 80 1F	
1CA1		JMP BEGIN	C3 0D 1C	
1CA4	REST 1	LDA CHECK	3A 08 20	
1CA7		ANI 04	E6 04	SELECT FEEDER 3
1CA9		JN REST2	CA B5 1C	
1CAC		CALL REST3:	CD C6 1C	RESET FEEDER3 INDICATOR
1CAF		CALL DELAY1	CD 80 1F	
1CB2		JMP BEGIN	C3 0D 1C	
1CB5	REST 2	LDA CHECK	3A 08 20	
1CB8		ANI 02	E6 02	SELECT FEEDER2
1CBA		JN REST 3	CA C6 1C	
1CBD		CALL RES2:	CD 20 1F	RESET FEEDER2 INDICATOR
1CC0		CALL DELAY1	CD 80 1F	
1CC3		JMP BEGIN	C3 0D 1C	
1CC6	REST3	LDA CHECK	3A 08 20	
1CC9		ANI 01:	E6 01	SELECT FEEDER1
1CCB		JZ BACK	CA D1 1C	
1CCE		CALL RES1	CD 00 1F	RESET FEEDER1 INDICATOR
1CD1	BACK	CALL DELAY1	CD 80 1F	
1CD4		JMP BEGIN	C3 0D 1C	

TITLE LOAD SHEDDING AND RESTORATION

PROGRAM LISTING

MEMORY ADDRESS	LABEL	MNEMONICS	OP-CODE (HEX)	COMMENTS
1F2C		RETURN	C9	
1F40	RES 3	MVI A, 05	3E 05	SUBROUTINE TO RESET FEEDER3 INDICATOR
1F42		OUT PORT C	D3 33	
1F44		LDA CHECK	3A 08 20	
1F47		ANI FB	E6 FB	
1F49		STA CHECK	32 08 20	
1F4C		RETURN	C9	
1F60	AVE	MVI B, 08	06 08	SUBROUTINE TO PERFORM DIVISION
1F62	DIV 1	DAD H	29	
1F63		MOV A, H	7C	
1F64		SUB C	91	
AF65		JC DIV 2	DA 6A 1F	
1F68		MOV H, A	67	
1F69		INR L	2C	
1F6A	DIV 2	DCR B	05	
1F6B		JNZ DIV1	C2 62 1F	
1F6E		MOV A, H	7C	
1F6F		RETURN	C9	
1F80	DELAY1	MVI B, 5F	96 5F	SUBROUTINE TO GET 5 SECONDS DELAY
1F82	LINK	CALL DELAY	CD BE 04	53 msecs DELAY

TITLE LOAD SHEDDING AND RESTORATION

PROGRAM LISTING

MEMORY ADDRESS	LABEL	MNEMONICS	OP-CODE (HEX)	COMMENTS
1EDA	LOOP 2	IN PORT A	DB 38	
1EDC		ANI 40	E6 40	
1EDE		JNZ LOOP2	CA DA 1E	
1EE1	LOOP 3	INX B	03	
1EE2		IN PORT A	DB 38	
1EE4		ANI 40	36 40	
1EE6		JNZ LOOP3	CA E1 1E	
1EE9		MOV L, C	69	
1EEA		MOV H, B	60	
1EEB		SHLD SFREQ	22 51 20	
1EEE		RETURN	C9	
1F00	RES1	MVI A, 01	3E 01	SUBROUTINE TO RESET FEEDER1 INDICATOR
1F02		OUT PORT C		
1F04		LDA CHECK	3A 08 20	
1F07		ANI FE	E6 FE	
1F09		STA CHECK	32 08 20	
1F0C		RETURN	C9	
1F20	RES2	MVI A, 03	3E 03	SUBROUTINE TO RESET FEEDER2 INDICATOR
1F22		OUT PORT C	D3 33	
1F24		LDA CHECK	3A 08 20	
1F27		ANI FD	E6 FD	
1F29		STA CHECK	32 08 20	

TITLE LOAD SHEDDING AND RESTORATION

PROGRAM LISTING

MEMORY ADDRESS	LABEL	MNEMONICS	OP-CODE (HEX)	COMMENTS
1F85		DCR B	05	
1F86		JNZ LINK	C2 82 1F	
1F89		RETURN	C9	
1FA0	COND2	LDA CHECK	3A 08 20	
1FA3		ANI 02	E6 02	
1FA5		JNZ FEED3	C2 84 1C	
1FA8		MVI A, 02	3E 02	SELECT FEEDER 2
1FAA		OUT PORT A	D3 38	
1FAC		CALL ADC	CD 00 1D	
1FAF		MOV B, A	47	
1FB0		LDA F2REF	3A 0A 20	
1FB3		CMP B	B8	
1FB4		JC FEED 3	DA 84 1C	
1FB7		RETURN	C9	

DISPLAY

The output of the system, ie., the trip/restore signals are indicated using LED indicators. The LED is driven by the microprocesor through the PPI, an invertor and a resistor as shown in Fig.1.6. The indication in any feeder circuit indicator shows that the feeder is to be removed. Similarly indicators are also provided to show the undervoltage and normal frequency conditions.

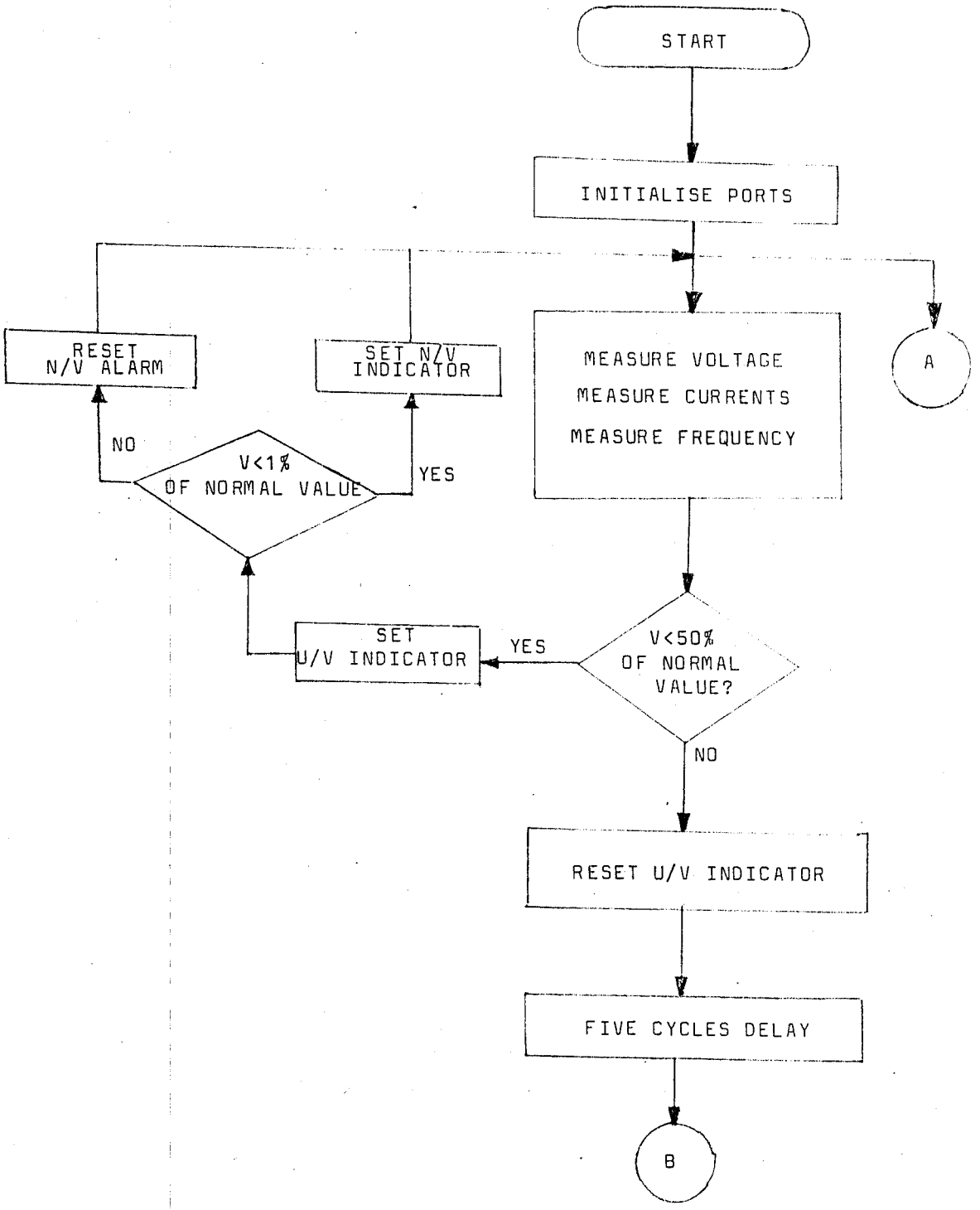
CONCLUSION

A system for shedding and restoration of loads based on an 8 bit microprocessor incorporating novel decision logics has been successfully developed. In addition to the usual criterion of fall in the system frequency for shedding loads, the logic used takes into account the actual loads on the feeders, exempting the very lightly loaded ones from disconnection of feeders.

The feeders are restored in a sequence reverse to the sequence in which they are disconnected. Disconnection of loads is prevented on voltage dips and temporary frequency dips caused by faults in the energy system. With all these considerations made, the entire load shedding and restoration operation is put on a very sound and rational footing.

It is simple to incorporate rotational sequencing of disconnection of feeders by minor modification of software. Similarly, sensing of over frequency condition and giving appropriate indication/control output signals can also be incorporated.

APPENDIX I

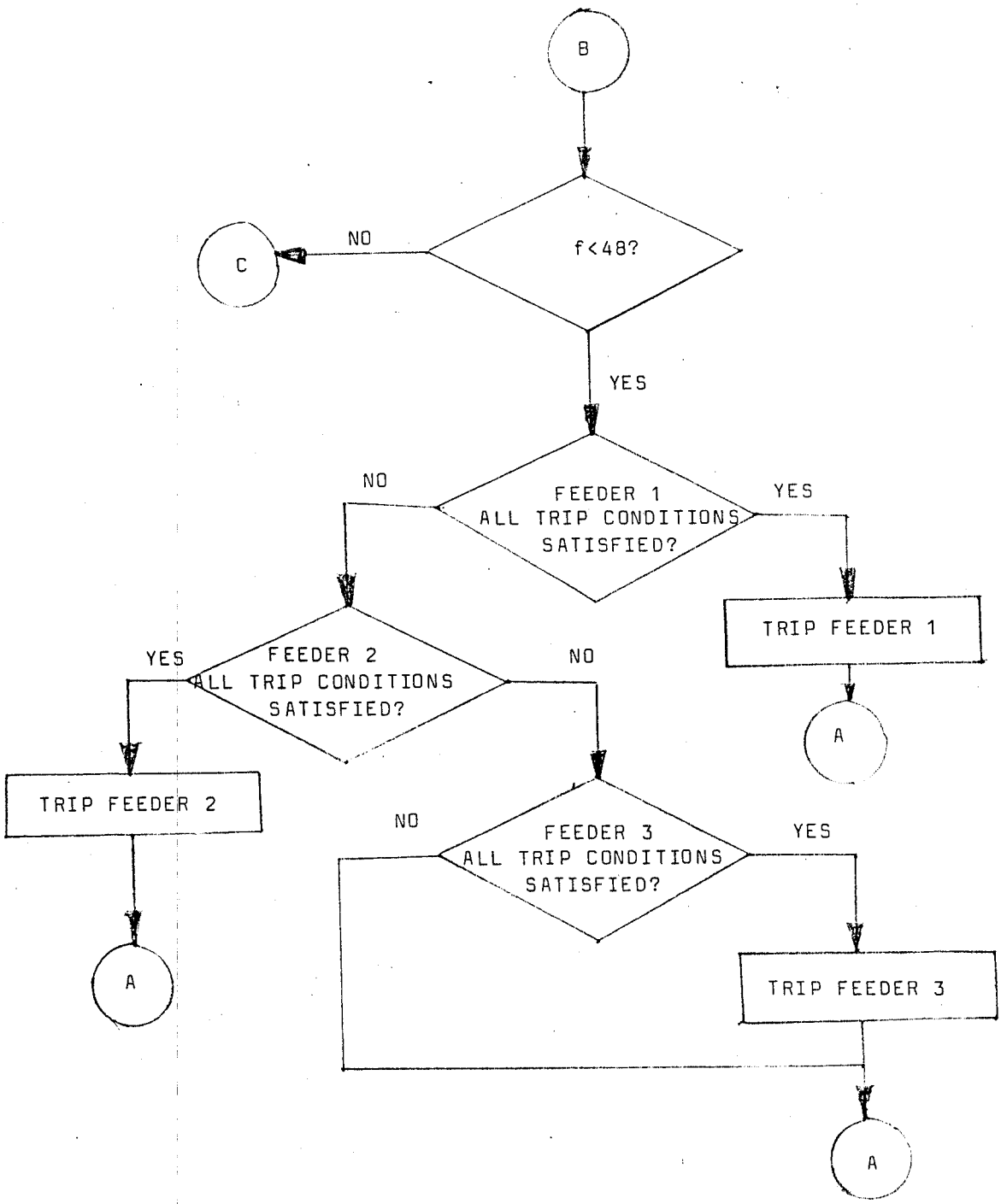


U/V - UNDER VOLTAGE

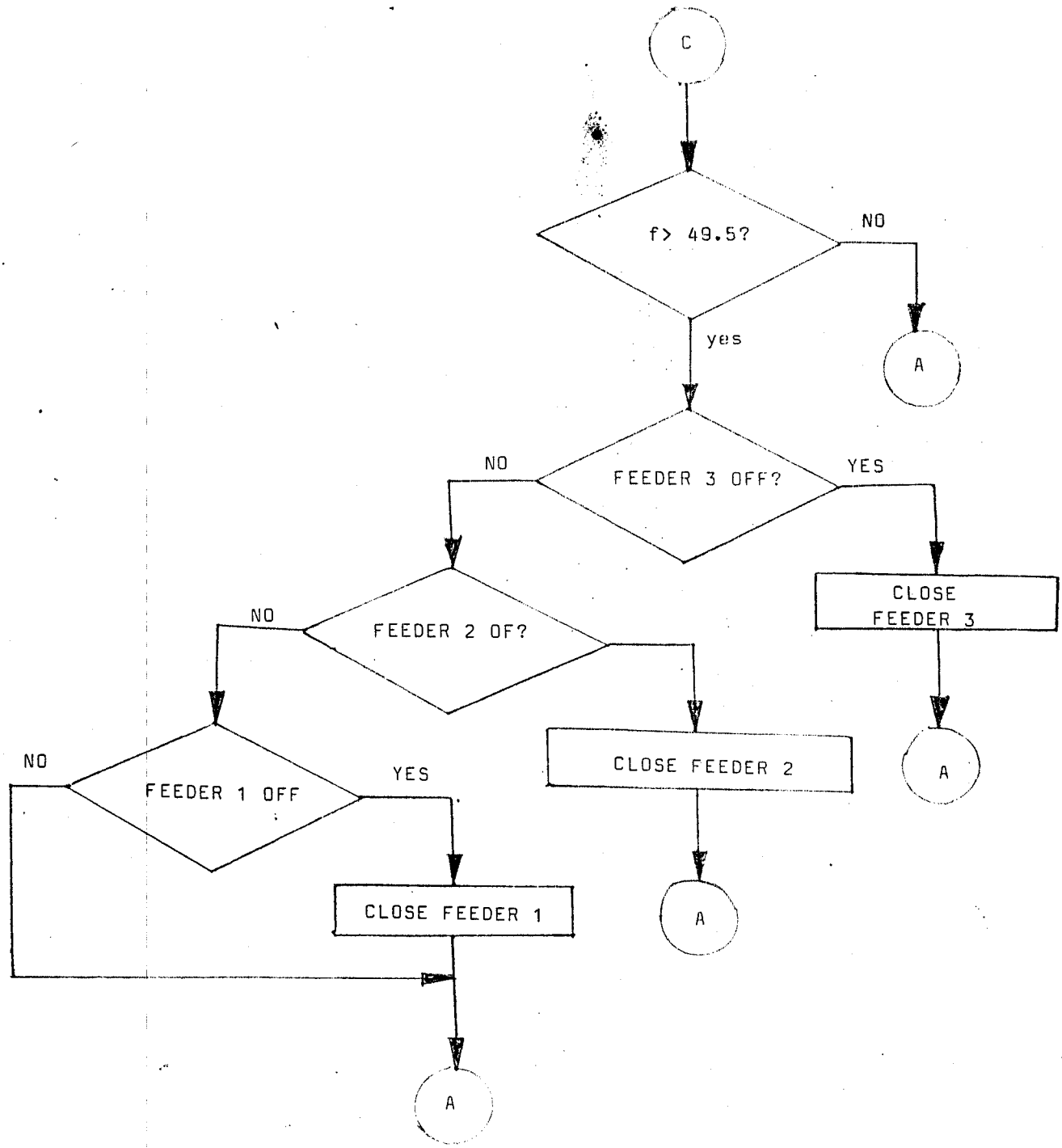
N/V - NO VOLTAGE

V - MEASURED VOLTAGE

VOLTAGE STATUS INDICATION



LOAD SHEDDING



RESTORATION

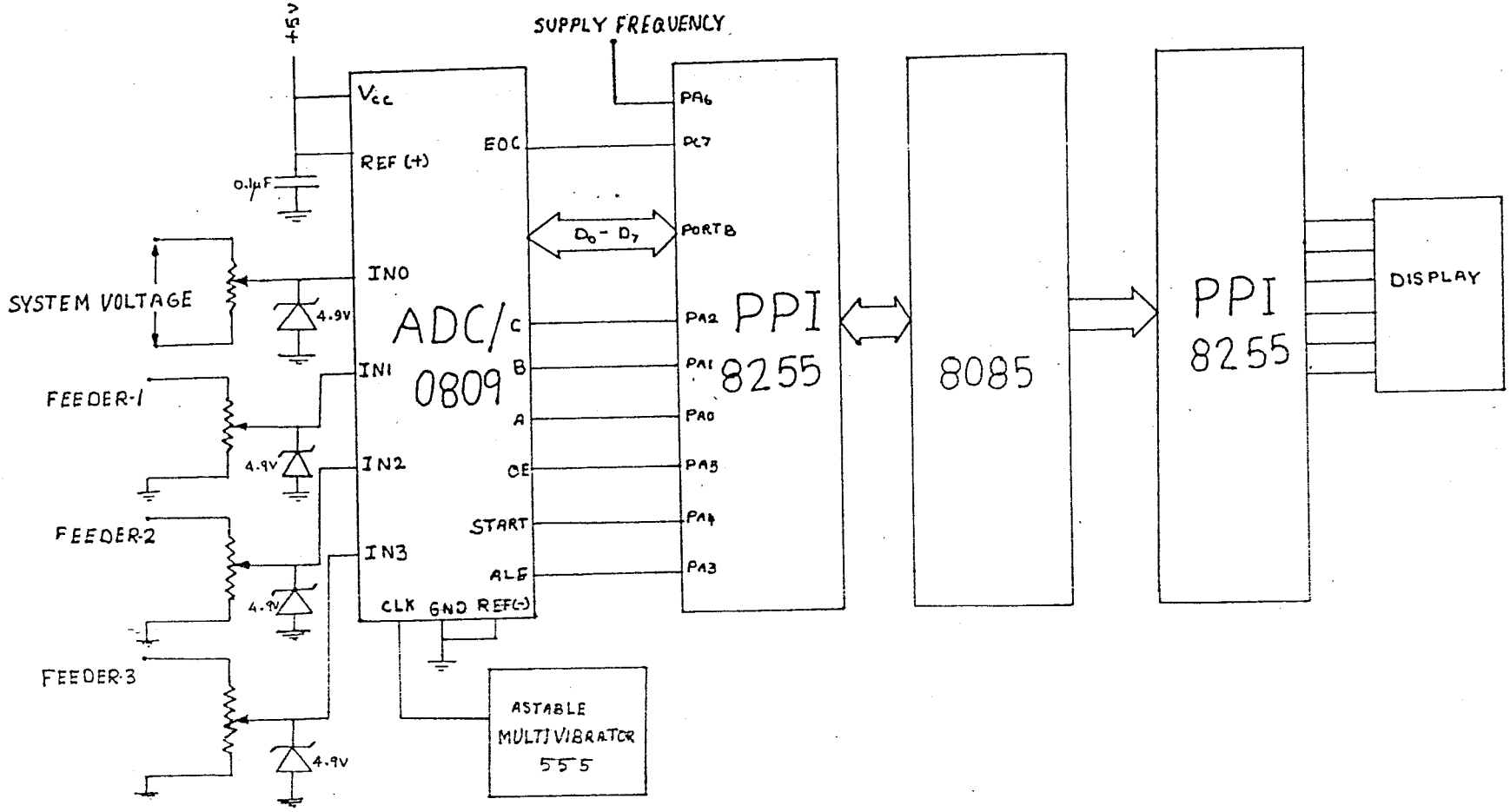
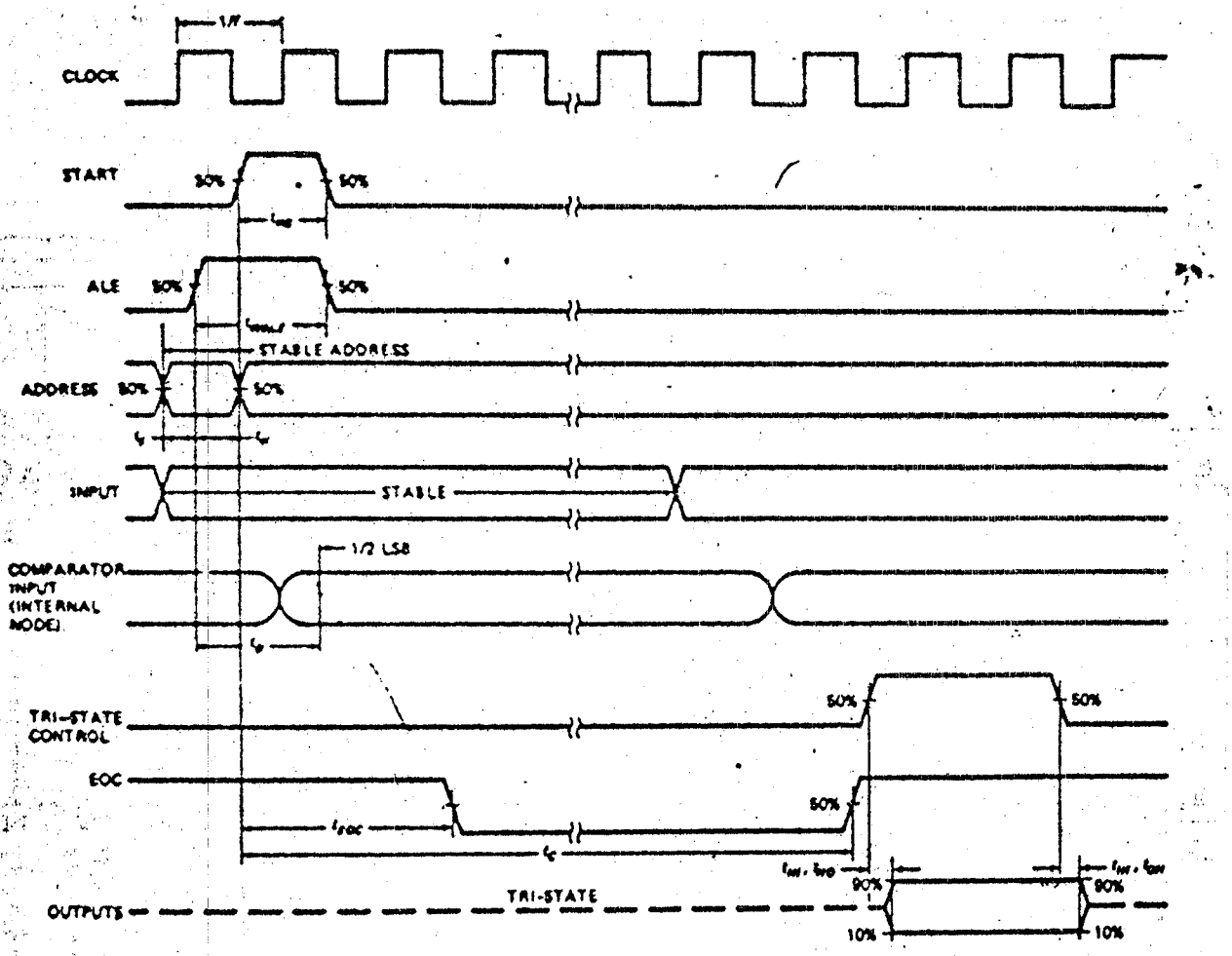
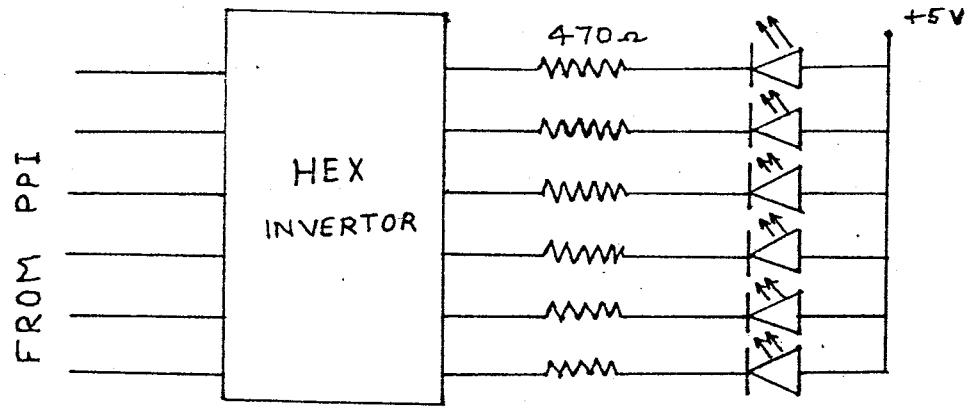


FIG-I BLOCK DIAGRAM



Timing waveforms for the ADC0808 data acquisition system.



DISPLAY CIRCUIT

APPENDIX II

SDA-85 SYSTEM

Specifications:

The specification of the system are given below:

CPU	:	8085 A
Memory	:	ROM 2716 x 1 RAM 2114 x 2
Input/Output	:	Prallel 48 lines, 8255 x 2 Serial through SID/SOD lines
Interrupts	:	TRAP, RST 7.5. RST 6.5 RST 5.5 and INTR.
Timer	:	8253 x 1
Interfaces	:	All bus and parallel Input/output signals are TTL compatible. Optional Bus drivers for BUS Expansion available. Input/output connection and Bus connection through flexible flat cables.
Keyboard/Display	:	Implemented using the 8279 Keyboard/Display controller. Six seven-segment displays, four for address field and two for data field.
Addresses	:	ROM 0 to 7 FF H 800 to FFF H (Optional) RAM IC00 to IFFF H 1800 to IBFF H (Optional)

	8279 2000 H - Data
	2001 H - Control
	8255(1) 30 H - PORT A
	(PPI) 31 H - PORT B
	32 H - PORT C
	33 H - CONTROL 1
	8255(2)
	(PPI) 38 H - PORT A
	39 H - PORT B
	3A H - PORT C
	3B H - CONTROL 2
	8253
	(TIMER) 28 H - COUNTER 0
	29 H - COUNTER 1
	2A H - COUNTER 2
	2B H - CONTROL
	8212 1 H - INPUT PORT
	$\overline{\text{INTA}}$ - Interrupt Instruction Port (Rst.Instruction)
Monitor commands	GO, SUBSTITUTE MEMORY, EXAMINE REGISTER, SINGLE STOP, BLOCK MOVE, INSERT, DELETE, DISPLAY/ PUNCH A PAPER TAPE, READ AN EPROM PROGRAM IN EPROM.
Power supply Basic kit requirement	5V $\pm$ 5%, 1.5A; $\pm$ 12V $\pm$ 10%, 100mA.

HARDWARE INFORMATION

The system consists of a keyboard, an address display of 4 digits a data display of 2 digits, Read only and Read/Write memory, 48 Programmable Input/Output lines, 3 programmable 16 bit Counter/Timers, and 8 bit interrupt Instruction port.

The 8085A CPU, operating with a 6.144 MHZ crystal, constitutes the heart of the system. The low order address lines (A_0 to A_7) are demultiplexed using an 8212, 8 bit latch/buffer. A 7418138, 3 line to 8 line decoder, is used to generate the chip selects for the on board IC's. The 74LS139, dual 2 line to 4 line decoder is used to generate chip selects for RAM and to produce $\overline{\text{MEMRD}}$ and $\overline{\text{MEMWR}}$ signals.

The keyboard/display functions are handled by another powerful peripheral IC, the 8279 keyboard/display controller.

2K x 8 EPROM(2716) contains the monitor software and provision is there, on board, for another 2716 1k x 8 RAM is provided with provision for an option 1k x 8.

Two 8255's are provided that allow the CPU, 48 programmable Input/Output lines.

Three 16 bit programmable counter/timers are made available using an 8253 peripheral IC.

An 8 bit Interrupt Instruction port is provided and it allows the user to jam an RSt instruction on the Data Bus in response to an INTR interrupt, when the CPU issues $\overline{\text{INTA}}$.

The data and control lines are buffered, using a 74LS243 bus transceiver and 74LS241 Bus driver.

The component layout of the SDA 85 kit is shown in Fig.2.1. The parallel Input/Output connector pin connections are given in Table 2.1. The Input/Output map and connector connections are given in Table 2.2.

APPENDIX III

ORGANISATION OF 8085

Data and Address Busses.

The 8085 is an 8 bit microprocessor, available as a 40 pin DIP*. The data bus is 8 bits wide which implies that 8 bits of data can be transferred to or from the 8085 in parallel. There are 8 pins which are dedicated to transmit the most significant 8 bits of the memory address. The least significant 8 bits of the address are transmitted on the 8 liner on which data is transmitted. Thus, the data and part of the address are transmitted over a set of shared lines. This is known as multiplexing.

Thus effectively, the 8085 has a 16 bit address transmission capability This implies that a total of 216 (=65536) memory locations can be addressed directly by 8085. Each location is a byte as 8 bits of data is transferred in parallel between the 8085 and the memory.

In any microcomputer,the microprocessor will be connected to memory as well as I/O devices. It is possible to design a microcomputer in since a way that an input, or an output device is treated by the microprocessor as one memory location. Thus for example, address 5may correspond to a LED display and 6 to a keyboard. This would mean that no byte in the memory would have an address 5 or 6. This form connecting I/O devices to a µp is known as memory mapped I/O.

However, it is also possible to treat I/O devices as distinct from the memory and assign to them addresses which do not conflict with the memory addresses. According to such a scheme an address such as 5 could be the address of a memory location as well as I/O devices.This scheme is known as I/O mapped I/O.

The I/O mapped I/O scheme if used, an address on the address bus may refer to either a memory location or an I/O devices. In order that the memory and the I/O devices be able to decide which one the address is meant for, the microprocessor issues another signal on the IO/M line. If this line is high then the address is meant for the I/O device otherwise it is for the memory. However the address for any input or output device can be 0 to 255 only. Thus the memory and I/O devices may use this line to decide for whom the address on the address bus is meant.

REGISTERS IN THE 8085

Inside the 8085 there are several registers which are used during the execution of a program. There is one 8 bit register known as the accumulator (abbreviated as Acc). It is used in various arithmetic and logical operation. There are six general purpose 8 bit registers that can be used for a variety of purposes.

There is a 16 bit register which is used by the 8085 to keep track of the address of the instruction that has to be executed next. The register is called the program counter (PC). The contents of the program counter are automatically updated by the 8085 during the exe-

cution of an instruction so that at the end of execution of this instruction it points to the address of the next instruction in the memory.

There is another 16 bit register known as the stack pointer (abbreviated as SP). It is used by the programmer to maintain a stack in the memory.

APPENDIX IV

PROGRAMMABLE PERIPHERAL INTERFACE

Major Features

* MCS-85 TM Compatible 8255A-5
* 24 Programmable I/O Pins
* Completely TTL Compatible
* Fully Compatible with Intel Microprocessor Families
* Improved Timing Characteristics
* Direct Bit Set/Reset Capability Easing Control Application Interface
* 40-Pin Dual-In-Line Package
* Reduces System Package Count
* Improved DC Driving Capability

The Intel 8255A is a general purpose programmable I/O device designed for use with Intel Microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the First mode(MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the seconds mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

FUNCTIONAL DESCRIPTION

General

The 8255A is a programmable peripheral interface (PPI) device designed for use in Intel microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 8255A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 8255A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/write and Control logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

(CS)

Chip Select. A "low" on this input pin enables the communication between the 8255A and the CPU.

(RD)

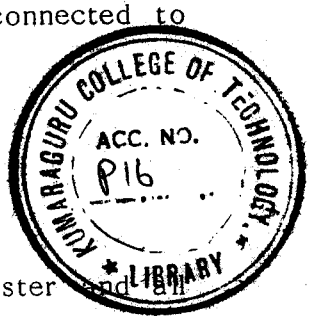
Read. A "low" on this input pin enables the 8255A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255A.

(WR)

Write. A "low" on this input pin enables the CPU to write data or control words into the 8255A.

(A_0 and A_1)

Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus (A_0 and A_1).



(RESET)

Reset. A "high" on this input clears the control register and all ports (A, B, C) are set to the input mode.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 8255A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 8255.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words"

OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software.

Mode 0 - Basic Input/Output

Mode 1 - Strobed Input/Output

Mode 2 - Bi-directional Bus

When the reset input goes "high" all ports will be set to the input mode (i.e., all 24lines will be in the high impedance state). After the reset is removed the 8255A can remain in the input mode with no additional initialization required. During the execution of the system program any of the other modes may be selected using a single output instruction. This allows a single 8255A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be seperately defined, while Port C is divided into two portions as required by the Port A and Port B definition. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance, Group B can be programmed in Mode O to monitor simple switch closings or display computational results. Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

from the internal data bus and issues the proper commands to its associated ports.

Ports A, B and C

The 8255A contains three 8-bit prots (A,B and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255A.

Port A. One 8-bit data output latch/buffer and one 8-bit data input latch.

Port B. One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C. One 8-bit output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit ports contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 8255A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single Output instruction. This feature reduces software requirements in Control-based applications. When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Note

All mask flip-flops are automatically reset during mode selection and device Reset:

Operating modes

Mode 0 (Basic Input/Output)

This functional configuration provides simple input and output operations for each of the three ports. No 'handshaking' is required, data is simply written to or read from a specified port.

Mode 0 - Basic functional definitions

* Two 8-bit ports and two 4-bit ports
* Any port can be input or output
* Outputs are latched
* Inputs are not latched
* 16 different input/output configurations are possible in this mode.

Mode 1 (Strobed Input/output)

This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or 'handshaking' signals. In mode 1, port A and port B use the lines on port C to generate or accept these 'handshaking' signals.

Mode 1 - Basic function definitions

* Two groups (Group A and Group B)
* Each group contains one 8-bit data port and one 4-bit control/data port
* The 8-bit data port canbe either input/or output. Both inputs and outputs are latched.
* The 4-bit port is used for control and status of the 8-bit data port.

Mode 2 (Strobed Bidirectional Bus I/O)

This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both trans-

mitting and receiving data (bidirectional bus I/O). 'Handshaking' signals are provided to maintain proper bus flow discipline in a similar manner to mode 1. Interrupt generation and enable/disable functions are also available.

Mode 2- Basic functional definitions

* Used in Group A only
* One 8-bit, bidirectional bus port (Port A) and a 5-bit control port (Port C)
* Both inputs and outputs are latched
* The 5-bit control port (Port C) is used for control or status for the 8-bit, bidirectional bus port (Port A).

Special Mode Combination Considerations

There are several combinations of modes when not all of the bits in port C are used for control or status. The remaining bits can be used as follows.

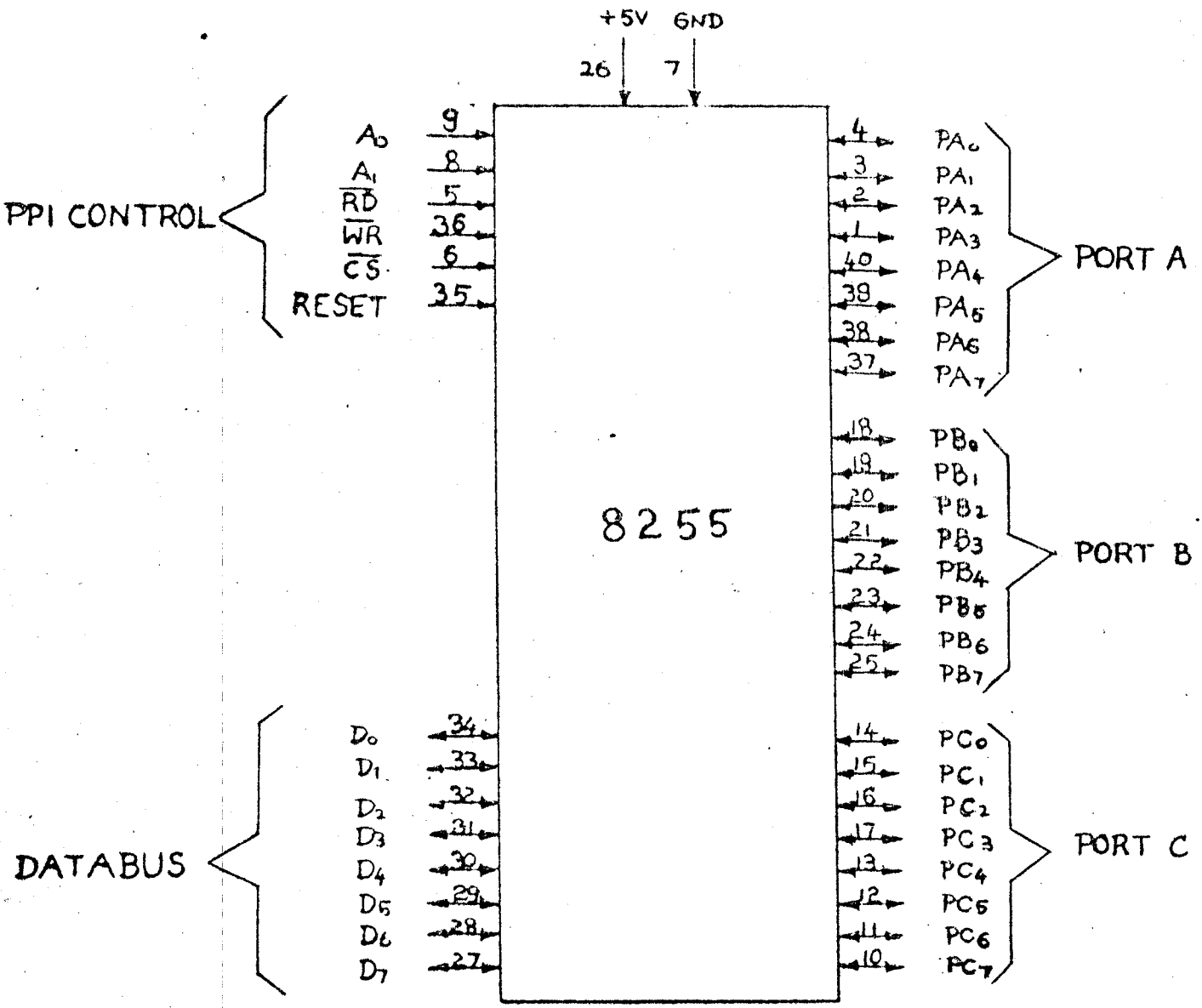
If programmed as inputs-

All input lines can be assesed during a normal port C read

If programmed as outputs-

Bits in C upper (PC_4 - PC_7) must be individually accessed using the bit set/reset function.

Bits in C lower (PC_0 - PC_3) can be accessed using the bit set/reset function or acessed as a three some by writing into port C.


+5V
GND
26
7
PPI CONTROL
A0
A1
RD
WR
CS
RESET
9
8
5
36
6
35
8255
4
3
2
1
40
39
38
37
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PORT A
18
19
20
21
22
23
24
25
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PORT B
DATABUS
D0
D1
D2
D3
D4
D5
D6
D7
34
33
32
31
30
29
28
27
14
15
16
17
13
12
11
10
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
PORT C

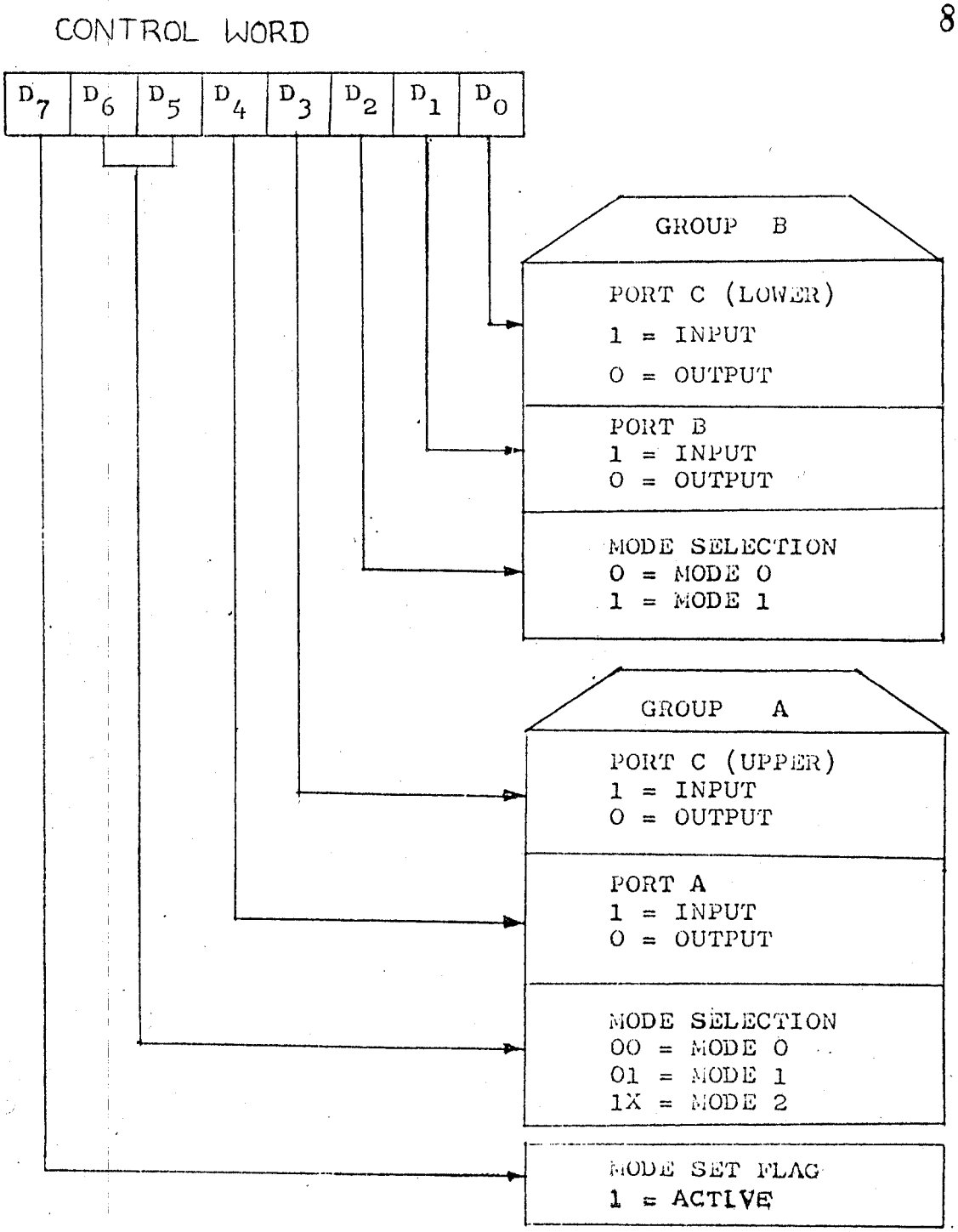


FIG-9.2-MODE DEFINITION FORMAT

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APPENDIX A

8085A INSTRUCTION SET REFERENCE CHART

DATA TRANSFER GROUP

Mnemonic		OP Code	T States	Machine Cycles
MOV	A,A	7E	4	F
	A,B	78	4	F
	A,C	79	4	F
	A,D	7A	4	F
	A,E	7B	4	F
	A,H	7C	4	F
	A,L	7D	4	F
	A,M	7E	7	FR
MOV	B,A	47	4	F
	B,B	4Ø	4	F
	B,C	41	4	F
	B,D	42	4	F
	B,E	43	4	F
	B,H	44	4	F
	B,L	45	4	F
	B,M	46	7	FR
MOV	C,A	4F	4	F
	C,B	48	4	F
	C,C	49	4	F
	C,D	4A	4	F
	C,E	4B	4	F
	C,H	4C	4	F
	C,L	4D	4	F
	C,M	4E	7	FR
MOV	D,A	57	4	F
	D,B	5Ø	4	F
	D,C	51	4	F
	D,D	52	4	F
	D,E	53	4	F
	D,H	54	4	F
	D,L	55	4	F
	D,M	56	7	FR
MOV	E,A	5F	4	F
	E,B	58	4	F
	E,C	59	4	F
	E,D	5A	4	F
	E,E	5B	4	F
	E,H	5C	4	F
	E,L	5D	4	F
	E,M	5E	7	FR
MOV	H,A	67	4	F
	H,B	60	4	F
	H,C	61	4	F
	H,D	62	4	F
	H,E	63	4	F
	H,H	64	4	F
	H,L	65	4	F
	H,M	66	7	FR
MOV	L,A	6F	4	F
	L,B	68	4	F

DATA TRANSFER GROUP (CONTD.)

Mnemonic		OP Code	T States	Machine Cycles
	L,C	69	4	F
	L,D	6A	4	F
	L,E	6B	4	F
	L,H	6C	4	F
	L,L	6D	4	F
	L,M	6E	4	FR
MOV	M,A	77	7	FW
	M,B	7Ø	7	FW
	M,C	71	7	FW
	M,D	72	7	FW
	M,E	73	7	FW
	M,H	74	7	FW
	M,L	75	7	FW

MOVE IMMEDIATE

MVI	A,D8	3E	7	FR
	B,D8	Ø6	7	FR
	C,D8	ØE	7	FR
	D,D8	16	7	FR
	E,D8	1E	7	FR
	H,D8	26	7	FR
	L,D8	2E	7	FR
	M,D8	36	1Ø	FRW

LOAD IMMEDIATE

LXI	B,D16	Ø1	1Ø	FRR
	D,D16	11	1Ø	FRR
	H,D16	21	1Ø	FRR
	SP,D16	31	1Ø	FRR

LOAD/STORE

LDAX	B,	ØA	7	FR
LDAX	D,	1A	7	FR
LDA	,ADR	3A	13	FRRR
LHLD	,ADR	2A	16	FRRRR
STAX	B,	Ø2	7	FW
STAX	D,	12	7	FW
STA	,ADR	32	13	FRRW
SHLD	,ADR	22	16	FRRWW

MISC

DAA		27	4	F

ARITHMETIC AND LOGICAL GROUP

Mnemonic		OP code	T state	Machine Cycle
ADD	A	87	4	F
	B	8Ø	4	F
	C	81	4	F
	D	82	4	F
	E	83	4	F
	H	84	4	F
	L	85	4	F
	M	86	7	FR
ADC	A	8F	4	F
	B	88	4	F
	C	89	4	F
	D	8A	4	F
	E	8B	4	F
	H	8C	4	F
	L	8D	4	F
	M	8E	7	FR
SUB	A	97	4	F
	B	9Ø	4	F
	C	91	4	F
	D	92	4	F
	E	93	4	F
	H	94	4	F
	L	95	4	F
	M	96	7	FR
SBB	A	9F	4	F
	B	98	4	F
	C	99	4	F
	D	9A	4	F
	E	9B	4	F
	H	9C	4	F
	L	90	4	F
	M	9E	7	FR
INR	A	3C	4	F
	B	Ø4	4	F
	C	ØC	4	F
	D	14	4	F
	E	1C	4	F
	H	24	4	F
	L	2C	4	F
	M	34	1Ø	FRW
INX	B	Ø3	6	S
	D	13	6	S
	H	23	6	S
	SP	33	6	S
DCR	A	3D	4	F
	B	Ø5	4	F
	C	ØD	4	F
	D	15	4	F
	E	1D	4	F
	H	25	4	F
	L	2D	4	F
	M	35	1Ø	FRW
DCX	B	ØB	6	S
	D	1B	6	S
	H	2B	6	S
	SP	3B	6	S

Mnemonic		OP code	T state	Machine Cycle
ANA	A	A7	4	F
	B	AØ	4	F
	C	A1	4	F
	D	A2	4	F
	E	A3	4	F
	H	A4	4	F
	L	A5	4	F
	M	A6	7	FR
XRA	A	AF	4	F
	B	A8	4	F
	C	A9	4	F
	D	AA	4	F
	E	AB	4	F
	H	AL	4	F
	L	AD	4	F
	M	AE	7	FR
ORA	A	B7	4	F
	B	BØ	4	F
	C	B1	4	F
	D	B2	4	F
	E	B3	4	F
	H	B4	4	F
	L	B5	4	F
	M	B6	7	FR
CMP	A	BF	4	F
	B	B8	4	F
	C	B9	4	F
	D	BA	4	F
	E	BB	4	F
	H	BC	4	F
	L	BD	4	F
	M	BE	7	FR

ARTH/LOGIC IMMEDIATE

ADI	D8	C6	7	FR
ACI	D8	CE	7	FR
SUI	D8	D6	7	FR
SBI	D8	DE	7	FR
ANI	D8	E6	7	FR
XRI	D8	EE	7	FR
ORI	D8	F6	7	FR
CPI	D8	FE	7	FR

BRANCH I/O AND CONTROL

JMP	Adr	C3	1Ø	FRR
JNZ	Adr	C2	7/10	FR/FRR
JZ	Adr	CA	7/10	FR/FRR
JNC	Adr	D2	7/10	FR/FRR
JC	Adr	DA	7/10	FR/FRR
JPO	Adr	E2	7/10	FR/FRR
JPE	Adr	EA	7/10	FR/FRR
JP	Adr	F2	7/10	FR/FRR

IN	DB	1Ø	FRI
OUT	D3	1Ø	FRO

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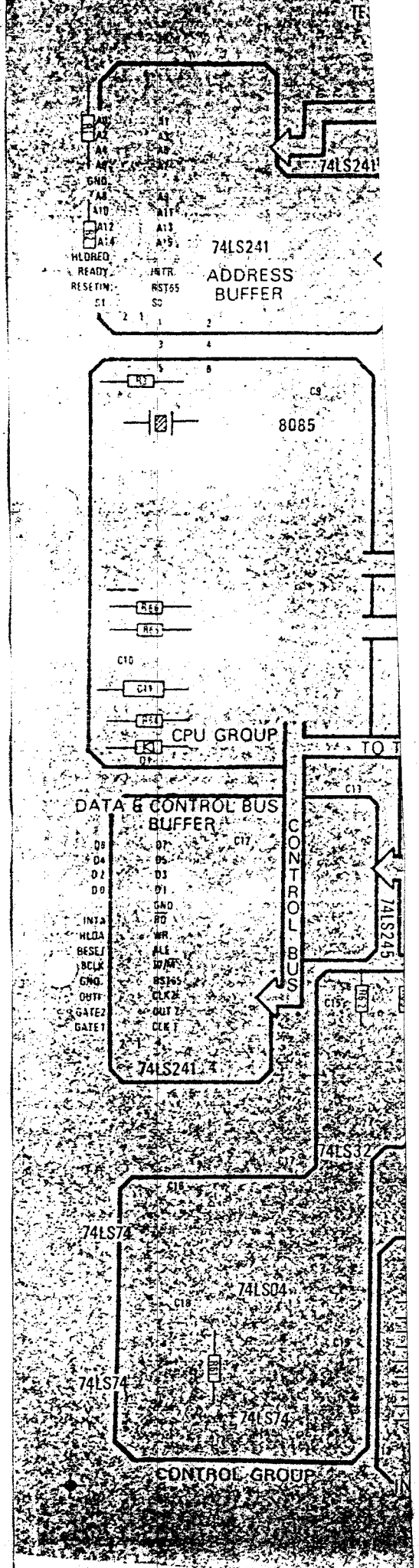
74LS241
ADDRESS
BUFFER
8085
CPU GROUP
DATA & CONTROL BUS
BUFFER
CONTROL BUS
74LS245
74LS241
74LS32
74LS74
74LS04
74LS74
74LS74
CONTROL GROUP