Microprocessor Controlled Versatile Process Monitoring System

A PROJECT REPORT
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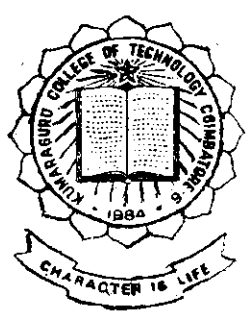

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P-171

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SYNOPSIS

A recent and fascinating innovation in the digital electronics field is the automation of the industrial activities in performing continuous tasks. The versatile process monitoring system deals mainly on the automatic product despatching system in major industries by implementing on line inspection, achieved by optical line crossing and sensing method. Whenever the object crossed the light path, it will be immediately sensed by the Light dependent resistor (LDR) whose output is given to the pulse shaping circuit. The output is given to the microcontroller through the interfacing circuitry. This microcontroller is again pre-programmed to meet our needs of despatching the required number of pieces. Once the condition is met the microcontroller gives out a control signal to open the relay thereby stopping the motor and simultaneously gives an alarm signal to the operator informing the termination of the process.

CONTENTS

CHAPTER I

INTRODUCTION

Now-a-days industries have entered into the modern field of making innovative approches to achieve better results. This versatile process monitoring system is mainly intended to areas where automation in continuous process is very much needed. Now-a-days the importance of industrial automation has been greatly realised and is made in all major industries. One of this achievement is the despatching of the industrial products automatically to meet our needs. This is made possible through the use of a Microprocessor which has the central processing unit, along with its peripherals and interfacing unit which helps to drive the system. The entire process is initiated by the software program developed for this purpose. Thus the microprocessor surpases the human capability in performing repetitious operations.

Obviously this shows the power of using micro-computers in the industries. There are lot more to be known in automative electronics.

This project confines to the following :

1. Counting the number of products as and when they are passed over the conveyor belt automatically.

2. Pre-programming the number of products to be despatched over the conveyor belt automatically and stopping the despatch process once the pre-programmed level is reached.

1.2 Advantages of Digital system:

The advantages of digital method over analog method are as follows :

1. Increased resolution.
2. Reliability.
3. Higher Accuracy.
4. Less manual error.
5. Less maintenance.

Due to the above salient features of digital methods and the rapid developments in the field of digital ICs, the use of microprocessor for process monitoring system stands out to be the efficient, simpler and best choice.

CHAPTER II PROCESS IN NUTSHELL

The main aim of this project is to automate the product despatching system in major industries by implementing on line inspection system. On line inspection system is achieved by optical line crossing and sensing method. In this method the object is moved on the conveyor belt. To one side of the conveyor belt is the optical source and to the other side is the optical sensor unit. Once the object crosses the optical beam, it obstructs the optical beam path and this is sensed by the sensor unit. Which is mainly the light dependent resistor LDR. This detected pulse is transferred to a micro computer by suitable interfacing techniques. The micro computer is programmed in such a way that the quantity to be despatched and their designation is met. Thus each contents are stored in the memory registers and when the desired quantity has been reached control signals are received from the micro computer and these controls will be utilised to monitor further process and alarms are given to the operator. By incorporating this method, apart from attaining the automation in despatching, we are also on the safer side of over riding the errors that may occur during the despatching process done manually. Also the time taken for this process is very much less compared to the manual process and it is more accurate.

CHAPTER III FUNCTIONAL BLOCK DIAGRAMS

The block diagram is the simple pictorial representation of the step by step process of the system under operation. The block diagram 3.1 gives the principal blocks involved in the versatile process monitoring system from which we get an idea behind its operation in an explicit manner. Later we will take each block into account and discuss in detail.

The figure 3.1 illustrates the closed loop control system involved in the process monitoring system. The set value is the desired quantity in hexadecimal code which is stored in the micro computer register. Light Dependent Resistor (LDR) acts as the photo sensing element and the schmitt trigger unit acts as the pulse shaping circuit which is connected to the micro computer unit. Thus each count pulses are fed back to the digital comparator unit in micro computer unit and compared with the set value everytime. If the difference between set value and count value becomes zero, control circuitry is activated to stop the drive system and gives an alarm signal to the operator.

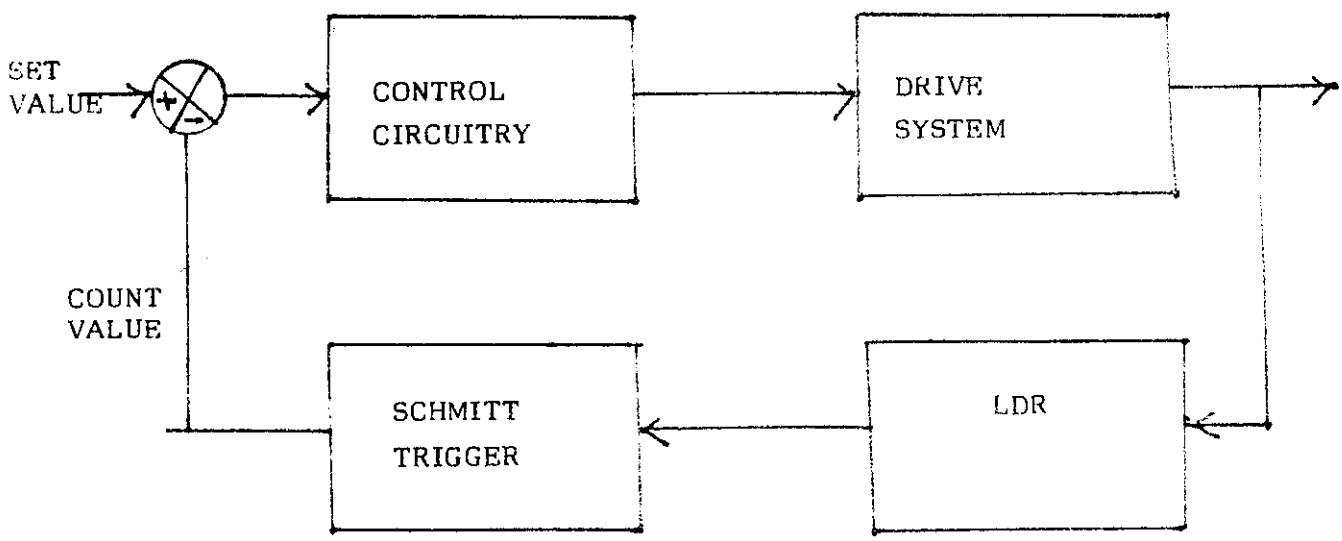


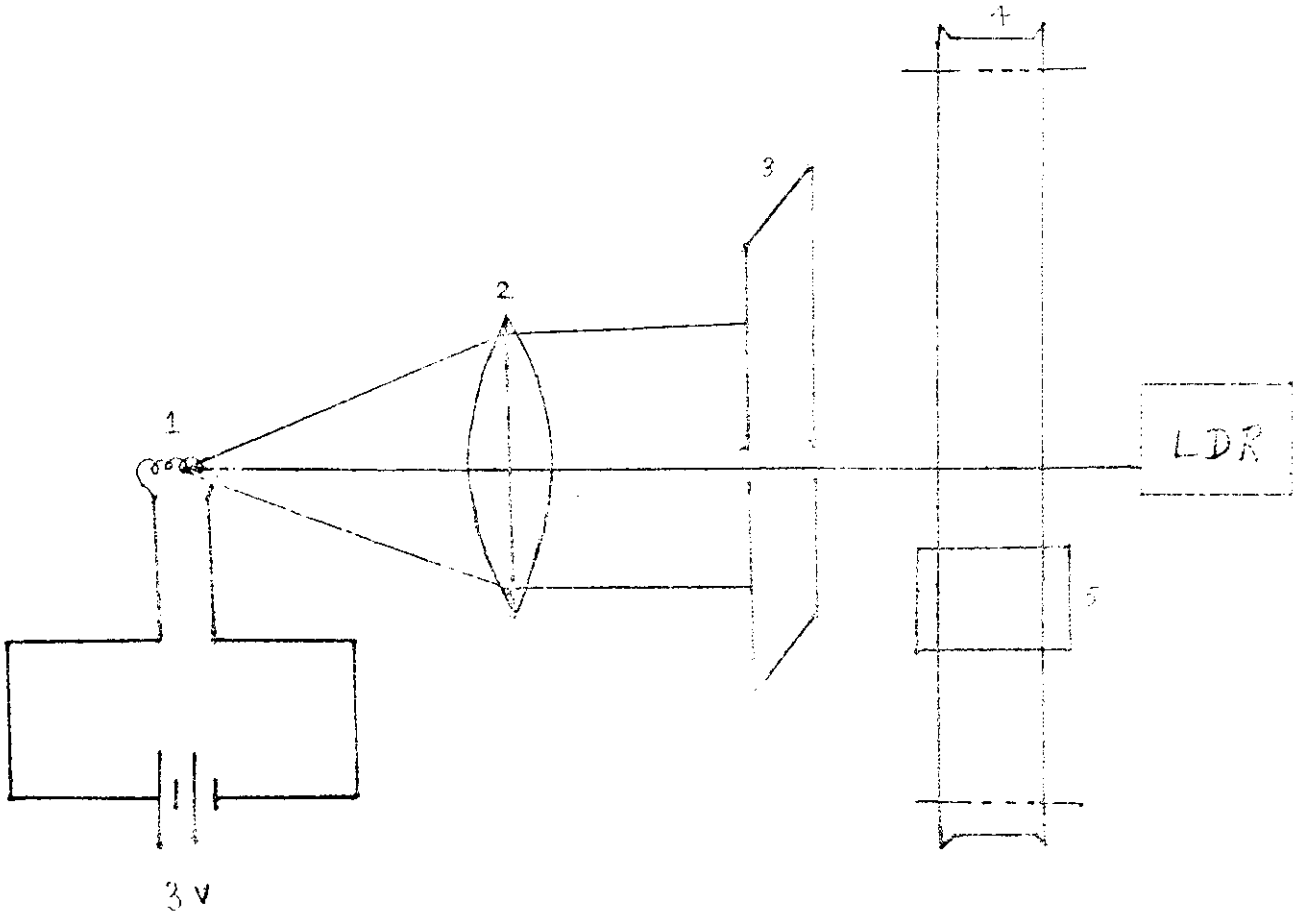
FIG. 3.0 : BLOCK DIAGRAM

3.1 Optical source unit:

The optical source used here is a 6V bulb or a pen torch activated by battery arrangement. The diverging beam from the source is converged to a thin pencil beam of ray by using a fibre optic flat type convex lens. Then the converged beam from the lens is passed through a slit arrangement. By doing so, we get a more precised and sharp beam of optical light to be focusseD on the Light dependent resistor (LDR). So as the beam width decreases, the resolution increases and hence small objects which cross the optical path can be easily detected. Which bends the incoming parallel rays so that they coverage to a real focus. The distance from a lens to its focal point for parallel rays is called the focal length of the lens. For the converging lens used here the focal length is positive.

The rays extending from the slit to the LDR all have the same optical path lengths. Since the light rays are in phase at the plane of the slit, they will still be in phase at LDR and hence the central point of the LDR has the maximum intensity.

The pictorial representation of the optical source unit is shown clearly in fig. 3.1.



1. BULB
2. CONVEX LENS
3. SLIT
4. CONVEYOR
5. OBJECT

FIG. 3.1. OPTICAL SOURCE UNIT

3.2 Optical sensor unit:

The second section of the project is the optical sensor unit. We intend to use Light dependent resistor (LDR) as our optical sensor unit. LDR is placed on the opposite side of the optical source in such a way that the focussed beam of light falls on the LDR.

The Light dependent resistor has negative resistance co-efficient with the intensity of the light. It implies that whenever the LDR is exposed to the optical source, the resistance gets reduced to a lower value and the resistance becomes higher when the LDR is unexposed to the light.

The pictorial representation of the optical sensor unit is clearly shown fig. 3.2.

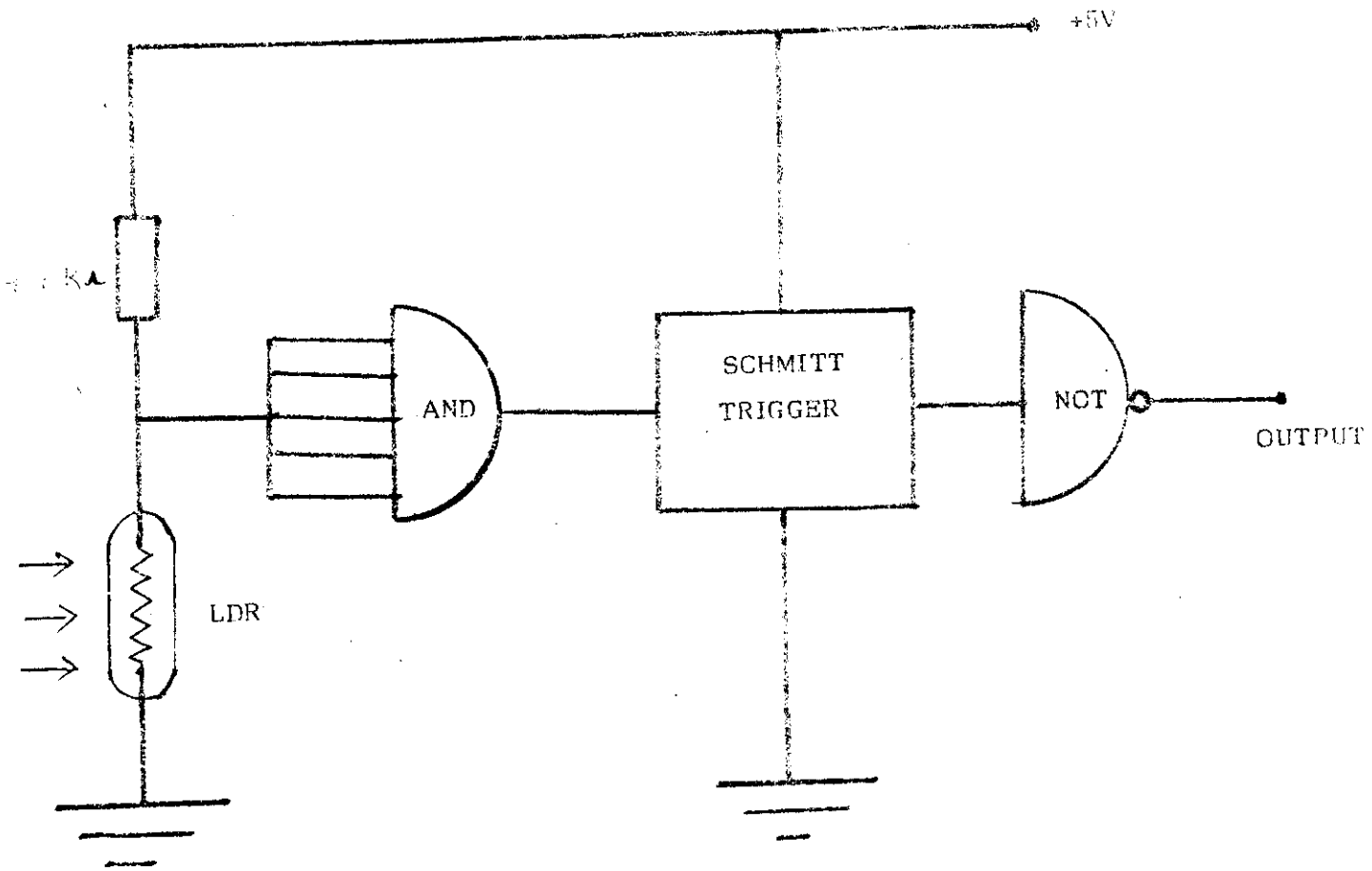


FIG. 3.2. OPTICAL SENSOR UNIT

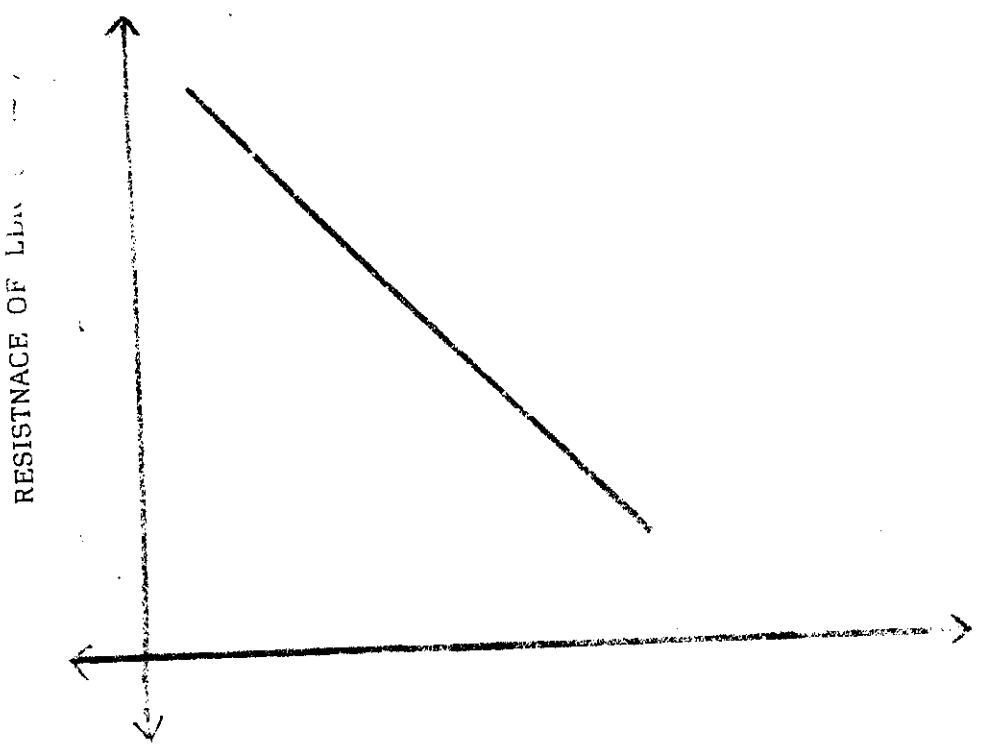


FIG. 3.2.A : VARIATION OF LIGHT INTENSITY WITH RESISTANCE

3.3 Pulse shaping circuitry:

The output of the optical sensor unit (i.e) the LDR which is about 5V is fed to pulse shaping circuit. Here we use dual 4 input nand Schmitt trigger chip IC74LS13 for the pulse shaping phenomenon.

The dual Schmitt trigger functions are compatible with standard TTL output logic levels. Each function is essentially a 4 input Nand gate with different input threshold levels for positive and negative going signals. Typically the hysteresis, the difference between the two threshold levels is 800 mV. They are capable of transforming slowly changing input signals in to sharply defined, jitter-free output signals. Additionally, they have a greater noise margin than conventional NAND gate.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter that drives a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions and provide different input threshold voltages for positive and negative going transitions. This hystersis between the positive going and negative going input thresholds is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations. The Schmitt trigger can be triggered from slow input ramps and straight dc levels.

Circuit operations:

The dual Nand Schmitt trigger IC is used as the pulse generating device. In the Fig. 3.2. the resistor R is designed to set the upper tripping point (UTP) for the Schmitt trigger. When the light falls on the LDR, its resistance goes low and the conductivity increases in proportion to the intensity of light rays. Thus the lower tripping point (LTP) of the Schmitt trigger is zero volts. It is fed at the input of the invertor gate. So +5 volts is available at the output.

If the light rays are absent, the resistance of the LDR will go higher and the Schmitt trigger is biased with the upper tripping point. Now the Schmitt trigger output will b +5 volts. and the inverter gate will give zero volts at the output terminal. The optical sensor output is fed to the port A of 8255.

3.4 Control circuitary:

The control circuit consists of a switching transistor, a control relay, a damping diode and a spike quencher circuit.

The figure 3.4 illustrates all the circuit elements in detail. The supply voltage for the switching transistor has been fixed as V_{cc} = 12V.

Circuit operation:

The required number of objects to be maintained is pre-setted. When the number of objects increases, the LDR output also increases and results in the value of V_{IN} has been raised in proportion to the number of objects. As the number of objects exceed the limit, the output voltage from the comparator becomes positive and fed to the base of the switching transistor.

As soon as the base becomes positive, the transistor turns 'ON' and the collector current flows through the relay circuit thereby energizing the relay. Across the relay coils, there is a damping diode and a spike quencher circuit. The damping diode is nothing but a PN silicon junction diode which

D - DAMPING DIODE
CR - CONTROL RELAY
IMPEDANCE : 200
VOLTAGE : 12V
Z - ZENER DIODE
R+C - SPIKE QUENCHER

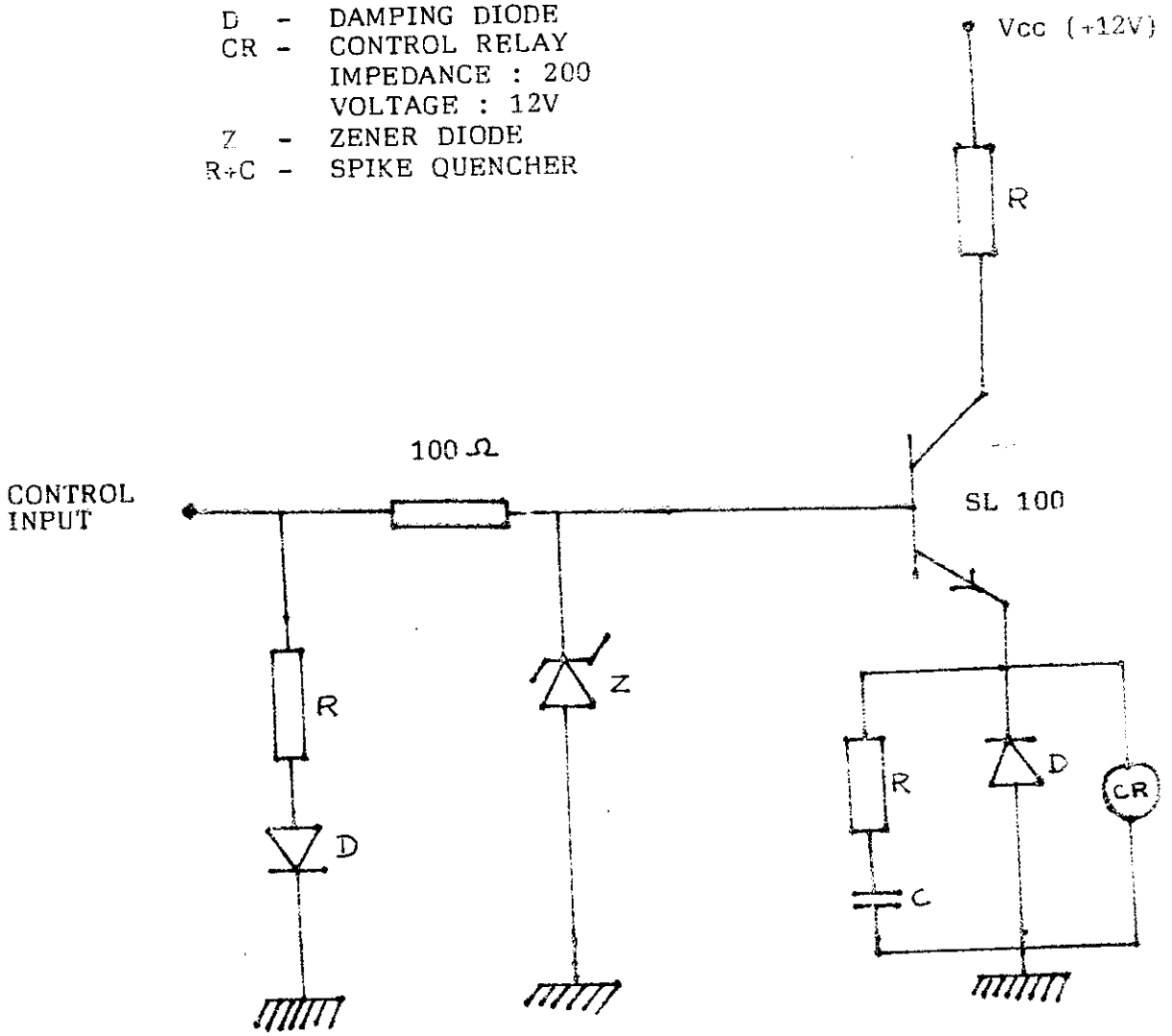


FIG. 3.4 CONTROL CIRCUITARY

acts as a degenerating element for the induced emf across the relay coil. It provides a reverse path for the residual magnetizing current during the relay operations. The spike squencher or killer degenerates the sharp spikes during frequent operations of the relay unit. The resistor and capacitor elements in series acts as a filter circuit for damped spikes.

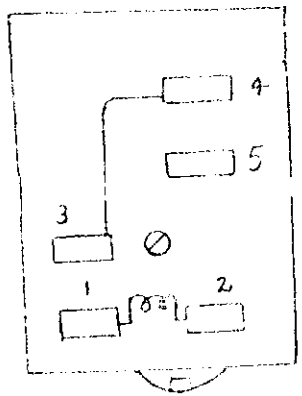
Zener operation:

This is a voltage limiting circuit consisting of a reverse biased zener diode and a bleeding resistor. This reverse biased zener diode acts as a voltage limiter element. The value of the zener breakdown voltage is selected as V_Z = 1.8 volts, which is enough for switching the transistor 'ON'. The bleeding resistor acts as a voltage dividing element, whose function is to drop the excessive voltage rather than 1.8 volts. Thus the buffer and voltage limiting circuit is essential to prevent the switching transistor from over voltage breakdown.

3.5 Control relay structure:

The internal structural details of an electromagnetic relay can be well understood from the pictorial representation of figure 3.5.

1. ELECTROMAGNET HEAD
2. IRON PLATE
3. POLE REED
4. RESTORING SPRING
5. RELAY COIL
6. FIXING SCREW
7. TOGGLE POINT
8.



FRONT VIEW

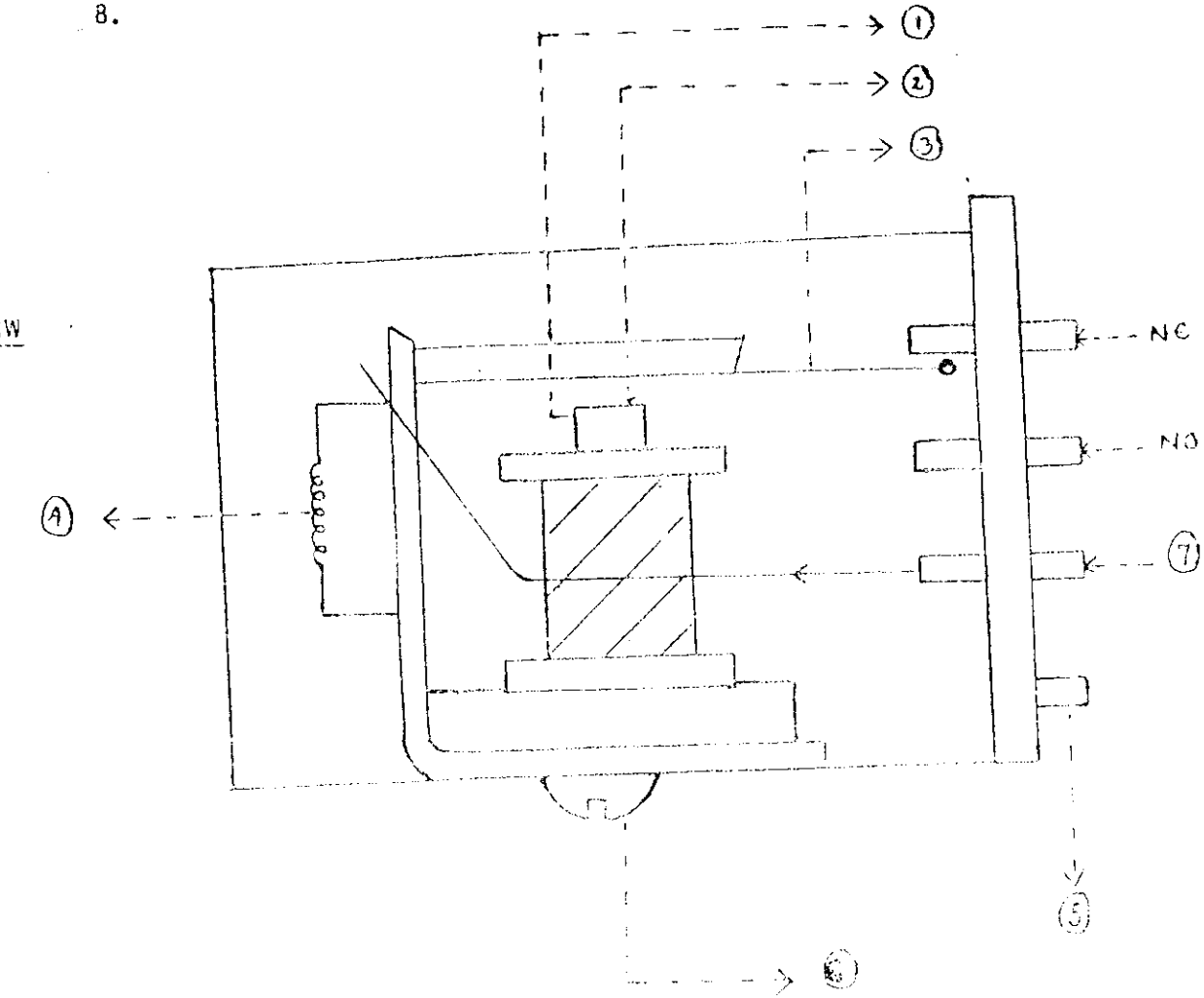


FIG. 5. CONTROL RELAY STRUCTURE

As shown in fig. 3.5 there is an electromagnet and pole reed arrangement whose displacement is restored by a restoring spring. The pole reed is attracted by the electromagnet head while the relay coil has been emergised. Since the coil is activated, the normally connected point is turned to normally opened position. When the relay coil has been de-energised, the pole reed is brought back to its initial position by the restoring spring. There are provisions for mounting the relay on a PCB using screws and nuts. The whole unit has been enclosed with a dielectric plastic chassis to prevent electric shock.

3.6 Sensitivity range selection:

In the normal biasing condition as shown in the circuit, (i.e. V_{cc} = 5V ; R_L = 47K) the input threshold voltage for the Schmitt trigger to switch 'ON' is defined as 0.9V for negative going pulse and 1.7V for positive going pulse. But the need for selecting the intensity range to various intensity of light range in industrial operating condition is essential.

Thus we are adopting range selector switch to select various input impedence which will suit our requirement. Here the minimum input threshold voltage is varied to lower values depending upon the open light atmosphere. The characteristic curve (input Vs output curve) is shifted to desired position by implementing the range selector switch.

3.7 Drive system:

Many industrial applications require the provision of a variable-speed rotary drive for their operation. Initially the majority of variable-speed drives, used DC motors as the work machine because the provision of the variable - frequency supply required to control the AC machine was complicated and uneconomic. However, the development of controllable power electronic switching devices has resulted in the development of a wide range of drives using both DC and AC induction motors. More recently, micro-processor - based digital control systems have replaced the analogue controllers, giving an increased sophistication of operation and facilitating the use of machines such as stepper motors and the switched reluctance motor.

In our project, we use a DC shunt motor with armature control. The armature voltage is controlled by the operation of the switching transistor SL100. The DC motor is coupled to the conveyor belt through a pulley.

3.8 Definition of a count:

The output of the pulse shaping circuit is interfaced to the programmable peripheral interface (PPI) (i.e) fed as input to the port A of the 8255 chip. At the initial stage when no

object is on the conveyor belt, the output of Port A will be 5V. When a object comes across the conveyor belt, at first the front end of the object will cross and hence the light rays from the optical source are obstructed from falling on the LDR and hence the output goes to '0' volt. At this instant $P_{A0} = 0$. The output stays at this level until the second end of the object just leaves the conveyor belt, the light rays from the optical source falls on LDR and hence the output switches back to 5 volt (i.e) $P_{A0} = 1$ and stays at that level until the next object arrives. Here, in our process of counting we are not worried about the size, length of the object. Even the smallest object will be detected by the sensor and hence counted as the light beam is focussed to a very thin beam. The count defined here is independent of the size and length and speed of the object.

4.1 General description:

The 8255 A is a programmable peripheral interface device designed for use in INTEL micro computer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the micro computer system BUS. The functional configuration of the 8255A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

DATA BUS TRANSFER:

The 3-state bidirectional 8 bit buffer is used to interface the 8255A to the system data bus. Data is transmitted by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

READ/WRITE CONTROL LOGIC:

The function of this block is to manage all the internal and external transfers. It accepts inputs from the CPU address

and control buses and in turn issues commands to both of the central groups. A and B.

4.2 PERIPHERAL INTERFACE SECTION:

Any microprocessor based system design involves interfacing of the processor with one or more peripheral device for the purpose of communication with the environment. A large numbers of general purpose and special purpose peripheral devices have been developed, most of them being single chip circuits. Their use reduces the chip count of the system and simplify the design process. They can be programmed to fit a variety of configurations. A few carefully chosen types of peripheral devices that are very relevant with regard to this project are discussed below.

The INTEL 8255A is a general purpose programmable I/O device designed for the use of the intel-up. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In the second mode, each group may be programmed to have 8 lines of input or output, of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation is a bidirectional bus mode which uses 8 lines for the bidirectional bus and 5 lines, borrowing one from the other group for handshaking.

CHIP SELECT ($\overline{CS}$):

A "low" on this input pin enables the communication between the 8255A and the CPU.

READ ($\overline{RD}$):

A "low" on this input pin enables the 8255A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255A.

WRITE ($\overline{WR}$):

A "low" on this input pin enables the CPU to write data or control words into the 8255A i.e (A_0 and A_1).

PORT SELECT 0 AND PORT SELECT 1:

These input signals in conjuction with RD and WR inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus i.e (A_0 and A_1).

RESET:

A "high" on this input clears the control register and all ports (A,B,C) are set the input mode.

GROUP A AND GROUP B CONTROLS:

The functional configuration of each port is programmed by system software. In essence the CPU outputs a control word to the 8255A. The control word contains information such "mode", "Bit set", "Bit Reset", etc. that initializes the functional configuration of the 8255A. Each of the control logic receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control group A ..... Port A and Port C UPPER (C_7-C_4)

Control group B ..... Port B and Port C LOWER (C_3-C_0)

The control word register can only be written into. No read operation of the control word register is allowed.

4.3 PORTS OF 8255:

Ports A, B and C:

The 8255A contains three 8 bit ports (A,B,C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255A.

PORT A:

One 8 bit data output latch/buffer and one 8 bit data input latch.

PORT B:

One 8 bit data input/output latch/buffer and one 8 bit data I/P buffer.

PORT C:

One 8 bit data output latch/buffer and one 8 bit data input buffer (no latch for input). This port can be divided into two 4 bit ports under the mode control. Each 4 bit port contains a 4 bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

4.4 8255A OPERATIONAL DESCRIPTION (Control word format for I/O mode):

MODE SELECTION:

There are three basic modes of operation that can be selected by the system software.

MODE 0 ..... Basic input/output.

MODE 1 ..... Strobed input/output.

MODE 2 ..... Bi-directional bus.

When the reset input goes "high" all ports will be set to the input mode. After the reset is removed the 8255A can remain in the input mode with no additional initialization required.

During the execution of the system program any of the other modes may be selected using a single output instruction. This allows a single 8255A to service a variety of peripheral devices with a simple software maintenance routine. In our project we make use of 8255A in basic input/output mode

PORT A ..... INPUT

PORT B ..... OUTPUT.

4.5 SIMPLE SOFTWARE MAINTENANCE ROUTINE:

The modes for Port A and Port B can be seperately defined, while Port C is divided into two portions as required by the Port A and Port B defined. All of the output registers, including the status Flip-Flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance, Group B can be programmed in Mode 0 to monitor simple switch closing or display computational results. Group A could be programmed in Mode 1 to monitor a key board or tape reader on an interrupt driver basis.

The design of the 8255A has taken into account things such as efficient PC board layout contro signal definition Vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic.

5.1 General Description of 8085A:

It is an 8 bit general purpose microprocessor. It has 16 line address bus and is capable of addressing 64K of memory. Its operating frequency is 3MHz (single phase clock). It has 40 pins and requires a power supply of + 5V. It is an enhanced version of 8080A. Its instruction set is upward compatible with that of 8080A.

ADDRESS AND DATA BUS:

The address bus consists of A_0 - A_{15} out of which A_{15} - A_8 is unidirectional. A_0 - A_7 is bidirectional as it is multiplexed for data and it is also the lower order bus.

CONTROL AND STATUS SIGNAL:

This signals are used to identify the nature of operation. They are

ADDRESS LATCH ENABLE (ALE):

This is a positive going pulse generated every time the 8085A begins an operation. It indicates that the bits on A_{D7}-A_{D0}

are address bits. This signal is used primarily to latch the low order address from the multiplexed bus and generate a seperate set of eight address line A_7-A_0.

READ ($\overline{RD}$):

This is a read control signal (active low). This signal indicates that the selected I/O or memory device is to be read and data are available on the data bus.

WRITE ($\overline{WR}$):

This is a write control signal (active low). This signal indicates that the data on the data bus are to be written into a selected memory or I/O location.

IO/$\overline{M}$:

This is a status signal used to differentiate between I/O and memory operations. When it is high, it indicates an I/O operation. When it is low, it indicates a memory operation. This signal is combined with RD and WR to generate I/O and memory control signals.

S1 and S0:

These status signals, similar to IO/M can identify various operations, but they are rarely used in small systems.

8085A MACHINE CYCLE, STATUS AND CONTROL SIGNALS

MACHINE CYCLE	IO/$\overline{M}$	STATUS		CONTROL SIGNALS
		S1	S0	
Opcode Fetch	0	1	1	$\overline{RD}$ = 0
Memory Read	0	1	0	$\overline{RD}$ = 0
Memory Write	0	0	1	$\overline{WR}$ = 0
I/O Read	1	1	0	$\overline{RD}$ = 0
I/O Write	1	0	1	$\overline{WR}$ = 0
INTR Acknowledge	1	1	1	$\overline{INTA}$ = 0
Halt	Z	0	0	$\overline{RD}$, $\overline{WR}$=Z $\overline{INTA}$ = 1
Hold	Z	X	X	-
Reset	Z	X	X	-

CLOCK FREQUENCY:

X1, X2 : Crystal is connected at these two pins. The frequency is internally divided by two ; therefore, to operate a system at 3MHz, the crystal should have a frequency of 6MHz.

5.2 INTERRUPTS AND EXTERNALLY INITIATED OPERATIONS:

The 8085 has got five interrupt signals that can be used to interrupt a program execution.

INTR INTERRUPT REQUEST:

This is used as a general purpose interrupt. The various types of interrupt requests are

RST 7.5

RST 6.5

RST 5.5

These are vectored interrupts and transfer the program control to specific memory location. Among these three the priority order is 7.5, 6.5 and 5.5.

TRAP:

This is a non-maskable interrupt and has got the highest priority.

HOLD:

This signal indicates that a peripheral such as a DMA controller is requesting the use of address and data buses.

$\overline{\text{DUTA}}$:

This is an output signal and is used to acknowledge the interrupt.

HLDA:

This signal acknowledges the hold request.

READY:

This is also on output signal. This signal is used to delay the microprocessor read or write cycles until a slow responding signal goes low, the microprocessor waits for an integral number of clock cycles until it goes high.

5.3 GENERATING CONTROL SIGNALS:

RD since this signal is used both for reading memory and for reading an input device, it is necessary to generate two different read signals one for memory and another for input. Similarly two seperate write signals must be generated.

Fig. 5.3 shows that four different control signals are generated by combining RD, WR and IO/M.

ALU:

The Arithmetic logic unit performs the computing functions, it includes the accumulator, the temporary register, the arithmetic and logic operations. The result is stored in the accumulator and flags are set or reset according to the result of operation. The descriptions and functions of the flags are as follows:

SIGN FLAG S:

After the execution of an arithmetic or logic operation if bit D_7 of the result is 1, the sign flag is set. This flag is used with signed numbers. In a given byte, if D_7 is 1, the number will be viewed as a negative number. If it is 0, the number will be considered as positive. In arithmetic operations with signal numbers, bit D_7 is reserved for indicating the sign and the remaining seven bits are used to represent the magnitude of a number.

AUXILLARY CARRY FLAG (AC):

In an arithmetic operation, when a carry is generated by digit D_3 and passed on to digit D_4, the AC flag is set. The flag is used only internally for BCD operations and is

not available for the programmer to change the sequence of a program with a jump instruction.

ZERO FLAG (Z):

The zero flag is set if the ALU operation results is 0, and the flag is reset if the result is not 0. This flag is modified by the results in the accumulator as well as in the other registers.

PARITY FLAG (P):

After an arithmetic or logic operation, if the result has an ever number of 1's, the flag is set. If it has an odd number of 1's, the flag is reset.

CARRY FLAG (CY):

If an arithmetic operation results in a carry the carry flag is set, otherwise it is reset.

EXECUTION:

The MPU places the memory address of the instruction on the address bus and it indicates the operation status on the status lines. MPU sends the MEMR signal to enable

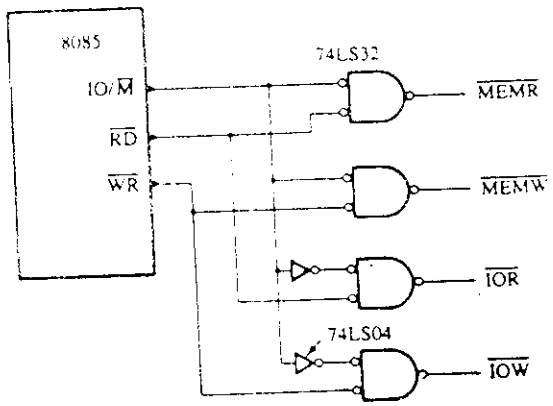


FIGURE 5-31
Schematic to Generate Read/Write Control Signals for Memory and I/O

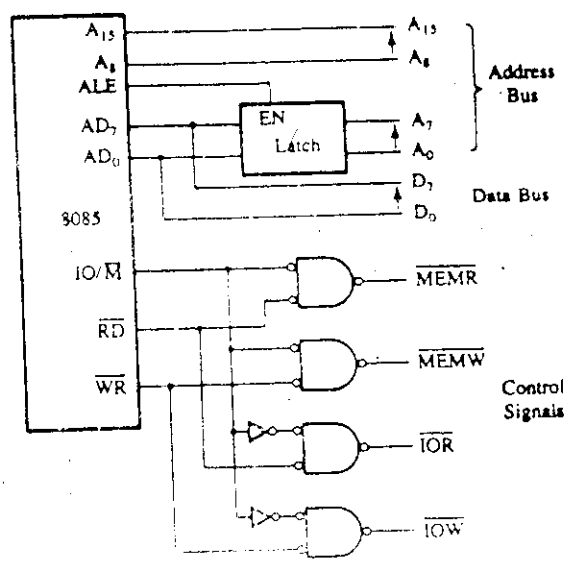


FIGURE 5-32
8085 Demultiplexed Address and Data Bus with Control Signals

the memory, fetches the instrucior byte and places it in the instruction decoder and also the MP. executes the instruction.

5.4 SINGLE CHIP 8 - BIT N-CHANNEL MICROPROCESSOR (8085A):

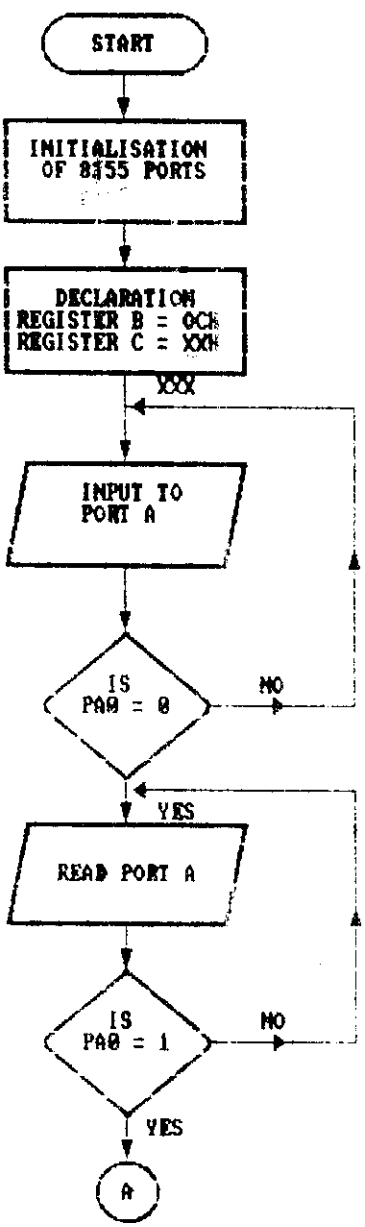
1. Single +5V power supply.
2. 100% software compatible with 8080A.
3. 1.3 micro sec. instruction cycle.
4. On chip clock generator (with external crystal, LC or RC Network).
5. On chip system controller, advanced cycle status information available for large system control.
6. Four vectored interrupt inputs (one is non-maskable) plus an 8080A compatible interrupt.
7. Serial In/serial out port.
8. Decimal, binary and double precision arithmetic.
9. Direct addressing capability to 64K bytes of memory.

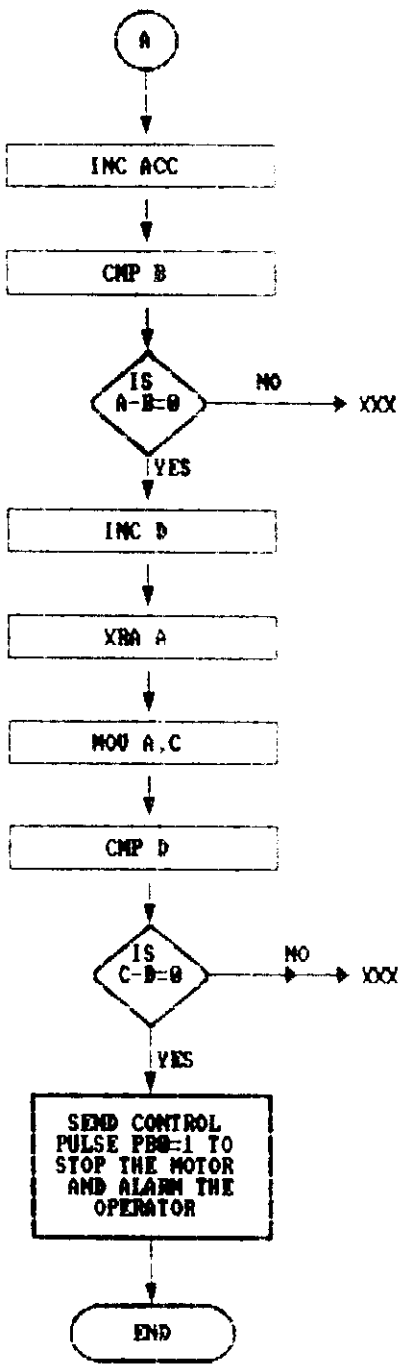
The 8085A is complete 8 bit parallel central processing unit (CPU). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's [8085A (CPU), 8156 (RAM/IO) and 8355/8755A (ROM/PROM/IO)] while maintaining total system expandability.

The 8085A incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A, thereby offering a high level of system integration.

The 8085A uses a multiplexed data bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of 8155/8156/8355/8755A memory products allow a direct interface with the 8085A.

6.1 System Flowchart




A
INC ACC
CMP B
IS A-B=0
NO
XXX
YES
INC D
XBA A
MOV A,C
CMP D
IS C-D=0
NO
XXX
YES
SEND CONTROL PULSE PB0=1 TO STOP THE MOTOR AND ALARM THE OPERATOR
END

6.2 Software Routine

ADDRESS	LABLE	MNEMONICS	OPCODE
8000		MVI A, 90	3E, 90
8002		OUT 43	D3,43
8004		MVI A, 00	3E, 0C
8006		OUT 41	D3, 41
8008		LXI H, 9002	21, 02, 90
800B		MOV C, M	4E
800C		DCX H	2B
800D	Loop 1	MOV B, M	46
800E	Loop 2	IN 40	DB, 40
8010		ANI 01	E6, 01
8012		JNZ Loop 2	C2, 0E, 80
8015	Loop 3	IN 40	DB, 40
8017		ANI 01	E6, 01
8019		JZ Loop 3	CA, 15, 80
801C		DCR B	05
801D		JNZ Loop 2	C2, 0E, 80
8020		DCR C	0D
8021		JNZ Loop 1	C2, 0D, 80
8024		MVI A, 01	3E, 01
8026		OUT 41	D3, 41
8027		LDA 9001	3A, 01, 90
802A		MOV D, A	57
802B		LXI H, 8400	21, 00, 84

ADDRESS	LABLE	MNEMONICS	OPCODE
802E		CALL 8500	CD, 00, 85
8031		CALL 8600	CD, 00, 86
8034		LDA 9002	3A, 02, 90
8037		MOV D, A	57
8038		LXI H, 8200	21, 00, 82
803B		CALL 8500	CD, 00, 85
803F		CALL 8600	CD, 00, 86
8041		JMP 8027	C3, 27, 80
8500		MVI C, 04	0E, 04
8502		MVI B, 80	06, 80
8504	Loop 1	MOV A, B	78
8506		OUT 31	D3, 31
8507		MOV A, M	7E
8508		OUT 30	D3, 30
850A		INX H	23
850B		INR B	04
850C		DCR C	0D
850D		JNZ Loop 1	C2, 04, 85
8510		MVI H, 83	26, 83
8512		MV A, 84	3E, 84
8514		OUT 31	D3, 31

ADDRESS	LABLE	MNEMONICS	OPCODES
8516		MOV A,D	7A
8517		ANI F0	E6, F0
8519		RRC	0F
851A		RRC	0F
851B		RRC	0F
851C		RRC	0F
851D		MOV L, A	6F
851E		MOV A, M	7E
851F		OUT 30	D3, 30
8521		MVI A, 85	3E, 85
8523		OUT 31	D3, 31
8525		MOV A, D	7A
8526		ANI 0F	E6, 0F
8528		MOV L, A	6F
8529		MOV A, M	7E
852A		OUT 30	D3, 30
852C		RET	C9
8600		MVI D, 08	16, 08
8602	Loop 2	LXI B, FFFF	01, FF, FF
8605	Loop 1	DCX B	0B
8606		MOV A, C	79
8607		ORA B	B0

ADDRESS	LABLE	MNEMONICS	OPCODES
8608		JNZ Loop 1	C2, 05, 86
860B		DCR D	15
860C		JNZ Loop 2	C2, 02, 86
860F		RET	C9
8300		0	F3
8301		1	60
8302		2	B5
8303		3	F4
8304		4	66
8305		5	D6
8306		6	D7
8307		7	70
8308		8	F7
8309		9	76
8400		0	00
8401		1	E5
8402		2	F3
8403		3	BD

ADDRESS	LABLE	MNEMONICS	OPCODES
8200		P	37
8201		1	6C
8202		C	93
8203		E.	9F

CHAPTER VII CONCLUSION

The versatile process monitoring system, used for industrial automation is the present trend involved in the despatching of the finished products. Although the hardware forms the principle section of our process, the microprocessor plays a vital role in controlling the entire process. We have interfaced our hardware with the microprocessor and carried out the process successfully. Moreover, by replacing the microprocessor, with a computer it is possible to provide assistance to solve both the long term and day to day operational problems faced by material planners, engineers, shop supervisors production planners and other responsible for the creation and transmission of information in the manufacturing environment.

CHAPTER VIII FUTURE DEVELOPMENTS

If this type of on line Processing system is to be adopted in large scale industries, then it would be better to interface with a CRT Monitor rather than a microprocessor. Here we can have a centralised Monitor which takes control of all the other monitors. The centralised monitor keeps an account of all the previous data and also that of the present ones.

This by doing so, the following implementations can be achieved

1. It covers a wide range of a company's activities with modules covering the marketing and sales functions by providing facilities for forecasting future sales, processing sales orders as they are received and analysing sales figures after the event.

2. If also covers the manufacturing side of a company's requirements by providing facilities for recording the movement of stock, planning the future replenishment of stock, planning shop floor capacity and controlling activity on the shop floor.

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1. Ramesh. S. Gaonkar - Microprocessor architecture. programming and applications with the 8085/8080 A. Wiley Eastern Ltd.

2. Microprocessors, Principles and Applications Mc Graw Hill International Edition.

3. Kenneth. L. Short - Microprocessors and programmed Logic, Prentice Hall.

4. Optics - John. M. Cleveland

5. Power Electronics - DA Bradley van Nostraud Reinhold Co. Ltd.

DUAL 4-INPUT SCHMITT TRIGGER

DESCRIPTION

The T54LS13/T74LS13 contains two 4-Input NAND Gates that accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, they have a greater noise margin than conventional NAND gates.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter that drives a TTL totem-pole output. The Schmitt trigger uses positive feedbak to effectively speed-up slow input transitions and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

B1
Plastic Package

D1/D2
Ceramic Package

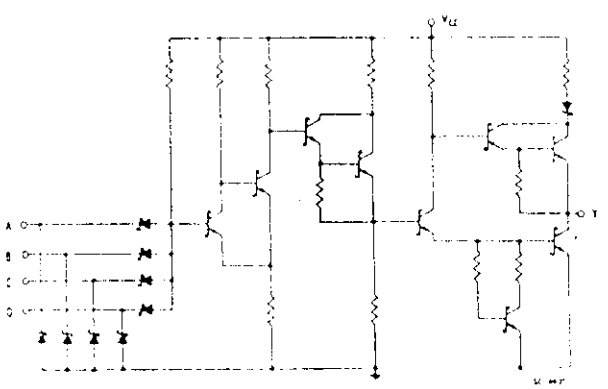
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

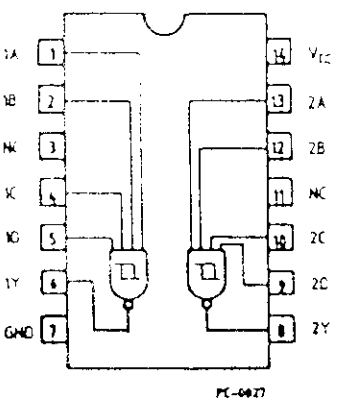
T54LS13 D2	T74LS13 C1
T74LS13 D1	T74LS13 M1
T74LS13 B1	

SCHEMATIC

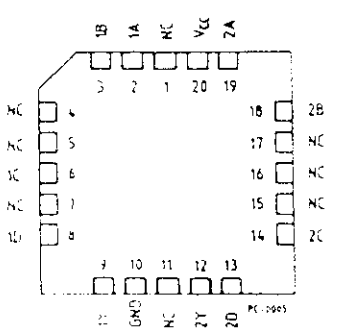


PIN CONNECTION
(top view)

DUAL IN LINE

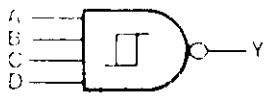


CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE



A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	- 0.5 to 7	V
V_I	Input Voltage, Applied to Input	- 0.5 to 15	V
V_O	Output Voltage, Applied to Output	- 0.6 to 5.5	V
I_I	Input Current, Into Inputs	- 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS13D2	4.5 V	5.0 V	5.5 V	- 55°C to + 125°C
T74LS13XX	4.75 V	5.0 V	5.25 V	0°C to + 70°C

XX = package type.

μA7800 Series
3-Terminal Positive Voltage Regulators

Description

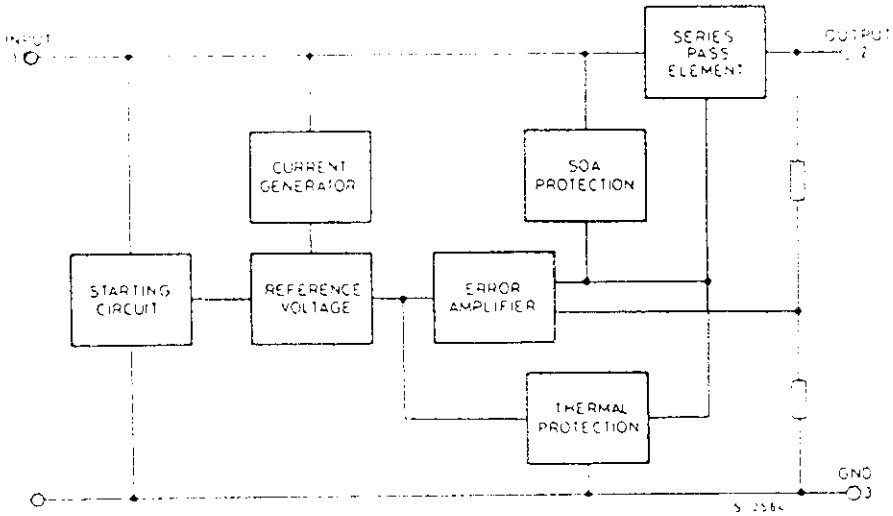
The μA7800 series of monolithic 3-terminal positive voltage regulators is constructed using the Fairchild Planar Epitaxial process. These regulators employ internal current-limiting, thermal shutdown and safe-area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1.0 A output current. They are intended as fixed voltage regulators in a wide range of applications including local (on-card) regulation for elimination of noise and distribution problems associated with single-point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents.

- Output Current In Excess Of 1.0 A
- No External Components
- Internal Thermal Overload Protection
- Internal Short Circuit Current-Limiting
- Output Transistor Safe-Area Compensation
- Available In JEDEC TO-220 And TO-3 Packages
- Output Voltages Of 5 V, 6 V, 8 V, 8.5 V, 12 V, 15 V, 18 V, And 24 V
- Available In Extended Temperature Range

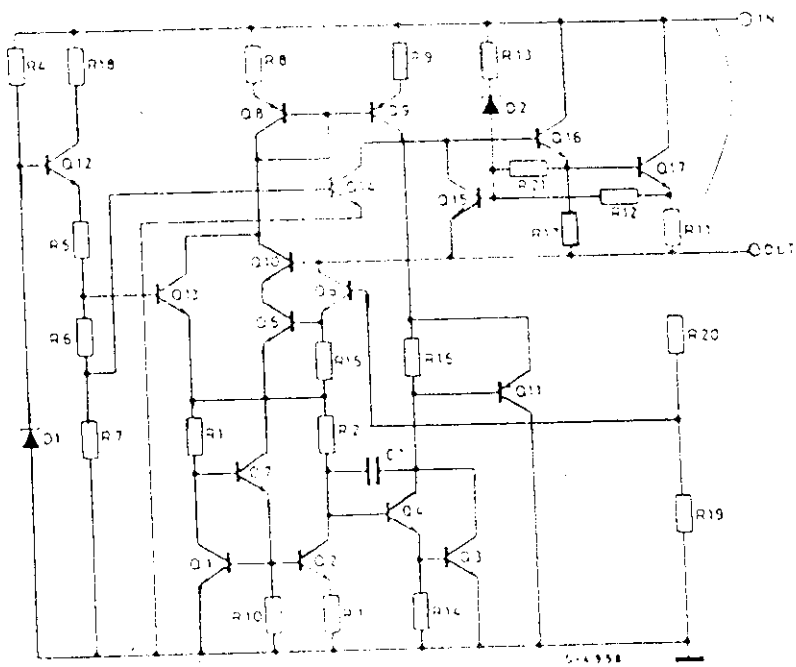
Absolute Maximum Ratings

Storage Temperature Range	
TO-3 Metal Can	−65°C to +175°C
TO-220 Package	−65°C to +150°C
Operating Junction Temperature Range	
Extended (μA7800M)	−55°C to +150°C
Commercial (μA7800C)	0°C to +150°C
Lead Temperature	
TO-3 Metal Can (soldering, 60 s)	300°C
TO-220 Package (soldering, 10 s)	265°C
Power Dissipation	Internally Limited
Input Voltage	
5.0 V to 18 V	35 V
24 V	40 V

BLOCK DIAGRAM

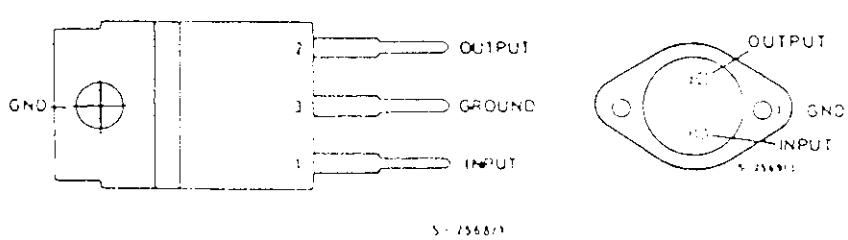


SCHEMATIC DIAGRAM



CONNECTION DIAGRAMS AND ORDERING NUMBERS

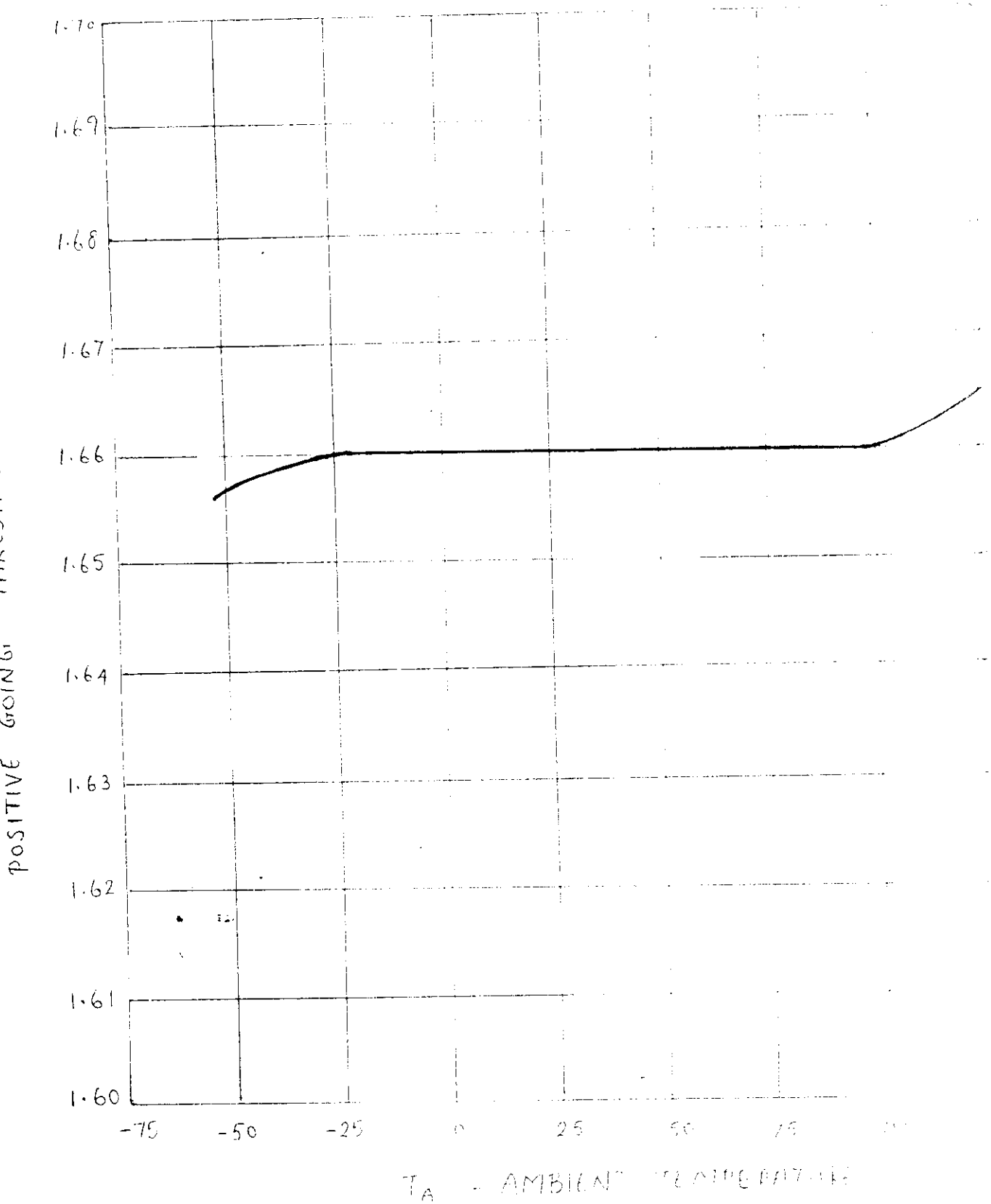
(top views)



POSITIVE GOING THRESHOLD VOLTAGE

VERSUS

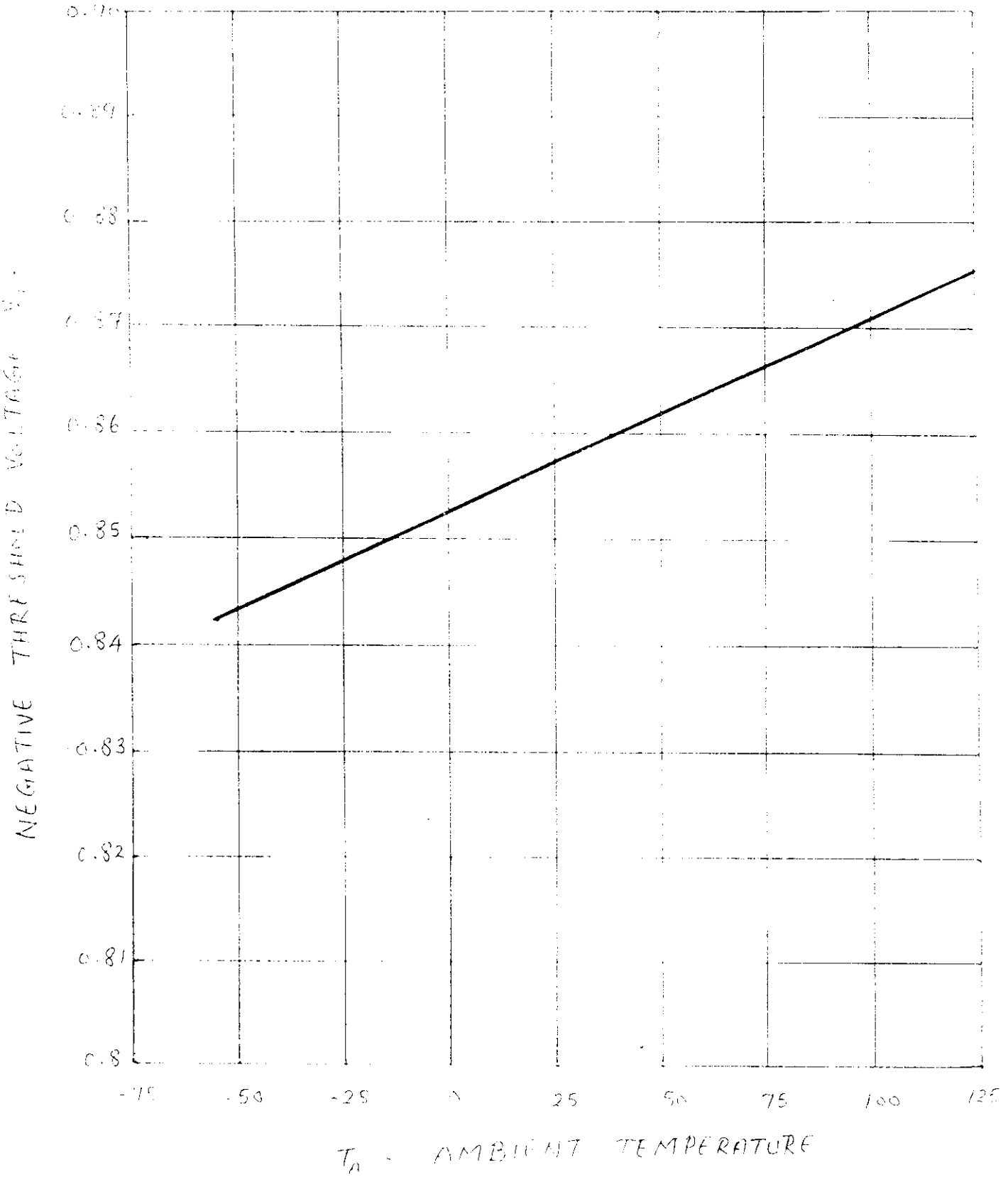
AMBIENT TEMPERATURE

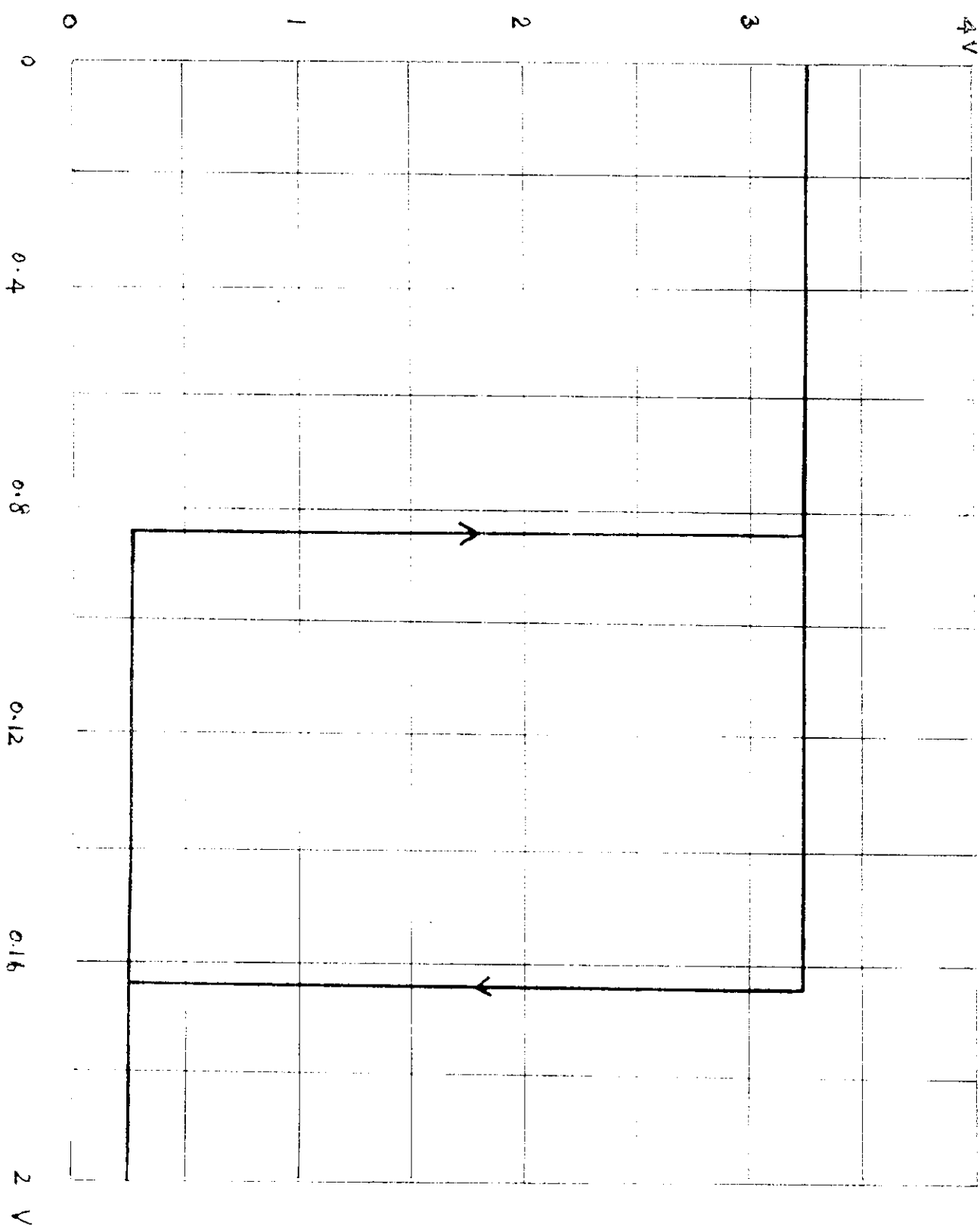


NEGATIVE GOING THRESHOLD VOLTAGE

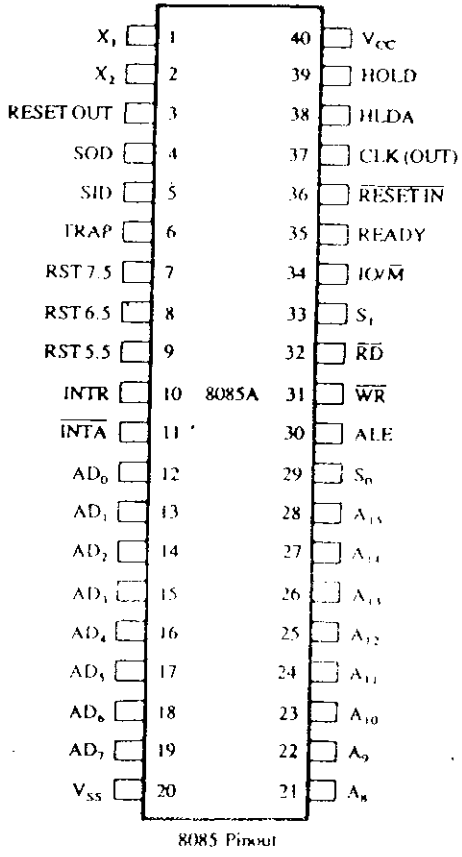
VERSUS

AMBIENT TEMPERATURE





OUTPUT VOLTAGE VERSUS INPUT VOLTAGE



8085 Pinout

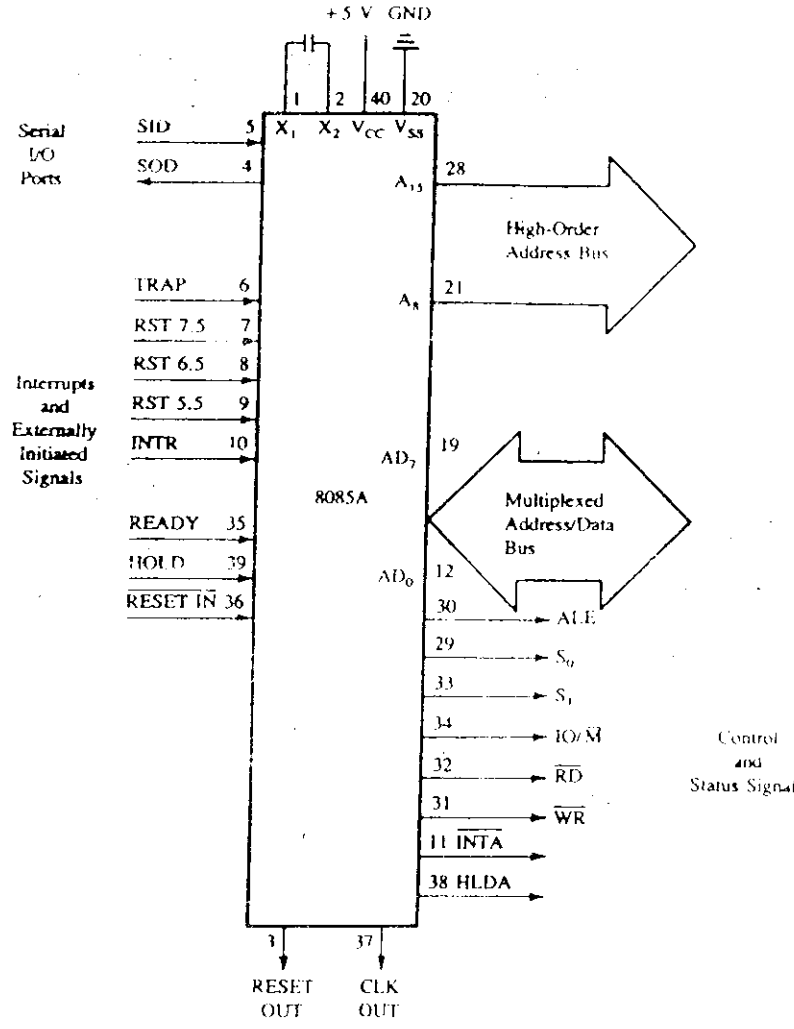


FIG. 8085A PINOUT AND SIGNALS

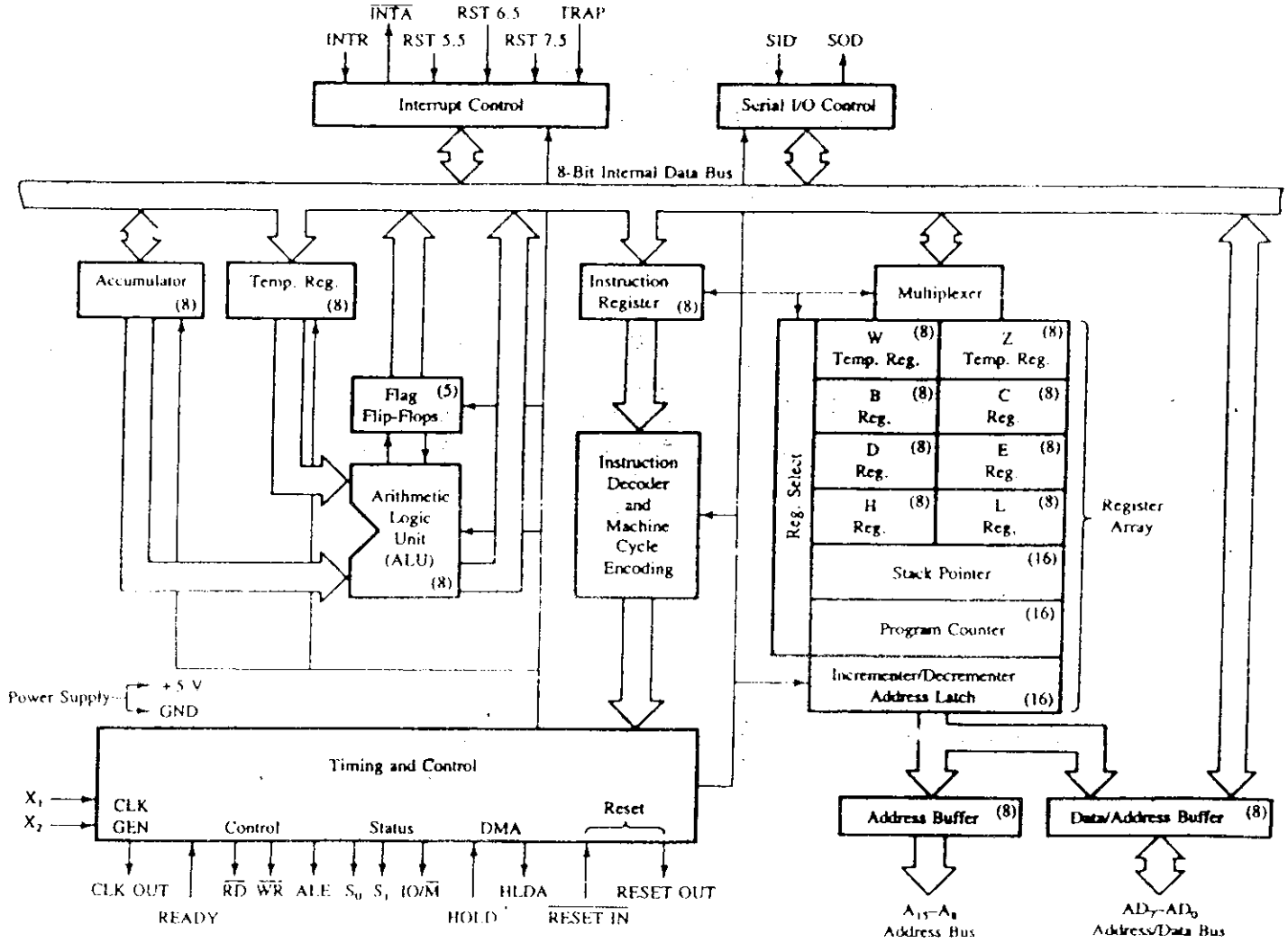
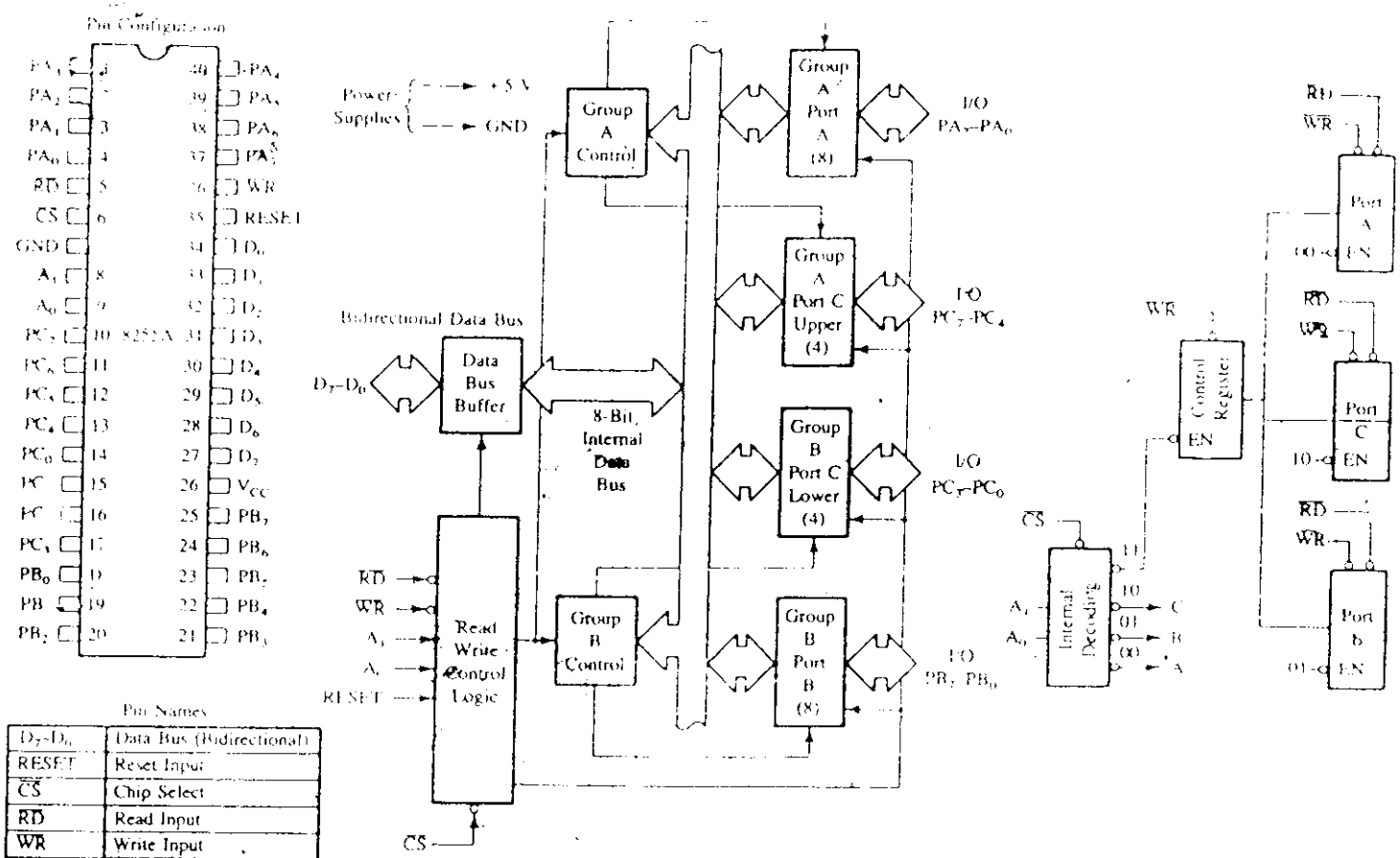


FIG. FUNCTIONAL BLOCKDIAGRAM OF 8085A



Pin Names	
D_7-D_0	Data Bus (Bidirectional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0, A_1	Port Address
PA_7-PA_0	Port A (Bit)
PB_7-PB_0	Port B (Bit)
PC_7-PC_0	Port C (Bit)
V_{CC}	+5 Volts
GND	0 Volts

FIG. PINOUT AND BLOCKDIAGRAM OF 8255A

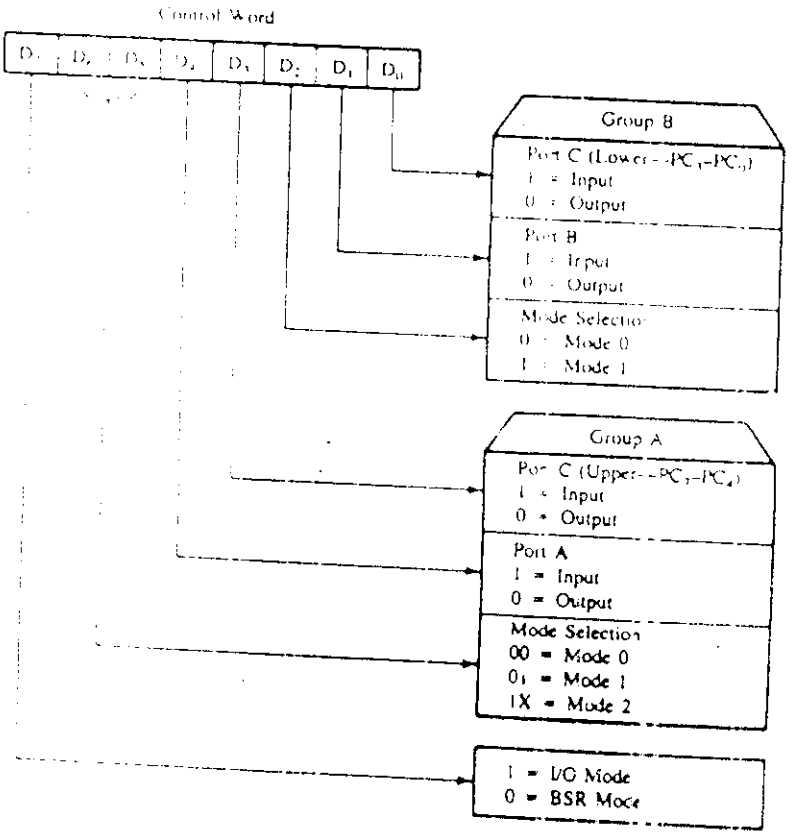
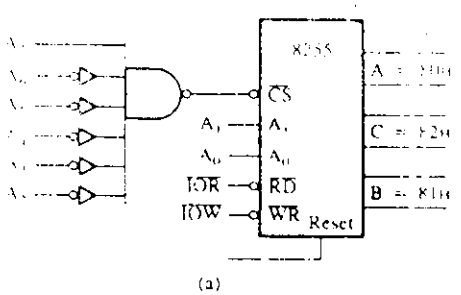


FIG. 8255A CONTROL WORD FORMAT FOR I/O MODE



CS		Hex Address	Port
A9 A8 A7 A6 A5 A4	A1 A0		
1 0 0 0 0 0	0 0	= 80H	A
	0 1	= 81H	B
	1 0	= 82H	C
	1 1	= 83H	Control Register

(b)

FIG. 8255A CHIP SELECT LOGIC

FIG. I/O PORT ADDRESSES