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HUMAN TRACKING USING GPS AND GSM

A Project Report

Submitted by

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BONAFIDE CERTIFICATE

Certified that this project report **"HUMAN TRACKING USING GPS AND GSM "** is the bonafide work of **"M.KAVIN, P.KEERTHI, R.KISHORE, A.NITHIYANAND"** Who carried out the project work under my supervision.

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To whomsoever it may concern

This is to certify that the students of final year ECE of Kumaraguru College of Technology, Coimbatore, TamilNadu, had undergone their final year project work in our esteemed organization successfully. Their project details are given below,

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Project Title : "Human Tracking Using GPS and GSM"

Duration : January - 2007 to April – 2007

Further to the company rules and regulations, source code is not permitted to be taken out of the premises.

During the project period, the students conduct and the performance were good.

For Sukra Telecom

Partner

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ABSTRACT

The project is to track the human or object using GPS and GSM. Global positioning system (GPS) is a satellite based navigation system made up of a network of 24 satellites placed into orbit by US DOD.GPS was originally intended for military applications , but now it is available for civilian use .This project "**HUMAN TRACKING USING GPS AND GSM"** uses a GPS receiver to calculate user's 3D position(Latitude, Longitude and Altitude). This information is then transmitted to the central station using GSM.

Many police, fire, and emergency medical service units use GPS receivers to determine the police car, fire truck, or ambulance nearest to an emergency. Hence GPS is used to calculate user's exact location with great fidelity.

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1. OVERVIEW OF THE PROJECT

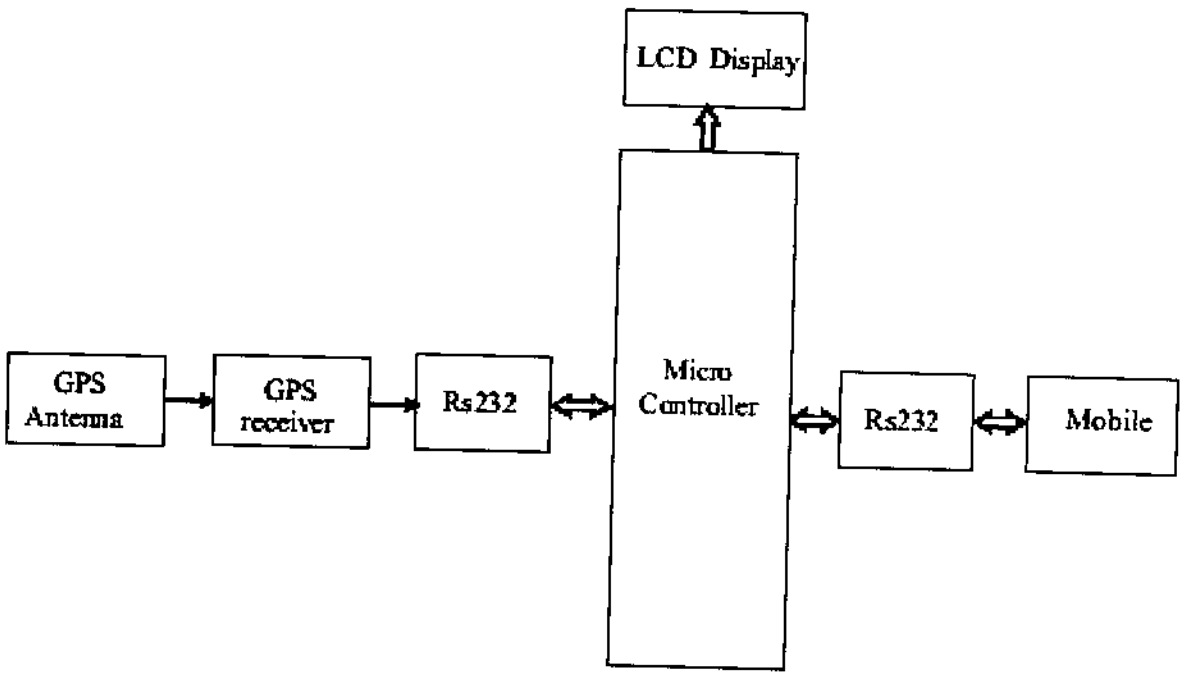
1.1 INTRODUCTION

The project is to track the object moving anywhere around the world using GPS and GSM. Global positioning system (GPS) is a satellite based navigation system. GPS was originally intended for military applications. Later on, it is made available for civilian use.

Now days, the most common mode of communication is through mobile, so the project makes tracking of human or object easily with the use of two mobiles. One is interfaced with the GPS kit which is present with the object to be traced and other is the central station.

The location of the object in terms of latitude, longitude & altitude is transmitted as a single Short Message Service (SMS) from the transmitted mobile interfaced with the GPS kit to the mobile at the central station at a regular interval automatically.

1.2 BLOCK DIAGRAM DESCRIPTION



GPS KIT (HAND CARRIED)

The GPS kit is a hand carried kit. The front end of the GPS kit consists of a GPS antenna which is a patch antenna (also called as microstrip antenna) and is used to receive signals from the GPS satellites. The satellites transmit signals that can be detected with a GPS receiver. GPS receiver processes the received signal and sends it to the microcontroller unit by means of a serial interface (RS232). The advantage of the microcontroller unit is that two interface is possible. The other serial interface is to the mobile in the GPS kit. The information (latitude, longitude, altitude, date and time) obtained from the GPS satellites can be seen through the LCD display of the GPS kit.These information are transmitted as SMS using GSM to the central station.

2. GLOBAL POSITIONING SYSTEM

2.1 GPS

The Global Positioning System (GPS) is a satellite-based navigation system made up of a network of 24 satellites placed into orbit by the U.S. Department of Defence. GPS was originally intended for military applications, but in the 1980s, the government made the system available for civilian use. GPS works in any weather conditions, anywhere in the world, 24 hours a day. There are no subscription fees or setup charges to use GPS.

The Global Positioning System (GPS) is a world wide radio-navigation system formed from a constellation of 24 satellites and their ground stations. GPS uses these "man made stars" as reference points to calculate positions accurate to a matter of meters. In fact, with advanced form of GPS measurements can be made to better than a centimeter! In a sense it's like giving every square meter on the planet unique address. GPS receivers have been miniaturized to just a few integrated circuits and so are becoming very economical. And that makes the technology accessible to virtually everyone. These days GPS is finding its way into cars, boats, planes, construction equipments, movie making gear, farm machinery, even laptop computers. Soon GPS will become almost as basic as the telephone.

GPS satellites circle the earth twice a day in a very precise orbit and transmit signal information to earth. GPS receivers take this information and use triangulation to calculate the user's exact location. Essentially, the GPS receiver compares the time a signal was transmitted by a satellite with the time it was received. The time difference tells the GPS receiver how far away the satellite is. Now, with distance measurements from a

few more satellites, the receiver can determine the user's position and display it on the unit's electronic map.

A GPS receiver must be locked on to the signal of at least three satellites to calculate a 2D position (latitude and longitude) and track movement. With four or more satellites in view, the receiver can determine the user's 3D position (latitude, longitude and altitude). Once the user's position has been determined, the GPS unit can calculate other information, such as speed, bearing, track, trip distance, distance to destination, sunrise and sunset time and more.

2.2 THE GPS SATELLITE SYSTEM

The 24 satellites that make up the GPS space segment are orbiting the earth about 12,000 miles above us. They are constantly moving, making two complete orbits in less than 24 hours. These satellites are travelling at speed of roughly 7,000 miles an hour.

GPS satellites are powered by solar energy. They have backup batteries onboard to keep them running in the event of a solar eclipse, when there's no solar power. Small rocket boosters on each satellite keep them flying in the correct path.

Here are some other interesting facts about the GPS satellites (also called NAVSTAR, the official U.S. Department of Defense name for GPS):

- The first GPS satellite was launched in 1978.
- A full constellation of 24 satellites was achieved in 1994.
- Each satellite is built to last about 10 years. Replacements are constantly being built and launched into orbit.

- A GPS satellite weighs approximately 2,000 pounds and is about 17 feet across with the solar panels extended.
- Transmitter power is only 50 watts or less.

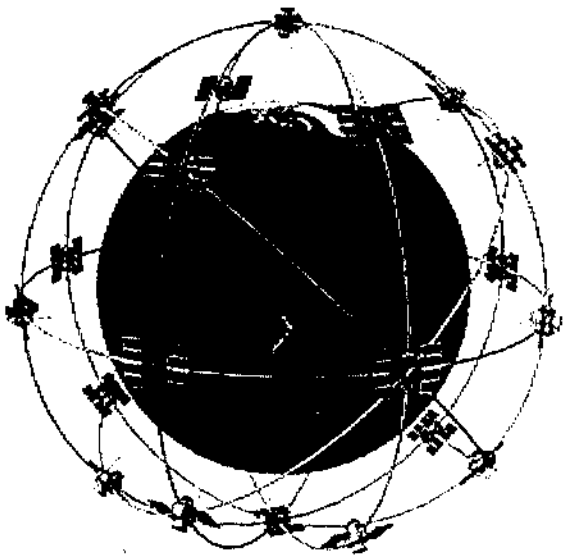


FIGURE 2.1 GPS SATELLITES

2.3 GPS SIGNAL

GPS satellites transmit two low power radio signals, designated L1 and L2. Civilian GPS uses the L1 frequency of 1575.42 MHz in the UHF band. The signals travel by line of sight, meaning they will pass through clouds, glass and plastic but will not go through most solid objects such as buildings and mountains.

A GPS signal contains three different bits of information : a pseudorandom code, ephemeris data and almanac data. The pseudorandom code is simply an I.D. code that identifies which satellite is transmitting information.

Ephemeris data tells the GPS receiver where each GPS satellite should be at any time throughout the day. Each satellite transmits

ephemeris data showing the orbital information for that satellite and for every other satellite in the system.

Almanac data, which is constantly transmitted by each satellite, contains important information about the status of the satellite (healthy or unhealthy), current date and time. This part of the signal is essential for determining a position.

2.4 SOURCES OF GPS SIGNAL ERRORS

Factors that can degrade the GPS signal and thus affect accuracy include the following:

- **Ionosphere and troposphere delays** — The satellite signal slows as it passes through the atmosphere. The GPS system uses a built-in model that calculates an average amount of delay to partially correct for this type of error.
- **Signal multipath** — This occurs when the GPS signal is reflected off objects such as tall buildings or large rock surfaces before it reaches the receiver. This increases the travel time of the signal, thereby causing errors.
- **Receiver clock errors** — A receiver's built-in clock is not as accurate as the atomic clocks onboard the GPS satellites. Therefore, it may have very slight timing errors.
- **Orbital errors** — Also known as ephemeris errors, these are inaccuracies of the satellite's reported location.
- **Number of satellites visible** — The more satellites a GPS receiver can "see," the better the accuracy. Buildings, terrain, electronic interference, or sometimes even dense foliage can block signal reception, causing position errors or possibly no position reading at

all. GPS units typically will not work indoors, underwater or underground.

- **Satellite geometry/shading** — This refers to the relative position of the satellites at any given time. Ideal satellite geometry exists when the satellites are located at wide angles relative to each other. Poor geometry results when the satellites are located in a line or in a tight grouping.
- **Intentional degradation of the satellite signal** — Selective Availability (SA) is an intentional degradation of the signal once imposed by the U.S. Department of Defense. SA was intended to prevent military adversaries from using the highly accurate GPS signals. The government turned off SA in May 2000, which significantly improved the accuracy of civilian GPS receivers.

3. GPS ANTENNA

GPS modules can either be operated with a passive or active antenna. Active antenna , with a built-in preamplifier (LNA: Low Noise Amplifier) are powered from the GPS module, the current being provided by the HF signal .For mobile navigational purposes combined antenna (e.g. GSM/FM and GPS) are supplied. Antenna receives right-handed circular polarized waves.

3.1 TYPES

Two types of antenna are obtainable on the market, Patch antenna and Helix antenna. Patch antenna is flat, generally have a ceramic and metallised body and are mounted on a metal base plate. In order to ensure a sufficiently high degree of selectivity, the base to patch surface ratio has to be adjusted. Patch antenna are often cast in a housing. Helix antenna is cylindrical in shape and have a higher gain than the Patch antenna.

FIGURE4.1 GPS ANTENNA

3.2 ACTIVE ANTENNA

The GLP1-RA model, Capsule Compact Active Antenna is a high performance 3.3V DC GPS antenna, this compact size active antenna is commonly used for OEM, system integrator and end user applications. The antenna offers a 27 dB gain (active patch). It features a "bottom exit" coaxial cable configuration with SMA, TNC or SMB connector. This

antenna performs well in foliage, urban and noisy environments. It is designed for fixed location, permanent mount applications and complies with automotive temperature and vibration standards

3.3 SPECIFICATIONS

Electrical

- Frequency: 1.575 GHz
- Output / VSWR: 2.0 Max
- Impedance: 50 D.
- Gain: 27 dB Typical
- Noise Figure: 1.2dB
- DC Voltage: DC 3.3V
- DC Current: 22 mA Typical

Environmental

- Working Temp: - 40°C - +8SoC
- Weatherproof: 100% waterproof

Mechanical

- Size: 60 mm Diam. X 22 mm
- Cable: RG 174 with 5 meter long
- Connector: SMA | TNC | SMB

Mounting: Permanent Mount

4. GPS RECEIVER

4.1 GENERAL DESCRIPTION

The uTracker02-LLP OEM GPS receiver board is based on the high performance iTrax02/8 GPS receiver architecture .The uTracker02-LLP is ideally suited for applications that require easy replacement for Trimble Lassen LP and where the state of the art GPS performance including fast TTFF even in extreme temperature is required.

The uTracker02-LLP offers user configurable, low power consumption with three different operational modes. Full navigation, Idle mode and Sleep mode can be customized to perfectly meet the requirements of each specific GPS application. The uTracker02-LLP performance regarding sensitivity and very fast TTFF makes it applicable even for extremely demanding applications and environments with full industrial temperature range.

4.2 FUNCTIONALITY AND I/O 'S

The uTracker02-LLP supports the basic GPS functionality plus support for versatile control for sleep state and even the Data logger to Store position information to the internal non-volatile flash memory.

The 2x4 pin header connector with 2.0 mm pitch includes two serial ports, one with TX & RX , the other with Rx only. NMEA and iTalk protocols are supported with standard firmware. The I/O includes also power supply, ground, accurate 1 PPS output for timing applications and Power Mode Control input. Nominal power supply is +3.3V and typical current consumption is 52mA.

All navigational data is stored in non-volatile 8 Mbit Flash memory meaning that no external back -up battery is required.

4.3 ANTENNA CONNECTOR

The antenna connector is a MCX jack , which provides also the active antenna bias supply. The module supports optionally the Antenna Bias Supervisor , which detects a faulty condition, either Open or Short and sends a respective message to the host.

4.4 FEATURES

- Low power consumption – 52mA typical
- Sensitivity – 152 dBm (Tracking)
- Data Logger
- Option for Antenna Bias Supervisor
- Power supply,+3.3 V nominal.

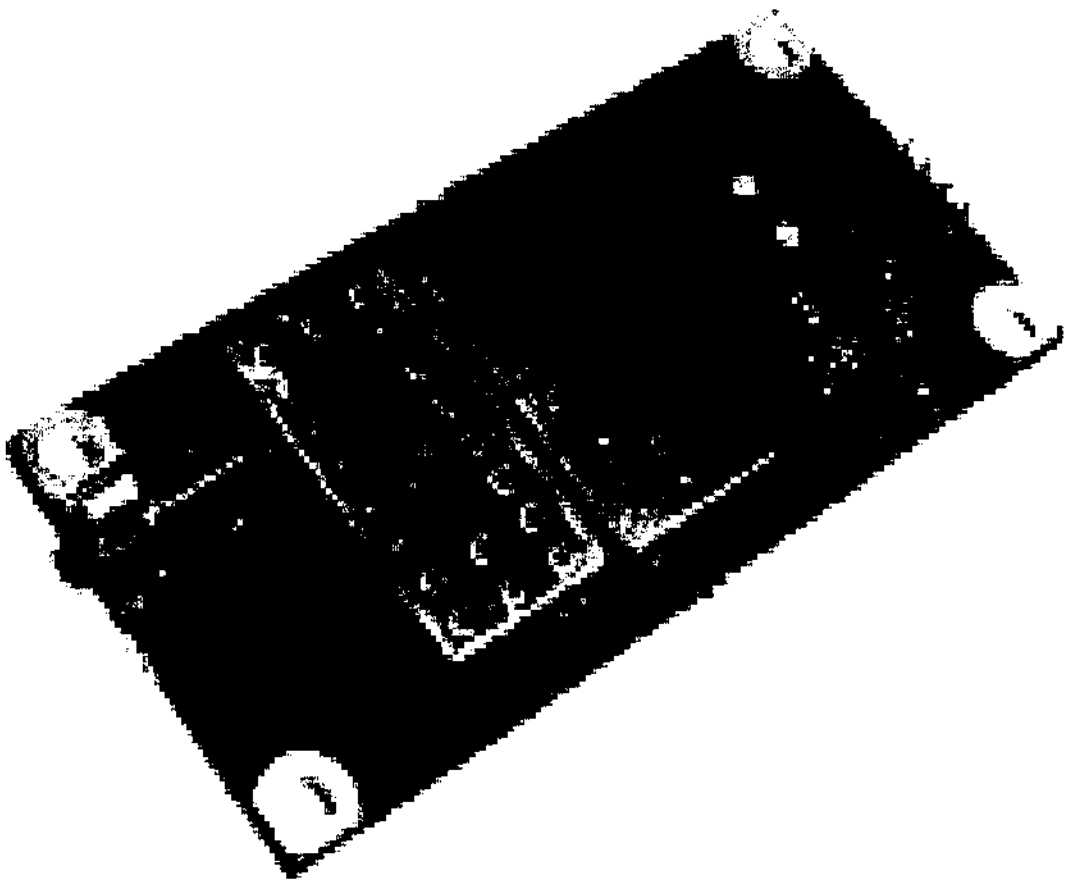


FIGURE 4.1 GPS RECEIVER

5. RENESAS

5.1 OVERVIEW

This MicroControllerUnit(MCU) is built using the high-performance silicon gate CMOS process using a R8C/Tiny Series CPU core and is packaged in a 32-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, it is capable of executing instructions at high speed. The data flash ROM (2 KB X 2 blocks) is embedded.

5.2 CENTRAL PROCESSING UNIT

The CPU contains 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. Two sets of register banks are provided.

Data Registers (R0, R1, R2 and R3)

R0 is a 16-bit register for transfer, arithmetic and logic operations. The same applies to R1 to R3. The R0 can be split into high-order bit (R0H) and low-order bit (R0L) to be used separately as 8-bit data registers.

The same applies to R1H and R1L as R0H and R0L. R2 can be combined with R0 to be used as a 32-bit data register (R2R0). The same applies to R3R1 as R2R0.

Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. They also are used for transfer, arithmetic and logic operations. The same applies to A1 as A0. A0 can be combined with A0 to be used as a 32-bit address register (A1A0).

Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

Interrupt Table Register (INTB)

INTB is a 20-bit register indicates the start address of an interrupt vector table.

Program Counter (PC)

PC, 20 bits wide, indicates the address of an instruction to be executed.

User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointer (SP), USP and ISP, are 16 bits wide each.

The U flag of FLG is used to switch between USP and ISP.

Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

Flag Register (FLG)

FLG is a 11-bit register indicating the CPU state.

Carry Flag (C)

The C flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic logic unit.

Debug Flag (D)

The D flag is for debug only. Set to "0".

Zero Flag (Z)

The Z flag is set to "1" when an arithmetic operation resulted in 0; otherwise, "0".

Sign Flag (S)

The S flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, "0".

Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is "0". The register bank 1 is selected when this flag is set to "1".

Overflow Flag (O)

The O flag is set to "1" when the operation resulted in an overflow; otherwise, "0".

Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.

An interrupt is disabled when the I flag is set to "0", and are enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt request is acknowledged.

Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0", USP is selected when the U flag is set to "1".

The U flag is set to "0" when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has greater priority than IPL, the interrupt is enabled.

Reserved Bit

When write to this bit, set to "0". When read, its content is indeterminate.

5.3 MEMORY

This MCU provides 1-Mbyte address space from addresses 0000016 to FFFFF16.The internal ROM (program ROM) is allocated lower addresses beginning with address 0FFFF16. For example, a 16-Kbyte internal ROM is allocated addresses from 0C00016 to 0FFFF16.

The fixed interrupt vector table is allocated addresses 0FFDC16 to 0FFFF16. They store the starting address of each interrupt routine.

The internal ROM (data flash) is allocated addresses from 0200016 to 02FFF16.The internal RAM is allocated higher addresses beginning with address 0040016. For example, a 1-Kbyteinternal RAM is allocated addresses 0040016 to 007FF16. The internal RAM is used not only for storing data, but for calling subroutines and stacks when interrupt request is acknowledged. Special function registers (SFR) are allocated addresses 0000016 to 002FF16. The peripheral function control registers are located them. All addresses, which have nothing allocated within the SFR, are reserved area and cannot be accessed by users.

6. RS 232(SERIAL INTERFACE)

Modems and other devices used to send serial data are often referred to as DATA CIRCUIT-TERMINATING EQUIPMENT (DCE). The terminals or computers that are sending or receiving the data are referred to as DATA TERMINAL EQUIPMENT (DTE). In response to the need for signal and handshake standards between DTE and DCE, the Electronic Industries Association (EIA) developed EIA standard RS-232C. This standard describes the functions of 25 signal and handshake pins for serial data transfer. It also describes the voltage levels. Impedance levels, rise and fall times, maximum bit rate, and maximum capacitance for these signal lines.

6.1 INTERFACING DEVICES TO RS-232 PORTS

RS-232 waveforms

RS-232 communication is asynchronous. That is a clock signal is not sent with the data. Each word is synchronized using it's start bit, and an internal clock on each side, keeps tabs on the timing.

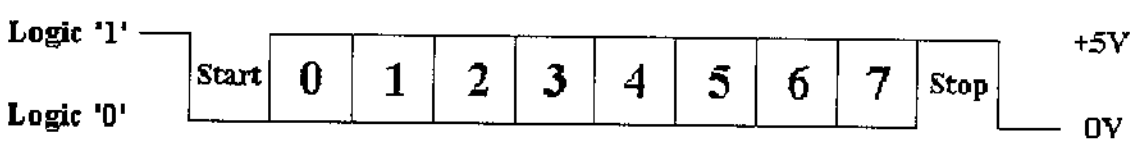


FIGURE6.1 TTL/CMOS SERIAL LOGIC WAVEFORM

The diagram above, shows the expected waveform from the UART when using the common 8N1 format. 8N1 signifies 8 Data bits, No Parity and 1 Stop Bit. The RS-232 line, when idle is in the Mark State (Logic 1). A transmission starts

with a start bit which is (Logic 0). Then each bit is sent down the line, one at a time. The LSB (Least Significant Bit) is sent first.

A Stop Bit (Logic 1) is then appended to the signal to make up the transmission.The diagram, shows the next bit after the Stop Bit to be Logic 0. This must mean another word is following, and this is it's Start Bit. If there is no more data coming then the receive line will stay in it's idle state(logic 1). We have encountered something called a "Break" Signal. This is when the data line is held in a Logic 0 state for a time long enough to send an entire word. Therefore if you don't put the line back into an idle state, then the receiving end will interpret this as a break signal.

The data sent using this method, is said to be framed. That is the data is framed between a Start and Stop Bit. Should the Stop Bit be received as a Logic 0, then a framing error will occur. This is common, when both sides are communicating at different speeds. The above diagram is only relevant for the signal immediately at the UART. RS-232 logic levels uses +3 to +25 volts to signify a "Space" (Logic 0) and -3 to -25 volts for a "Mark" (logic 1).

Any voltage in between these regions (ie between +3 and -3 Volts) is undefined. Therefore this signal is put through a "RS-232 Level Converter". This is the signal present on the RS-232 Port of your computer, shown below.

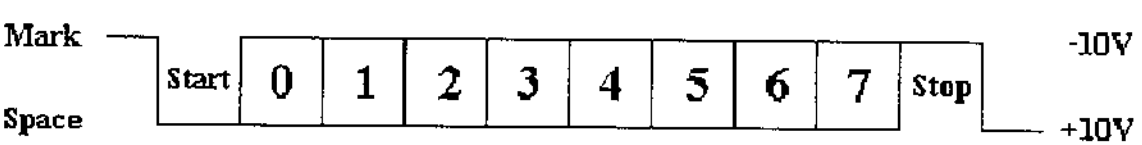


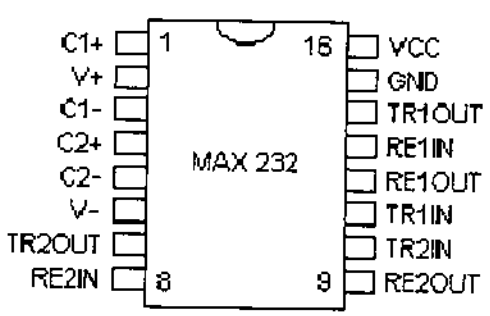
FIGURE 6.2 RS-232 LOGIC WAVEFORM

The above waveform applies to the Transmit and Receive lines on the RS-232 port. These lines carry serial data, hence the name Serial Port. There are other lines on the RS-232 port which, in essence are Parallel lines. These lines (RTS, CTS, DCD, DSR, DTR, RTS and RI) are also at RS-232 Logic Levels.

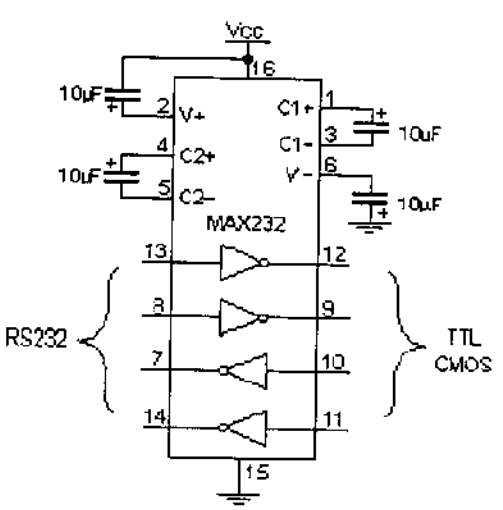
6.2 RS-232 LEVEL CONVERTERS

Almost all digital devices which we use require either TTL or CMOS logic levels. Therefore the first step to connecting a device to the RS-232 port is to transform the RS-232 levels back into 0 and 5 Volts. As we have already covered, this is done by RS-232 Level Converters.

Two common RS-232 Level Converters are the 1488 RS-232 Driver and the 1489 RS-232 Receiver. Each package contains 4 inverters of the one type, either Drivers or Receivers. The driver requires two supply rails, +7.5 to +15v and -7.5 to -15V. As you could imagine this may pose a problem in many instances where only a single supply of +5V is present.



Pinouts for the MAX-232, RS-232 Driver/Receiver.



Typical MAX-232 Circuit.

FIGURE 6.3 MAX 232

Another device is the MAX-232. It includes a Charge Pump, which generates +10V and -10V from a single 5V supply. This IC also includes two receivers and two transmitters in the same package.

This is handy in many cases when you only want to use the Transmit and Receive data Lines. You don't need to use two chips, one for the receive line and one for the transmit. However all this convenience comes at a price, but compared with the price of designing a new power supply it is very cheap. There are also many variations of these devices. The large value of capacitors are not only bulky, but also expensive. Therefore other devices are available which use smaller capacitors and even some with inbuilt capacitors. (Note : Some MAX-232's can use 1 micro farad Capacitors)

7. LCD DISPLAY

7.1 INTRODUCTION

Liquid crystal displays (LCDs) have materials which combine the properties of both liquids and crystals. Rather than having a melting point, they have a temperature range within which the molecules are almost as mobile as they would be in a liquid, but are grouped together in an ordered form similar to a crystal.

The LCD's are lightweight with only a few millimeters thickness. Since the LCD's consume less power, they are compatible with low power electronic circuits, and can be powered for long durations.

The LCD's don't generate light and so light is needed to read the display. By using backlighting, reading is possible in the dark. The LCD's have long life and a wide operating temperature range.

Changing the display size or the layout size is relatively simple which makes the LCD's more customer friendly.

The LCDs used exclusively in watches, calculators and measuring instruments are the simple seven-segment displays, having a limited amount of numeric data. The recent advances in technology have resulted in better legibility, more information displaying capability and a wider temperature range. These have resulted in the LCDs being extensively used in telecommunications and entertainment electronics. The LCDs have even started replacing the cathode ray tubes (CRTs) used for the display of text and graphics, and also in small TV applications.

7.2 POWERSUPPLY

The power supply should be of +5V, with maximum allowable transients of 10mv. To achieve a better / suitable contrast for the display, the voltage (VL) at pin 3 should be adjusted properly.

A module should not be inserted or removed from a live circuit. The ground terminal of the power supply must be isolated properly so that no voltage is induced in it. The module should be isolated from the other circuits, so that stray voltages are not induced, which could cause a flickering display.

7.3 HARDWARE

Develop a uniquely decoded 'E' strobe pulse, active high, to accompany each module transaction. Address or control lines can be assigned to drive the RS and R/W inputs.

Utilize the Host's extended timing mode, if available, when transacting with the module. Use instructions, which prolong the Read and Write or other appropriate data strobes, so as to realize the interface timing requirements.

If a parallel port is used to drive the RS, R/W and 'E' control lines, setting the 'E' bit simultaneously with RS and R/W would violate the module's set up time. A separate instruction should be used to achieve proper interfacing timing requirements.

7.4 MOUNTING

Cover the display surface with a transparent protective plate, to protect the polarizer.

Don't touch the display surface with bare hands or any hard materials. This will stain the display area and degrade the insulation between terminals.

Do not use organic solvents to clean the display panel as these may adversely affect tape or with absorbant cotton and petroleum benzene.

The processing or even a slight deformation of the claws of the metal frame will have effect on the connection of the output signal and cause an abnormal display.

Do not damage or modify the pattern wiring, or drill attachment holes in the PCB. When assembling the module into another equipment, the space between the module and the fitting plate should have enough height, to avoid causing stress to the module surface.

Make sure that there is enough space behind the module, to dissipate the heat generated by the ICs while functioning for longer durations.

When an electrically powered screwdriver is used to install the module, ground it properly.

While cleaning by a vacuum cleaner, do not bring the sucking mouth near the module. Static electricity of the electrically powered driver or the vacuum cleaner may destroy the module.

7.5 ENVIRONMENTAL PRECAUTIONS

Operate the LCD module under the relative condition of 40°C and 50% relative humidity. Lower temperature can cause retardation of the blinking speed of the display, while higher temperature makes the overall display discolor.

When the temperature gets to be within the normal limits, the display will be normal. Polarization degradation, bubble generation or polarizer peel-off may occur with high temperature and humidity.

Contact with water or oil over a long period of time may cause deformation or colour fading of the display. Condensation on the terminals can cause electro-chemical reaction disrupting the terminal circuit.

7.6 TROUBLE SHOOTING

When the power supply is given to the module, with the pin 3 (VL) connected to ground, all the pixels of a character gets activated in the following manner:

All the characters of a single line display, as in CDM 16108.

The first eight characters of a single line display, operated in the two-line display mode, as in CDM 16116.

The first line of characters of a two-line display as in CDM 16216 and 40216. The first and third line of characters of a four-line display operated in the two-line display mode, as in CDM 20416.

If the above mentioned does not occur, the module should be initialized by software.

Make sure that the control signals 'E' , R/W and RS are according to the interface timing requirements.

7.7 IMPROPER CHARACTER DISPLAY

When the characters to be displayed are missing between, the data read/write is too fast. A slower interfacing frequency would rectify the problem.

When uncertainty is there in the start of the first characters other than the specified ones are rewritten, check the initialization and the software routine.

In a multi-line display, if the display of characters in the subsequent lines does'nt take place properly, check the DD RAM addresses set for the corresponding display lines.

When it is unable to display data, even though it is present in the DD RAM, either the display on/off flag is in the off state or the display shift function is not set properly. When the display shift is done simultaneous with the data writa operation, the data may not be visible on the display.

If a character not found in the font table is displayed, or a character is missing, the CG ROM is faulty and the controller IC have to be changed

If particular pixels of the characters are missing, or not getting activated properly, there could be an assembling problem in the module.

In case any other problems are encountered you could send the module to our factory for testing and evaluation.

7.8 CRYSTALONICS DISPLAY

Crystalonics dot –matrix (alphanumeric) liquid crystal displays are available in TN, STN types, with or without backlight. The use of C-MOS LCD controller and driver ICs result in low power consumption. These modules can be interfaced with a 4-bit or 8-bit micro processor /Micro controller.

The built-in controller IC has the following features:

- Correspond to high speed MPU interface (2MHz)
- 80 x 8 bit display RAM (80 Characters max)
- 9,920 bit character generator ROM for a total of 240 character fonts. 208 character fonts (5 x 8 dots) 32 character fonts (5 x 10 dots)

- 64 x 8 bit character generator RAM 8 character generator RAM 8 character fonts (5 x 8 dots) 4 characters fonts (5 x 10 dots)
- Programmable duty cycles
- 1/8 – for one line of 5 x 8 dots with cursor
- 1/11 – for one line of 5 x 10 dots with cursor
- 1/16 – for one line of 5 x 8 dots with cursor
- Wide range of instruction functions display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift.
- Automatic reset circuit, that initializes the controller / driver ICs after power on.

FUNCTIONAL DESCRIPTION OF THE CONTROLLER IC

REGISTERS:

The controller IC has two 8 bit registers, an instruction register (IR) and a data register (DR). The IR stores the instruction codes and address information for display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can be written, but not read by the MPU.

The DR temporally stores data to be written to /read from the DD RAM or CG RAM. The data written to DR by the MPU, is automatically written to the DD RAM or CG RAM as an internal operation.

When an address code is written to IR, the data is automatically transferred from the DD RAM or CG RAM to the DR. data transfer between the MPU is then completed when the MPU reads the DR. likewise, for the next MPU read of the DR, data in DD RAM or CG RAM at the address is sent to the DR automatically. Similarly, for the

MPU write of the DR, the next DD RAM or CG RAM address is selected for the write operation.

The register selection table is as Shown in TABLE 7.1.

RS	R/W	OPERATION
0	0	IR write as an internal operation
0	1	Read busy flag (DB7) and address counter (DB0 to DB6)
1	0	DR write as an internal operation (DR to DD RAM or CG RAM)
1	1	DR read as an internal operation (DD RAM or CG RAM to DR)

TABLE 7.1 REGISTER SELECTION AND THEIR OPERATIONS

7.9 BUSY FLAG:

When the busy flag is1, the controller is in the internal operation mode, and the next instruction will not be accepted.

When RS = 0 and R/W = 1, the busy flag is output to DB7.

The next instruction must be written after ensuring that the busy flag is 0.

7.10 ADDRESS COUNTER:

The address counter allocates the address for the DD RAM and CG RAM read/write operation when the instruction code for DD RAM address or CG RAM address setting, is input to IR, the address code is transferred from IR to the address counter. After writing/reading the display data to/from the DD RAM or CG RAM, the address counter

increments/decrements by one the address, as an internal operation. The data of the address counter is output to DB0 to DB6 while R/W = 1 and RS = 0.

The characters to be displayed are written into the display data RAM (DD RAM), in the form of 8 bit character codes present in the character font table. The extended capacity of the DD RAM is 80 x 8 bits i.e. 80 characters.

The character generator ROM generates 5 x 8 dot 5 x 10 dot character patterns from 8 bit character codes. It generates 208, 5 x 8 dot character patterns and 32, 5 x 10 dot character patterns.

In the character generator RAM, the user can rewrite character patterns by program. For 5 x 8 dots, eight character patterns can be written, and for 5 x 10 dots, four character patterns can be written.

7.11 INTERFACING THE MICROPROCESSOR / CONTROLLER:

The module, interfaced to the system, can be treated as RAM input/output, expanded or parallel I/O.

Since there is no conventional chip select signal, developing a strobe signal for the enable signal (E) and applying appropriate signals to the register select (RS) and read/write (R/W) signals are important.

The module is selected by gating a decoded module – address with the host – processor's read/write strobe. The resultant signal, applied to the LCDs enable (E) input, clocks in the data.

The 'E' signal must be a positive going digital strobe, which is active while data and control information are stable and true. The falling edge of the enable signal enables the data / instruction register of the controller. All module timings are referenced to specific edges of the 'E' signal. The 'E' signal is applied only when a specific module transaction is desired.

The read and write strobes of the host, which provides the 'E' signals, should not be linked to the module's R/W line. An address bit which sets up earlier in the host's machine cycle can be used as R/W.
When the host processor is so fast that the strobes are too narrow to serve as the 'E' pulse

a. Prolong these pulses by using the hosts 'Ready' input
b. Prolong the host by adding wait states
c. Decrease the Hosts Crystal frequency.

Inspite of doing the above mentioned, if the problem continues, latch both the data and control information and then activate the 'E' signal
When the controller is performing an internal operation he busy flag (BF) will set and will not accept any instruction. The user should check the busy flag or should provide a delay of approximately 2ms after each instruction.

The module presents no difficulties while interfacing slower MPUs.The liquid crystal display module can be interfaced, either to 4-bit or 8-bit MPUs.

For 4-bit data interface, the bus lines DB4 to DB7 are used for data transfer, while DB0 to DB3 lines are disabled. The data transfer is complete when the 4-bit data has been transferred twice. The busy flag must be checked after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.For 8-bit data interface, all eight-bus lines (DB0 to DB7) are used.

8. POWER SUPPLY

8.1 INTRODUCTION

The present chapter introduces the operation of power supply circuits built using rectifiers, filters, and then voltage regulators. Starting with an ac voltage, a steady dc voltage is obtained by rectifying the ac voltage, then filtering to a dc level, and finally, regulating to obtain a desired fixed dc voltage. The regulation is usually obtained from an IC voltage regulator unit, which takes a dc voltage and provides a somewhat lower dc voltage, which remains the same even if the input dc voltage varies, or the output load connected to the dc voltage changes.

A block diagram containing the parts of a typical power supply and the voltage at various points in the unit is shown in fig 8.1. The ac voltage, typically 120V rms , is connected to a transformer, which steps that ac voltage down to the level for the desired dc output. A diode rectifier then provides a full-wave rectified voltage that is initially filtered by a simple capacitor filter to produce a dc voltage. This resulting dc voltage usually has some ripple or ac voltage variation. A regulator circuit can use this dc input to provide a dc voltage that not only has much less ripple voltage but also remains the same dc value even if the input dc voltage varies somewhat, or the load connected to the output dc voltage changes. This voltage regulation is usually obtained using one of a number of popular voltage regulator IC units.

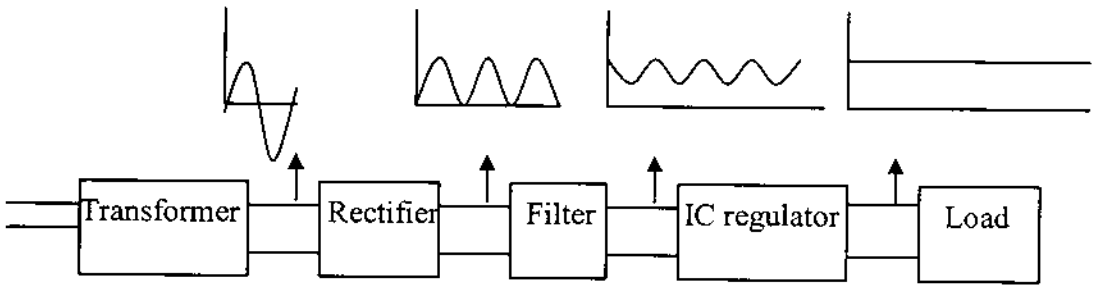


FIGURE 3

8.1 POWER SUPPLY

8.2 IC VOLTAGE REGULATORS:

Voltage regulators comprise a class of widely used ICs. Regulator IC units contain the circuitry for reference source, comparator amplifier, control device, and overload protection all in a single IC. Although the internal construction of the IC is somewhat different from that described for discrete voltage regulator circuits, the external operation is much the same. IC units provide regulation of either a fixed positive voltage, a fixed negative voltage, or an adjustably set voltage. The regulators can be selected for operation with load currents from hundreds of milliamperes to tens of amperes, corresponding to power ratings from milliwatts to tens of watts.

8.3 IC 7805

Fig 3.2 shows the basic connection of a three-terminal voltage regulator IC to a load. The fixed voltage regulator has an unregulated dc input voltage (Vi) applied to the input terminal, a regulated output dc voltage(Vo) is taken from the second terminal, with the third terminal connected to ground. For a selected regulator, IC device specifications list a voltage range over which the input voltage can vary to maintain a

regulated output voltage over a range of load current. The specifications also list the amount of output voltage change resulting from a change in load current (load regulation) or in input voltage (line regulation).

Fixed Positive Voltage Regulators:

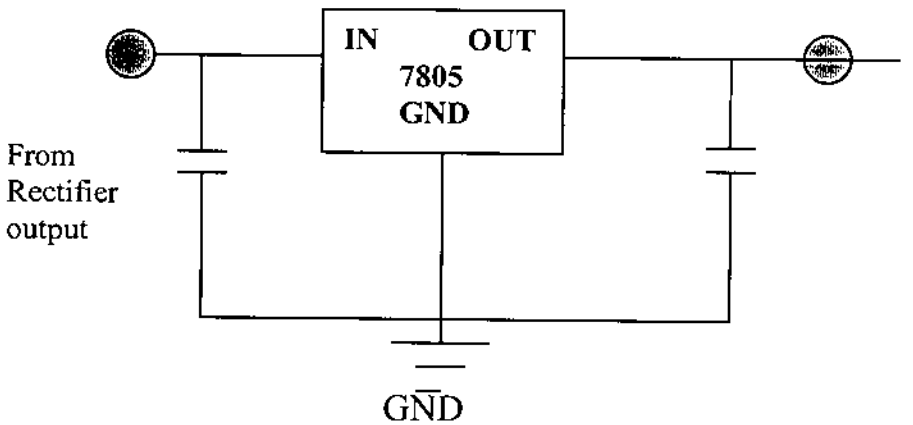


FIGURE 8.2 VOLTAGE REGULATION USING 7805

The series 78 regulators provide fixed regulated voltages from 5 to 24 V. Figure 19.26 shows how one such IC, a 7812, is connected to provide voltage regulation with output from this unit of +12V dc. An unregulated input voltage (Vi)is filtered by capacitor C1 and connected to the IC's IN terminal. The IC's OUT terminal provides a regulated + 12V which is filtered by capacitor C2 (mostly for any high-frequency noise). The third IC terminal is connected to ground (GND). While the input voltage may vary over some permissible voltage range, and the output load may vary over some acceptable range, the output voltage remains constant within specified voltage variation limits. These limitations are spelled out in the manufacturer's specification sheets. A table of positive voltage regulated ICs are provided in table 8.1.

IC Part	**Output Voltage (V)**	**Minimum Vi (V)**
7805	+5	7.3
7806	+6	8.3
7808	+8	10.5
7810	+10	12.5
7812	+12	14.6
7815	+15	17.7
7818	+18	21.0
7824	+24	27.1

TABLE 8.1 Positive Voltage Regulators in 7800 series

9. CONCLUSION

The project can be used effectively with in the globe. Police, fire, and emergency medical service units use GPS receivers to determine the police car, fire truck, or ambulance nearest to an emergency.

Moreover, Automobile manufacturers are also offering moving-map displays guided by GPS receivers as an option on new vehicles, for use in planning a trip. Tamilnadu government is going to use global positioning system to curb smuggling of rations.

The future scope of the project are as follows. The GPS kit can be miniatured using nano technology and can be placed inside the mobile present with the object to be traced. It can also be fabricated as a single GPS transmitting chip and placed within the object itself.

REFERENCES

1. E.Balagurusamy, "Programming in ANSI C" , Tata McGraw-Hill Publishing company Ltd., New Delhi, 1992.

2. John D.Krauss, "Antenna and propagation " II edition, McGraw-Hill International edition, 1988 .

3. www.gpsworld.com

4. www.wikipedia.com

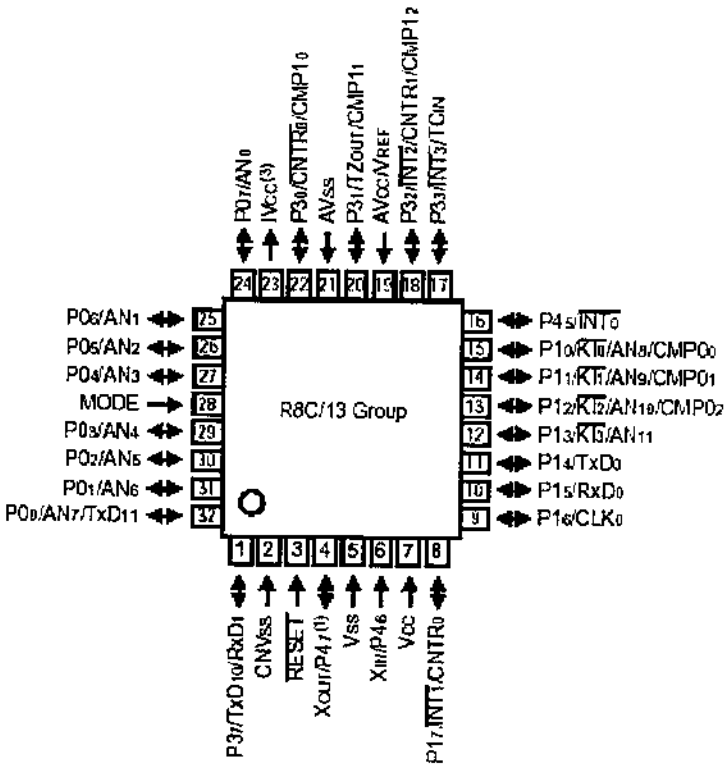
5. www.gpsy.com

6. www.microchip.com

APPENDIX A

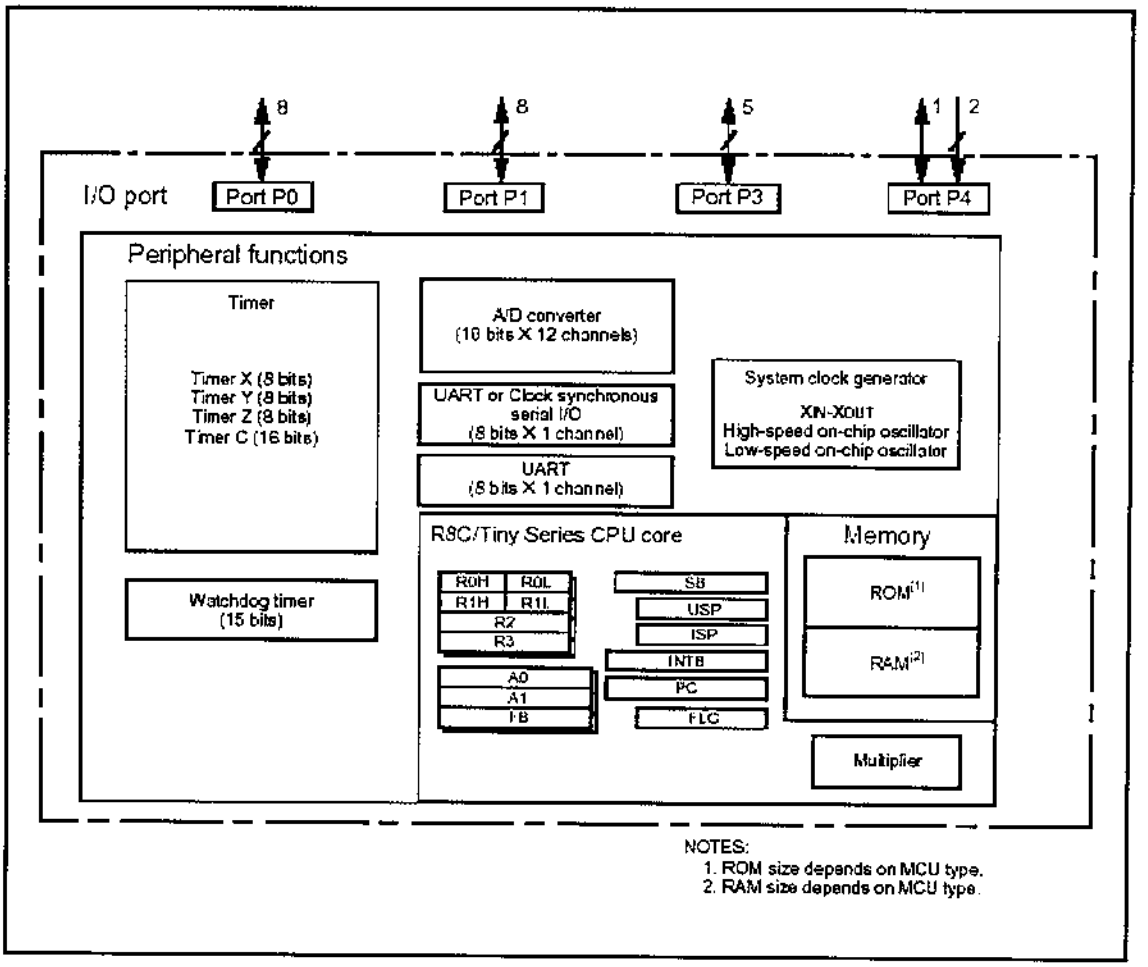
RENESAS

PIN DIAGRAM



NOTES:
1. P47 functions only as an input port.
2. When using On-chip debugger, do not use P00/AN7/TxD11 and P37/TxD10/RxD1 pins.
3. Do not connect IVcc to Vcc.

BLOCKDIAGRAM



APPENDIX B

MAX 232

Function Tables

EACH DRIVER

INPUT TIN	OUTPUT TOUT
L	H
H	L

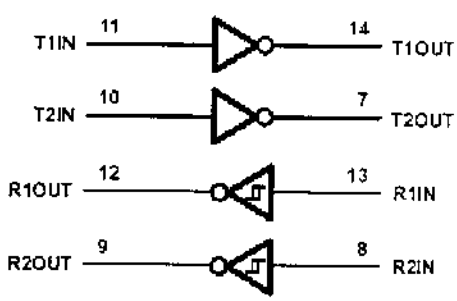
H = high level, L = low level

EACH RECEIVER

INPUT RIN	OUTPUT ROUT
L	H
H	L

H = high level, L = low level

logic diagram (positive logic)



APPENDIX C

CODING

```
#include "sfr_R813.h"                    //Definition of R8C/10 SFR
#include "lcd.h"

void sfr_init();                  /* Initial setting of SFR registers */
void ser_out(unsigned char);
void ser_out1(unsigned char);
void uart_sral();                  /* UART serial I/O sub routine */
void uart_sral1();
void gps_init();
void ser_dis(unsigned char*,unsigned char);
void ser_dis1(unsigned char*,unsigned char);
void msg_send();
void wait(unsigned int);
unsigned char x,er,aa,y,er1,bb,ms;
unsigned char v[250],da,hh,mm,ss,dd,m[10];
void msg();

void main()
{
  prc0=1;                          //Protect off
      cm05=0;cm13=1;cm14=0;    //Main Clock selected(cm0 bit 5, cm1
bit 3 and 4, ocd bit 2)
      cm15=1;                 //High Drive Capacity selected(CM1 bit 5)
      cm16=0;cm17=0;cm06=1;    //Divide by 8 selected(cm0 bit 5)
      prc0=0;                 //Protect on
```

```
    lcd_init();
    sfr_init();
    read(0x01);
    read(0x80);
    read(0x80);
    lcd_dis("TRACKING SYSTEM ",16);
    read(0xc0);
    lcd_dis("  GPS  & GSM   ",16);
    gps_init();
    uart_sral();
    wait(5);
    read(0x01);
while(1)
{
        uart_sral1();
        if(da>172)
  {
    for(da=57;da<70;da++)
                {
                  if(v[da]=='W')
                  {
                        read(0xC0);

                        write(v[da-11]);
                        write(v[da-10]);
                        write(':');
                        write(v[da-9]);
                        write(v[da-8]);
                }
```

```
}
for(da=125;da<133;da++)
{
                    if(v[da]=='M')
                    {
                        m[1]=v[da-6];
                        m[2]=v[da-5];
                        m[3]=v[da-4];
                        m[4]=v[da-3];
                        m[5]=v[da-2];
                        m[6]=v[da-1];

                        m[7]=v[da];
                }
        }
for(da=7;da<13;da++)  v[da]=v[da]-0x30;
hh=(v[7]*10)+v[8];
        mm=(v[9]*10)+v[10];
        ss=(v[11]*10)+v[12];
hh=hh+5;
            mm=mm+30;
            if(mm>60) {mm=mm-60;hh++;}

            msg();
            if(ms>0)  goto ls;
    read(0x80);
            lcd_dis("LAT:",4);
            for(da=19;da<30;da++) write(v[da]);
            wait(5);
```

```
                read(0x80);
                lcd_dis("LON:",4);
        for(da=31;da<43;da++) write(v[da]);
                wait(5);
                read(0x80);
        lcd_dis("          ",16);
                read(0x80);
                lcd_dis("ALT:",4);
        for(da=1;da<8;da++) write(m[da]);
                ls:
                wait(5);
                read(0xC8);
                write(hh/10+0x30);
                write(hh%10+0x30);
                write(':');
                write(mm/10+0x30);
                write(mm%10+0x30);
                write(':');
                write(ss/10+0x30);
                write(ss%10+0x30);
        if(ss<10) msg_send();
                da=0;
            }
    }
}



void sfr_init()
```

```
{
   pd1 = pd1 | 0x10;          //i/o setting
   pd0_0=1;              // output
       pd3_7=0;             // input

       u0mr = 0x05;         /* Setting UART0 transmit/receive mode
register */
   u0c0 = 0x00;         /* Setting UART0 transmit/receive control register
0 */
   u0rrm = 0;          /* Continuous receive mode disabled */
   u0brg = 103;        //baud rate reg
   re_u0c1 = 1;         /* Reception enabled */

       txd1en=0;                        // ser input
       txd1sel=1;
       u1mr = 0x05;         /* Setting UART1 transmit/receive mode
register */
   u1c0 = 0x00;         /* Setting UART1 transmit/receive control register
0 */
   u0rrm = 0;          /* Continuous receive mode disabled */
       u1brg = 103;       // 9600 baud rate reg
   re_u1c1 = 1;        /* Reception enabled */
}



void uart_sral()
{
```

```
    if (ir_s0ric)
    {
            x=1;
              ir_s0ric = 0;
     aa = u0rbl;
        er = u0rbh;          /* Get Reception error flags */
    }
}

void ser_out(unsigned char ss)
{
  u0tbl = ss;
  te_u0c1 = 1;              /* Transmission enabled */
     for(i=0;i<8000;i++);
}



void uart_sral1()
{
   if (ir_s1ric)
   {
            y=1;
              ir_s1ric = 0;
    bb=u1rbl&0x7f;
        er1=u1rbh;          /* Get Reception error flags */
              v[da]=bb;
              if(v[0]!='$'){da=0;goto last;}
              else if(v[0]=='$'&&v[1]!='G'){da=1;goto last;}
```

```
void msg_send()
{
 read(0x80);
 lcd_dis(" MSG TRANSMITED ",16);
 ser_dis("AT+CMGS=",8);
 ser_out("");
 ser_dis("9994694549",10);
 ser_out("");
 ser_out(0x0d);
 wait(10);
 if(ms==1) ser_dis("  Mp..pro. Lab  ",16);
 else if(ms==2)  ser_dis("Electronic Lab  ",16);
 else
 {
        ser_dis("LAT:",4);
        for(da=19;da<30;da++) ser_out(v[da]);
        ser_out(' '); ser_out(' ');
    ser_dis("LON:",4);
    for(da=30;da<43;da++) ser_out(v[da]);
    ser_out(' '); ser_out(' ');
    ser_dis("ALT:",4);
    for(da=1;da<8;da++) ser_out(m[da]);
 }
 ser_out(0x1a);
 read(0x80);
 lcd_dis("               ",16);
}
```

```
void msg()
{

 if((v[24]=='7'&&v[25]=='2')||(v[24]=='7'&&v[25]=='3'))
 {
   ms=1;
        read(0x80);
        lcd_dis("  Mp..pro. Lab  ",16);
 }
 else if((v[24]=='7'&&v[25]=='2')||(v[24]=='7'&&v[25]=='3'))
 {
   ms=2;
        read(0x80);
        lcd_dis("Electronic Lab  ",16);
 }

}



void ser_dis(unsigned char *dis,unsigned char rr)
{
 unsigned char m;



for (m=0;m<rr;m++)
 {
```

```
   ser_out(dis[m]);
  }
}

void ser_dis1(unsigned char *dis,unsigned char rr)
{
 unsigned char m;
 for (m=0;m<rr;m++)
 {
  ser_out1(dis[m]);
 }
}

void wait(unsigned int de)
{
  while(de--)
  {
   del();
  }
}
```