# PC COMMUNICATION THROUGH AC POWER LINES

## PROJECT REPORT

SUBMITTED BY



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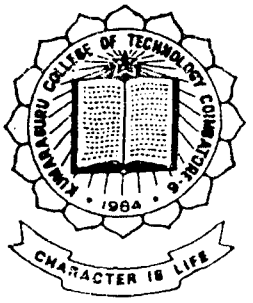
UNDER THE GUIDANCE OF

MISS. P. SUPRIYA, B.E., M.I.S.T.E.,

IN PARTIAL FULFILMENT OF THE REQUIREMENTS
FOR AWARD OF THE DEGREE OF

**BACHELOR OF ENGINEERING**

IN ELECTRICAL AND ELECTRONICS ENGINEERING OF THE
BHARATHIAR UNIVERSITY, COIMBATORE




DEPARTMENT OF
ELECTRICAL AND ELECTRONICS ENGINEERING

**KUMARAGURU COLLEGE OF TECHNOLOGY**

DEPARTMENT OF
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COIMBATORE - 641 006

## CERTIFICATE

This is to Certify that the
Report Entitled

# PC COMMUNICATION THROUGH AC POWER LINES

HAS BEEN SUBMITTED BY

*Mr. / Miss.* _____

*in partial fulfilment for the award of the Degree of Bachelor of Engineering in Electrical and Electronics Engineering Branch of the Bharathiar University, Coimbatore - 641 046 during the academic year 1994 - 95*

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*and the University Register Number was* _____

EXTERNAL EXAMINER

**CONTENTS**

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# PC COMMUNICATION THROUGH AC POWER LINES

## CONTENTS

## SYNOPSIS

Computers, the miraculous machines, have bright future for the decades to come. To increase their power and intelligence, they should have proper channels to communicate between them and the world. The communication of computer are sure to shrink the world to its smallest extent.

Our project **PERSONAL COMPUTER COMMUNICATION THROUGH A.C. POWER LINES** is one way of giving the computer an effective communicating power.

The Basis of carrier current communication is the transmission and reception of a carrier, modulated by data over the A.C lines. The carrier current chip utilises FSK modulation not only for its excelent impulse noise rejection but also for the simplicity of implementation in both the transmitter and receiver sections.

The carrier current communication of computers has its own versatility for their higher communication power with low cost. Due to complexity and noise interference it is not normally implied for their greater advantages.

We have succeeded in doing this PC communication through AC power lines, with higher accuracy and less complexity.

With good future developments our system might have greater impact in the forth coming years of our country.

A good software support is also with our project for making this more effective. It is certain that our project PC communication through AC power lines will gain a lighting attraction with future expansion.

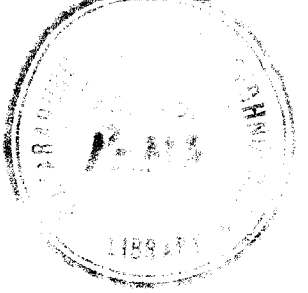
# CHAPTER I

## INTRODUCTION

Everywhere around us information is being exchanged between two or more points. Several methods are commonly used to convey this information, including optical, RF, ultrasonic and hardwired links. Anyone who has made use of one of these techniques will certainly remember its limitations : optical links operate only by line of sight, RF links are restricted by numerous regulations, ultrosonic links are interrupted by walls, and hardwired links require the costly installation of signal-carrying lines. Another alternative, a close relative of the harwired link, is carrier current communication the exchange of data via pre-existing AC lines.

The AC line makes a great data link. No after market installation is required most buildings are already wired. The link can be established anywhere there is an AC socket by simply plugging in a line cord one then wonders why such a wounderful communication link is seldom used? The answer lies in the basis of the link itself : The AC line contains not only 230V RMS of unwanted signal, but also kilo-volt spikes,

both of which present fundamental design challenges for carrier current circuits. Meeting these challenges necessarily leads to complex and costly discrete circuit designs. The concept of a carrier current link should not be abandoned, however, as a recently introduced integrated circuit now offers the solution for carrier current links. This new carrier current tranceiver IC forms the heart of a sophisticated single-chip half duplex AC line link.



# CHAPTER 2

## SYSTEM DESCRIPTION

### 2.1 THE AC POWER LINE:

The noise on the line can be loosely put into two categories: borad band and impulse. Broad-band noise come from many sources, with universal motors being one notorious example. The level varies from a few to hundreds of millivolts. Impulse noise also varies widely in a level ranging from millivolts to tens of volts and sometimes much more. The impulses are more often than not sychronized to the power line frequency and ring with the natural frequency of the line (another widely varying parameter). The prime culprits here are switching thyristers. In general, noise is worst in factories, moderate in offices, and least in private dwellings.

The impedance of the line is likewise ill-defined. It may be resistive, inductive or capacitive. Above 50KHz, the impedance rises to a sufficiently high value to be driven as a load (at low frequencies, it approximates a voltage source). Frequencies below 50KHz also have considerable difficulty - capacitively coupling across the windings of power distribution transformer. This is some times an asset,

but often a curse. Frequencies above 300 KHz experience greater attenuation due to the distributed LC nature of power cabling and are more adversely affected by capacitive loads in the form of line bypass capacitors that are finding increasing use in an RFI.

For the reasons stated, a range of operation that encompasses 50 - 300 KHz was deemed adquate for most applications. At 125 KHz in an office environment, an impedance of (5+j10) Ω might be considered typical. Impedances in home wiring may be over 50 Ω, while factory impedances may be less than 1 Ω. Line bypass capacitors of 1 μf or more will short the carrier in most enviorments unless isolated with chokes or driven with several watts of carrier power.

Line attenuation is very difficult to estimate because it is extremely load dependent. A high power load can significantly reduce the impedance of the line at the point of connection and thus dominate attenuation for all points of communication that occur beyond the offending load unless that load is isolated with chokes. Capacitive loads can be equally troublesome and are not necessarily with high power loads. Care must be taken to ensure that once a carrier current command is passed to turn on such a low impedance load, the command to turn it back off again will

likewise be received. Another large component of the net attenuation can be the signal loss incurred in coupling across the multiple windings of a power distribution transformer. This alone can amount to 20 to 40 dB, depending upon the carrier frequency and transformer construction. External capacitors are effective in bridging signals across windings in areas where this is desired. The power cabling itself has little opportunity to behave like a transmission line at such low frequecies, although the distributed LC losses can become significant for long runs. In extreme cases of attenuation, frequency - translating repeaters can be used to boost signal levels or brute force signal power can be exployed.

## 2.2 THE CHIP ARCHITECTURE :

The chip architecture is shown in fig 1 . The important blocks and its functions are given below,

### 2.21 MODULATOR :

Modulator modulates the data signal with high frequency carrier signal. This process is called modulation. Here the transmitter utilizes the modulator which uses FSK modulation. The modulator must generate three currents representing F low, F high and F centre.

## 2.22 THE CURRENT CONTROLLED OSCILLATOR :

The ICO is shared by the RX and TX modes and thus runs continuously. It has two wide band, low TC, and linearly controllable for analog signals. Its output must be a square wave to drive PLL and good quality triangle wave to drive the sine shaper.

## 2.23 THE SINE SHAPER :

The output of the sine shaper drives the Automatic Level Controller (ALC). The triangle wave is first attenuated to the optimum amplitude and then used to switch a differential pair degenerated at the optimum level. The tuned output transformer reduces the distortion to typically below 0.1 percent before it is fed to the line.

## 2.24 OUTPUT AMPLIFIER :

The constraints imposed by the power line interface were felt most severly by the output stage; These constraints, coupled with several other circuit requirements meant that the output stage had to meet the following formidable list of criteria,

1. Ability to withstand and protect the whole chip from high energy line transient.

2. High current gain equal to 200.

3. Gain boostable with external device to greater than 2000.

4. Sufficient gain-bandwidth product to pass a large signal at 300 KHz

5. Ability to be easily put into a high impedance state.

6. Ability to withstand an indefinite short circuit.

7. Ability to maintain waveform purity with loads that range from near shorts to near open circuits.

8. Ability to maintain closed-loop stability for any value of complex load impedance.

9. Ability to swing to nearly twice the supply voltage.

10. Ability to tolerate large supply ripple.

## 2.25 THE LIMITER :

The limiter provides some needed amplification (33dB) for the PLL. It also removes some amplitude noise, as well as band limiting the input to lie between 50 and 300 KHz. The signal from the line passes through the tuned transformer where it is stepped up and filtered of extraneous signals, noise and 50 Hz.

The importance of the rejection of the 50 Hz line voltage and 120 Hz supply ripple should not be underestimated. To acheieve 1 mv sensitivity, 50 Hz must be rejected by at least 107 dB and 120 Hz by at least 63 dB. The high pass characteristics at the input to the transformer, the tuned tank itself, the balance of the input stage and the frequency selective feedback amplifier all combine to acheieve these numbers.

## 2.26 PHASE LOCKED LOOP :

The PLL is essentiallly a frequency feedback system comprising a phase comparator, a low pass filter, an error amplifier in the forward signal path and a voltage controlled oscillator (VCO) in the feedback path. The operation of the PLL as follows,

When there is no input signal to the PLL, error voltage $V_e$ is zero. The VCO operates at a set frequency fo , which is known as the free running frequency. If an input signal (fs ) is applied to the PLL, the phase comparator compares the phase and frequency of the input signal with the VCO frequency and generates an error voltage Ve(t) that is related to the phase and the frequency difference between the two signals. The Ve(t) is then filtered, amplified and applied as input to the VCO. The effect of

Vd(t) is to force the VCO frequency to vary in a direction that reduces the frequency difference between the VCO output and the input signal. If fs is sufficiently close to fo , the feedback nature of the PLL causes the VCO to synchronize with the incoming signal. Once synchronized, fo is identical to fs , except for a finite phase difference (Ø ). This is necessary to generate the corrective error voltage Vd to shift the VCO frequency from its free running value of fs , thereby maintaining the PLL in lock.

## 2.27 THE OFFSET CANCEL CIRCUIT :

Due to the high gain in the signal path, some provision has to be made for cancelling offset voltage prior to accurate data slicing in the comparator. Straight forward capacitive coupling will eliminate offset, but has a lower frequency limit problem (if the capacitor is sized small enough for rapid changing in a TX to RX switch over) and will charge to the net dc value of the data, thus restricting users to keeping the signal duty cycle near 50 percent.

DC feedback loops also cannot separate dc inherent in the data from dc offset. The offset cancelling circuit will eliminate dc offsets from the data path without responding to [illegible] inherent in the data stream

itself. Strings of 100 ones or zeros or more can be accommmodated and the setup time for the circuit in switching from TX to RX is only two bit times.

## 2.28 THE TIME DOMAIN FILTER :

Impulse noise creates severe problems for carrier current systems. Fortunately, the impulses do not usually last very long provided no tuned circuits in the system can store substantial energy. By keeping data rates low (less than 1K baud is recommended), the noise pulses will usually be significantly shorter than data pulses. This means a filter that discriminates against noise based upon its time duration rather than its frequency spectrum can be quite useful. The time domain filter used here is very simple, yet very effective in removing impulse noise. The external capacitor it uses can be selected to set the time cut off; the minimum pulse width that the filter allow to pass.

## 2.3 TYPICAL PERFORMANCE :

### GENERAL

Supply voltage.....18v

Programmable carrier frequency Fo.....50 to 300 KHZ

Oscillator TC of Fo.....± 100 ppm / °C

## TRANSMITTER

FSK deviation ..... ± 2.5%

Output Current ..... 60mA p-p

Output Voltage(line z=10Ω) ..... 4.0V p-p

Output Voltage distortion(Q=10tank) ..... 0.1%

Power output (Line z=10Ω) ..... 200mW

RX to TX Switch over time ..... 40µs

Supply Current ..... 38mA

## RECEIVER

Sensitivity ..... 1mV rms

Data rate ..... 0 to 4K Baud

TX to RX switch over time ..... 2 bits

Supply Current ..... 13 mA

For Pin Details of LM 1893 TRANSCEIVER IC Refer APPENDIX 1

## 2.4 FEATURES OF LM 1893 IC :

* Noise resistant FSK modulation.
* User selected impulse noise filtering.
* Up to 4.8 Kbaud data transmission rate.
* Strings of 0's and 1's in data allowed.
* Sinsoidal line drive for low RFI.
* [illegible] easily boosted 10-fold.

* 50 to 300 KHZ carrier frequency choice.
* TTL and MOS compatible digital levels.
* Regulated voltage to power logic.
* Drives all conventional power lines.

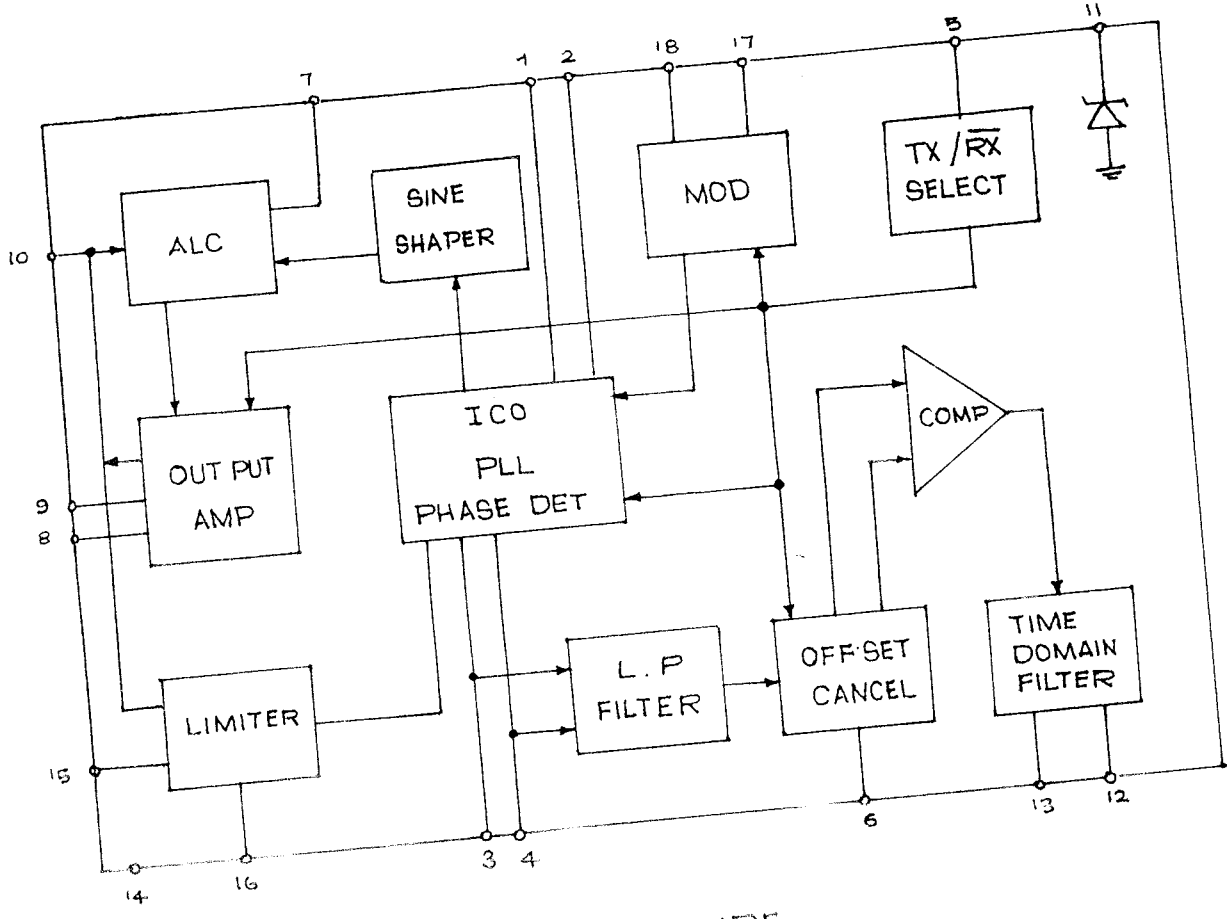



FIG. 1. CHIP ARCHITECTURE.

# CIRCUIT DESCRIPTION

# CIRCUIT DESCRIPTION

## 3.1 INTRODUCTION;-

Each line interface requires one chip along with a handful of inexpensive passive components. A simple unregulated supply with up to 2V p-p of ripple can be used. Three logic compatible ports DATA IN, DATA OUT and TX/RX SELECT, interface to the digital circuitry, while the fourth line from the 5.6 V Zener diode can be buffered with an n.p.n emitter follower and used to power the digital circuitary.

When in the transmit mode, the incoming serial data stream switches the modulator which drives the low TC current controlled osicllator (ICO) to produce a triangle wave with a ±2.5 percent frequency deviation. The triangle wave is then attenuated and fed to a sine shaper which delivers a current sinusoid through an automatic level control (ALC) circuit to the power current amplifier. The tuned transformer converts the 60mA p-p current sinusoid to a voltage that depends upon line impedance , steps the voltage down, and then drives the line through a coupling capacitor. Should line impedance be high, the ALC circuit diverts signal current away from the output amplifier to maintain waveform purity by preventing saturation of the amplifier.

In the receive mode, the DATA IN PORT is inhibited, the transmitter output is put into a high impedance state and the ICO is set to run at the carrier center frenceny. The coupling capacitor and tuned transformer pass the desired signal while attenuating 50 Hz to a large degree and filtering out some noise. A rugged Norton-input limiter amplifier further attenuates 50 Hz and certain noise components before passing the signal to the PLL detector. The demodulated output from the second order loop passed through a three stage differential low pass filter and on the offset cancelling circuit. After Vos has been removed, the data are then accurately separated into ones and zeros (sliced) by one comparator. At this point, the data often still riddled with impulse noise, pass through a time domain filter before driving the open-collector output stage.

## 3.2 HOW TO USE THE LM 1893 TRANSCEIVER :-

### 3.21 PURPOSE :-

The purpose of this kit is to provide the designer with a complete LM 1893 circuit which can be easily adapted to an existing digital system for evaluation. To this end the enclosed printed circuit board has been designed to be as compact as possible. All of the special components required for operation are included in this kit. The assembled board require an 18V, 100ma power supply, 3 connection to the

associated digital circuitry, and two connections to the power line.

## 3.22 PRECAUTIONS :-

The power line is a potential source for diaster, and several precautions are recommended : First, a line cord with a polarized plug must be used. Neutral (N) is to be connected to the coil side of the input and live (L) to the 220nF line coupling capacitor. The capacitor must have a breakdown rating of at least 1.5 times the RMS line voltage. Failure to use a capacitor with adequate voltage rating will result in a shock and fire hazard. In addition, capacitors of lower voltage ratings may explode when connected to the line. When the power line portion of the board has been assembled it is wise to place a strip of PVC electrical tape over the copper side to reduce the chance of an accidental short circuit. Two small mounting holes have been included and should be used to secure the board (copper side down) to a solid surface.

Energy at the power line frequency is greatly attenuated by the input coupling network. Large energy surges can still occur at or near the band pass frequency of this network. While the LM 1893 is designed to absorb a 30W pulse, much higher power levels are often experienced. To handle these occurances, a 600w or larger transient absorbing Zener diode

and 5.1 Ω resistor are connected to the chip side of the coupling network, and the Zener diode is included in this kit.

## 3.23 TUNING

This kit is intended to operate at a carrier frequency of 125 KHz and a data rate of 360 baud. Before the boards are used this tuning procedure must be followed,

1. Attach a frequency counter to the prongs of the power cord. Note that the power cord must NOT be plugged into the line.

2. Temporarily tie pins 5 and 17 to pin 15.

3. Connect an 18V power supply and adjust the trim pot for a indicated frequency of 122.25KHz.

4. Remove the power supply and the connections made in step 2. the input coupling network tuning is affected by the impedance of the power line. Therefore, tuning must be adjusted with the power cord connected to the line, or to an impedance simulation network. If one power line is involved, extreme caution must be exercised during this procedure.

5. Temporarily connect pin5 to pin15 (v+)

6. Temporarily connect a 390 Ω resistor from pin 10 to 15.

[illegible] oscilloscope to pin 10.

7. Input a data stream (360 baud) or 5V square wave (180 Hz) to pin17.
8. Connect an 18V power supply.
9. Plug power cord into line and adjust T1 for equal amplitude signal envelopes as carrier follows modulation.
10. Disconnect power cord from line.
11. Disconnect supply, signal, 390 Ω resistor and pin 5 jumper.

The LM 1893 has been disigned with digital interface in mind. The digital input (pin17) and the transmit/receiver switch (pin5) are designed to accept all standard 5V logic levels. The digital output (pin12) is an open collector. Holes are provided on the board to optionally pull this pin up to 5.6V. In this instance, Rz must be sized accordingly to carry the current of pin 12.

## 3.24 LINE COUPLING TRANSFORMER :

Essential to the transformer is its loaded Q. Loaded Q is a function of frequency, parallel load resistance, and inductance. The coil supplied has a primary inductance of 49μH and gives a loaded Q of approximately 10 at 125 KHz. A tapped secondary provides matching into 2.5, 5 and 10 Ω lines.

## 3.25 LINE COUPLING CAPACITOR :-

Since this component is connected to the power line, its breakdown voltage rating is important. The part supplied is rated at 400V and is adequate for up to 250V power lines.

## 3.26 COUPLING COIL:-

The coupling coil plays an important role in transmitting and receiving signals on the A.C line. To fully understand the design of this coil, one must consider the characteristics of the A.C line. Generally the A.C.line, measured at a frequency of 100 KHz, can be modelled as a resistor and an inductor connected in series. Typical line parameters are shown in fig (4)

The inductance parameter varies widely regardless of environment, resistance shows a much stronger dependence. Industrial enviornments present a resistance of 2 to 5Ω and residential environments shows a resistance of 5 to 30Ω. Impedance also varies with changes in the loading of the AC line.

With such unpredictable line impedance, coupling the output amplifier is difficult. The coupling will couples signal to one line via a step down secondary.

When operating in receive mode, the coupling line performs several important functions. These include

1. 50Hz Rejection
2. Signal Bandpassing
3. Ohmic Isolation from the AC line.

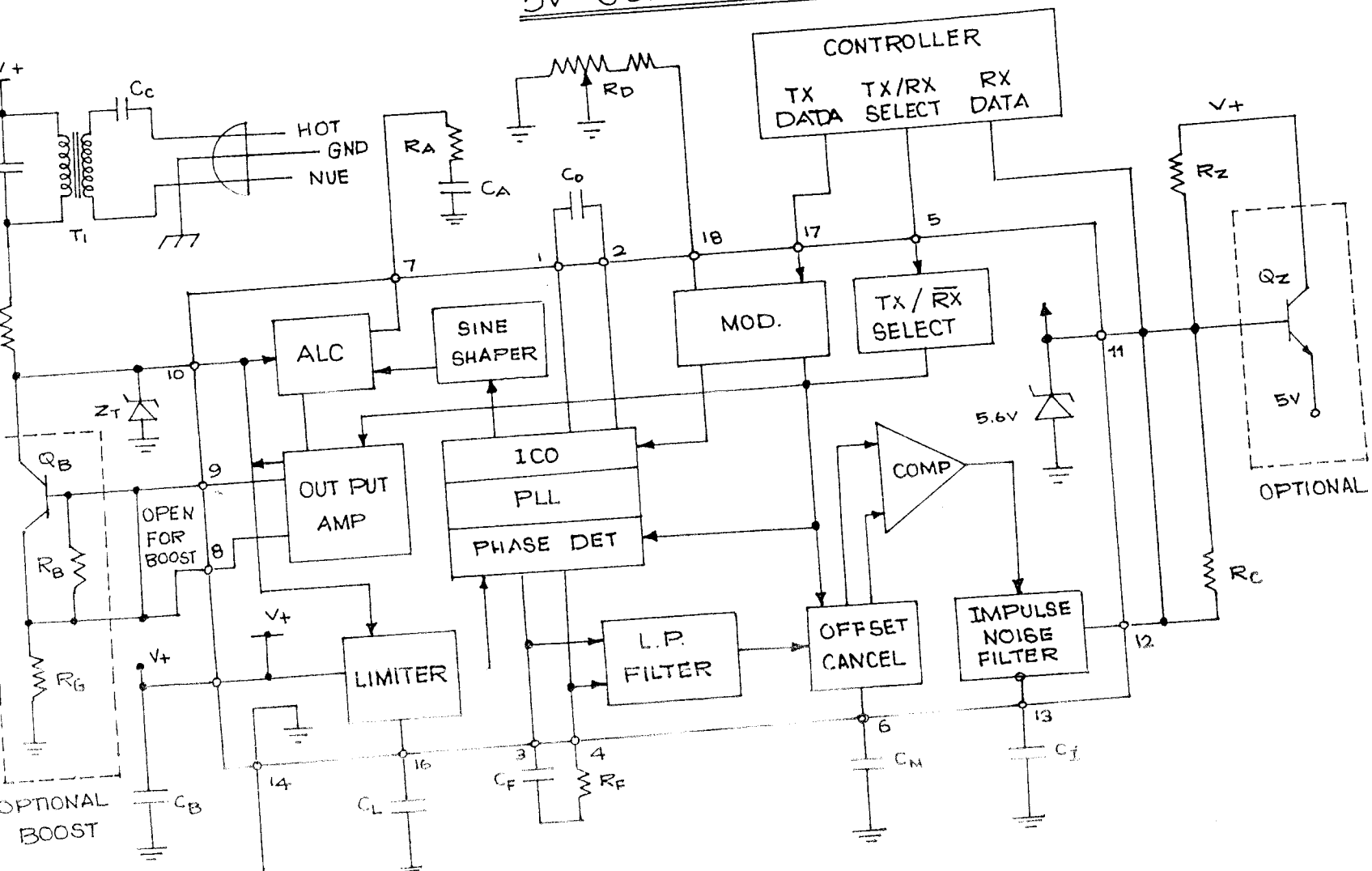
In addition the coupling coil is connected in such a way so as to step up the received signal by a factor of the turns ratio.

The general electrical characterisics, transmitter electrical characterisics and receiver electrical characterisics are shown appendix II

## 3.3 WAVE FORMS :-

Operating wave forms of a line synchronized tranceiver pair are shown. The diagram shown how the transmitted data transitions may be used as received data sampling points. The wave forms are shown in fig (3)

# CCT SYSTEM WITH BOOST AND 5V SUPPLY OPTIONS



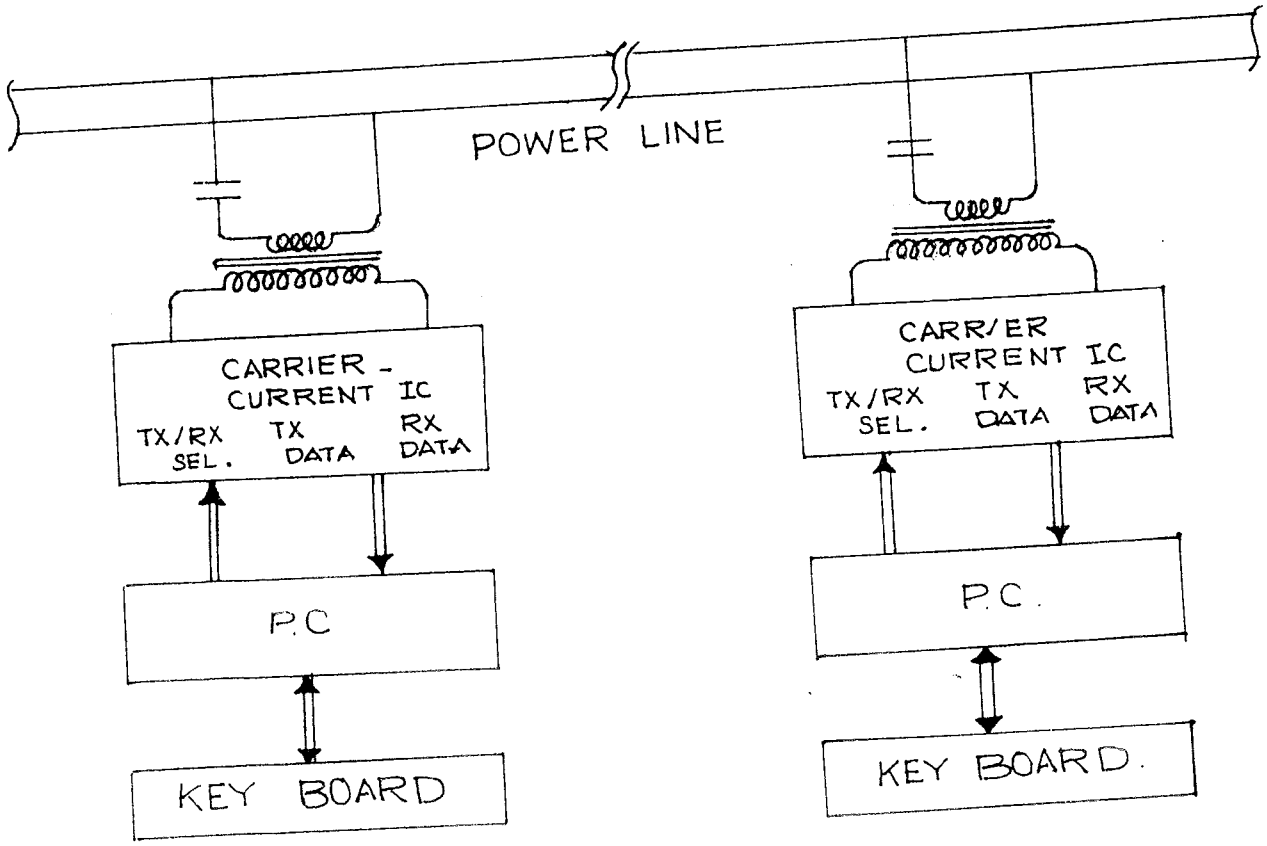



FIG. 2. INTERFACING PC TO POWER LINE.

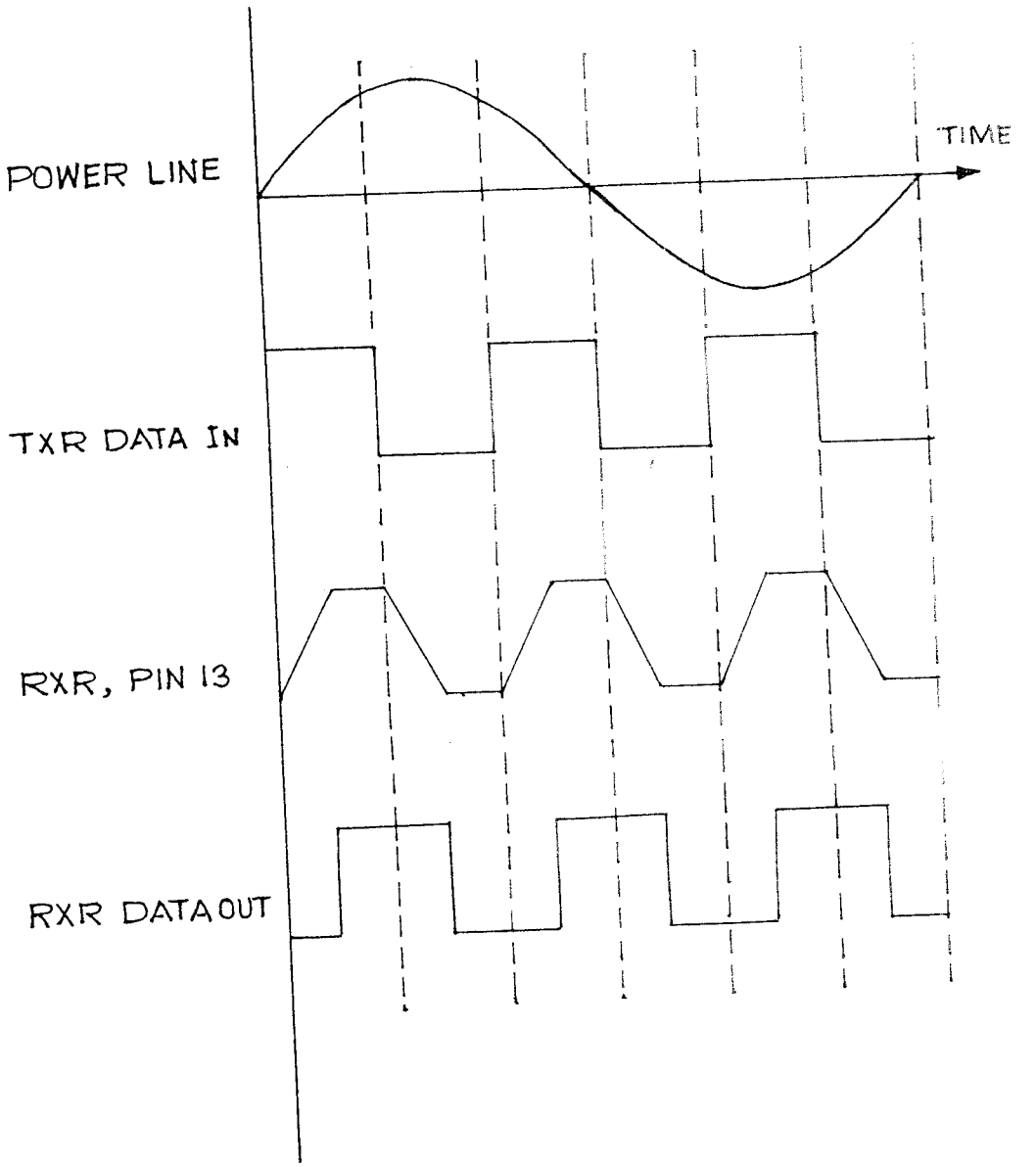



FIG. 3. OPERATING WAVE FORMS.

# DESIGN

# CHAPTER 4

## DESIGN

The circuit consists of the following components $C_O$, $R_O$, $C_F$, $R_F$, $C_C$, $C_Q$, $T_1$, $C_A$, $R_A$, $C_L$, $C_M$, $C_I$, $R_C$, $Z_T$, $R_T$, $R_B$, $Q_B$, $R_B$ and $C_G$. The design is carried out by referring APPENDIX 2.

Typical value of all the components for V+ = 18v , Fo = 125 KHz, $F_{DATA}$ = 360 Baud using 230V , 50Hz power line are given below,

### 4.1 Co and Ro :

Co :

Purpose : Together, Co and Ro set ICO Fo.

Smaller : Increases Fo

Larger : Decreases Fo

Recommended Value : 560 pF

Ro :

Purpose : Together, Co and Ro set ICC Fo.

Smaller : Increases Fo

Larger : Decreases Fo

Recommended Value : 6.2 KOhm

4.2 $C_F$ and $R_E$ :

$C_F$ :

Purpose : PLL Loop Filter pole.

Smaller : Less noise immune,higher $F_{DATA}$, more PLL stability

Larger : More noise immune,lower $F_{DATA}$, less PLL stability

Recommended Value : 0.047 μF

$R_F$ :

Purpose : PLL Loop Filter zero

Smaller : PLL less stable,allows less $C_F$. Less ringing.

Larger : PLL more stable,allows more $C_F$. More ringing.

Recommended Value : 3.3 KOhm

4.3 Cc :

Cc :

Purpose : Couple Fo to line, Cc and T1 low-pass attenuates 50 Hz.

Smaller : Low TX line amplitude. Less 50

Larger : Drives Lower line Z, More 50 Hz T1 current. More stored charge

Recommended Value : 0.22 µF

Purpose : Tank matches line Z, bandpass filters, isolates from line and attenuates transients

Smaller : Tank Fo up or increase L of T1 for constant Fo Smaller L: Higher Fo or increase Cc; decreased Fo line pull

Larger : Tank Fo down or decrease L of T1 for constant Fo Larger L: Lower Fo or decrease Cc; increased line pull

Recommended Value : 0.033 µF

## 4.4 $C_Q$ and $T_1$ :

$C_Q$ :

Purpose : Tank matches line Z, bandpass filters, isolates from line and attenuates transients

Smaller : Tank Fo up or increase L of T1 for constant Fo Smaller L: Higher Fo or increase Cc; decreased Fo line pull

Larger : Tank Fo down or decrease L of T1 for constant Fo Larger L: Lower Fo or decrease Cc; increased Fo line pull

Recommended Value : 0.033 µF

T1 :

Purpose : Tank matches line Z, bandpass filters, isolates from line and attenuates transients

Smaller : Tank Fo up or increase L of T1 for constant Fo Smaller L: Higher Fo or increase Cc; decreased Fo line pull

Larger : Tank Fo down or decrease L of T1 for constant Fo Larger L: Lower Fo or decrease Cc; increased Fo line pull

Recommended Value : Use recommended XFMR

4.5 $C_A$ and $R_A$ :

$C_A$ :

Purpose : ALC pole

Smaller : Noise spikes turn ALC off.

Larger : Slower ALC response

Recommended Value: 0.1 µF

$R_A$ :

Purpose : ALC zero

Smaller : Less stable ALC

Larger : More stable ALC

Recommended Value: 10 KOhm

4.6 $C_L$ :-

Purpose : Limiter 50 kHz pole, 50 Hz rejection

Smaller : Higher pole F, more 50 Hz reject. Fo attenuation.

Larger : Lower pole F, less 60 Hz reject, more noice BW.

Recommended Value: 0.1 µF

4.7 $C_M$ :-

Purpose : Holds RX path $V_{OS}$

Smaller : Less noice immune, shorter $V_{OS}$ hold , faster $V_{OS}$ aquisition, shorter preamble.

Larger : more noice immune, longer $V_{OS}$ hold , slower $V_{OS}$ aquisition, longer preamble.

Recommended Value: 0.47 µF

4.8 $C_I$ :-

Purpose : Rejects short pulses like impulse noise.

Smaller : Less impulse reject, delay

Larger : More impulse reject, delay

Recommended Value : 0.47 µF

4.9 $R_C$ :-

Purpose : Open-col. pull up

Smaller : Less available sink I .

Larger : Less available source I .

Recommended Value: 10 KOhm.

4.10 $R_Z$ :-

Purpose : 5.6 V Zener bias

Smaller : Larger shunt current, more chip dissipation

Larger : smaller shunt current, less V+ current draw

Recommended Value: 12 KOhm.

4.11 $Z_T$ and $R_T$ :-

$Z_T$ :

Purpose : Transient clamp

Smaller : Higher $R_Z$ - excess peak V, Zener and chip damage.

Larger : Lower $R_Z$ gives enhanced transient clamp, costly.

Value: > 44 V BV

$R_T$ :-

Purpose : Transient I limit

Smaller : Damage Z$_T$ , pull up V+ .

Larger : Excessive TX attenuation .

Recommended Value: 4.7 Ohm.

## 4.12 $P_B$ , $Q_B$ and $R_G$ :-

$R_B$ :

Purpose : Base bleed

Smaller : Faster , lower THD $I_O$ .

Larger : Inadequate turn-off speed .

Recommended Value: 180 Ohm.

$Q_B$ :-

Purpose : Boost gain device .

Smaller : Excessive $I_J$ and $V_{SAT}$ .

Larger : More rugged, but costly .

Recommended Value: Power NPN .

$R_G$ :-

Purpose : Current setting $R_G$ .

Smaller : More $I_0$ , need higher $h_{fe}$ .

Larger : Less $I_0$ , lower min. $h_{fe}$ .

Recommended Value: 1.1 Ohm.

4.13 $C_B$ :-

Purpose : Supply bypass .

Smaller : Transients destroy chip.

Larger : Less supply spike .

Recommended Value: ≥ 47 µF.

# CHAPTER 5

## FUNCTIONAL DESCRIPTION

The data is serially transmitted and received through the asynchronous communication port which supports RS-232C standards. In the IBM PC serial ports are configured as COM1 and COM2. The addresses for these ports

| | | | | |
|---|---|---|---|---|
| COM 1 | 3F8 | - | 3FF | H |
| COM 2 | 2F8 | - | 2FF | H |

The communication port utilises INS 8250 for serial transmission and reception. To do this it has a number of accessible registers. These registers can be controlled by programmer through PC.

### LINE CONTROL REGISTER :

The system programmer specifies the format of the asynchronous data communications through the line register. In addition to this we may retrieve the contents of the line control register for inspection. This feature simplifies the system programming.

| | | |
|---|---|---|
| Bit 7 | - | Divisor latch access bit. |
| Bit 6 | - | Set break. |
| Bit 5 | - | Stick parity. |
| Bit 4 | - | Even parity select. |

Bit 3 - Parity enable.

Bit 2 - No. of Stop bits.

Bit 1 - Word length select bit 1.

Bit 0 - Word length select bit 0.

## 5.3 BIT DESCRIPTION :

**Bit 0 & 1 :**

These two bits specify the number of bits in each transmitted or received serial character. Encoding of bits are as follows.

| Bit 1 | Bit 0 | Word length |
|---|---|---|
| 0 | 0 | 5 bits |
| 0 | 1 | 6 bits |
| 1 | 0 | 7 bits |
| 1 | 1 | 8 bits |

**Bit 2 :**

This bit specifies the number of stop bits in the transmitted or received serial character. If this is logical '0' one stop bit is generated or checked in the received data. If it is logical '1' , when a 5 bit word length is selected, then 1½ stop bits are generated or checked.

Bit 3 :

This is the parity enable bit. When bit3 is logic 1 a parity is generated (transmitted data) or checked (received data).

Bit 4 :

This is the even parity select bit. If it is logic '1' and bit 3 is logical '1' transmission and checking is done for even number of bits. If it is logical '0' odd parity is established.

Bit 5 :

This bit is stick parity bit.

Bit 6 :

This is set break control. If this is logical '1' the serial output is forced to the spacing state and remains there regardless of the transmitter activity.

Bit 7 :

Device latch access bit, which is set high to access the devisor latches of the baud rate generator during a read or write operation. It is set slow to access the receiver buffer.

## 5.4 PROGRAMMABLE BAUD RATE GENERATOR :

INS 8250 contains a programmable baud rate generator that is capable of taking the system clock and dividing it by any divisor from 1 to 216. Two 8 bit latches are used to store the divisor. The divisor used for generating various baud rate are

| | In Hex |
|---|---|
| 50 | 900 |
| 75 | 600 |
| 110 | 417 |
| 150 | 300 |
| 300 | 180 |
| 1200 | 060 |
| 1800 | 040 |

## 5.5 LINE STATUS REGISTER :

The status information concerning the data transfer from a processor is provided. The bit indication are given below.

| Hex Address | 3 FD H |
|---|---|
| Bit 7 | 0 |
| Bit 6 | Tx Shift register empty |
| Bit 5 | Tx Holding register empty |
| Bit 4 | Break interrupt |
| Bit 3 | Framing error |

| | |
|---|---|
| Bit 2 | parity error |
| Bit 1 | over run error |
| Bit 0 | Data ready |

## 5.6 INTERRUPT IDENTIFICATION REGISTER :

INS 8250 has an on chip interrupt capability that allows complete flexibility in interfacing it tp almost all the microprocessor. It priorities into four levels.

1. Receiver line status.
2. Received data Ready.
3. Transmitter circuit holding register empty.
4. Modem status.

respectively.

## 5.7 INTERRUPT ENABLE REGISTER :

It controls the interface with the modem. It is of 8 bit length.

| | |
|---|---|
| Bit 7,6,5 | 0 |
| Bit 4 | Loop Back |
| Bit 3 | Out 2 |
| Bit 2 | Out 1 |
| Bit 1 | Request to send |
| Bit 0 | Data terminal ready |

The receiver buffer register which contains the received character which is of 8 bit length.

The 8 bit transmitter holding register contains the character to be serially transmitted.

The 8 bit modem status register provides the current state of the control lines from the modem to the PC.

## - 232C STANDARD :

This is the universal standard followed for the serial data communication. Here the logical states 0 and 1 are represented by +12 and -12 voltage. The logical 1 which is represented by -12V is done so in order to reduce the noise interference and to increase the accuracy of reception. Special purpose IC's are available for converting the digital into RS - 232C standards. In this IC communication our serial communication. A 9 pin RS - 232 connector is used in PC communication whose details are enclosed in appendix III

## 1489 RS - 232 RECEIVER :

Since the transmitter transmits the data of 5 V logic, so it is important to convert the RS 232C output of 12V into 5V it is done by 1489-RS232 Receiver Chip. Pin detail see Appendix III.

## 1488 RS - 232C DRIVER :

To communicate with the PC, the received 5V signal must be converted into 12V which is done by 1488 RS 232 driver. For pin detail see appendix III.

# CHAPTER 6

## SOFTWARE DESCRIPTION

A proper software support to satisfy the requirements of our system is also provided. The software is developed in 'TURBO C'.

Here the communication between computers takes place through the asynchronous communication port. The speed with which the information gets transmitted (Baud rate) is programmable using the file MODE.COM in DOS.

Our system can operate under 150 and 300 baud. The initialisation of baud rate with all necessary options like type of parity, number of stop bits and number of bits etc., can be done from our software itself. As we enter into the software and choose the first option the computer will request for the initialisation operation.

Operations 2,3,4 from the three modes of transmission in our system. Using option 2 we can transmit a set of words continously aso that a synchonisation can be achived between the transmitter and receiver, provided the initialisation ... in both the systems.

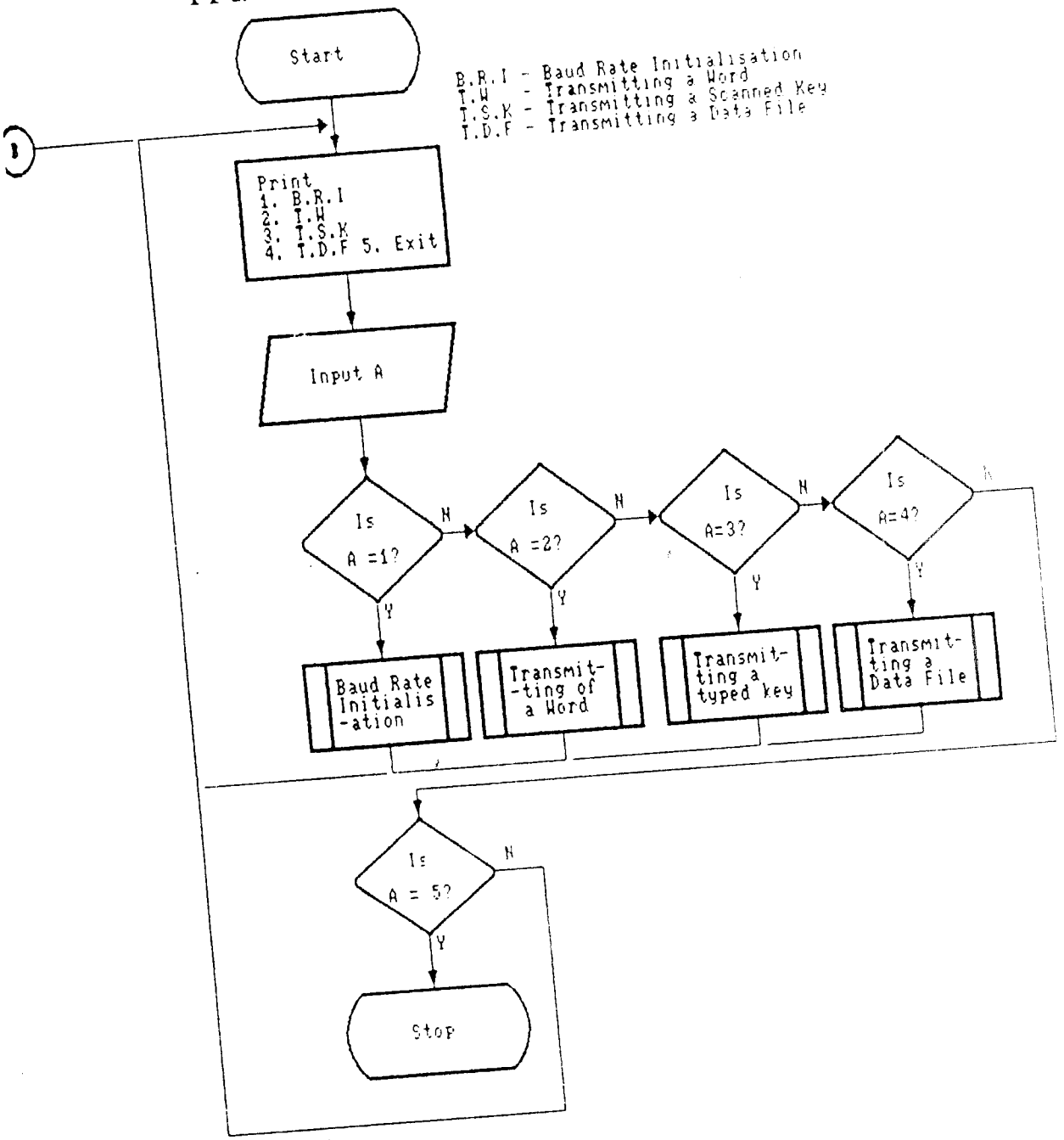
The Next option transmits a scanned Key (ie) any key pressed on the keyboard is converted into the corresponding ASCII and gets transmitted. We have provided facility to return from the option to the main menu which is done by pressing the ENTER KEY.

The fourth option is for data file transmission. Any data file can be transmitted through Rs-232 and can be received at the receiver. For the users knowledge the data file while transmission is monitred in the screen. Again at the receiving end the data received is displayed on the computer moniter and gets stored to secondary devices like floppy diskettes.

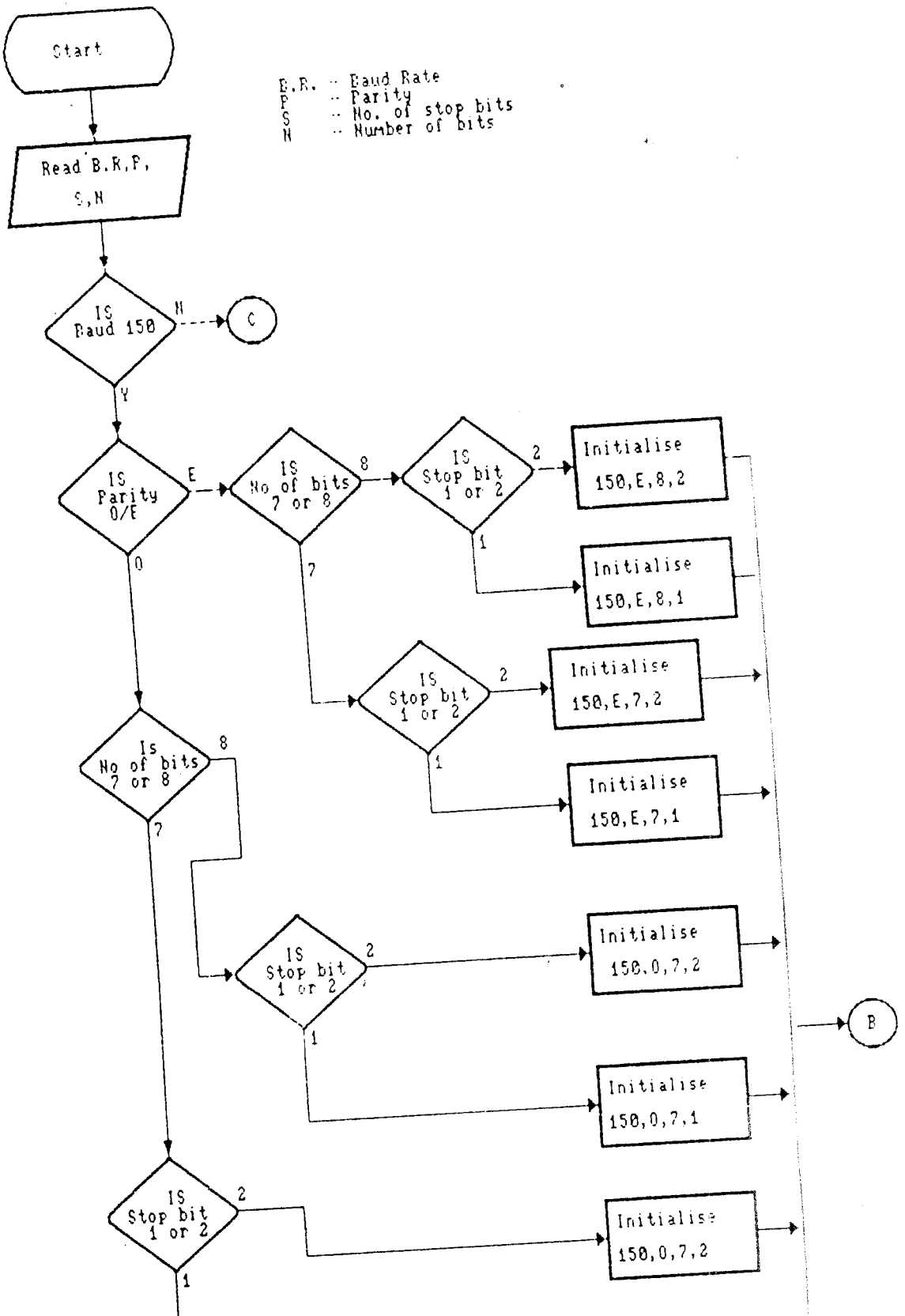
The last and final option is to quit from out software. When this option is selected the compter comes out of our software saying "GOOD BYE"..... ! and waits for further usage in the DOS prompt.

The above mentioned options are all provided in receiving computer and should be properly selected for receiving the transmitted signal.

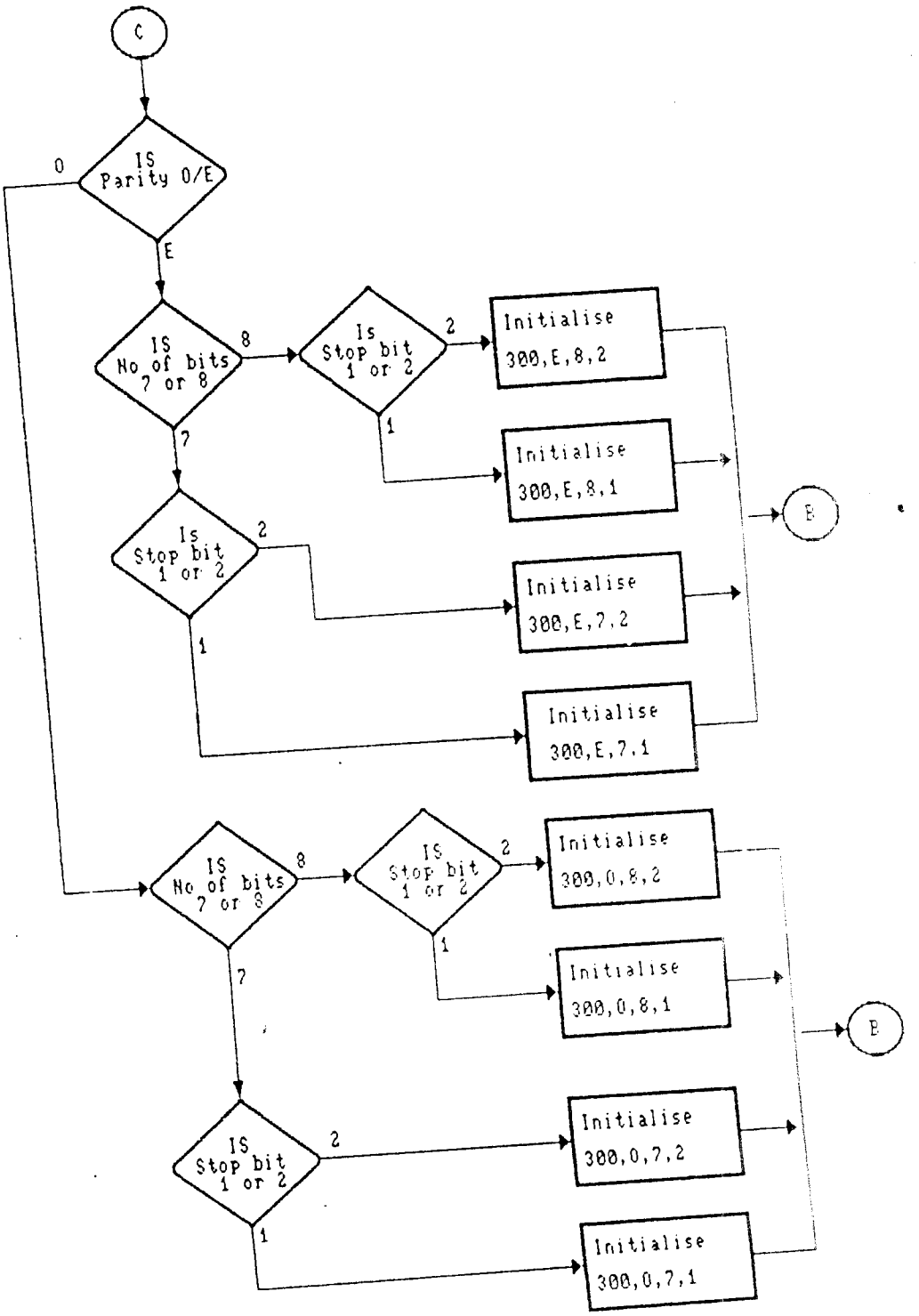
# Main Flow Chart for Transmitting Software



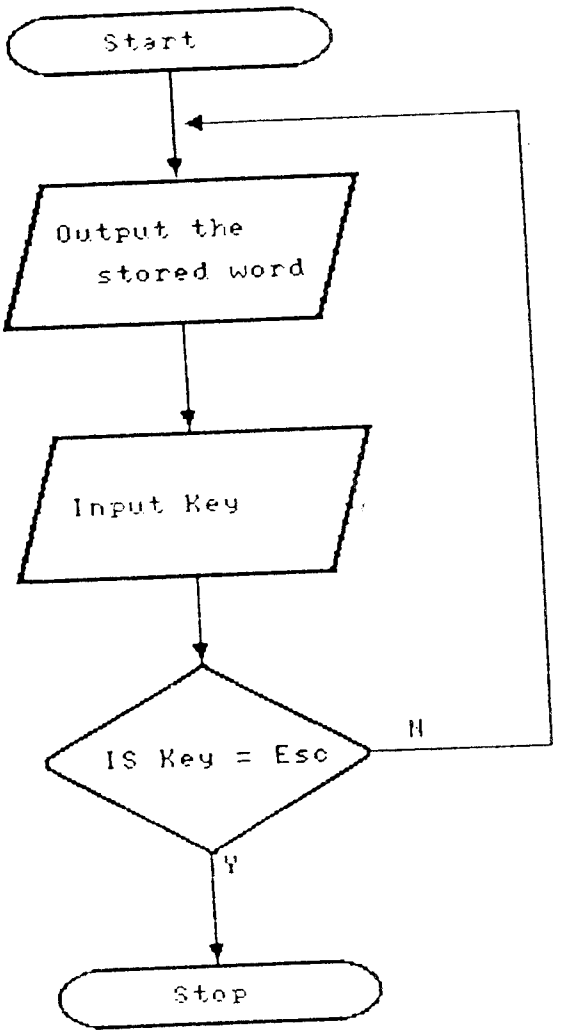
# Baud Rate Initialisation



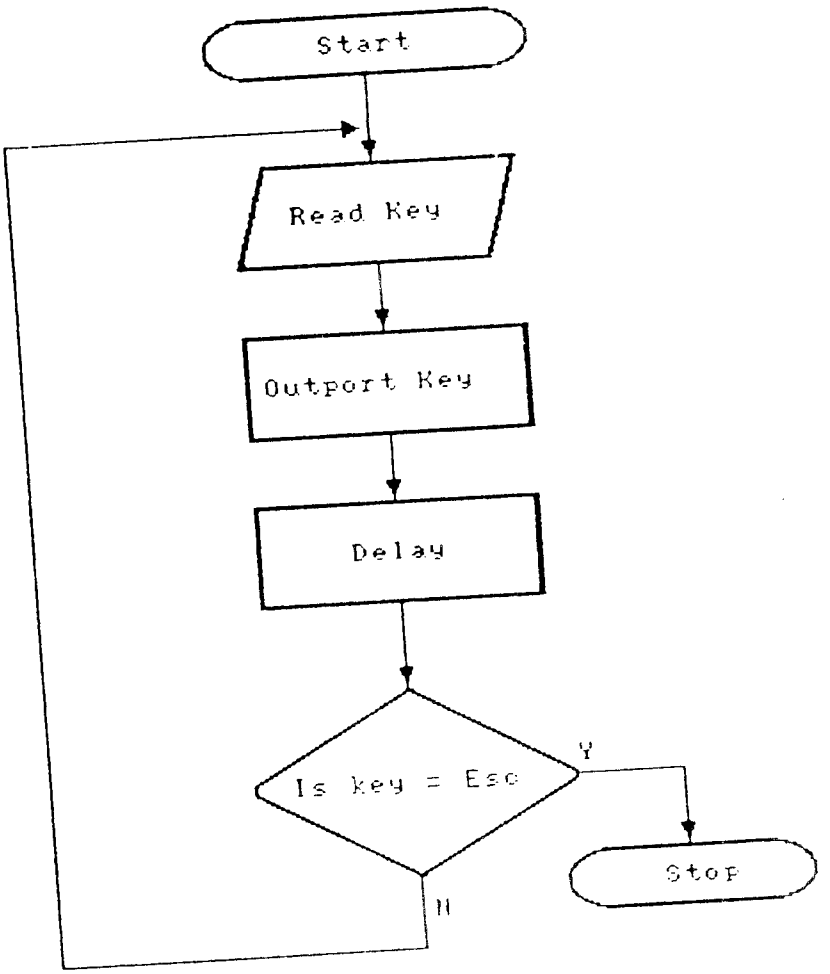
## When Baud Rate is 300



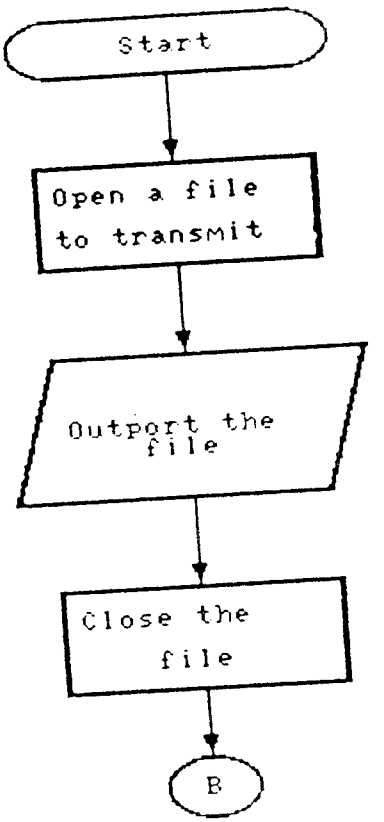
# Transmit a Name (Contineously)



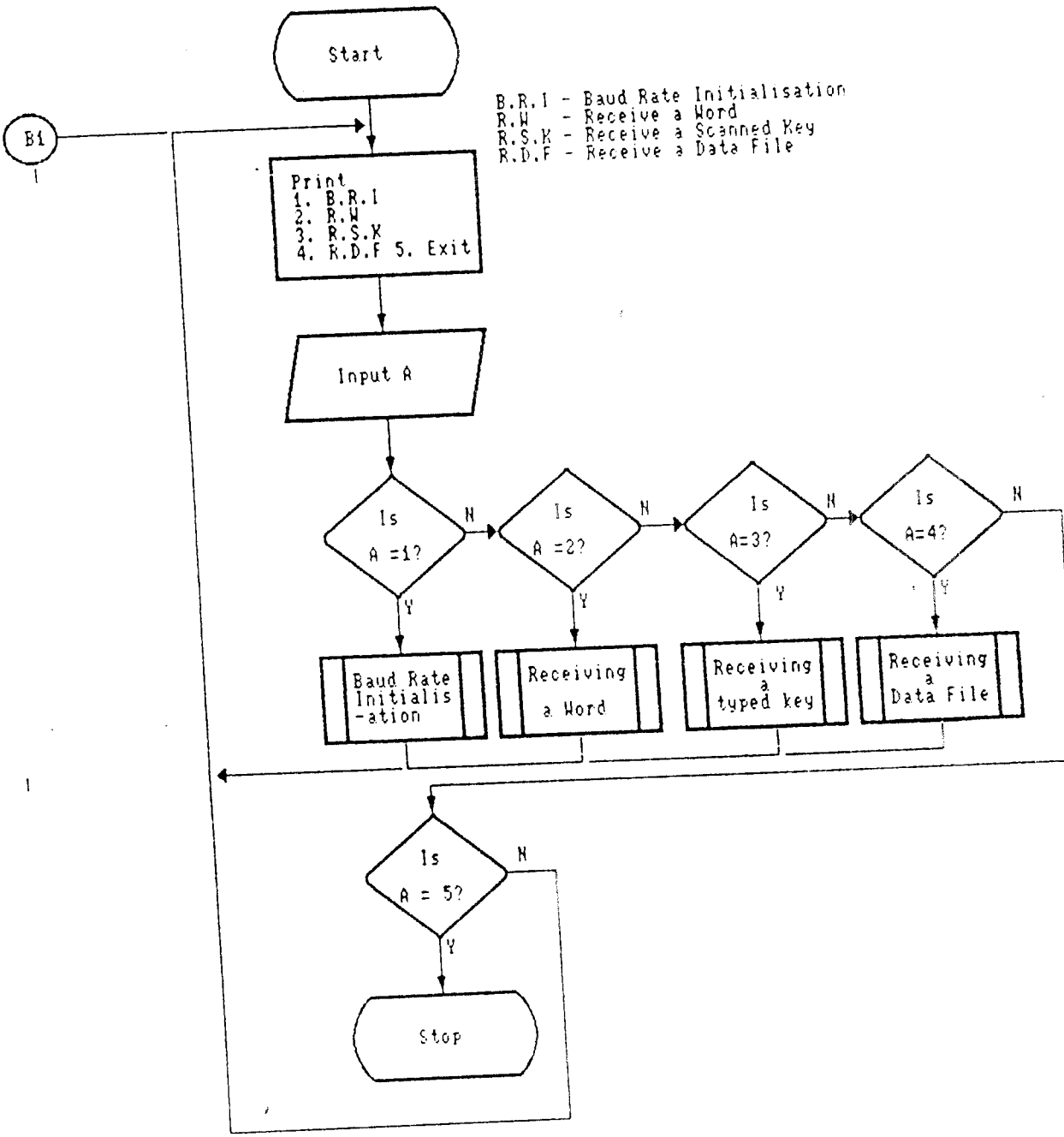
# Transmitting A scanned Key



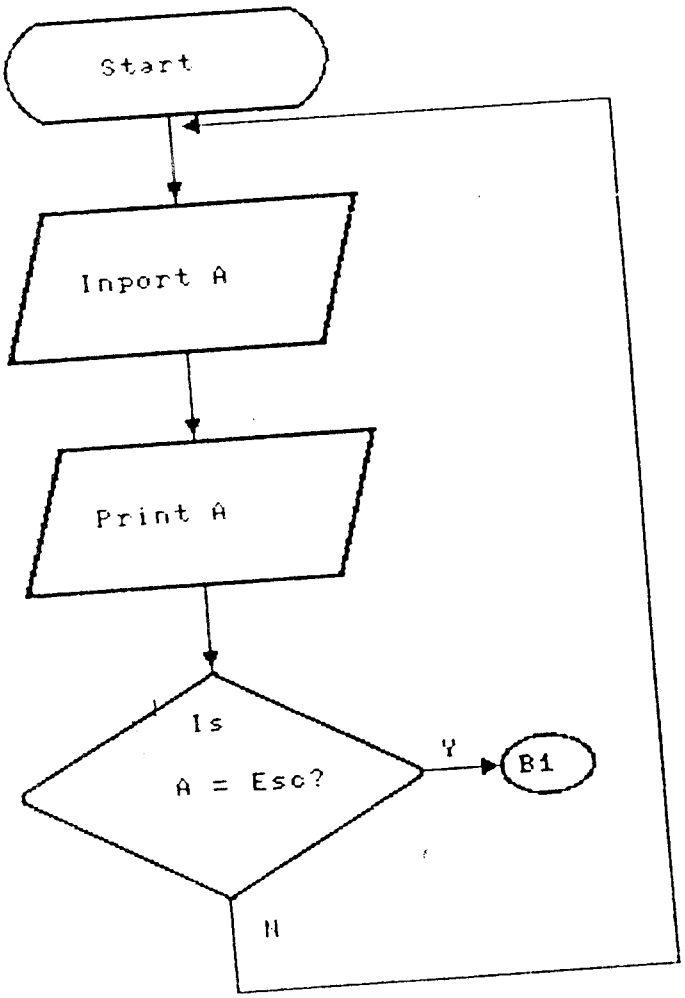
# Transmitting a Data File



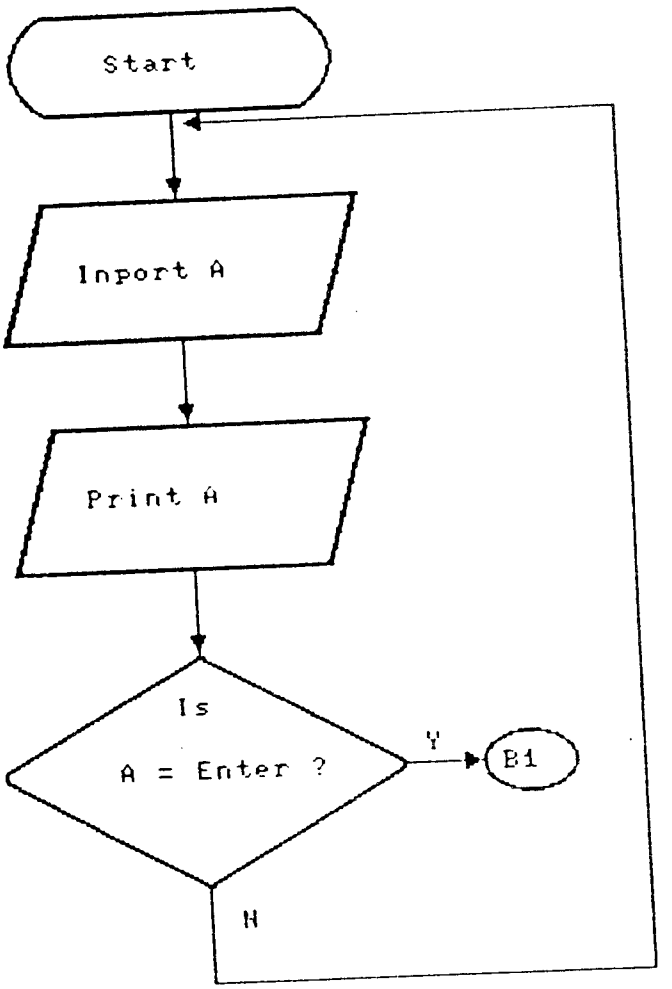
# Main flow chart for receiving data



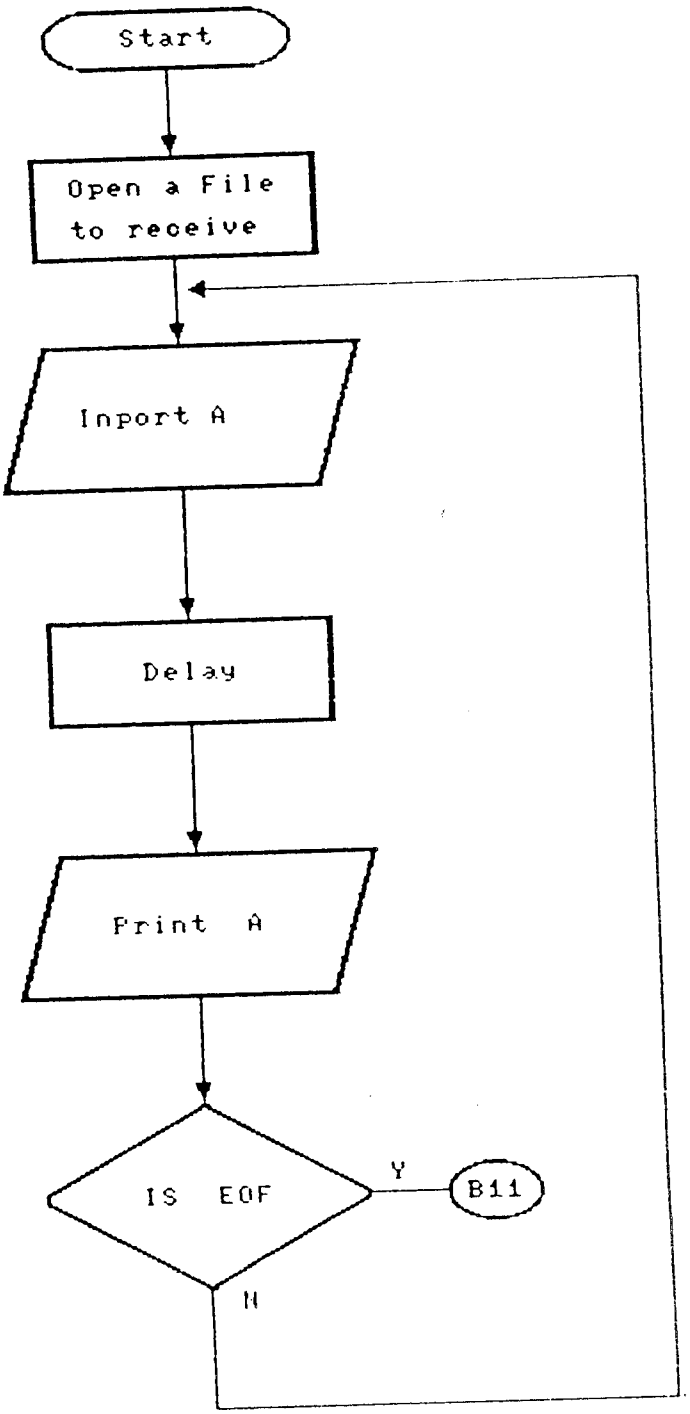
# Flow Chart to receive a name contineously



# Flow chart for receiving a scanned key



# Flow Chart to Receive a File



# SOFTWARE LISTING

# CHAPTER 7

## PROGRAM LISTING

```
/*   The Main Program For Transmission ....   transmit.c   */
  #include <process.h>
  #include <dos.h>
  #include <stdio.h>
  #include <conio.h>
  #include <graphics.h>
  #include "modemo.h"
  #include "MOD3.h"
  #include "outname.h"
  #include "outtype.h"
  #include "filetran.h"
  main()
    {     /* definitions  */
          int i,j;
          char c;
          podee();
          clrscr();
      tt:   textmode(C80);
          textattr(WHITE+(BLACK<<0));
          clrscr();
          window(2,1,78,24);
          textbackground(LIGHTBLUE);
```

```
gotoxy(1,6);
putch(200);
for (i=2;i<77;i++)
{
gotoxy(i,6);
putch(205);
}
gotoxy(78,6);
putch(188);
for (j=5;j>1;--j)
{
gotoxy(1,j);
putch(186);
}
for(j=5;j>1;--j)
{
gotoxy(77,j);
putch(186).
}
gotoxy(1,1);
putch(201);
for(i=2;i<77;++i)
{
gotoxy(i,1);
putch(205);
}
```

```
gotoxy(77,1);
putch(187);
gotoxy(1,7);
putch(218);
gotoxy(77,7);
putch(191);
for(i=8;i<23;++i)
{
gotoxy(1,i);
putch(179);
gotoxy(77,i);
putch(179);
}
gotoxy(1,23);
putch(192);
gotoxy(77,23);
putch(217);
for(i=2;i<77;++i)
{
gotoxy(i,7);
putch(196);
gotoxy(i,23);
putch(196);
}
gotoxy(23,3);
cprintf("PC    COMMMUNICATION    THROUGH    AC    POWER
```

```
LINES");
            textcolor(CYAN);
            gotoxy(25,10);
            cprintf("1. BAUD RATE INITIALIZATION  ");
            gotoxy(25,13);
            cprintf("2. TRANSMITTING A WORD ");
            gotoxy(25,16);
            cprintf("3. TRANSMITTING SCANNED KEY");
            gotoxy(25,19);
            cprintf("4. TRANSMITTING A DATA FILE ");
            gotoxy(25,22);
            cprintf("5. EXIT ");
            c=getch();
            if  ((c=='1') || (c=='2') || (c=='3') ||  (c=='4')
    || (c=='5'))
            switch (c)
            {
            case '1': initialize();/* Baud Rate Initialisation
     */
                      break;
             case '2': clrscr();
                       gotoxy(40,20);
                       textcolor(WHITE);
                       cprintf("Transmission is going on . .
      ");
                       word();  /* Transmitting a word */
```

```
                clrscr();
                break;
        case '3': textcolor(WHITE);
                scan(); /* Transmitting a scanned key */
                clrscr();
                break;
        case '4': clrscr();
                textattr(YELLOW+(CYAN<<4));
                dataf(); /* Transmission of a Data  File
*/
                clrscr();
                break;
        case '5': textattr(WHITE+(BLACK<<0));
                clrscr();
                gotoxy(30,20);
                cprintf("G O O D   B Y E .....!");
                sound(650);
                sleep(1);
                nosound();
                exit(0);
    }
   goto tt;
   }
```

```
podee()
{
int gd=MCGA,gm=0,c;
        initgraph(&gd,&gm,"");
        cleardevice();
        setbkcolor(RED);
        settextstyle(GOTHIC_FONT,0,4);
        setcolor(YELLOW);
        outtextxy(20,35,"PC COMMUNICATION");
        outtextxy(70,65,"THROUGH");
        outtextxy(120,95,"AC POWER LINES");
        getch();
        cleardevice();
        setbkcolor(BLUE);
        settextstyle(SANS_SERIF_FONT,0,3);
        setcolor(BROWN);
        outtextxy(5,20,"Guided By :");
        settextstyle(TRIPLEX_FONT,0,2);
        outtextxy(35,50,"Miss.P. Supriya");
        getch();
        cleardevice();
        setbkcolor(BROWN);
        setcolor(BLUE);
        settextstyle(GOTHIC_FONT,0,3);
        outtextxy(10,10,"Project Done By :");
        outtextxy(60,40,"K.Ganesh");
```

```
        outtextxy(50,70,"** K.Kalaiselvi");
        outtextxy(40,100,"*** P.Kamalakkannan");
        getch();
        closegraph();
}
```

```
/*---------- PROGRAM FOR BAUD RATE INITIALIZATION -------*/

        /*---------- File Name  :  MOD3.H  ----------*/

initialize()
      {
        int i=0,j=0,baud,no,st;
        char par[10];
        clrscr();
        textmode(C80);
        textattr(WHITE+(BLACK<<4));
        clrscr();
        textattr(WHITE+(RED<<4));
        window(2,1,78,24);
        clrscr();
        gotoxy(1,6);
        putch(200);
        for (i=2;i<
        {
        gotoxy(i,6);
        putch(205);
        }
        gotoxy(78,6);
        putch(188);
        for(j=5;j>1;--j)
        {
```

```
        putch(186);
        }
        for(j=5;j>1;--j)
        {
        gotoxy(77,j);
        putch(186);
}
gotoxy(1,1);
putch(201);
for (i=2;i<77;++i)
{
gotoxy(i,1);
putch(205);
        }
        gotoxy(77,1);
        putch(187);
        gotoxy(1,7);
        putch(218);
        gotoxy(77,7);
        putch(191);
        for(i=8;i<23;++i)
             {
             gotoxy(1,i);
             putch(179);
             gotoxy(77,i);
```

```
gotoxy(1,23);
putch(192);
gotoxy(77,23);
putch(217);
for(i=2;i<77;++i)
{
gotoxy(i,7);
putch(196);
gotoxy(i,23);
putch(196);
}
textcolor(WHITE+BLINK);
gotoxy(23,3);
cprintf("PC   COMMUNICATION   THROUGH   AC   POWER
LINES");
textcolor(CYAN);
gotoxy(4,9);
cprintf("Baud Rate Required  (150/300)?  : ");
cscanf("%d",&baud);
gotoxy(4,12);
cprintf(" Type Of Parity   (O/N)?          : ");
cscanf("%s",par);
gotoxy(4,15);
cprintf("Number Of Bits   (7/8)            : ");
cscanf("%d",&no);
gotoxy(4,18);
```

```
    cscanf("%d",&st);
    getch();
    gotoxy(50,15);
    clrscr();
    textattr(WHITE+(BLACK<<0));
    clrscr();
    setdisk(0);
if (baud==150)
    {
    if(par=='o')
      {
        switch (no)
        {
         case 7:
                  {
                  if(st==1)
                    {
                    system("mode com1:150,o,7,1,p");
                    setdisk(2);
                    break;
                    }
                    else
                         {
                         system("mode
com1:150,o,7,2,p");
                         setdisk(2);
```

```
                    break;
                     }
                  }
            case 8:
                  {
                  if(st==1)
                    {
                    system("mode com1:150,o,8,1,p");
                    setdisk(2);
                    break;
                     }
                     else
                          {
                          system("mode
com1:150,o,8,2,p");
                           setdisk(2);
                           break;
                           }

               }
          }
      else
          {
            switch (no)
            {
```

```
case 7:
        {
        if(st==1)
          {
          system("mode com1:150,n,7,1,p");
          setdisk(2);
          break;
          }
          else
              {
              system("mode
com1:150,n,7,2,p");
              setdisk(2);
              break;
              }
          }
case 8:
        {
        if(st==1)
          {
          system("mode com1:150,n,8,1,p");
          setdisk(2);
          break;
          }
          else
              {
```

```
            system("mode com1:150,n,8,2,p");
            setdisk(2);
            break;
                    }

                }
        }
        }
        }
else
        {
            if(par  o )

    switch (no)
    {
     case 7:
              {
              if(st==1)
                 {
                 system("mode com1:300,o,7,1,p");
                 setdisk(2);
                 break;
                 }
                 else
                      {
                      system("mode
```

```
                    setdisk(2);
                    break;
                    }
                  }
            case 8:
                  {
                  if(st==1)
                    {
                    system("mode com1:300,o,8,1,p");
                    setdisk(2);
                    break;
                    }
                    else
                        {
                        system("mode
com1:300,o,8,2,p");
                        setdisk(2);
                        break;
                        }
                    }
                }
            )
          else
              {
                switch (no)
```

```
case 7:
        {
        if(st==1)
          {
          system("mode com1:300,n,7,1,p");
          setdisk(2);
          break;
          }
          else
              {
              system("mode
com1:300,n,7,2,p");
              setdisk(2);
              break;
              }
          }
case 8:
        {
        if(st==1)
          {
          system("mode com1:300,n,8,1,p");
          setdisk(2);
          }
        }
```

```
        }
        }
        getch();
}
```

```
/*------  PROGRAM TO TRANSMIT A WORD CONTINEOUSLY  -----*/
       /*-------  File Name  :  OUTNAME.H  ---------*/

word ()
{
        int i,q;
        char a,b,c,d,e,f,g,h,j,k,l,m,n;
        void fool();
        for (q=1;q<20;q++);
        (
                a='G';
                i=a;
                outport(0x3f8,i);
                fool();
                b='O';
                i=b;
                outport(0x3f8,i);
                fool ();
                c='D';
                i=c;
                 outport(0x3f8,i);
                fool ();
                d=' ';
                i=d;
                 outport(0x3f8,i);
                fool ();
                e='I';
```

```
outport(0x3f8,i);
fool ();
f='S';
i=f;
 outport(0x3f8,i);
 fool ();
 g=' ';
 i=g;
 outport(0x3f8,i);
  fool ();
  h='G';
  i=h;
   outport(0x3f8,i);
   fool ();
   j='R';
   i=j;
    outport(0x3f8,i);
    fool ();
    k='E';
    i=k;
     outport(0x3f8,i);
     fool ();
     l='A';
     i=l;
      outport(0x3f8,i);
      fool ();
```

```
        i=m.
        outport(0x3f8,i);
        fool();
        n=' ';
        i=n;
        outport (0x3f8,i);
        fool();
        }
        }
void fool()
{
delay(1500);
}
```

```
/*---------- PROGRAM TO TRANSMIT A TYPED KEY --------*/

   /*---------- File Name  :  OUTTYPE.H ----------*/

scan ()
     {
       int i,k;
       char c;
       clrscr ();
       do
        {
         outport (0x3f8,0);
         c=getch();
         i=c;
         outport (0x3f8,i);
         putch(c);
         delay (500);
         outport(0x3f8,0);
         for (k=1;k<168;k++);
        }
       while (i != 13);
     }
```

```
/* ---------  PROGRAM FOR TRANSMITTING A DATA FILE --------*/
/* ----------     FILETRAN.H     ------------  */
dataf()
{
    FILE * fpt;
    int i=2, a;
    char d;
    fpt = fopen ("kct.dat", "r");
    while (!feof(fpt))
    {
        d=getc(fpt);
        a=d;
        outport(0x3f8,a);
        printf ("%c",d);
        delay (200);
     }
     for(i=0;i<=2;i++)
         outport(0x3f8,0x1a);
         fclose (fpt);
    }
```

```
/* The main program for receiving transmitted data  */

   /* Receive.c    */

   #include <process.h>
   #include <dos.h>
   #include <stdio.h>
   #include <conio.h>
   #include <graphics.h>
   #include "modemo.h"
   #include "MOD3.h"
   #include "inname.h"
   #include "intype.h"
   #include "filerece.h"
   main()

{
      int i,j;
      char c;
      podee();
      clrscr();
     tt:    textmode(C80);
      textattr(WHITE+(BLACK<<0));
      clrscr();
      window(2,1,78,24);
      textbackground(LIGHTBLUE);
      textcolor(WHITE);
      clrscr();
```

```
putch(200);
for(i=2;i<77;i++)
{
gotoxy(i,6);
putch(205);
}
gotoxy(78,6);
putch(188);
for (j=5;j>1;--j)
{
gotoxy(1,j);
putch(186);
}
for(j=5;j>1;--j)
{
gotoxy(77,j);
putch(186);
}
gotoxy(1,1);
putch(201);
for(i=2;i<77;++i)
{
gotoxy(i,1);
putch(205);
}
```

```
putch(187);
 gotoxy(1,7);
 putch(218);
 gotoxy(77,7);
 putch(191);
 for(i=8;i<23;++i)
 {
   gotoxy(1,i);
   putch(179);
   gotoxy(77,i);
   putch(179);
 }
   gotoxy(1,23);
   putch(192);
   gotoxy(77,23);
   putch(217);
   for(i=2;i<77;++i)
   {
   gotoxy(i,7);
   putch(196);
   gotoxy(i,23);
   putch(196);
   }
   gotoxy(23,3);        /*   Menu   */
   cprintf("PC COMMUNICATION THROUGH AC POWER LINES");
```

```
      cprintf("1. BAUD RATE INITIALIZATION");
      gotoxy(25,13);
      cprintf("2. RECEIVING A WORD");
      gotoxy(25,16);
      cprintf("3. RECEIVING THE PRESSED KEY");
      gotoxy(25,19);
      cprintf("4. RECEIVING A DATA FILE");
      gotoxy(25,22);
      cprintf("5. EXIT");
      c=getch();
      if  ((c=='1')  || (c=='2') || (c=='3') ||  (c=='4')  ||
(c=='5'))
       switch (c)
       {
       case '1': initialize(); /* Baud Rate Initialisation */
                 break;
        case '2': clrscr();
                  gotoxy(1,1);
                  word1();    /* Receiving the transmitted  word
 */
                  clrscr();
                  break;
         case '3': clrscr();
                   textcolor(WHITE);
                   scan1();  /* Receiving the typed key  */
                   clrscr();
```

```
        case '4': clrscr();
                  textattr(YELLOW+(CYAN<<4));
                  dataf1();  /*  Receiving the trasmitted  data
file */
                  clrscr();
                  break;
          case '5': textattr(WHITE+(BLACK<<0));
                  clrscr();
                  gotoxy(30,20);
                  cprintf(" G O O D  B Y E  ....!");
                  sound(550);
                  sleep(1);
                  nosound();
                  exit(0);
            }
        goto tt;
        }
```

```
/* ------ PROGRAM FOR RECEIVING A WORD CONTINEOUSLY ---- */
     /* ------  File Name :  INNAME.H  ---------------*/

word1()
{
        int i,k;
        char c;
        for(k=1;k<260;++k)
        {
            i=inport(0x3f8);
            c=i;
            printf("%c",c);
            delay(1575);
         }
   }
```

```
/*--------  PROGRAM FOR RECEIVING A SCANNED  KEY ------*/
   /*---------  File Name  :  INTYPE.H  ----------*/

scan1()
{
int  a;
  11: a = inport(0x3f8);
      if (a==0) goto  rr;
      printf("%c",a);
   rr: delay(500);
      if (a==13) exit(0);
      goto 11;
 }
```

```
/*      -------        File Name  :  FILERECE.H  -------   */
dataf1()
{
FILE *frt;
int i,a;
char l;
frt = fopen("samp.dat","w");/*Opening a file for reception
while((a=inport(0x3f8)) != 0x1a)
{
        printf("%c",l);
        delay(200);
        l=a;
//      putc(l,frt);
        fputc(l,frt);
        }
fclose(frt);
}
```

## CONCLUSION

The hardware circuitry has been fabricated, using the transceiver IC and other possible components, RS-232C is the interface link between the hardware and software. The software has been developed in 'C' language.

The pulse transmitted by the transceiver in the transmit mode has been received by the other transceiver which is in the receive mode. The pulse has been observed on the CRO as a test for the hardware functioning. By using the software - the data fed as input to one PC is obtained as o/p in the other PC - the two PC's paving the way for communication.

By boosting the carrier signal, communication between PC's can be effected for long distance.

An improvement that can be made in our system is to increase the baud rate of transmission, so that audio signal transmission can be done.

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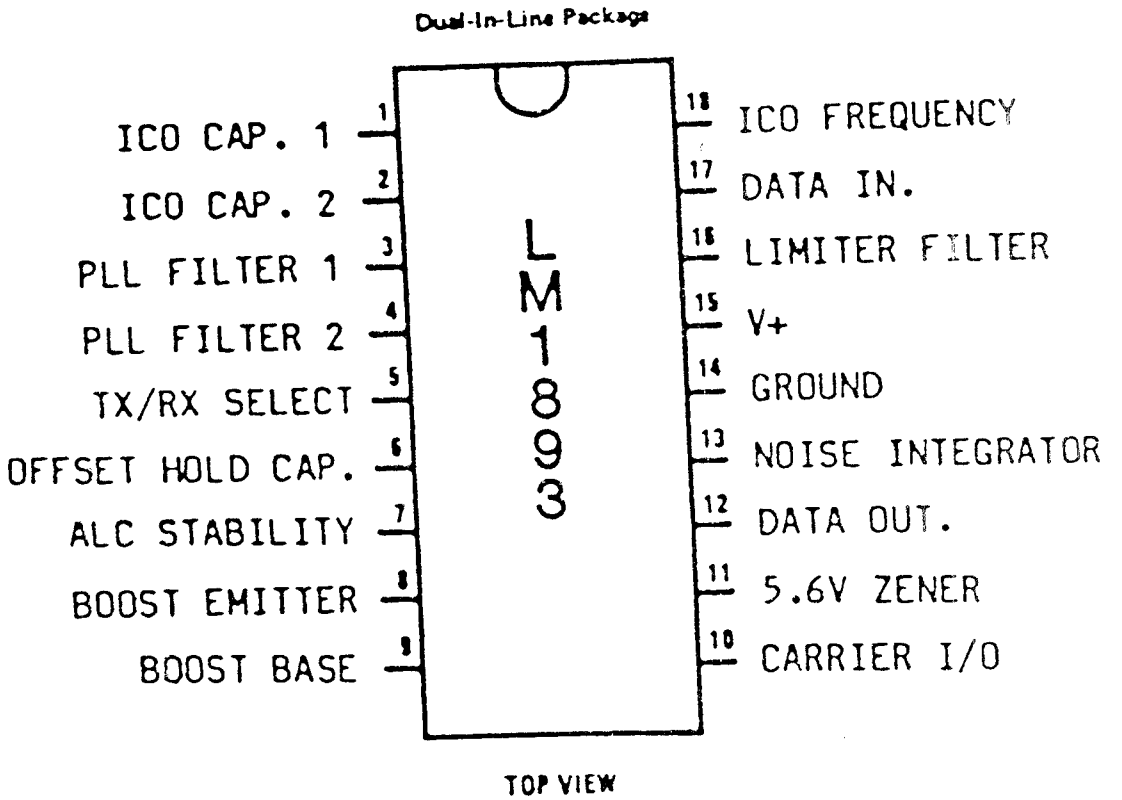



PIN DETAILS OF LM 1893.

## Absolute Maximum Ratings

| | | |
|---|---|---|
| Supply voltage | | 30 V |
| Voltage on pin 12 | | 55 V |
| Voltage on pin 10 (note 1) | | 41 V |
| Voltage on pins 5 and 17 | | 40 V |
| 5.6 V DC zener current | | 100 mA |
| Junction temperature: | transmit mode | 150°C |
| | receive mode | 125°C |
| Maximum continuous dissipation, Ta=25°C, (note 2): | plastic DIP N | 1.66 W |
| Operating ambient temp. range | | -25 to 85°C |
| Storage temperature range | | -65 to 150°C |
| Lead temperature, soldering, 10 s. | | 300°C |

Note 1: Transients may reach above 60 V; see the transient peak voltage characteristic curve.
Note 2: The maximum power dissipation rating should be derated for device operation above 25°C to insure that the junction temperature remains below the maximum rating. Use a $\theta_{JA}$ of 75°C/W for the N package using a socket in still air. Consult the Application Information section for more detail.

## General Electrical Characteristics (note 3)

The test conditions are: V+=18 V and $F_0$=125 KHz, unless otherwise noted.

| # | Parameter | Conditions | Typical | Test Limit (note 4) | Design Limit (note 5) | Limit Units |
|---|---|---|---|---|---|---|
| 1 | 5.6 V Zener voltage, $V_Z$ | Pin 11, $I_Z$=2 mA | 5.6 | 5.2<br>5.9 | | V min.<br>V max. |
| 2 | 5.6 V Zener resistance, $R_Z$ | Pin 11, $R_Z=(V_Z@10mA-V_Z@1mA)/(10mA-1mA)$ | 5 | | | Ohm |
| 3 | Carrier I/O peak survivable transient voltage, $V_{OT}$ | Pin 10, discharge 1 µF cap. charged to $V_{OT}$ | 80 | 60 | | V max. |
| 4 | Carrier I/O clamp voltage, $V_{OC}$ | Pin 10, $I_{OC}$=10 mA, RX mode | 44 | 41<br>50 | | V min.<br>V max. |
| 5 | Carrier I/O clamp resistance, $R_{IO}$ | Pin 10, $I_{OC}$=10 mA | 20 | | | Ohm |
| 6 | TX/$\overline{RX}$ low input voltage, $V_{IL}$ | Pin 5 | 1.8 | 0.8 | | V max. |
| 7 | TX/$\overline{RX}$ high input voltage, $V_{IH}$ | Pin 5 (note 9) | 2.2 | 2.8 | | V min. |
| 8 | TX/$\overline{RX}$ low input current, $I_{IL}$ | Pin 5 at 0.8 V | -2 | -20<br>0 | | µA min.<br>µA max. |
| 9 | TX/$\overline{RX}$ high input current, $I_{IH}$ | Pin 5 at 40 V | $10^{-4}$ | 0<br>10 | | µA min.<br>µA max. |
| 10 | RX-TX switch-over time, $T_{RT}$ | Time to develop 63% of full current drive through pin 10 | 10 | | | µs |
| 11 | TX-RX switch-over time, $T_{TR}$ | 1 bit time $T_B=1/(2F_{DATA})$ Time $T_{TR}$ is user controlled with $C_M$, see Apps. Info. | 2 | | | bit |
| 12 | ICO initial accuracy of $F_0$ | TX mode, $R_0$ = 6.7 KOhm, $C_0$ = 560 pF | 125 | 113<br>137 | | KHz min.<br>KHz max. |
| 13 | ICO temperature coefficient of $F_0$ | TX mode, $(F_{0MAX}-F_{0MIN})/(T_{JMAX}-T_{JMIN})$ | (±200) | | | PPM/°C |
| 14 | Temperature drift of $F_0$ | TX mode, $-25\leq T_J\leq 150°C$ | (±2.0) | | (±5.0) | % max. |

## Transmitter Electrical Characteristics (note 3)

The test conditions are: V+=18 V and $F_0$=125 kHz unless otherwise noted. The transmit center frequency is $F_0$, FSK low is $F_1$, and FSK high is $F_2$.

| # | Parameter | Conditions | Typical | Test Limit (note 4) | Design Limit (note 5) | Limit Units |
|---|---|---|---|---|---|---|
| 15 | Supply voltage, V+, range | Meets Test 17 spec. at $T_J$=25°C and:<br>$\lvert(F_1[14V]-F_1[18V])/F_1[18V]\rvert<0.01$<br>$\lvert(F_1[24V]-F_1[18V])/F_1[18V]\rvert<0.01$ | (12) | 14<br>24 | (15)<br>(23) | V min.<br>V max. |
| 16 | Total supply current, $I_{QT}$ | Pin 15. Pin 12 high. $I_{QT}$ is $I_Q$ through pin 15 and the average current $I_{ODC}$ of the Carrier I/O through pin 10 | 42 | 59 | | mA max. |
| 17 | Carrier I/O output current, $I_O$ | 100 Ohm load on pin 10 | 70 | 45 | | mApp min. |
| 18 | Carrier I/O lower swing limit, $V_{ALC}$ | Pin 10. Set internally be ALC | 4.7 | 4.0<br>5.7 | | V min.<br>V max. |
| 19 | THD of $I_O$ (note 6) | Q of 10 tank driving 10 Ohm line<br>100 Ohm load, no tank | 0.6<br>5.5 | | (2.0)<br>9 | % max.<br>% max. |
| 20 | FSK deviation, $F_2-F_1$ | $(F_2-F_1)/([F_2+F_1]/2)$ | 4.4 | 3.8<br>5.2 | | % min.<br>% max. |
| 21 | Data In. low input voltage, $V_{IL}$ | Pin 17 | 1.7 | 0.8 | | V max. |
| 22 | Data In. high input voltage, $V_{IH}$ | Pin 17 (note 9) | 2.1 | 2.8 | | V min. |
| | | | | 1 | 10 | µA min. |

## eceiver Electrical Characteristics (note 3)

he test conditions are: V+=18 V, $F_0$=125 KHz, 2.2 deviation FSK, $F_{DATA}$=2.4 KHz, $V_{in}$=100 mVpp, in the receive mode, unless therwise noted.

| # | Parameter | Conditions | Typical | Test Limit (note 4) | Design Limit (note 5) | Limit Units |
|---|---|---|---|---|---|---|
| 25 | Supply voltage, V+, range | Functional receiver (note 7) | (11) | 13<br>30 | (13.5)<br>(28) | V min.<br>V max. |
| 26 | Supply current, $I_{QT}$ | $I_{QT}$ is pin 15 (V+) plus pin 10 (carrier I/O) current | 13 | 5<br>14 | | mA min.<br>mA max. |
| 27 | Carrier I/O input resistance, $R_{IO}$ | Pin 10 | 19.5 | 14<br>30 | | KOhm min.<br>KOhm max. |
| 28 | Max. data rate, $F_{MD}$ | Functional receiver (note 7) square-wave data, 2.4 kHz=4.8 kBaud | 10 | 4.8 | (2.4) | kBaud |
| 29 | PLL capture range, $F_C$ | $C_F$=100 pF, $R_F$=0 Ohm | ±40 | ±20 | | % min. |
| 30 | PLL lock range, $F_L$ | $C_F$=100 pF, $R_F$=0 Ohm | ±45 | ±20 | | % min. |
| 31 | Receiver input sensitivity, $S_{IN}$ | For a functional receiver (note 8)<br>Referred to chip side (pin 10) of the line-coupling XFMR: $F_0$=50 kHz<br>$F_0$=300 kHz<br>Referred to line side of XFMR: (assuming a 7.07:1 XFMR) $F_0$=50 kHz<br>$F_0$=300 kHz | 1<br>1<br>1<br>0.14<br>0.14<br>0.14 | 10 | | $mV_{RMS}$<br>$mV_{RMS}$<br>$mV_{RMS}$<br>$mV_{RMS}$<br>$mV_{RMS}$<br>$mV_{RMS}$ |
| 32 | Tolerable input dc voltage offset range, $V_{INDC}$ | Pin 10 lower than pin 15 by: | 2 | 0.1 | | V max. |
| 33 | Data Out. breakdown voltage | Pin 12, leakage I≤20 µA | 70 | 55 | | V min. |
| 34 | Data Out. low output, $V_{OL}$ | Pin 12, sat. voltage at $I_{OL}$=5mA | 0.15 | 0.4 | | V max. |
| 35 | Time-domain filter current, $I_I$ | Pin 13 charge and discharge current | ±50 | ±35<br>±75 | | µA min.<br>µA max. |
| 36 | Offset hold cap. bias voltage, $V_{CM}$ | Pin 6 | 2.0 | 1.3<br>3.5 | | V min.<br>V max. |
| 37 | Offset hold capacitor max. drive current, $I_{MCM}$ | Pin 6. V(pin 3)-V(pin 4)=±250 mV | ±48 | ±25<br>±80 | | µA min.<br>µA max. |
| 38 | Offset hold bias current, $I_{OHB}$ | Pin 6, TX mode. Bias pin 6 as it self-biased during test 32. | 0.5 | | (-20)<br>(20) | nA min.<br>nA max. |
| 39 | Phase comparator current, $I_{PC}$ | Bias pins 3 and 4 at 8.5 V<br>$I_{PC}$=I(pin 3) + I(pin 4) | 100 | 50<br>150 | | µA min.<br>µA max. |
| 40 | Phase detector output resistance, $R_{PD}$ | Pins 3 and 4.<br>$R_{PD}$=(V@100µA-V@50µA)/(50µA) | 10 | 6<br>15 | | KOhm min.<br>KOhm max. |
| 41 | Phase detector demodulated oputput voltage, $V_{PD}$ | Pin 3 to 4, measured after filtering out the $2F_0$ component | 100 | 60<br>180 | | mVpp min.<br>mVpp max. |
| 42 | Fast offset cancel voltage "window" -to-$V_{PD}$ ratio, $V_W/V_{PD}$ | $V_{PIN3}$-$V_{PIN4}$ = ±$V_{WINDOW}$ + DC offset Drive for ±5 µA pin 6 current | 0.95 | 0.75<br>1.10 | | V/V min.<br>V/V max. |
| 43 | Power supply rejection, PSRR | $C_L$ = 0.1 µF. PSRR = CMRR. 120 Hz | 80 | | | dB min. |

Note 3: The values inside parenthesis () apply over the full operating temperature range after warmup for the specified suppl voltage range. All other numbers apply at $T_A$=$T_J$=25°C.
Note 4: Guaranteed and 100% production tested.
Note 5: Guaranteed (but not 100% production tested) over the temperature and supply voltage ranges. These limits are not use to calculate outgoing quality levels.
Note 6: Total harmonic distortion is measured using THD=[$I_{RMS}$(all components at or above $2F_0$)]/[$I_{RMS}$(fundamental)].
Note 7: Receiver function is defined as the error-free passage of 2 cycles of 50% duty-cycle 2.4 KHz square-wave data (4 seque tial 208 µs bits), with the first bit being a "1." All of the data transitions (edges) must fall within ±10% (±20.6 µs) their noise-free positions. RX time delay is minimized by using no impulse noise filter cap. $C_I$ for this test.
Note 8: During the sensitivity check, note 7 requirements are followed with these exceptions: (1) data rate $F_{DATA}$=1.2 KHz, ( all of the data transitions must fall within ±10% (±20.6 µs) of their noise-free positions, and (3), a time-domain filt capacitor ($C_I$) is used. The time delay of $C_I$ is 1/2 bit, or 208 µs ($C_I$ is approximately 6200 pF).
Note 9: For TTL compatibility, use a pull-up resistor to increase min. $V_{OH}$ to above 2.8 V.

# e Transmitter

entral to chip operation is the low TC of $F_0$ emitter-coupled oscillator. With proper $C_0$, the $F_0$ of the $V_{BE}$ amplitude triangle-wave oscillator output may vary from near DC to above 300 KHz. While $C_0$ may have any value, $C_0$ should be made above 10 pf so that parasitic capacitance is not dominant. Excessive or unbalanced common-mode-to-ground capacitance should be avoided. A low temperature coefficient (TC) of capacitance (<100 PPM/°C), such as a monolithic NP0 ceramic multilayer type, preserves low TC of $F_0$. Figure 6 finds a $C_0$ value given $F_0$.

## )

Resistor $R_0$ is used by the IC to generate a $V_{BE}/R$ related current that is multiplied by 2 to produce the 200 µA ICO control current that sets $F_0$. The control current TC "bucks" the $V_{BE}$ related tri-wave amplitude across $C_0$ to effect a low TC of $F_0$. Vary $R_0$ to trim $F_0$, within limits. Raising $F_0$ more than 20% above its untrimmed value by means of decreasing $R_0$ more than 20% is not recommended. Low $R_0$, and so high control current, risks ICO saturation and poor IC under worst-case conditions. Raising $R_0$ reduces the demodulated signal amplitude from the phase detector; raising $R_0$ by more than a factor of 2 (1 octave) is not recommended.

Since lower TC pots are relatively costly, it is recommended that $R_0$ be made up of a 5.6 K fixed (<100 PPM/°C) resistor with a 2 KOhm (<250 PPM/°C) series pot.

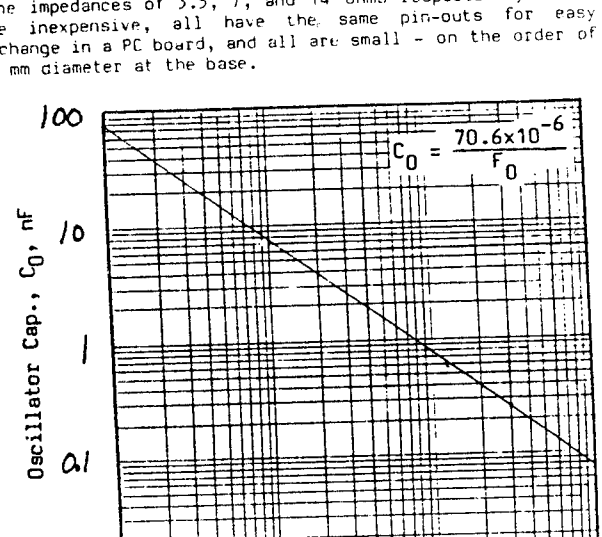
## $C_A$ and $R_A$

Components $C_A$ and $R_A$ control the dynamic characteristics of the transmitter output envelope. Their values are not critical. Use the values given in figure 5. $C_A$ and $R_A$ are functions of loaded $T_1$ tank Q, $F_0$, $F_{DATA}$, and line impulse noise. Any changes mode in $C_A$ and $R_A$ should be made based on empiracle measurements of a CCT on the line. Roughly, $C_A$ acts as an ALC pole and $R_A$ an ALC zero.

## $T_1$

At this point, the CCT system designer may choose to use one of the recommended transformers or to design $T_1$ oneself. Consult "The Coupling Transformer" section to help with the design of $T_1$ if a new or boost-capable transformer is needed. The recommended 125 KHz transformer functions with an $I_0$ of up to 600 mApp.

It is recommended that CCT systems use the recommended transformers, described in figure 7, for $T_1$. The 3 transformers are optimized for use in the ranges of 50-100 KHz, 100-200 KHz, and 200-400 KHz with unloaded Q's ($Q_U$) of about 35, and loaded Q's ($Q_L$) of about 12. Three secondary taps are supplied with nominal 7.07, 10, and 14.1 turns ratios (N) to drive industrial and residential power line impedances of 3.5, 7, and 14 ohms respectively. All are inexpensive, all have the same pin-outs for easy exchange in a PC board, and all are small - on the order of 10 mm diameter at the base.



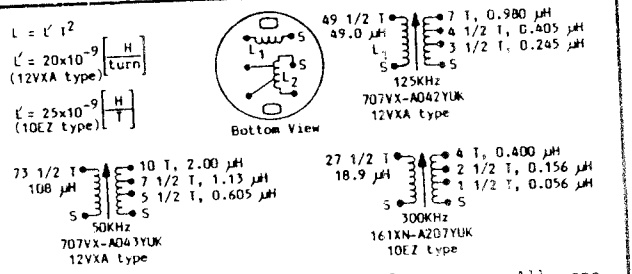




FIGURE 7. The recommended $T_1$ transformers. All are available through Toko America, 5520 W. Touhy Ave., Skokie, IL, 60077, 312-677-3640 (use the part numbers listed above).

## $C_Q$

Tank resonant frequency $F_0$ must be correct to allow passage of transmitter signal to the line. Use figure 8 to find $C_Q$'s value. Trimming $F_0$ to equal $F_0$ is done with $T_1$'s trimming slug. The inductance of $T_1$ has a TC of +150 PPM/°C which may be cancelled by using a -150 PPM/°C cap such as polystyrene. Since circulating current in the tank is 1/4 $A_{RMS}$, $C_Q$ should have a low series resistance (a 1 Ohm series resistance is too much). Polypropelene caps. are excellent, "orange drop" mylars are adequate, while many other mylars are inadequate. A 100 V rating is needed for transient protection.

## $C_C$

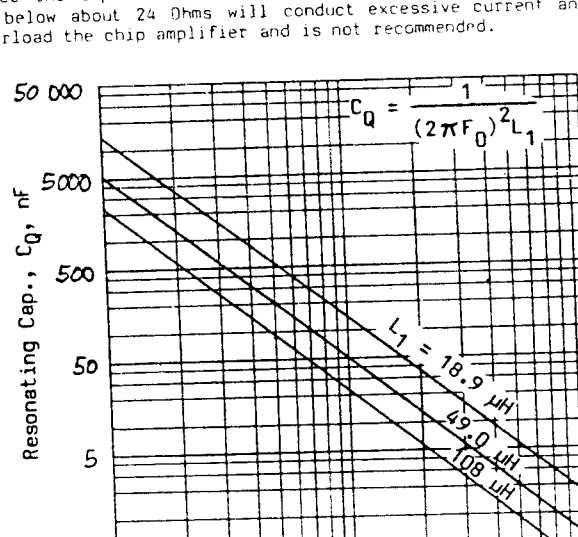
Capacitor $C_C$'s primary function is to block the power line voltage from $T_1$'s line-side winding. Also, $C_C$ and $T_1$'s line-side winding comprise a LC highpass filter. The self-inductance of $T_1$ is far too low to support a direct line connection. $C_C$ must have a low enough impedance at $F_0$ to allow $T_1$ to drive transmitted energy onto the line. To drive a 14 Ohm power line, the impedance of $C_C$ should be below 14 Ohm.

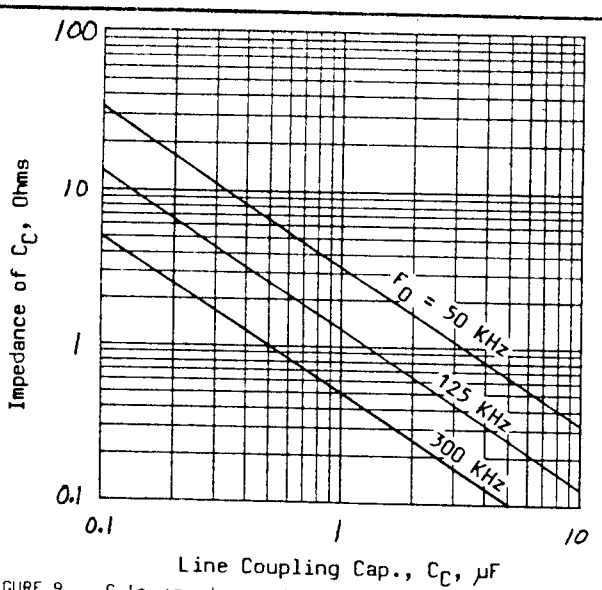
Use figure 9 and 10 to find the reactive impedance of $C_C$ to check that it is less than the line impedance. Then check to see that the power line current is small enough to keep $T_1$ well out of saturation; the recommended transformers can withstand a 10 Amp-turn magnetizing force (1 Ap through the worst-case 10 turn line-side winding).

Caution is required when choosing $C_C$ to avoid series resonance of the series combination of $C_C$, the transformer inductance, and the reflected tank impedance. The low resistance of the network under series resonance will load the line, possibly decreasing range. For your particular line coupling circuit, measure for series resonance using some expected line impedance load.

## $R_B$

This base-bleed resistor turns $Q_B$ off quickly - important since the amplifier output swing is about 200 V/µs. A $R_B$ below about 24 Ohms will conduct excessive current and overload the chip amplifier and is not recommended.






IGURE 9. $C_C$'s impedance should be, as a rule-of-thumb, smaller than the lowest expected line impedance.

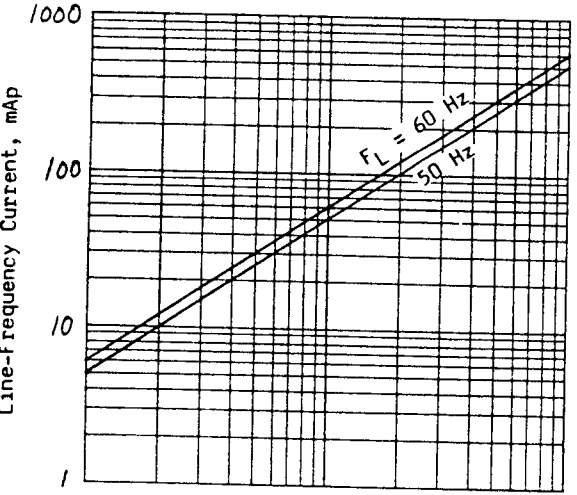
C

This resistor, in parallel with the internal 10 Ohm resistor, fixes the current gain of the output amplifier, and so the output current amplitude. Figure 11 gives output current and minimum AC current gain $h_{fe}$ for $Q_B$ when $R_G$ is used to boost output current.

B

The boost gain transistor $Q_B$ must be fast. Double-diffused devices with 50 MHz $F_T$'s work, slower transistors (epi-base types) do not preserve a sinusoidal waveform when $F_O$ is high or oscillate. $Q_B$ must have a certain minimum $h_{fe}$ for given boost levels, as shown in figure 11. Figure 12 shows the power $Q_B$ must dissipate continuously operating with a shorted output. $BV_{CER}$ ($R = R_B$) must be 60 V or greater and $Q_B$ must have adequate SOA for transient survival.

Unfortunately, potentially damaging transient energy passes through transformer $T_1$ onto the Carrier I/O pin (instantaneous power of greater than 1 KW has been measured using the recommended transformers). For self protection, the Carrier I/O has an internal 44 V voltage clamp with a 20 Ohm series resistance. A parallel low impedance 44 V external transient suppression diode will then conduct the lion's share of any current when transients force the Carrier I/O to a high voltage.



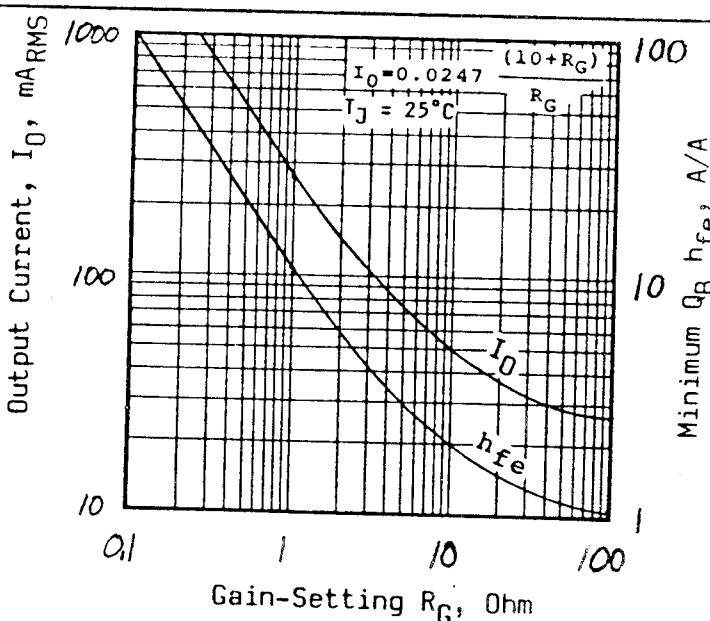




FIGURE 11. Output amplifier current and required min. $Q_B$ $h_{fe}$ versus gain-setting resistor $R_G$.

$Z_T$ must be used unless some precaution is taken to protect the Carrier I/O pin from line transients or transients caused when stored line energy in $C_C$ is discharged by the random phase of power line connection and disconnection. Worst case, $C_C$ may discharge a full peak-to-peak line voltage into the tuned circuit. Another way to reduce the need for $Z_T$ is by placing another magnetic circuit in the signal path that relies on a high, but easily saturated, permeability to couple a primary and secondary winding - a toroidal transformer for example Toroids cost more than $Z_T$.

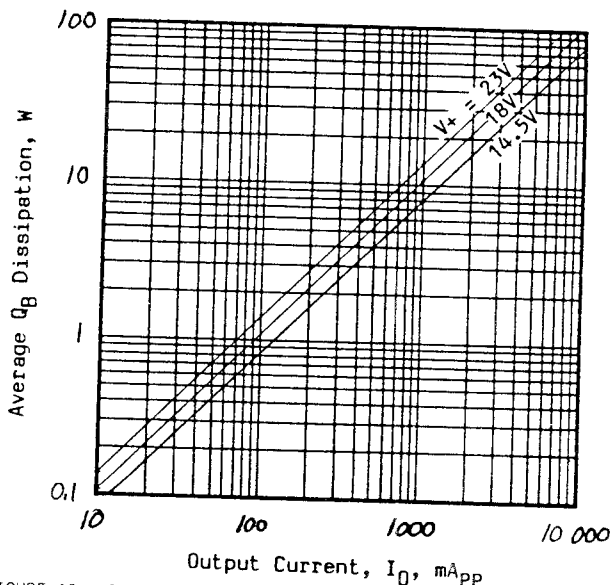



FIGURE 12. Boost transistor power dissipation versus amplifier output current.

| | |
|---|---|
| Breakdown Voltage | 44-49V @ 1mA |
| Maximum Leakage | 1µA @ 40V |
| Capacitance | 300pF @ 8V |
| Maximum Clamp Voltage | 64.5V @ 7.8A |
| Peak Non-Repetitive Pulse Power (REA Standard Exponential Pulse) | 10.2KW for 1us |
| Surge Current | |

Use an avalanche diode designed specifically for transient suppression - they have orders of magnitude higher pulse power capability than standard avalanche diodes rated for equal DC dissipation. Metal oxide varistors have not proven useful because of their inferior clamping coefficient. Specifications for an example minimum diode are given in figure 13.

## The Receiver

The receiver and transmitter share components $C_C$, $T_1$, $C_Q$, $R_T$, $Z_T$, $C_Q$, $R_Q$, and peripheral supply and bias components that are not in need of change for RX mode operation. Values for the balance of the components are now found.

## Line-Frequency Rejection

To use the ultimate sensitivity of the device, fully 110 dB of 115 V, 60 Hz attenuation is required between the line and the limiter amplifier output. Using the circuit topology of figure 4, the combined attenuation of the $C_C/T_1$ highpass, the tuned transformer, and the bandpass filter attenuation of the limiter amplifier give far more line rejection than the above-stated minimums. However, if some other CCI line coupling circuit is used, line rejection will become important to the system designer.

Receiver input power supply rejection (PSRR) and common-mode rejection (CMRR) are one-in-the-same using the supply-referenced signal input of figure 4. Ripple swings both differential inputs of the Norton amp. equally, while the single-ended input signal swings only the positive input. Overall PSRR consists of the input CMRR (set by the input stage component matching) and the ripple-frequency attenuation of the input amplifier bandpass response that passes carrier frequency but stops low frequencies. A typical 1% resistor and 1 mV n-p-n mirror offsets give 26 dB of attenuation, the bandpass gives 54 dB 120 Hz attenuation, for an overall 80 dB PSRR to allow tens of volts of ripple before impacting ultimate sensitivity.

### $C_C$

A value was chosen earlier. Knowing $T_1$'s secondary inductance allows a check of LC line attenuation using figure 14.

### $C_L$

The Norton input limiter amplifier has a bandpass filter for enhanced receiver selectivity, noise immunity, and line frequency rejection. The nominal response curve for $F_0$ = 50 KHz is shown in figure 15. The 300 KHz pole is fixed. The 50 KHz pole is set by $C_L$'s value. After $C_L$ is found, the resulting line frequency attenuation is found for the bandpass filter.

Use figure 15 to find a $C_L$ value given $F_0$. The approximate line frequency attenuation of the bandpass filter may then be found in figure 16. Figure 15 returns a value for $C_L$ 33% larger than nominal, giving a low frequency pole 33% low to allow for component tolerances.

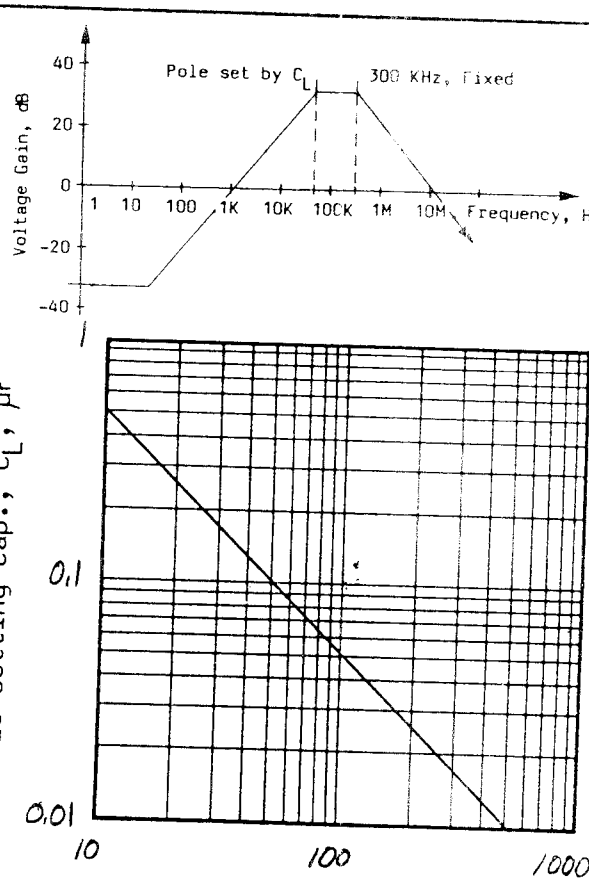
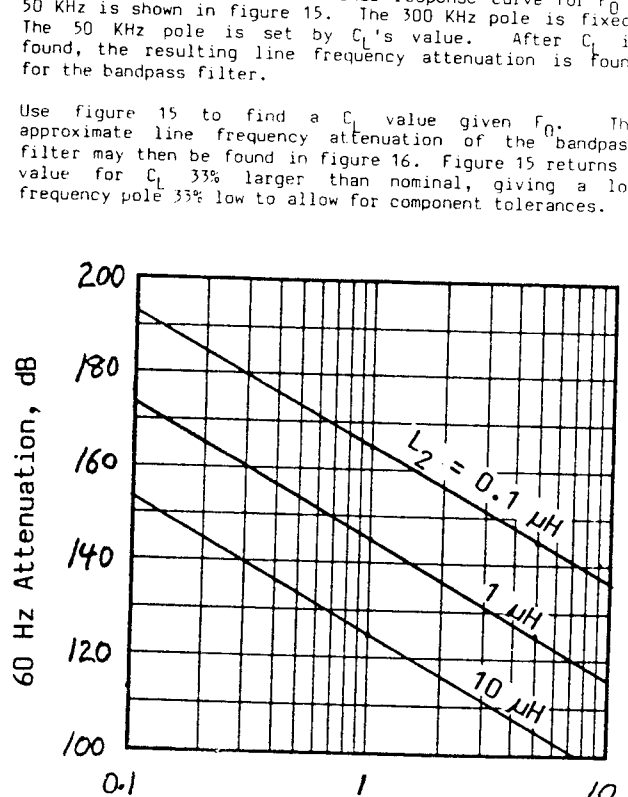
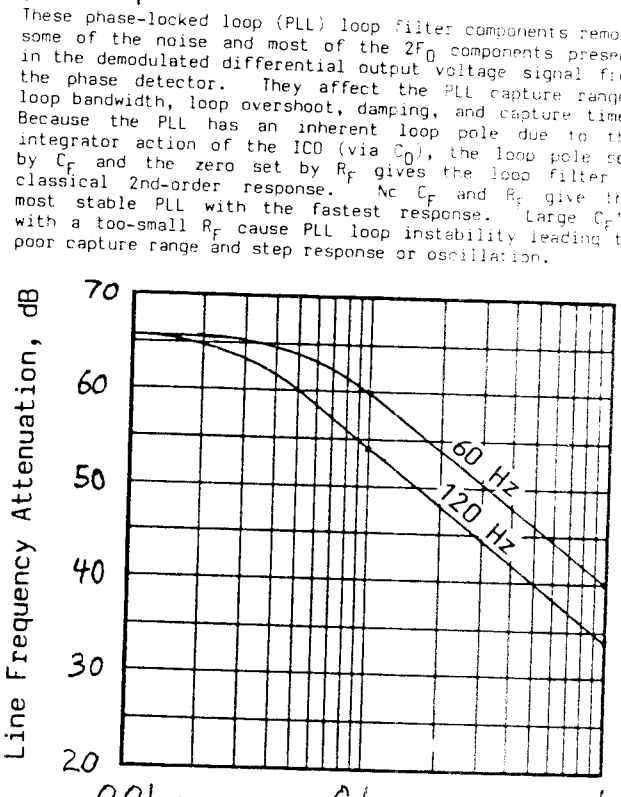


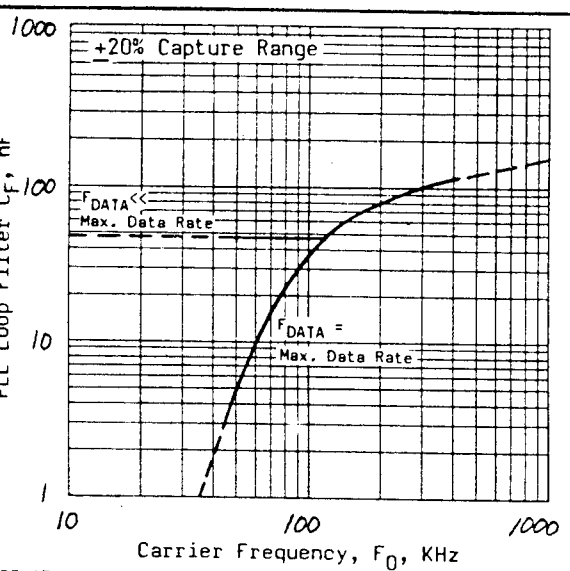

FIGURE 15. Given $F_0$, $C_L$ is found. Also shown is the input amplifier's small signal amplitude response.

### $C_F$ and $R_F$

These phase-locked loop (PLL) loop filter components remove some of the noise and most of the $2F_0$ components present in the demodulated differential output voltage signal from the phase detector. They affect the PLL capture range, loop bandwidth, loop overshoot, damping, and capture time. Because the PLL has an inherent loop pole due to the integrator action of the ICO (via $C_Q$), the loop pole set by $C_F$ and the zero set by $R_F$ gives the loop filter a classical 2nd-order response. No $C_F$ and $R_F$ give the most stable PLL with the fastest response. Large $C_F$'s with a too-small $R_F$ cause PLL loop instability leading to poor capture range and step response or oscillation.



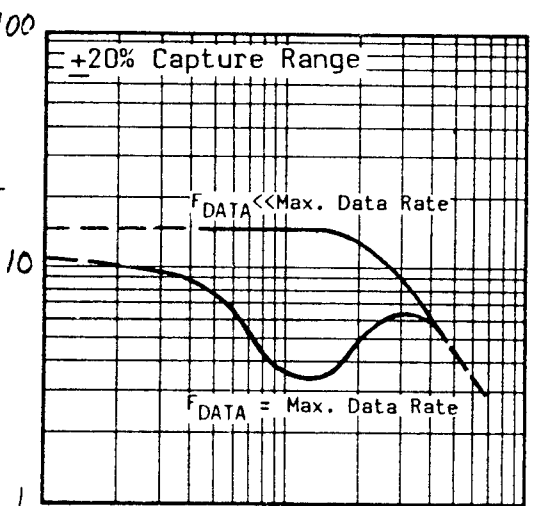






RE 17. Find $C_F$ given $F_0$. Figure 19 gives the maximum data rate.

lculation of $C_F$ and $R_F$ is quite difficult, involving t only the 2nd-order loop step response, but also the PLL n-dominant poles, the tuned transformer stepped-frequency sponse, and the RC lowpass step response (for data rates proaching 1 KHz). $C_F$ and $R_F$ values are best found piracly. Tolerance is not critical. Component values e selected to give the best possible impulse noise jection while preserving a ±20% capture range and wide ability margin. Figures 17 and 18 give $C_F$ and $R_F$ lues versus $F_0$.

te that $C_F$ and $R_F$ are a function of data rate only r high data rates and are not plotted against data rate - one might expect. The reason for this is important to derstand if the CCT system designer wishes to find $C_F$ d $R_F$ empiracly. Data signal is, loosely speaking, ssed through the PLL loop and is therefore potentially enuated if the loop bandwidth is on the order of the 3rd rmonic of the data rate, or less. Overall loop bandwidth held as low as possible for maximum noise rejection ile passing the data. Loop bandwidth is roughly pportional to the geometric mean of the unfiltered loop ndwidth and the filter pole set by $C_F$. Therefore, $C_F$ related to data rate. Unfortunately, the loop capture nge falls to critically low values when large enough lues of $C_F$ are used to reduce loop bandwidth down to 100's of Hz range, for low data rates. The obvious way is to then reduce the unfiltered loop bandwidth. That ndwidth is approximately proportional to the value of For a fixed $F_0$, unfiltered loop bandwidth duction requires a larger $C_0$ and larger control rrent. With this chip, changing the control current is



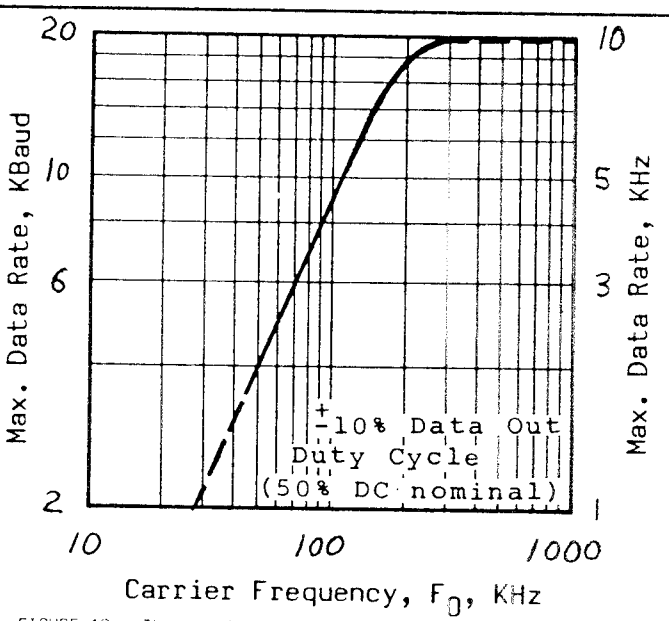



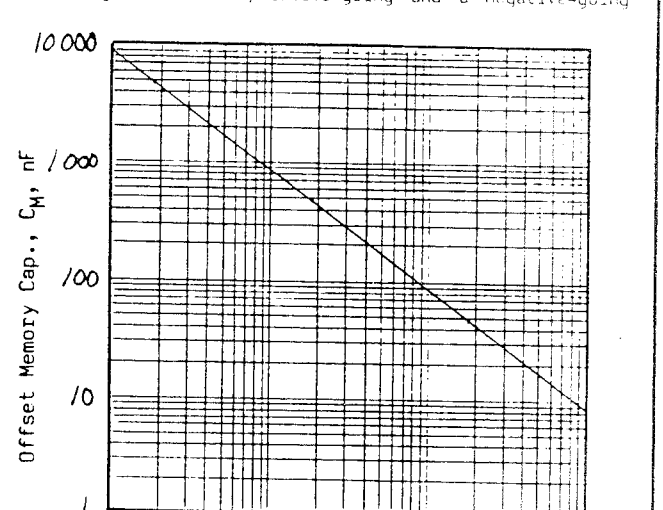

FIGURE 19. The maximum data rate versus $F_0$ using loop filter components optimized for max. noise performance while retaining a min. ±20% capture range (large signal).

not allowed. So one is forced to choose a $C_F/R_F$ combination with some minimum capture range, say ±20%, that is within some guardband from the point of loop instability. Happily, impulse noise tends to last only fractions of a millisecond so that the lack of low bandwidth loop response with low data rates is not a heavy penalty. As long as there is adequate capture range, the impulse noise filter performs admirably. Note that reducing $F_0$ will reduce the no-filter loop bandwidth, and indeed the maximum data rate falls below the limit set by the RC lowpass filter as $F_0$ falls below 100 KHz.

The tuned transformer characteristics will affect the demodulated data waveform more than $C_F$ and $R_F$ at low data rates. Tank Q and off-tuning will affect overshoot during the FSK frequency steps. This is a property of tuned circuits.

## $C_M$

Capacitor $C_M$ stores a voltage corresponding to a correction factor required to cancel the phase detector differential output DC offsets. The stored voltage is 5/6 of the DC offset plus some bias level of about 2.2 V. A large $C_M$ value increases the time required to bias-up the receive path at the beginning of transmission. A large $C_M$ does filter well and store its bias voltage long. Because of the initial random charge of $C_M$, the receiver must be given both a positive-going and a negative-going



data transition to charge to the proper bias voltage. Therefore, reducing $C_M$'s value to one that may be charged in less than 1 bit time will not save biasing time and is not recommended.

Use figure 20 to find $C_M$'s value knowing $F_{DATA}$, assuming the standard 2 bit receive charge time is desired. The cap. value and TC are not critical, but the cap. should have low leakage.

The impulse noise filter integrator capacitor $C_I$ is used to disallow the passage of any pulse shorter than the integrator charge time. That charge time, set to a nominal 1/2 bit time, is the time required for a $\pm 50$ µA charge current to swing $C_I$ over a 2 $V_{BE}$ range. Charge time under worst case conditions must never be greater than a bit time since no signal could then pass. Using a $\pm 10\%$ cap., full junction temperature range, and full specified current range, a maximum charge time of 1/2 bit is recommended. Figure 21 gives $C_I$ versus data rate under those conditions.

The collector pull-up resistor is sized to supply adequate pull-up current drive and speed while preserving adequate output low current drive.

## Breadboarding Tips

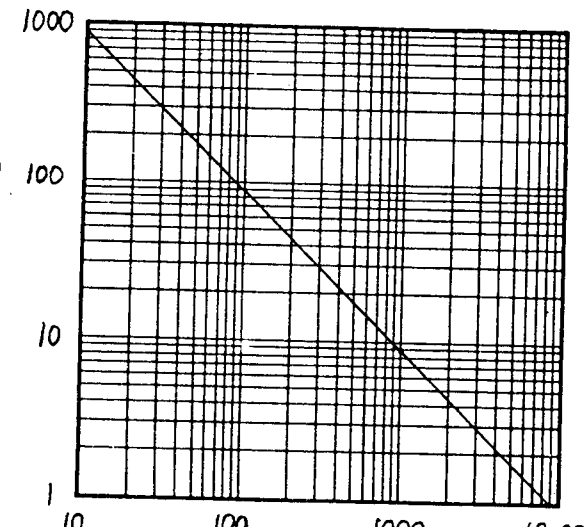
During CCT system evaluation, some techniques listed below will simplify certain measurements.

- Use caution when working on this circuit - dangerous line voltages may be present.

- When evaluating PLL operation, offset cancel circuit operation, and loop filter values, use the filter of figure 22 to view the demodulated signal minus the $2F_0$ and noise components. This filter models the RC lowpass filter on chip.

- When evaluating CCT system noise performance on a real power line, it is desirable to vary the signal amplitude to the receiver. This is not easy. An in-line line-proof L-pad is fine except that the line impedance is unknown and variable and so the L-pad will rarely match. Instead, the power output of a chip transmitter may be controlled using the circuit of figure 23. This circuit controls the ALC.

- Monitoring charge current in $C_M$ is sometimes important to analyze the offset cancel circuit. Measuring the current by droping more than a few mV in a series resistor affects operation and is not recommended. A workable method is to make $C_M$ small so that it may follow any data signal. Any change in pin 6 voltage shows that the data signal reaching the offset cancel circuit is larger than its nominal $\pm 50$ mV voltage window. A $C_M$ on the order of 500 pF with a 1 µA pull-down allows pin 6 to follow the internal signal (with a gain of about 5/6).



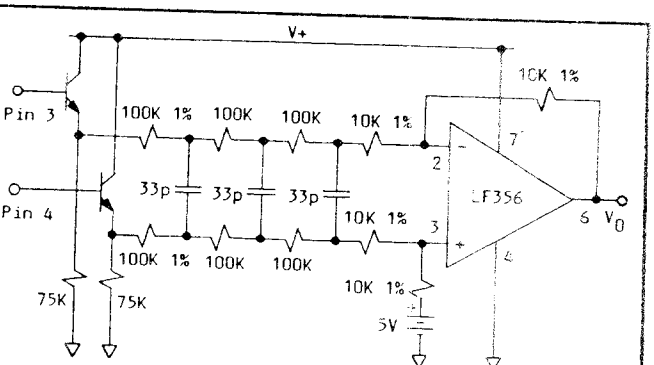




FIGURE 22. Circuit to view the differential demodulated data signal, minus the noise and $2F_0$ components, conveniently with a single-ended gain-of-ten output.

- It is sometimes desirable to place impulse noise on the line. A simple light dimmer with a 100 W light bulb load produces representative impulse noise.

- Do not allow peak currents of over 1 A through the 5.6 V Zener. In other words, don't short charged capacitors into this low-impedance device. Take care not to momentarily short pins 10 and 11 - damaging the IC.

- Figure 24 shows some typical signals beginning with serial data transmitted to received signal.

## Tuning Procedure

First, trim $F_0$ by putting the chip in the TX mode, setting a logical high data input, and measuring the TX high frequency, 1.022 $F_0$, on the Carrier I/O using these steps:

1. Take pin 17 to a logic low.
2. Take pin 5 to a logic high.
3. Place a counter on pin 10.
4. Adjust $R_0$ on pin 18 for $F = 1.022F_0$.

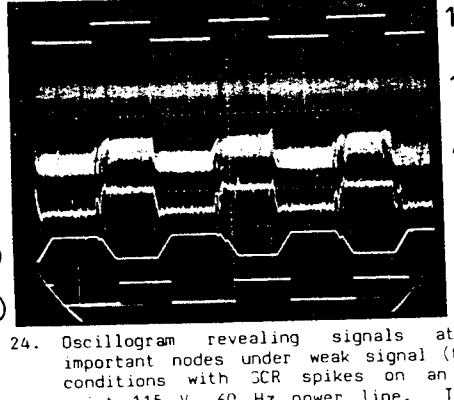
Second, the line transformer is tuned. The chip is placed in the TX mode, a resistive line load is connected to disable the ALC by reducing tank voltage swing below its limit. FSK data is then passed through the tank so that the tank envelope may be adjusted for equal amplitude for high and low data.

1. Take pin 5 to a logic high.
2. Place a logic-level square wave at or below the receiver's maximum data rate on pin 17.
3. Temporarily place a 330 Ohm resistor across the tank.
4. Place a scope on pin 10.
5. Adjust the transformer slug for the lowest envelope modulation.

In lieu of the 330 Ohm resistive load, $T_1$ may be coupled to the power line to better simulate actual load and tank pull conditions during tank tuning. Alternatively, a passive network representing an average line impedance may be connected to the line side of $T_1$. The circuit of figure 23 should then be used to defeat the leveling effect of the ALC.

## Thermal Considerations

It is desirable to place the largest possible signal on the power line for maximum range, limited only by the chip power dissipation and maximum junction temperature $T_J$. The falling output power at elevated $T_J$ allows a more optimal power output - high power at low $T_J$ and lower power at high $T_J$ for chip self-protection. However, it is still possible to exceed the maximum $T_J$ within the specified ambient temperature limit ($T_A$ = 85°C) under worst case conditions of 100% TX duty cycle, high supply, shorted load, poor PC board layout (with small copper foil




IGURE 24. Oscillogram revealing signals at several important nodes under weak signal (0.5 $mV_{RMS}$) conditions with SCR spikes on an otherwise quiet 115 V, 60 Hz power line. The signals are: 1) transmitted data, 2) RX carrier on the tuned transformer, 3) demodulated signal from the PLL, 4) signal after RC lowpass, 5) data at impulse noise filter integrator, and 6) received data. Horizontal scale is 10 ms per div.

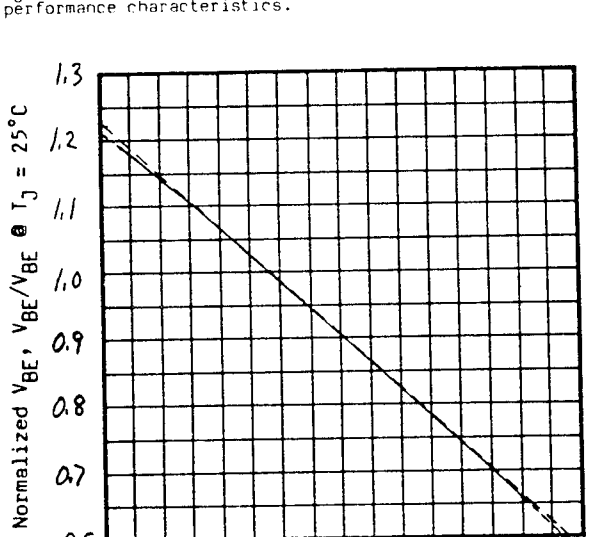
area), and an above nominal current part. Under those conditions, a part may dissipate 2140 mW, reaching a $T_J$ = 170°C worst-case (admittedly a rare occurrence). Proper system design includes the measurement or calculation of $T_J$ max. to guarantee function under worst-case operation. Like all devices with failure modes modeled by the Arrhenius model, the high chip reliability is further enhanced by keeping the die temperature mercifully below the absolute maximum rating.

A direct method of measuring operating junction temperature is to measure the $V_{BE}$ voltage on pin 18, which is always available under all operating modes. The graph of figure 25 may be used to find $T_J$, knowing $V_{BE}$ at the operating point in question and $V_{BE}$ at $T_A = T_J = 25°C$. $V_{BE}$ is found by powering up a chip (in RX mode) that has been dissipating zero power at some $T_A$ for some time and measuring $V_{BE}$ in under 1 s (for better than 5°C accuracy).

Alternately, $T_J$ may be calculated using:

$$T_J = T_A + \theta_{JA} P_D \qquad (1)$$

where $\theta_{JA}$ is 75°C/W for the plastic (N) package using a socket. That $\theta_{JA}$ value is for a high confidence level; nominal $\theta_{JA}$ for an N package is 60°C/W, lower with good PC board layout. Since $P_D$ is a relatively strong function of $T_J$, an iterative solution process starting with an initial guess for $T_J$ is used. With the estimated $T_J$, find the total supply current found in the typical performance characteristics.




## Transmit-To-Receive Switch-Over Time

An important figure-of-merit for a half-duplex CCT link, affecting effective data rate, is the TX-to-RX switch time $T_{TR}$. Using the recommended component values gives this part a nominal 2 bit-time (1 bit time = $1/[2F_{DATA}]$) over a wide range of operating conditions, where the receiver requires 1 positive-going and 1 negative-going data transition. $T_{TR}$ cannot be decreased significantly but does increase as noise filtering, especially via $C_M$, is increased. Impulse noise at switch, signals near the limiting sensitivity, poor $F_0$ match between receiver and transmitter because of poor trim or worst-case conditions, and the statistical nature of PLL locking may all contribute to increase $T_{TR}$ to possibly 4 bit-times.

$T_{TR}$ is lower when a pair of LM1893's handshake rapidly. The receiver was designed to "remember" the RX-mode DC operating points on $C_M$ and $C_F$ while in the TX mode. Under noisey worst case conditions, $C_M$ will discharge to the point of false operation after 35 bit-times in the TX mode (1400 bit times with no noise and a nominal part, $F_{DATA}$ = 180 Hz). $T_{TR}$ is about 0.8 ms (proportional to the selected $F_0$) plus 1/2 bit-time.

The major components of $T_{TR}$ are described below for a nominal 125 KHz $F_0$, 180 Hz $F_{DATA}$, lightly-loaded tank with a Q of 20, and the circuit of figure 4. The remote CCT has been operating in the TX mode with a 26.6 $V_{PP}$ tank swing and is now selected as a receiver. An incoming signal requiring the ultimate receiver sensitivity immediately is placed on the line.

First, the tank stored energy at the transmit frequency must decay to a level below the 2.8 $mV_{PP}$ swing caused by the 0.14 $mV_{RMS}$ incoming line signal containing the information to be received.

$$\text{decay time} = \frac{Q}{\pi F_0} \ln\left(\frac{V_1}{V_0}\right) =$$

$$\frac{20}{\pi \times 125\,000} \ln\left(\frac{26.6}{0.0028}\right) = 0.466 \text{ ms} \qquad (2)$$

That is 0.47 ms of delay (proportional to $1/F_0$ and Q).

Second, the PLL must acquire the signal, it must lock and settle. Acquisition time is statistical and may take any length of time, but average acquisition time depends on the loop filter components $C_F$ and $R_F$ and the difference in center frequencies, $\Delta F_0$, of the TX/RX pair. Using the recommended $C_F$ and $R_F$ (47 nF and 6.2 KOhm) with a ± 4.4% $\Delta F_0$ (a ± 100 mV DC offset on $C_F$ and $R_F$), lock was measured to take less than 50 cycles of $F_0$. That is a 0.40 ms delay (proportional to $1/F_0$).

Acquisition is incomplete until the second order PLL loop settles. For the above-mentioned $C_F$ and $R_F$, the loop natural frequency $F_N$ and damping factor are found to be (reference 1) 2.3 KHz and 1.0 respectively. From Dorf (reference 2), settling to within ±25 mV of the ±100 mV DC offset change requires 2.7 periods of $F_N$, or 1.2 ms (a function of $C_F$ and $R_F$).

Third, the RC lowpass filter introduces a 0.12 ms delay.

Fourth, $C_M$ must charge up to ±(5/6)100 = 83 mV depending on the polarity of $F_0$. Borderline data squaring with zero noise immunity is possible with only ±(5/6) 50 mV of charging. $C_M$ charge current is a linear and asymptotic function approximated by assuming a 50 µA charge current and a full 83 mV charge voltage. $C_M$ charge time is then 1.7 ms (proportional to $1/F_{DATA}$).

Fifth, the impulse noise filter adds a 1/2 bit-time delay.

Total $T_{TR}$ is 3.9 ms plus 1/2 bit-time for a total of 1. bit-times at 360 Baud. This rough estimate neglects tha part of the $C_M$ charge may happen while the PLL settles etc.

## Receive-To-Transmit Switch-Over Time

Assume the chip has been in the RX mode and the TX mode i now selected. In less than 10 µs, full output current i exponentially building tank swing. 50% of full swing i achieved in less than 10 cycles - or under 80 µs at 12

## er Line Attenuation

spective of how wide the limits on power line impedance are placed, there are no guarantees. However, since CCT design requires an estimate of the lowest expected impedance $Z_{LN}$ encountered for the most efficient smitter-to-line coupling, line impedance should be ured and $Z_L$ limits fixed to a given confidence l. Reasonable values for $T_1$ turns ratio, loaded Q, tank resonant frequency pull $F_Q$ may be found to le a CCT system design that functions with the rwhelming majority of power lines.

limited sampling of $Z_L$ was made during the LM1893 ign of residential and commercial 115 V 60 Hz power e. Data was also drawn from the research of Nicholson Malack (reference 3), among others, to produce figures and 27. All measured impedances are contained within shaded portions of figure 27. A nominal 3.5, 7.0, and Ohm $Z_{LN}$ is used throughout the application information h a nominal 45° phase (0° is sometimes used for plicity).

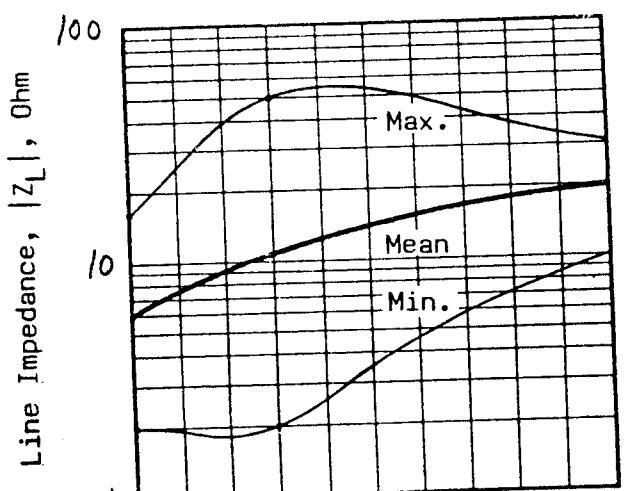
## er Line Impedance

wiring in most US buildings is a flat 3 conductor cable led Amerflex, BX, or Romex. All referenced line edances refer to hot-to-neutral impedances with a unded center conductor. The cable has a 100 Ohm aracteristic impedance, a 125 KHz quarter-wavelength of m (250 m at 300 KHz), and a measured 7 dB attenuation r a 50 m run with a 10 Ohm termination. Generally, line ads may be treated as lumped impedances. Instrument line rds exhibit about 0.7 uH and 30 pF per meter.

mited tests of CCT link range using this chip show tensive coverage while remaining on one phase of a stribution transformer (100's of m) with link failure ross transformer phases or through transformers. Total ine attenuation allowed from full signal to limiting ensitivity is more than 70 dB. Typically, signal is upled across transformer phases by parasitic winding apacitance, typically giving 40 dB attenuation between nased 115 V windings. Coupling capacitors must be nstalled for link operation across phases. Power factor orrecting capacitor banks on industrial lines or filter apacitors across the power lines of some electronic gear hort carrier signal and should be isolated with nductors. Increasing range is sometimes accomplished by lecting to install the isolating inductors and coupling apacitors, as well as by electing to use the boost option nd by building repeaters.

## e Coupling Transformer

he design arrived at for $T_1$ is the result of an unhappy ompromise - but a workable one. The goals of 1) building $_1$ with a stable resonant frequency, $F_Q$, that is little ffected by the de-tuning effect of the line impedance $_L$, and of 2) building a tightly line-coupled transformer or transmitted carrier with loose coupling for transients, re somewhat mutually exclusive. The tradeoffs are exposed n the following pedagogue for the CCT designer attempting a new boost-capable or different core transformer design.



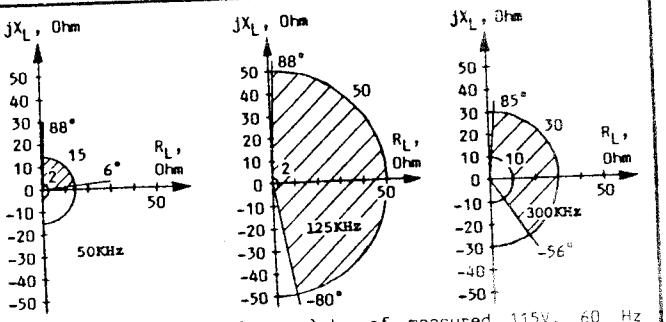




FIGURE 27. Complex-plane plots of measured 115V, 60 Hz line impedance where $Z_L = R_L + jX_L$.

The compromises might be eliminated by separating the TX output and RX input. An untuned TX coupling transformer with only core coupling (not air-coupled solenoid windings) would employ a high permeability, high magnetic field, low loss, square saturating, toroidal core. The resonant RX path would be isolated from line-pull problems by a unilateral amplifier that operates at line voltages with much more than 110 dB of dynamic range. The solution is prohibitively complex and expensive, and is not used.

First, choose the turns ratio N based on an estimated lowest $Z_L$ likely encountered, $Z_{LN}$. Figure 28 shows graphically how N affects line signal. N should be as large as possible to drive $Z_{LN}$ with full signal. If $T_1$ has an unloaded Q, $Q_U$, of well less than 35, a guess of N somewhat high should be used and later checked for accuracy. The recommended transformers have secondary taps giving a choice of N=7.07, 10, and 14.1 (nominally) for driving $Z_{LN}$'s of 14, 7.0, and 3.5 Ohm respectively (at $T_J = 25°C$, $V_+ = 18V$, and $Q_U = 35$).

The resonating inductance of the tuned primary, $L_1$, is sought. Note that, while standard transformer design gives a transformer self-inductance with an impedance at operating frequency well above load impedance, the tuned transformer requires a low $L_1$ for adequate $Q_U$ and minimum line pull. Result: relatively poor mutual coupling.

$$L_1 = \frac{R}{2\pi F_Q Q} \qquad (3)$$

It is known that resonant frequency $F_Q = F_0$ and some minimum bandwidth, or maximum Q, will be required to pass signal under full load conditions.

$$L_1 = \frac{R_Q \parallel |Z_{LN}|'}{2\pi F_0 Q_L} \qquad (4)$$

$|Z_{LN}|'$ is the reflected $Z_{LN}$, $Q_L$ is the loaded Q, and parallel resistance $R_Q$ models all transformer losses and sets $Q_0$.

$R_Q \parallel |Z_{LN}|'$ is found knowing that it absorbs full rated power.

$$P_0 = I_0 V_0 = \frac{I_{OPP}}{2\sqrt{2}} \left[ \frac{2(-V_{ALC} + V+)}{2\sqrt{2}} \right] = \frac{(-4.7 + V+) I_0}{4} \qquad (5)$$

where $I_0$ is in App. At an elevated $T_J$

$$P_0 = \frac{(18-4.7)0.06}{4} = 0.200W \qquad (6)$$

$$R_Q \parallel |Z_{LN}|' = \frac{V_0^2}{P_0} = \frac{(-V_{ALC} + V+)\sqrt{2}}{I_0} = 442 \text{ Ohm} \qquad (7)$$

$$R_Q = \frac{1}{\frac{1}{R_Q \| |Z_{LN}|^2} - \frac{1}{|Z_{LN}|^2}} = \frac{1}{\frac{1}{442} - \frac{1}{695}} = 1210 \text{ Ohm} \qquad (9)$$

$$R_{QS} = \frac{R_Q}{1+Q_U^2} = \frac{1210}{1+35^2} = 1 \text{ Ohm} \qquad (10)$$

Only $Q_L$ remains to be found to calculate $L_1$. $Q_L$ is related to the -3 dB (half-power) bandwidth by

$$Q_L = \frac{1}{BW\ (\%\ of\ F_Q)} \qquad (11)$$

An iterative solution is forced where line pull, $\Delta F_Q$, must be guessed to find $Q_L$ and $L_1$. $L_1$ is then used to check the line pull guess; a large error requires a new guess. Try a BW of 8.7% - that is 4.4% for deviation, 1% for TC of $F_Q$, and 3.3% for $F_Q$ - giving $Q_L$ = 11.5.

$$L_1 = \frac{442}{2\pi \times 125\ 000 \times 11.5} = 49.0\ \mu H$$

Knowing the core inductance per turn, $L$ , and $L_1$, the number of turns is found.

$$T_1 = \sqrt{\frac{L_1}{L}} = 49.0 = 49\ 1/2 \text{ turns} \qquad (14)$$

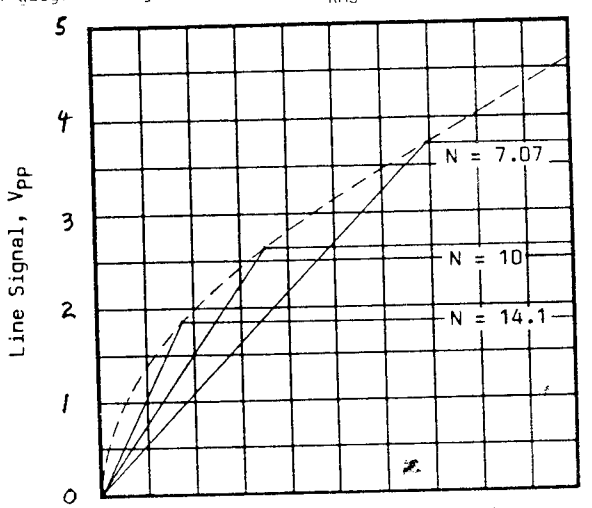
T is normally an integer, but these transformers require so few turns that half-turns are specified, remembering that the remaining 1/2 turn is completed on the P.C. board and is loosely coupled. The secondary turns are calculated

$$T_2 = \frac{T_1}{N} = \frac{49.5}{7.07} = 7.00 = 7 \text{ turns} \qquad (15)$$

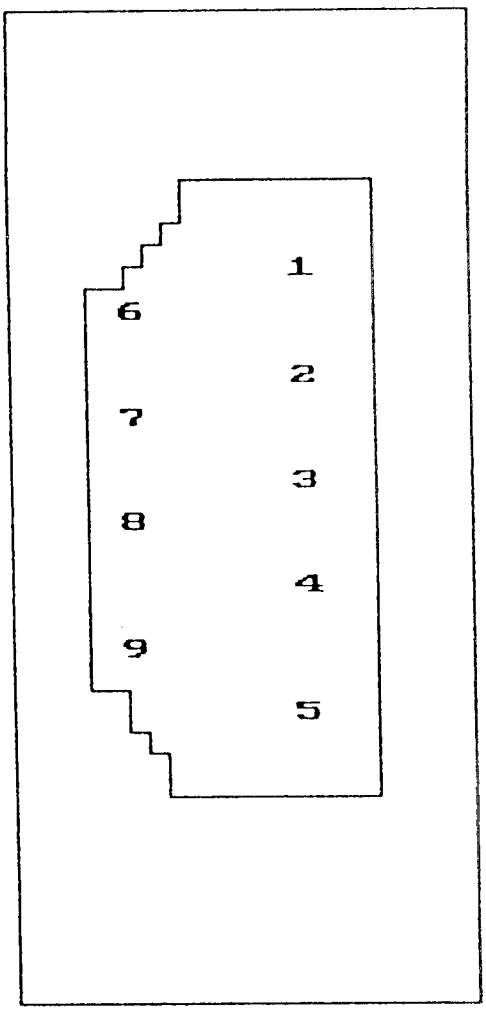
giving an $L_2$ of 0.98 uH. Note that the recommended 125 KHz transformer mirrors these specifications. The resonating capacitor is

$$C_Q = \frac{1}{(2\pi F_Q)^2 L_1} = 33.1 \times 10^{-9} = 33 \text{ nF} \qquad (16)$$

Line pull $\Delta F_Q$ was calculated (reference 5) for a $Z_L$ magnitude of 14 Ohm and up with any phase angle from -90° to 90°. $\Delta F_Q$ was 6.4% - well above the 3.3% estimate. Referring to (11), an 11.8% bandwidth is required, forcing $L_1$ to be reduced to reduce Q. That fix was not implemented; some signal attenuation under worst-case drift and $\Delta F_Q$ is allowed. $L_1$ is already so small that the 31 gauge winding conducts a 1/4 $A_{RMS}$ circulating current.

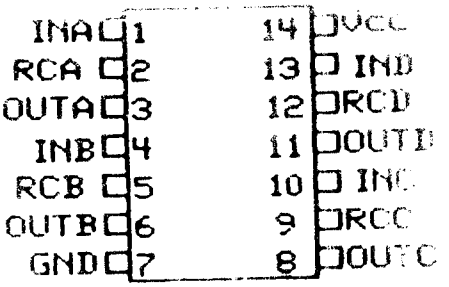


# RS-232 - 9 Pin Assignment




1. Carrier detect
2. Receive data
3. Transmit data
4. DT Ready
5. Signal Ground
6. Data set ready
7. Request to Send
8. Clear to Send
9. Ring Indicator

# MC1489 QUAD RS-232C RECEIVER




RC = RESPONSE CONTROL

# MC1488 QUAD RS-232C DRIVER