Department of Electrical & Electronics Engineering

Kumaraguru College of Technology

(Affiliated to Bharathiar University)
Coimbatore - 641 006

D – 2 : 2

Certificate

This is to certify that the Project Report entitled

Transmission Lines protection by using Symmetrical Components of Currents

is the bonafide record of project work done by

Mr _____

University Reg No. _____ *Roll No* _____

in partial fulfilment of the requirements

for the award of the

Bachelor of Engineering in

Electrical & Electronics Engineering

branch of the Bharathiar University, Coimbatore

during the academic year 1995-96

PROFESSOR & HEAD
Dept. of Electrical & Electronics Engg.
Kumaraguru College of Tech., Coimbatore

Guide

submitted for the viva voce examination held on _____

Internal Examiner

External Examiner

ACKNOWLEDGEMENT

We wish to convey our profound appreciation and gratitude to our guide **Mrs.T.RANI M.E.,** Lecturer, Department of Electrical and Electronics Engineering who has given us invaluable help and support to complete this project successfully.

We are greatly obliged to **Dr.K.A.PALANISWAMY B.E., M.Sc (Engg.), Ph.D., M.I.S.T.E., C.Eng.(I), F.I.E.,** Professor and Head of the Department of Electrical and Electronics Engineering for his leadership and his expert suggesstions through out the course of the project.

We would like to record our sincere thanks to our principal **Dr.S.SUBRAMANIAN, B.E., M.Sc(Engg)., Ph.D., S.M.IEEE** for providing the necessary facilities to complete this project.

Our since thanks are due to all the staff of department of Electrical and Electronics Engineerng. We would also like to express our thanks to **Mr.E.MATHIVANNAN. M.E.,** Lecturer, Electronics and Communication Engineering for this help.

SYNOPSIS

A balanced 3 phase system can be solved on per phase basis. The solution of unbalanced system is not as simple as that of balanced system. However the solution of unbalanced system can be simplified by the application of symmetrical components.

In this project a circuit is designed to measure the symmetrical components of currents in a unbalanced circuit. For measurement of symmetrical components, coils with the phase shift of 60° are employed at present. In this project an electronic circuit is used to produced a phase of 120° for direct measurements of symmetrical components. This proves to be more economical and accurate. Operational amplifier are used for the design of filters in the circuit for phase shift.

From the values of the symmetrical conmponent measured under fault condition the type of the fault can be known and these measured values can be used for effective protection for the power system.

CONTENTS

CHAPTER 1

INTRODUCTION

1.1 POWER SYSTEM :

A power system consists of power source (alternator), Transformers, Transmission lines and the Electrical load. The power sources are not only the connected to the load but also are interconnected to enable continous supply of power, This entire system from alternator to electrical loads forms a grid network.

1.2 TYPES OF FAULT :

The faults in a power system can be classifed as

1. symmetrical fault
2. Asymmetrical fault

1.2.1 SYMMETRICAL FAULT :

The fault is caused in the system either by insulation failure of equipment or flashover of lines initiated by a lightning stroke or through accidental faulty operation.

During symmetrical fault the system impedances in each phases are identical and the three phase voltage and the current throughout the system are completely balanced in time phase by 120 degrees. In a balanced system analysis can be done on a single phase basis. The knowledge of voltage and current in one phase is sufficient to completely determine voltage and current in other two phases. Real and reactive powers are simply three times the corresponding per phase values.

1.2.2. UNSYMMETRICAL FAULT :

Unsymmetrical faults occurs either in conductor to ground or in between conductors. these faults are characterised by increase in current and fall in voltage and frequency. Unsymmetrical faults can be classified as

1. Line to ground fault
2. Line to line fault
3. Double line to ground fault

During unsymmetrical fault the system operation will be unbalanced. Analysis under unbalanced conditions has to be carried out on a three phase basis. Alternatively, a more convenient method of analyzing unbalanced operation is transforming three phase unbalanced voltages and currents into a sets of balanced voltages and currents called symmetrical components.

1.3 SYSTEM PROTECTION :

Faults can be very destructive to power system. A great deal of study, development of devices and design of protection schemes have resulted in improvement in the prevention of damage to transmission lines and equipment and interruptions at generation station following the occurence of fault.

Fault caused by surges are usually of such short duration that any circuit breakers which are permanent, the faulted sections of the system must be isolated to maintain normal operation of the system.

The operation of circuit breakers is controlled by relays which sense the fault. In the application of relay, zones of protection are specified to define the parts of the system for which various relays, are responsible.

CHAPTER 2

FAULT ANALYSIS

2.1 SYMMETRICAL COMPONENTS

A set of three balanced voltages V_a, V_b, V_c is characterised by equal magnitudes and interphase differences of 120 degrees. The set is said to have a phase sequence abc (positive sequence) if V_b lags V_a by 120 degrees and V_c lags V_b by 120 degrees. The three phasors can then be expressed in terms of the reference phasor V_a as

$$V_a = V_a,\ V_b = a^2 V_a,\ V_c = aV_a \qquad \text{----------} > \qquad 2.1$$

The complex number operator is defined as

$$a = e^{j\,120^\circ} \qquad \text{----------} > \qquad 2.2$$

If the phase sequence is acb (negative sequence), then

$$V_a = V_a,\ V_b = aV_a,\ V_c = a^2 V_a$$

Thus a set of balanced phasors is fully characterised by its reference phasor (V_a) and its phase sequence (positive and negative).

Suffix 1 is commonly used to indicate positive sequence. A set of (balanced) positive sequence phasor is written as

$$V_a , V_{b1} = a_2 V_{a1}, V_{c1} = a.V_{a1}$$

It can be represented as shown in Fig.2.1

Similarly, suffix 2 is used to indicate negative sequence. A set of (balanced) negative sequence phasor is written as

$$V_{a2}, V_{b2} = a.V_{a2}, V_{c2} = a^2 .V_{a2}$$

It can be represented as shown in Fig. 2.2

A set of three voltages (phasors) equal in magnitude and having the same phase is said to have zero sequence. Thus a set of zero sequence phasor is written as

$$V_{ao}, V_{bo} = V_{ao}, V_{co} = V_{ao}$$

It can be represented as shown in Fig.2.3

The three phasors can be expressed as the sum of positive, negative and zero sequence phasors defined above, Thus

$$V_a = V_{ao} + V_{a1} + V_{a2} \quad \text{----------} > \quad 2.3$$

$$V_b = V_{bo} + V_{b1} + V_{b2} \quad \text{----------} > \quad 2.4$$

$$V_c = V_{co} + V_{c1} + V_{c2} \quad \text{----------} > \quad 2.5$$

The three phasor sequences (positive, negative and zero) are called the symmetrical components of the original phasor set V_a, V_b, V_c. The addition of symmetrical components as per the above equation can be represented in the phasor digram as shown in Fig 2.3

The above voltage equation can be represented in terms of reference phasors phasors V_{ao},V_{a1},V_{a2}. Thus

$$V_a = V_{ao} + V_{a1} + V_{a2}$$

$$V_b = V_{ao} + a^2V_{a1} + aV_{a2}$$

$$V_c = V_{ao} + aV_{a1} + a^2V_{a2}$$

These equation can be expressed in the matrix form

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \begin{bmatrix} V_{ao} \\ V_{a1} \\ V_{a2} \end{bmatrix} \quad \text{----------} > \quad 2.6$$

$$\begin{bmatrix} V_{ao} \\ V_{a1} \\ V_{a2} \end{bmatrix} = 1/3 \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad \text{---------->} \quad 2.7$$

Similarly current equation can be represented as follows

$$\begin{bmatrix} I_{ao} \\ I_{a1} \\ I_{a2} \end{bmatrix} = 1/3 \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \quad \text{---------->} \quad 2.8$$

2.2 FACTS ABOUT SEQUENCE CURRENTS :

1. A balanced 3 phase system consists of positive sequence components only, its negative and zero sequence components being zero.
2. The presence of negative or zero sequence currents in a 3-phases system introduces unsymmetry and is indicative of an abnormal condition of the circuit in which these components are found.
3. The vector sum of the positive and negative sequence current of an unbalanced three phase system is zero. The resultant consists of three zero sequence currents i.e., vector sum of all sequence currents in three phase unbalanced system

   = $I_{ao} + I_{bo} + I_{co}$

2.3 SEQUENCE IMPEDANCES :

Each element of power system will offer impedance to different phase sequence components of current which may not be the same. For example, the impedance which any piece of equipment offers to positive sequence current will not necessarily be the same as offered to negative sequence current or zero sequence current. Therefore, in un-symmetrical fault calculations, each sequence current - viz.,

1. Positive sequence impedance (Z_1)

2. Negative sequence impedance (Z_2)

3. Zero sequence impedance (Z_0)

The impedance offered by an equipment or circuit to positive sequence current is called positive sequence impedance and is represented by Z_1. Similarly, impedances offered by any circuit or equipment to negative and zero sequence current are respectively called negative sequence impedance (Z_2) and zero sequence impedance (Z_0).

The following points may be noted :

1. In a three phase balanced system, each piece of equipment or circuit offers only one impedance - the one offered to positive or normal sequence current. This is expected because of the absence of negative and zero sequence current in the three phase balanced system.

2. In a three phase unbalanced system, each piece of equipment or circuit will have three values of impedance viz., positive sequence impedance, negative sequence impedance and zero sequence impedance.

3. The positive and negative sequence impedance of linear, symmetrical and static circuits are equal and are the same as those used on the analysis of balanced conditions. This is due to the fact that impedance of such circuit is independant of the phase order, provided the applied voltages are balanced. It may be noted that positive and negative sequence impedance of rotating machines are normally different.

4. The sequence impedance depends upon the path taken by the zero sequence current; as this path is generally different from the path

taken by the positive and negative sequence currents. Therefore, zero sequence is usually different from positive or negative sequence impedances.

2.4 ASSUMPTIONS MADE FOR THE CALCULATION OF UNSYMMETRICAL FAULT :

1. The generated emf system is positive sequence only.

2. No current flows in the network other than due to fault, i.e., load currents are neglected.

3. The impedance of the fault is zero.

4. Phase 'R' shall be taken as the reference phase.

2.5 SEQUENCE NETWORKS

POSITIVE SEQUENCE NETWORK

The positive sequence network for a given power system shows all the paths for the flow of positive sequence current in the system. While drawing the positive sequence network of a given power system, the following points may be kept in view.

1. Each generator in the system is represented by the generated voltage in series with appropriate reactance and resistance.
2. Current limiting impedances between the generators neutral and ground pass no positive sequence current and hence are not included in the positive sequence network.
3. All resistances and magnetising currents for each transformer are neglected as a matter of simplicity.
4. For transmission lines, the shunt capacitances and resistances are generally neglected.
5. Motor loads are included in the network as generated e.m.f. in series with appropriate reactance.

The synchronous machine is designed with symmetrical winding, it includes e.m.fs of positive sequence only i.e., no negative and zero sequence voltages are induced in it.

Since it is a balanced network it can be represented as shown in Fig 2.5 by the single phase network model as shown in fig 2.6. This can be used for the purpose of analysis.

The positive sequence voltage of terminal `a' with respect to the reference bus is given by

$$V_{a1} = E_a - Z_1.I_{a1}$$

and represented in Fig. 2.5

NEGATIVE SEQUENCE NETWORK

The negative sequence network for a given power system shows all the paths for the flow of negative sequence currents in the system. The paths for the flow of negative sequence currents in the system. The one line digram composed of impedances offered to the negative sequence currents. The negative sequence network can be readily obtained from positive sequence network with the following modifications.

1. Omit the e.m.fs of three phase generator and motor in the positive sequence network. It is because these devices have only positive sequence generated voltages.
2. Change, if necessary, the impedance that represent rotatary machinary in the positive sequence network. It is because negative sequence impedance of rotating machinary is generally different from that of positive sequence impedance.

3. Current limiting impedance between generators neutral and ground pass no negative. sequence current and hence are not included in the negative sequence network.

4. For static devices such as transmission lines and transformers the negative sequence impedance have same value as the corresponding sequence impedance.

The negative sequence voltage of terminal 'a' with respect to the reference bus is given by

$$V_a = - I_{a2}.Z_2$$

and is represented in Fig 2.7

ZERO SEQUENCE NETWORK :

The zero sequence network for a given power system shows all the paths for the flow of zero sequence currents. The zero sequence network of a system depends upon the nature of connection of the three phase windings of the components in the system. The following points may be noted about the zero sequence network.

1. The zero sequence currents will flow only if there is a return path i.e., path from netural in the circuit.

2. In the case of a system with no current path for zero sequence currents, these currents cannot exist.

The zero sequence voltage and current will also be induced in the network. This configuration is shown in the figure 2.5. The current flowing in the impedance Z_n between netural and ground is $I_n = 3I_{a0}$. The zero sequence voltage of terminal `a' with respect to ground reference is $I_n = 3I_{a0}$.

The zero sequence voltage of terminal `a' with respect to ground (the reference bus) is therefore

$$V_{a0} = -3.Z_n.I_{a0} - Z_{og}.I_{a0}$$

$$= (-3Z_n + Z_{og})\ I_{a0}$$

and is represented as in Fig 2.9. Where Z_{og} is the zero sequence impedance per phase of the machine. Since the single phase zero sequence current, its total zero sequence impedance must be

$$Z_0 = 3Z_n + A_{0g}$$

$$V_{a0} = -Z_0\ I_{a0} \qquad \text{----------} > \quad 2.9$$

2.6 ANALYSIS OF FAULT

Let the line to ground fault occur at point 'F' in a transmission line.

The conditions during the fault are

$V_a = 0;\ I_b = 0;\ I_c = 0;$

$V_{a0} = 1/3\ (V_a + V_b + V_c)$

$= 1/3\ (V_b + V_c)$ ----------> 2.10

$I_{a1} = I_{a2} = I_{a3}$

$V_{a1} + V_{a2} + V_{a0} = 0$

$V_{a1} = 1/3(V_a + aV_b + a^2V_c)$

$= 1/3(aV_b + a^2V_c)$ ----------> 2.11

$V_a^2 = 1/3(V_a + a^2V_b + aV_c)$

$= 1/3(a^2V_b + aV_c)$ ----------> 2.12

LINE TO LINE FAULT :

Let the line to line fault between the phase b and c. Conditions during fault are

$$I_a = 0;\ I_b + I_c = 0;\ V_b = V_c$$

Here,

$$V_{a1} = V_{a2}$$

From the sequence network we know that

$$V_{a0} = -Z_o.I_{a0}$$

Here

$$I_{a0} = 1/3\ (I_a + I_b + I_c) = 0$$

$$V_{a0} = 0$$

Thus line to line fault the inferences are

$$V_{a0} = 0;\ V_{a1} = V_{a2} \quad \text{----------} > \quad 2.13$$

$$\begin{bmatrix} I_{a0} \\ I_{a1} \\ I_{a2} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix}$$

$$= \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} 0 \\ I_b \\ I_c \end{bmatrix}$$

The phasor digram of line to line fault is shown in Fig 2.13

DOUBLE LINE TO GROUND FAULT :

Let the double line to ground fault occur between the phases b and c.

Condition during the fault are $I_a = 0$; $V_b = V_c = 0$

Thus double line to ground fault inference is

$$V_{a0} = V_{a1} = V_{a2} = 1/3\ V_a$$

Since

$$I_a = 0$$

$$I_{a0} = -(I_{a1} + I_{a2}) \quad \text{----------> } 2.14$$

The phasor diagram of double line to ground fault is shown in Fig 2.15

THREE PHASE FAULT :

Let the fault occur at all the three phases.

Conditions during the fault are

$$V_a = V_b = V_c = 0$$

$$I_a + I_b + I_c = 0 \qquad \text{----------} > \quad 2.15$$

So,

$$V_{a0} = V_{a1} = V_{a2} = 0 \qquad \text{----------} > \quad 2.16$$

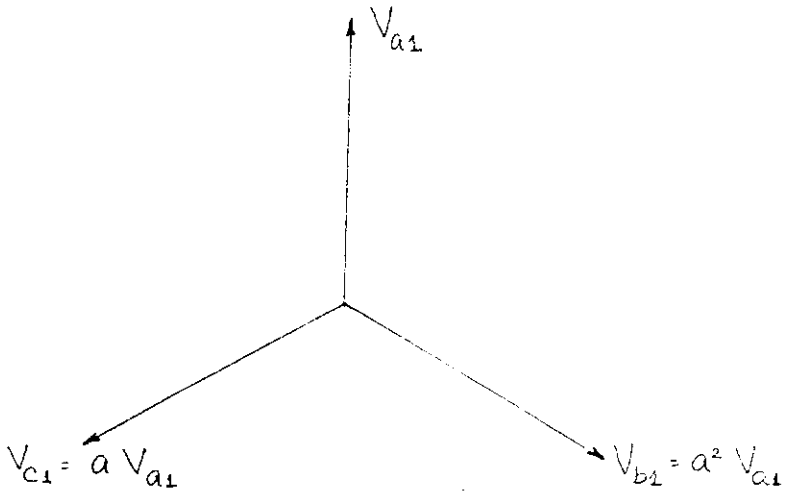


FIG. 2·1 : POSITIVE SEQUENCE PHASOR DIAGRAM.

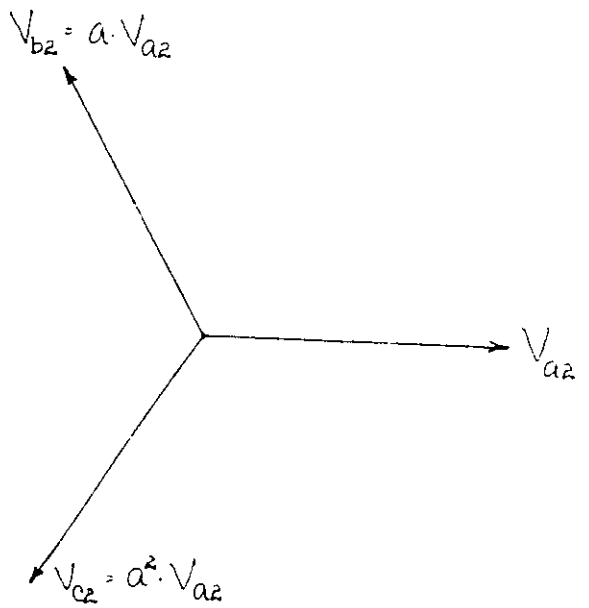


FIG. 2·2 : NEGATIVE SEQUENCE PHASOR DIAGRAM.

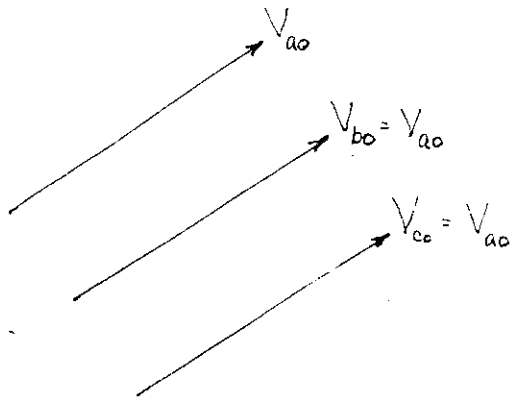


FIG. 2·3 : ZERO SEQUENCE PHASOR DIAGRAM.

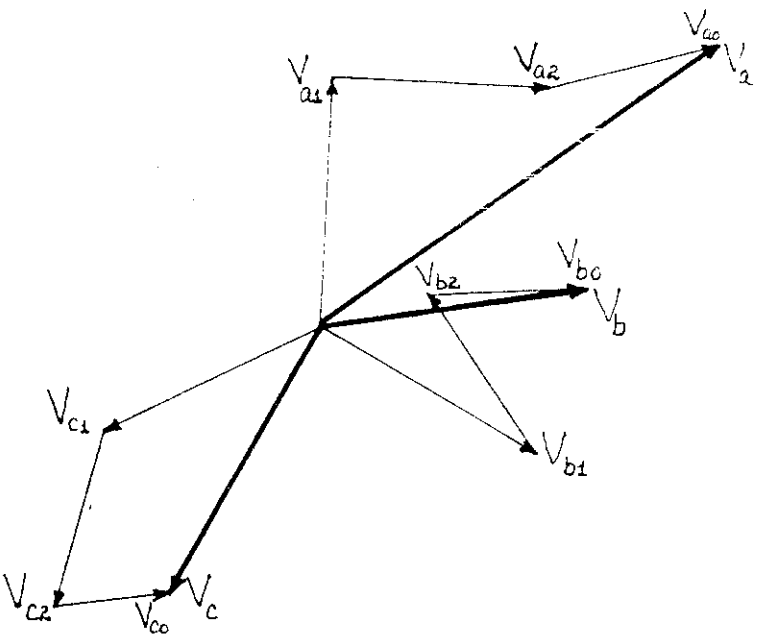


FIG. 2·4 : PHASOR DIAGRAM.

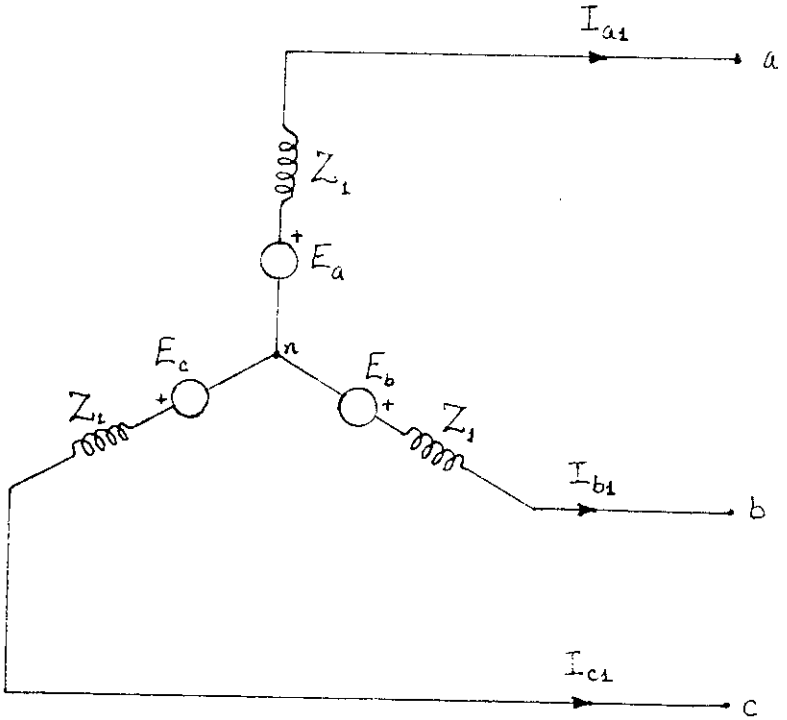


FIG. 2·5 : THREE PHASE GENERATOR WITH ONLY POSITIVE SEQUENCE COMPONENTS OF CURRENT FLOWING.

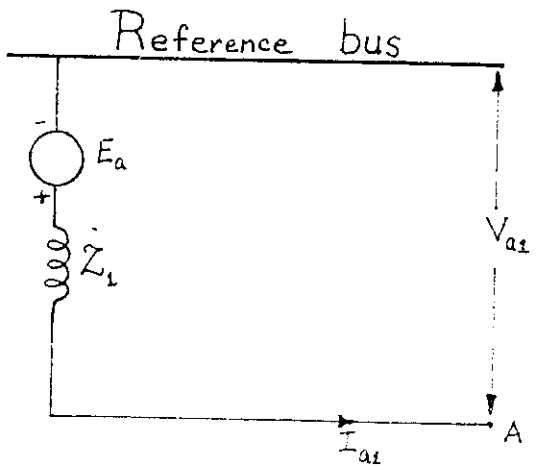


FIG. 2·6 : POSITIVE SEQUENCE NETWORK OF GENERATOR.

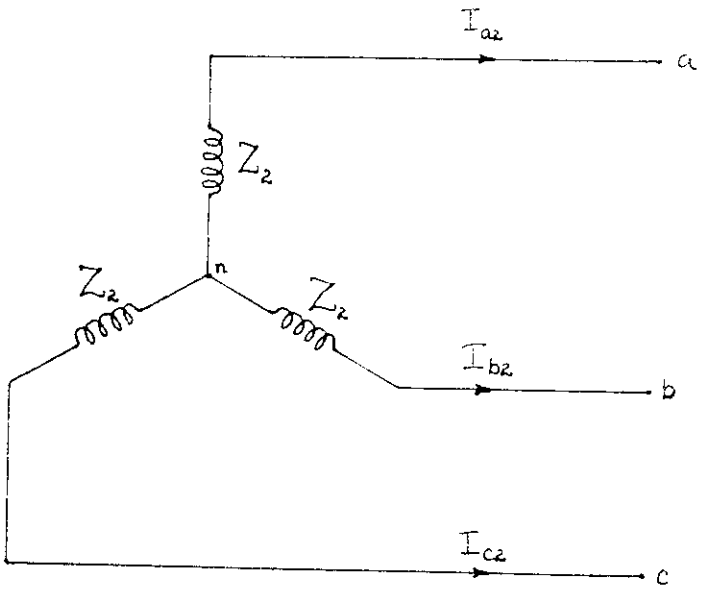


FIG. 2·7 : THREE PHASE GENERATOR WITH ONLY NEGATIVE SEQUENCE COMPONENTS OF CURRENT FLOWING.

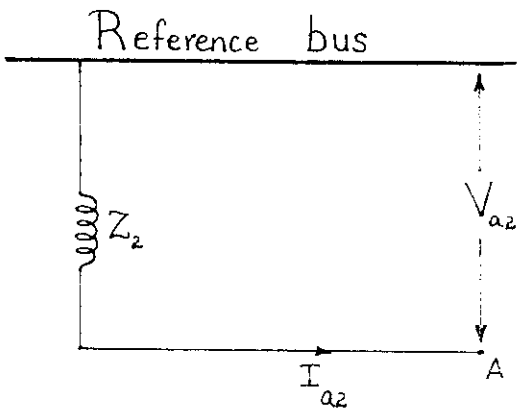


FIG. 2·8 : NEGATIVE SEQUENCE NETWORK OF GENERATOR.

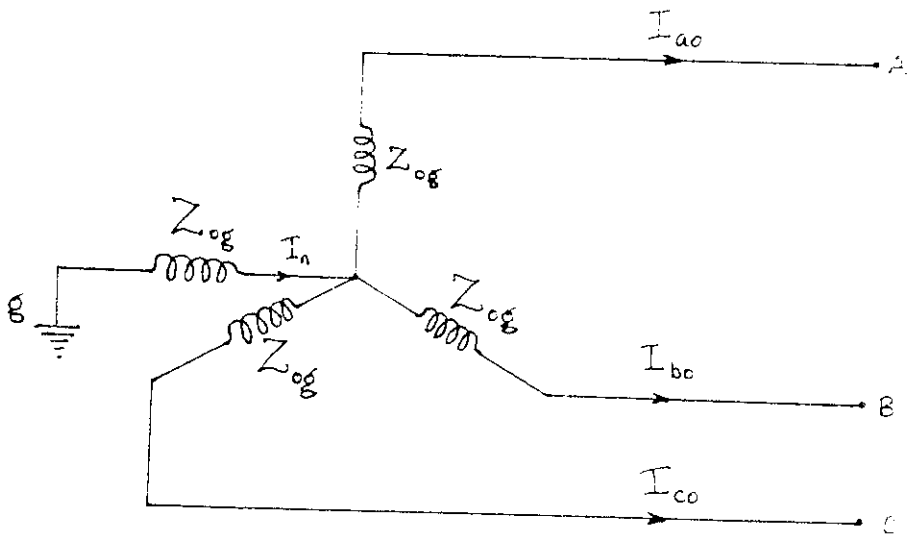


FIG. 2.9 : THREE PHASE GENERATOR WITH ONLY ZERO-SEQUENCE COMPONENT OF CURRENT FLOWING.

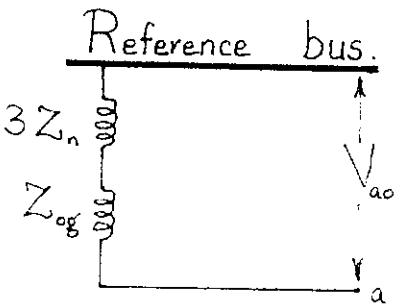


FIG. 2.10 : ZERO-SEQUENCE NETWORK OF A GENERATOR.

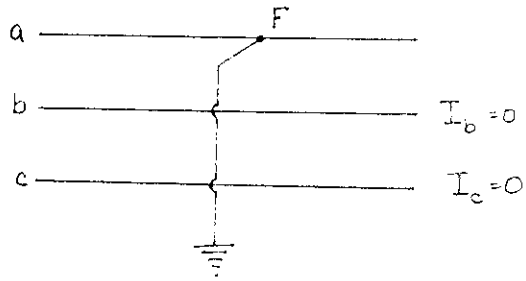


FIG. 2·11 : LINE TO GROUND FAULT.

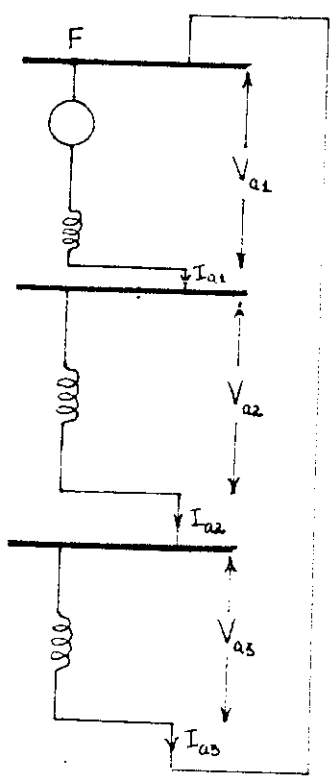


FIG. 2·12 : CONNECTION OF SEQUENCE NETWORKS TO REPRESENT SINGLE LINE TO GROUND FAULT.

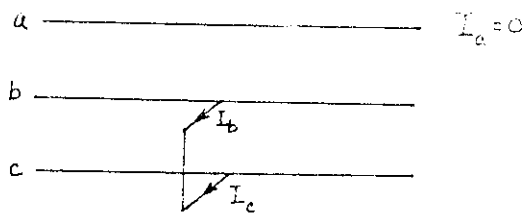


FIG. 2·13 : LINE TO LINE FAULT.

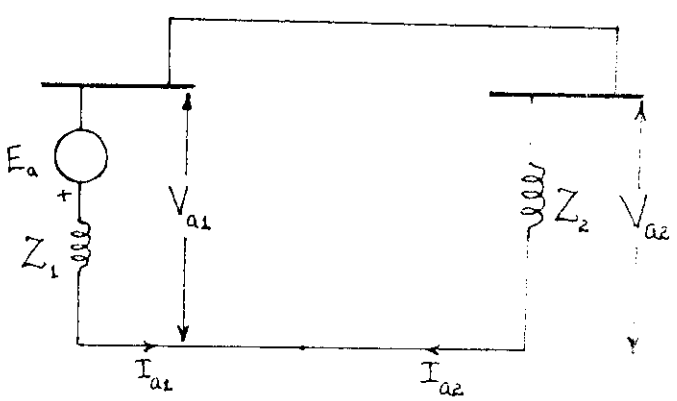


FIG. 2·14 : CONNECTION OF SEQUENCE NETWORK TO REPRESENT LINE TO LINE FAULT.

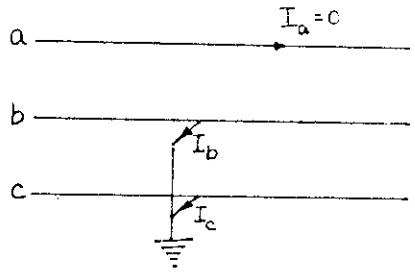


FIG. 2.15 : DOUBLE LINE TO GROUND FAULT.

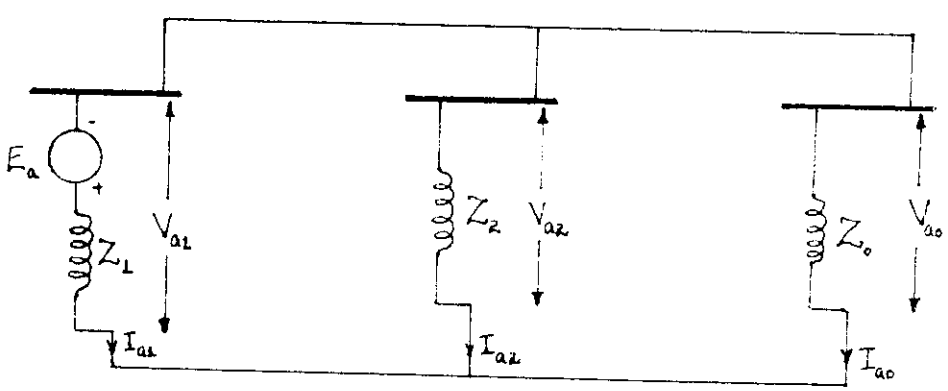


FIG. 2.16 : CONNECTION OF SEQUENCE NETWORKS TO REPRESENT A DOUBLE LINE TO GROUND FAULT.

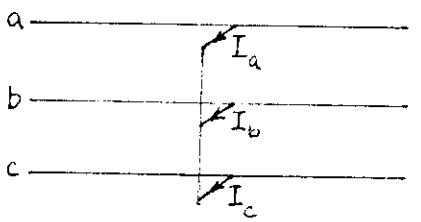


FIG. 2·17 : THREE PHASE FAULT.

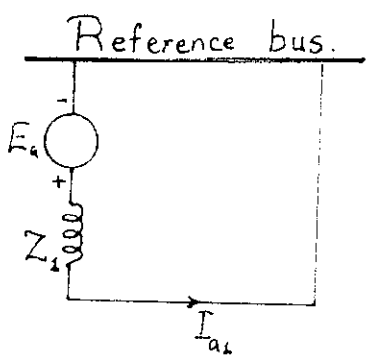


FIG. 2·18 : CONNECTION OF SEQUENCE NETWORKS TO REPRESENT A THREE PHASE FAULT.

CHAPTER 3

OPERATIONAL AMPLIFIERS AND VOLTAGE REGULATORS

3.1 THE IDEAL OPERATIONAL AMPLIFIER :

An operational amplifier is considered is considered ideal if it offers

1) Infinite voltage gain.

2) Infinite Input impedance.

3) Zero output impedance.

Such op-amp can be called as a voltage-controlled voltage source.

The advantage of an idea op-amp is that it can be used to perform a large number of mathematical operation or generate number of circuit functions by applying passive feed back around the amplifier. If the input and output impedance levels are respectively high and low with respect to the feed back impedances, and if the voltage gain is sufficiently high, then the resulting amplifier performance becomes solely determined by the external feedback components.

The symbol for operational amplifier is given in Fig 3.1.

Here the voltage gain A_v is greater than zero. Equivalent circuit for op-amp is given in fig 3.2

The output voltage V_o is an amplified signal of V_i, which is applied to input, and is equal to (V_1-V_2). Signal appearing at the negative terminal (V_2) is inverted at the output and the signal appearing at the positive terminal (V_1) has no change in sign. Hence the negative terminal is called the inverting terminal and the positive terminal is called the non-inverting terminal.

3.1.1 CHARACTERISTICS OF AN OP-AMP :

1) The voltage gain $A_v \dashrightarrow \infty$, The output voltage $V_o = -A_v V_i$ is finite, (ie) $V_o < \infty$, thus, as $A_v \dashrightarrow \infty$ it is required that $V_i = 0$.

2) If the input resistance $R_i \dashrightarrow \infty$. consequently no current enters either of the input terminal. Thus $I_1 = I_2 = 0$

3) The output resistance $R_o = 0$.

4) When $V_1 = V_2$, $V_o = 0$, this means zero offset.

5) The band width is finite.

3.1.2 VIRTUAL GROUND CONCEPT :

The voltage $V_i = 0$ implies the terminal 1, has same potential as that of terminal 2, since terminal 2 is grounded. Hence terminal 1 is virtually grounded. Thus we can say that there is virtual ground at the negative terminal as shown in Fig.3.3. The term `virtual' is used to imply that the feedback serves to keep the voltage V_i at zero, no current actually flows from terminal 1 to terminal2. So the virtual ground has a zero voltage can sink infinite current while a virtual ground has a zero voltage and zero current.

3.2 INVERTING AND NON INVERTING AMPLIFIERS

3.2.1 INVERTING AMPLIFIER :

The inverting op-amp is shown in the Fig. 3.4.The output voltage V_o is feedback to the inverting input terminal through the R_f - R_1 network. Here R_f is the feedback resistance and R_1 is the input resistance. V_i is the input signal applied to the inverting input terminal.

For ideal op-amp $V_d = 0$.

Now,

$$I_i = \frac{V_i - V'}{R_1} \quad \text{and} \quad I_f = \frac{V' - V_o}{R_f}$$

By virtual ground concept $V' = 0$ and $I_i = I_f$.

$$I_i = \frac{V_i}{R_1} \quad \text{and} \quad I_f = -\frac{V_o}{R_f}$$

$$A_v = \frac{V_o}{V_i} = -\frac{R_f}{R_1} \qquad \text{--------->} \qquad 3.1$$

The term V_o/V_i is referred to as the closed loop voltage gain of the inverting op-amp. For inverting amplifier the closed loop gain reverses because of the reverse sign of the input signal and output is out of phase with input.

3.2.2 NON - INVERTING AMPLIFIER :

The non - inverting amplifier configuration is shown in fig 3.5. Here the input is applied to the positive terminal of the op-amp.

The voltage V_1 is same as V_i since the potential difference is zero according to virtual ground concept. Now R_f and R_1 forms a potential divider.

Here,

$$V_i = \frac{V_o}{R_1 + R_f} R_1$$

$$A_v = \frac{V_o}{V_1} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1} \quad \text{----> 3.2}$$

3.3 FREQUENCY RESPONSE :

Ideally, an op-amp should have an infinite bandwidth. This mean that, if the open loop gain is 90dB with dc signal its gain should remain the same 90dB through audio and on to high radio frequencies. But the practical op-amp gain decreases at higher frequencies. This is due to the presence of capacitive component in the equivalent circuit of the operational amplifier. The capacitance is due to the physical characteristics of the device used and the internal construction of op-amp.

For an op-amp with only one break frequency, all the capacitor effects can be represented by a single capacitor 'C' as shown in fig. 3.6. This figure represents the high frequency model of the op-amp with a single corner - frequency. It may be observed that the high frequency model of the figure shown is a modified version of the low frequency model with a capacitor 'C' at the output. There is one pole due to R_o.C and obviously one -20dB/decade comes into effect.

The open loop voltage gain of an op-amp with only one corner frequency is obtained from the figures shown in Fig 3.7 A and Fig 3.7B.

$$V_o = \frac{-j X_c}{R_o - j X_c} A_{oL} \cdot V_d$$

$$A_v = \frac{V_o}{V_d} = \frac{A_{oL}}{1 - \frac{R_o}{j X_c}} = \frac{A_{oL}}{1 + j 2\pi f C R_o}$$

$$A_v = \frac{A_{oL}}{1 + j(f/f_1)} \quad \text{----------> 3.3}$$

Where

f_1 = $1/2\pi R_o C$ is the corner frequency of the op-amp. The magnitude and the phase angle of the open loop voltage gain are functions of frequency and can be written as

$$| A | = \frac{A_{oL}}{\sqrt{1 + \left(\frac{f}{f_1}\right)^2}} \quad \text{3. 4}$$

$$\phi = - \tan^{-1} (f/f_1) \quad \text{----------> 3.5}$$

It can be seen that

1) For frequency $f<<f_1$., the magnitude of the gain is 20log A_{oL} in dB.

2) At frequency $f = f_1$, the gain is 3 dB from the dc value of A_{oL} in dB. This frequency f_1 is called corner frequency.

3) For $f>>f_1$, the gain rolls - off at the rate of -20dB/decade (or) -6dB/Octave.

From the phase characterstics the phase angle is zero at frequency f = 0. At corner frequency f_1 the phase angle is - 45° (lagging) and at infinite frequency the phase angle is 90°.

3.4 INVERTING SUMMING AMPLIFIER :

A summing amplifier with three input voltages V_1, V_2 and V_3, three input resistors R_1, R_2, R_3 and a feedback resister R_f is shown in the figure 3.8.

By virtual ground concept $V^1 = 0$ as the non - inverting input terminal is grounded. By nodal equation

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_o}{R_f} = 0$$

$$V_o = -R_f \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right)$$

WHEN $R_1 = R_2 = R_3 = R$

$$V_o = -\frac{R_f}{R}(V_1 + V_2 + V_3)$$

$$R_f = R/3$$

$$V_o = -\frac{V_1 + V_2 + V_3}{3} \quad \text{---------->} \quad 3.6$$

3.5 COMPARATOR

A comparator is a circuit which compares a signal voltage applied at one input terminal of an op-amp with a known reference voltage at the other input terminal. It is basically an open loop op-amp with output $\pm V_{sat}$ (= V_{cc}).The circuit diagram for the comparator is shown in the fig. 3.9.

The circuit shown in fig.3.9 is called a non - inverting comparator. A fixed reference voltage V_{ref} is applied to negative input and a time varting signal V_i is applied to positive input. The output voltage is at $-V_{sat}$ for $V_i < V_{ref}$. And V_o goes to $+V_{sat}$ for $V_i > V_{ref}$. The output waveform for a sinusoidal input signal applied to the positive input is shown in fig.3.10 for positive and negative V_{ref} respectively.

3.6 ALL PASS FILTER :

The All Pass Filters (or) phase shifters permit the phase shift to be adjusted over a wide range, but in which the amplitude response remains constant, hence the name All Pass. The phase shift produced is frequency dependent. Phase delay

is equivalent to time delay and hence, phase shifter may be thought of as an incremental time delay filter (i.e) for an incremental shift in signal frequency a predictable change in time delay results as the signal traverses the filter from input to output. A phase shift of 90° will delay the signal by one quarter of cycle. The phase shifters are also called delay equalizer or phase correctors. They are useful to compensate phase change in signal that are transmitted over transmission lines, such as telephone wires.

Fig.3.11 shows the All Pass Filter circuit fig.3.12 shows the amplitude and phase response.

To analyze the circuit we can consider the circuit equivalent to one having two identical inputs. Here we don't need the change in the amplitude of the supply voltage. Hence $R_i = R_f$.

By applying the super position theorem transfer function can be found out.

From the fig.3.13

$$V_p = \frac{R}{R + 1/jwC} V_s = \frac{jwRC}{1 + jwRC} V_s \quad \text{-----> 3.7}$$

For non-inverting input amplifier

$$A_v = 1 + \frac{R_f}{R_1} = \frac{V_{01}}{V_p}$$

Here $R_f = R_1$

$$A_v = 2 = \frac{V_{01}}{V_p}$$

$$V_{01} = 2V_p = 2V_s \frac{jwRC}{1+jwRC} \qquad \text{---------->} \qquad 3.8$$

From the Fig.3.13 B

$$A_v = - \frac{R_f}{R_1} = \frac{V_{01}}{V_s}$$

Here V_1 is virtually grounded. So the above expression can be obtained from the voltage gain equation of the inverting op-amp.

$$V_{02} = - V_s$$

$$V_o = V_{01} + V_{02}$$

$$jwRC = \frac{2 V_s}{1 + jwRC} - V_s$$

$$= V_s \frac{2jwRC - jwRC}{1 + jwRC}$$

$$= V_s \frac{jwRC - 1}{jwRC + 1} \quad \text{---------->} \quad 3.9$$

Taking laplace transform on both the sides

$$V_o(S) = V_s(S) \frac{SRC - 1}{SRC + 1}$$

$$T.F = \frac{S - 1/RC}{S + 1/RC}$$

$$= \frac{S - a}{S + a} \quad \text{---------->} \quad 3.10$$

$$T(jw) = \frac{jwRC - 1}{jwRC + 1}$$

$$= \frac{j2\pi fRC - 1}{j2\pi fRC + 1}$$

$$= \frac{(f/f_c) - 1}{(f/f_c) + 1}$$

where $f_c = 1/2\pi RC$

The amplitude response is

$$| T(jw) | = \frac{\sqrt{1 - (f/f_c)^2}}{\sqrt{1 + (f/f_c)^2}} \qquad 3.12$$

The phase response is

$| \phi (jw) = -\tan^{-1} (f/f_c) - \tan^{-1} (f/f_c)$

$= -\tan^{-1} (2\pi fRC) - \tan^{-1} (2\pi fRC)$

$= -2 \tan^{-1} (2\pi fRC)$ -----> 3.13

The phase shift can be provided by this arranggement of from 0 to 180°.

Phase shift = $180° - 2 \tan^{-1} (2\pi fRC)$ -------> 3.14

VOLTAGE REGULATORS :

3.7 Type and function :

The function of a voltage regulator is to provide a stable dc voltage for powering other electronic circuits. A voltage regulator should be capable of providing substantial output current. The voltage regulators are classified as

1) Series voltage regulator

2) Switching regulator

Series regulators use a power transistor connected in series between the unregulated dc input and the load. The output voltage is controlled by the continuous voltage drop taking place across the series pass transistor. Since the transistor conducts in the active (or) linear region, these regulators are also called linear regulators. These may have fixed or variable output voltage and could be positive or negative. Example for linear regulators are 78XX series and IC723

3.7.1 IC VOLTAGE REGULATORS :

The fixed IC voltage regulator are having low cost, high reliability, reduction in size and excellent performance. Example for these type are 78XX/79XX series regulators.

78XX series are three terminal, positive fixed voltage regulators. There are seven output voltage options available such as 5,6,8,12,15,18 and 24V. In 78XX the last two numbers indicate the output voltage. Thus 78XX represents a 5V regulator. There are also available 79XX series of fixed output, negative voltage regulators which are complements of 78XX series devices. Fig. 3.14 shows the standard representation of monolithic voltage regulator. A capacitor Ci (0.33 mF)

is usually connected between input terminal and ground to cancel the indicative effects due to long distribution leads. The output capacitor (1MF) improves the terminal response.

3.7.2 CHARACTERISTICS OF REGULATORS :

There are 4 characteristics of three terminal IC regulators which must be mentioned.

1) **V_o :** The regulated output voltage is fixed at a value as specified by the manufacturers. There are a number of models available for different output voltages. For examble 78XX series has output voltage at 5,6,8 etc

2) **$V_{in} > V_o + 2$ volts :** The unregulated input voltage must be atleast 2V more than the regulated output voltage. For example if $V_o = 5V$, then $V_{in} = 7V$.

3) **I_o max :** The load current may vary from zero to rated maximum output current. The IC is usually provided with a heat sink, otherwise it may not provide the rated maximum output current.

4) **Thermal shutdown :** The IC has a temperature sensor which turns off the IC when it becomes too hot. The output current will drop and remain ther until the IC has cooled significantly.

3.8 FIXED VOLTAGE REGULATOR :

The figure 3.16 shows the fixed voltage regulators circuit. Let the required output be +5V.

The supply voltage is reduced to the required level by the use of step down transformer. This will be rectified and is given to the regulator input as shown in the figure. So the output will be at +5V whatever be the change in the input.

These type of regulator are widely used since this occupies very small size and the output will be accurate.

3.8.1 DUAL VOLTAGE SUPPLY :

Many discrete IC circuit like op-amp require bipolar (dual (or) ± V) supplies. This can be easily done with two, three terminal regulators. The Fig 3.17 shows the one such type for the output of ± 12V.

The input voltage can be reduced to appropriate level by using the transformer. This will be rectified by means of the bridge rectifier. This will be rectified by means of the bridge rectifier. So the dual output can be obtained through 7812 and 7912 regulator ICs.

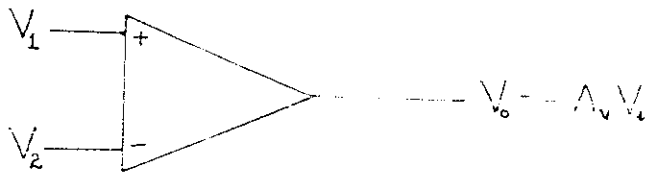


FIG. 3·1 : IDEAL OPERATIONAL AMPLIFIER.

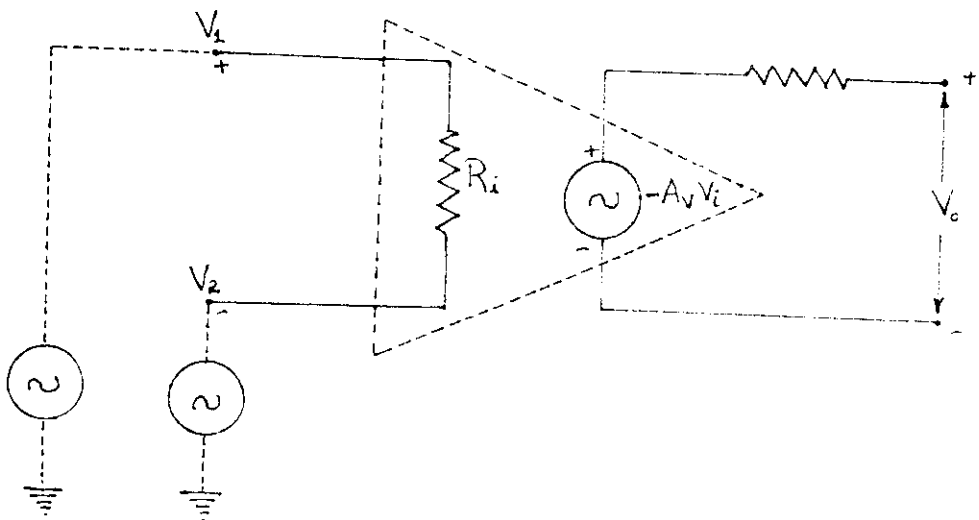


FIG. 3·2 : EQUIVALENT CIRCUIT OF AN IDEAL OP-AMP.

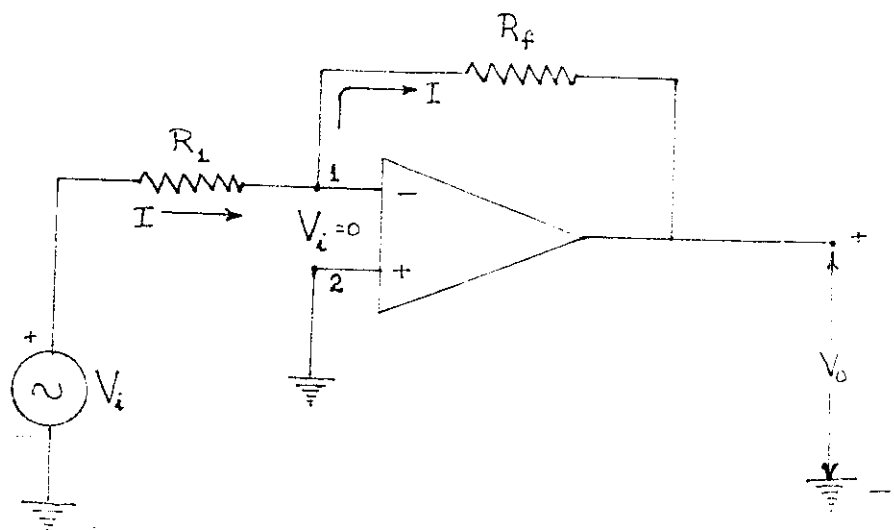


FIG. 3·3 : INVERTING AMPLIFIER.

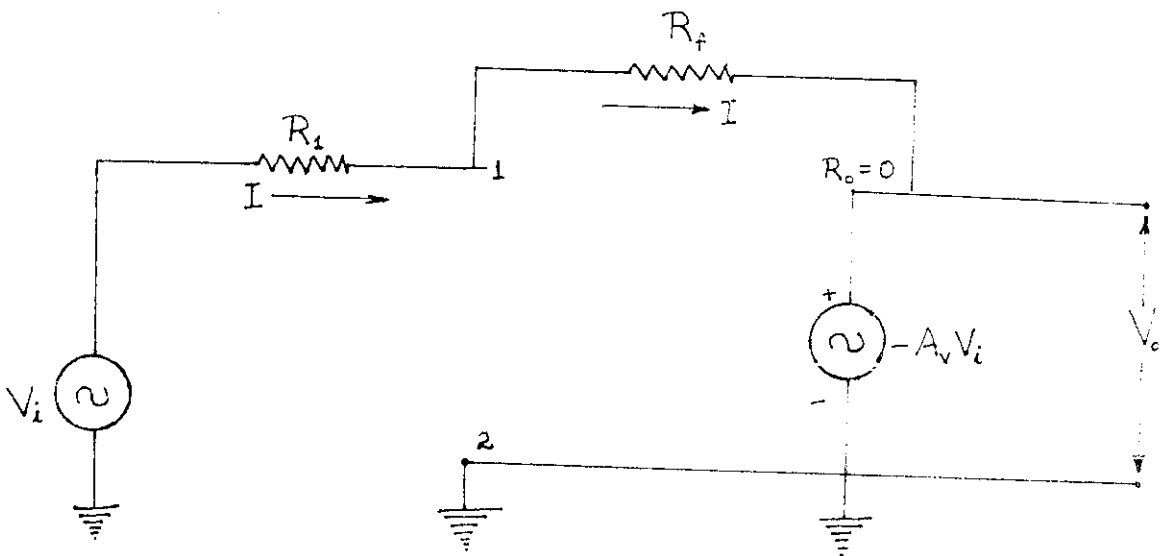


FIG. 3.4 : EQUIVALENT CIRCUIT OF INVERTING AMPLIFIER

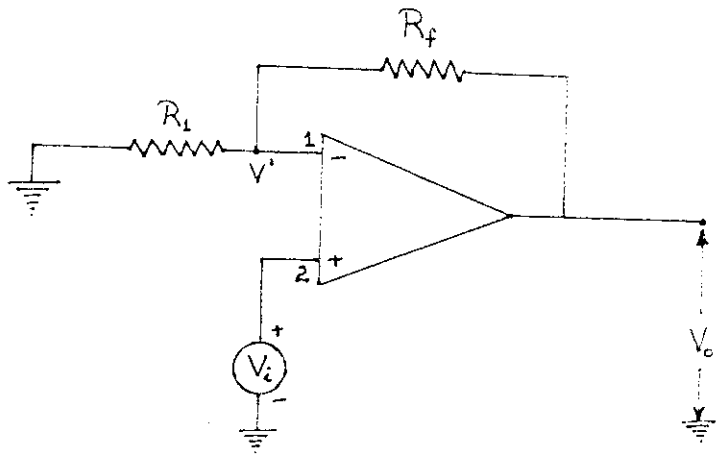


FIG. 3.5 : NON- INVERTING AMPLIFIER.

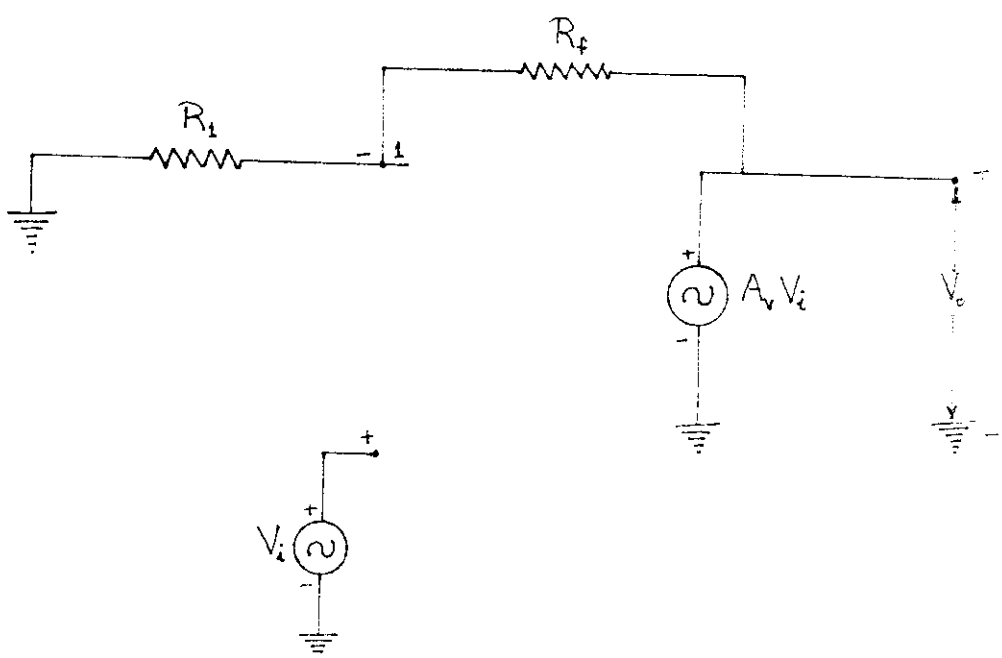


FIG. 3.5 : EQUIVALENT CIRCUIT OF NON- INVERTING AMPLIFIER.

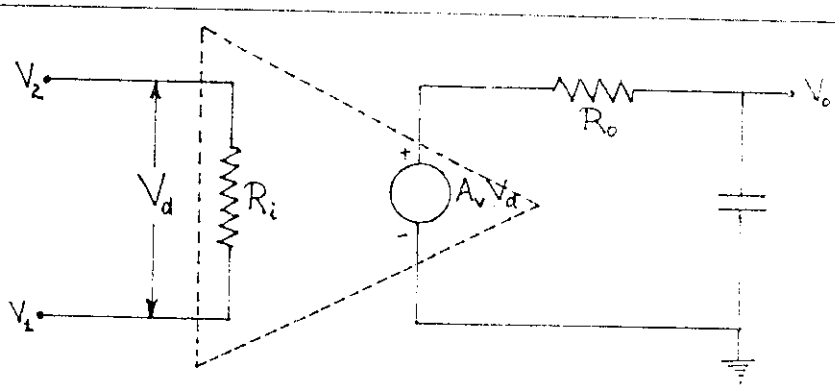


FIG. 3.6 : FREQUENCY RESPONSE.

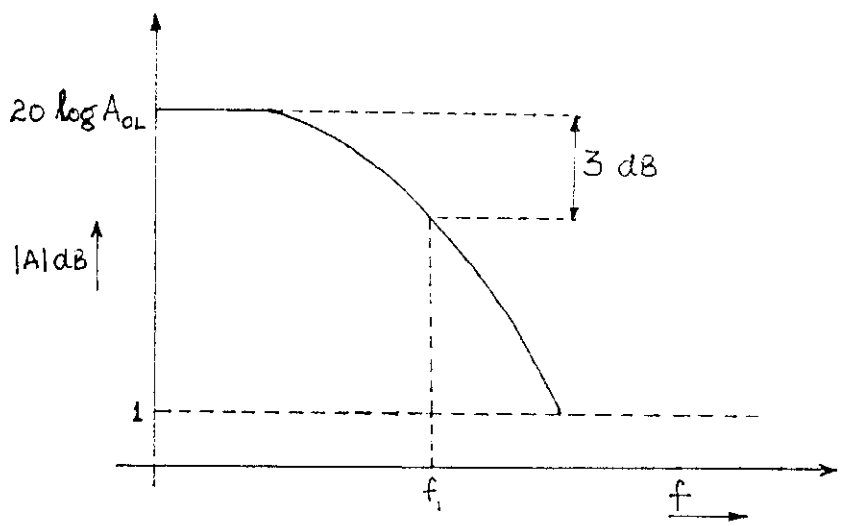


FIG. 3.7A : OPEN LOOP MAGNITUDE CHARACTERISTICS.

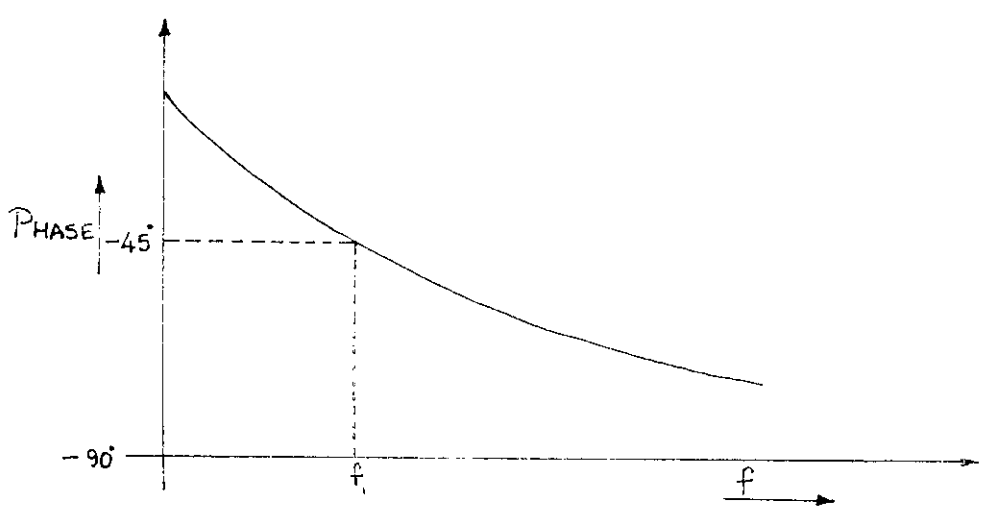


FIG. 3.7B : PHASE CHARACTERISTICS.

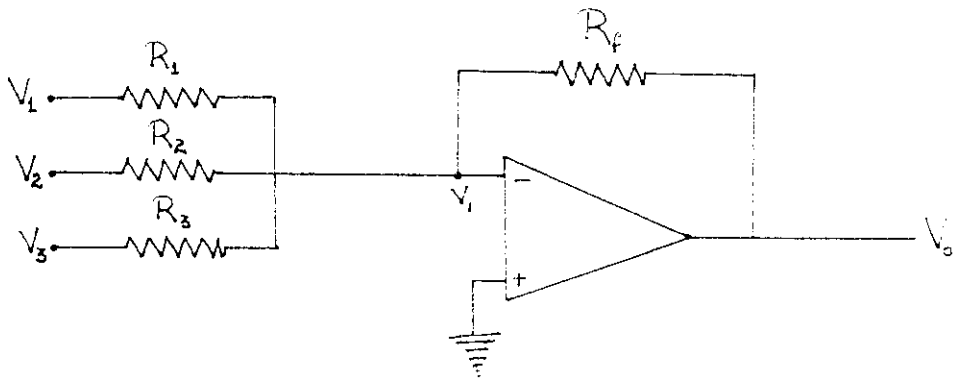


FIG. 3·8 : INVERTING SUMMING AMPLIFIER.

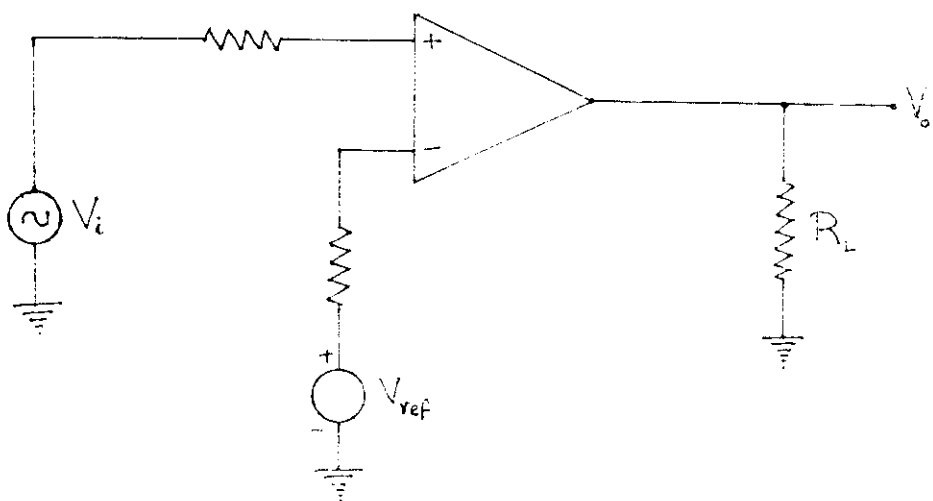


FIG. 3·9 : COMPARATOR.

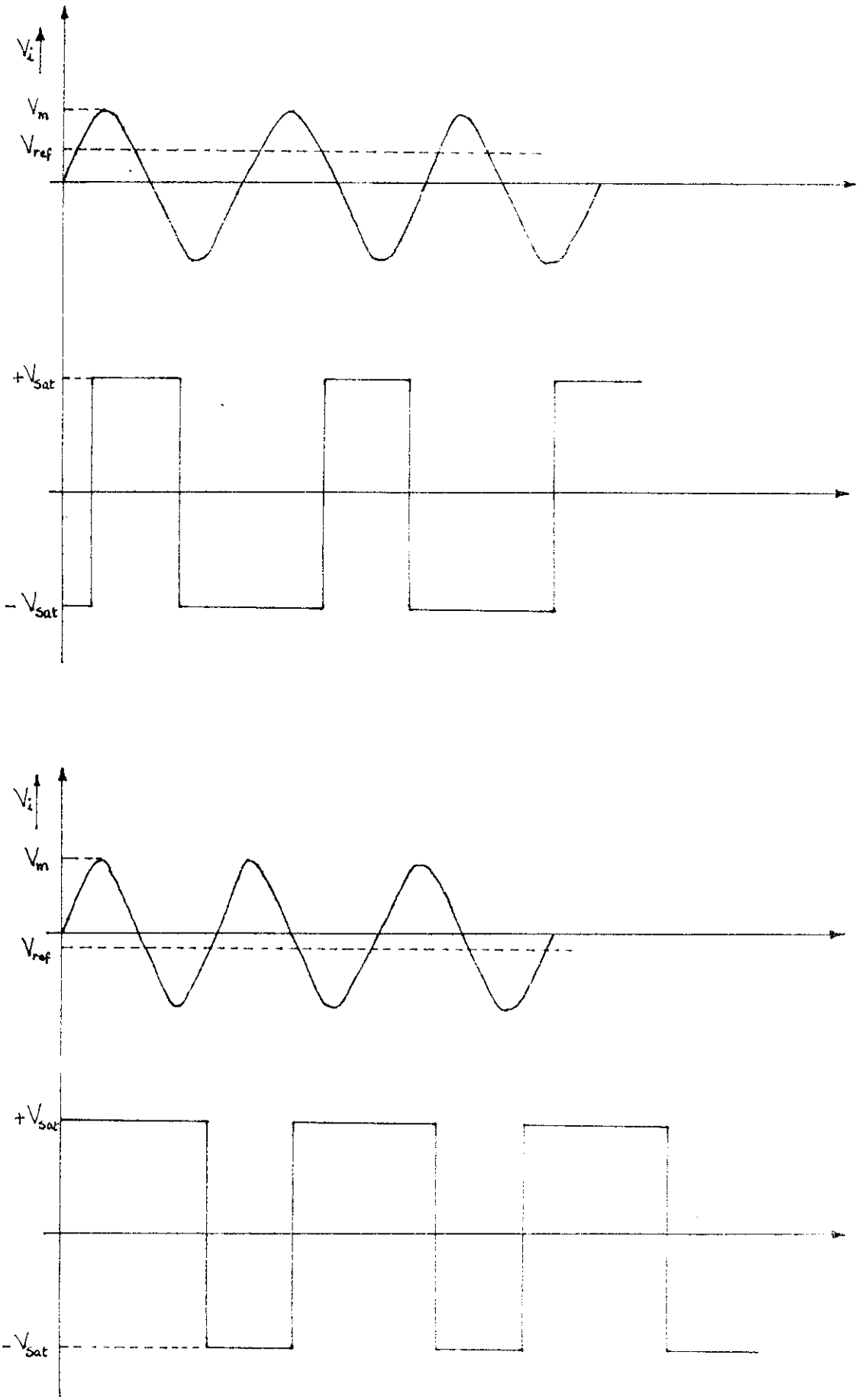


FIG. 3.10 : OUTPUT WAVEFORMS OF COMPARATOR.

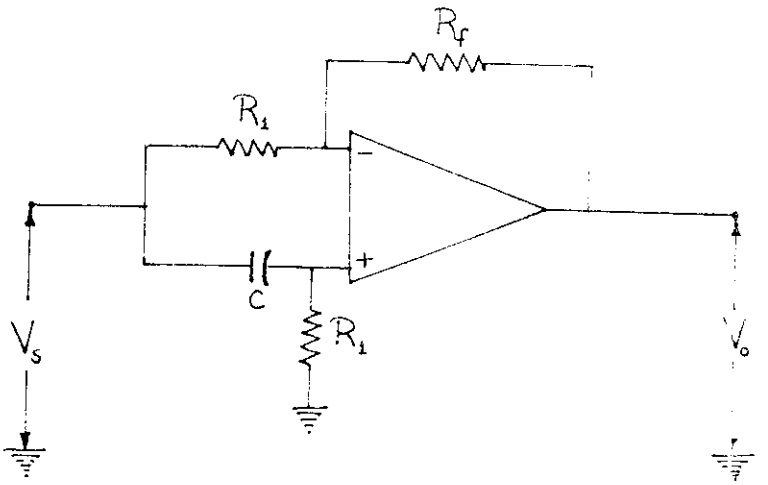


FIG. 3·11 : ALL PASS FILTER.

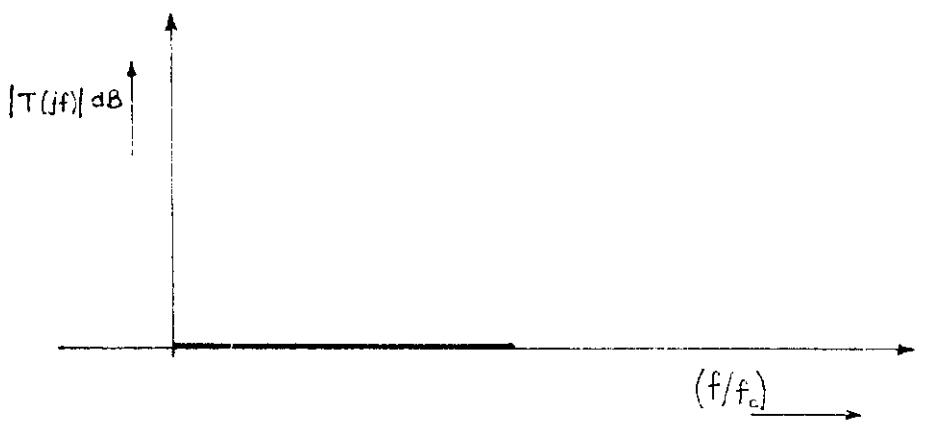


FIG. 3·12 A : AMPLITUDE RESPONSE

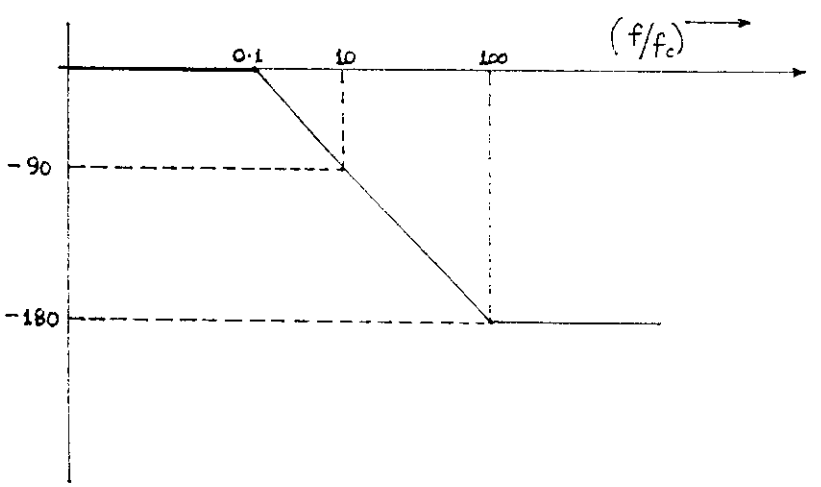


FIG. 3·13 B : PHASE RESPONSE.

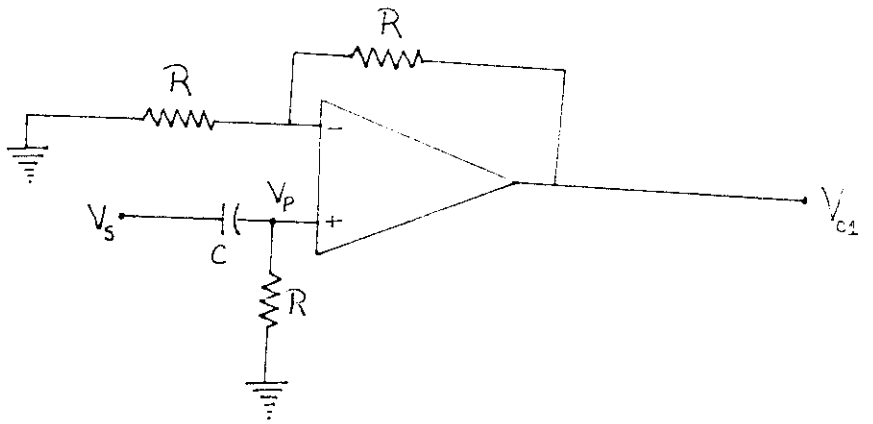


FIG. 3·13A : APF DESIGN

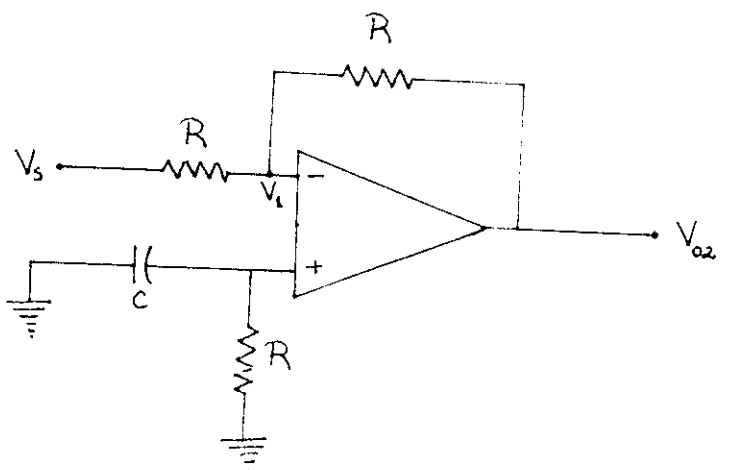


FIG. 3·13B : APF DESIGN

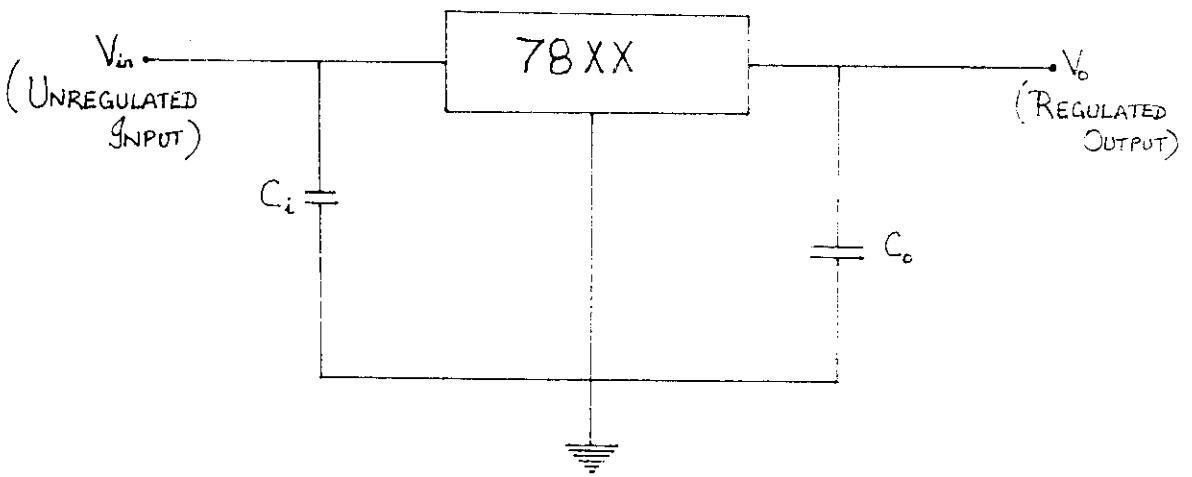
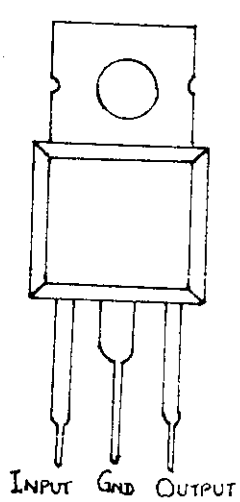
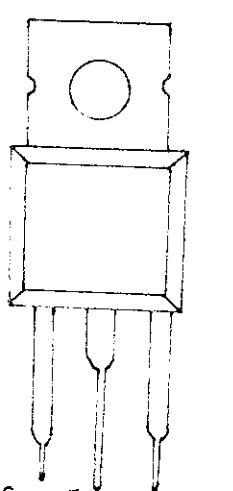


FIG. 3·14 : I·C· VOLTAGE REGULATOR.



78XX



79XX

FIG. 3·15 :

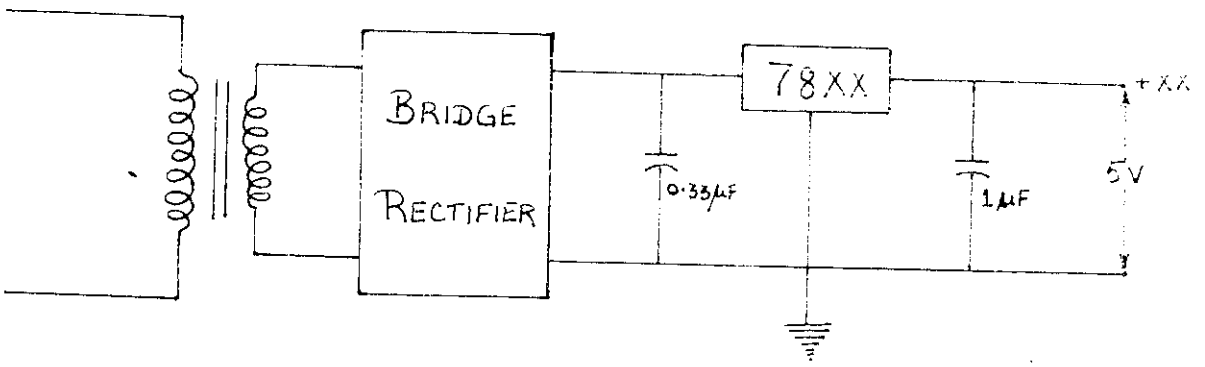


FIG. 3·16 : FIXED VOLTAGE REGULATOR.

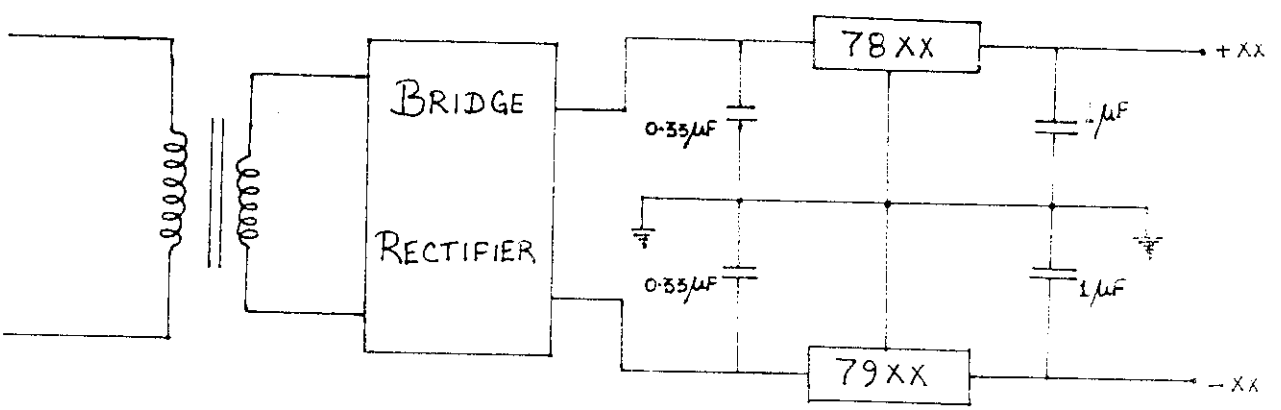


FIG. 3·17 : DUAL VOLTAGE SUPPLY.

CHAPTER IV

DESIGN AND DEVELOPMENT

4.1 DESIGN :

The symmetrical components can be related with the terminal voltage with the help of equation 2.10 which is given by

$$\begin{bmatrix} V_0 \\ V_1 \\ V_2 \end{bmatrix} = 1/3 \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$$

Here 'a' represents the phase shift of 120°. Which is obtained by using the all pass filter discussed in 3.6 of chapter 3.

For extraction of the symmetrical components we need the proper design of All Pass Filter and the input voltage which explained in 4.2 of chapter 4.

4.2 DEVELOPMENT :

4.2.1 SUPPLY VOLTAGE :

The circuit used for converting unsymmetrical components to symmetrical component is designed by using the operational amplifier, which require a small voltage for its input. Hence the supply voltage is stepped down by using the potential transformer(6V).

4.2.2 DESIGN OF ALL PASS FILTER :

The schematic diagram of the All Pass Filter is shown in fig 4.21. Here we require a phase shift of 120°. For the design of All Pass Filter we require the values for R and C which can be obtained from the phase shift equation 3.14 of chapter 3.

$$\text{Phase shift} = 180^\circ - 2\tan^{-1}(2\pi fRC)$$

$$120^\circ = 180^\circ - 2\tan^{-1}(2\pi fRC)$$

$$RC = 1.8377 \times 10^{-3}.$$

Here we should assume a proper value for `C' If the value `C' is in picofarad then the tolerance value will be in between 10% to 30% of its designed value. If it is in the range of milli farad, the physical size of the capacitor will be big. So for normal operating conditions capacitors of micro farad range are used. Taking these considerations micro farad capacitor is chosen whose tolerance value is between + 10% to +20%.

So,

$$R = \frac{1.8377 \times 10^{-3}}{0.1 \times 10^{-6}} = 18.377\ \text{K}\ \Omega$$

240° phase shift can be obtained by using the cascaded connection of two 120° phase shift all pass filters. From the Fig 4.22, point `a' represents the phase shift of 120° and `b' represents the phase shift of 240°.

4.2.3 DESIGN OF SUMMING AMPLIFIER :

To obtain the symmetrical components V_o, V_1 and V_2 we have to sum up the input voltages with the required phase shift which is given by the equation 2.10 of chapter 2.

The summing amplifier is explained in chapter 3.4. Here we need the proper values of R_1, R_2,R_3 and R_f which is shown in the fig 4.23. Here the magnitude of the voltage levels are equal. Hence we can choose $R_1 = R_2 = R_3$. We require the same magnitude of input voltage at the summing point hence the same value of R which is used in the design of All Pass Filter is used. So the complexity involving in different values of resistors will also be reduced. So the output voltage from the summing amplifier will be

$$V_o = \frac{-R_f}{R}(V_1+V_2+V_3)$$

which is explained in chapter 3.4. we require the output voltage is have same magnitude.

$$V_o = \frac{V_1 + V_2 + V_3}{3}$$

Hence we use the value of $R_f = R/3$ to obtain the required voltage level.

4.2.4 DESIGN OF COMPARATOR AND ZENER DIODE :

During faulted condition the symmetrical components will be of less magnitude. In order to operate the circuit breaker, we require a voltage of 5V. Hence a comparator circuit is used as a zero crossing detector which is been explained in chapter 3.5.

When a voltage is sensed at the input terminal of the components then it drives the output from $+V_{sat}$ to $-V_{sat}$. This will be in the range of + 12V to - 12V. In order to limit the voltage level a zener diode of rating 5.1 volts is used.

4.2.5 DESIGN FOR PROTECTIVE RELAYING :

When a fault occurs the symmetrical component voltages will be sensed for energising the relay coil. So two input EX-NOR and NAND gates are used.

The truth table for EX-NOR and NAND gates are as follows

EX - NOR			NAND		
Input		Output	Input		Output
x	y	z	x	y	z
0	0	1	0	0	1
0	1	0	0	1	1
1	0	0	1	0	1
1	1	1	1	1	0

The advantage of having EX-NOR is that if both the inputs are same than only the output will be at high level else if will be at low level. The advantage of using NAND gate is that when any one of the input is at low level then the output will have high level.

During faulty condition the symmetrical components voltages will be given with the supply voltage to the NAND gates. So the effective way of protection can be given which is been discussed in detail in chapter 5.

4.2.6 VOLTAGE REGULATORS :

Voltage regulators are used for the excitation of 741 ICs and digital ICs such as 7400, 7404 and 7421. 741 ICs require the voltages of +12V and -12V.

This can be obtained by using the dual voltage supply regulators as has been discussed in chapter 3.8. For this operation ± 30 V dc input is required. This can be obtained by using the potential transformer and bridge rectifier as shown in Fig 4.24. For +12V and -12V output, IC 7812 and IC 7912 voltage regulators are used.

For digital IC's we require the voltage of +5V for excitation. This can be obtained by using the fixed voltage regulators as been discussed, in chapter 3.8. This requires the voltage of + 6V dc as its input. This can be obtained by using the potential transformer and bridge rectifier unit as shown in figure 4.25. For the fixed +5V output IC 7805 regulator is used.

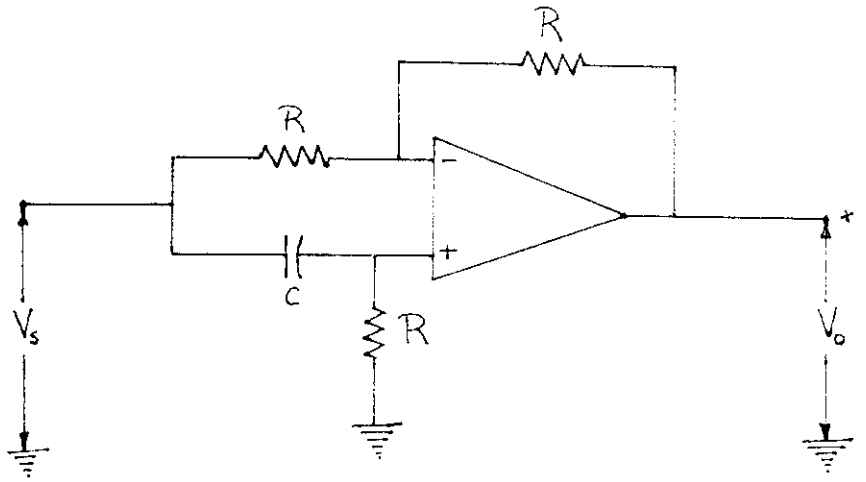


FIG. 4·1 : ALL PASS FILTER.

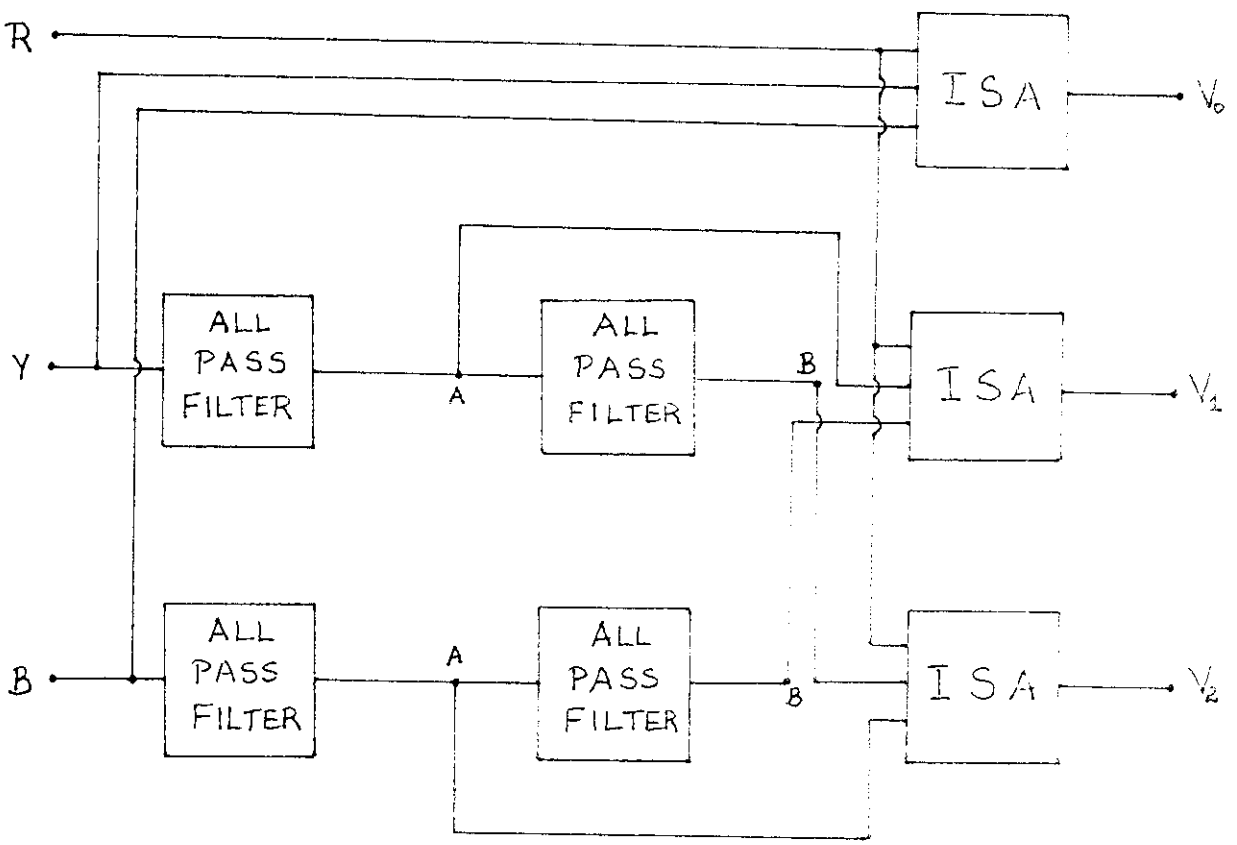


FIG. 4·2 : BLOCK DIAGRAM FOR SEPARATION OF SYMMETRICAL COMPONENTS

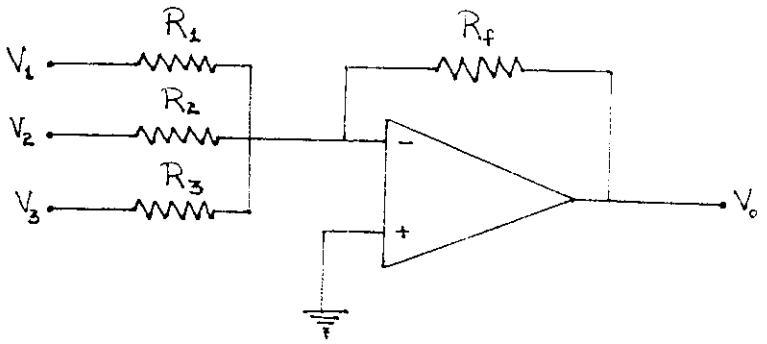


FIG. 4·3 : INVERTING SUMMING AMPLIFIER.

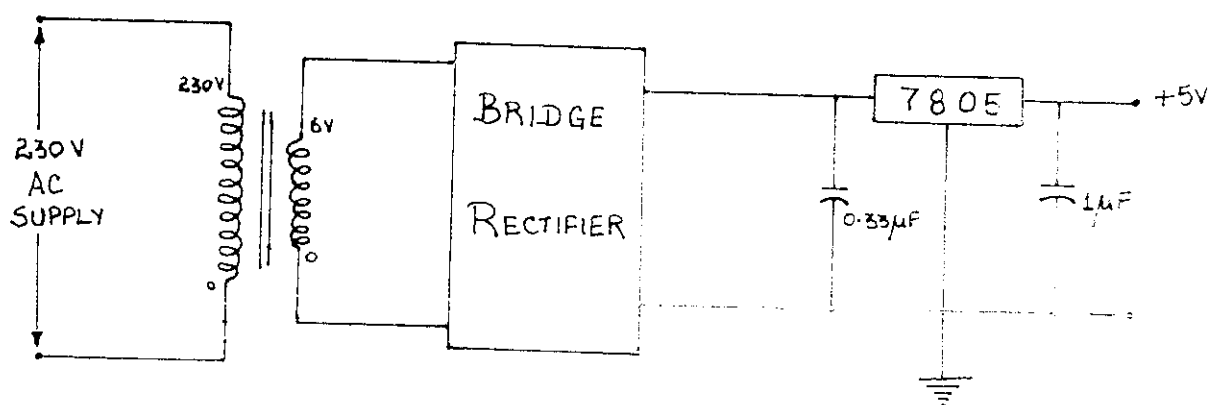


FIG. 4·4 : FIXED VOLTAGE REGULATOR.

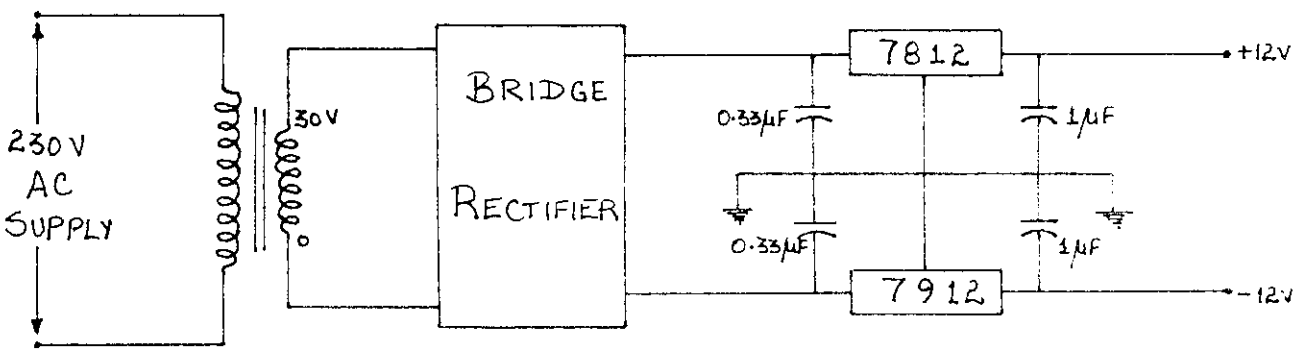


FIG. 4·5 : DUAL VOLTAGE SUPPLY.

CHAPTER V

FABRICATION AND TESTING.

5.1 FABRICATION :

The layout for the entire circuit is shown in Fig.5.1. PCB fabrication is done for the entire circuit the advantage of PCB is that the component can be fixed and connected as compact as possible. Hence size of the circuit will be as minimum as possible. Risk of short circuit due to running of the wires for connecting the components is avoided. In case of huge production the cost will be cheaper.

5.2 TESTING:

For each fault condition the circuit has been tested and verified with the test data. The fault conditions for which the circuit is tested are.

5.2.1 LINE TO GROUND FAULT :

Let the fault occur between phase R to neutral. In this case all the symmetrical components of voltages will have some value. Similarly the phase R will have zero magintude with respect to neutral and Y and B phase will have its own magnitude.

Initially V_0 and V_1 are given to EX-NOR. So the output will be at high level. Again this is componed with V2 through EX-NOR. So this output will also be at high level. Hence for all the 3 NAND gates one input terminal will be at high level. The second input terminal, only R phase input will be at low level and for the remaining other 2 phases it will be high level. So the circuit breker corresponds to R phase will be tripped since one of the input is at low level. This function has been discussed in 4.2.5 of chapter4

5.2.2 LINE TO LINE FAULT :

Let the fault occur between phases R and Y, In this case V_0 will be at low level and V_1 and V_2 will be at high level. The output of EX-NOR will be at low level. Here the B phases will be at low level and R and Y phases will be at high level. So the phases R and Y will be tripped.

5.2.3. DOUBLE LINE TO GROUND FAULT:

Let the fault occur between phases Y,B and ground. So the phases Y and B will be at low level and R will be at high level. Hence V_0, V_1 and V_2 will be at high level. So the output of EX-NOR will be at high level. This is given to the NAND gate with phase voltages. So the phases Y and B will be tripped

5.2.4. THREE PHASE FAULT:

In this case all the symmetrical components will have low level and also the phase magnitude, so the output of EX-NOR will be at low level. Here all the 3 Phases will be tripped since all the phases will have zero value with respect to the neutral.

CHAPTER 6

CONCLUSION

A technique for determining the faulted linesand the opening up the same line during fault condition has been developed and tested. This circuit can be used for the protection of Transmission lines.

This is based on the symmetrical components produced during fault condition. This method is very simple, accurate, and cheaper.

For the extraction of symmetrical components, electronic components are used. The use of electronic components reduces the operating time of the protective system.

REFERENCES

1. J.NANDA and D.P.KOTHARI, "**Recent trends in electric energy systems**", Printice Hall International Limited, New Delhi - 1984

2. K.R.BOTKAR, "**Integrated Circuits**" Khanna Publishers, New Delhi - 1985.

3. D. ROYCHOUDARY and SHAIL JAIN, "**Linear Integrated Circuits**", Wiley Eastern Limited, New Age Interational Limited, New Delhi - 1991

4. I.J.NAGARATH and D.P.KOTHARI, "**Modern Power System Analysis**", Tata McGraw Hill Publishing Company Limited, New Delhi - 1979

5. C.L.WADHWA, "**Modern Power System Analysis**", Wiley Eastern Limited, New Age International Limited, New Delhi.

6. V.K.MEHTA, "**Principles of Power Systems**", S.Chand and Company, New Delhi - 1988.