BLOODBANK AUTOMATION SYSTEM

A PROJECT REPORT

Submitted by

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BONAFIDE CERTIFICATE

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INTERNAL EXAMINER

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TO WHOMSOEVER IT MAY CONCERN

This is to certify

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Final year ECE students of KCT college has successfully completed their project entitled "BLOOD BANK AUTOMATION SYSTEM" in embedded system using PIC microcontroller at our concern.

FOR AKIRA CONTROLS

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ABSTRACT

Blood is essentially the lifeline of the human body. During emergency cases, fast accessibility of compatible blood can decide between life and death for a friend, a family member or a fellow human being. The crux of our project is to automize the blood bank storage details and to implement remote accessing of the details through GSM the amount and quantity of blood units available in the blood bank directly to the user mobile phone.

We have incorporated RFID and GSM technologies in our project along with a seven segment display module. Each of the blood bag units are fitted with passive RFID tags. When a blood bag is supplied to the blood bank, the user has to place the tag of the blood bag near the RFID reader for identification of the blood group .The RFID Processor reads the ID number in the card and the quantity of that particular blood group is incremented. If the user withdraws a blood bag, then he has to press the corresponding key so that the amount of blood bag display gets decremented. The number of blood bags of the particular blood types available currently in the blood bank (the number displayed in the display) is transmitted to the slave IC using I2C serial communication. The slave is connected to the GSM modem. When the user in the remote area sends an SMS to the SIM number present in the GSM modem, then the number of units of each blood group present in the blood bank is send as SMS to the remote user.

This automization project of the blood banks is extremely useful in case of late night, early morning accidents and other medical emergencies.It provides straightforward and prompt information about the amount of units of a particular type of blood group available in the blood banks to the user, who can make arrangements for procuring the amount required

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CHAPTER 1

INTRODUCTION

Nowadays the technology is exponentially attaining its various stepping stones and more or less it has attained its saturation level. So as far as this advancement is concerned the industrial life is slowly being fully converted, into an automated one. Actually the term automation means reducing the manual power, therefore reducing the burden of manual work to perform a particular task. Automation not only reduces the man power but also it avoids the human error and provides proficient accuracy in the task that is going to be performed.

Automation provides the utmost security for the work that is to be performed. Time consumption is reduced by this automation and the total cost of the project can be considerably reduced by subjecting the system to automation. Now as far as the technical and modernized world is concerned, the automation plays a vital role and it occupies the core area in our project, which aims at making blood bank system as an automated one. So this type of complication less automation gives us an easy way to save lives as well as lead our lives peacefully.

1.1. PROBLEM STATEMENT

The main objective of our project is to make available an automated blood banking system in which the manual power used is condensed to its smallest amount, the accuracy and security provided to its maximum. In the present condition, the blood banking systems are operating under the manual control; so many problems are sustained due to the currently prevailing system. The automation of the blood banking system if implemented will provide

1.2 THE BLOCK DIAGRAM OF RFID BASED BLOOD BANK AUTOMATION SYSTEM

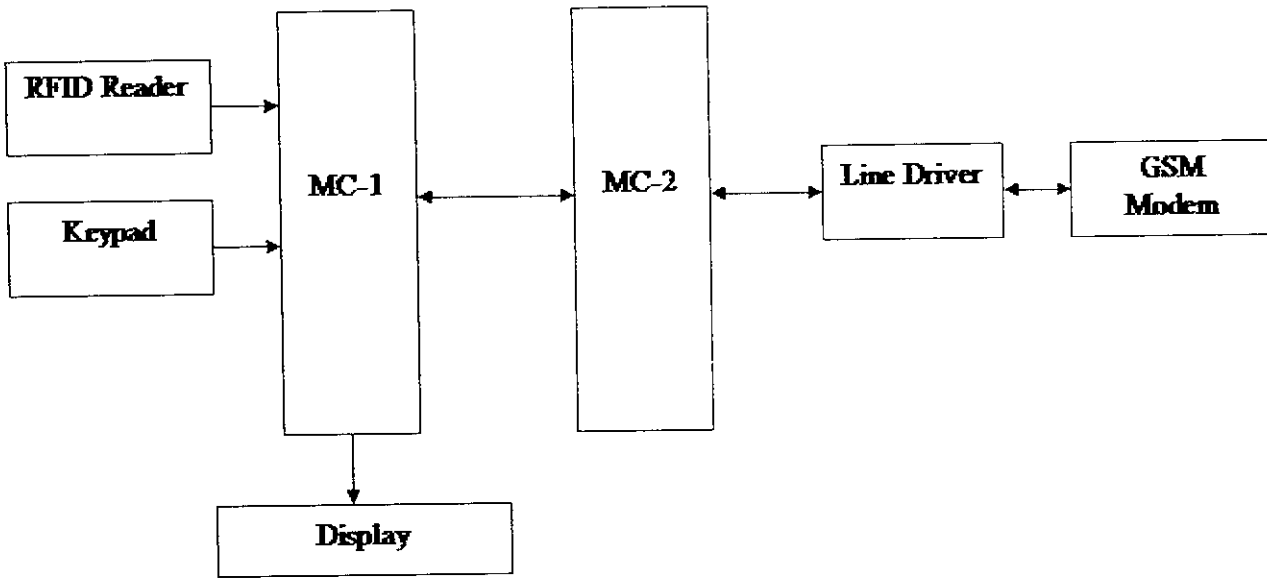


Fig 1.1: Blood bank Automation System

The Block diagram comprises of the overview of PIC microcontroller (16F873), RFID, transceiver which are shown in Fig 1.1

1.2.1 Overview of RFID Reader Block

The RFID Reader senses the Unique tag of the blood bag and increments the quantity of the corresponding blood type in the seven segment display as well as in the PIC Microcontroller. It is interfaced using ICMax232.Passive tags are used since proximity is not considered as a serious issue and for reducing cost.

1.2.2 Overview of PIC16F873A Microcontroller Block

In this project the PIC 16F873 microcontroller is used for storing the blood group and availability details. We use two PIC16F873 Microcontrollers; one is configured as master and the other as slave. The Master

as well as the slave with the blood bank details. The Slave is connected to the GSM module through the MAX232 IC and is responsible for reading incoming messages, checking for the proper text parameters and replying the status of the blood groups Via SMS provided the parameters in the SMS received matches the specified keywords. USART is serial communication protocol, which is for Micro controller to mobile communication.

1.2.3 Overview of IC MAX232 Block

Transceiver is an IC MAX 232. It is a RS 232 transceiver IC. It is popularly known as voltage shifter. It converts CMOS level micro controller data into RS232 level data and vice-versa. It internally consists of voltage doublers and inverters.

1.2.4 Overview of the GSM Modem Block.

The GSM Modem is an external modem device, such as the Wavecom FASTRACK Modem. GSM SIM card is inserted into this modem, and is connected to the slave microcontroller using an available serial port through RS232 protocol and IC MAX232.

1.3 MODULES:

A brief overview of the project modules are explained below for better understanding of block diagram:

- Power Supply
- RFID Reader module
- PIC Microcontroller (PIC16F873A)
- Seven Segment LED display
- GSM Modem

1.4 OVERALL CIRCUIT DIAGRAM

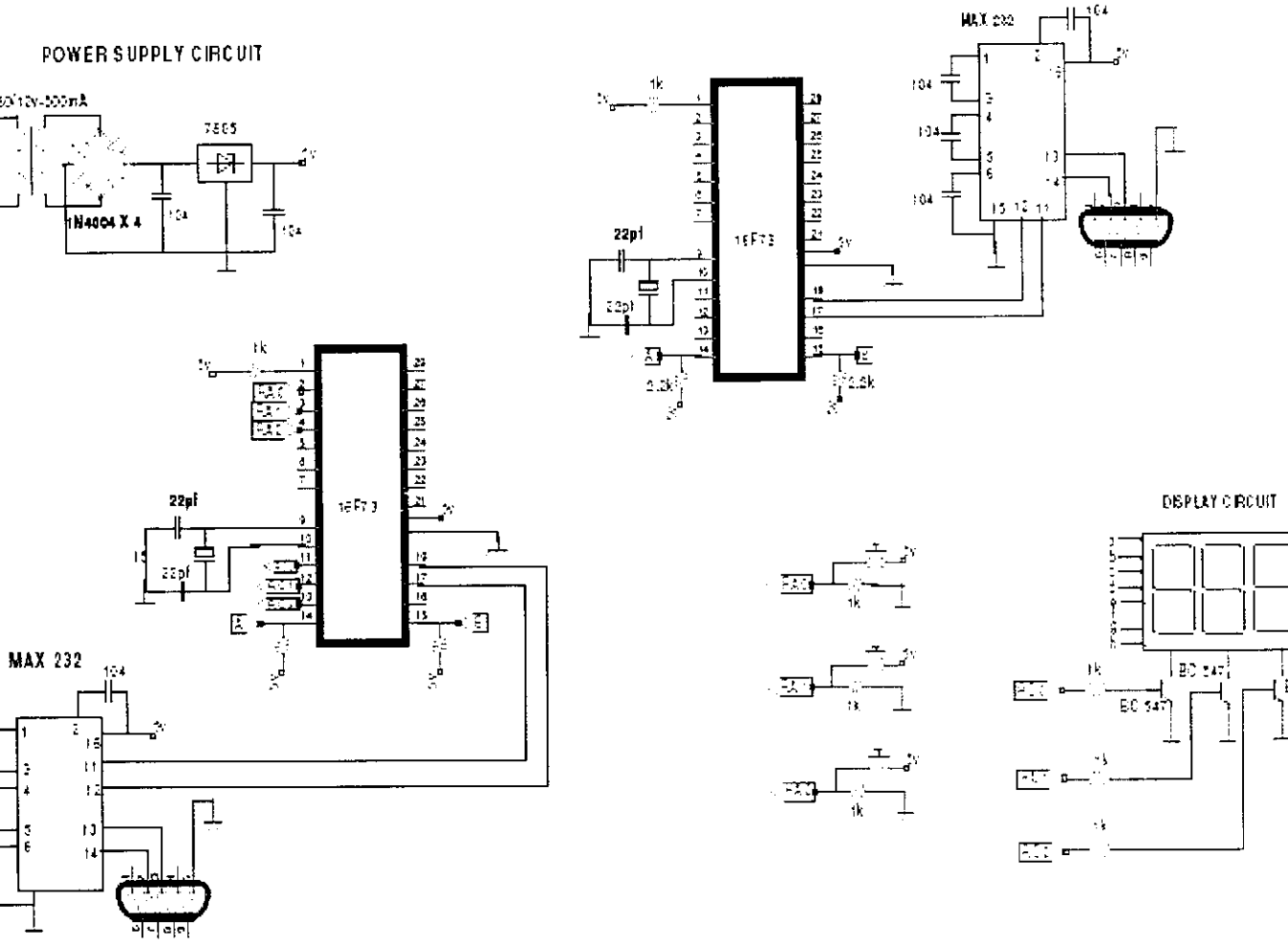


Fig1.2 Circuit diagram

CHAPTER 2

RFID READER MODULE

2.1 RFID SYSTEM

Although it may seem like a new technology, Radio Frequency Identification (RFID) has been around since the 1940's. In fact the United States Air Force first used RF id technology to track friendly aircraft in World War II.

Today, RFID has the potential to dramatically improve many applications in the industrial, transportation and service industries through automatic detection, identification, and control of products and assets. The expectation for RFID is to provide supply chain efficiencies, reduced labor costs, and accurate real-time resource information.

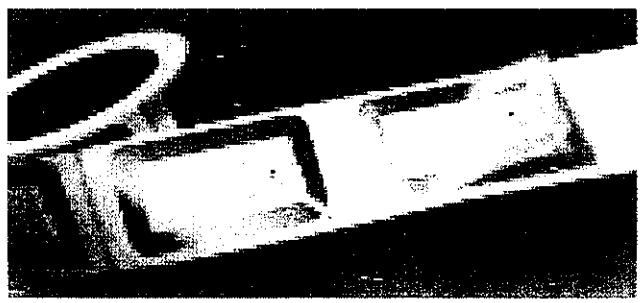


Fig.2.1 RFID Strip

2.2 DEFINITION

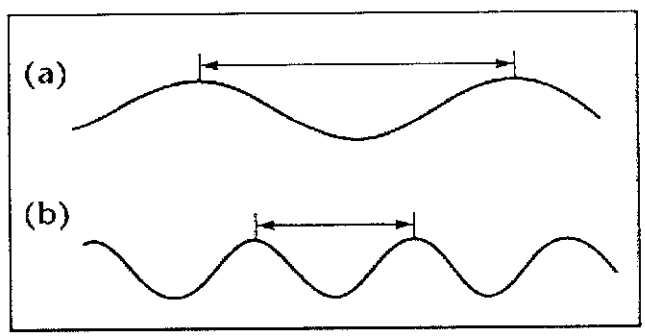
RFID is a term used for any device that can be sensed at a distance by radio frequencies or thereabouts, with few problems from obstruction or mis-orientation. The origins of the term lie in the invention of tags that reflect or re-transmit a radio frequency signal. In its current usage, those working below 300 Hz and those working above 300 MHz, such as microwave (GHz) tags, are included. For example, one type of chip less tag works at 100 Hz and one recent

at one frequency. Higher frequencies such as visible and infrared devices are excluded as these systems have very different properties and are frequently sensitive to obscuration, heat, light, and orientation. The term "tag" is used to describe any small device – the shapes vary from pendants to beads, nails, labels or micro wires and fibers – that can be incorporated into paper and even special printed inks on, for example, paper.

2.3 UNDERSTANDING THE RADIO FREQUENCY

Radio Frequency (RF) is all about physics. RF communication works by creating electromagnetic waves at a source and picking up those electromagnetic waves at a specified destination. These electromagnetic waves travel through the air at near the speed of light. The wavelength of an electromagnetic signal is inversely proportional to the frequency; the higher the frequency, the shorter the wavelength.

Frequency is measured in Hertz (cycles per second) and radio frequencies are measured in kilohertz (KHz or thousands of cycles per second), megahertz (MHz or millions of cycles per second) and gigahertz (GHz or billions of cycles per second). Higher frequencies result in shorter wavelengths. The wavelength for a 900 MHz device is longer than that of a 2.4 GHz device.



(a) A Long Wavelength
(b) A Short Wavelength
Note how the length of the wave affects the *frequency* of waves (two versus four in the same space).

In general, signals with longer wavelengths travel a greater distance and penetrate through, and around objects better than signals with shorter wavelengths. Imagine an RF transmitter wiggling an electron in one location. This wiggling electron causes a ripple effect, somewhat akin to dropping a pebble in a pond. The effect is an electromagnetic (EM) wave that travels out from the initial location resulting in electrons wiggling in remote locations. An RF receiver can detect this remote electron wiggling.

The RF communication system then utilizes this phenomenon by wiggling electrons in a specific pattern to represent information. The receiver can make this same information available at a remote location; communicating with no wires.

In most wireless systems, there are two primary concerns: it must operate over a certain distance (range) and transfer a certain amount of information within a time frame (data rate).

2.4. ABOUT RFID

RFID uses wireless technology operating with the 50 kHz to 2.5 GHz frequency range. A RFID system consists of a RFID tag or transponder that contains data about the tagged item/object, and antenna, a RF transceiver to generate RF signals, and a RFID reader used for collecting RFID data. which it passes to a host system for processing.

RFID does not require line-of-sight to operate for communications between a tagged object (which could be almost anything including a car, merchandise, package, files etc.) and a reader (an electronic device used to capture the RFID signal, as in the picture above).

Data encoded on the RFID tag can contain a variety of

electronic product code (EPC). The EPC is an electronic representation of a product, which can include information about the product, manufacturer, and uniquely identify the product.

2.5 WORKING PRINCIPLE OF RFID

An RFID tag consists of a microchip and a coiled antenna. RFID tags may be either active or passive. Active tags tend to be larger and more expensive than passive tags as they contain more electronics due to the fact that they actively transmit data to a reader. In comparison, passive tags draw power from the magnetic field generated between itself and a reader to power its microchip's circuits, allowing it to reflect the RF signal transmitted to it from a reader, adding information by modulating the reflected signal. Tags can also be either read-only, volatile read/write, or write one/read many.

In order for communication to occur between a tag and a reader, they must be tuned to the same frequency. RFID systems can be configured to operate in a variety of frequencies from low to ultra-high frequency (UHF) or even microwave. Being that RF propagation is different at different frequencies due to power and wave form properties, RFID system configuration must be considered in accordance with the applications that the system is designed to support. For example, low frequency tags are a good choice for applications in which the distance between tag and reader is small (typically less than a foot) as opposed to UHF, which supports applications at greater distances (up to about 20 feet).

Data gathered about the tagged RFID item/object may include its Electronic Product Code (EPC), Location, Physical parameters (temperature, pressure, humidity, etc.), Time Scanned, etc.

Fig.2.3 Photo of RFID Tags

2.6 RFID TAGS

Tag options include the following:

- Passive or active
- Read-only, Read-write, or write once
- Short range or long range

Each option has certain advantages and disadvantages. For example, active tags cost more and are larger, but are a better choice for use with high value goods and/or those that require continuous identification and location. Read-write tags, while expensive compared to read-only, are a good choice for monitoring for security, quality assurance, and/or theft deterrence.

Active tags may either provide active presence or active location information. This means that they can either provide general information about the presence of an object/item or more precise location information. Active location RFID systems support a higher effective read range with greater resolution capabilities, allowing for more precise tag location determination. Read-write tags have reduced range due to the increased signal overhead of the

full duplex communications, causing these systems to not perform location determination as well as read-only systems.

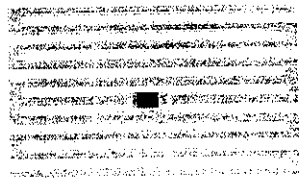


Fig.2.4 Internal View of RFID Tags

2.6.1 Tag Response

There is much debate on this particular topic. Keeping in mind that the tag response is a modification of the reflection of the signal it receives (backscatter); there is not much power available to communicate back to the reader. With respect to the signal emitted by the reader, the backscatter response is much closer to the noise floor than the peak reader emissions. Different methods of encoding data are used by a variety of manufacturers, but basically all can be discussed in two types – in-band, and out of band.

In-band responses offer a very discrete channel of operation, which seems on the surface a clean design. But as it turns out, in-band signaling for backscatter responses offers some large hurdles for reader designs that are not much of a problem for out of band designs. Out of band designs do have to take into account the effect of signals within the target backscatter receiver band, and also the interference of RFID systems into other systems operating in the chosen frequencies. It can easily be shown that RFID readers themselves emit a majority of the radiation that would interfere with their own receiver circuits. Thus placing signals to be received by an RFID reader outside the band in a

The tag cannot reflect 100% of the power received by the reader – backscatter is created by detuning the antenna and this in actuality can only achieve in the 10's of percentages of variance. The smaller the change the better, as tags require as much power absorbed as possible to maintain operational power.

Tags are most likely to be located away from the reader antenna by several meters. Reflections from the tag in the first few feet are the only considerably powered out of band signals that could be generated.

Passive tags are quite small circuits, without the ability to regulate power via resistance / heat dissipation design. Instead, the tags will detune the antenna so as not to absorb the excess power. This substantially inhibits the tag's ability to generate large variances of detuning and backscatter power under substantial power conditions (close to the reader).

Backscatter is not a generated precise tone; in real designs it is a sub-modulation of a reflected signal, and more closely resembles a square wave control signal than a pure tone sine wave. Energy is evenly divided into the higher and lower frequencies by nature. The square wave effect further spreads energy out into even higher offset frequencies, but at extremely low levels as opposed to this it confines a majority of energy into a particular frequency.

2.7 RFID VS OTHER TECHNIQUES (i.e. Bar coding)

While Universal Product Codes (UPC) used with bar coding systems have provided many benefits, EPC's used with RFID systems are poised to provide increased efficiency and productivity by way of automatic identification and tracking.

Unlike bar code systems, which use a reader and code labels that

an RF signal at an RFID reader. Information is transferred via an optical signal with bar codes as opposed to RF signals with RFID.

Bar codes and RFID tend to be used for different applications. The fact that RFID does not depend on line-of-sight, makes it particularly useful for applications, such as package management, in which the item must be handled many times. Being that standard bar codes typically only contain information about the manufacturer or originator of an item and basic information about the object itself, RFID is particularly useful for applications in which the item must be identified uniquely.

Since RFID uses radio waves rather than optics, RFID can penetrate non-metallic materials, allowing the RFID tag to be embedded or encased within an item or object. In contrast, the bar code must be physically exposed to the surface of the object, and in the case of bar code labels, can fall off the object.

Generally speaking, RFID is a better choice for situations in which there is a need for a lot of handling, such as in manufacturing and/or moving inventory situations, transferring units of blood, Medical Supplies etc

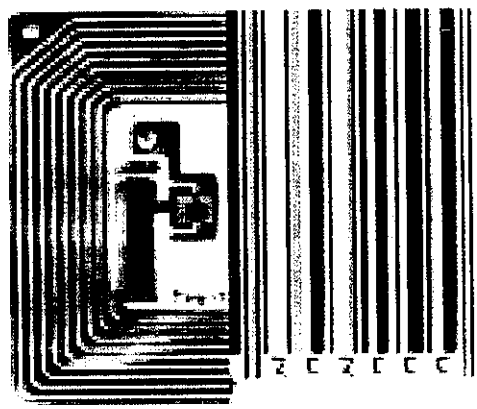


Fig.2.5 RFID Tags VS Barcodes

2.8 RFID APPLICATIONS

Applications enabled by RFID systems are limited only by the imagination, but generally fall into the following categories:

- Metering applications such as electronic toll collection
- Telemetry and sensor applications
- Inventory control and tracking such as merchandise control
- Asset tracking and recovery such as computing equipment monitoring
- Tracking parts moving through a manufacturing process
- Tracking goods in a supply chain
- Payment systems.

RFID systems can improve CRM systems through inventory control. In addition to the CRM benefit, this can provide a huge benefit in productivity, virtually eliminating the time and expense of employees locating merchandise.

Combining RFID systems with sensor applications enables solutions such as detecting when a uniquely identified object has come into contact with an environment that it should not, such as an area that is too hot, too dusty, to humid, etc. Sensor systems can also provide valuable CRM data via RFID communication such as detecting that car engine needs maintenance when a consumer brings a car in for an oil change.

RFID can be invaluable for applications in which uniquely identifying the item/object is critical due to concern over safety or quality

assurance such as management of hazardous materials or manufacturing situations in which quality control depends on precise parts control.

As RFID evolves to allow for standardization and personal RFID readers, various presence-based wireless marketing features will be enabled such as the ability to automatically inform a consumer when they are within the vicinity of a product type that they desire.

2.9. RFID PRIVACY, IMPLEMENTATION AND OPERATIONAL ISSUES

2.9.1 RFID Privacy Issues

Some consumer and privacy advocacy groups fear that RFID will take away personal privacy through exploiting the use of RFID to monitor peoples' movements and behaviors without their knowledge or consent, for example, by tracking them via RFID tags in their clothes.

While there may be some legitimate concern about RFID privacy, this type of issue is not well founded, as it would require satellite-based tracking, which while possible, is not practical for commercial consumer operations such as consumer market research.

2.9.2 Implementation and Operational Issues.

Since radio waves bounce off metal and are absorbed by water, RFID tags may not be embedded within metal objects or items with high water content. This can be overcome by using lower frequency tags, which have better penetration capabilities. However, low frequency tags also require a clearer signal path between the tag and the reader, but not as close as bar codes.

Readers are often designed to support time division multiplexing to prevent the signal from one reader interfering with the signal from another reader known as tag collision. Designing RFID systems to capture signals from individual tags in a serial fashion prevents reader collision.

2.10 LOW COST RFID

In the past few years, the term "low cost RFID" has begun to be used, and this may seem an artificial distinction at first sight. However, low cost RFID tags, typically taken as those costing less than one dollar each for up to 1 meter range and less than $5 above that, are different from conventional tags in several important respects. These differences mean that low cost RFID tags can be applied in very different, new applications and interest very different groups of suppliers and end users. This alternative to the barcode, magnetic stripe or printed label has advantages that include tolerance of mis-orientation and obscuration, lower cost over life and ability to "read". Most importantly, they are usually cheap enough to be disposable and thin enough to go in new locations, even inside sheets of paper in some cases, so all flat versions, including smart tickets and laminates, are usually called smart labels. Almost all conventional RFID devices contain a transistor circuit employing a microchip. By contrast, the potential in low cost RFID is split between chip-based technologies and "chipless" tags. Chip less tags can still be interrogated through a brick wall and hold data but most are cheaper and more primitive in electronic performance than chip tags.

CHAPTER 3

PIC MICROCONTROLLER

3.1 PERIPHERAL INTERFACE CONTROLLER (PIC16F873A)

A Single chip microcontroller is obtained by integrating all the components of a microcomputer in one IC package. Hence apart from CPU such a single chip microcomputer will therefore contain its own clock generator and some amount of ROM or EPROM, RAM and I/O ports on the same chip. It may also have other features like timer/counter, USART, PWM, A/D etc., on the chip.

3.2 SPECIAL FEATURES:

- 100,000 erase/write cycle Enhanced Flash program Memory typical
- 1,000,000 erase/write cycle Data EEPROM memory typical
- Data EEPROM Retention greater than 40 years
- Self-reprogrammable under software control
- In-Circuit Serial Programming (ICSP) via two pins
- Single-supply 5V In-Circuit Serial Programming
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving Sleep mode
- Selectable oscillator options
- I2C Protocol Compatible via two pins
- USART Compatibility

3.3 ARCHITECTURE OF THE PIC MICROCONTROLLER

Microcontroller is a tiny chip. It has inbuilt memory, timer, ports and other additional features. There are several companies manufacturing the micro controllers like Intel, Motorola and Microchip. PIC is the product of microchip. The following are the special characteristics of PIC. The architecture of PIC microcontroller (16F873A) is shown in the figure 3.1.

3.3.1. Features of the PIC

1. Long Word Instructions
2. Single Word Instructions
3. Instruction Pipeline
4. Single Cycle Instruction
5. Reduced Instruction Set
6. Register File Architecture
7. Orthogonal (Symmetric) Instructions
8. Instruction Flow/Pipelining

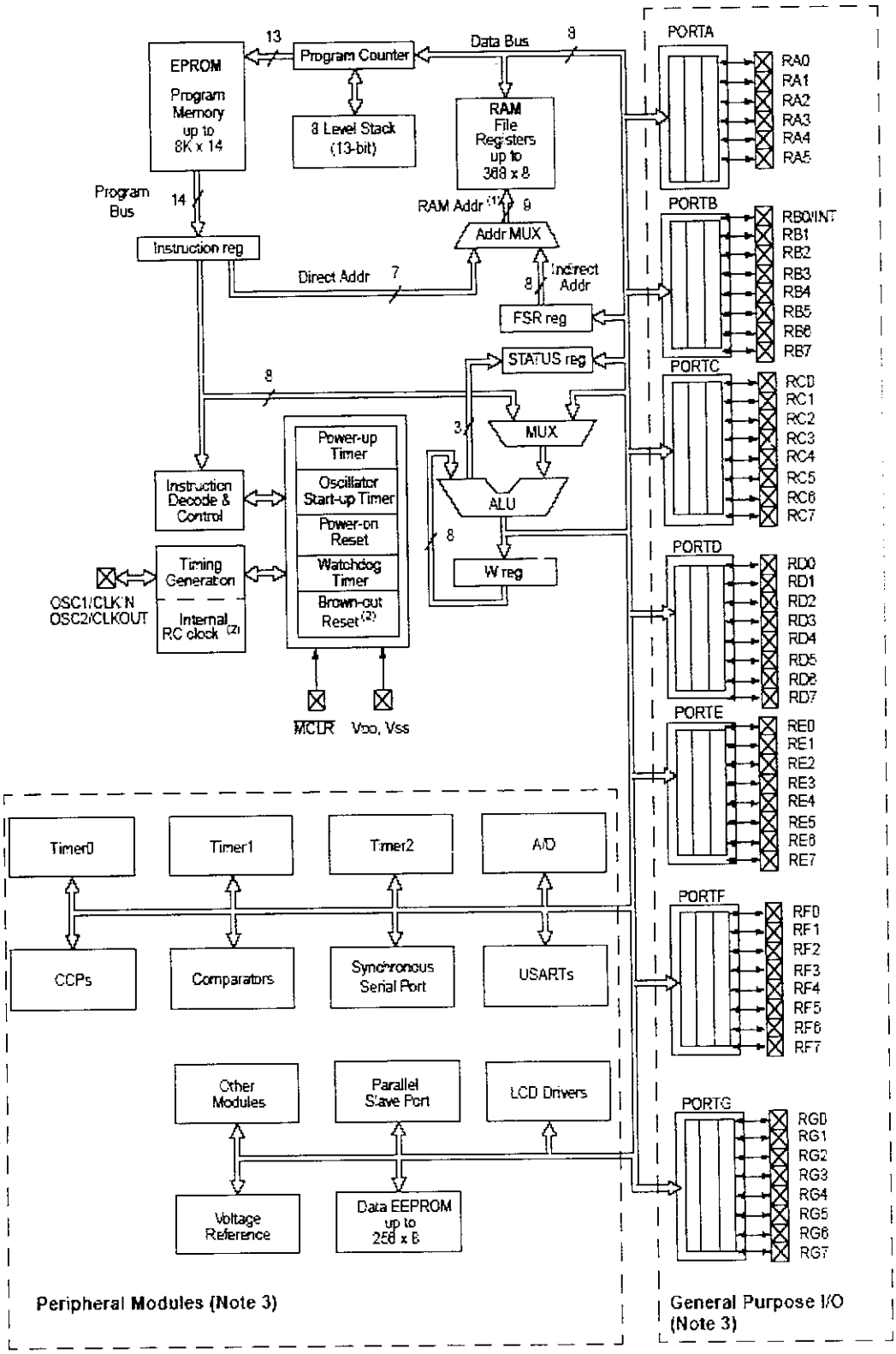


Fig 3.1 Architecture of PIC 16F873A

3.3.2 Arithmetic Logical Unit (ALU)

PIC Micro controllers contain an 8-bit ALU and an 8-bit working register. The ALU is a general-purpose arithmetic and logical unit. It performs arithmetic and Boolean functions between the data in the working register and any register file.

The ALU is 8-bits wide and is capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register ('W' register). The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the 'W' register or a file register. The 'W' register is an 8-bit working Register used for ALU operations. It is not an addressable register. Fig 3.2 shows the block diagram of ALU of PIC 16F876.

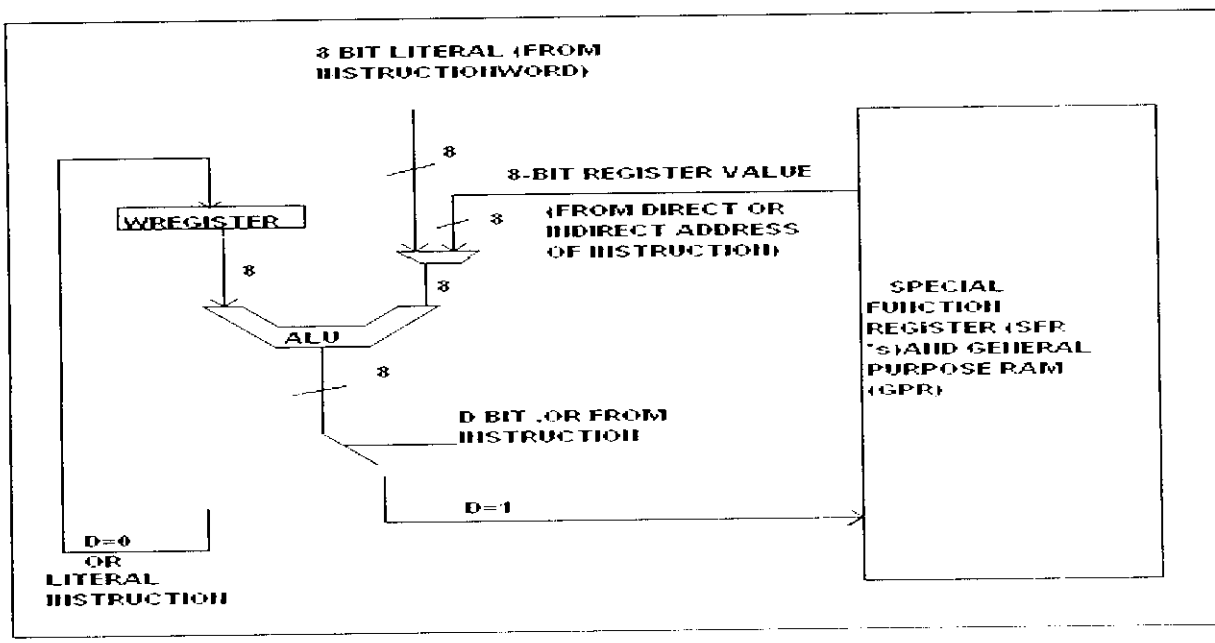


Fig. 3.2 Block diagram of ALU of PIC

3.3.3 Status Register

The STATUS register contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory. Since this register controls the selection of the Data Memory banks, it is required to be present in every bank. Also, this register is in the same relative position (offset) in each bank.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS registers, as destination may be different than intended. For example, CLRF STATUS will clear the upper-three bits and set the Z bit. This leaves the STATUS register as 000u uluu (where u=unchanged).

It is recommended therefore, that only BCF, BSF, SWAPF and MOVWF instructions be used to alter the STATUS register because these instructions do not affect the Z, C or DC bits from the STATUS register.

3.3.4 Oscillator

The internal oscillator circuit is used to generate the device clock. The device clock is required for the device to execute instructions and for the peripherals to function. Four clock periods generate one internal instruction clock (TCY) cycle. There are up to eight different modes, which the oscillator may have. There are two mode which allow the selection of the internal RC oscillator clock out (CLKOUT) to be driven on an I/O pin, or allow that I/O pin

and the operating mode is determined by the value written during device programming the RC oscillator option saves system cost while the LP crystal option saves power. Configuration bits are use to select the various option.

3.3.5 Port Control registers

3.3.5.1 PortA and TrisA Register

The RA4 pin is a Schmitt Trigger input and an open drain output. All other port pins have TTL input levels and full CMOS output drivers. All pins have data direction bits (TRIS registers), which can configure these pins as output or input. Setting a TRISA register bit puts the corresponding output driver in a hi-impedance mode. Clearing a bit in the TRISA register puts the contents of the output latch on the selected pin(s)

3.3.5.2 PortB and TrisB Register

PORTB is an 8-bit wide bi-directional port. The corresponding data direction register is TRISB. Setting a bit in the TRISB register puts the corresponding output driver in a high-impedance input mode. Clearing a bit in the TRISB register puts the contents of the output latch on the selected pin(s).

3.3.5.3 PortC and TrisC Register

PORTC is an 8-bit bi-directional port. Each pin is individually configurable as an input or output through the TRISC register. PORTC pins have Schmitt Trigger input buffers. When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override.

CHAPTER 4

DISPLAY CIRCUIT

4.1. SEVEN SEGMENT DISPLAY

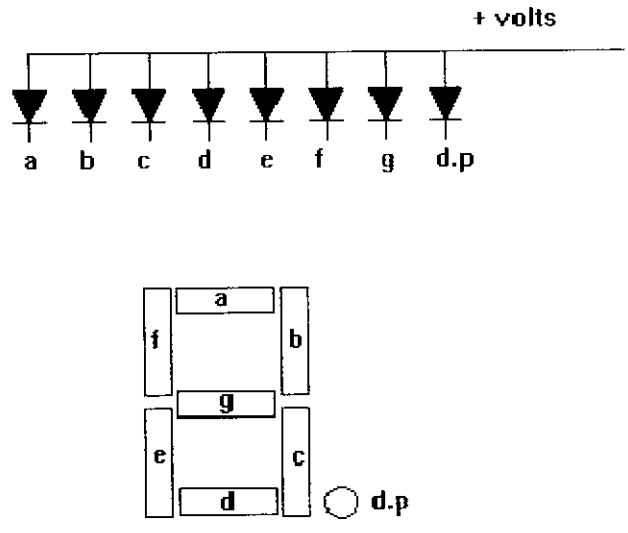


Fig.4.1 Seven Segment Display

The 7 segment display is used as a numerical indicator on many types of test equipment. It is an assembly of light emitting diodes which can be powered individually. They most commonly emit red light. They are arranged and labeled as shown in the diagram. Powering all the segments will display the number 8. Powering a, b, c, d and g will display the number 3. Numbers 0 to 9 can be displayed. The d.p represents a decimal point. The one shown is a common anode display since all anodes are joined together and go to the positive supply.

The cathodes are connected individually to zero volts. Resistors must be placed in series with each diode to limit the current through each diode to a safe value. Early wrist watches used this type of display but they used so much current that

Common cathode displays where all the cathodes are joined are also available. Liquid crystal displays do a similar job and consume much less power. Alphanumeric displays are available which can show letters as well as numbers.

CHAPTER 5

SERIAL PORT MODULE

5.1 SERIAL PORT STANDARDS

PC communication is established using RS232 protocol. RS232 is a serial protocol mainly used for PC communication. The maximum distance it can run is 15 meters.

5.1.1 RS 232 Connector Pin Assignment

RS 232 connector was originally developed to use 25 pins. In this, pin-out provisions were made for a secondary RS232 communication channel. Now a days, the smaller 9-pin version is most commonly used which is shown in the fig5.1 and fig5.2.

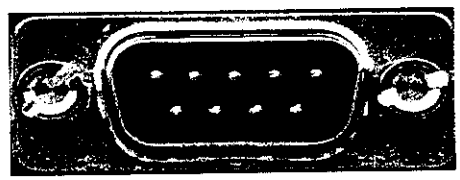
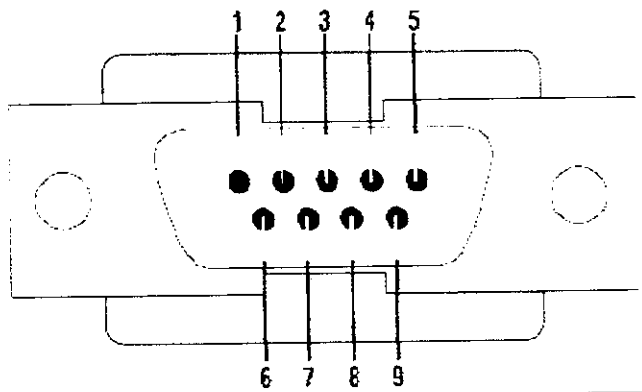


Fig 5.1 RS-232 Pin out on a DB-9 pin Used for asynchronous Data



Pin	Signal	Pin	Signal
1	Data Carrier Detect	6	Data Set Ready
2	Received Data	7	Request to Send
3	Transmitted Data	8	Clear to Send
4	Data Terminal Ready	9	Ring Indicator
5	Signal Ground		

Electronic data communications between elements will generally fall into two broad categories, single-ended and differential. RS232 (single-ended) was introduced in 1962, and despite rumors for its early demise, has remained widely used through the industry. Independent channels are established for two-way (full-duplex) communications. The RS232 signals are represented by voltage levels with respect to a system common (power / logic ground). The "idle" state (MARK) has the signal level negative with respect to common, and the "active" state (SPACE) has the signal level positive with respect to common. RS232 has numerous handshaking lines (primarily used with modems), and also specifies a communications protocol. The RS-232 interface presupposes a common ground between the DTE and DCE. This is a reasonable assumption when a short cable connects the DTE to the DCE, but with longer lines and connections between devices that may be on different electrical busses with different grounds, this may not be true.

RS232 data is bi-polar.... +3 TO +12 volts indicate an "ON or 0-state (SPACE) condition" while A -3 to -12 volts indicates an "OFF" 1-state (MARK) condition.... Modern computer equipment ignores the negative level and accepts a zero voltage level as the "OFF" state. In fact, the "ON" state may be achieved with lesser positive potential. This means circuits powered by 5 VDC are capable of driving RS232 circuits directly; however, the overall range that the RS232 signal may be transmitted/received may be dramatically reduced. The output signal level usually swings between +12V and -12V. The "dead area" between +3v and -3v is designed to absorb line noise. In the various RS-232-like definitions this dead area may vary. For instance, the definition for V.10 has a dead area from +0.3v to -0.3v. Many receivers designed for RS-232 are sensitive to differentials of 1v or less. This can cause problems when using pin-powered widgets - line drivers, converters, modems etc. These types of

(the RS-232 I/O chip) allows up to 50ma per output pin - so if the device needs 70ma to run we would need to use at least 2 pins for power. Some devices are very efficient and only require one pin (some times the Transmit or DTR pin) to be high - in the "SPACE" state while idle.

An RS-232 port can supply only limited power to another device. The number of output lines, the type of interface driver IC, and the state of the output lines are important considerations. Data is transmitted and received on pins 2 and 3 respectively.

5.2 IC MAX 232

This IC is popularly known as a voltage shifter. It's a 16- pin IC used for the PC to microcontroller communication. This IC is connected between router and PC. Pin diagram of MAX 232 is shown in fig 5.3.

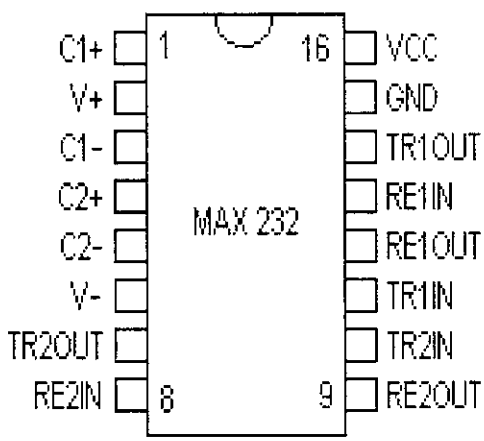


Fig 5.3 Pin diagram of MAX 232

The voltage level of microcontroller is 0 TO 5 Volts. In order to make communication between PC and microcontroller voltage conversion is essential. MAX 232 achieves this voltage conversion. This internally consists of diodes, logic gates, and capacitors. MAX 232 modifies the voltage level with

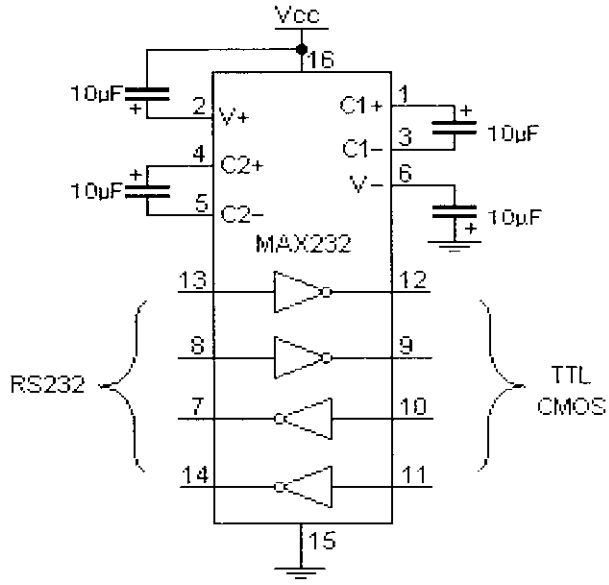


Fig 5.4 Logic diagram of MAX 232

CHAPTER 6

USART PROTOCOL

6.1 USART

USART is the abbreviation for Universal synchronous asynchronous receiver transmitter. It is a serial protocol, which makes the communication between PC–to-router and router-to-RTUs. Fundamentally, protocol is nothing but a rules and regulations derived for the communication.

6.2 BLOCK DIAGRAM OF USART TRANSMITTER

The Block diagram of USART transmitter is shown in Fig. 6.1

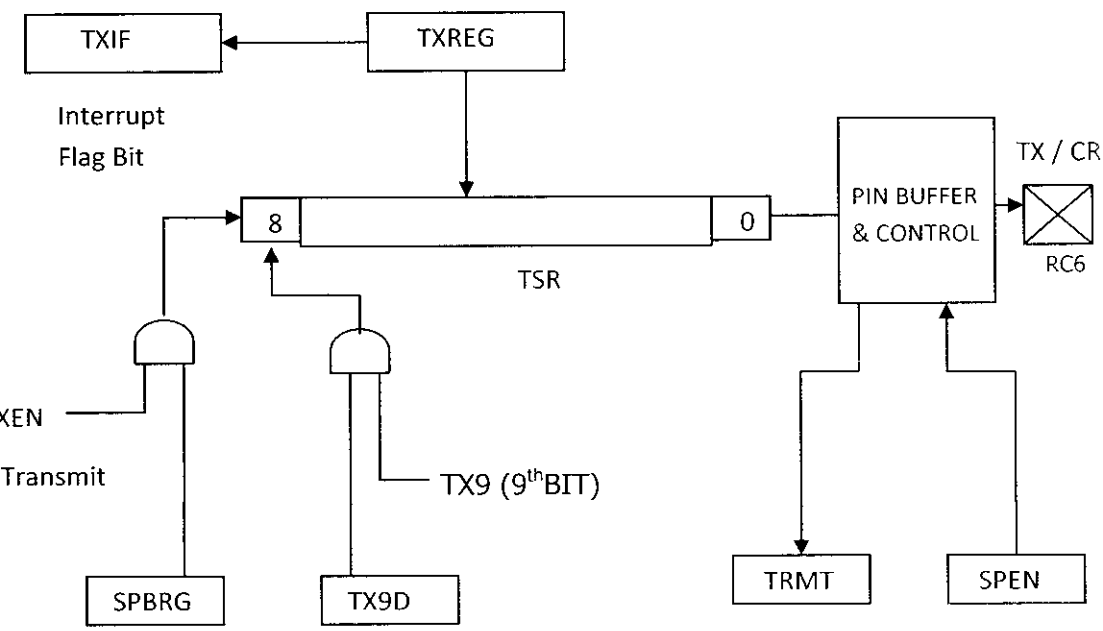


Fig 6.1 Block diagram of USART Transmitter

6.3 PROCEDURE FOR USART TRANSMISSION

1. The seventh pin (RC6) of the PortC is dedicated for USART transmission. So, it is assigned as input by setting seventh pin of TrisC
2. Baud rate for communication is set by SPBRG register. For that decimal value of twenty-five is move on to SPBRG.
3. Bit SPEN is set to one (This is available in RCSTA) to enable serial data communication.
4. Sending data 0x20 configures transmission control register TXSTA.
5. In this register only TXEN pin is set to one to initiate transmission.
6. Required data is moved to the TXREG.
7. Finally TRMT pin is checked to know the transmission is completed or not

6.4 BLOCK DIAGRAM OF USART RECEIVER

The block diagram of USART receiver is shown in fig 6.2

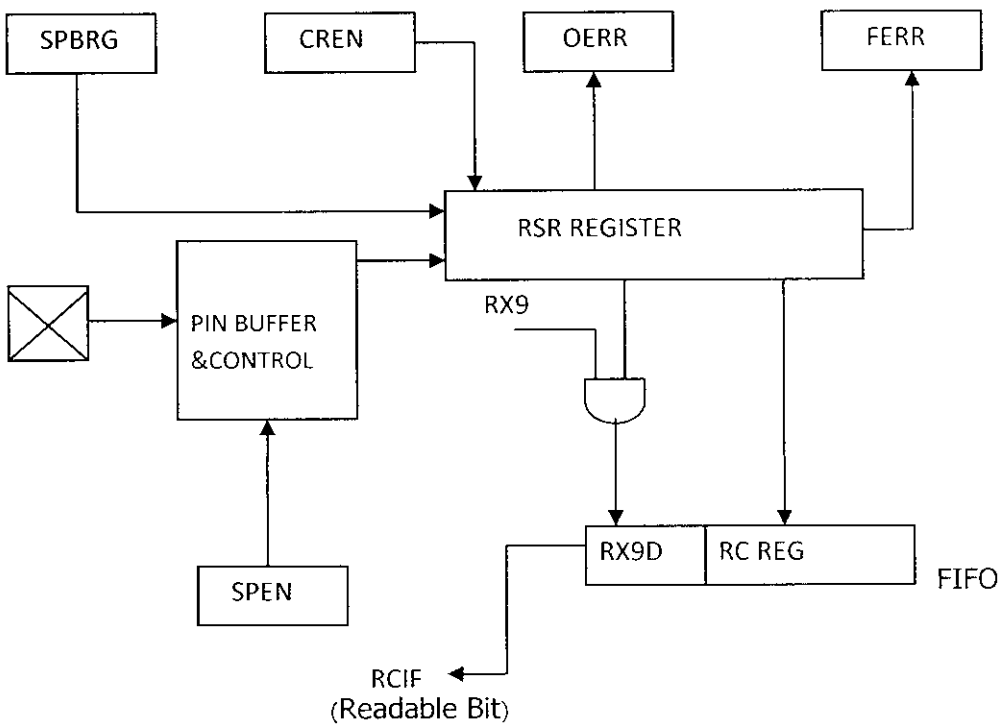


Fig 6.2 Block diagram of USART Receiver

6.5. PROCEDURE FOR USART RECEPTION

1. The eighth pin (RC7) of the Port C is dedicated for USART reception. So, it is assigned as input by setting seventh pin of TrisC.
2. Baud rate for communication is set by SPBRG register. For that decimal value of twenty-five is move on to SPBRG.
3. Bit SPEN is set to one (This is available in RCSTA) to enable serial data communication.
4. The bit CREN (Continues receive enable bit) is set to one to enable continues data reception.
5. Poll the RCIF flag (flag in the PIR 1 register) to check either the reception is completed or not.

CHAPTER 7
I2C PROTOCOL

7.1. I2C

I²C is a multi-master serial computer bus invented by Philips that is used to attach low-speed peripherals to a motherboard, embedded system, or cell phone. The name stands for Inter-Integrated Circuit and is pronounced *I-squared-C* and also, incorrectly, *I-two-C*.

I²C uses only two bidirectional open-drain lines, Serial Data (SDA) and Serial Clock (SCL), pulled up with resistors. Typical voltages used are +5 V or +3.3 V although systems with other, higher or lower, voltages are permitted.

The I²C reference design has a 7-bit address space with 16 reserved addresses, so a maximum of 112 nodes can communicate on the same bus. The most common I²C bus modes are the 100 Kbit/s *standard mode* and the 10 kbit/s *low-speed mode*, but clock frequencies down to DC are also allowed. Recent revisions of I²C can host more nodes and run faster (400 kbit/s *Fast mode*, 1 Mbit/s *Fast mode plus* or Fm+, and 3.4 Mbit/s *High Speed mode*), and also support other extended features, such as 10-bit addressing. The maximum number of nodes is obviously limited by the address space, and also by the total bus capacitance of 400 pF.

The I2C is a bus with a clock (SCL) and data (SDA) lines with 7-bit addressing. The bus has two roles for nodes: master and slave:

- Master node — node that issues the clock and addresses slaves
- Slave node — node that receives the clock line and address.

The bus is a multi-master bus which means any number of master nodes

messages (after a STOP is sent).There is four potential modes of operation for a given bus device, although most devices only use a single role and its two modes:

- master transmit — master node is sending data to a slave
- master receive — master node is receiving data from a slave
- slave transmit — slave node is sending data to a master
- slave receive — slave node is receiving data from the master

The master is initially in master transmit mode by sending a start bit followed by the 7-bit address of the slave it wishes to communicate with, which is finally followed by a single bit representing whether it wishes to write(0) to or read(1) from the slave. If the slave exists on the bus then it will respond with an ACK bit (acknowledge) for that address. The master then continues in either transmit or receive mode (according to the read/write bit it sent), and the slave continues in its complementary mode (receive or transmit, respectively).

The address and the data bytes are sent most significant bit first. The start bit is indicated by a high->low transition of SDA with SCL high; the stop bit is indicated by a low->high transition of SDA with SCL high.If the master wishes to write to the slave then it repeatedly sends a byte with the slave sending an ACK bit. (In this situation, the master is in master transmit mode and the slave is in slave receive mode.)If the master wishes to read from the slave then it repeatedly receives a byte from the slave, the master sending an ACK bit after every byte but the last one. (In this situation, the master is in master receive mode and the slave is in slave transmit mode.) The master then ends transmission with a stop bit, or it may send another START bit if it wishes to retain control of the bus for another transfer (a "combined message").

7.2 MESSAGE PROTOCOLS

I²C defines three basic types of message, each of which begins with a START and ends with a STOP:

- Single message where a master writes data to a slave;
- Single message where a master reads data from a slave;
- "Combined" messages, where a master issues at least two reads and/or writes to one or more slaves.

In a combined message, each read or write begins with a START and the slave address. After the first START, these are also called "repeated START" bits.

Any given slave will only respond to particular messages, as defined by its product documentation. Pure I²C systems support arbitrary message structures. In practice most slaves adopt request/response control models, where one or more bytes following a write command are treated as a command or address. Those bytes determine how subsequent written bytes are treated and/or how the slave responds on subsequent reads.

7.3 PHYSICAL LAYER

At the physical layer, both SCL & SDA lines are of open-drain design, thus, pull-up resistors are needed. Pulling the line to ground is considered a logical zero while letting the line float is a logical one. This is used as a channel access method. High speed systems (and some others) also add a current source pull up, at least on SCL; this supports faster rise times and higher bus capacitance. Transitions for data bits are always performed while the clock is low; transitions while it is high indicate start and stop bits.

When one node is transmitting a logical one (i.e., letting the line float to

because the line is not in a logical one state — it is not pulled up to Vdd. On SDA, this can be used for arbitration for I²C since it is a multi-master bus; when the data that's read back isn't what was written, one master drops out in favor of another master. Slaves may also use this on SCL to stretch the clock from the master. A master may also hold SCL low for longer than needed, if it needs to slow the data rate for any reason.

7.4 CLOCK STRETCHING

One of the more interesting features of the I²C protocol is clock stretching. An addressed slave device may hold the clock line low after receiving (or sending) a bit, indicating that it is not yet ready to process more data. The master that is communicating with the slave will attempt to raise the clock to transfer the next bit, but must verify that the clock line was actually raised. If the slave is clock stretching, the clock line will still be low (because the connections are open-drain).

Clock stretching allows receivers that cannot keep up with a transmitter to control the flow of incoming data. Some masters, such as those found inside custom ASICs may not support clock stretching; often these devices will be labeled as a "two-wire interface" and not strict I²C.

7.5 ARBITRATION

Every master monitors the bus for a start bit, and does not start a transmission while the bus is busy. However, two masters may start transmission at about the same time; in this case, arbitration occurs. In contrast to protocols (such as Ethernet) that use random back-off delays before issuing a retry, I²C has a deterministic arbitration policy. During transmission, each master checks the level of the lines and compares them with the levels it is

another master sets it to 0 (pull to ground), the result is that the line is low. The first master then observes that the level of the line is different than expected, and concludes that another master is transmitting. The first master to notice such a difference is the one that loses arbitration: it stops and waits for the bus to be free again. In the meantime, the other master has not noticed any difference between the expected and actual levels on the lines, and therefore continues transmission. It can do so without problems because so far the levels of the lines have been exactly as it expected, which means that the other master has not disturbed its transmission. If the two masters are sending a message to two different slaves, the one sending the lower slave address always "wins" arbitration in the address stage. Since the two masters may send messages to the same slave, arbitration must continue into the data stages. Arbitration occurs very rarely, but is necessary for proper multi-master support. As with clock-stretching, not all devices support arbitration. Those that do generally label themselves as supporting "multi-master" communication.

7.6 TIMING DIAGRAM

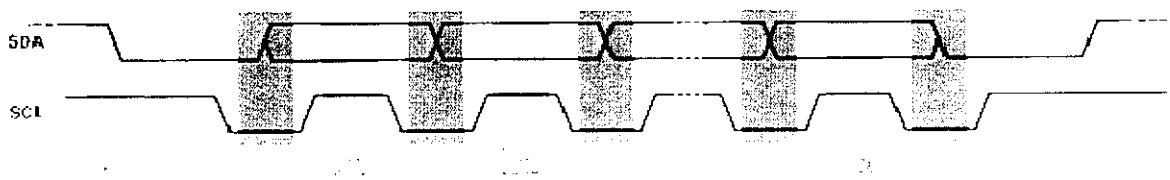


Fig 7.1 Timing Diagram of I2C Protocol

Data transfer is initiated with the START bit (**S**) when SDA is pulled low while SCL stays high. Then, SDA sets the transferred bit while SCL is low (blue) and the data is sampled (received) when SCL rises (green). When the transfer is complete, a STOP bit (**P**) is sent by releasing the data line to allow it

CHAPTER 8

GSM MODEM

8.1 INTRODUCTION

The global system for mobile(GSM) is an ETSI standard for 2G pan European digital cellular with international roaming.GSM is an integrated voice service and provides a number of services beyond cellular telephone. The GSM system is organized in three major segments they are

- Mobile Station (MS)
- Base Station Sub System(BSS)
- Network And Switching Subsystem(NSS)

8.2 MOBILE STATION

The MS communicates the information with the user and modifies it with the transmission protocols of the air interface to communicate with the BSS. The MS has two elements the first element is the mobile equipment which contains all the components needed for the implementation of the protocols including the radio modem. The second element of the MS in the GSM is the Subscriber Identity Module (SIM) i.e. a smart card issued at the subscription time identifying the speci9fications of the user such as address and type of services. The calls in GSM are directed to the SIM

8.3 BASE STATION SUBSYSTEM

The base station communicates with the user through the wireless air interface and with the wired infrastructure through the wired protocols. There

communication over the air interfaces and is physically located in the center of the cell where the BSS antenna is installed. The second architectural element of the BSS is the BSC that is a small switch inside the BSS in charge of frequency administration and hand over among the BTS. For a single BTS sight BSC is located in the antenna, for multiple BTS systems BSC is in a switching center along with the NSS hardware.

8.4 NETWORK AND SWITCHING SUBSYSTEMS

The NSS is responsible for the network operation. The NSS is a wireless specific switch that communicates with other switches in the PSTN and at the same time supports functionalities that are needed for a cellular mobile environment. The NSS interconnects to the PSTN through the ISDN protocols .it has one hardware MSC and four software elements such as

- Visitor Location Register(VLR)
- Home Location Register (HLR)
- Equipment Identification Register(EIR)
- Authentication Center(AUC)

MSC provides to the network the specific information on the status of mobile terminals. HLR is database software that handles management of mobile subscriber account.VLR is temporary database software identify only the subscribers visiting inside the coverage areas of the MSC. The AUC hold different algorithms that are used for authentication and encryption of a subscriber. The EIR is another database managing the identification of the mobile equipment against thefts and faults.

CHAPTER 9

POWER SUPPLY

9.1 INTRODUCTION

Since all electronic circuits work only with low DC voltage, a power supply unit is needed to provide the appropriate voltage supply. This unit consists of transformer, rectifier, filter and regulator. AC voltage typically 230V is connected to a step down transformer. The output of transformer is given to the bridge rectifier and then a simple capacitor filter to produce a DC voltage initially filters it. This DC voltage is given to regulator, which gives a constant DC voltage. The Power supply unit and the Circuit diagram of Blood bank Automation System is shown in Figure 9.1 and Figure 9.2 respectively.

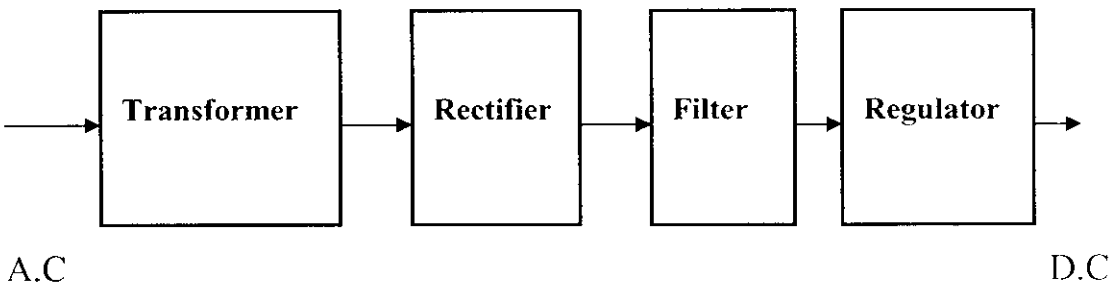
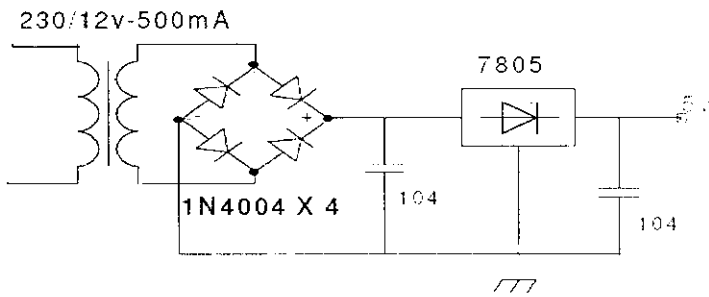


Fig. 9.1 Power supply unit



9.2 TRANSFORMER

A transformer is a static piece of which electric power in one circuit is transformed into electric power of same frequency in another circuit. It can raise or lower the voltage in a circuit but with corresponding decrease or increase in current. Step down transformer have been used for providing a necessary supply for the electronic circuits. In this project 230/12V transformer is used.

9.3 RECTIFIER

The DC level obtained from a sinusoidal input can be improved 100% using a process called full wave rectification. It uses four diodes in a bridge configuration. From the bridge configuration two diodes (D2 & D3) are conducting when the other two diodes (D1 & D4) are in off state. Accordingly for the negative of the input the conducting diodes are D1 & D4. Thus the polarity across the load is the same.

9.4 FILTER

The filter circuit used here is capacitive filter circuit. This is connected at the rectifier output and the DC is obtained across it. The filtered waveform is essentially a DC voltage with negligible ripples.

9.5 REGULATOR

Regulator IC units contain the circuitry for reference source, comparator amplifier, control device and over load protection in a single IC. Although the internal construction of the IC is somewhat different from that described for discrete voltage regulator circuits, the external operation is the same. IC units provide regulation of either a fixed positive voltage, a fixed negative voltage, are an adjustably set voltage.

A power supply can be built using a transformer connected to the AC supply line to step the AC voltage to the desired amplitude. It is then rectified, filtered with the capacitor and finally regulating the dc voltage using an IC regulator. The regulators can be selected for operation with load currents from hundreds of milliamperes to tens of amperes, corresponding to power ratings from milliwatts to tens of watts.

CHAPTER 10

SOFTWARE DEVELOPMENT TOOLS USED FOR PROGRAMMING

10.1 SOFTWARE TOOLS

1. MPLAB - IDE (Integrated Development Environment).
2. HITECH-C - Cross compiler.
3. PROPIC - PIC Programmer.
4. PROTEL - PCB Designing software

10.2 MPLAB

To make working with the PIC microcontroller even easier, Microchip provides an excellent group of software it is called MPLAB IDE. MPLAB IDE is a software program that runs on a PC to develop applications for Microchip microcontrollers. It is called an Integrated Development Environment, or IDE, because it provides a single integrated "environment" to develop code for embedded microcontrollers. MPLAB IDE contains a text editor, assembler (MPASM assembler) and simulator (MPSIM) and this stuff will run under DOS or WINDOWS. With MPLAB IDE in hand we can write the program using the included text editor, and then assemble it with the MPASM assembler program. The MPASM assembler will develop the code format (HEX) that the PIC Microcontroller wants that code can then be burned into a PIC with the programmer.

10.2.1 Sample Program

This program is used for initializing the first microcontroller and loads the values A-2, B-3, C-4 initially

```
init()
{
```

```
TRISA=0x07;
TRISC=0XD8;
PORTA=0;
PORTB=0;
PORTC=0;
SSPBUF=0;
SSPCON=0X28;
SSPCON2=0;
SSPSTAT=0X80;
SSPADD=100;
ADCON1=0X07;
OPTION=0x05;
TMR0=100;
T0IE=1;
PR2=250;
T2CON=0X25;
TMR2IE=1;
INTCON=0XC0;
RCSTA=0;
TXSTA=0;
SPEN=1;
BRGH=1;
SPBRG=25;
RCIE=1;
CREN=1;
Agroup=2;
Bgroup=3;
Ogroup=4;
```

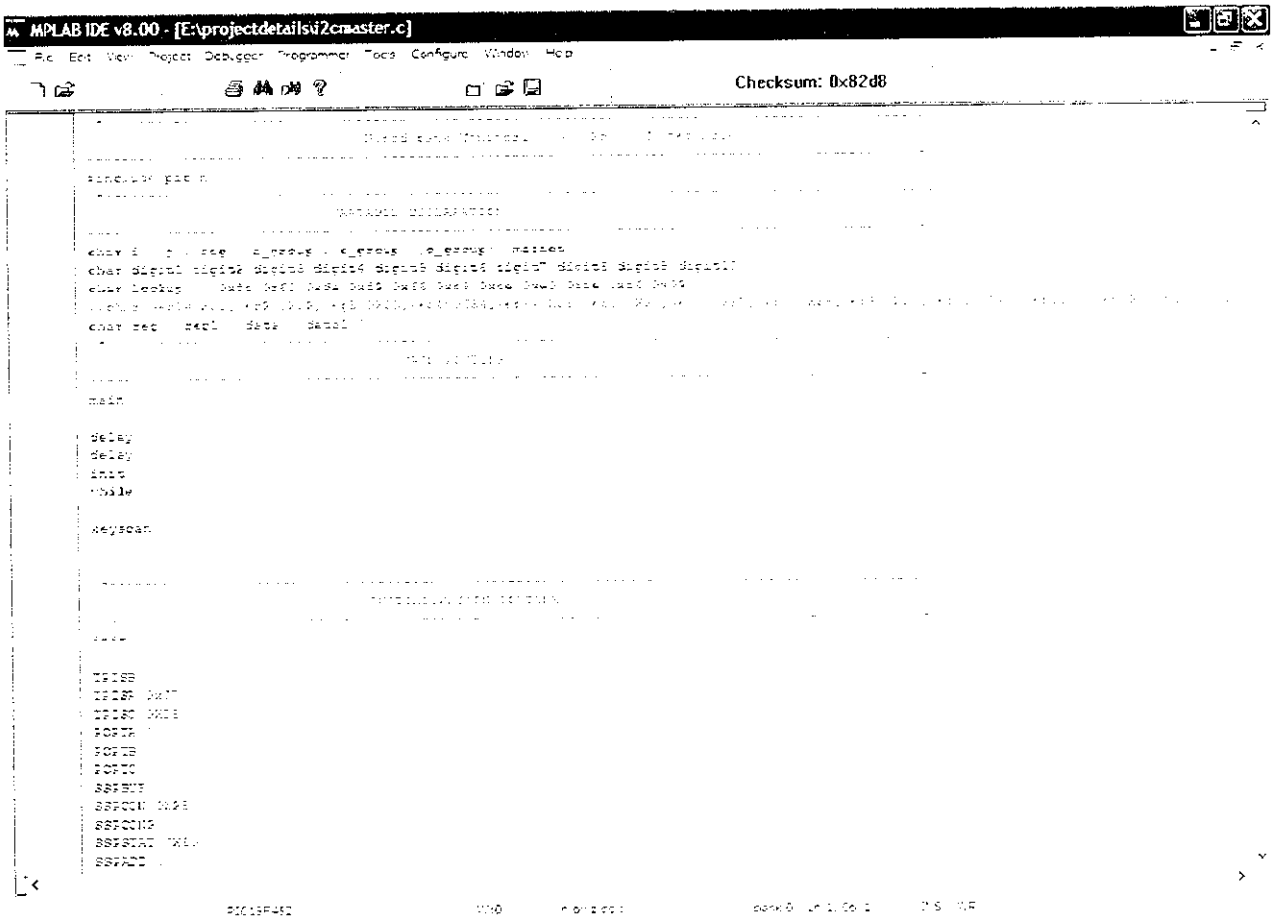
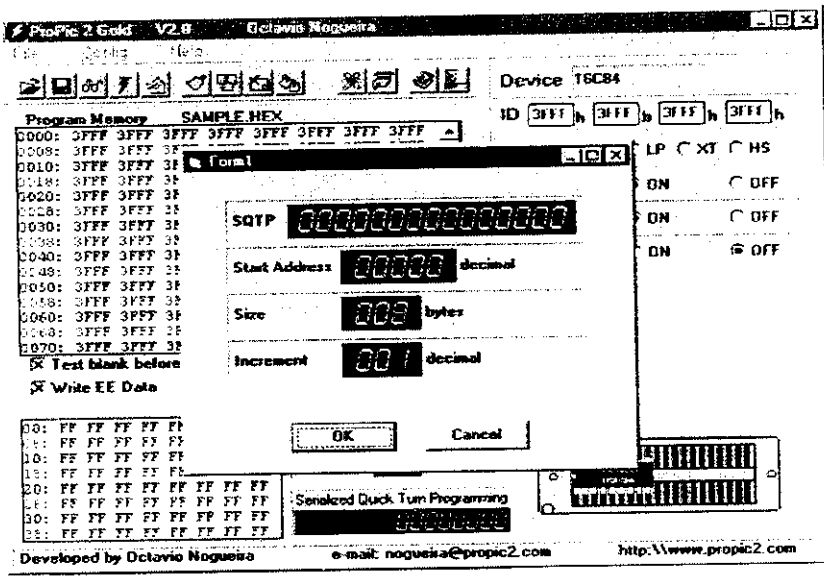


Fig 10.1 Screenshot of MPLAB Software

10.3 PROPIC

PROPIC software helps to burn the PIC. The program is converted into HEX code and it is loaded in the software. The oscillator type is also mentioned in the software (i.e.) XT, AT, etc. The power up timer (PWRTE) is switched on. The PIC is placed in the programming kit and the PIC is burned with the program. It gives security for the code which we have burned by selecting the code protection option.



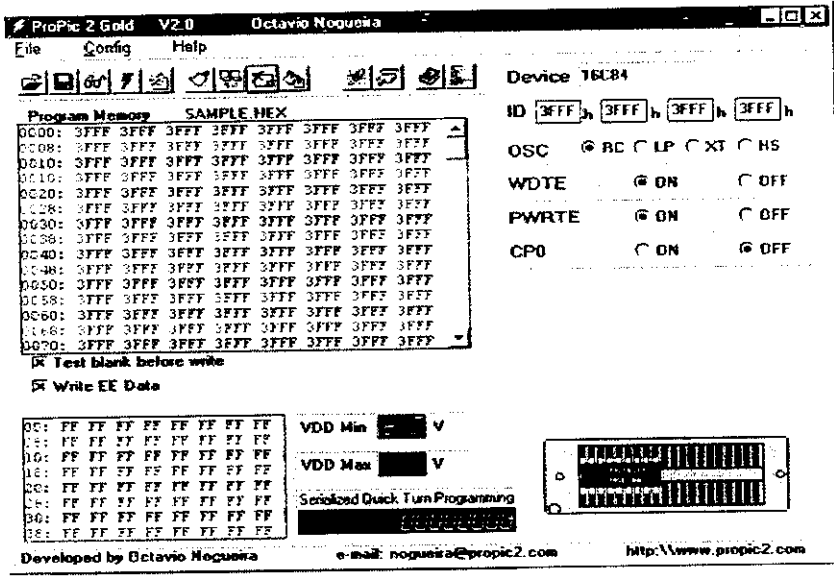


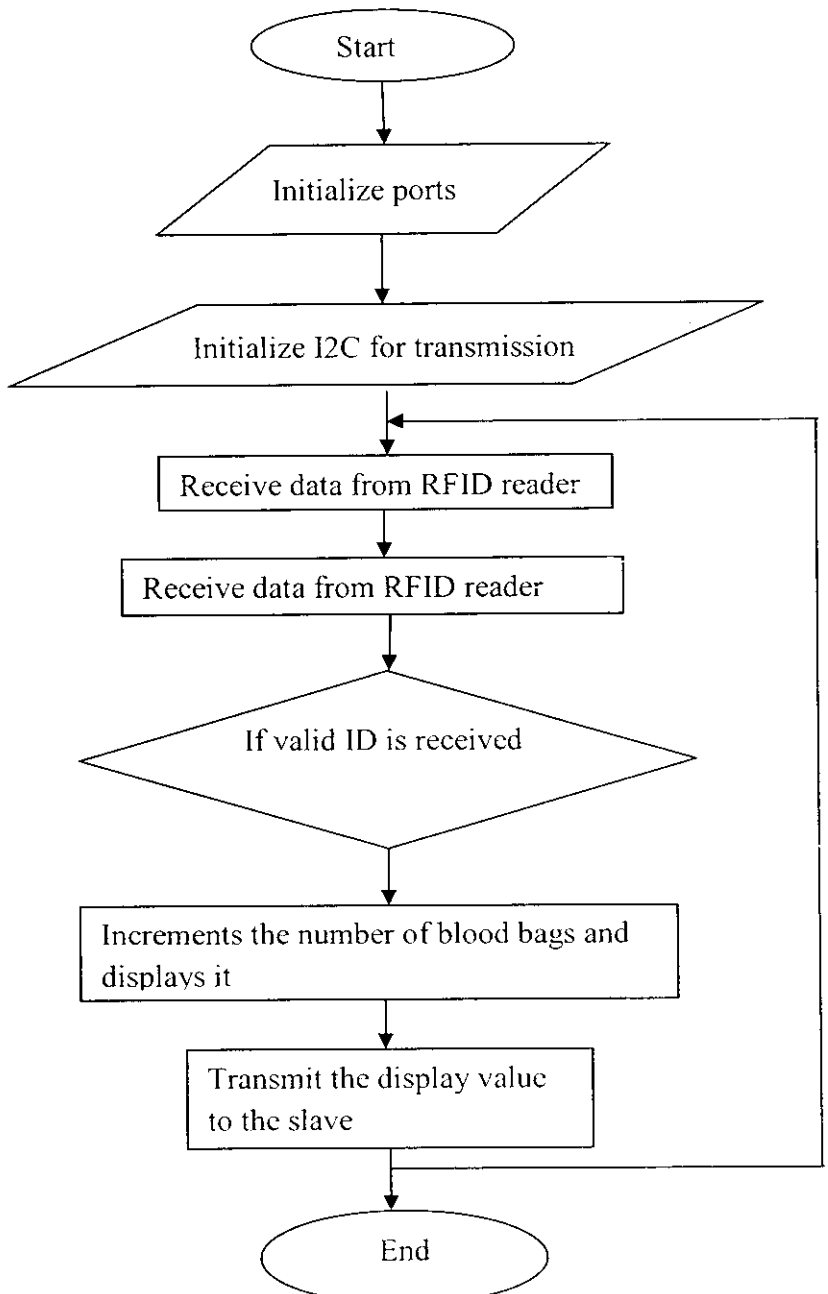
Fig 10.2 Screenshot of PROPIC Software

CHAPTER 11

FLOWCHART

11. 1 FLOWCHART OF OPERATION OF RFID BASED BLOOD BANK SYSTEM

The flowchart of operation of RFID based blood bank system is shown in the figure 11.1 and 11.2 respectivley



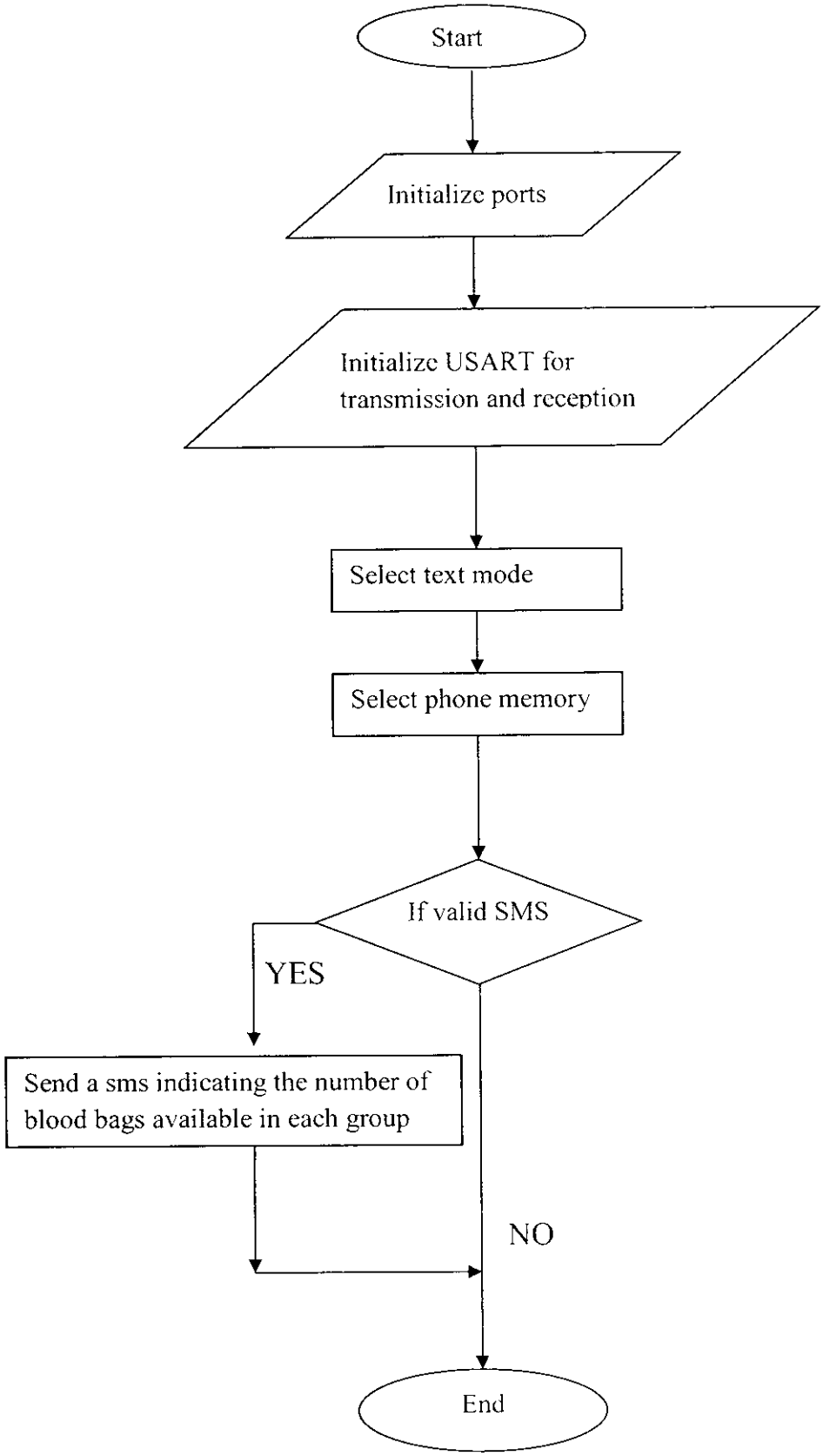


Fig 11.2 Slave Flowchart

CONCLUSION

Thus if the concept of automated blood bank system is implemented, it is clear that the present difficulties in the blood bank system can be avoided. This Automated system brings out the maximum functionality appropriately as well as reduces the cost factor, so that this application can be implemented at any level. Some of the important advantages that can be obtained by implementing this system are listed below.

- Man power Error is reduced due to automation.
- Cost centralization can be subjected effectively.
- Availability of the blood group can be known from the remote area.
- Total capital investment of the project can be reduced.
- 24hrs service can be provided at any cause without extra remuneration.

FUTURE EXPANSION

Future plans include automation of the blood banks on a state level, and then on a national scale, finally connecting all the blood banks in the nation through a synchronous network. We also have an idea to extend this automation system to the organ donor system, to provide continuous updates to various hospitals linked to the network about the availability of vital organs like heart, brain, eyes, liver including various details like blood group for transplant purposes.

APPENDIX A

PIC 16F873A

MICROCHIP

PIC16F87XA

28/40/44-Pin Enhanced Flash Microcontrollers

Devices Included in this Data Sheet:

- PIC16F873A
- PIC16F874A
- PIC16F876A
- PIC16F877A

High-Performance RISC CPU:

- Only 35 single-word instructions to learn
- All single-cycle instructions except for program branches, which are two-cycle
- Operating speed: DC – 20 MHz clock input
  DC – 200 ns instruction cycle
- Up to 8K x 14 words of Flash Program Memory, Up to 368 x 8 bytes of Data Memory (RAM), Up to 256 x 8 bytes of EEPROM Data Memory
- Pinout compatible to other 28-pin or 40/44-pin PIC16CXXX and PIC16FXXX microcontrollers

Peripheral Features:

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler, can be incremented during Sleep via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules
  - Capture is 16-bit, max. resolution is 12.5 ns
  - Compare is 16-bit, max. resolution is 200 ns
  - PWM max. resolution is 10-bit
- Synchronous Serial Port (SSP) with SPI™ (Master mode) and I^2C™ (Master/Slave)
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with 9-bit address detection
- Parallel Slave Port (PSP) – 8 bits wide with external $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ controls (40/44-pin only)
- Brown-out detection circuitry for Brown-out Reset (BOR)

Analog Features:

- 10-bit, up to 8-channel Analog-to-Digital Converter (A/D)
- Brown-out Reset (BOR)
- Analog Comparator module with:
  - Two analog comparators
  - Programmable on-chip voltage reference (V_{REF}) module
  - Programmable input multiplexing from device inputs and internal voltage reference
  - Comparator outputs are externally accessible

Special Microcontroller Features:

- 100,000 erase/write cycle Enhanced Flash program memory typical
- 1,000,000 erase/write cycle Data EEPROM memory typical
- Data EEPROM Retention > 40 years
- Self-reprogrammable under software control
- In-Circuit Serial Programming™ (ICSP™) via two pins
- Single-supply 5V In-Circuit Serial Programming
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving Sleep mode
- Selectable oscillator options
- In-Circuit Debug (ICD) via two pins

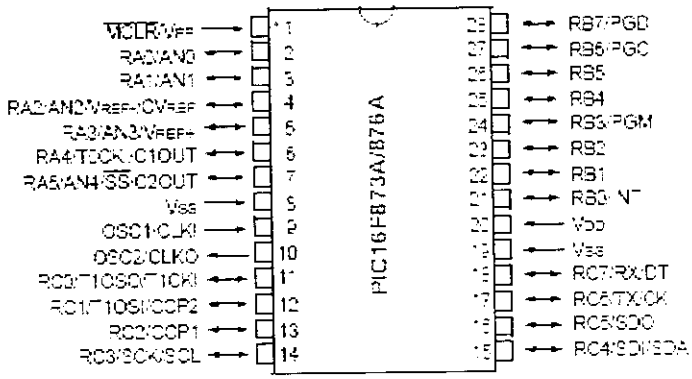
CMOS Technology:

- Low-power, high-speed Flash/EEPROM technology
- Fully static design
- Wide operating voltage range (2.0V to 5.5V)
- Commercial and Industrial temperature ranges
- Low-power consumption

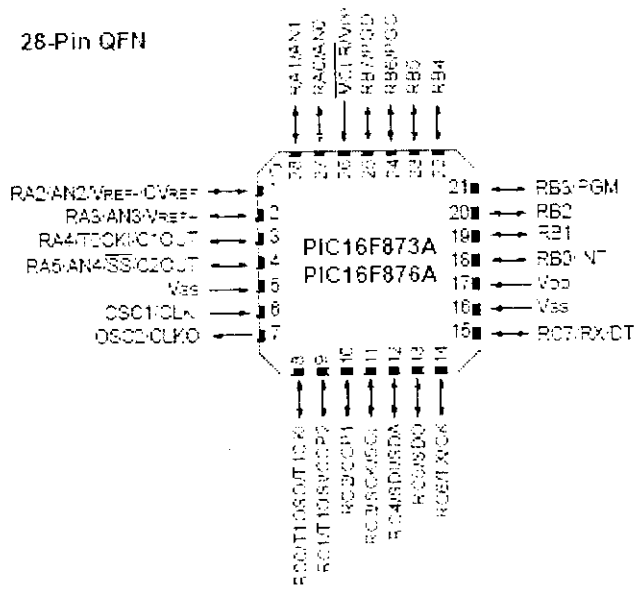
Device	Program Memory		Data SRAM (Bytes)	EEPROM (Bytes)	I/O	10-bit A/D (ch)	CCP (PWM)	MSSP		USART	Timers 8/16-bit	Comparators
	Bytes	# Single Word Instructions						SPI	Master I^2C			
PIC16F873A	7.2K	4096	192	128	22	5	2	Yes	Yes	Yes	2/1	2
PIC16F874A	7.2K	4096	192	128	33	8	2	Yes	Yes	Yes	2/1	2
PIC16F876A	14.3K	8192	368	256	22	5	2	Yes	Yes	Yes	2/1	2
PIC16F877A	14.3K	8192	368	256	33	8	2	Yes	Yes	Yes	2/1	2

Pin Diagrams

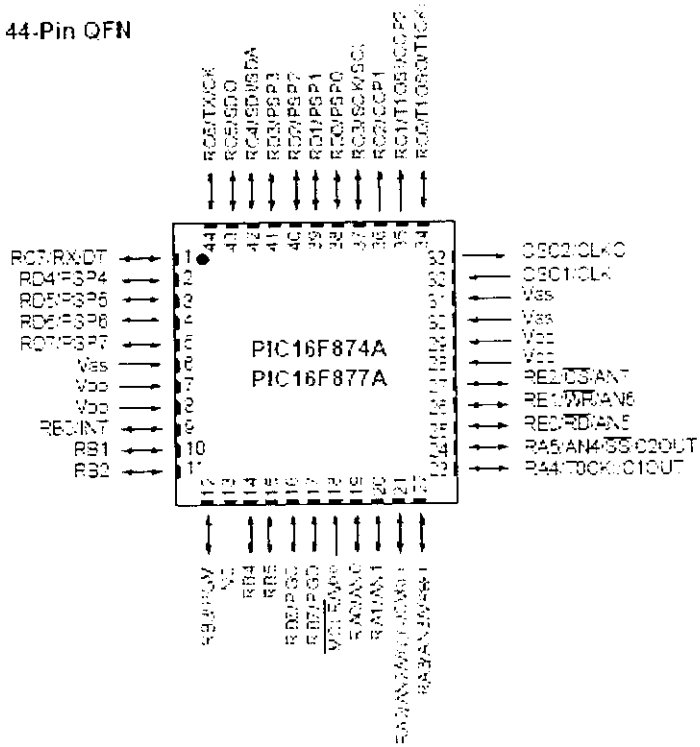
28-Pin PDIP, SOIC, SSOP



28-Pin QFN



44-Pin QFN



1.0 DEVICE OVERVIEW

This document contains device specific information about the following devices:

- PIC16F873A
- PIC16F874A
- PIC16F876A
- PIC16F877A

PIC16F873A/876A devices are available only in 28-pin packages, while PIC16F874A/877A devices are available in 40-pin and 44-pin packages. All devices in the PIC16F87XA family share common architecture with the following differences:

- The PIC16F873A and PIC16F874A have one-half of the total on-chip memory of the PIC16F876A and PIC16F877A
- The 28-pin devices have three I/O ports, while the 40/44-pin devices have five
- The 28-pin devices have fourteen interrupts, while the 40/44-pin devices have fifteen
- The 28-pin devices have five A/D input channels, while the 40/44-pin devices have eight
- The Parallel Slave Port is implemented only on the 40/44-pin devices

The available features are summarized in Table 1-1. Block diagrams of the PIC16F873A/876A and PIC16F874A/877A devices are provided in Figure 1-1 and Figure 1-2, respectively. The pinouts for these device families are listed in Table 1-2 and Table 1-3.

Additional information may be found in the PICmicro® Mid-Range Reference Manual (DS33023), which may be obtained from your local Microchip Sales Representative or downloaded from the Microchip web site. The Reference Manual should be considered a complementary document to this data sheet and is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

TABLE 1-1: PIC16F87XA DEVICE FEATURES

Key Features	PIC16F873A	PIC16F874A	PIC16F876A	PIC16F877A
Operating Frequency	DC – 20 MHz	DC – 20 MHz	DC – 20 MHz	DC – 20 MHz
Resets (and Delays)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)
Flash Program Memory (14-bit words)	4K	4K	8K	8K
Data Memory (bytes)	192	192	368	368
EEPROM Data Memory (bytes)	128	128	256	256
Interrupts	14	15	14	15
I/O Ports	Ports A, B, C	Ports A, B, C, D, E	Ports A, B, C	Ports A, B, C, D, E
Timers	3	3	3	3
Capture/Compare/PWM modules	2	2	2	2
Serial Communications	MSSP, USART	MSSP, USART	MSSP, USART	MSSP, USART
Parallel Communications	—	PSP	—	PSP
10-bit Analog-to-Digital Module	5 input channels	8 input channels	5 input channels	8 input channels
Analog Comparators	2	2	2	2
Instruction Set	35 Instructions	35 Instructions	35 Instructions	35 Instructions
Packages	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN	40-pin PDIP 44-pin PLCC 44-pin TQFP 44-pin QFN	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN	40-pin PDIP 44-pin PLCC 44-pin TQFP 44-pin QFN

TABLE 1-2: PIC16F873A/876A PINOUT DESCRIPTION

Pin Name	PDIP, SOIC, SSOP Pin#	QFN Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKI	9	6		ST/CMOS(3)	Oscillator crystal or external clock input.
OSC1			I		Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; otherwise CMOS.
CLKI			I		External clock source input. Always associated with pin function OSC1 (see OSC1/CLKI, OSC2/CLKO pins).
OSC2/CLKO	10	7		—	Oscillator crystal or clock output.
OSC2			O		Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO			O		In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	1	28		ST	Master Clear (input) or programming voltage (output).
$\overline{MCLR}$			I		Master Clear (Reset) input. This pin is an active low Reset to the device.
VPP			P		Programming voltage input.
					PORTA is a bidirectional I/O port.
RA0/AN0	2	27		TTL	
RA0			I/O		Digital I/O.
AN0			I		Analog input 0.
RA1/AN1	3	28		TTL	
RA1			I/O		Digital I/O.
AN1			I		Analog input 1.
RA2/AN2/VREF-/CVREF	4	1		TTL	
RA2			I/O		Digital I/O.
AN2			I		Analog input 2.
VREF-			I		A/D reference voltage (Low) input.
CVREF			O		Comparator VREF output.
RA3/AN3/VREF+	5	2		TTL	
RA3			I/O		Digital I/O.
AN3			I		Analog input 3.
VREF+			I		A/D reference voltage (High) input.
RA4/T0CKI/C1OUT	6	3		ST	
RA4			I/O		Digital I/O – Open-drain when configured as output.
T0CKI			I		Timer0 external clock input.
C1OUT			O		Comparator 1 output.
RA5/AN4/$\overline{SS}$/C2OUT	7	4		TTL	
RA5			I/O		Digital I/O.
AN4			I		Analog input 4.
$\overline{SS}$			I		SPI slave select input.
C2OUT			O		Comparator 2 output.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

TABLE 1-2: PIC16F873A/876A PINOUT DESCRIPTION (CONTINUED)

Pin Name	PDIP, SOIC, SSOP Pin#	QFN Pin#	I/O/P Type	Buffer Type	Description
					PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/INT	21	18		TTL/ST(1)	
RB0			I/O		Digital I/O.
INT			I		External interrupt.
RB1	22	19	I/O	TTL	Digital I/O.
RB2	23	20	I/O	TTL	Digital I/O.
RB3/PGM	24	21		TTL	
RB3			I/O		Digital I/O.
PGM			I		Low-voltage (single-supply) ICSP programming enable pin.
RB4	25	22	I/O	TTL	Digital I/O.
RB5	26	23	I/O	TTL	Digital I/O.
RB6/PGC	27	24		TTL/ST(2)	
RB6			I/O		Digital I/O.
PGC			I		In-circuit debugger and ICSP programming clock.
RB7/PGD	28	25		TTL/ST(2)	
RB7			I/O		Digital I/O.
PGD			I/O		In-circuit debugger and ICSP programming data.
					PORTC is a bidirectional I/O port.
RC0/T1OSO/T1CKI	11	8		ST	
RC0			I/O		Digital I/O.
T1OSO			O		Timer1 oscillator output.
T1CKI			I		Timer1 external clock input.
RC1/T1OSI/CCP2	12	9		ST	
RC1			I/O		Digital I/O.
T1OSI			I		Timer1 oscillator input.
CCP2			I/O		Capture2 input, Compare2 output, PWM2 output.
RC2/CCP1	13	10		ST	
RC2			I/O		Digital I/O.
CCP1			I/O		Capture1 input, Compare1 output, PWM1 output.
RC3/SCK/SCL	14	11		ST	
RC3			I/O		Digital I/O.
SCK			I/O		Synchronous serial clock input/output for SPI mode.
SCL			I/O		Synchronous serial clock input/output for I²C mode.
RC4/SDI/SDA	15	12		ST	
RC4			I/O		Digital I/O.
SDI			I		SPI data in.
SDA			I/O		I²C data I/O.
RC5/SDO	16	13		ST	
RC5			I/O		Digital I/O.
SDO			O		SPI data out.
RC6/TX/CK	17	14		ST	
RC6			I/O		Digital I/O.
TX			O		USART asynchronous transmit.
CK			I/O		USART1 synchronous clock.
RC7/RX/DT	18	15		ST	
RC7			I/O		Digital I/O.
RX			I		USART asynchronous receive.
DT			I/O		USART synchronous data.
VSS	8, 19	5, 6	P	—	Ground reference for logic and I/O pins.
VDD	20	17	P	—	Positive supply for logic and I/O pins.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

TABLE 1-3: PIC16F874A/877A PINOUT DESCRIPTION

Pin Name	PDIP Pin#	PLCC Pin#	TQFP Pin#	QFN Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKI	13	14	30	32		ST/CMOS(4)	Oscillator crystal or external clock input
OSC1					I		Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; otherwise CMOS.
CLKI					I		External clock source input. Always associated with pin function OSC1 (see OSC1/CLKI, OSC2/CLKO pins).
OSC2/CLKO	14	15	31	33		—	Oscillator crystal or clock output.
OSC2					O		Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO					O		In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
MCLR/VPP	1	2	18	18		ST	Master Clear (input) or programming voltage (output).
MCLR					I		Master Clear (Reset) input. This pin is an active low Reset to the device.
VPP					P		Programming voltage input.
							PORTA is a bidirectional I/O port.
RA0/AN0	2	3	19	19		TTL	
RA0					I/O		Digital I/O.
AN0					I		Analog input 0.
RA1/AN1	3	4	20	20		TTL	
RA1					I/O		Digital I/O.
AN1					I		Analog input 1.
RA2/AN2/VREF-/CVREF	4	5	21	21		TTL	
RA2					I/O		Digital I/O.
AN2					I		Analog input 2.
VREF-					I		A/D reference voltage (Low) input.
CVREF					O		Comparator VREF output.
RA3/AN3/VREF+	5	6	22	22		TTL	
RA3					I/O		Digital I/O.
AN3					I		Analog input 3.
VREF+					I		A/D reference voltage (High) input.
RA4/T0CKI/C1OUT	6	7	23	23		ST	
RA4					I/O		Digital I/O – Open-drain when configured as output.
T0CKI					I		Timer0 external clock input.
C1OUT					O		Comparator 1 output.
RA5/AN4/SS/C2OUT	7	8	24	24		TTL	
RA5					I/O		Digital I/O.
AN4					I		Analog input 4.
SS					I		SPI slave select input.
C2OUT					O		Comparator 2 output.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

TABLE 1-3: PIC16F874A/877A PINOUT DESCRIPTION (CONTINUED)

Pin Name	PDIP Pin#	PLCC Pin#	TQFP Pin#	QFN Pin#	I/O/P Type	Buffer Type	Description
							PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs
RB0/INT	33	36	8	9		TTL/ST(1)	
RB0					I/O		Digital I/O
INT					I		External interrupt
RB1	34	37	9	10	I/O	TTL	Digital I/O
RB2	35	38	10	11	I/O	TTL	Digital I/O
RB3/PGM	36	39	11	12		TTL	
RB3					I/O		Digital I/O
PGM					I		Low-voltage ICSP programming enable pin.
RB4	37	41	14	14	I/O	TTL	Digital I/O
RB5	38	42	15	15	I/O	TTL	Digital I/O
RB6/PGC	39	42	16	16		TTL/ST(2)	
RB6					I/O		Digital I/O
PGC					I		In-circuit debugger and ICSP programming clock.
RB7/PGD	40	44	17	17		TTL/ST(2)	
RB7					I/O		Digital I/O
PGD					I/O		In-circuit debugger and ICSP programming data.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

APPENDIX B

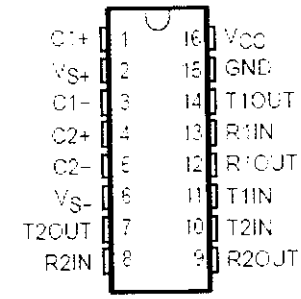
MAX232

MAX232, MAX232I
DUAL EIA-232 DRIVERS/RECEIVERS

SLLS047L – FEBRUARY 1989 – REVISED MARCH 2004

- Meets or Exceeds TIA/EIA-232-F and ITU Recommendation V.28
- Operates From a Single 5-V Power Supply With 1.0-μF Charge-Pump Capacitors
- Operates Up To 120 kbit/s
- Two Drivers and Two Receivers
- ±30-V Input Levels
- Low Supply Current . . . 8 mA Typical
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
- Upgrade With Improved ESD (15-kV HBM) and 0.1-μF Charge-Pump Capacitors is Available With the MAX202
- Applications
  - TIA/EIA-232-F, Battery-Powered Systems, Terminals, Modems, and Computers

MAX232 . . . D, DW, N, OR NS PACKAGE
MAX232I . . . D, DW, OR N PACKAGE
(TOP VIEW)



description/ordering information

The MAX232 is a dual driver/receiver that includes a capacitive voltage generator to supply TIA/EIA-232-F voltage levels from a single 5-V supply. Each receiver converts TIA/EIA-232-F inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V, a typical hysteresis of 0.5 V, and can accept ±30-V inputs. Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASIC™ library.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (N)	Tube of 25	MAX232N	MAX232N
	SOIC (D)	Tube of 40	MAX232D	MAX232
		Reel of 2500	MAX232DR	
	SOIC (DW)	Tube of 40	MAX232DW	MAX232
		Reel of 2000	MAX232DWR	
	SOP (NS)	Reel of 2000	MAX232NSR	MAX232
−40°C to 85°C	PDIP (N)	Tube of 25	MAX232IN	MAX232IN
	SOIC (D)	Tube of 40	MAX232ID	MAX232I
		Reel of 2500	MAX232IDR	
	SOIC (DW)	Tube of 40	MAX232IDW	MAX232I
		Reel of 2000	MAX232IDWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input supply voltage range, V_{CC} (see Note 1)		−0.3 V to 6 V
Positive output supply voltage range, V_{S+}		V_{CC} − 0.3 V to 15 V
Negative output supply voltage range, V_{S-}		−0.3 V to −15 V
Input voltage range, V_I: Driver		−0.3 V to V_{CC} + 0.3 V
Receiver		±30 V
Output voltage range, V_O: T1OUT, T2OUT		V_{S-} − 0.3 V to V_{S-} + 0.3 V
R1OUT, R2OUT		−0.3 V to V_{CC} + 0.3 V
Short-circuit duration: T1OUT, T2OUT		Unlimited
Package thermal impedance, θ_{JA} (see Notes 2 and 3):	D package	73°C/W
	DW package	57°C/W
	N package	67°C/W
	NS package	64°C/W
Operating virtual junction temperature, T_J		150°C
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to network GND.

2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage (T1IN, T2IN)		2			V
V_{IL}	Low-level input voltage (T1IN, T2IN)				0.8	V
R1IN, R2IN	Receiver input voltage				±30	V
T_A	Operating free-air temperature	MAX232	0		70	°C
		MAX232I	−40		85	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_{CC}	Supply current	V_{CC} = 5.5 V, All outputs open, T_A = 25°C		8	10	mA

‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.

NOTE 4: Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (see Note 4)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	T1OUT, T2OUT	R_L = 3 kΩ to GND	5	7		V
V_{OL}	Low-level output voltage‡	T1OUT, T2OUT	R_L = 3 kΩ to GND		–7	–5	V
r_o	Output resistance	T1OUT, T2OUT	V_{S+} = V_{S-} = 0, V_O = ±2 V	300			Ω
I_{OS}§	Short-circuit output current	T1OUT, T2OUT	V_{CC} = 5.5 V, V_O = 0		±10		mA
I_{IS}	Short-circuit input current	T1IN, T2IN	V_I = 0			200	µA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
§ Not more than one output should be shorted at a time.
NOTE 4: Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Note 4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Driver slew rate	R_L = 3 kΩ to 7 kΩ, See Figure 2			30	V/µs
SR(t)	Driver transition region slew rate	See Figure 3		3		V/µs
	Data rate	One TOUT switching		120		kbits

NOTE 4: Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (see Note 4)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	R1OUT, R2OUT	I_{OH} = –1 mA	3.5			V
V_{OL}	Low-level output voltage‡	R1OUT, R2OUT	I_{OL} = 3.2 mA			0.4	V
V_{IT+}	Receiver positive-going input threshold voltage	R1IN, R2IN	V_{CC} = 5 V, T_A = 25°C		1.7	2.4	V
V_{IT-}	Receiver negative-going input threshold voltage	R1IN, R2IN	V_{CC} = 5 V, T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis voltage	R1IN, R2IN	V_{CC} = 5 V	0.2	0.5	1	V
r_i	Receiver input resistance	R1IN, R2IN	V_{CC} = 5, T_A = 25°C	3	5	7	kΩ

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
NOTE 4: Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Note 4 and Figure 1)

PARAMETER		TYP	UNIT
$t_{PLH(R)}$	Receiver propagation delay time, low- to high-level output	500	ns
$t_{PHL(R)}$	Receiver propagation delay time, high- to low-level output	500	ns

NOTE 4: Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

APPENDIX C

CONTROL REGISTERS FOR I2C PROTOCOL

SSPSTAT: SYNC SERIAL PORT STATUS REGISTER (ADDRESS: 94h)

REGISTER 9-1: SSPSTAT: MSSP STATUS REGISTER (SPI MODE) (ADDRESS 94h)

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF
bit 7							bit 0

bit 7 **SMP:** Sample bit

SPI Master mode:

1 = Input data sampled at end of data output time

0 = Input data sampled at middle of data output time

SPI Slave mode:

SMP must be cleared when SPI is used in Slave mode.

bit 6 **CKE:** SPI Clock Select bit

1 = Transmit occurs on transition from active to Idle clock state

0 = Transmit occurs on transition from Idle to active clock state

Note: Polarity of clock state is set by the CKP bit (SSPCON1<4>).

bit 5 **D/$\overline{A}$:** Data/$\overline{Address}$ bit

Used in I^2C mode only.

bit 4 **P:** Stop bit

Used in I^2C mode only. This bit is cleared when the MSSP module is disabled. SSPEN is cleared.

bit 3 **S:** Start bit

Used in I^2C mode only.

bit 2 **R/$\overline{W}$:** Read/$\overline{Write}$ bit information

Used in I^2C mode only.

bit 1 **UA:** Update Address bit

Used in I^2C mode only.

bit 0 **BF:** Buffer Full Status bit (Receive mode only)

1 = Receive complete, SSPBUF is full

0 = Receive not complete, SSPBUF is empty

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

SSPCON: SYNC SERIAL PORT CONTROL REGISTER (ADDRESS 14h)

REGISTER 9-2: SSPCON1: MSSP CONTROL REGISTER 1 (SPI MODE) (ADDRESS 14h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0
bit 7							bit 0

bit 7 **WCOL:** Write Collision Detect bit (Transmit mode only)

1 = The SSPBUF register is written while it is still transmitting the previous word. (Must be cleared in software.)

0 = No collision

bit 6 **SSPOV:** Receive Overflow Indicator bit

SPI Slave mode:

1 = A new byte is received while the SSPBUF register is still holding the previous data. In case of overflow, the data in SSPSR is lost. Overflow can only occur in Slave mode. The user must read the SSPBUF, even if only transmitting data, to avoid setting overflow. (Must be cleared in software.)

0 = No overflow

Note: In Master mode, the overflow bit is not set, since each new reception (and transmission) is initiated by writing to the SSPBUF register.

bit 5 **SSPEN:** Synchronous Serial Port Enable bit

1 = Enables serial port and configures SCK, SDO, SDI, and $\overline{SS}$ as serial port pins

0 = Disables serial port and configures these pins as I/O port pins

Note: When enabled, these pins must be properly configured as input or output.

bit 4 **CKP:** Clock Polarity Select bit

1 = Idle state for clock is a high level

0 = Idle state for clock is a low level

bit 3-0 **SSPM3:SSPM0:** Synchronous Serial Port Mode Select bits

0101 = SPI Slave mode, clock = SCK pin. $\overline{SS}$ pin control disabled. $\overline{SS}$ can be used as I/O pin.

0100 = SPI Slave mode, clock = SCK pin. $\overline{SS}$ pin control enabled.

0011 = SPI Master mode, clock = TMR2 output/2

0010 = SPI Master mode, clock = Fosc/64

0001 = SPI Master mode, clock = Fosc/16

0000 = SPI Master mode, clock = Fosc/4

Note: Bit combinations not specifically listed here are either reserved or implemented in I^2C mode only.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

SSPCON2: SYNC SERIAL PORT CONTROL REGISTER2 (ADDRESS 91h)

REGISTER 9-5: SSPCON2: MSSP CONTROL REGISTER 2 (I^2C MODE) (ADDRESS 91h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7							bit 0

bit 7 **GCEN:** General Call Enable bit (Slave mode only)

1 = Enable interrupt when a general call address (0000h) is received in the SSPSR
0 = General call address disabled

bit 6 **ACKSTAT:** Acknowledge Status bit (Master Transmit mode only)

1 = Acknowledge was not received from slave
0 = Acknowledge was received from slave

bit 5 **ACKDT:** Acknowledge Data bit (Master Receive mode only)

1 = Not Acknowledge
0 = Acknowledge

Note: Value that will be transmitted when the user initiates an Acknowledge sequence at the end of a receive.

bit 4 **ACKEN:** Acknowledge Sequence Enable bit (Master Receive mode only)

1 = Initiate Acknowledge sequence on SDA and SCL pins and transmit ACKDT data bit. Automatically cleared by hardware.
0 = Acknowledge sequence Idle

bit 3 **RCEN:** Receive Enable bit (Master mode only)

1 = Enables Receive mode for I^2C
0 = Receive Idle

bit 2 **PEN:** Stop Condition Enable bit (Master mode only)

1 = Initiate Stop condition on SDA and SCL pins. Automatically cleared by hardware
0 = Stop condition Idle

bit 1 **RSEN:** Repeated Start Condition Enabled bit (Master mode only)

1 = Initiate Repeated Start condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Repeated Start condition Idle

bit 0 **SEN:** Start Condition Enabled/Stretch Enabled bit

In Master mode:
1 = Initiate Start condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Start condition Idle

In Slave mode:
1 = Clock stretching is enabled for both slave transmit and slave receive (stretch enabled)
0 = Clock stretching is enabled for slave transmit only (PIC16F87X compatibility)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

APPENDIX D

CONTROL REGISTERS FOR USART PROTOCOL

TXSTA: Transmit Status and Control Register

CSRC	TX9	TXEN	SYNC	-------	BRGH	TRMT	TX9D
bit 7							Bit 0

Bit 7 **CSRC:** Clock Source Select bit

Asynchronous mode

Don't care

Synchronous mode

1 = Master mode (Clock generated internally from BRG)

0 = Slave mode (Clock from external source)

Bit 6 **TX9**: 9-bit Transmit Enable bit

1 = Selects 9-bit transmission

0 = Selects 8-bit transmission

Bit 5 **TXEN**: Transmit Enable bit

1 = Transmit enabled

0 = Transmit disabled

Bit 4 **SYNC**: USART Mode Select bit

1 = Synchronous mode

0 = Asynchronous mode

Bit 3 **Unimplemented:** Read as '0'

Bit 2 **BRGH**: High Baud Rate Select bit

Asynchronous mode

1 = High speed

0 = Low speed

Synchronous mode

Bit 1 **TRMT**: Transmit Shift Register Status bit

1 = TSR empty

0 = TSR full

Bit 0 **TX9D:**

9th bit of transmit data. Can be parity bit

RCSTA: Receive Status and Control Register

SPEN	RX9	SREN	CREN	-----	FERR	OERR	RX9D

Bit 7 bit 0

bit 7 **SPEN:**Serial Port Enable bit

1 = Serial port enabled (Configures RX/DT and TX/CK pins as serial port pins)

0 = Serial port disabled

bit 6 **RX9**: 9-bit Receive Enable bit

1 = Selects 9-bit reception

0 = Selects 8-bit reception

bit 5 **SREN**: Single Receive Enable bit

Asynchronous mode

Don't care

Synchronous mode - master

1 = Enables single receive

0 = Disables single receive

This bit is cleared after reception is complete.

Synchronous mode - slave

Unused in this mode

bit 4 **CREN** : Continuous Receive Enable bit

Asynchronous mode

0 = Disables continuous receive

Synchronous mode

1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)

0 = Disables continuous receive

bit 3 **Unimplemented:**

Read as '0'

bit 2 **FERR**: Framing Error bit

1 = Framing error (Can be updated by reading RCREG register and receive next valid byte)

0 = No framing error

bit 1 **OERR**: Overrun Error bit

1 = Overrun error (Can be cleared by clearing bit CREN)

0 = No overrun error

bit 0 **RX9D**

9th bit of received data can be parity bit.

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