ROBOT ASSISSTED NAVIGATION FOR VISUALLY IMPAIRED

A PROJECT REPORT

Submitted by

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BONAFIDE CERTIFICATE

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"WE DEDICATE THIS PROJECT TO OUR PARENTS,
FRIENDS AND OUR PROJECT GUIDE
WHO HAVE INSPIRED US...."

ABSTRACT

The main aim of the project is to implement robot assisted navigation for the visually impaired. For most visually impaired people, the main barrier in improving their quality of life is the inability to navigate. A robotic guide for the visually impaired that could interact well with them and make their navigation very easy is illustrated.

The user can interact with the robot in unimaginable ways like speech, wearable keyboard, audio, etc unlike guide dogs and white canes. Radio Frequency Identification (RFID) is used in identifying the blocks. The navigation is not dependent on the RFID tags.

Usage of Radio Frequency Identification (RFID) in robot-assisted indoor navigation for visually impaired is discussed. The experiments illustrate that passive RFID tags deployed in the environment can act as reliable stimuli that trigger local navigation behaviors to achieve global navigation objectives.

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INTRODUCTION

Visually impaired population face a lot of problems in moving from place to place. They have to depend on guide dogs, canes or some others to help them to move around. This project can make them move independently in indoor environment like airport, shopping mall, industries, technology centers, etc.

The components used are

- Voice processing unit
- RFID unit
- Microcontroller
- Object sensor
- Robot model and
- Keypad

Voice processing unit is used to speak out the identified locations, when the RFID reader senses the tag.

Object sensor is used to sense any obstacles in the path. Keypad is used to enter the user's desired destination.

Micro controller is used to control the robotic motion and other components. Micro controller coding is done using c language with help of KEIL C software.

The general block diagram of the project is shown below.

1. BLOCK DIAGRAM:

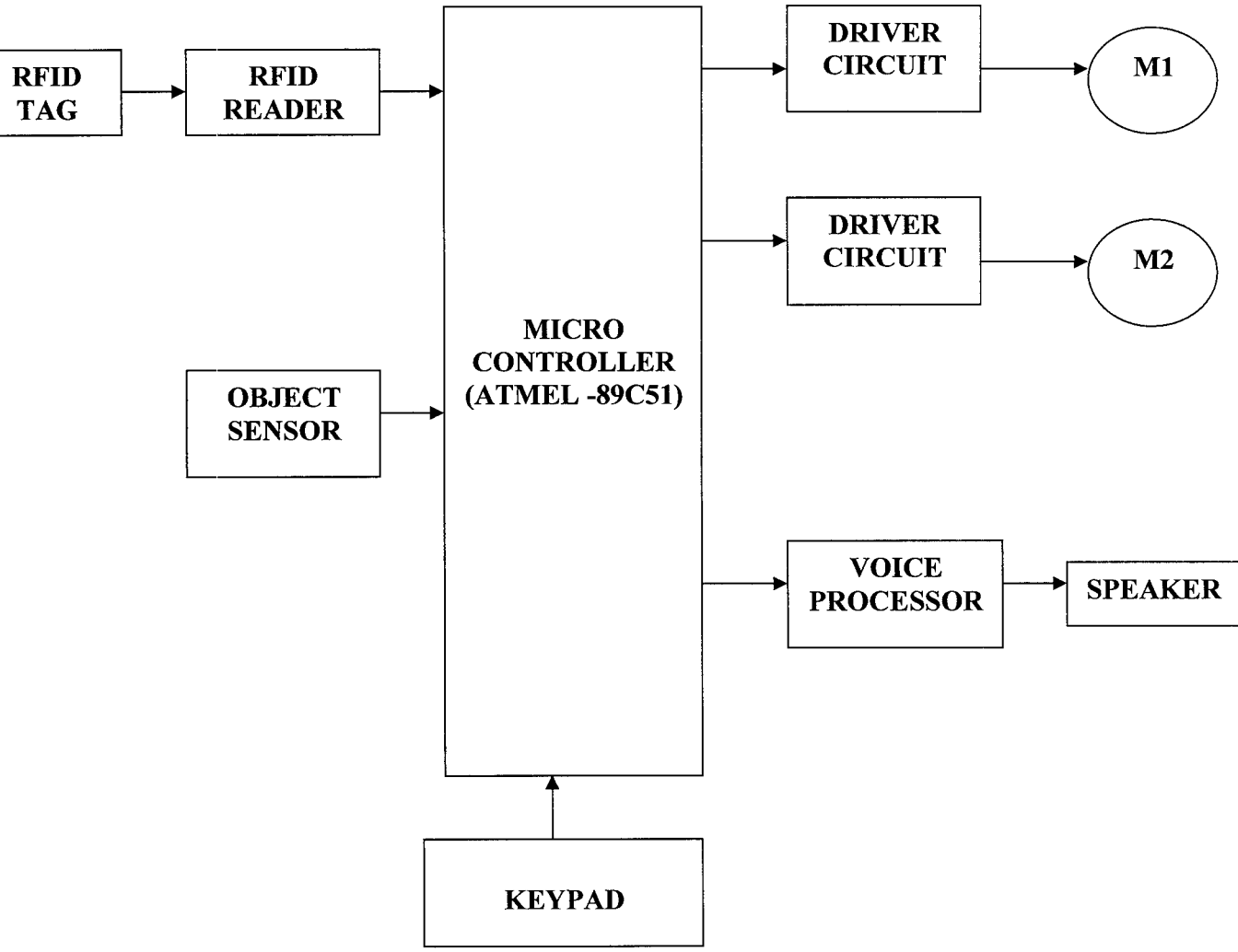


FIGURE 1.1

2. MICROCONTROLLER (ATMEL 89C51):

2.1 Description:

Microcontroller is a general purpose device, which integrates a number of components of a microprocessor system onto a single chip. It has inbuilt CPU, memory and peripherals to make it as a mini computer. A microcontroller combines on to the same microchip:

- The CPU core
- Memory(both ROM and RAM)
- Some parallel digital i/o

Microcontrollers will combine other devices such as:

- A timer module to allow the microcontroller to perform tasks for certain time periods.
- A serial I/O port to allow data to flow between the controller and other devices such as a PIC or another microcontroller.
- An ADC to allow the microcontroller to accept analogue input data for processing.

Microcontrollers are:

- Smaller in size
- Consumes less power
- Inexpensive

Micro controller is a stand alone unit, which can perform functions on its own without any requirement for additional hardware like I/O ports and external memory. The heart of the microcontroller is the CPU core. In the past, this has traditionally been based on a 8-bit microprocessor unit. For example Motorola uses a basic 6800 microprocessor core in their 6805/6808 microcontroller devices.

In the recent years, microcontrollers have been developed around specifically designed CPU cores, for example the microchip PIC range of microcontrollers.

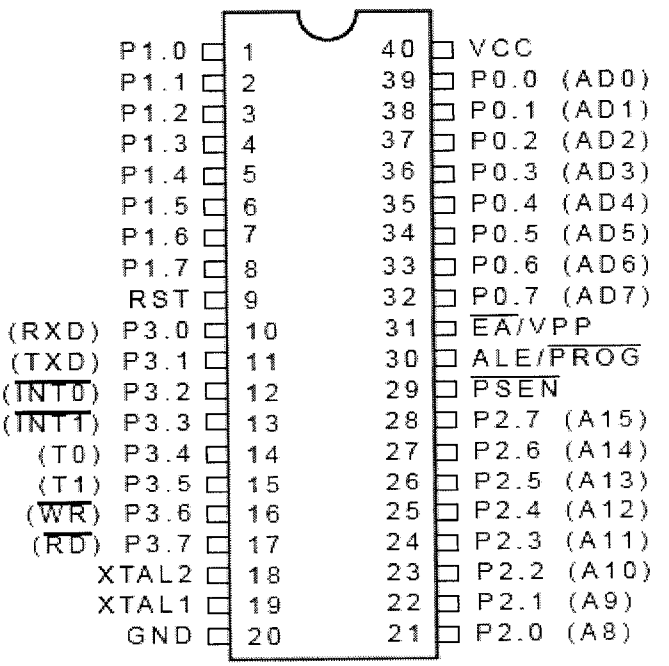
AT89C51 is the 40 pins, 8 bit Microcontroller manufactured by Atmel group. It is the flash type reprogrammable memory.

Advantage of this flash memory is we can erase the program with in few minutes. It has 4kb on chip ROM and 128 bytes internal RAM and 32 I/O pin as arranged as port 0 to port 3 each has 8 bit bin .Port 0 contains 8 data line(D0-D7) as well as low order address line(AO-A7). Port 2 contains higher order address line (A8-A15). Port 3 contains special purpose register such as serial input receiver register SBUF, interrupt INT0,INT1 and timers T_0 , T_1. Many of the pins have multi functions which can be used as general purpose I/O pins (or) Special purpose function can be decided by the programmer itself.

- 4K Bytes of In-System Reprogrammable Flash Memory
- Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-Level Program Memory Lock
- 128 x 8-Bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low Power Idle and Power Down Modes

The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K bytes of Flash Programmable and Erasable Read Only Memory (EPROM). The device is manufactured using Atmel is high density nonvolatile memory technology and is compatible with the industry standard MCS-51™ instruction set and pin out. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications

2.2 PIN CONFIGURATION:



(ATMEL 89C51)

FIGURE 2.1

2.3 Pin Description:

VCC - Supply voltage.

GND - Ground.

2.3.1 Port 0:

Port 0 is an 8-bit open drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high impedance inputs. Port 0 can also be configured to be the multiplexed low order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups. Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pull-ups are required during program verification.

2.3.2 Port 1:

Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL) because of the internal pull-ups. In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively, as shown in the following table. Port 1 also receives the low-order address bytes during Flash programming and verification.

Functions:

Port Pin	*Alternate Functions*
P 1.0	T2 (external count input to Timer/Counter2), clock-out
P 1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P 1.5	MOSI (used for In-System Programming)
P 1.6	MISO (used for In-System Programming)
P 1.7	SCK (used for In-System Programming)

TABLE 2.1 (PORT1 FUNCTIONS)

2.3.3 Port 2:

Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL) because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that uses 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that uses 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register. Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

2.3.4 Port 3:

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL) because of the pull-ups. Port 3 also serves the functions of various special features of the AT89S52, as shown in the following table. Port 3 also receives some control signals for Flash programming and verification.

Functions:

Port Pin	Alternate Functions
P 3.0	RXD (serial input port)
P 3.1	TXD (serial output port)
P 3.2	INT0 (external interrupt 0
P 3.3	INT1 (external interrupt 1)
P 3.4	T0 (timer 0 external input)
P 3.5	T1 (timer 1 external input)
P 3.6	WR (external data memory write strobe
P3.7	RD (external data memory read strobe)

TABLE 2.2 (PORT3 FUNCTIONS)

2.3.5 RST:

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 96 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

2.3.6 ALE/PROG:

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory. If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the micro-controller is in external execution mode.

2.3.7 PSEN:

Program Store Enable (PSEN) is the read strobe to external program memory. When the AT89S52 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

2.3.8 EA/VPP:

External Access Enable, EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset. EA should be strapped to VCC for internal program executions. This pin also receives the 12-volt programming enable voltage (VPP) during Flash programming.

2.3.9 XTAL1:

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

2.4 Block Diagram (ATMEL 89C51):

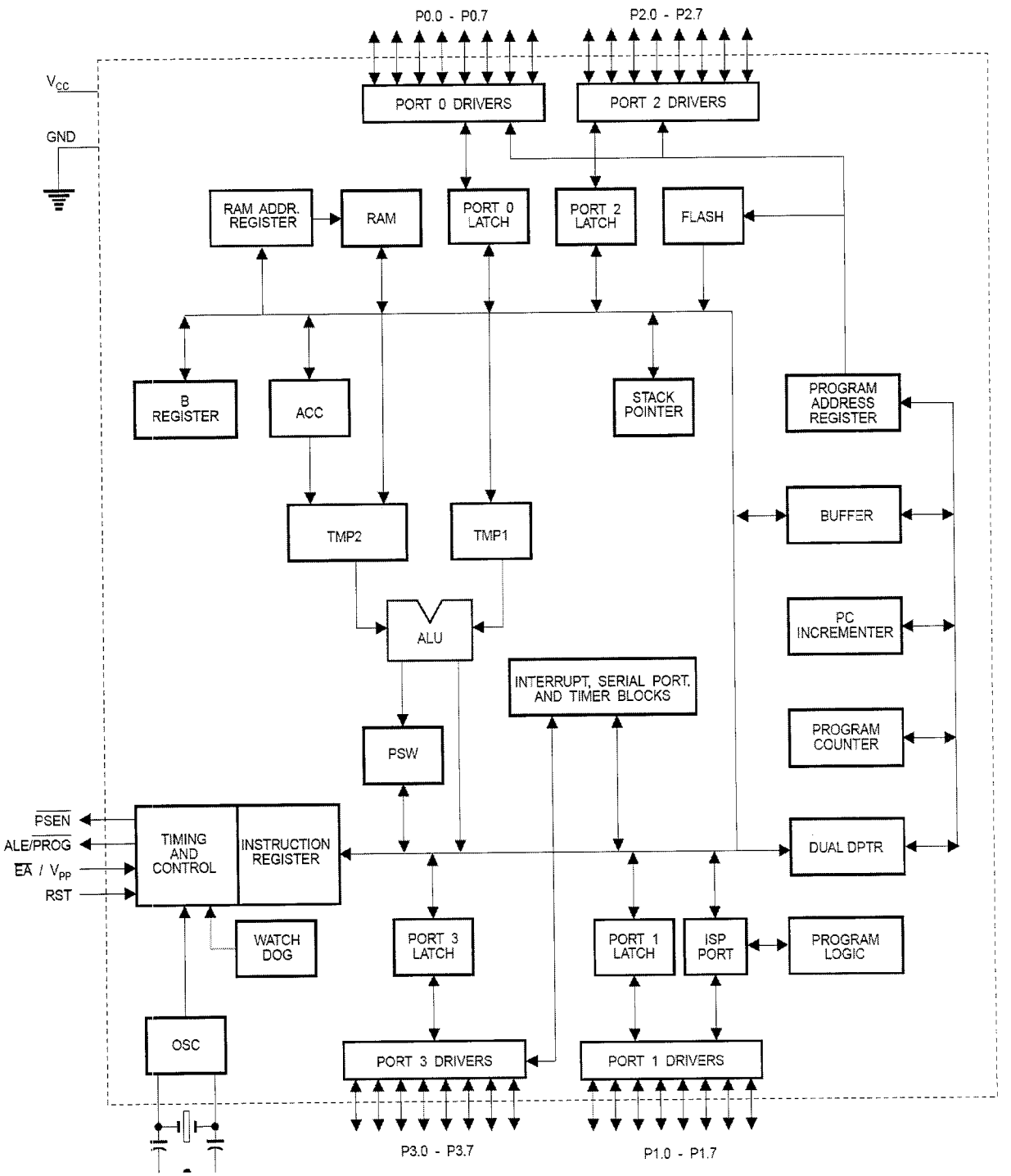


FIGURE 2.2

2.5 Oscillator Characteristics:

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator. Either a quartz crystal or ceramic resonator may be used. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maxi-mum voltage high and low time specifications must be observed.

2.6 Idle Mode:

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

2.7 Power down Mode:

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and

Special Function Registers retain their values until the Power-down mode is terminated. Reset redefines the SFRs but does not change the on-chip RAM.

The reset should not be activated before VCC is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

2.8 Status of external pins during Idle and Power Down Modes:

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-Down	Internal	0	0	Data	Data	Data	Data
Power-Down	External	0	0	Float	Data	Data	Data

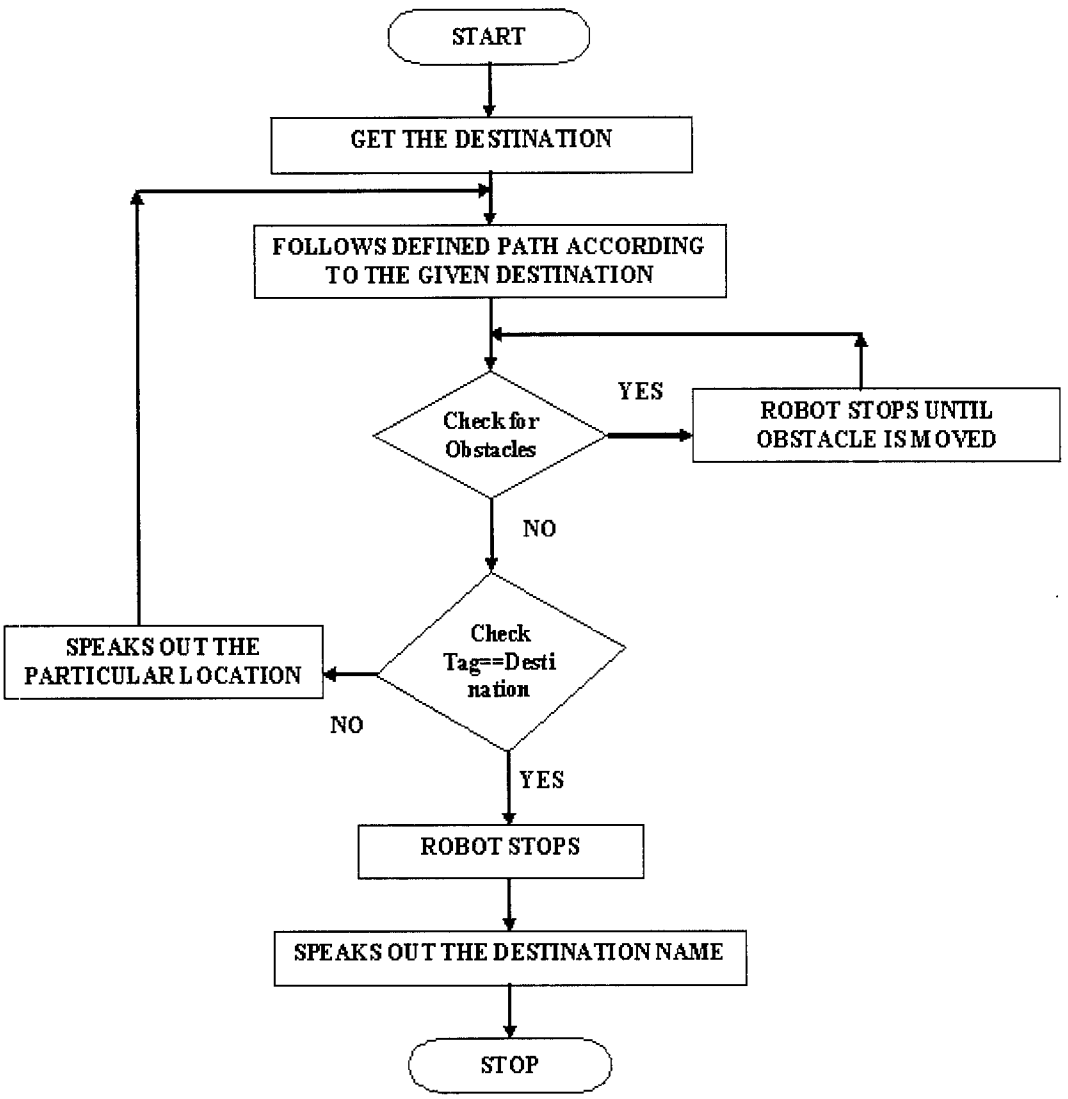
TABLE 2.3

2.9 Program Memory Lock Bits:

The AT89S52 has three lock bits that can be left un-programmed(U) or can be programmed (P) to obtain the additional features .When lock bit 1 is programmed, the logic level at the EA pins sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of EA must agree with the current logic level at that pin in order for the device to function properly.

2.10. MICROCONTROLLER PROGRAMMING:

Microcontroller coding is done in C language and it is converted into a language that can be used by the microcontroller through software called as "KEIL C". The flowchart for the microcontroller coding is given below



3. APR9600-VOICE PROCESSING UNIT:

3.1 INTRODUCTION:

APR9600 is a low-cost high performance sound record/replay IC incorporating flash analogue storage technique. Recorded sound is retained even after power supply is removed from the module. The replayed sound exhibits high quality with a low noise level.

Sampling rate for a 60 second recording period is 4.2 kHz that gives a sound record/replay bandwidth of 20Hz to 2.1 kHz. However, by changing an oscillation resistor, a sampling rate as high as 8.0 kHz can be achieved. This shortens the total length of sound recording to 32 seconds. Total sound recording time can be varied from 32 seconds to 60 seconds by changing the value of a single resistor.

The IC can operate in one of two modes: serial mode and parallel mode. In serial access mode, sound can be recorded in 256 sections. In parallel access mode, sound can be recorded in 2, 4 or 8 sections. The IC can be controlled simply using push button keys. It is also possible to control the IC using external digital circuitry such as micro-controllers and computers.

The APR9600 has a 28 pin DIP package. Supply voltage is between 4.5V to 6.5V. During recording and replaying, current consumption is 25 mA. In idle mode, the current drops to 1A.

The APR9600 experimental board is an assembled PCB board consisting of an APR9600 IC, an electret's microphone, support components and necessary switches to allow users to explore all functions of the APR9600 chip. The oscillation resistor is chosen so that the total recording period is 60 seconds with a sampling rate of 4.2 kHz. The board measures 80mm by 55mm.

3.2 WORKING PRINCIPLE:

During sound recording, sound is picked up by the microphone. A microphone pre-amplifier amplifies the voltage signal from the microphone. An AGC circuit is included in the pre-amplifier, the extent of which is Controlled by an external capacitor and resistor.

If the voltage level of a sound signal is around 100 mV peak to- peak, the signal can be fed directly into the IC through ANA IN pin (pin 20). The sound signal passes through a filter and a sampling and hold circuit. The analogue voltage is then written into non-volatile flash analogue RAMs.It has a 28 pin DIP package. Supply voltage is between 4.5V to 6.5V. During recording and replaying, current consumption is 25 mA. In idle mode, the current drops to 1A.

During sound replaying, the IC's control circuit reads analogue data from flash RAMs. The signal then passes through a low-pass filter, a power amplifier and output to an 8 to 16 Ohm speaker. There is different sound recording and replaying modes (Table 2). These modes are selected using MSEL1 (Pin 24), MSEL2 (Pin 25) and –M8 (Pin 9). –M1 to –M7 keys have different functions in different modes.

3.3 PIN DIAGRAM:

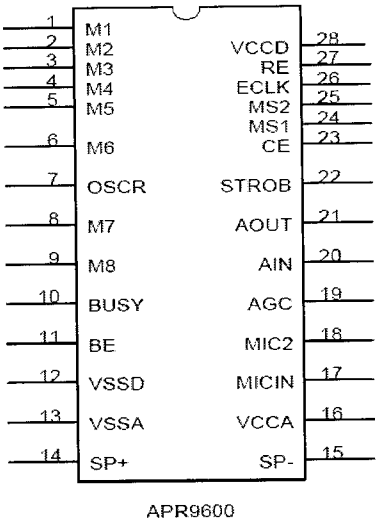


FIGURE 3.1

3.4 PIN FUNCTIONS:

Pin	Name	Functions	Pin	Mane	Functions
1	-M1	Select 1st section of sound or serial mode recording and replaying control (low active)	15	SP-	Speaker, negative end
2	-M2	Select 2nd section or fast forward control in serial mode (low active)	16	VCCA	Analogue circuit power supply
3	-M3	Select 3rd section of sound	17	MICIN	Microphone input (electret type microphone)
4	-M4	Select 4th section of sound	18	MICREF	Microphone reference input
5	-M5	Select 5th section of sound	19	AGC	AGC control
6	-M6	Select 6th section of sound	20	ANA-IN	Audio input (accept a signal of 100 mV p-to-p)
7	OSCR	Resistor to set clock frequency. See Table 3 for details	21	ANA-OUT	Audio output from the microphone amplifier
8	-M7	Select 7th section of sound or IC overflow indication	22	STROBE	During recording and replaying, it produces a strobe signal
9	-M8	Select 8th section of sound or select mode (see Table 2)	23	CE	Reset sound track counter to zero/ Stop or Start / Stop
10	-BUSY	Busy (low active)	24	MSEL1	Mode selection 1 (see Table 2)
11	BE	=1, beep when a key is pressed =0, do not beep	25	MSEL2	Mode selection 2 (see Table 2)
12	VSSD	Digital circuit ground	26	EXTCLK	External clock input
13	VSSA	Analogue circuit ground	27	-RE	=0 to record, =1 to replay
14	SP+	Speaker, positive end	28	VCCD	Digital circuit power supply

Table 3.1

3.5 MODES AND SELECTION OF MODES:

MSEL1	MSEL2	-M8	Function Keys	Functions
0	1	0 or 1	-M1, -M2 to select 1st and 2nd sound tracks. CE to stop	Parallel mode, 2 sections, 30 seconds for each
1	0	0 or 1	-M1 to –M4 to select a sound track, CE to stop	Parallel mode, 4 sections, 15 seconds for each
1	1	1	-M1 to –M8 to select a sound track, CE to stop	Parallel mode, 8 sections, 7.5 seconds for each
1	1	1	-M1 to –M8 to select a sound track, CE to stop	Pressing and hold down a key from –M1 to M8 to play the selected sound track repeatedly
0	0	1	-M1 and CE	Serial mode, allow up to 256 sound tracks to be recorded and played. Sound tracks are played from 1st to N in order after –M1 is toggled. Press CE to play from the 1st sound track.
0	0	0	-M1,-M2 and CE	Serial mode, Press –M1 to replay one sound track. Toggle –M2 once to move to the next sound track. Press CE to play sound from the 1st sound track

Table 3.2

NOTES:

- RE=0 to record sound. RE=1 to replay sound
- Press -M1 to -M8 once to replay a sound track. Press the key again to stop replaying the track
- Press and hold –M1 to -M8 continuously, the corresponding track will be replayed repeatedly
- During recording, -M1 to M8 should be pressed while the sound is being recorded. Releasing the key terminates recording.

3.6 APR MODULE:

The module consists of an APR9600 chip, an electret's microphone, support components, a mode selection switch (-RE, MSEL1, MSEL2 and –M8) and 9 keys (-M1 to –M8 and CE). The oscillation resistor is chosen so that the total recording period is 60 seconds with a sampling rate of 4.2 kHz.

Users can change the value of the ROSC to obtain other sampling frequencies. It should be noted that if the sampling rate is increased, the length of recording time is decreased. Table 3 gives the details.

An 8-16 Ohm speaker is to be used with the module. Users can select different modes using mode selection switch. The module is measured 80mmx55mm.

Connection points (0-8, C and B) can connect to other switches or external digital circuits. In this cased, on-board keys M1 to M8 and CE are by-passed.

3.7 PARALLEL MODE RECORDING AND REPLAYING:

3.7.1 RECORD SOUND TRACKS:

For recording 8 sound tracks, the mode switch should have the following pattern: MSEL1=1(switched to left-hand side of the mode selection switch), MSEL2=1 (left-hand side). –M8=1 (left-hand side). RE=0 (right-hand side). The maximum length of the 8 tracks is 7.5seconds.

Press –M1 continuously and you will see BUZY LED illuminates. You can now speak to the microphone. Recording will terminate if –M1 is released or if the recording time exceeds 7.5seconds. Similarly, press –M2 to -M8 to record other sound tracks.

3.7.2 REPLAY SOUND TRACKS:

Now make RE=1 (switched to Left-hand side of the mode selection switch) while keep other switches at the same location. Toggle –M1 to –M8 (press key and release) causes a particular sound track to replay once.

While the sound is playing, press the same key again or press CE key will terminate the current sound track. Press other key while a sound is being played causes a new sound track to be played.

If a key from –M1 to -M8 is pressed continuously, the particular sound track will be played continuously. Press CE to stop playing the sound track.

4. DC MOTOR FORWARD & REVERSE CONTROL:

4.1 CIRCUIT DIAGRAM:

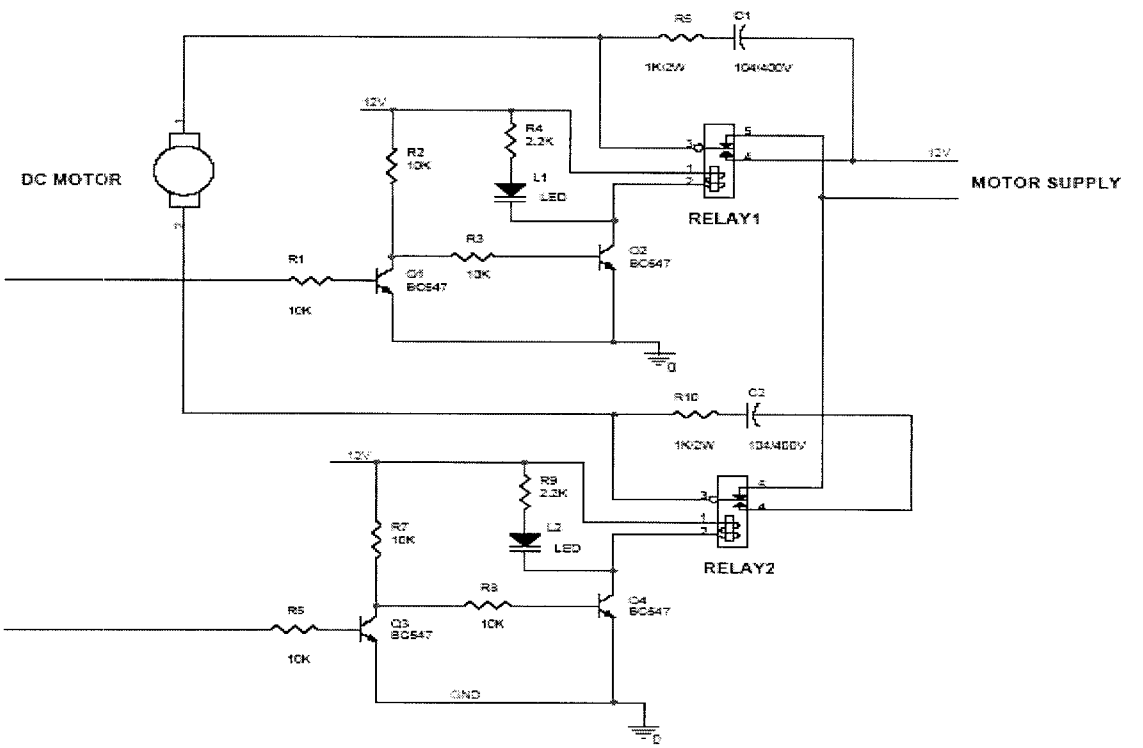


FIGURE 4.1

4.2 WORKING:

This circuit is designed to control the motor in the forward and reverse direction. It consists of two relays named as relay1 and relay2. The relay ON and OFF is controlled by the pair of switching transistors. A Relay is nothing but electromagnetic switching device which consists of three pins. They are Common, Normally close (NC) and normally open (NO). The common pin of two relay is connected to positive and negative terminal of motor through snubber circuit respectively. The relays are connected in the collector terminal of the transistors T2 and T4.

When high pulse signal is given to either base of the T1 or T3 transistors, the transistor is conducting and shorts the collector and emitter terminal and zero signals is given to base of the T2 or T4 transistor. So the relay is turned OFF state.

When low pulse is given to either base of transistor T1 or T3 transistor, the transistor is turned OFF. Now 12v is given to base of T2 or T4 transistor so the transistor is conducting and relay is turn ON. The NO and NC pins of two relays are interconnected so only one relay can be operated at a time.

The series combination of resistor and capacitor is called as snubber circuit. When the relay is turn ON and turn OFF continuously, the back emf may fault the relays. So the back emf is grounded through the snubber circuit.

- When relay 1 is in the ON state and relay 2 is in the OFF state, the motor is running in the forward direction.

- When relay 2 is in the ON state and relay 1 is in the OFF state, the motor is running in the reverse direction.

5. RELAY:

A relay is an electrically operated switch. Current flowing through the coil of the relay creates a magnetic field which attracts a lever and changes the switch contacts. The coil current can be on or off so relays have two switch positions and they are double throw (changeover) switches. Relays allow one circuit to switch a second circuit which can be completely separate from the first. For example a low voltage battery circuit can use a relay to switch a 230V AC mains circuit. There is no electrical connection inside the relay between the two circuits; the link is magnetic and mechanical. The coil of a relay passes a relatively large current, typically 30mA for a 12V relay, but it can be as much as 100mA for relays designed to operate from lower voltages. Most ICs (chips) cannot provide this current and a transistor is usually used to amplify the small IC current to the larger value required for the relay coil. The maximum output current for the popular 555 timer IC is 200mA so these devices can supply relay coils directly without amplification.

Relays are usually SPDT or DPDT but they can have many more sets of switch contacts, for example relays with 4 sets of changeover contacts are readily available. Most relays are designed for PCB mounting but you can solder wires directly to the pins providing you take care to avoid melting the plastic case of the relay. The animated picture shows a working relay with its coil and switch contacts. A lever is on the left being attracted by magnetism when the coil is switched on. This lever moves the switch contacts. There is one set of contacts (SPDT) in the foreground and another behind them, making the relay DPDT.

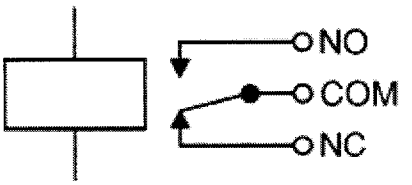


FIGURE 5.1

The relay's switch connections are usually labeled COM, NC and NO:

- **COM** = Common, always connect to this, it is the moving part of the switch.
- **NC** = Normally Closed, COM is connected to this when the relay coil is **off**.
- **NO** = Normally Open, COM is connected to this when the relay coil is **on**.

5.1 Circuit Diagram:

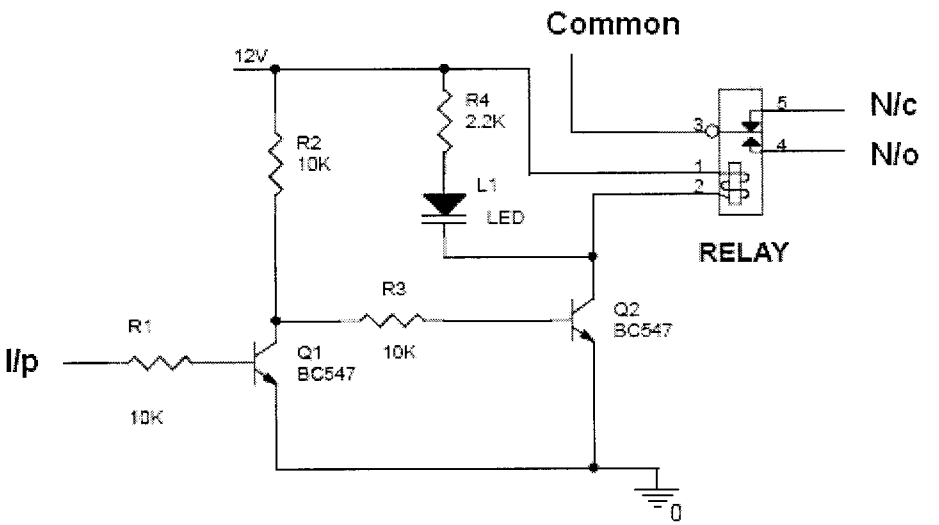


FIGURE 5.2

5.2 Circuit description:

This circuit is designed to control the load. The load may be motor or any other load. The load is turned ON and OFF through relay. The relay ON and OFF

is controlled by the pair of switching transistors (BC 547). The relay is connected in the Q2 transistor collector terminal. A Relay is nothing but electromagnetic switching device which consists of three pins. They are Common, Normally close (NC) and Normally open (NO).

The relay common pin is connected to supply voltage. The normally open (NO) pin connected to load. When high pulse signal is given to base of the Q1 transistors, the transistor is conducting and shorts the collector and emitter terminal and zero signals is given to base of the Q2 transistor. So the relay is turned OFF state.

When low pulse is given to base of transistor Q1 transistor, the transistor is turned OFF. Now 12v is given to base of Q2 transistor so the transistor is conducting and relay is turned ON. Hence the common terminal and NO terminal of relay are shorted. Now load gets the supply voltage through relay.

Voltage signal from microcontroller or PC	Transistor Q1	Transistor Q2	Relay
1	on	off	off
0	off	on	on

TABLE 5.1

6. RFID SYSTEM:

6.1 Introduction:

Radio Frequency Identification has become a hot topic around the world. RFID system delivers what bar codes cannot: real time information on the precise location and status of goods in a process flow. It does it through wireless transfer of data between the RFID reader and the RFID tags. The purpose of RFID system is to enable data to be transmitted by a portable device called a tag, which is read by an RFID reader and processed according to the needs of a particular application.

The read/write capability of an active RFID system is also a significant advantage in interactive applications such as work-in-process or maintenance tracking. Though it is a costlier technology (compared with barcode), RFID has become indispensable for a wide range of automated data collection and identification applications that would not be possible otherwise. Their frequency ranges also distinguish RFID systems. Low-frequency (30 KHz to 500 KHz) systems have short reading ranges and lower system costs. They are most commonly used in security access, asset tracking, and animal identification applications. High-frequency (850 MHz to 950 MHz and 2.4 GHz to 2.5 GHz) systems, offering long read ranges (greater than 90 feet) and high reading speeds, are used for such applications as railroad car tracking and automated toll collection.

The significant advantage of all types of RFID systems is the non-contact, non-line-of-sight nature of the technology. The tag is energized by a time-varying electromagnetic radio frequency (RF) wave that is transmitted by the reader. This RF signal is called a carrier signal. When the RF field passes through an antenna coil, there is an AC voltage generated across the coil. This voltage is rectified to supply power to the tag.

The information stored in the tag is transmitted back to the reader. This is often called backscattering. By detecting the backscattering signal, the information stored in the tag can be fully identified.

6.2 Passive Tag and Reader:

Passive tags are those energized by the reader itself, they contain no power source, typically have very long lifetimes (near indefinite) a drawback over active tags is the read range, typically 2cm (1in) to 1.5m (4.5 ft), a strong positive is individual tag cost. RFID Passive tag is composed of a integrated electronic chip and a antenna coil that includes basic modulation circuitry and non-volatile memory. For most general applications passive tags are usually the most cost effective. These are made in a wide variety of sizes and materials: there are durable plastic tags for discouraging retail theft, wafer thin tags for use within "smart" paper labels, tiny tracking tags which are inserted beneath an animal's skin and credit card sized tags for access control. In most cases the amount of data storage on a passive tag is fairly limited - capacity often being measured in bits as opposed to bytes.

However for most applications only a relatively small amount of data usually needs to be codified and stored on the tag, so the limited capacity does not normally pose a major limitation. Most tags also carry an unalterable unique electronic serial number, which makes RFID tags potentially very useful in applications where item tracking is needed or where security aspects are important.

The reader powers the tag (transponder), by emitting a radio frequency wave. The tag then responds by modulating the energizing field. This modulation can be decoded to yield the tags unique code, inherent in the tag. The resultant data can be the passed to a computer from processing. Tags have various salient

features apart from their physical size: Other available features are: Read Only, Read Write, Anti-Collision.

1. Reader module has to be mounted on non-metallic surface, else it may affect the operation of reader.
2. Buzzer & LED are Active low signals.
3. For Buzzer & LED current limiting Resister has to be mounted. MAX current is 20mA.(470 or 510 ohms for LED and 240 or 270 Ohms for Buzzer)
4. LED's Anode and Buzzer's Positive marked pin to be connected to Vcc.
5. Antenna Inductance should be about 1 mH. The same needs tuning at Factory.

6.3 Pin Diagram:

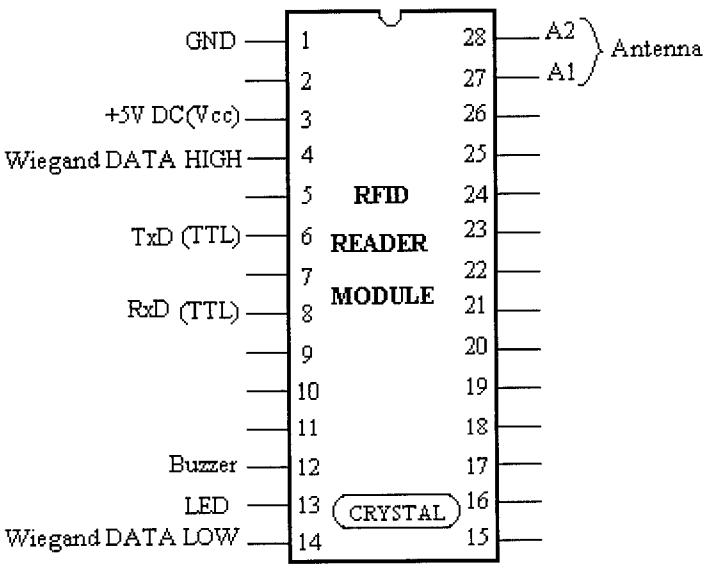


FIGURE 6.1

6.4 Pin description of RFID 125 Reader Module:

PIN NO.	*SIGNAL*	DESCRIPTION
Pin No : 6	TxD	Transmit data (TTL level) output from module to serial interface
Pin No : 4	Wiegand DATA HIGH (available in Wiegand)	It will give DATA HIGH signal.
Pin No : 8	RxD	Receive data (TTL level) input to the module from serial interface
Pin No : 12	Buzzer (active low)	Buzzer will buzz for 280 ms when tag is detected
Pin No : 13	LED (active low)	LED will glow for 280 ms when tag is detected
Pin No : 14	Wiegand DATA LOW (available in Wiegand)	It will give DATA LOW signal.
Pin No:27,28	Antenna Input	Loop Antenna should be connected.

TABLE 6.1

6.5 DEFINITIONS:

6.5.1 Reader:

Usually a microcontroller-based unit with a wound output coil, peak detector hardware, comparators, and firmware designed to transmit energy to a tag and read information back from it by detecting the backscatter modulation.

6.5.2 Tag:

An RFID device incorporating a silicon memory chip (usually with on-board rectification bridge and other RF front-end devices), a wound or printed input/output coil, and (at lower frequencies) a tuning capacitor.

6.5.3 Carrier:

A Radio Frequency (RF) sine wave generated by the reader to transmit energy to the tag and retrieve data from the tag. In these examples the ISO frequencies of 125 kHz and 13.56 MHz are assumed; higher frequencies are used for RFID tagging but the communication methods are somewhat different. 2.45 GHz, for example, uses a true RF link. 125 kHz and 13.56 MHz, utilize transformer-type electromagnetic coupling.

6.6 Modulation:

Periodic fluctuations in the amplitude of the carrier, used to transmit data back from the tag to the reader. Systems incorporating passive RFID tags operate in ways that may seem unusual to anyone who already understands RF or microwave systems. There is only one transmitter – the passive tag is not a transmitter or

transponder in the purest definition of the term, yet bidirectional communication is taking place. The RF field generated by a tag reader (the energy transmitter) has three purposes:

1. Induce enough power into the tag coil to energize the tag.

Passive tags have no battery or other power source; they must derive all power for operation from the reader field. 125 kHz and 13.56 MHz tag designs must operate over a vast dynamic range of carrier input, from the very near field (in the range of 200 VPP) to the maximum read distance (in the range of 5 VPP).

2. Provide a synchronized clock source to the tag.

Most RFID tags divide the carrier frequency down to generate an on-board clock for state machines, counters, etc., and to derive the data transmission bit rate for data returned to the reader. Some tags, however, employ on-board oscillators for clock generation.

3. Act as a carrier for return data from the tag.

Backscatter modulation requires the reader to peak-detect the tag's modulation of the reader's own carrier. See Section for additional information on backscatter modulation.

6.7 SYSTEM HANDSHAKE:

Typical handshake of a tag and reader is as follows:

1. The reader continuously generates an RF carrier sine wave, watching always for modulation to occur. Detected modulation of the field would indicate the presence of a tag.

2. A tag enters the RF field generated by the reader. Once the tag has received sufficient energy to operate correctly, it divides down the carrier and begins clocking its data to an output transistor, which is normally connected across the coil inputs.
3. The tag's output transistor shunts the coil, sequentially corresponding to the data which is being clocked out of the memory array.
4. Shunting the coil causes a momentary fluctuation (dampening) of the carrier wave, which is seen as a slight change in amplitude of the carrier.
5. The reader peak-detects the amplitude-modulated data and processes the resulting bit stream according to the encoding and data modulation methods used.

6.8 BACKSCATTER MODULATION:

This terminology refers to the communication method used by a passive RFID tag to send data back to the reader. By repeatedly shunting the tag coil through a transistor, the tag can cause slight fluctuations in the reader's RF carrier amplitude. The RF link behaves essentially as a transformer; as the secondary winding (tag coil) is momentarily shunted, the primary winding (reader coil) experiences a momentary voltage drop. The reader must peak-detect this data at about 60 dB down (about 100 mV riding on a 100V sine wave) as shown in Figure 1. This amplitude-modulation loading of the reader's transmitted field provides a communication path back to the reader. The data bits can then be encoded or further modulated in a number of ways

6.9 DATA ENCODING:

Data encoding refers to processing or altering the data bitstream in-between the time it is retrieved from the RFID chip's data array and its transmission back to the reader. Entire textbooks are written on the subject, but there are several popular methods used in RFID tagging today:

1. **NRZ (Non-Return to Zero) Direct:**

In this method no data encoding is done at all; the 1's and 0's are clocked from the data array directly to the output transistor. A low in the peak-detected modulation is a '0' and a high is a '1'.

2. **Differential Biphase:**

Several different forms of differential biphase are used, but in general the bitstream being clocked out of the data array is modified so that a transition always occurs on every clock edge, and 1's and 0's are distinguished by the transitions within the middle of the clock period. This method is used to embed clocking information to help synchronize the reader to the bitstream; and because it always has a transition at a clock edge, it inherently provides some error correction capability. Any clock edge that does not contain a transition in the data stream is in error and can be used to reconstruct the data.

3. **Biphase_L (Manchester):**

This is a variation of biphase encoding, in which there is not always a transition at the clock edge.

6.10 DATA MODULATION:

Although all the data is transferred to the host by amplitude-modulating the carrier (backscatter modulation), the actual modulation of 1's and 0's is accomplished with three additional modulation methods:

1. **Direct Modulation:**

In direct modulation, the Amplitude Modulation of the backscatter approach is the only modulation used. A high in the envelope is a '1' and a low is a '0'. Direct modulation can provide a high data rate but low noise immunity.

2. **FSK (Frequency Shift Keying):**

This form of modulation uses two different frequencies for data transfer; the most common FSK mode is Fc/8/10. In other words, a '0' is transmitted as an amplitude-modulated clock cycle with period corresponding to the carrier frequency divided by 8, and a '1' is transmitted as an amplitude-modulated clock cycle period corresponding to the carrier frequency divided by 10. The amplitude modulation of the carrier thus switches from Fc/8 to Fc/10 corresponding to 0's and 1's in the bit stream, and the reader has only to count cycles between the peak-detected clock edges to decode the data. FSK allows for a simple reader design, provides very strong noise immunity, but suffers from a lower data rate than some other forms of data modulation. FSK data modulation is used with NRZ encoding.

3. **PSK (Phase Shift Keying):**

This method of data modulation is similar to FSK, except only one frequency is used, and the shift between 1's and 0's is accomplished by shifting the phase of the backscatter clock by 180 degrees.

Two common types of PSK are:

- Change phase at any '0', or
- Change phase at any data change (0 to 1 or 1 to 0).

PSK provides fairly good noise immunity, a moderately simple reader design, and a faster data rate than FSK. Typical applications utilize a backscatter clock of Fc/2.

6.11 ANTICOLLISION:

In many existing applications, a single-read RFID tag is sufficient and even necessary: animal tagging and access control are examples. However, in a growing number of new applications, the simultaneous reading of several tags in the same RF field is absolutely critical: library books, airline baggage, garment, and retail applications are a few. In order to read multiple tags simultaneously, the tag and reader must be designed to detect the condition that more than one tag is active. This is referred to as a collision. No data would be transferred to the reader. The tag/reader interface is similar to a serial bus, even though the "bus" travels through the air. In a wired serial bus application, arbitration is necessary to prevent bus contention. The RFID interface also requires arbitration so that only one tag transmits data over the "bus" at one time. A number of different methods are in use and in development today for preventing collisions; most are patented or patent pending, but all are related to making sure that only one tag "talks" (backscatters) at any one time.

6.12 CONFIGURATION OF ANTENNA COILS:

6.12.1 Tag Antenna Coil:

An antenna coil for an RFID tag can be configured in many different ways, depending on the purpose of the application and the dimensional constraints. A typical inductance *L* for the tag coil is a few (mH) for 125 kHz devices. The coil is typically made of a thin wire. The inductance and the number of turns of the coil can be calculated by the formulas given in the previous section. An Inductance Meter is often used to measure the inductance of the coil. A typical number of turns of the coil is in the range of 100 turns for 125 kHz and 3~5 turns for 13.56 MHz devices. For a longer read range, the antenna coil must be tuned properly to the frequency of interest (i.e., 125 kHz). Voltage drop across the coil is maximized by forming a parallel resonant circuit. The tuning is accomplished with a resonant capacitor that is connected in parallel to the coil. The formula for the resonant capacitor value is given as

$$C=1/(2\pi f)^2 L \ ;$$

$$L=0.31(aN)^2 / 6a+9h+10b \ ;$$

where

a = average radius of the coil in cm
b = winding thickness in cm
N = number of turns
h = winding height in cm

6.12.2 VARIOUS CONFIGURATIONS OF TAG ANTENNA COIL:

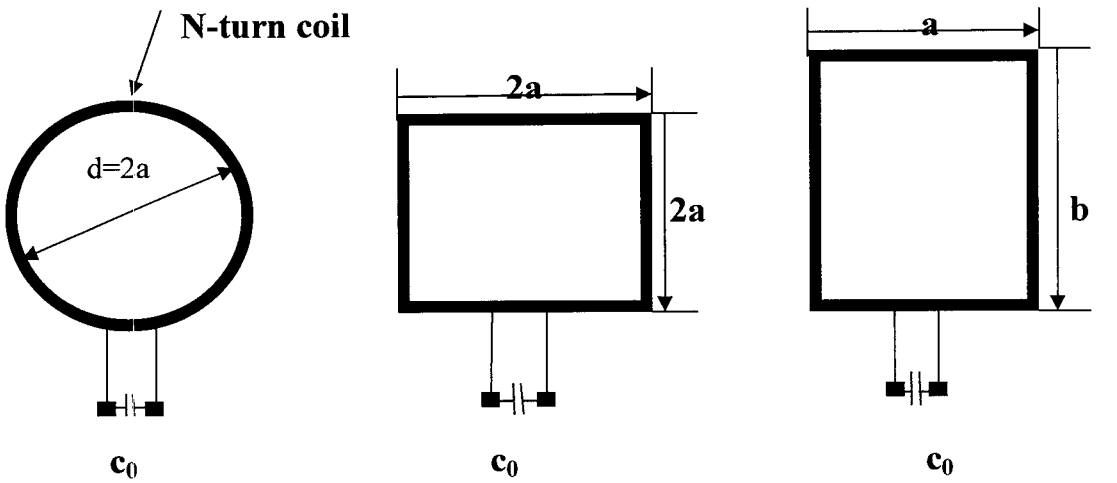


FIGURE 6.2

6.12.3 Reader Antenna Coil:

The inductance for the reader antenna coil is typically in the range of a few hundred to a few thousand micro-Henries (mH) for low frequency applications. The reader antenna can be made of either a single coil that is typically forming a series resonant circuit or a double loop (transformer) antenna coil that forms a parallel resonant circuit. The series resonant circuit results in minimum impedance at the resonance frequency. Therefore, it draws a maximum current at the resonance frequency.

On the other hand, the parallel resonant circuit results in maximum impedance at the resonance frequency. Therefore, the current becomes minimized at the resonance frequency. Since the voltage can be stepped up by forming a double loop (parallel) coil, the parallel resonant circuit is often used for a system where a higher voltage signal is required. The main loop (secondary) is formed

with several turns of wire on a large frame, with a tuning capacitor to resonate it to the resonance frequency (125 kHz). The other loop is called a coupling loop (primary), and it is formed with less than two or three turns of coil. This loop is placed in a very close proximity to the main loop, usually (but not necessarily) on the inside edge and not more than a couple of centimetres away from the main loop.

The purpose of this loop is to couple signals induced from the main loop to the reader (or vise versa) at more reasonable matching impedance. The coupling (primary) loop provides an impedance match to the input/output impedance of the reader. The coil is connected to the input/output signal driver in the reader electronics. The main loop (secondary) must be tuned to resonate at the resonance frequency and is not physically connected to the reader electronics. The coupling loop is usually untuned, but in some designs, a tuning capacitor C2 is placed in series with the coupling loop. Because there are far fewer turns on the coupling loop than the main loop, its inductance is considerably smaller. As a result, the capacitance to resonate is usually much larger.

6.12.4 READ RANGE OF RFID DEVICES:

Read range is defined as a maximum communication distance between the reader and tag. The read range of typical passive RFID products varies from about 1 inch to 1 meter, depending on system configuration. The read range of an RFID device is, in general, affected by the following parameters:

a) Operating frequency and performance of antenna coils
b) Q of antenna and tuning circuit
c) Antenna orientation

d) Excitation current and voltage

e) Sensitivity of receiver

f) Coding (or modulation) and decoding (or demodulation) algorithm

g) Number of data bits and detection (interpretation) algorithm

h) Condition of operating environment (metallic, electrical noise), etc.

7. KEY PAD:

7.1 CIRCUIT DIAGRAM:

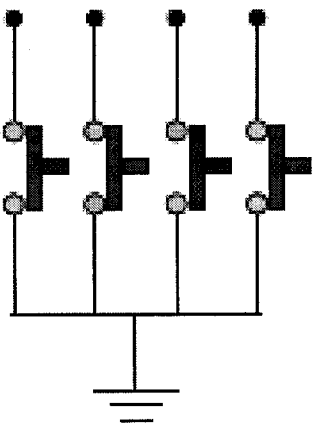


FIGURE7.1

7.2 Description:

A numeric keypad, or numpad for short, is the small, palm-sized, seventeen key section of a computer keyboard, usually on the very far right. The numeric keypad features digits 0 to 9, addition (+), subtraction (-), multiplication (*) and division (/) symbols, a decimal point (.) and Num Lock and Enter keys. Laptop

keyboards often do not have a numpad, but may provide numpad input by holding a modifier key (typically lapelled "Fn") and operating keys on the standard keyboard.

Particularly large laptops (typically those with a 17 inch screen or larger) may have space for a real numpad, and many companies sell separate numpads which connect to the host laptop by a USB connection.

Numeric keypads usually operate in two modes: when Num Lock is off, keys 8, 6, 2, 4 act like an arrow keys and 7, 9, 3, 1 act like Home, PgUp, PgDn and End; when Num Lock is on, digits keys produce corresponding digits. These, however, differ from the numeric keys at the top of the keyboard in that, when combined with the Alt key on a PC, they are used to enter characters which may not be otherwise available: for example, Alt-0169 produces the copyright symbol. These are referred to as Alt codes.

On Apple Computer Macintosh computers, which lack a Num Lock key, the numeric keypad always produces only numbers. The num lock key is replaced by the clear key.

Numeric keypads usually operate in two modes: when Num Lock is off, keys 8, 6, 2, 4 act like an arrow keys and 7, 9, 3, 1 act like Home, PgUp, PgDn and End; when Num Lock is on, digits keys produce corresponding digits. These, however, differ from the numeric keys at the top of the keyboard in that, when combined with the Alt key on a PC, they are used to enter characters which may not be otherwise available: for example, Alt-0169 produces the copyright symbol. These are referred to as Alt codes.

8. PCB DESIGN (Design and Fabrication of Printed circuit boards):

8.1 INTRODUCTION:

Printed circuit boards, or PCBs, form the core of electronic equipment domestic and industrial. Some of the areas where PCBs are intensively used are computers, process control, telecommunications and instrumentation.

8.2 MANUFATCURING:

The manufacturing process consists of two methods; print and etch, and print, plate and etch. The single sided PCBs are usually made using the print and etch method. The double sided plate through – hole (PTH) boards are made by the print plate and etch method.

The production of multi layer boards uses both the methods. The inner layers are printed and etch while the outer layers are produced by print, plate and etch after pressing the inner layers.

8.2.1 SOFTWARE:

The software used in our project to obtain the schematic layout is **MICROSIM.**

8.2.2 PANELISATION:

Here the schematic transformed in to the working positive/negative films. The circuit is repeated conveniently to accommodate economically as many circuits as possible in a panel, which can be operated in every sequence of subsequent steps in the PCB process. This is called panelisation. For the PTH boards, the next operation is drilling.

8.2.3 DRILLING:

PCB drilling is a state of the art operation. Very small holes are drilled with high speed CNC drilling machines, giving a wall finish with less or no smear or epoxy, required for void free through hole plating.

8.2.4 PLATING:

It is the heart of the PCB manufacturing process. The holes drilled in the board are treated both mechanically and chemically before depositing the copper by the electro less copper platting process.

8.2.5 ETCHING:

Once a multiplayer board is drilled and electro less copper deposited, the image available in the form of a film is transferred on to the out side by photo printing using a dry film printing process. The boards are then electrolyticaly plated on to the circuit pattern with copper and tin. The tin-plated deposit serves an etch resist when copper in the unwanted area is removed by the conveyorised spray etching machines with chemical etchants. The etching machines are attached to an automatic dosing equipment, which analyses and controls etchants concentrations.

8.2.6 SOLDER MASK:

Since a PCB design may call for very close spacing between conductors, a solder mask has to be applied on the both sides of the circuitry to avoid the bridging of conductors. The solder mask ink is applied by screening. The ink is dried, exposed to UV, developed in a mild alkaline solution and finally cured by both UV and thermal energy.

8.2.7 HOT AIR LEVELLING:

After applying the solder mask, the circuit pads are soldered using the hot air leveling process. The bare bodies fluxed and dipped in to a molten solder bath. While removing the board from the solder bath, hot air is blown on both sides of the board through air knives in the machines, leaving the board soldered and leveled. This is one of the common finishes given to the boards. Thus the double sided plated through whole printed circuit board is manufactured and is now ready for the components to be soldered.

CONCLUSION

All the modules were individually constructed and then integrated successfully. For demonstration purposes a pre defined square path is set up. Object sensor can help much in obstacle free navigation. This indoor propagation model can be very useful in large areas like airports, educational institutions, large industries, multiplexes etc.

FUTURE POSSIBILITIES

The project can be further refined and brought out commercially. Industries can use them according to their infrastructures. Object sensor can be made with ULTRASONIC rays so that object detection range can be larger.

An emergency alarm can be set up if the kit has some problem with navigation. A voice recognition system can be used to get input from the user.

The kit can be refined and made so compact. It can be made to move at a speed of 0.7 m/s which is the normal walking speed, which would be very helpful for the visually impaired population to navigate.

eatures

- Compatible with MCS-51™ Products
- 4K Bytes of In-System Reprogrammable Flash Memory
  - Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-Level Program Memory Lock
- 128 x 8-Bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low Power Idle and Power Down Modes

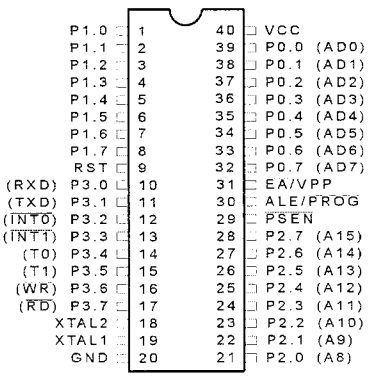
escription

he AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K ytes of Flash Programmable and Erasable Read Only Memory (PEROM). The evice is manufactured using Atmel's high density nonvolatile memory technology nd is compatible with the industry standard MCS-51™ instruction set and pinout. The n-chip Flash allows the program memory to be reprogrammed in-system or by a conentional nonvolatile memory programmer. By combining a versatile 8-bit CPU with ash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which ovides a highly flexible and cost effective solution to many embedded control applitions.

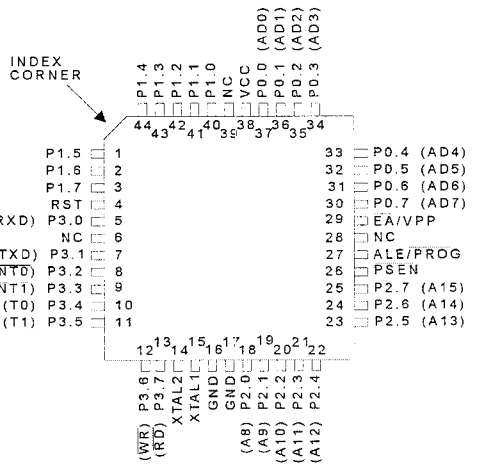
(continued)

in Configurations

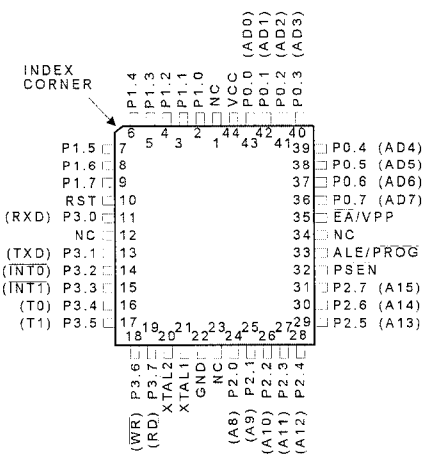
PDIP



PQFP/TQFP



PLCC

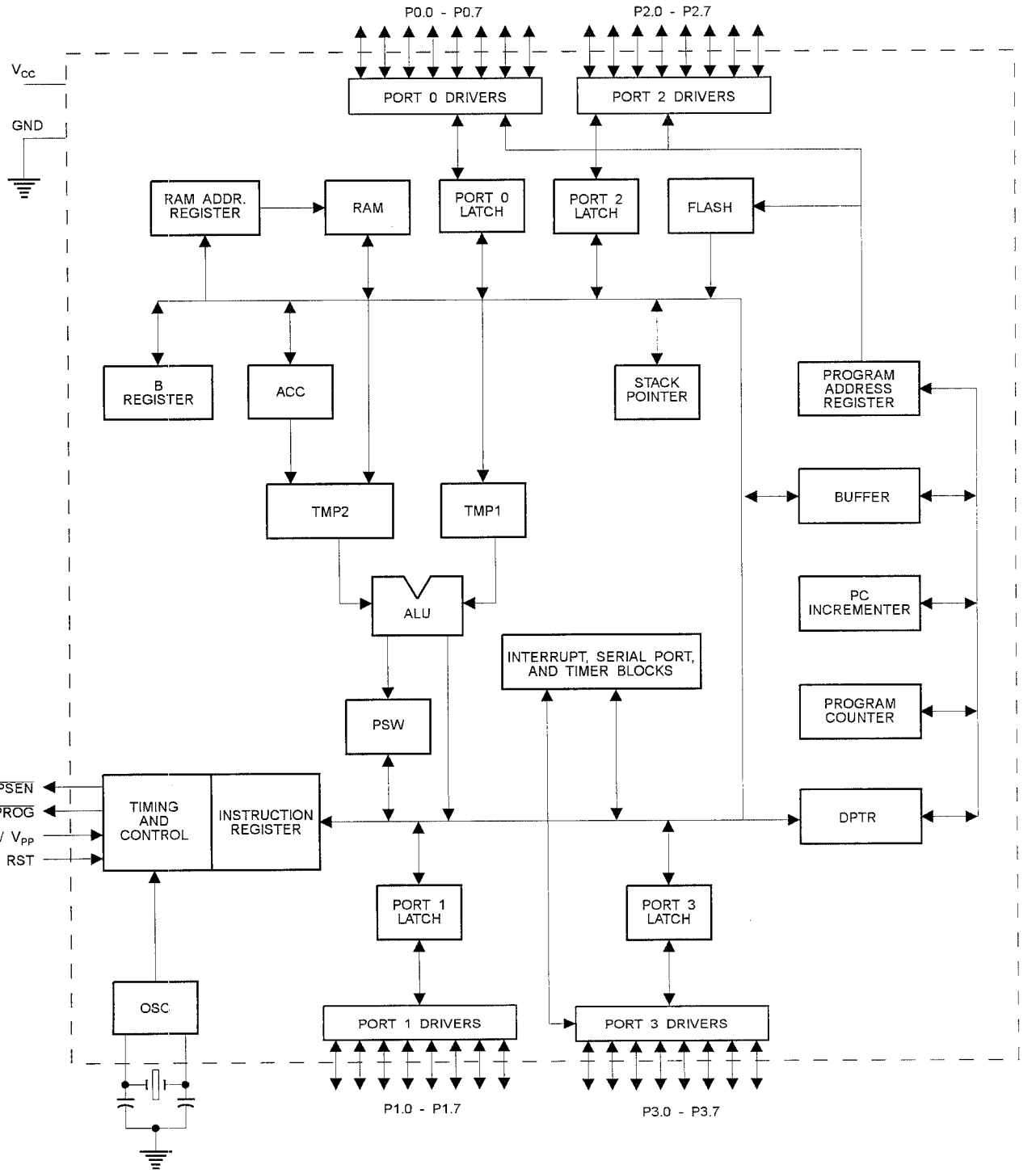


8-Bit Microcontroller with 4K Bytes Flash

AT89C51

0265F-A–12/97

ck Diagram


P0.0 - P0.7
P2.0 - P2.7
V_{CC}
GND
PORT 0 DRIVERS
PORT 2 DRIVERS
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
BUFFER
TMP2
TMP1
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PROGRAM COUNTER
PSW
PSEN
ALE/PROG
EA / V_{PP}
RST
TIMING AND CONTROL
INSTRUCTION REGISTER
DPTR
PORT 1 LATCH
PORT 3 LATCH
OSC
PORT 1 DRIVERS
PORT 3 DRIVERS
P1.0 - P1.7
P3.0 - P3.7

he AT89C51 provides the following standard features: 4K tes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit ner/counters, a five vector two-level interrupt architecture, full duplex serial port, on-chip oscillator and clock cir- itry. In addition, the AT89C51 is designed with static logic r operation down to zero frequency and supports two ftware selectable power saving modes. The Idle Mode ops the CPU while allowing the RAM, timer/counters, rial port and interrupt system to continue functioning. The ower Down Mode saves the RAM contents but freezes e oscillator disabling all other chip functions until the next rdware reset.

in Description

cc
upply voltage.

ND
round.

ort 0
ort 0 is an 8-bit open drain bidirectional I/O port. As an tput port each pin can sink eight TTL inputs. When 1s e written to port 0 pins, the pins can be used as high- pedance inputs.

ort 0 may also be configured to be the multiplexed low- der address/data bus during accesses to external pro- am and data memory. In this mode P0 has internal pul- os.

ort 0 also receives the code bytes during Flash program- ng, and outputs the code bytes during program verifica- n. External pullups are required during program verifica- n.

ort 1
ort 1 is an 8-bit bidirectional I/O port with internal pullups. he Port 1 output buffers can sink/source four TTL inputs. hen 1s are written to Port 1 pins they are pulled high by e internal pullups and can be used as inputs. As inputs, ort 1 pins that are externally being pulled low will source rrent (I_{IL}) because of the internal pullups.

ort 1 also receives the low-order address bytes during ash programming and verification.

ort 2
ort 2 is an 8-bit bidirectional I/O port with internal pullups. he Port 2 output buffers can sink/source four TTL inputs. hen 1s are written to Port 2 pins they are pulled high by e internal pullups and can be used as inputs. As inputs, ort 2 pins that are externally being pulled low will source rrent (I_{IL}) because of the internal pullups.

ort 2 emits the high-order address byte during fetches om external program memory and during accesses to ternal data memory that use 16-bit addresses (MOVX @ PTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3
Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and verification.

RST
Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$
Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$
Program Store Enable is the read strobe to external program memory.

When the AT89C51 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

EA/V_{PP}

External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset.

EA should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming, for parts that require 12-volt V_{PP}.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

Oscillator Characteristics

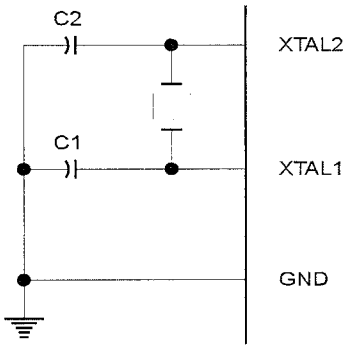
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

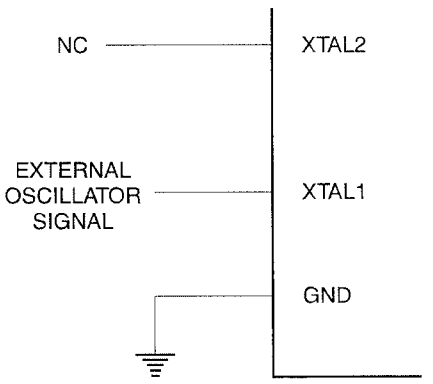
It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Figure 1. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 2. External Clock Drive Configuration



Status of External Pins During Idle and Power Down Modes

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

ower Down Mode

the power down mode the oscillator is stopped, and the struction that invokes power down is the last instruction ecuted. The on-chip RAM and Special Function Regis-rs retain their values until the power down mode is termi-ted. The only exit from power down is a hardware reset. eset redefines the SFRs but does not change the on-chip AM. The reset should not be activated before V_{CC} is stored to its normal operating level and must be held tive long enough to allow the oscillator to restart and sta-ize.

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below:

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

ock Bit Protection Modes

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash is disabled.
3	P	P	U	Same as mode 2, also verify is disabled.
4	P	P	P	Same as mode 3, also external execution is disabled.

rogramming the Flash

he AT89C51 is normally shipped with the on-chip Flash emory array in the erased state (that is, contents = FFH) d ready to be programmed. The programming interface ccepts either a high-voltage (12-volt) or a low-voltage $_{CC}$) program enable signal. The low voltage program-ing mode provides a convenient way to program the T89C51 inside the user's system, while the high-voltage ogramming mode is compatible with conventional third rty Flash or EPROM programmers.

he AT89C51 is shipped with either the high-voltage or w-voltage programming mode enabled. The respective p-side marking and device signature codes are listed in e following table.

	V_{PP} = 12V	V_{PP} = 5V
Top-Side Mark	AT89C51 xxxx yyww	AT89C51 xxxx-5 yyww
Signature	(030H)=1EH (031H)=51H (032H)=FFH	(030H)=1EH (031H)=51H (032H)=05H

he AT89C51 code memory array is programmed byte-by-te in either programming mode. *To program any non-ank byte in the on-chip Flash Memory, the entire memory ust be erased using the Chip Erase Mode.*

Programming Algorithm: Before programming the AT89C51, the address, data and control signals should be set up according to the Flash programming mode table and Figures 3 and 4. To program the AT89C51, take the following steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V for the high-voltage programming mode.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89C51 features $\overline{Data}$ Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

rogram Verify: If lock bits LB1 and LB2 have not been ogrammed, the programmed code data can be read back a the address and data lines for verification. The lock bits annot be verified directly. Verification of the lock bits is chieved by observing that their features are enabled.

hip Erase: The entire Flash array is erased electrically y using the proper combination of control signals and by olding ALE/$\overline{PROG}$ low for 10 ms. The code array is written ith all "1"s. The chip erase operation must be executed efore the code memory can be re-programmed.

eading the Signature Bytes: The signature bytes are ead by the same procedure as a normal verification of cations 030H,

31H, and 032H, except that P3.6 and P3.7 must be pulled a logic low. The values returned are as follows.

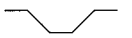
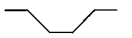
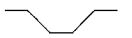
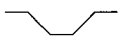
(030H) = 1EH indicates manufactured by Atmel
(031H) = 51H indicates 89C51
(032H) = FFH indicates 12V programming
(032H) = 05H indicates 5V programming

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Flash Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.6	P3.7
Write Code Data		H	L		H/12V	L	H	H	H
Read Code Data		H	L	H	H	L	L	H	H
Write Lock	Bit - 1	H	L		H/12V	H	H	H	H
	Bit - 2	H	L		H/12V	H	H	L	L
	Bit - 3	H	L		H/12V	H	L	H	L
Chip Erase		H	L	 (1)	H/12V	H	L	L	L
Read Signature Byte		H	L	H	H	L	L	L	L

ote: 1. Chip Erase requires a 10-ms PROG pulse.

gure 3. Programming the Flash

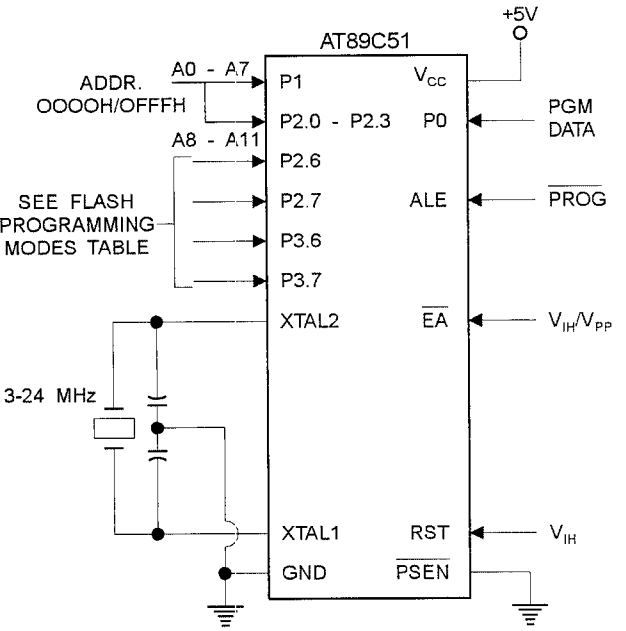
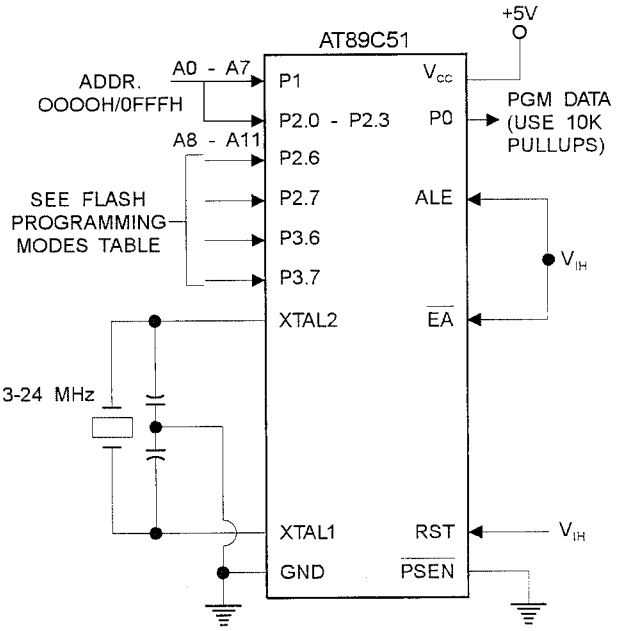


Figure 4. Verifying the Flash



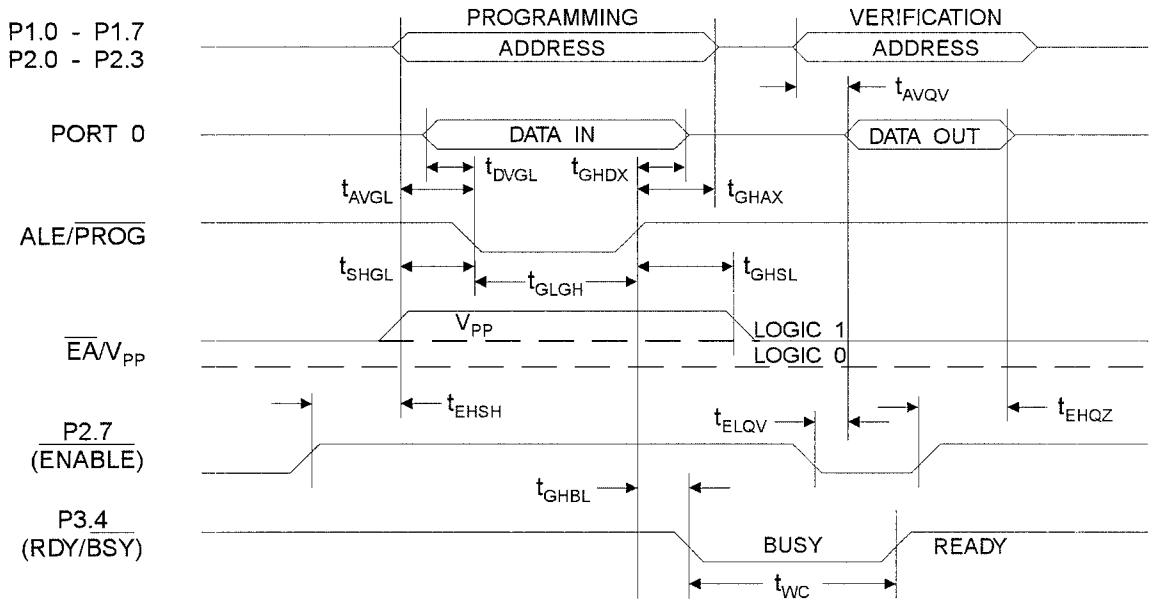
Flash Programming and Verification Characteristics

T_A = 0°C to 70°C, V_{CC} = 5.0 ± 10%

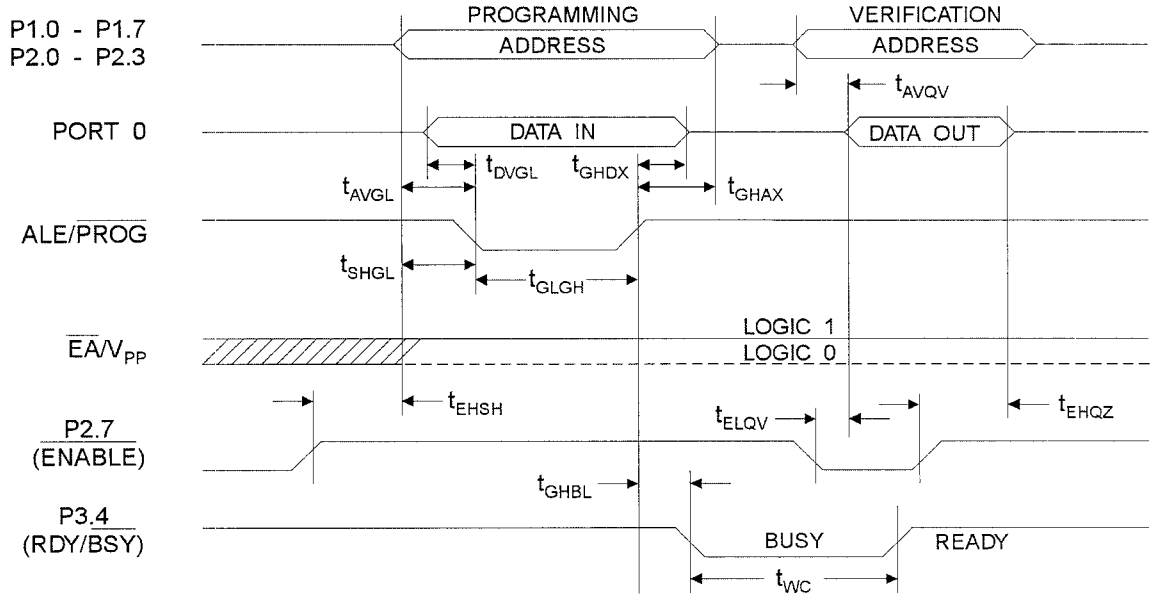
Symbol	Parameter	Min	Max	Units
V_{PP}(1)	Programming Enable Voltage	11.5	12.5	V
I_{PP}(1)	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	3	24	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GHSL}(1)	V_{PP} Hold After $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ Width	1	110	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		2.0	ms

lote: 1. Only used in 12-volt programming mode.

Flash Programming and Verification Waveforms - High Voltage Mode (V_{PP} = 12V)



Flash Programming and Verification Waveforms - Low Voltage Mode (V_{PP} = 5V)



Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 5.0V ± 20% (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage(1) (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low Voltage(1) (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, VCC = 5V ± 10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		20	mA
		Idle Mode, 12 MHz		5	mA
	Power Down Mode(2)	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port: Port 0: 26 mA
Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum V_{CC} for Power Down is 2V.

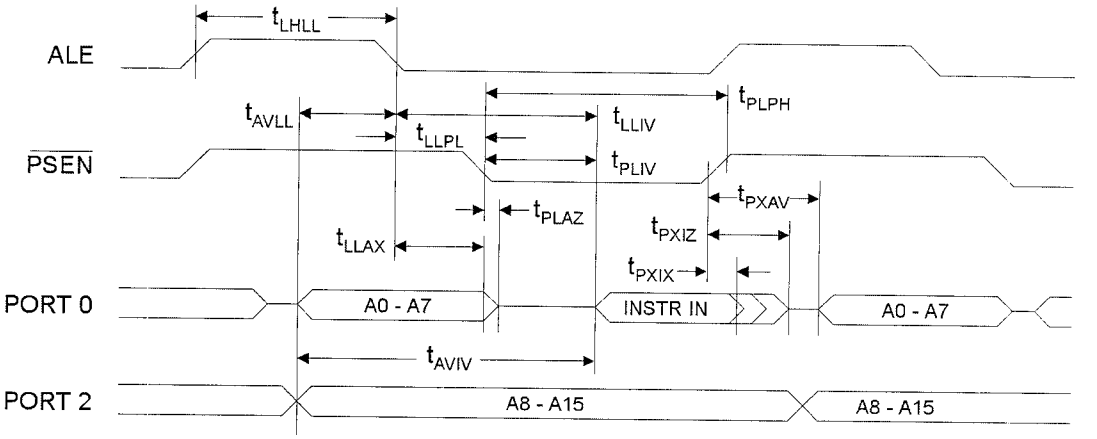
AC Characteristics

(Under Operating Conditions; Load Capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; Load Capacitance for all other outputs = 80 pF)

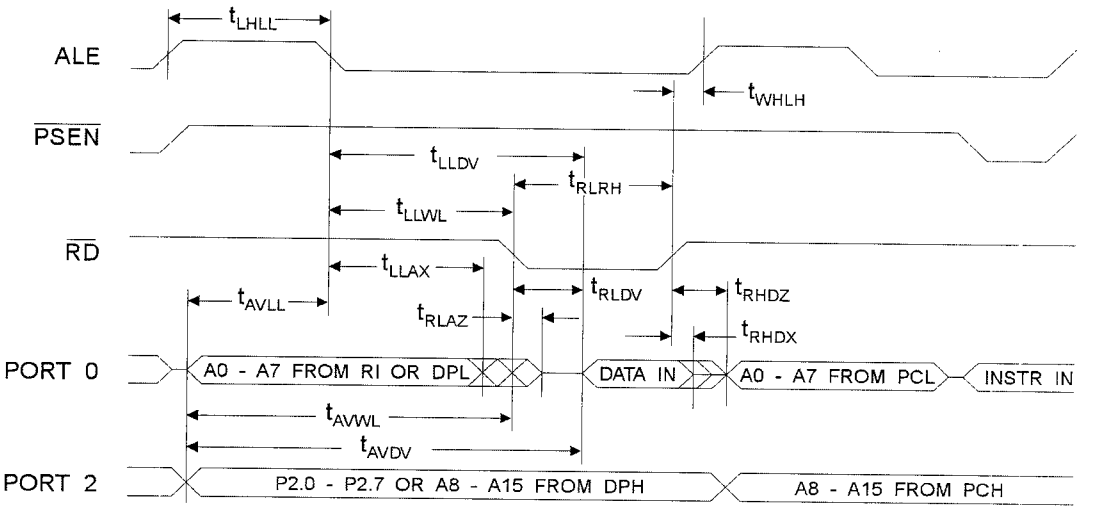
External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		16 to 24 MHz Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	24	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	43		t_{CLCL}-13		ns
t_{LLAX}	Address Hold After ALE Low	48		t_{CLCL}-20		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-13		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-20		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-45	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-10	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CLCL}$-55	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-20		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-120		ns
t_{WHQX}	Data Hold After $\overline{WR}$	33		t_{CLCL}-20		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-20	t_{CLCL}+25	ns

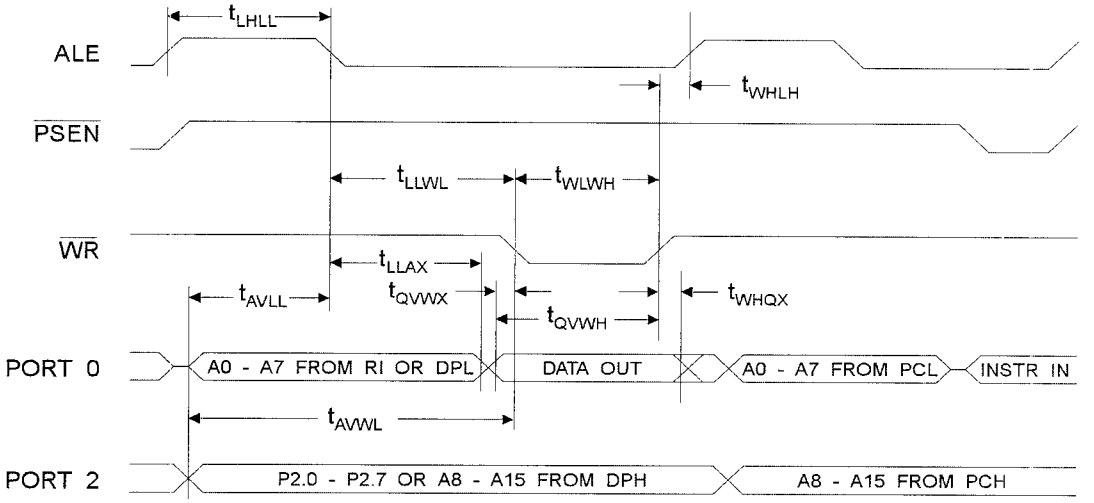
External Program Memory Read Cycle



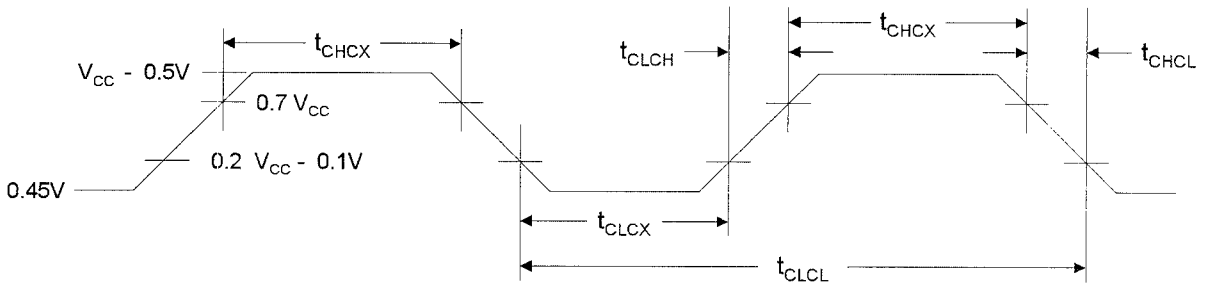
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

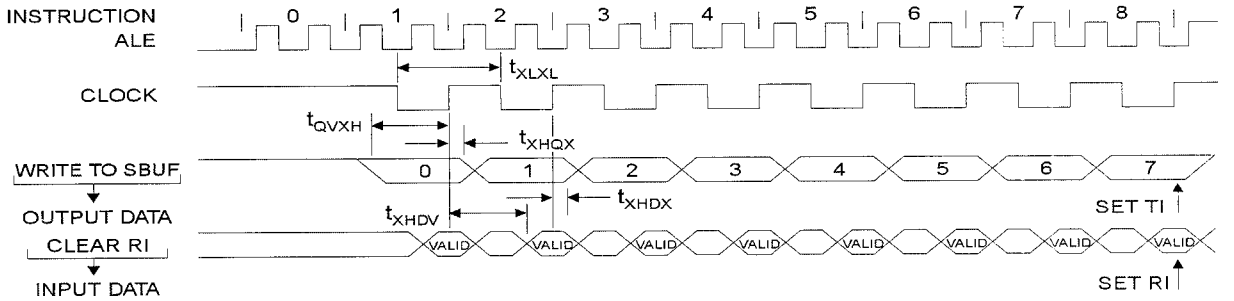
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	15		ns
t_{CLCX}	Low Time	15		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

Serial Port Timing: Shift Register Mode Test Conditions

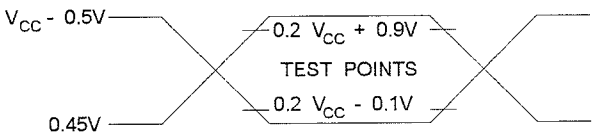
(V_{CC} = 5.0 V ± 20%; Load Capacitance = 80 pF)

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-117		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

Shift Register Mode Timing Waveforms

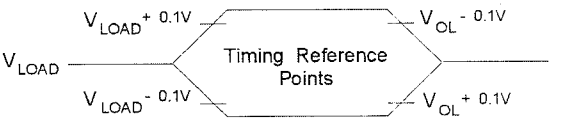


AC Testing Input/Output Waveforms[1]



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms[1]



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
12	5V ± 20%	AT89C51-12AC	44A	Commercial
		AT89C51-12JC	44J	(0°C to 70°C)
		AT89C51-12PC	40P6	
		AT89C51-12QC	44Q	
		AT89C51-12AI	44A	Industrial
		AT89C51-12JI	44J	(-40°C to 85°C)
		AT89C51-12PI	40P6	
		AT89C51-12QI	44Q	
		AT89C51-12AA	44A	Automotive
		AT89C51-12JA	44J	(-40°C to 105°C)
		AT89C51-12PA	40P6	
		AT89C51-12QA	44Q	
16	5V ± 20%	AT89C51-16AC	44A	Commercial
		AT89C51-16JC	44J	(0°C to 70°C)
		AT89C51-16PC	40P6	
		AT89C51-16QC	44Q	
		AT89C51-16AI	44A	Industrial
		AT89C51-16JI	44J	(-40°C to 85°C)
		AT89C51-16PI	40P6	
		AT89C51-16QI	44Q	
		AT89C51-16AA	44A	Automotive
		AT89C51-16JA	44J	(-40°C to 105°C)
		AT89C51-16PA	40P6	
		AT89C51-16QA	44Q	
20	5V ± 20%	AT89C51-20AC	44A	Commercial
		AT89C51-20JC	44J	(0°C to 70°C)
		AT89C51-20PC	40P6	
		AT89C51-20QC	44Q	
		AT89C51-20AI	44A	Industrial
		AT89C51-20JI	44J	(-40°C to 85°C)
		AT89C51-20PI	40P6	
		AT89C51-20QI	44Q	

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	5V ± 20%	AT89C51-24AC	44A	Commercial
		AT89C51-24JC	44J	(0°C to 70°C)
		AT89C51-24PC	44P6	
		AT89C51-24QC	44Q	
		AT89C51-24AI	44A	Industrial
		AT89C51-24JI	44J	(-40°C to 85°C)
		AT89C51-24PI	44P6	
		AT89C51-24QI	44Q	

Package Type	
44A	44 Lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44Q	44 Lead, Plastic Gull Wing Quad Flatpack (PQFP)

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