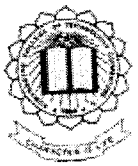

AIRCRAFT COLLISION AVOIDANCE USING GPS

A Project Report

Submitted by

J.ARCHANA	-	**71204106002**
B.DIVYA	-	**71204106011**
JAYALAXMI NAGARAJAN	-	**71204106017**
B.AKILA	-	**71204106700**

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COIMBATORE – 641006

ANNA UNIVERSITY : CHENNAI 600 025

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ANNA UNIVERSITY: CHENNAI 600 025

BONAFIDE CERTIFICATE

Certified that this project report **"AIRCRAFT COLLISION AVOIDANCE USING GPS "** is the bonafide work of **" J.ARCHANA, B.DIVYA, JAYALAXMI NAGARAJAN, B.AKILA " who carried** out the project work under my supervision.

SIGNATURE

(Dr.Rajeswari Mariappan)

HEAD OF THE DEPARTMENT

Electronics & Communication Engineering
Kumaraguru College of Technology
Coimbatore – 641006

SIGNATURE

(Mrs.D.Mohana Geetha)

SUPERVISOR

Senior Lecturer
Electronics &Communication Engineering
Kumaraguru College of Technology
Coimbatore – 641006

The candidates with University Register Nos. **71204106002, 71204106011, 71204106017, 71204106700** were examined by us in the project viva-voce examination held on 21.4.2008

INTERNAL EXAMINER

EXTERNAL EXAMINER

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Finally we thank **our parents** for giving us moral support and abundant blessing in all our activities. Last but not the least a heartfelt thanks to all the **friends** who helped us in our project work.

ABSTRACT

The idea of our system is to avoid the collision between aircrafts. GPS uses a constellation of 24 satellites in precise orbits approximately 11,000 miles above earth. The GPS satellites sends the navigation message to the GPS antenna. The navigation message contains almanac (it gives information about satellites own orbit), ephimeris (it is downloaded to calculate satellites precise position). The GPS antenna sends this information to the GPS receiver. The output of the GPS receiver is in the NMEA format containing the position (latitude, longitude, altitude) of the aircraft. This information is passed on to the microcontroller and the value is displayed in the LCD which is interfaced with the microcontroller.

The microcontroller is coded to send this information to the mobile and then the PC in the receiver section. The value of another aircraft is manually given in the PC. The PC is coded such that it compares the value received from the transmitter section with the manually entered value. If both the values coincide, an alert message is sent to the mobile and then the microcontroller in the transmitter section.

This project is mainly used for military aircraft as well as domestic aircraft inorder to avoid the aircraft accident. Hence GPS is used to calculate receivers exact location with great fidelity.

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CHAPTER 1

1. OVERVIEW OF THE PROJECT

1.1 INTRODUCTION

This project is to avoid collision between the aircraft's using GPS. Global Positioning System (GPS) is a satellite based navigation system. GPS was originally intended for military applications . Later on, it was made available for civilian use .

Nowadays, the most common mode of communication is through mobile, so the project makes tracking of aircraft easily with the use of two mobiles. One is interfaced with the GPS kit , which is present with the aircraft to be traced and other is in the receiver section interfaced with PC.

The location of the aircraft in terms of latitude, longitude & altitude is transmitted as a single Short Message Service (SMS) from the transmitter section mobile interfaced with the GPS kit to the mobile in the receiver section at regular intervals automatically. Already another aircrafts value will be available in the PC. These two values will be compared as per the coding in PC and if they are equal, an alert message will be sent to the mobile and microcontroller in transmitter section.

1.2 BLOCK DIAGRAM DESCRIPTION

The figure 1.1 is explained as follows.The GPS kit is a hand carried kit.The front end of the GPS kit consists of a GPS antenna which is a patch antenna (also called as microstrip antenna) and is used to receive signals

from the GPS satellites. The satellites transmit signals that can be detected with a GPS receiver. GPS receiver processes the received signal and sends it to the microcontroller unit by means of a serial interface (RS232).

The advantage of the microcontroller unit is that two interface is possible. The other serial interface is to the mobile in the GPS kit.

The information (latitude, longitude, altitude, date and time) obtained from the GPS satellites can be seen through the LCD display of the GPS kit. These information are transmitted as SMS using the mobile in the GPS kit to the mobile in the receiver section which is interfaced with PC. In PC we can monitor the aircraft current position on the earth. It also indicates if any other aircraft comes near to it.

BLOCK DIAGRAM

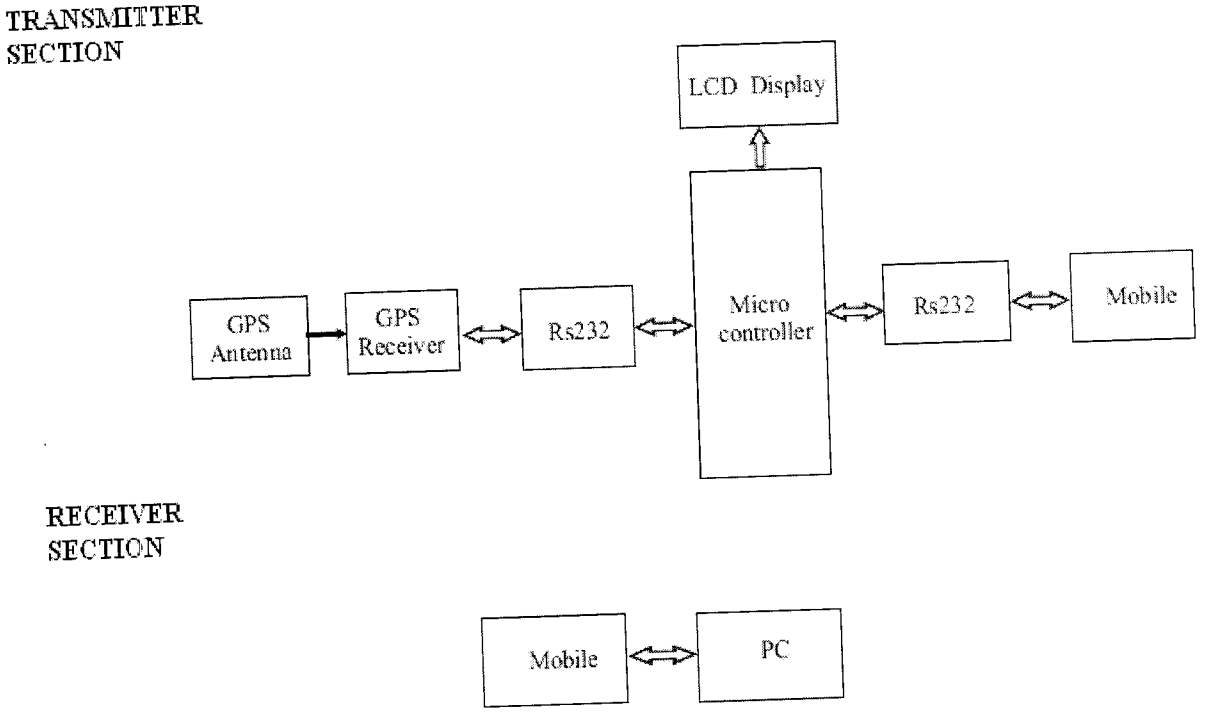
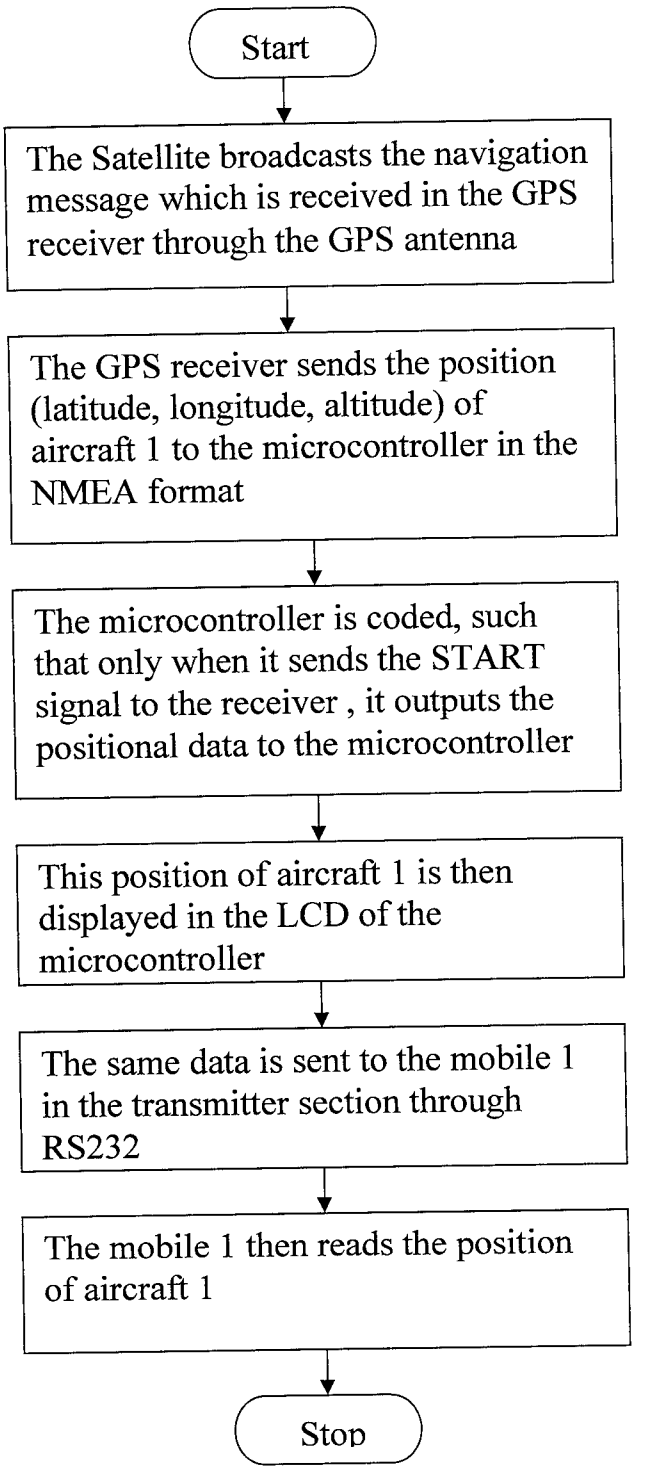
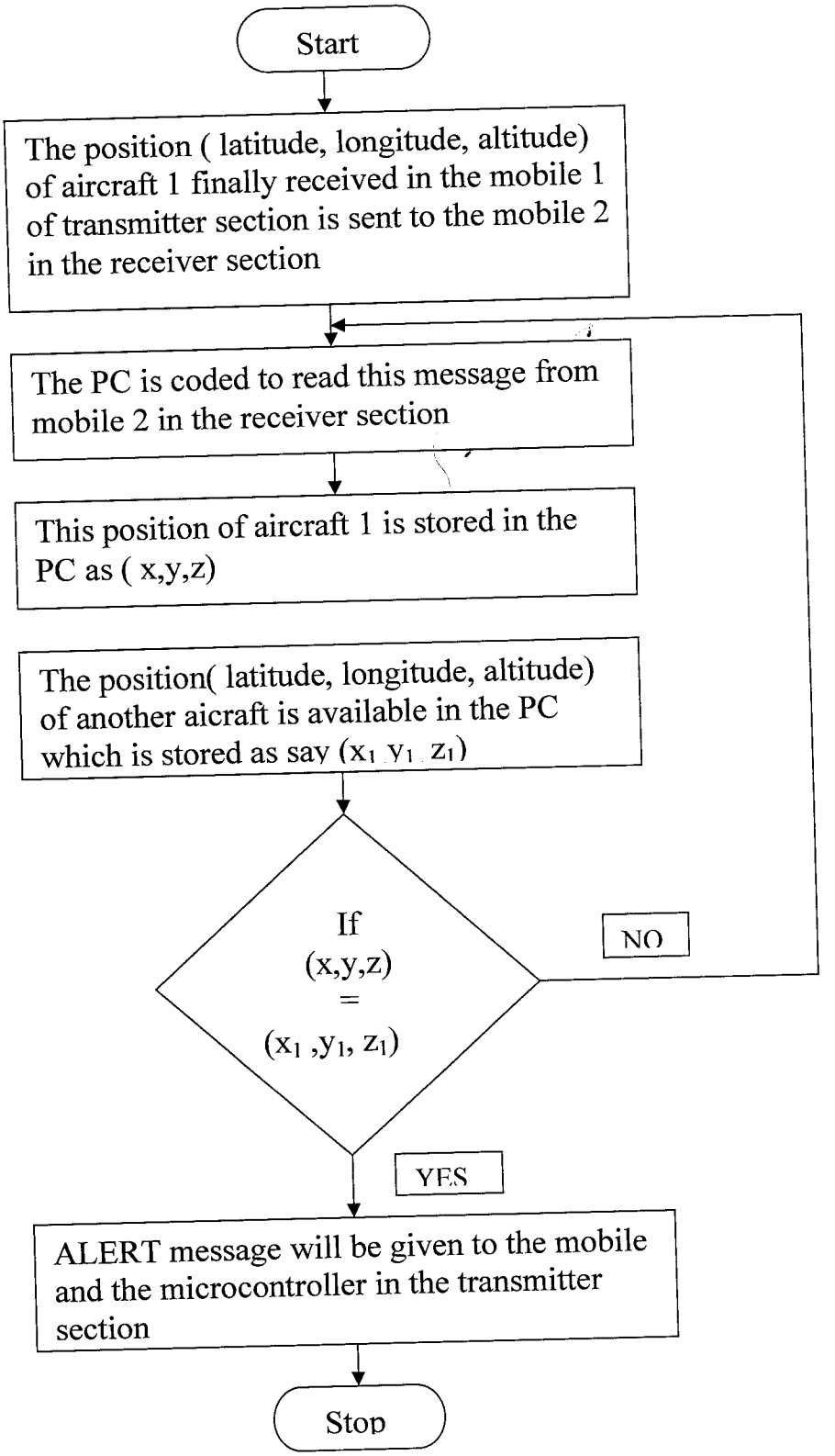


FIGURE 1.1 GPS KIT (HAND CARRIED)

1.3 FLOWDIAGRAM




Start
The position (latitude, longitude, altitude) of aircraft 1 finally received in the mobile 1 of transmitter section is sent to the mobile 2 in the receiver section
The PC is coded to read this message from mobile 2 in the receiver section
This position of aircraft 1 is stored in the PC as (x,y,z)
The position(latitude, longitude, altitude) of another aicraft is available in the PC which is stored as say (x_1 y_1 z_1)
If (x,y,z) = (x_1 ,y_1, z_1)
NO
YES
ALERT message will be given to the mobile and the microcontroller in the transmitter section
Stop

CHAPTER 2

2. GLOBAL POSITIONING SYSTEM

2.1 INTRODUCTION

The Global Positioning System (GPS) is a satellite-based navigation system made up of a network of 24 satellites placed into orbit by the U.S. Department of Defense. GPS was originally intended for military applications, later on the system was available for civilian use also. GPS works in any weather conditions, anywhere in the world, 24 hours a day. There are no subscription fees or setup charges to use GPS.

The Global Positioning System (GPS) is a world wide radio-navigation system formed from a constellation of 24 satellites and their unique address. GPS receivers have been miniaturized to just a few integrated circuits and so are becoming very economical. And that makes the technology accessible to virtually everyone.

GPS satellites circle the earth twice a day in a very precise orbit and transmit signal information to earth. GPS receivers take this information and use triangulation to calculate the user's exact location. Essentially, the GPS receiver compares the time a signal was transmitted by a satellite with the time it was received. The time difference tells the GPS receiver how far away the satellite is. Now, with distance measurements from a few more satellites, the receiver can determine the user's position and display it on the unit's electronic map.

A GPS receiver must be locked on to the signal of at least three satellites to calculate a 2D position (latitude and longitude) and track movement. With four or more satellites in view, the receiver can determine

the aircrafts 3D position (latitude, longitude and altitude). Using this position we are finding the position of the aircraft.

2.2 THE GPS SATELLITE SYSTEM

The 24 satellites that make up the GPS space segment are orbiting the earth about 12,000 miles above us. They are constantly moving, making, two complete orbits in less than 24 hours as shown in figure 2.1.

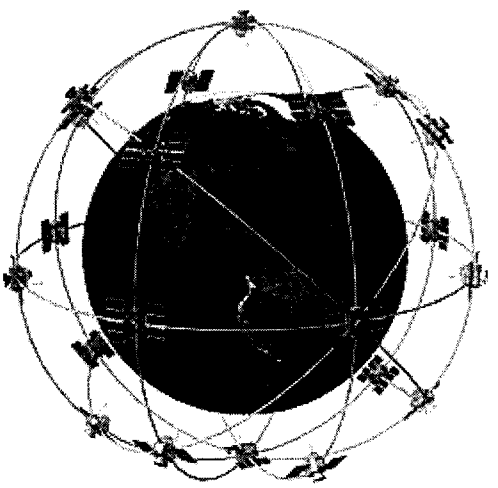


FIGURE 2.1 GPS SATELLITES

2.3 GPS SIGNAL

The Space vehicles transmit two microwave carrier signals. The L1 frequency (1575.42 MHz) carries the navigation message . The L2 frequency (1227.60 MHz) is used to measure the ionospheric delay.

- Three binary codes shift the L1 and L2 carrier phase.
    - The C/A Code (Coarse Acquisition) modulates the L1 carrier phase. The C/A code is a repeating 1 MHz Pseudo Random Noise (PRN) Code. This noise-like code modulates the L1 carrier signal, "spreading" the spectrum over a 1 MHz bandwidth. The C/A code repeats every 1023 bits (one millisecond). There is a different C/A code PRN for each Space vehicle. GPS satellites are often identified by their PRN number, the unique identifier for each pseudo-random-noise codeThe P-Code (Precise) modulates both the L1 and L2 carrier phases. The P-Code is a very long (seven days) 10 MHz PRN code. In the Anti-Spoofing (AS) mode of operation, the P-Code is encrypted into the Y-Code. The Navigation Message also modulates the L1-C/A code signal. The Navigation Message is a 50 Hz signal consisting of data bits that describe the GPS satellite orbits, clock corrections, and other system parameters.

A GPS signal contains three different bits of information : a pseudorandom code, ephemeris data and almanac data. The pseudorandom code is simply an I.D. code that identifies which satellite is transmitting information.

Ephemeris tells the GPS receiver where each GPS satellite should be at anytime throughout the day. Each satellite transmits ephemeris data showing the orbital information for that satellite and for every other satellite in the system.

Almanac data, which is constantly transmitted by each satellite, contains important information about the status of the satellite (healthy or unhealthy), current date and time. This part of the signal is essential for determining the signal.

2.4 LOCATING THE GPS RECEIVER

A GPS receiver determines its position by using the signals that it observes from different satellites. Since the receiver must solve for its position (X,Y,Z) and the clock error (x), four Space vehicles are required to solve receivers position

$$R_1^2 = (X - X_1)^2 + (Y - Y_1)^2 + (Z - Z_1)^2 + x^2$$
$$R_2^2 = (X - X_2)^2 + (Y - Y_2)^2 + (Z - Z_2)^2 + x^2$$
$$R_3^2 = (X - X_3)^2 + (Y - Y_3)^2 + (Z - Z_3)^2 + x^2$$
$$R_4^2 = (X - X_4)^2 + (Y - Y_4)^2 + (Z - Z_4)^2 + x^2$$

where (x_1, y_1) (x_2, y_2) (x_3, y_3) (x_4, y_4) stand for location of satellites and R_1, R_2, R_3, R_4 are the distances of satellites from the receiver position. Hence solving the four equations for four unknowns X, Y, Z and x, the position of the receiver is calculated.

2.5 SOURCES OF GPS SIGNAL ERRORS

The error 'x' is due to the following :

- Ionosphere and troposphere delays
- Signal multipath

- Receiver clock errors
- Orbital errors .
- Number of satellites visible
- Satellite geometry/shading
- Intentional degradation of the satellite signal

CHAPTER 3

3. GPS ANTENNA

GPS modules can either be operated with a passive or active antenna. Active antenna with a built-in preamplifier (LNA: Low Noise Amplifier) are powered from the GPS module, the current being provided by the HF signal. For mobile navigational purposes combined antenna (e.g. GSM/FM and GPS) are supplied.

3.1 TYPES

Two types of antenna can be used, Patch antenna and Helix antenna. Patch antenna is flat, generally have a ceramic and metallised body and are mounted on a metal base plate.

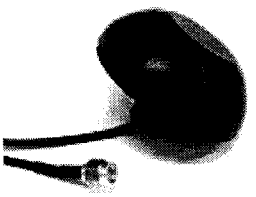


FIGURE 3.1 GPS ANTENNA

3.2 ACTIVE ANTENNA

In our project we use active antenna (patch antenna) as given in figure 3.1. The signal that is transmitted from GPS antenna to the GPS receiver is the Binary Phase Shift Keying modulated signal which is transmitted through Direct sequence spread spectrum modulation. The GLP1-RA model, Capsule Compact Antenna is a high performance 3.3 V DC GPS

antenna. This compact size active antenna is commonly used for OEM (Original Equipment Manufacturer). system integrator and end user applications. The antenna offers a 27 dB gain (active patch). This antenna performs foliage, urban and noisy environments. It is designed for fixed location, permanent mount applications and complies with automotive temperature and vibration standards.

3.3 SPECIFICATIONS

Electrical

- Frequency: 1.575 GHz
- Output / VSWR: 2.0 Max
- Impedance : 50 ohms
- Gain: 27 dB Typical
- Noise Figure: 1.2 dB
- DC voltage: DC 3.3V
- DC Current: 22 mA Typical

Environmental

- Working temperature : -40° C to + 85° C
- Weatherproof: 100% waterproof

Mechanical

- Cable RG 174 - 5 meter long
- Connector: SMA | TNC | SMB

Mounting

- Permanent mount

CHAPTER 4

4. GPS RECEIVER

4.1 GENERAL DESCRIPTION

The uTracker02 OEM (Original Equipment Manufacturer) GPS receiver board is based on the high performance iTrax02/8 GPS receiver architecture . The GPS receiver is given in figure 4.1.

The uTracker02 offers user configurable, low power consumption with three different operational modes. Full navigation mode , Idle mode and Sleep mode can be customized to perfectly meet the requirements of each specific GPS application. The uTracker02 performance regarding sensitivity makes it applicable even for extremely demanding applications and environments with full industrial temperature range.

4.2 FUNCTIONALITY AND I/O'S

The uTracker02 supports the basic GPS functionality plus support for versatile control for sleep state and even the Data logger to Store position information to the internal non-volatile flash memory.

The 2 × 4 pin header connector with 2.0 mm pitch includes two serial ports, one with Transmitter and receiver , the other with receiver only. NMEA and iTalk protocols are supported with standard firmware. The I/O also includes power supply, ground, accurate 1PPS output for timing applications and Power Mode Control input. Nominal power supply is +3.3 V and typical current consumption is 52 mA. The navigational data is stored in non-volatile 8Mbit Flash memory .

4.3 ANTENNA CONNECTOR

The antenna connector is a MCX jack, which provides the active antenna bias supply. The module supports optionally the Antenna Bias Supervisor, which detects a faulty condition, either Open or Short and sends a respective message to the host.

4.4 FEATURES

- Low power consumption – 52mA typical
- Sensitivity – 152 dBm (Tracking)
- Data Logger
- Option for Antenna Bias Supervisor
- Power supply, +3.3 V nominal

The GPS receiver in our project is used to receive the navigation message from the satellite through the GPS antenna. It sends the positional data of the aircraft in the NMEA format to the microcontroller. GPS receiver has inbuilt MAX 232 in it and it is used for voltage conversion.

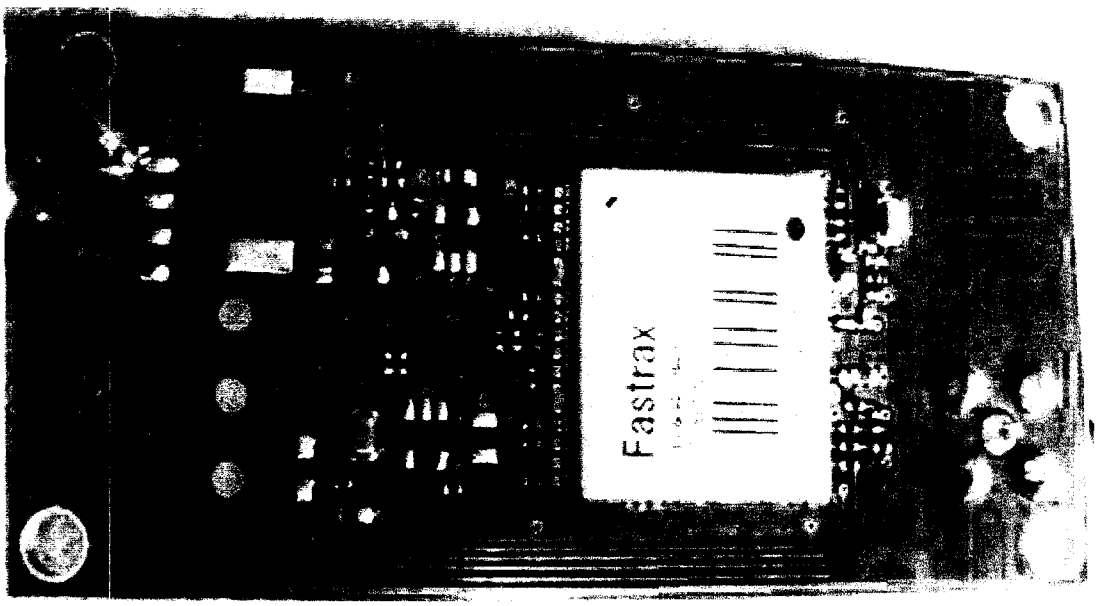


FIGURE 4.1 GPS RECEIVER

CHAPTER 5

5. NATIONAL MARINE ELECTRONICS ASSOCIATION PROTOCOL

NMEA 0183 is a ASCII protocol which defines both the communication interface and the data format. NMEA 0183 has also gained popularity for use in applications other than marine electronics. The scientech receiver supports the latest release of NMEA 0183, Version 3.0. For those applications requiring output only from the GPS receiver, NMEA 0183 can be used.

5.1 THE NMEA 0183 COMMUNICATION INTERFACE

NMEA 0183 allows a single source (talker) to transmit serial data over a single twisted wire pair to one or more receivers (listeners). The table 5.1 below lists the standard characteristics of NMEA 0183 data transmissions.

SIGNAL CHARACTERISTIC	NMEA STANDARD
Baud Rate	4800
Data Bits	8
Parity	None (Disabled)
Stop Bits	1

Table 5.1 Standard Characteristics of NMEA

5.2 NMEA 0183 MESSAGE FORMAT

The NMEA 0183 protocol covers a broad array of navigation data. This broad array of information is separated into discrete messages which convey a specific set of information. The entire protocol encompasses over 50 messages, but only a sub-set of these messages apply to a GPS receiver like the scientech GPS receiver. The NMEA message structure is described below:

$IDMSG, D1, D2, D3, D4, ..., Dn*CS[CR][LF]

Where:

"$"	signifies the start of a message
ID	The talker identification is a two letter mnemonic which describes the source of the navigation information .The GP identification signifies a GPS source.
MSG	The message identification is a three letter mnemonic which describes the message content and the number and order of the data fields.
","	Commas serve delimiters for the data fields.
Dn	Each message contains multiple data fields which are delimited by commas.
"*"	The asterisk serves as a checksum delimiter.

CS	The checksum field contains two ASCII characters which indicates the hexadecimal value of the checksum.
[CR][LF]	The carriage return **[CR]** and line feed **[LF]** combination terminate the message.

NMEA 0183 messages vary in length, but each message is limited to 75 characters or less. This length information excludes the "$" and the [CR][LF]. The data field block including the delimiters, is limited to 74 characters or less.

5.3 NMEA 0183 MESSAGE OPTIONS

The scientech GPS receiver can output any or all of the messages. These messages are sent at milliseconds interval with the "GP" talker ID and checksums. These messages are sent at all times during operation, with or without a fix. If a different set of messages have been selected and this setting has been stored in Flash memory, the default messages are permanently replaced until the receiver is returned to the factory default settings.

5.4 INTERRUPTION OF GPS SIGNAL

If the GPS signal is interrupted temporarily, the NMEA will continue to send the output according to the user-specified message list and output rate. Position and velocity fields will be blank until the next fix, but most of the other fields will be filled.

RMC – Recommended Minimum Specific GNSS (Global Navigation Satellite System) Data

The RMC message contains the time of the position fix, date, the latitude and longitude and the altitude of the present vehicle position, course and speed data.

$GPRMC, hhmmss.dd, s, xxmm.dddd,<N|S>, yyymm.dddd,<E|W>, s.s, h.h, ddmmyy, d.d,<E|W>, M*hh <CR> < LF>

Hhmmss.dd	UTC time hh = hours mm = minutes ss = seconds dd = decimal part of seconds
S	Status indicator A = valid V = invalid
Xxmm. .dddd	Latitude xx = degrees mm = minutes dddd = decimal part of minutes
<N|S>	Either character N or character S, (N = North, S = South)

yyymm.dddd	Longitude yyy = degrees mm = minutes dddd = decimal part of minutes
<E|W>	Either character E or character W , E = East , W = West
s,s	Speed, Knots
h.h	Heading
ddmmyy	Date dd = Date mm = Month yy = Year
d.d	Magnetic variation . This value is available if magnetic model data has been stored to the flash memory (available since firmware rev .1 .08)
<E|W>	Declination, Either character E or character W, E = East, W = West
M	Mode indicator A = autonomous N = data not valid

CHAPTER 6

6. RENESAS

6.1 OVERVIEW

This Micro controller Unit (MCU) is built using the high-performance silicon gate CMOS process using a R8C/Tiny Series CPU core and is packaged in a 32-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, it is capable of executing instructions at high speed. The data flash ROM (2 KB × 2 blocks) is embedded. The pin details of renesas microcontroller is given in figure 6.1.

6.2 CENTRAL PROCESSING UNIT

The block diagram of renesas microcontroller shown in figure 6.2 contains the following: The CPU contains 13 registers. R0, R1, R2, R3, A0, A1 and FB comprise a register bank

Data Registers (R0, R1, R2 and R3)

R0, R1, R2, R3 are 16-bit registers used for transfer, arithmetic and logic operations. The R0 can be split into high-order bit (R0H) and low-order bit (ROL) and can be used separately as 8-bit data registers.Similarly R1 register can also be split into R1H and R1L . R2 can be combined with R0 and can be used as a 32-bit data register (R2R0).

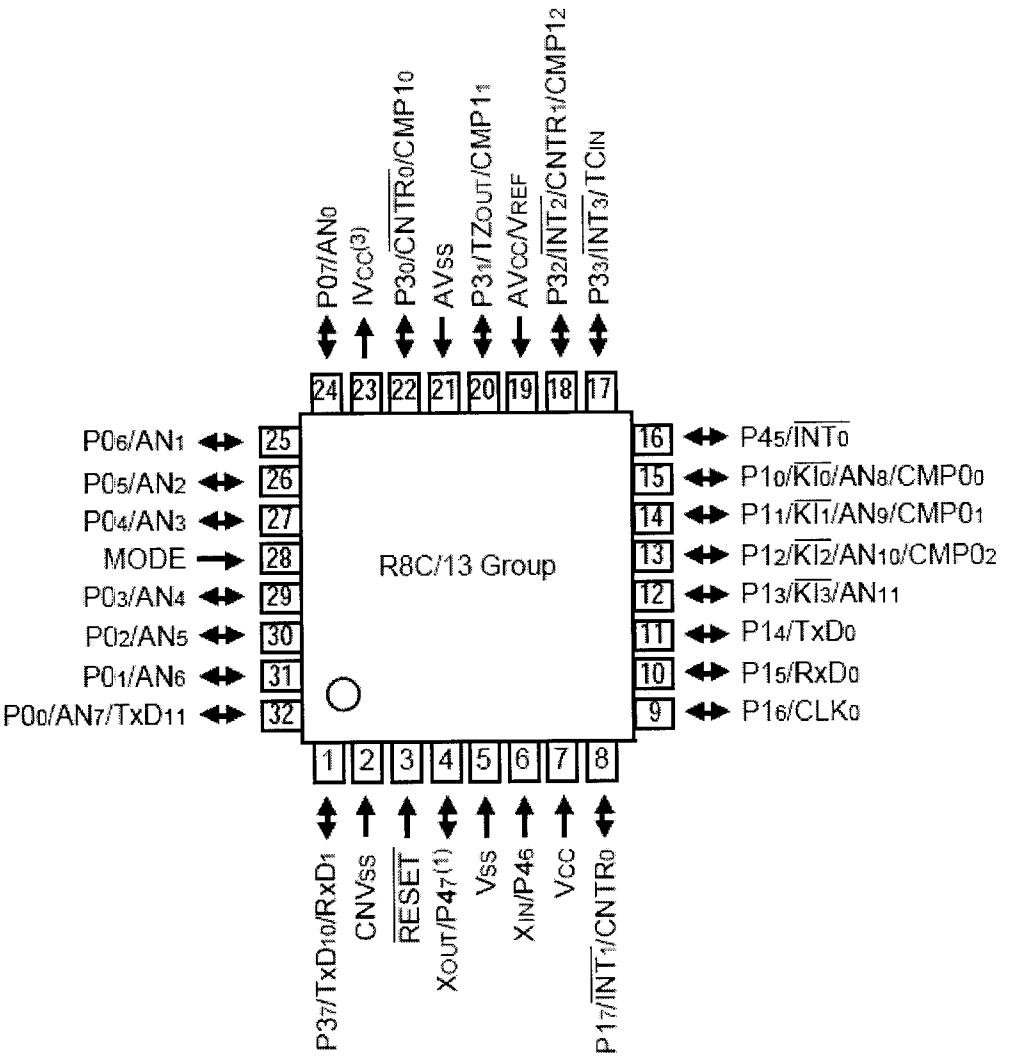


FIGURE 6.1 : PIN DIAGRAM OF RENESAS MICROCONTROLLER

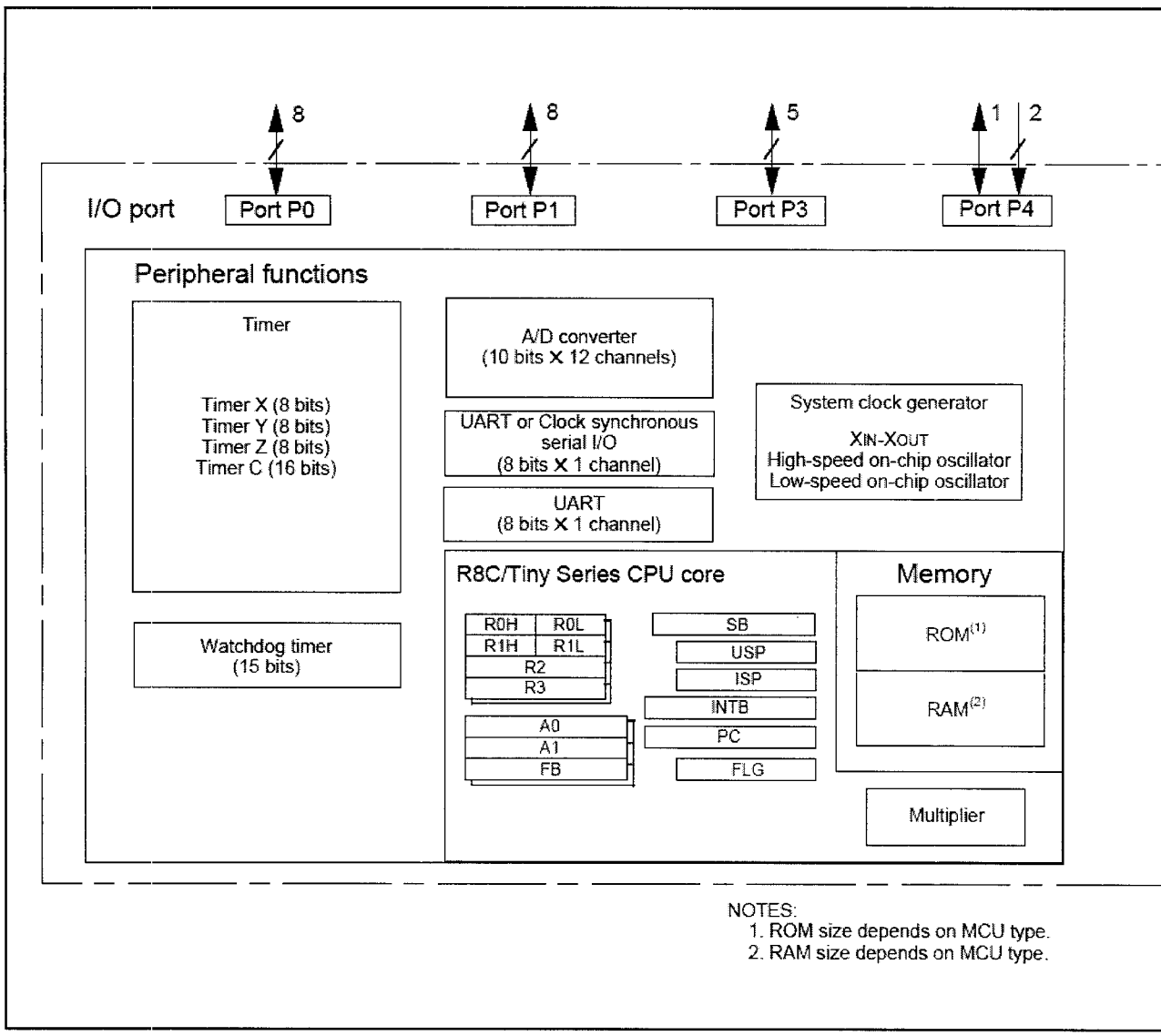


FIGURE 6.2 BLOCK DIAGRAM OF RENASAS MICROCONTROLLER

Address Registers (A0 and A1)

A0 and A1 are 16-bit registers used for address register relative addressing. They are also used for transfer, arithmetic and logic operations.. A0 can be combined with A1 to be used as a 32-bit address register (A1A0).

Frame Base Register (FB) – 16-bit register used for relative addressing.
Interrupt Table Register (INTB) – 20-bit register that indicates the start address of an interrupt vector table.
Program Counter (PC) – 20-bit register that indicates the address of an instruction to be executed.
User Stack Pointer (USP) and Interrupt Stack Pointer (ISP) – 16 bit registers. The U flag of FLG is used to switch between USP and ISP.
Static Base Register (SB) - 16-bit register used for relative addressing.
Flag Register (FLG) - 11-bit register indicating the CPU state.
Carry Flag (C)

The C flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic logic unit.

Debug Flag (D) – When D flag is set to "0" it is used for debug only.
Zero Flag (Z) - The Z flag is set to "1" when an arithmetic operation result is 0.
Sign Flag (S) - The S flag is set to "1" when an arithmetic operation result is a negative value.
Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is "0". The register bank 1 is selected when this flag is set to "1".

Overflow Flag (O) - The O flag is set to "1" when the operation results in an overflow.

Interrupt Enable Flag (I)

The I flag enables a maskable interrupt. An interrupt is disabled when the I flag is set to "1".The I flag is set to "0" when an interrupt request is acknowledged.

Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0", USP is selected when the U flag is set to "1". The U flag is set to "0" when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

Process Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.If a requested interrupt has greater priority than IPL, the interrupt is enabled.

6.3 MEMORY

This MCU provides 1-Mbyte address space from addresses 0000016 to FFFFF16. The internal ROM (program ROM) is allocated lower addresses beginning with address 0FFFF16.

The fixed interrupt vector table is allocated addresses 0FFDC16 to 0FFFF16.They store the starting address of each interrupt routine.The internal ROM is allocated addresses from 0200016 to 02FFF16.The internal RAM is allocated higher addresses beginning with address 0040016.

The internal RAM is not only used for storing data, but also for calling subroutines and stacks when interrupt request is acknowledged. Special function registers (SFR) are allocated addresses 0000016 to 002FF16.

Thus in our project the renesas microcontroller is used since we are in need of two serial ports, one for accepting data from GPS receiver and the other to send the data to the mobile. The microcontroller is coded such that it reads the positional data of the aircraft, which is sent by the GPS receiver and the microcontroller also sends a short message service(SMS) to the mobile in the receiver section. Finally the microcontroller also reads the ALERT message sent by the receiver section.

CHAPTER 7

7. RS 232 (SERIAL INTERFACE)

Modems and other devices used to send serial data are often referred to as DATA CIRCUIT-TERMINATING EQUIPMENT (DCE).The terminals or computers that are sending or receiving the data are referred to as DATA TERMINAL EQUIPMENT (DTE). In response to the need for signal and handshake standards between DTE and DCE, the Electronics Industries Association (EIA) developed EIA standard RS-232C. This standard describes the functions of 25 signals and handshake pins for serial data transfer. It also describes the voltage levels, Impedance levels, rise and fall times, maximum bit rate, and maximum capacitance for these signal lines.

7.1 INTERFACING DEVICES TO RS-232 PORTS

RS-232 waveforms

RS-232 communication is asynchronous. That is a clock signal is not sent with the data. Each word is synchronized using it's start bit, and an internal clock on each side, keeps tabs on the timing.

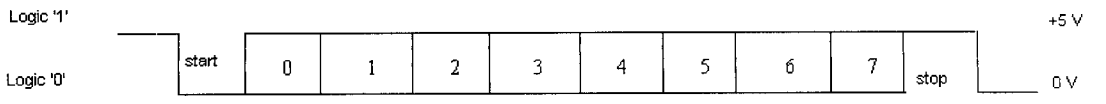


FIGURE 7.1 TTL/CMOS SERIAL LOGIC WAVEFORM

The figure 7.1 above, shows the expected waveform from the UART . The RS-232 line, when idle is in the Mark stage (Logic 1). A transmission starts with a start bit which is (Logic 0). Then each bit is sent down the line, one at a time. The LSB (Least Significant Bit) is sent first.

A Stop Bit (Logic 1) is then appended to the signal to make up the transmission. The diagram, shows the next bit after the Stop Bit to be logic 0. This must mean another word is following, and that is Start Bit. If there is no more data coming then the receiver line will stay in it's idle stage (Logic 1). We have encountered something called a "Break" Signal, This is when the data line is held in a logic 0 state for a time long enough to send an entire word. Therefore if you don't put the line back into an idle state, then the receiving end will interpret this as a break signal.

As per the figure 7.2 , the data sent using this method, is said to be framed. That is the data is framed between a Start and Stop Bit. RS-232 logic level uses +3 to +25 volts to signify a "Space" (Logic 0) and –3 to –25 volts for a "Mark"(logic 1).

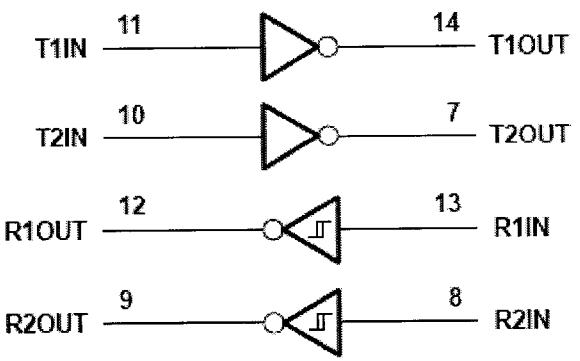


FIGURE 7.2 LOGIC DIAGRAM (POSITIVE LOGIC)

Any voltage in between these regions (ie between +3 and –3 Volts) is undefined. Therefore this signal is put through a "RS-232 Level Converter". This is the signal present on the RS-232 port of the computer, shown below.

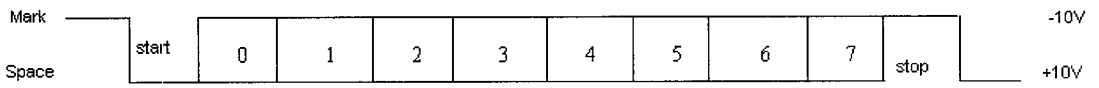


FIGURE 7.3 RS-232 LOGIC WAVEFORM

The waveform shown in figure 7.3 applies to the trasmit and receive lines on the RS-232 port. These lines carry serial data, hence the name Serial Port. There are other lines on the RS-232 port which, in essence are Parallel lines.

7.2 RS-232 LEVEL CONVERTERS

Almost all digital devices which we use require either TTL or CMOS logic levels. Therefore the first step to connecting a device to the RS-232 port is to transform the RS-232 levels back into 0 and 5 Volts.

Two common RS-232 Level Converters are the 1488 RS-232 Driver and the 1489 RS-232 Receiver. Each package contains 4 inverters of the one type, either Drivers or Receivers. The driver requires two supply rails, +7.5 to +15v and –7.5 to -15V. As you could imagine this may pose a problem in many instances where only a single supply of +5V is present.

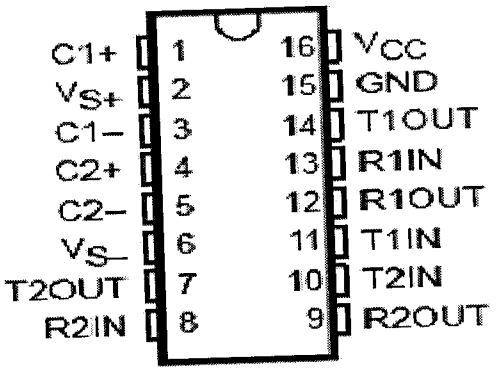


FIGURE 7.4 PINOUTS FOR MAX-232, RS-232 DRIVER/RECEIVER

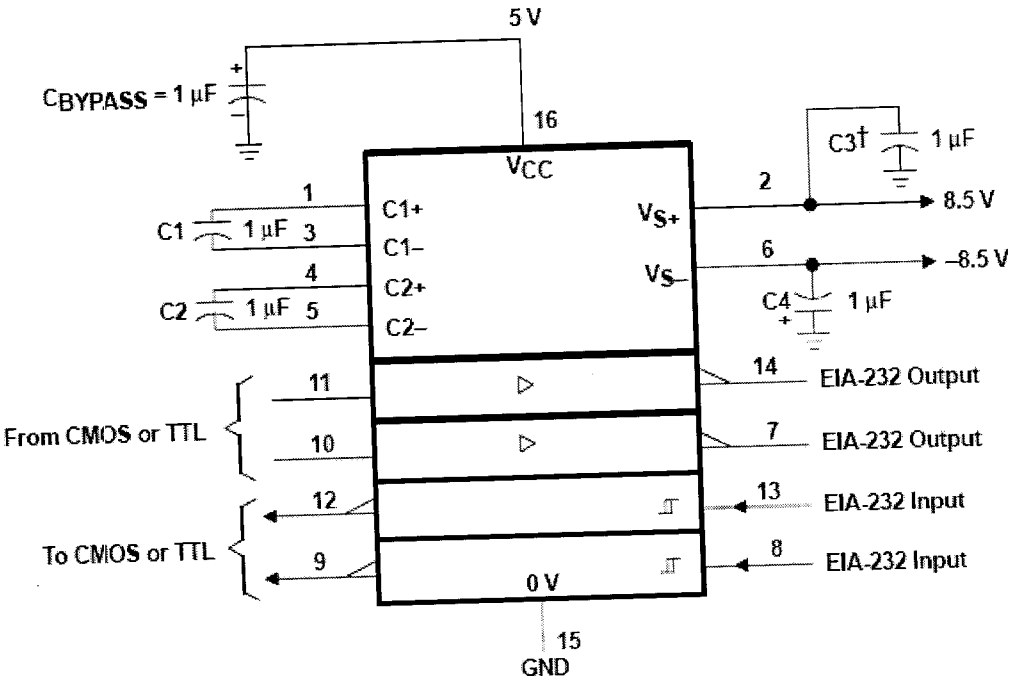


FIGURE 7.5 TYPICAL MAX-232 CIRCUIT

Another device is the MAX-232 which is shown in figure 7.5. It includes a Charge Pump, which generates +10V and –10V from a single 5V supply. This IC also includes two receivers and two transmitters in the same package. The pin details of MAX-232 is given in figure 7.4

This is handy in many cases when we want to use the Trasmit and Receive data lines. compared with the price of designing a new power supply it is very cheap. . The large value of capacitors are not only bulky, but also expensive. Therefore other devices are available which use smaller capacitors and some with inbuilt capacitors. The function table 7.1 gives the details of each drive and receiver.

EACH DRIVER

INPUT TIN	OUTPUT TOUT
L	H
H	L

H = high level, L = low level

EACH RECEIVER

INPUT RIN	OUTPUT ROUT
L	H
H	L

H = high level, L = low level

TABLE 7.1 FUNCTION TABLES

In our project, we have used RS232 for interfacing GPS with the microcontroller and also for interfacing microcontroller with the mobile. The MAX232 does voltage conversion from 5volts to 12volts and vice-versa.

CHAPTER 8

8. LCD DISPLAY

8.1 INTRODUCTION

Liquid crystal displays (LCDs) have materials which combine the properties of both liquids and crystals The LCD's are lightweight with only a few millimeters thickness. Since the LCD's consume less power, they are compatible with low power electronic circuits, and can be powered for long durations.

The LCD's don't generate light and so light is needed to read the display. By using backlighting, reading is possible in the dark. The LCD's have long life and a wide operating temperature range. Changing the display size or the layout size is simple.

The LCDs used exclusively in watches, calculators and measuring instruments are the simple seven-segment displays, having a limited amount of numeric data.

The recent advances in technology have resulted in better legibility, more information displaying capability and a wider temperature range. These have resulted in the LCDs being extensively used in telecommunications and entertainment electronics. The LCDs have even started replacing the cathode ray tubes (CRTs) used for the display of text and graphics, and also in small TV applications.

8.2 POWERSUPPLY

The power supply should be of +5V, with maximum allowable transients of 10mV. To achieve a better / suitable contrast for the display, the voltage (VL) at pin 3 should be adjusted properly.

A module should not be inserted or removed from a live circuit. The ground terminal of the power supply must be isolated properly so that no voltage is induced in it. The module should be isolated from the other circuits, so that stray voltages are not induced, which could cause a flickering display.

8.3 CRYSTALONICS DISPLAY

Crystalonics dot-matrix (alphanumeric) liquid crystal displays are available with or without backlight. The use of C-MOS LCD controller and driver ICs result in low power consumption. These modules can be interfaced with a 4-bit or 8-bit micro processor/Micro controller.

The built-in controller IC has the following features:

- Correspond to high speed MPU interface (2MHz)
- 80 x 8 bit display RAM (80 Characters max)
- 9,920 bit character generator ROM for a total of 240 character fonts. 208 character fonts (5 x 8 dots) 32 character fonts (5 x 10 dots)
- 64 x 8 bit character generator RAM 8 character generator RAM 8 character fonts (5 x 8 dots) 4 characters fonts (5 x 10 dots)
- Programmable duty cycles

- 1/8 – for one line of 5 x 8 dots with cursor
- 1/11 - for one line of 5 x 10 dots with cursor
- 1/16 – for one line of 5 x 8 dots with cursor
- Wide range of instruction functions display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift.
- Automatic reset circuit, that initializes the controller / driver ICs after power on.

FUNCTIONAL DESCRIPTION OF THE CONTROLLER IC

REGISTERS:

The controller IC has two 8 bit registers, an instruction register (IR) and a data register (DR). The IR stores the instruction codes and address information for display data RAM (DDRAM) and character generator RAM (CGRAM). The IR can be written, but not read by the MPU.

The DR temporally stores data to be written to / read from the DDRAM or CGRAM. The data written to DR by the MPU, is automatically written to the DDRAM or CGRAM as an internal operation.

When an address code is written to IR, the data is automatically transferred from the DDRAM or CGRAM to the DR. Data transfer between the MPU is then completed when the MPU reads the DR. Likewise, for the next MPU read of the DR, data in DDRAM or CGRAM at the address is sent to the DR automatically. Similarly, for the MPU write of the DR, the next DDRAM or CGRAM address is selected for the write operation.

The register selection table is as shown in TABLE 8.1

RS	R/W	OPERATION
0	0	IR write as an internal operation
0	1	Read busy flag (DB7) and Address counter (DB0 to DB6)
1	0	DR write as an internal operation (DR to DD RAM or CG RAM)
1	1	DR read as an internal operation (DDRAM or CGRAM to DR)

TABLE 8.1 REGISTER SELECTION AND THEIR OPERATIONS

8.4 BUSY FLAG:

When the busy flag is1, the controller is in the internal operation mode, and the next instruction will not be accepted. When RS = 0 and R\W = 1 , the busy flag is output to DB7.The next instruction must be written after ensuring that the busy flag is 0.

8.5 ADDRESS COUNTER:

The address counter allocates the address for the DDRAM and CGRAM read/write operation when the instruction code for DDRAM address or CG RAM address setting, is input to IR, the address code is transferred from IR to the address counter. After writing/reading the display data to/from the DDRAM or CGRAM, the address counter increments/decrements by one the address, as an internal operation. The data of the address counter is output to DB0 to DB6 while R/W = 1 and RS = 0.

The characters to be displayed are written into the display data RAM (DDRAM), in the form of 8 bit character codes present in the character font table. The extended capacity of the DDRAM is 80 x 8 bits i.e, 80 characters. The character generator ROM generates 5 x 8 dot 5 x 10 dot character patterns from 8 bit character codes. It generates 208, 5 x 8 dot character patterns and 32, 5 x 10 dot character patterns.

8.6 INTERFACING THE MICROPROCESSOR / CONTROLLER:

The module, interfaced to the system, can be treated as RAM input/output, expanded or parallel I/O. Since there is no conventional chip select signal, developing a strobe signal for the enable signal (E) and applying appropriate signals to the register select (RS) and read/ write (R/W) signals are important.

The module is selected by gating a decoded module – address with the host – processor's read/write strobe. The resultant signal , applied to the LCDs enable (E) input, clocks in the data. The 'E' signal must be a positive

going digital strobe, which is active while data and control information are stable and true. The falling edge of the enable signal enables the data / instruction register of the controller. All module timings are referenced to specific edges of the 'E' signal. The 'E' signal is applied only when a specific module transaction is desired. The read and write strobes of the host, which provides the 'E' signals, should not be linked to the modules R/W line. An address bit which sets up earlier in the host's machine cycle can be used as R/W.

When the controller is performing an internal operation the busy flag (BF) will be set and will not accept any instruction. The user should check the busy flag or should provide a delay of approximately 2ms after each instruction.

The module presents no difficulties while interfacing slower MPUs. The liquid crystal display module can be interfaced, either to 4-bit or 8-bit MPUs.

For 4-bit data interface, the bus lines DB4 to DB7 are used for data transfer, while DB0 to DB3 lines are disabled. The data transfer is complete when the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data. For 8-bit data interface, all eight-bus lines (DB0 to DB7) are used.

The LCD is used to display the positional data obtained in the microcontroller. The type of LCD used is crystalonics display.

CHAPTER 9

9. POWER SUPPLY

9.1 INTRODUCTION:

The present chapter introduces the operation of power supply circuits built using filters, rectifiers, and then voltage regulators. Starting with an ac voltage, a steady dc voltage is obtained by rectifying the ac voltage, then filtering to a dc level, and finally, regulating to obtain a desired fixed dc voltage. The regulation is usually obtained from an IC voltage regulator unit, which takes a dc voltage and provides a somewhat lower dc voltage, which remains the same even if the input dc voltage varies, or the output load connected to the dc voltage changes.

A block diagram containing the parts of a typical power supply and the voltage at various points in the unit is shown in fig 9.1. The ac voltage, typically 120 Vrms, is connected to a transformer, which steps that ac voltage down to the level for the desired dc output. A diode rectifier then provides a full-wave rectified voltage that is initially filtered by a simple capacitor filter to produce a dc voltage. This resulting dc voltage usually has some ripple or ac voltage variation. A regulator circuit can use this dc input to provide a dc voltage that not only has much less ripple voltage but also remains the same dc value even if the input dc voltage varies somewhat, or the load connected to the output dc voltage changes. This voltage regulation is usually obtained using one of the number of popular voltage regulator IC units.

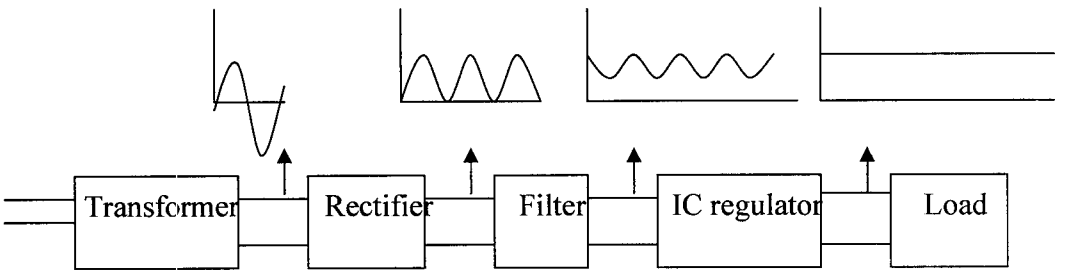


FIGURE 9.1 POWERSUPPLY

9.2 IC VOLTAGE REGULATORS:

Voltage regulators comprise a class of widely used ICs. Regulator IC units contain the circuitry for reference source, comparator amplifier, control device, and overload protection all in a single IC. Although the internal construction of the IC is somewhat different from that described for discrete voltage regulator circuits, the external operation is much the same. IC units provide regulation of either a fixed positive voltage, a fixed negative voltage, or an adjustable set voltage.

A power supply can be built using a transformer connected to the ac supply line to step the ac voltage to a desired amplitude, then rectifying that ac voltage, filtering with a capacitor and RC filter, if desired, and finally regulating the dc voltage using an IC regulator. The regulators can be selected for operation with load currents from hundreds of milli amperes to tens of amperes, corresponding to power ratings from milli watts to tens of watts.

9.3 THREE-TERMINAL VOLTAGE REGULATORS:

Fig shows the basic connection of a three-terminal voltage regulator IC to a load. The fixed voltage regulator has an unregulated dc input voltage, Vi, applied to one input terminal, a regulated output dc voltage, Vo, from a second terminal, with the third terminal connected to ground. For a selected regulator, IC device specifications lists a voltage range over which the input voltage can vary to maintain a regulated output voltage over a range of load current. The specifications also list the amount of output voltage change resulting from a change in load current (load regulation) or in input voltage (line regulation).

9.4 FIXED POSITIVE VOLTAGE REGULATORS:

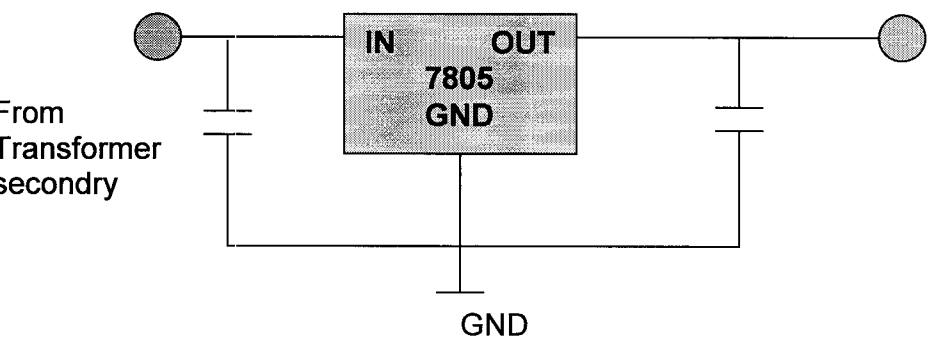


FIGURE 9.2 VOLTAGE REGULATION USING 7805

The series 78 regulators provide fixed regulated voltages from 5 to 24 V. Figure 9.2 shows how one such IC, a 7812, is connected to provide voltage regulation with output from this unit of +12V dc. An unregulated

input voltage Vi is filtered by capacitor C1 and connected to the IC's IN terminal. The IC's OUT terminal provides a regulated + 12V which is filtered by capacitor C2 (mostly for any high-frequency noise). The third IC terminal is connected to ground (GND). While the input voltage may vary over some permissible voltage range, and the output load may vary over some acceptable range, the output voltage remains constant within specified voltage variation limits. These limitations are spelled out in the manufacturer's specification sheets. A table of positive voltage regulated ICs is provided in table 9.1.

TABLE 9.1 Positive Voltage Regulators in 7800 series

IC Part	Output Voltage (V)	Minimum Vi (V)
7805	+5	7.3
7806	+6	8.3
7808	+8	10.5
7810	+10	12.5
7812	+12	14.6
7815	+15	17.7
7818	+18	21.0
7824	+24	27.1

CONCLUSION

The project can be used effectively within the globe. It can be used to avoid collision between manned and unmanned aircrafts and military crafts.

The future scope of the project are as follows. The GPS kit can be miniatured using nano technology and can be placed inside the mobile present within the object to be traced. It can also be fabricated as a single GPS transmitting chip and placed within the object itself.

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