A DIRECT AC-AC CONVERTER BASED ON MATRIX METHOD

A PROJECT REPORT

Submitted by

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BONAFIDE CERTIFICATE

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ABSTRACT

The frequency conversion of single phase AC supply was done with Rectifier-inverter module using capacitors. The DC link between the rectifier and the output bridge requires the use of large electrolytic capacitors. These not only occupy a lot of space, they are also the components most likely to limit the useful life of the drive, since they lose capacity over time, especially when operated at high ambient temperatures. With the advancement of technology, solid state switches came into exists and replaced the Capacitor Rectifier-Inverter module.

In this module of solid state switches, the incoming AC supply is rectified by a diode bridge to produce DC, and then fed to an output bridge that, in turn, produces an AC output to drive the motor. The majority of Cyclo-Converter are naturally commutated SCRs and the maximum output frequency is limited to a value that is only a fraction of input frequency (0-20 Hz output for 50 Hz input). More over the output voltage is present with high order of harmonics.

With the rapid advancement in fast acting fully controlled switches, Force-Commutated Cyclo-Converters (FCC) came into exist. With sinusoidal modulated output voltage/current can be achieved with new design of Cyclo-Converter. Here bidirectional switches are used for providing control of the magnitude and frequency of the generated output voltage/current.

Matrix converter is a Forced Commutated Cyclo-Converter based on bidirectional fully controlled switches, incorporating PWM technique with reduced switching devices. It has an unlimited output frequency range variation i.e., less than input frequency or above the input frequency ($f_O \leq f_i$ & $f_O \geq f_i$) as it possess static switches with controlled turn on and turn off capability. Compared with naturally commutated Cyclo-Converters, Matrix converter requires four bidirectional switches. So, switching losses can be reduced to a great extent.

In this project, a Single Phase to Single Phase Matrix Converter with passive load condition is presented. The results of the SPMC for both the simulation and experiments illustrates that it is feasible to realize the converter as a frequency step-up or step-down converter.

ACKNOWLEDGEMENT

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LIST OF SYMBOLS AND ABBREVIATIONS

NO.	SYMBOLS	ABBREVIATIONS
01	AC	Alternating Current
02	DC	Direct Current
03	PWM	Pulse Width Modulation
04	SPWM	Sinusoidal Pulse Width Modulation
05	SCR	Silicon Control Rectifier
06	MOSFET	Metal Oxide Semiconductor Field Effect Transistor
07	FCC	Force-Commutated Cyclo-Converters
08	SPMC	Single Phase Matrix Converter
09	PIC	Peripheral Interface Controller
10	IC	Integrated Circuits
11	ZCD	Zero Crossing Detector
12	CMOS	Complimentary Metal Oxide Semiconductor
13	LED	Light Emitting Diode
14	ILED	Infrared Light Emitting Diode
15	IGBT	Integrated Gate Bipolar Transistor
16	I/O	Input / Output
17	CRO	Cathode Ray Oscilloscope
18	DSO	Digital Signal Oscilloscope

CHAPTER 1

INTRODUCTION

1. INTRODUCTION

The frequency conversion of single phase AC supply was done with Rectifier-inverter module using capacitors. The DC link between the rectifier and the output bridge requires the use of large electrolytic capacitors. These not only occupy a lot of space, they are also the components most likely to limit the useful life of the drive, since they lose capacity over time, especially when operated at high ambient temperatures. With the advancement of technology, solid state switches came into exist and replace the capacitor Rectifier-inverter module. In this module the incoming AC supply is rectified by a diode bridge to produce DC, and then fed to an output bridge that, in turn, produces an AC output to drive the motor.

The AC to AC power converters in which AC power at one frequency is directly converted to Ac power at another frequency without any intermediate conversion link are known as Cyclo-Converters. The majority of Cyclo-Converter are naturally commutated SCRs and the maximum output frequency is limited to a value that is only a fraction of input frequency (0-20 Hz output, for 50 Hz input). More over the output voltage is present with high order of harmonics.

With the rapid advancement in fast acting fully controlled switches, Force-Commutated Cyclo-Converters (FCC) came into exist. With sinusoidal modulated output voltage/current can be achieved with new design of Cyclo-Converter. Here bidirectional switches are used for providing control of the magnitude and frequency of the generated output voltage/current.

In this project a Cyclo-Converter with bidirectional switches is designed. This new topology was first proposed by Gyugyi in 1976. A matrix of semiconductor switches replaces the rectifier and DC link in the power section of conventional AC drives. The incoming supply of drive is connected directly to the motor, via a matrix of bi-directional semiconductor switches. By correctly sequencing the operation of these switches, the voltage and frequency of the output to the motor can be precisely controlled. Single Phase Matrix Converter (SPMC) is more reliable and potentially has much longer lives, especially when they have to operate in tough environmental conditions.

Matrix Converter is a Forced Commutated Cyclo-Converter based on bidirectional fully controlled switches, incorporating PWM technique with reduced switching devices. It has an unlimited output frequency range i.e., less than input frequency or above the input frequency ($f_O \leq f_i$ & $f_O \geq f_i$) as it possess static switches with controlled turn on and turn off capability. Compared with naturally commutated Cyclo-Converters, Matrix converter requires four bidirectional switches. So, switching losses can be reduced to a great extent.

1.1. ADVANTAGES OF MATRIX CONVERTER:

- In comparison with conventional Cyclo-Converter, the bi-directional switches in Matrix topology can allow power to flow in either direction, hence the efficient operation can be achieved in all four quadrants
- In applications such as lifts and hoists where the drive is likely to spend a large proportion of its time braking and bulky braking resistors are needed in conventional Cyclo-Converter but in Matrix Module no need of bulky braking resistor
- In this topology heat generation can be reduced considerably and it is compact in size comparing with conventional module.
- With their superior performance in virtually every area, there is no doubt that matrix converter drives will eventually – as production volumes increase and prices fall make conventional drives obsolete.

1.2. APPLICATIONS OF MATRIX CONVERTER:

1. Electric traction
2. High Voltage DC transmission
3. Induction Heating
4. Speed control of high power AC motors
5. Variable speed, constant frequency power generation
6. Ball mill drives in cement factories (gearless drive)

1.3. DESIGN OF THE MATRIX TOPOLOGY:

The block diagram for the new design is shown in Fig. 1.1.It consist of

- Zero crossing detector circuit
- Control unit
- Driver circuit
- SPMC circuit

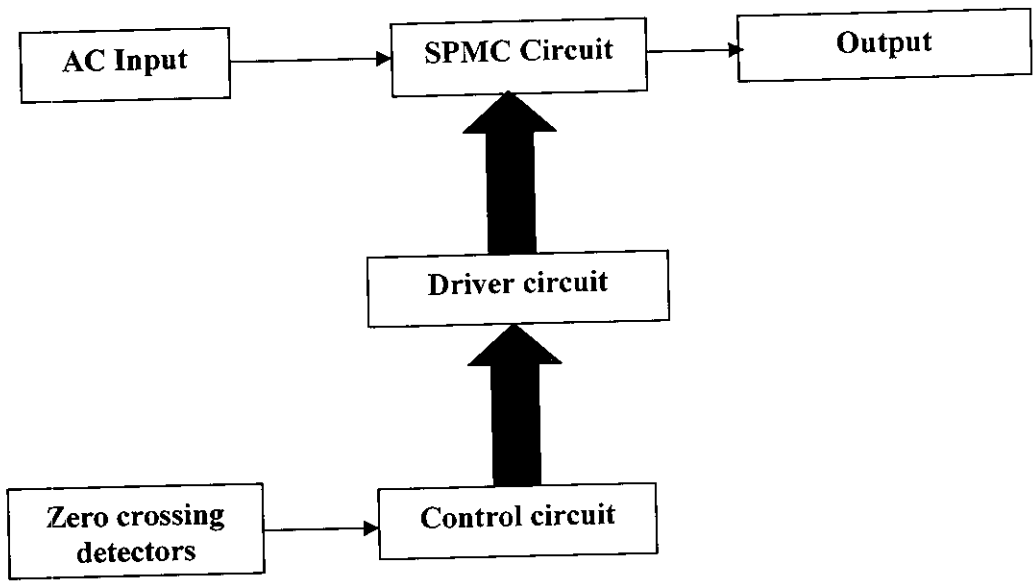


Fig 1.1. Block diagram of the proposed SPMC test Model

1.3.1. Zero Crossing Detector Circuit:

It is a circuit that converts the input line supply into the low voltage square pulses to analyze the zero crossing of the input sine wave. This circuit is designed with the help of Dual operational amplifier (LM358). The output terminal of the zero crossing detectors is connected to the input port of the Micro-Controller to fed the zero crossing data to the controller.

1.3.2. Control Circuit:

Micro-Controller is used to control the switching sequence of the MOSFETs present in SPMC circuit. PWM pulse is generated by the controller to trigger the gate terminal of MOSFETs. The frequency is varied by controlling the time of applying pulse to the gate of the MOSFETs. The type of controller used in this project is PIC (16F877A) due to its easiness, reliability, cost effective and various other features.

1.3.3. Driver Circuit:

The Micro-Controller output pins which generate gate signals for the MOSFETs cannot be directly connected to the gate terminal of the power device.
If it so connected, there is a chance for the back flow of high voltage from the SPMC circuit, that may damage the Controller. In addition, the gate signal from the PIC controller may be weak that it cannot trigger a MOSFET. So it has to be amplified by gate driver circuit. Opto-transistor (MCT2E) is used in this project for isolating the controller output and the gate terminal of a MOSFET.

1.3.4. Single phase Matrix Converter (SPMC) Circuit:

This is the main part of this project which is a power electronic converter circuit to convert Single phase AC power at one frequency to AC power at another frequency by AC to AC conversion without an intermediate conversion link. The frequency of the input AC supply can be varied according to the user input to the frequency control switch and the output frequency can be above or below the input supply frequency. In this project the input frequency (50 Hz) is converted into 25 Hz and 100 Hz of output frequency.

The arrangement of project report is as follows

Chapter 2: Zero Crossing Detectors--This chapter explains the design of Zero Crossing Detector Circuit used for finding the rising edges of the input AC supply.

Chapter 3: Control and Drive Circuit— This chapter explains the design of Drive and Control circuit used for generating the PWM pulses for trigger the Solid State Switches.

Chapter 4: SPMC Circuit—This chapter describes about the principal of operation and switching strategies of the Single phase Matrix Circuit.

Chapter 5: Software Implementation-- This chapter gives an introduction about MATLAB SIMULINK, design of Matrix Network, sequences of switching control and results of output waveforms.

Chapter 6: Hardware Implementation—This chapter explains the design and fabrication of Hardware implementation and hardware results.

Chapter 7: conclusion – Gives advantages and application of this module and future scope of the project.

CHAPTER 2

ZERO CROSSING DETECTOR

2. ZERO CROSSING DETECTORS

2.1. INTRODUCTION:

Zero crossing Detector is a circuit that converts the input line supply into the low voltage square pulses to analyze the zero crossing of the input sine wave. This circuit is designed with the help of Dual operational amplifier (LM358). The output terminal of the zero crossing detectors is connected to the input port of the Micro-Controller to feed the zero crossing data to the controller.

2.2. ZERO CROSSING DETECTORS:

The zero crossing detectors is a device for detecting the point where the voltage crosses zero in either direction. Zero crossing detectors as a group are not a well-understood application, although they are essential elements in a wide range of products. A zero crossing detector literally detects the transition of a signal waveform from positive and negative, ideally providing a narrow pulse that coincides exactly with the zero voltage condition. At first glance, this would appear to be an easy enough task, but in fact it is quite complex, especially where high frequencies are involved. In this instance, even 1 kHz starts to present a real challenge if extreme accuracy is needed.

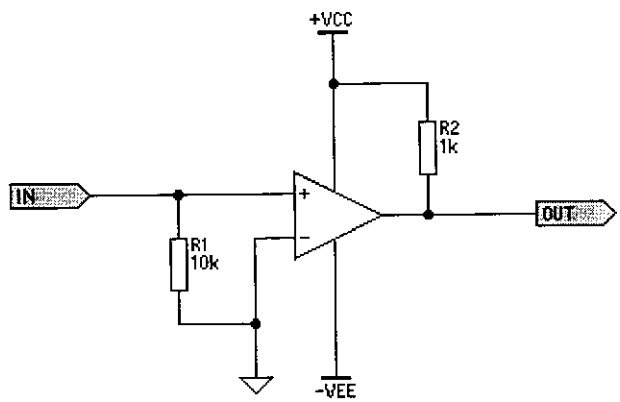


Fig.2.1.Camparator Zero Crossing Detector

The detector circuit is added to analyze the state of single phase input sine wave at each instant. The basic comparator circuit can be modified as zero crossing detector. Here, we have adapted comparator (LM 358).

The V+ and V- power supply terminals are connected to two DC voltage sources. V+ is connected to the positive terminal of one source and V- pin is connected to the negative terminal of the other source. The power supply voltage range from about 5V to 22V. The common terminal of V+ and V- sources is connected to the reference or ground.

2.3. PIN CONFIGURATION:

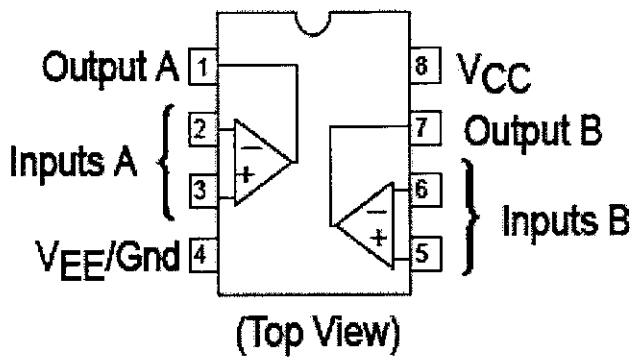


Fig.2.2. pin diagram

2.4. ZERO CROSSING DETECTION:

The input supply is stepped down to twelve volts and it is given to the non-inverting terminal of the op-amp through a resistance of 330 ohm. The inverting terminal is connected to the ground of the supply. The V+ pin is connected to the microcontroller supply and V- pin and ground terminals of op-amp are connected to the ground of the controller supply. The output is taken from the pin 6 through a resistance of 220 ohm and is fed to the input port of the controller. This is the extension of basic comparator circuit with Vref being set to zero.

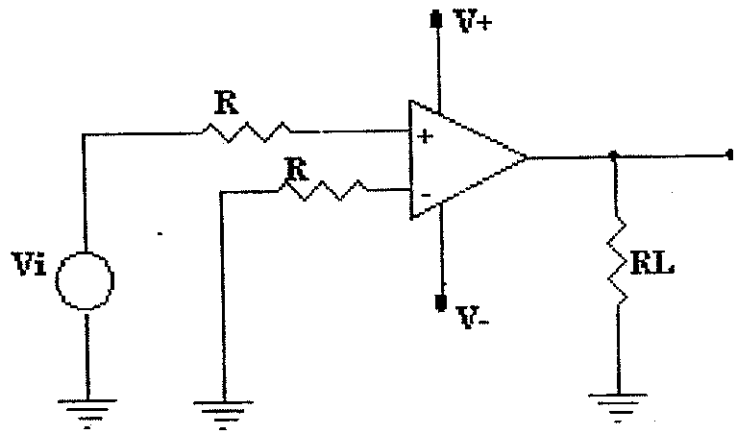


Fig. 2.2. Detection Circuit

When the input sine wave of the inverting terminal crosses 0V from negative to positive cycle, the output waveform of zero crossing detector shifts from +Vsat value to ground state. When the sine wave crosses the zero from positive to negative half cycle, the output waveform is suddenly shifted to the HIGH state from ground state. Thus the zero crossing detector generates square wave for the given sine wave. So, this circuit is also called sine to square wave generator.

2.5. CONCULSION:

The LM 358 has high gain compare with op-amp (IC 741) and also it has internal frequency compensation. These amplifiers have several distinct advantages over standard Operational amplifier types in single supply applications. They can operate at supply voltages as low as 3.0 V or as high as 32 V. So that LM358 has appropriate usage in this project and its data sheet is given in Appendix 2.

CHAPTER 3

CONTROL AND DRIVE CIRCUIT

3. CONTROL AND DRIVE CIRCUIT

3.1. INTRODUCTION:

The control and drive circuit consists of PIC Controller (16F877A) and Opto transistor (MCT2E) respectively. The PIC Micro-Controller is used to control the switching sequence of the MOSFETs present in Single Phase Matrix Converter (SPMC). Pulse Width Modulation (PWM) pulse is generated by the controller to trigger the gate terminal of MOSFETs. The frequency is varied by controlling the time of applying pulse to the gate of the MOSFETs.

The Micro-Controller output pins which generate gate signals for the MOSFETs cannot be directly connected to the gate terminal of the power device. If it so connected, there is a chance for the back flow of high voltage from the SPMC circuit, that may damage the Controller. In addition, the gate signal from the PIC controller may be weak that it cannot trigger a MOSFET. So it has to be amplified by gate driver circuit.

3.2. CONTROL AND DRIVER CIRCUIT:

The design circuit of control and driver circuit is shown in Fig.3.1. The input Ac supply (18 V) is given to Zero crossing Detector (ZCD-LM358) through an opto-transistor (MCT2E). The ZCD converts the input AC supply into low voltage square pulses to analyze the zero crossing of input sine wave. The output of ZCD is given to input port B (pin33) of the PIC controller to feed the zero crossing data to the controller. When the interrupt is high the controller generates timing pulses for the required output frequency. A 10 kHz PWM pulse is being generated at output port C (pin 17) and output timing pulses are generated at port B (pin 34, 35, 36, 37). Now the high frequency PWM pulse and timing pulses are multiplexed by AND gate (7408). Then the multiplexed output signal is given to corresponding power switching device through opto-transistor.

3.2.1. CIRCUIT DIAGRAM

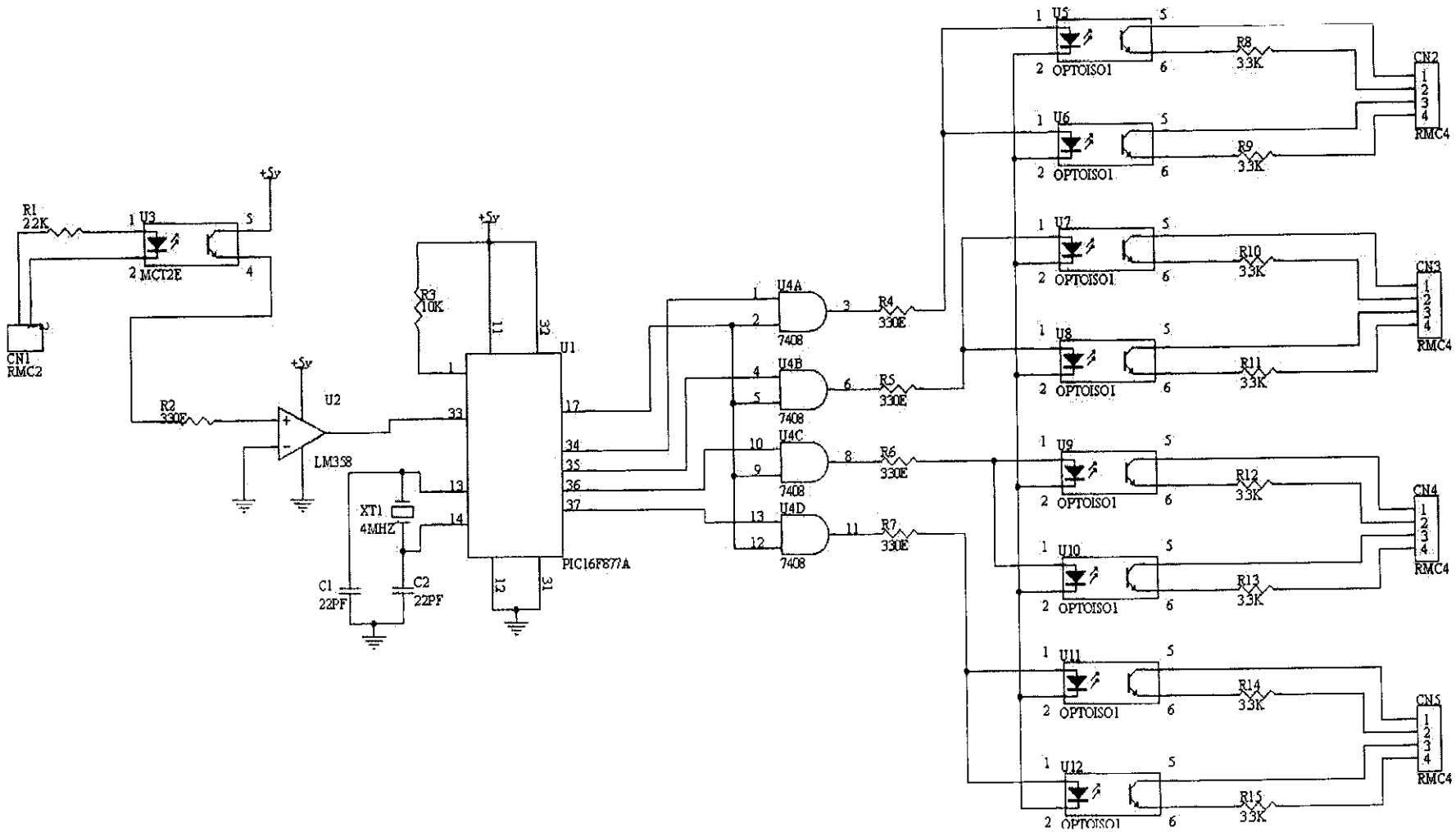


Fig.3.1. Control and Drive Circuit

3.2.2. PIC Micro-Controller:

The microcontroller that has been used for this project is from PIC series (16F877A).PIC stands for *PERIPHERAL INTERFACE CONTROLLER*. It has been first coined by Microchip microcontrollers. PIC Micro-controller's posses an array of features that make them attractive for a wide range of applications. PIC microcontroller is the first RISC based microcontroller fabricated in CMOS (complimentary metal oxide semiconductor) that uses separate bus for instruction and data allowing simultaneous access of program and data memory. The main advantage of CMOS and RISC combination is low power consumption resulting in a very small chip size with a small pin count. The main advantage of CMOS is that it has immunity to noise than other fabrication techniques.

PIC-16F877A:

Various Controllers offer different kinds of memories. EEPROM, EPROM, FLASH etc. are some of the memories of which FLASH is the most recently developed. Technology that is used in pic16F877 is flash technology, so that data is retained even when the power is switched off. Easy Programming and Erasing are other features of PIC 16F877.

PIC START PLUS PROGRAMMER:

The PIC start plus development system from microchip technology provides the product development engineer with a highly flexible low cost CONTROLLER design tool set for all microchip PIC micro devices. The PIC start plus development system includes PIC start plus development programmer and MPLAB.

The PIC start plus programmer gives the product developer ability to program user software in to any of the supported Controllers. The PIC start plus software running under MPLAB provides for full interactive control over the programmer.

3.2.2.1. SPECIAL FEATURES OF PIC CONTROLLER:

CORE FEATURES:

- High-performance RISC CPU
- Only 35 single word instructions to learn
- All single cycle instructions except for program branches which are two cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle
- Up to 8K x 14 words of Flash Program Memory,
  Up to 368 x 8 bytes of Data Memory (RAM)
  Up to 256 x 8 bytes of EEPROM data memory
- Pin out compatible to the PIC16C73/74/76/77
- Interrupt capability (up to 14 internal/external
- Eight level deep hardware stack
- Direct, indirect, and relative addressing modes
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC Oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options
- Low-power, high-speed CMOS EPROM/EEPROM technology
- Fully static design
- In-Circuit Serial Programming (ICSP) via two pins
- Only single 5V source needed for programming capability
- In-Circuit Debugging via two pins
- Processor read/write access to program memory
- Wide operating voltage range: 2.5V to 5.5V
- High Sink/Source Current: 25 mA
- Commercial and Industrial temperature ranges
- Low-power consumption:

< 2mA typical @ 5V, 4 MHz

20mA typical @ 3V, 32 kHz

< 1mA typical standby current

PERIPHERAL FEATURES:

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler, can be incremented during sleep via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules

  Capture is 16-bit, max resolution is 12.5 ns,

  Compare is 16-bit, max resolution is 200 ns,

  PWM max. Resolution is 10-bit
- 10-bit multi-channel Analog-to-Digital converter
- Synchronous Serial Port (SSP) with SPI. (Master Mode) and I2C. (Master/Slave)
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with 9- Bit addresses detection
- Brown-out detection circuitry for Brown-out Reset (BOR)

3.2.2.2. PWM MODE (PWM):

In pulse width modulation mode, the CCPx pin produces up to a 10-bit resolution PWM output. Since the CCP1 pin is multiplexed with the PORTC data latch, the TRISC<2> bit must be cleared to make the CCP1 pin an output.

A PWM output has a time-base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).

PWM PERIOD:

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula

PWM period = [(PR2) + 1] • 4 • TOSC • (TMR2 prescale value)

PWM frequency is defined as 1 / [PWM period].

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set (exception: if PWM duty

Cycle = 0%, the CCP1 pin will not be set)

- The PWM duty cycle is latched from CCPR1L into

CCPR1H

3.2.2.3. PIN DIAGRAM OF PIC 16F877:

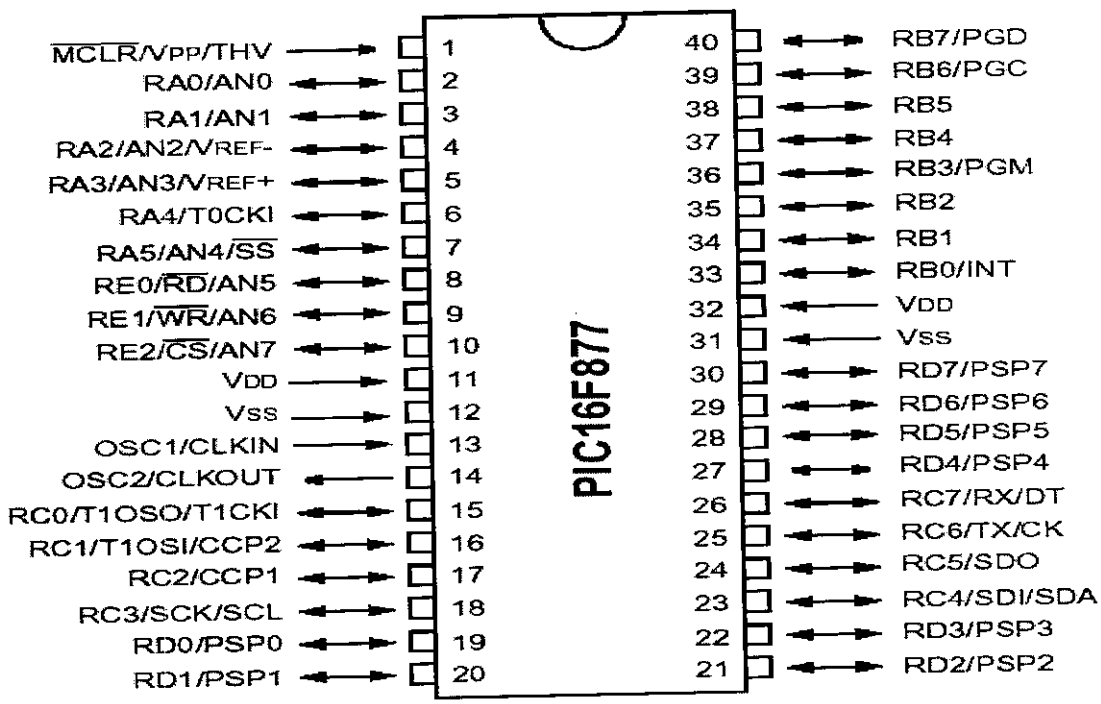


Fig.3.2. Pin Diagram

3.2.2.4. I/O PORTS:

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

PORT B AND TRISB REGISTER:

PORTB is an 8-bit wide bi-directional port. The corresponding data direction register is TRISB. Setting a TRISB bit (=1) will make the corresponding PORTB pin an input, i.e., put the corresponding output driver in a hi-impedance mode. Clearing a TRISB bit (=0) will make the corresponding PORTB pin an output, i.e., put the contents of the output latch on the selected pin. Three pins of PORTB are multiplexed with the Low Voltage Programming function; RB3/PGM, RB6/PGC and RB7/PGD.A single control bit can turn on all the pull-ups. Four of PORT B's pins, RB7:RB4, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (i.e. any RB7:RB4 pin configured as an output is excluded from the interrupt on change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>). This interrupt can wake the device from SLEEP.

PORT C AND THE TRISC REGISTER:

PORT C is an 8-bit wide bi-directional port. The corresponding data direction register is TRISC. Setting a TRISC bit (=1) will make the corresponding PORTC pin an input, i.e., put the corresponding output driver in a hi-impedance mode. Clearing a TRISC bit (=0) will make the corresponding PORTC pin an output, i.e., put the contents of the output latch on the selected pin. PORTC is multiplexed with several peripheral functions. PORTC pins have Schmitt Trigger input buffers.

PORT D AND TRISD REGISTERS:

This section is not applicable to the 28-pin devices. PORTD is an 8-bit port with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output. PORTD can be configured as an 8-bit wide microprocessor Port (parallel slave port) by setting control bit PSPMODE (TRISE<4>). In this mode, the input buffers are TTL.

3.2.2.5. MEMORY ORGANISATION:

There are three memory blocks in each of the PIC16F877 MUC's. The program memory and Data Memory have separate buses so that concurrent access can occur.

PROGRAM MEMORY ORGANISATION:

The PIC16f877 devices have a 13-bit program counter capable of addressing 8K *14 words of FLASH program memory. Accessing a location above the physically implemented address will cause a wraparound.

The RESET vector is at 0000h and the interrupt vector is at 0004h.

DATA MEMORY ORGANISTION:

The data memory is partitioned into multiple banks which contain the General Purpose Registers and the special functions Registers. Bits RP1 (STATUS<6) and RP0 (STATUS<5>) are the bank selected bits.

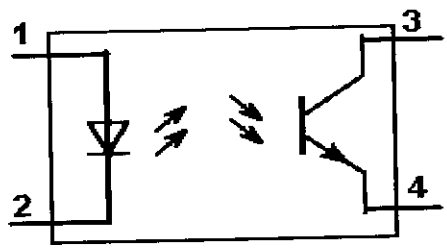
RP1:RP0	Banks
00	0
01	1
10	2
11	3

Each bank extends up to 7Fh (1238 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers, implemented as static RAM. All implemented banks contain special function registers. Some frequently used special function registers from one bank may be mirrored in another bank for code reduction and quicker access.

3.2.3. OPTO COUPLER:

In power electronics, an Opto-isolator (or optical isolator, Opto coupler, photo coupler) is a device that uses a short optical transmission path to transfer a signal between elements of a circuit, typically a transmitter and a receiver, while keeping them electrically isolated — since the signal goes from an electrical signal to an optical signal back to an electrical signal, electrical contact along the path is broken. A common implementation involves a LED and a phototransistor, separated so that light may travel across a barrier but electrical current may not. Unlike a transformer, the Opto-isolator allows for DC coupling and generally provides significant protection from serious over voltage conditions in one circuit affecting the other. With a photodiode as the detector, the output current is proportional to the amount of incident light supplied by the emitter.

For this project, Opto coupler isolation technique is adopted.



3.2.3.1. PIN DIAGRAM (MCT2E):

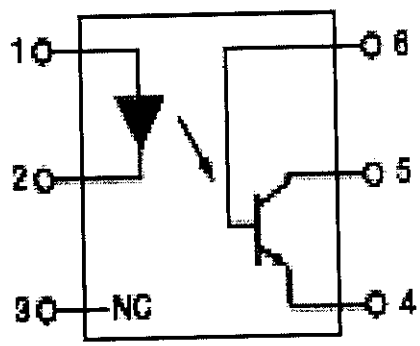


Fig.3.3. Schematic representation

1. Anode of ILED
2. Cathode of ILED
3. No connection
4. Emitter of npn photo-transistor
5. Collector
6. Base

3.2.3.2. OPTO-COUPLER ISOLATION:

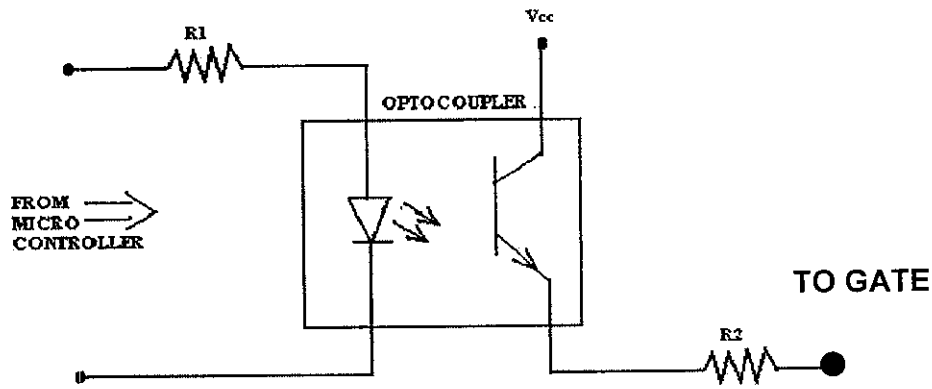


Fig. 3.4 Opto-isolator circuit

The infrared LED terminals are connected to the output port pin of the Micro-controller. The phototransistors base terminal is focused from the light emitted by the ILED. The collector terminal of the NPN phototransistor is conne cted with a separate supply V_{CC} and the emitter is connected to the gate of the MOSFET through a resistor as shown in the fig. 3.4.

WORKING:

The infrared light emitting diode (ILED) is connected to the output port pin of the microcontroller in which the gate signal is generated. The base of NPN transistor is left free. The collector terminal is supplied by the separate source voltage V_{CC} (+5V). The gate of the MOSFET is connected to the emitter of the phototransistor.

When the output pin of the Micro-controller is in HIGH state, the infrared LED glows which activates the base of the phototransistor. After the number of free electrons

presents in the base crosses a particular range, the photo transistor is triggered and the supply V_{CC} at the collector is connected to the emitter of the transistor. When Micro-controller output goes to LOW state, the ILED is turned off and the phototransistor is triggered OFF. Thus the emitter is not connected to the collector supply (V_{CC}).

Since there is no physical contact between the power circuit and the Micro-controller circuit, perfect isolation is achieved by this opto-coupler triggering circuit.

3.3.4. AND GATE:

Logic gates are the basic elements that make up a digital system. The AND gate performs logical multiplication and may have two or more inputs and a single output as shown in Fig. 3.5. However, an AND gate can have any number of inputs greater than one. The operation of AND gate is such that the output is HIGH only when all of the inputs are HIGH. When any of the inputs are LOW, the output is LOW. The type of AND gate used in this project is quad 2-input AND gate (SN74LS08).

3.3.4.1. PIN CONFIGURATION:

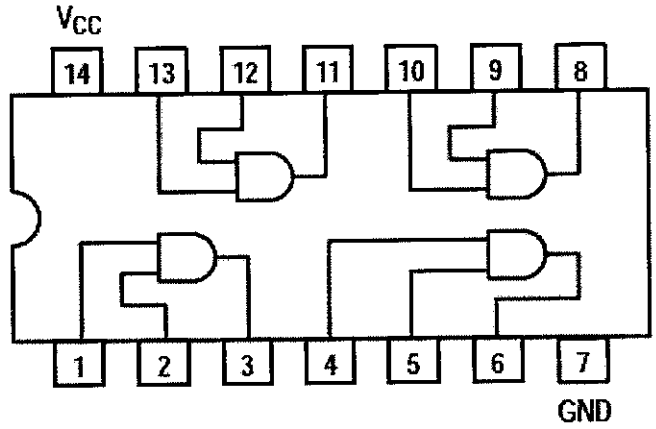


Fig.3.5.Pin Diagram of 7408

3.3. SINUSOIDAL PULSE WIDTH MODULATION (SPWM):

The Sinusoidal Pulse Width Modulation (SPWM) is a well known wave shaping technique in power electronics as illustrated in Fig. 3.6.

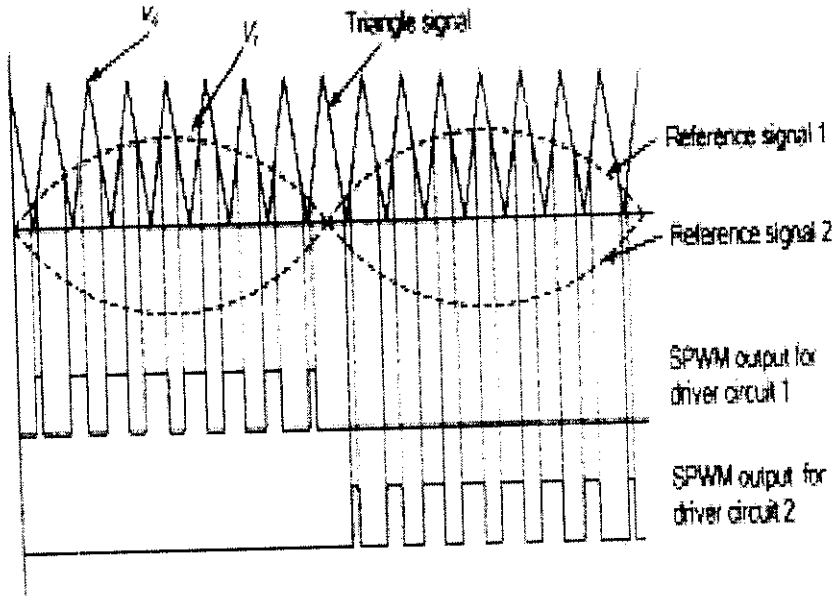


Fig. 3.6. Formation of SPWM

For realization, a high frequency triangular carrier signal, V_c, is compared with a sinusoidal reference signal, V_r of the desired frequency. The crossover variations to be made points are used to determine the switching instants. The magnitude ratio of the reference signal (V_r) to that of the triangular signal (V_c) is known as the modulation index (m_i). The magnitude of fundamental component of output voltage is proportional to m_i. The amplitude V_c, of the triangular signal is generally kept constant. By varying the modulation index, the output voltage could be controlled.

3.4. CONCULSION:

The operating speed of PIC (16F877A) Micro-Controller is very high (DC-20 MHz clock input) and also it has special features like 100,000 erase/write cycle Enhanced Flash program memory and 1,000,000 erase/write cycle Data EEPROM memory in comparison with other controller. Due to the above reason PIC (16F877A) is appropriate in this project. The data sheet for opto-transistor (MCT2E) and PIC (16F877A) is given in Appendix 3 and 4.

CHAPTER 4

SINGLE PHASE MATRIX CONVERTER

4. SINGLE PHASE MATRIX CONVERTER

4.1. INTRODUCTION:

Single Phase Matrix Converter (SPMC) is the main part of the project which is a power electronic converter circuit to convert Single phase AC power at one frequency to AC power at another frequency by AC to AC conversion without an intermediate conversion link. The frequency of the input AC supply can be varied according to the user input to the frequency control switch and the output frequency can be above or below the input supply frequency. In this project the input frequency (50 Hz) is converted into 25 Hz and 100 Hz of output frequency.

4.2 PRINCIPLE OF OPERATION:

The Single-phase matrix converter diagram is shown in figure 4.1. In this topology 4 bi-directional switches are used.

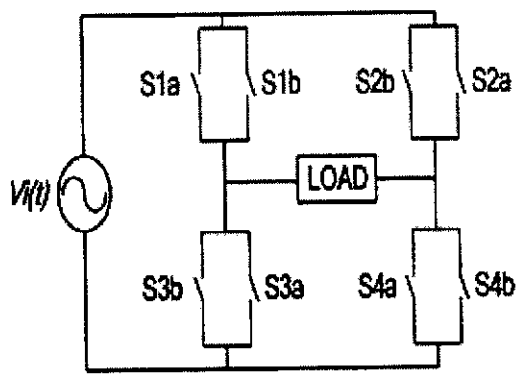


Fig. 4.1.SPMC circuit configuration

Each switches are conducting current in both directions, the main purpose of single phase matrix converter is one input frequency is converted to synthesize multiple frequency of (say 50Hz, 100Hz and 150Hz) using pulse width modulation technique. In this paper is to describe blocking forward and reverse voltages. The individual power switches using IGBTs are as in Fig. 4.2.

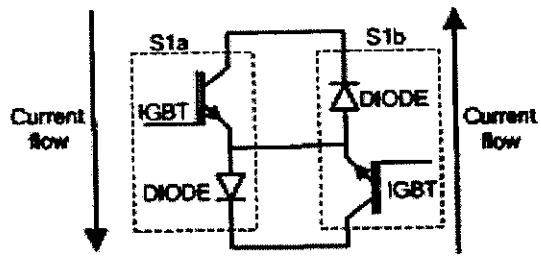


Fig. 4.2 Bidirectional switch module

The input and output voltage of the SPMC is given by

1. $V_i(t) = \sqrt{2}\, V_i \sin \omega_i t$
2. $V_o(t) = \sqrt{2}\, V_o \sin \omega_o t$

Loads represents in $V_o(t) = Ri_o(t) + L\, i_o(t)/dt$

Subscript i denote input, while o denotes output

Driver circuits are designed to generate the SPWM patterns that are used to control the power switches, comprising MOSFETs in the SPMC circuit. The switching angles of the 4 bi-directional switches sij (i = 1,2,3,4 and j = a, b) where 'a' and 'b' are representing driver one and two Vi (t) respectively. The following rules are then applied.

4.2.1. SWITCHING STRATEGIES

Stage 1:

At any time't', only two switches s_{ij} (i = 1, 4 and j = a) will be in 'ON' state and conduct the current flow during positive cycle of input source (state 1) in figure 4.3.

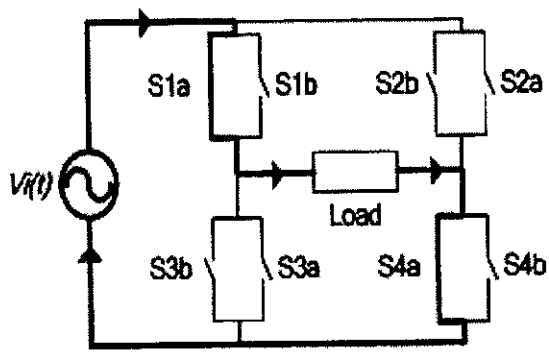


Fig. 4.3. State 1 (Positive Cycle)

Stage 2:

At any time't' only two switches s_{ij} (i = 1, 4 and j = b) will be in 'ON' state and conduct the current flow during negative cycle of input source (state 2) in figure 4.4.

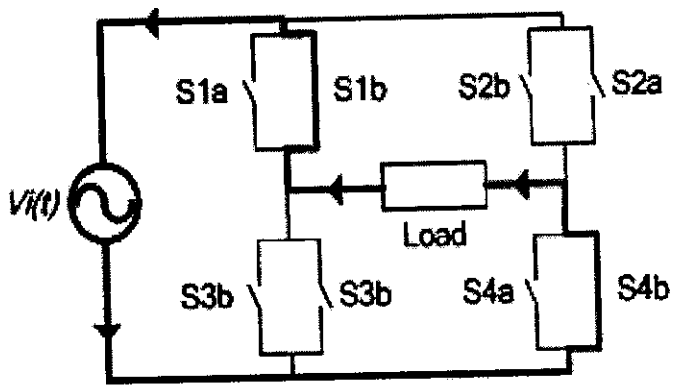


Fig. 4.4. State 2 (Negative Cycle)

Stage 3:

At any time't' only two switches S_{ij} (i = 2, 3 and j = b) will be in 'ON' state and conduct the current flow during positive cycle of input source (state 3) in figure 4.5.

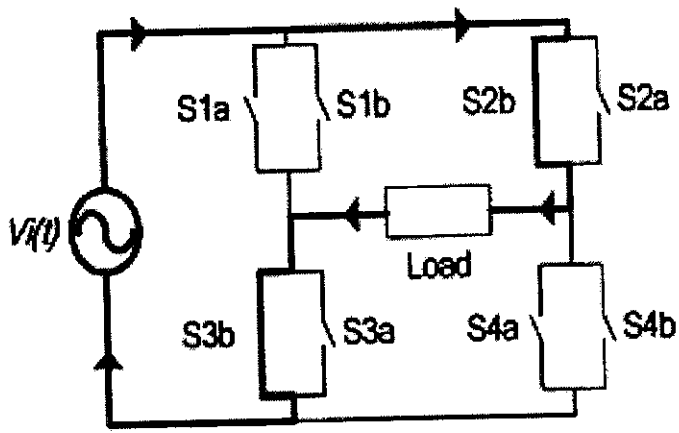


Fig. 4.5. State 3 (Positive Cycle)

Stage 4:

At any time't' only two switches s_{ij} (i = 2, 3 and j = a) will be in 'ON' state and conduct the current flow during negative cycle of input source (state 4) in figure 4.6.

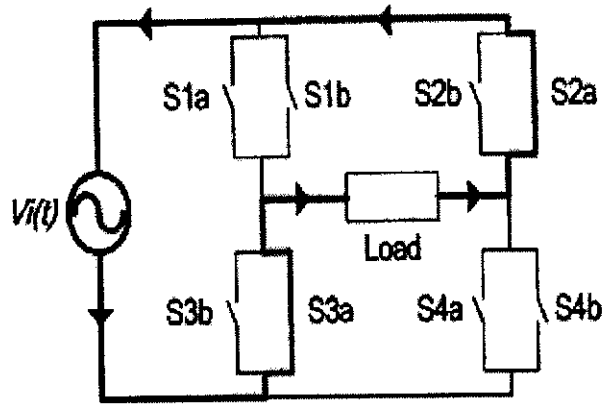


Fig. 4.6. State 4 (Negative Cycle)

4.3. POWER MOSFET:

The MOSFET device belongs to the unipolar device family, because it uses only the majority carriers in conduction. It is the fastest power switching device, with switching frequency >MHz, and with voltage power ratings up to 600 V and current rating as high as 40 A. MOSFET's are becoming popular in low to medium power applications and high frequency power electronic circuits, since the turn-on time is very less. In the case of transistor secondary breakdown takes place. But in the case of MOSFET's, it does not have the problem of secondary breakdown, as it operates in the safe operating area. Fig. 4.7 shows the symbol of n-channel enhancement-mode MOSFET.

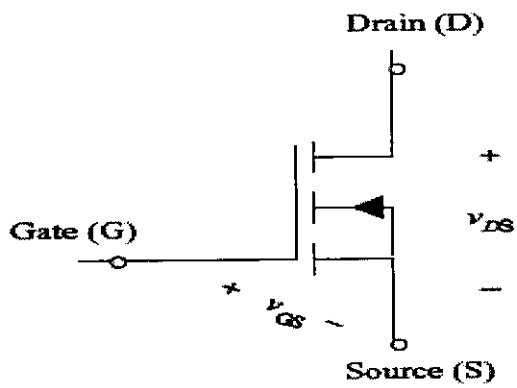


Fig.4.7. power MOSFET symbol

4.3.1. STATIC CHARACTERISTICS:

The V-I characteristics of MOSFET is shown in fig.4.8. The source terminal is common between the input and output of the MOSFET. The output characteristics, i.e. drain current i_D as a function of drain to source voltage V_{DS} with the gate to source voltage V_{GS} as a variable parameter. The saturation, cut-off and ohmic regions of the characteristics are shown in fig. 4.8. In the power electronic applications where the MOSFET is used as switch, the must be operated in the cut-off and ohmic region when turned off and on respectively. The operation in the saturation region should be avoided to reduce the power dissipation in the on state.

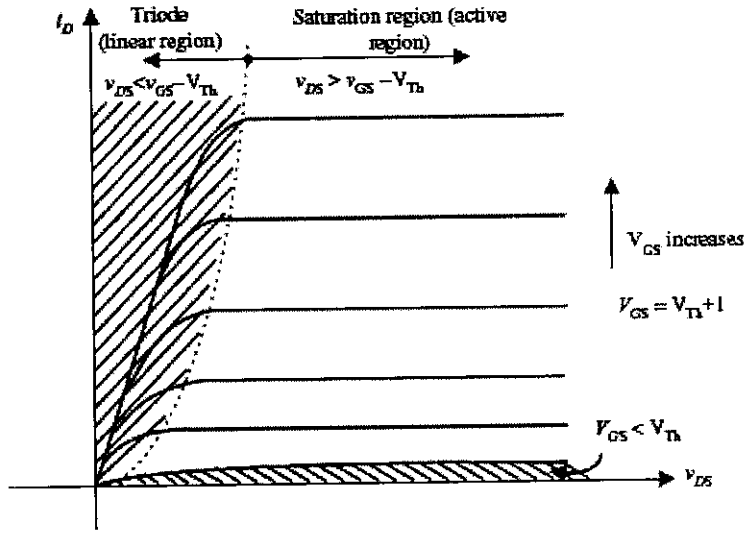


Fig. 4.8. V-I characteristics of n-channel MOSFET

4.3.2. SWITCHING CHARACTERISTICS:

The switching characteristics of a power MOSFET are determined largely by various capacitances inherent in its structure. To turn the device on and off the capacitances have to be charged and discharged, the rate at which this can be achieved is dependent on the impedance and the current sinking/sourcing capability of the drive circuit. Temperature has only a small effect on device capacitances therefore switching times are independent of temperature. The internal capacitances are shown in fig. 4.9.

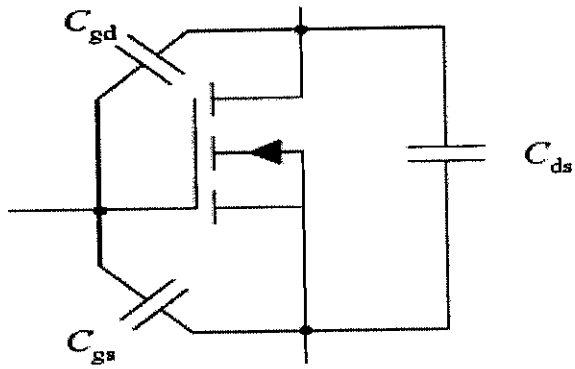


Fig.4.9. Internal capacitances of MOSFET

4.3.2.1. MOSFET TURN-ON CHARACTERISTICS:

The turn-on behavior of the MOSFET is shown in fig.4.10. As shown in this figure, the gate drive voltage changes in step function manner from 0 to V_{GG} which is above the threshold voltage $V_{GS\,(th)}$. During the turn on delay time t_d (on) the gate-source voltage V_{gs} rises from 0 to $V_{Gs\,(th)}$ in fashion similar to an RC circuit. This is due to the resistance in the current path in addition to the equivalent input MOSFET capacitance (C_{gs} and C_{gd}). The rise time constant is given by $t_1=R_G\,(C_{gs} + C_{gd1})$. Beyond $V_{GS\,(th)}$, V_{gs} keeps rising as before and Ids starts increasing. Once the MOSFET is carrying the full load current I_C, the gate-source voltage becomes temporarily clamped at V_{gs}, I_0. At this point, the gate current will flow through C_{gd} only. As a result, the drain-source voltage starts decreasing until it reaches the drop to the on-state resistance. At this point, the gate-source voltage becomes unclamped and rises again to V_{GG} with a time constant of $t_2=R_G\,(C_{gs}+C_{gd2})$. Note here that there are two values of C_{gd} due to the non-linear nature of this capacitance.

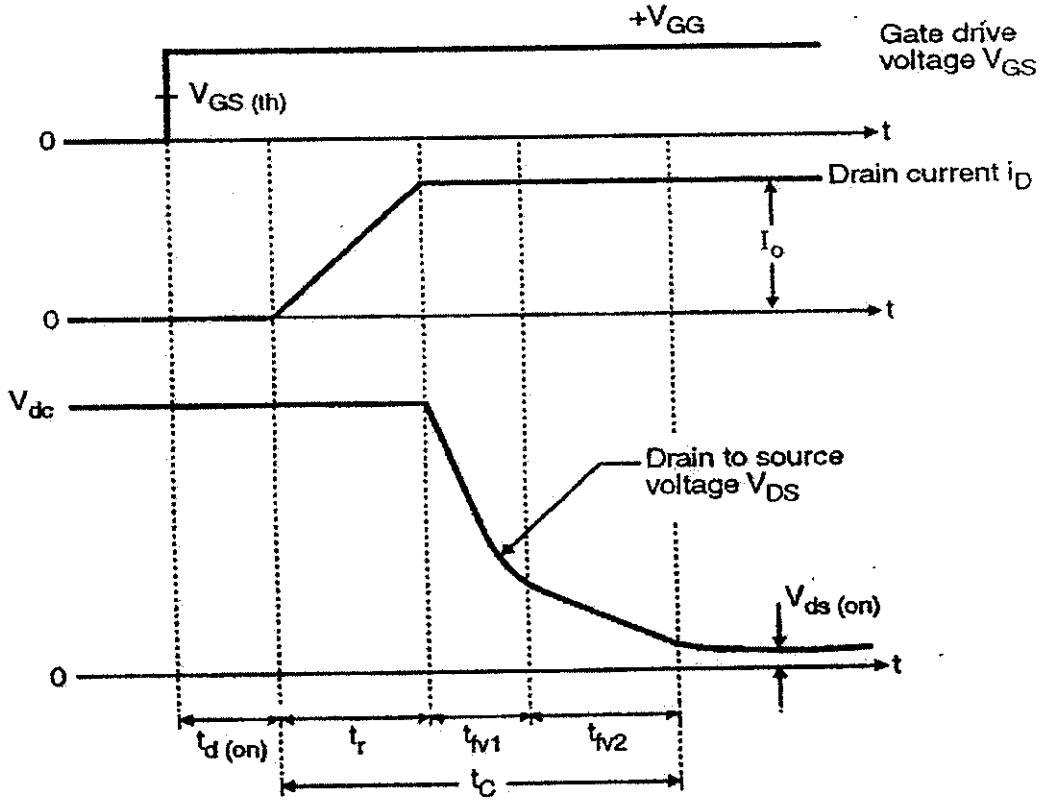


Fig.4.10. Turn-on characteristics of power MOSFET

4.3.2.2. MOSFET TURN-OFF CHARACTERISTICS:

The turn-off of the MOSFET involves the inverse sequence of events that occurred during turn-on. This is shown in Fig.4.11. The turn-off process is initiated by applying a step gate voltage of $-V_{GG}$.

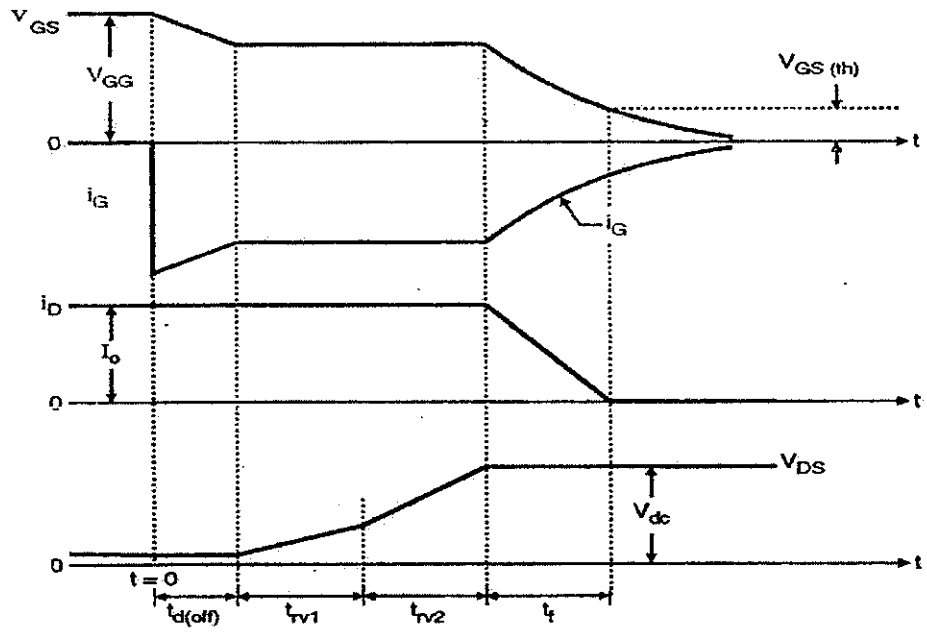


Fig.4.11. Turn-off characteristics of power MOSFET

4.4. CIRCUIT DIAGRAM

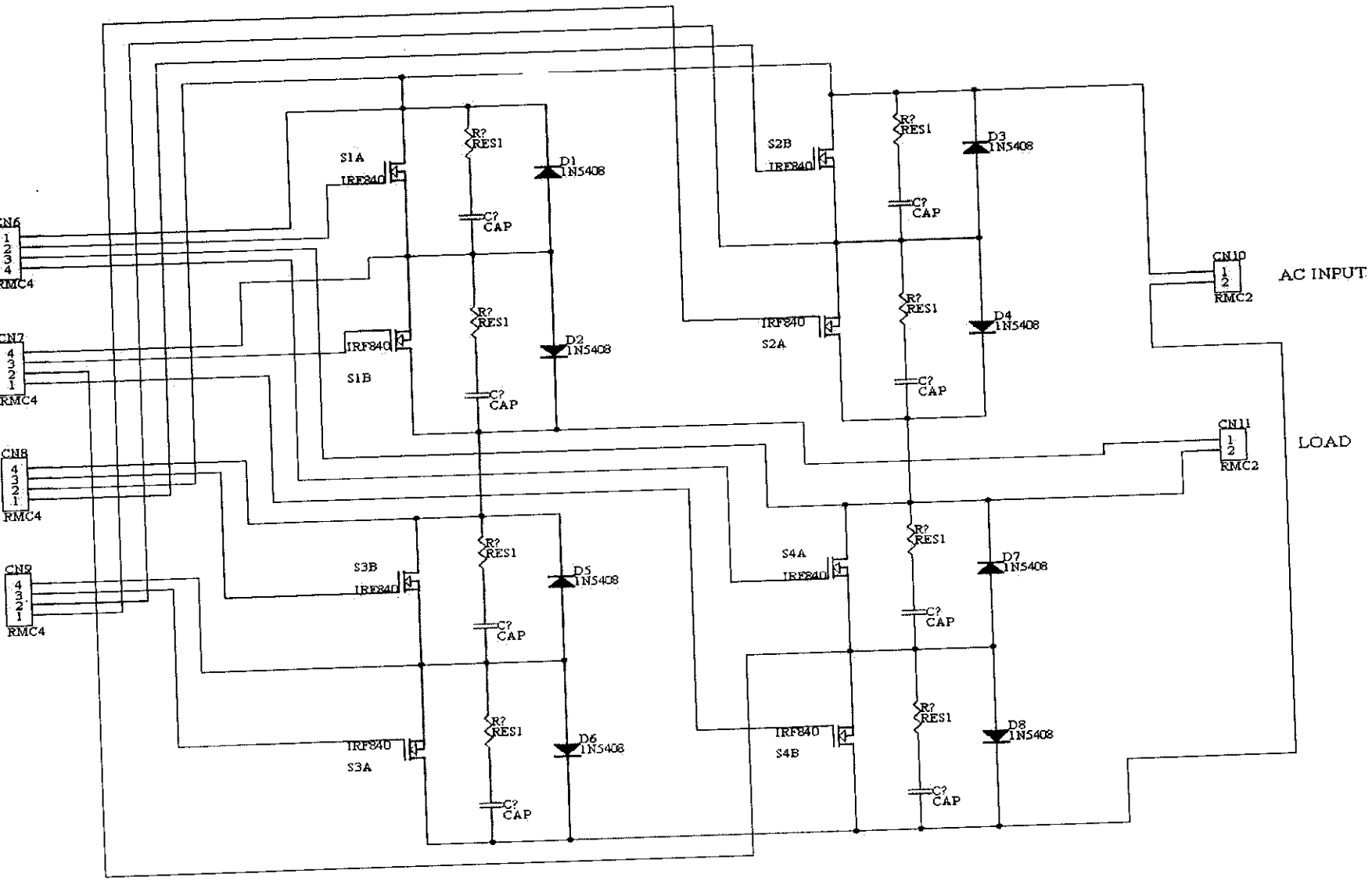


Fig.4.12. SPMC CIRCUIT

4.5. SEQUENCE OF SWITCHING CONTROL:

The sequences of switching are dependent on the time interval and state of the driver circuit, represented by table 4.1 (For the one cycle).

Let's say the output frequency is 50 Hz. To achieve this, when the supply voltage is positive the switch is in state 1 (S1a and S4a are turned ON). On the other hand switching state 2 are used during negative cycle to produce the next half cycle. For other output frequencies, the sequence of switching is similar to the 50 Hz output frequency as listed in table1 with a total of four (4) different switching states, capable of being used in various combinations to produce the desired Phase effect.

TABLE 4.1. SEQUENCE OF SWITCHING CONTROL

Input Frequency	Out put Frequency	Time Interval	State	Switch "ON"
50 Hz	50 Hz	1	1	S1a and S4a
		2	2	S1b and S4b
	100 Hz	1	1	S1a and S4a
		2	3	S2b and S3b
		3	4	S2a and S3a
		4	2	S1b and S4b
	150 Hz	1	1	S1a and S4a
		2	3	S2b and S3b
		3	1	S1a and S4a
		4	2	S1b and S4b
		5	4	S2a and S3a
		6	2	S1b and S4b

4.6. SINUSOIDAL INPUT AND SYNTHESIZED WAVE FORM:

The output frequency is synthesized in multiples of input frequency of 50Hz (say 50Hz, 100Hz, and 150Hz) and the operations are illustrated as in Fig.4.13.

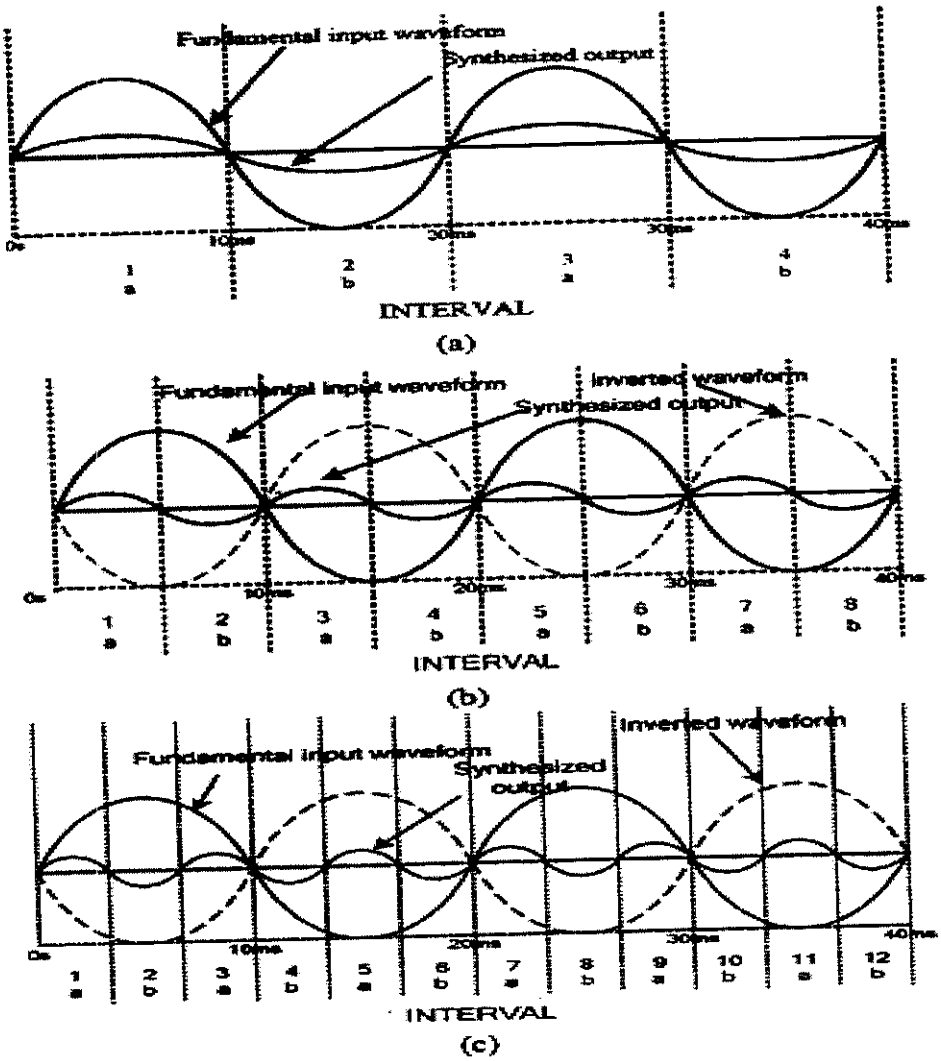


Fig. 4.13. Sinusoidal input and synthesized output

a: 50 Hz b: 100Hz c:150Hz

4.7. CONCULSION:

. Thus SPMC circuit is constructed and by sequence switching of the power switching device the variable output frequency is achieved .Here power MOSFET (IRF 840) is used as switching device. It provides superior switching performance, and withstands high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies. The data sheet for IRF 840 is given in appendix 5.

CHAPTER 5

SOFTWARE IMPLEMENTATION

5. SOFTWARE IMPLEMENTATION

5.1. INTRODUCTION:

New designs of power electronics systems are the norm due to new applications and lack of standardization in specifications is because of varying customer demands. Accurate simulation is necessary to minimize costly repetitions of designs and bread boarding and hence reduce the overall cost and the concept-to-production time.

There are many benefits of simulation in the design process, some of them are listed below here:

- Simulation is well suited for educational purpose. It is an efficient way for designer to Learn how a circuit and its control working.
- It is normally much cheaper to do a thorough analysis than to build the actual circuit in which component stresses are measured. A simulation can discover the possible problems and determine optimal parameters, increasing the possibility of getting the prototype
- New circuit concepts and parameter variation (including tolerances on components) are easily tested. Changes in the circuit topology are implemented at no cost. There is no need for components to be available on short notice.
- Simulated waveforms at different places in the circuit are easily monitored without the hindrance of measurement noise. As switching frequencies increases, the problem of laboratory measurements becomes increasingly difficult. Thus, simulations may become more accurate than measurement
- Destructive tests that cannot be done in the lab, either because of safety or because of costs involved, can easily be simulated. Response to faults and abnormal conditions can also be thoroughly analyzed.

The different Software available in market for simulation studies are:

- PSPICE
- ORCAD
- LABVIEW
- MATLAB
- MULTISIM

The software tool used for the simulation studies is MATLAB SIMULINK.

5.1.1. MATLAB/SIMULINK:

If we choose an equation solver, we must ourselves write differential and algebraic equations to describe various circuit states. The logical expressions and the controller that determine the circuit state. Then these differential/algebraic equations are simultaneously solved as a function of time.

The program MATLAB can easily perform array and matrix manipulations, where for example y=a*b results in y, which equals cell by cell manipulation of two arrays a and b. Similarly to convert a matrix, all one needs to specify is y=inv(x).powerful plotting routines are built in MATLAB also features various libraries, called toolboxes, which can be used to solve particular classes problem. For example, the neural network toolbox enables the simulation of an unlimited number of layers and interconnections.

Simulink is another toolbox for graphical entry and simulation of nonlinear dynamic systems. It consists of a large number of building blocks that enables the simulation of control based system. Some of the other features include seven integration routines and determination of equilibrium points.

MATLAB is widely used in industry. Also such programs are used in the teaching of under graduate courses in control systems and signal processing. Therefore, the students are usually familiar with MATLAB prior to taking power electronics courses.

5.2. DEVELOPING SIMULATION MODEL:

5.2.1. SCHEMATIC OF SPMC

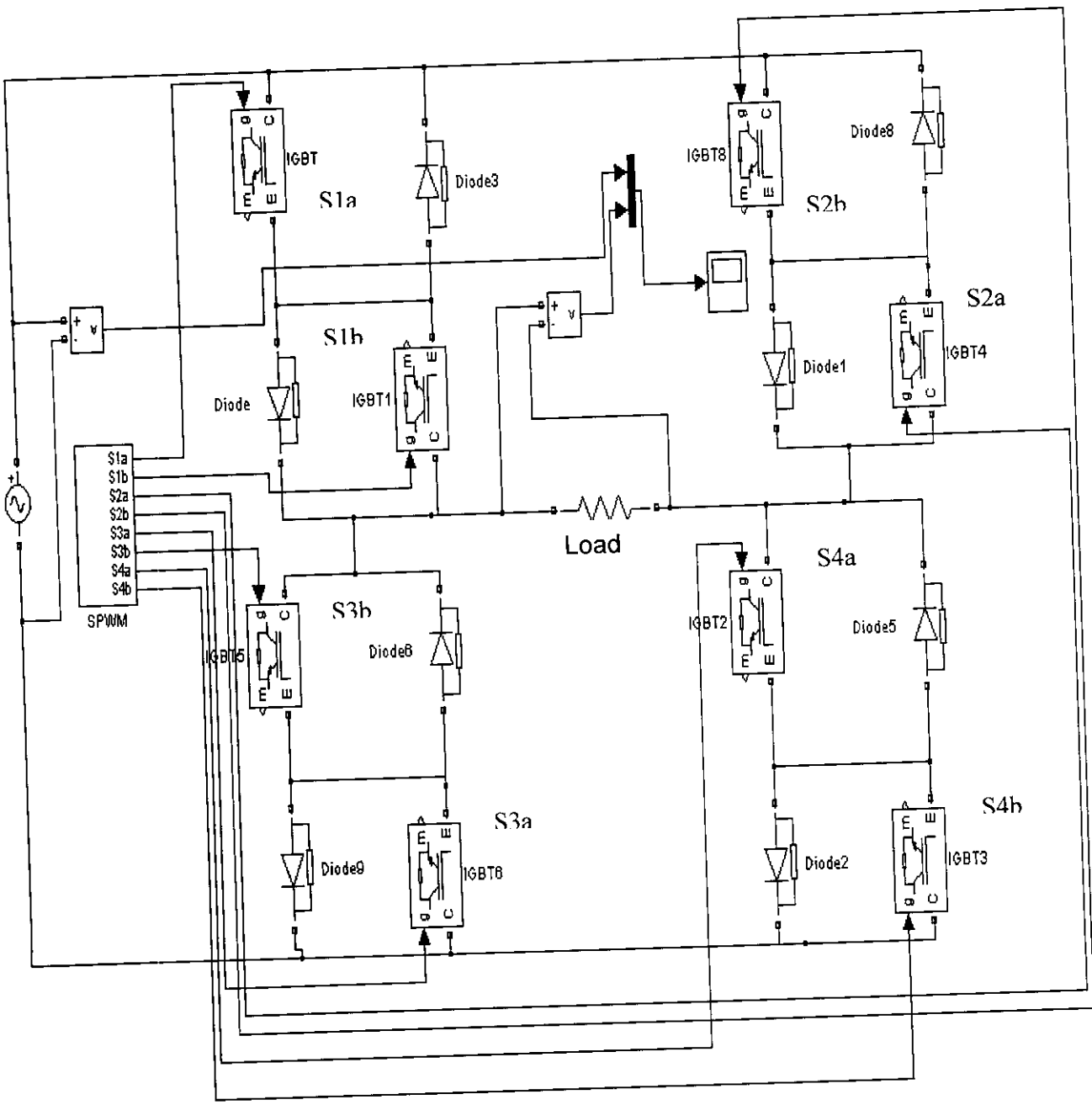


Fig.5.1. Single Phase Matrix Network

5.2.2. SUBSYSTEM OF SPMC NETWORK:

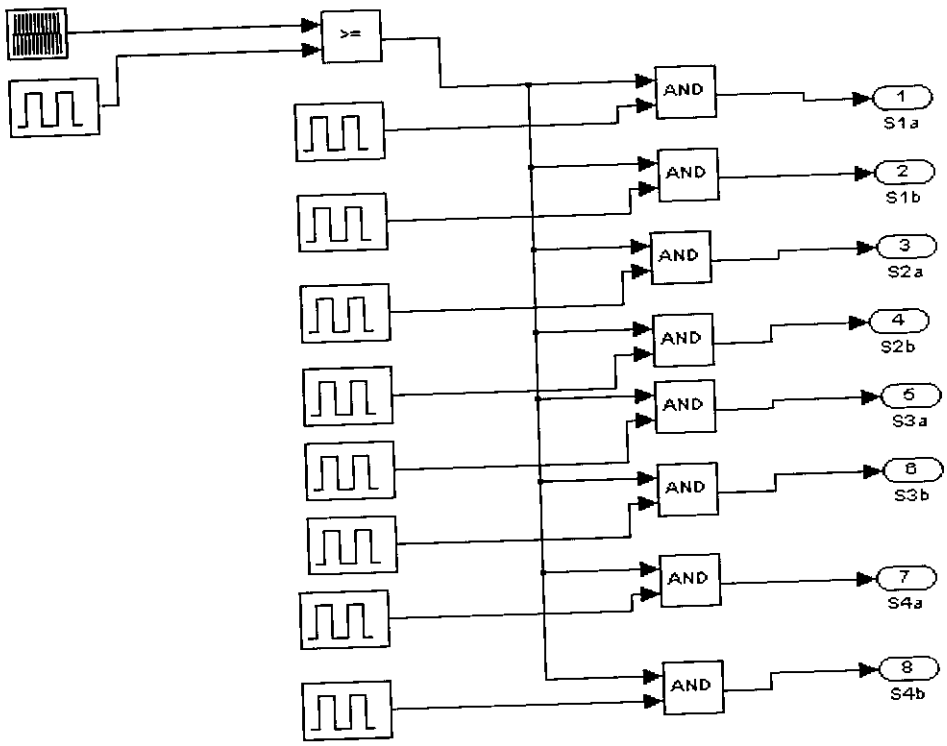


Fig.5.2.Control Circuit

5.2.3. ZERO CROSSING DETECTOR CIRCUIT:

As the switches used in the Single Phase Matrix Network are all ideal switches. So there is no need for Zero Crossing Detector in the simulation model.

5.2.4. DESCRIPTION OF SPMC MODEL:

In the SPMC circuit totally 4 bi-directional switches are being used. Each bi-directional switch consists of two anti-parallel limbs; each limb is a combination of two IGBTs and two Diodes.

5.2.4.1. SEQUENCE OF SWITCHING CONTROL:

In the case of **100 Hz** (output frequency), for the positive half cycles of the input the output is a both positive and negative cycle. The total time period of the output is

10ms.The switches S1a and S4a are conducting in the positive half cycle of the input (0 to 0.005 sec) to get positive output and switches S2b and S3b are conducting in the same positive half cycle (0.005 to 0.01 sec) to get negative output. In the negative half cycle of the input, switches S3a and S2a are conducting (0.01 to 0.015 sec) to get positive output and switches S1b and S4b are conducting (0.015 to 0.02 sec) to get negative output. Similarly for 25 Hz and 150 Hz of output frequency the switching control sequence is shown in table 5.1.

Table 5.1. Time delay for 100Hz Circuit

Switch		Start Time [ms]	End Time [ms]	Total ON [ms]	Pulse width (%)	Delay	
						ms	Sec
S1a	S4a	0	5	5	25%	0	0
S2b	S3b	5	10	5	25%	5	0.005
S3a	S2a	10	15	5	25%	10	0.01
S4b	S1b	15	20	5	25%	15	0.015

Table 5.2. Time delay for 150Hz Circuit

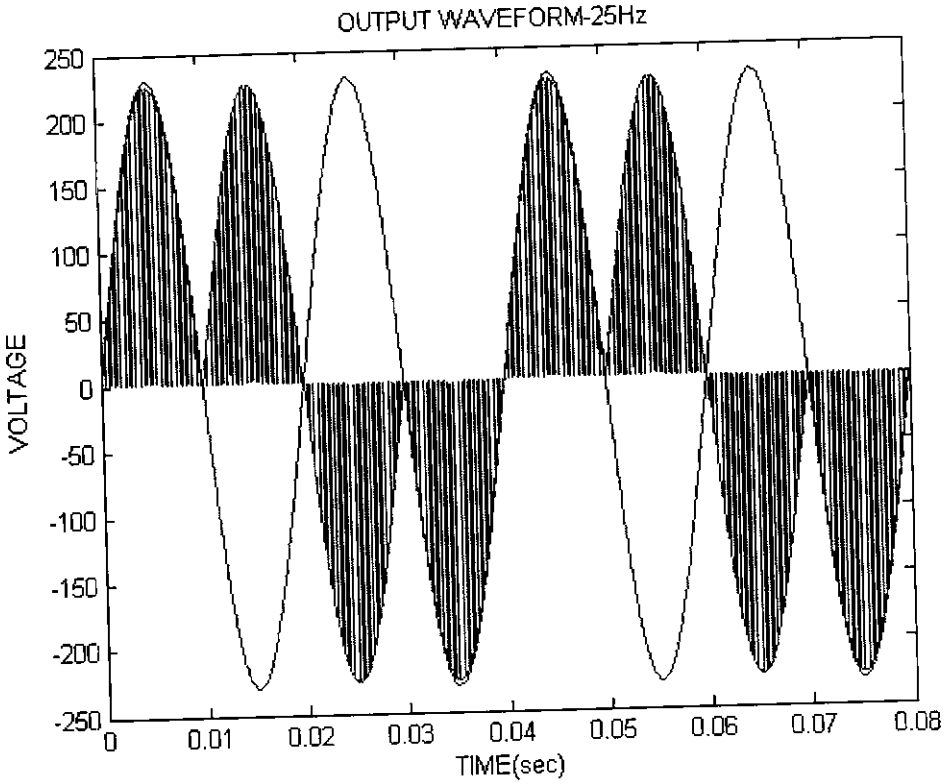
Switch		Start Time [ms]	End Time [ms]	Total ON [ms]	Pulse width (%)	Delay	
						ms	Sec
S1a	S4a	0.00	3.33	3.33	16.66	0.00	0
S2b	S3b	3.33	6.66	3.33	16.66	3.33	0.0033
S1a	S4a	6.66	10.00	3.33	16.66	6.66	0.0066
S4b	S1b	10.00	13.33	3.33	16.66	10.00	0.01
S3a	S2a	13.33	16.66	3.33	16.66	13.33	0.0133
S4b	S1b	16.66	20.00	3.33	16.66	16.66	0.0166

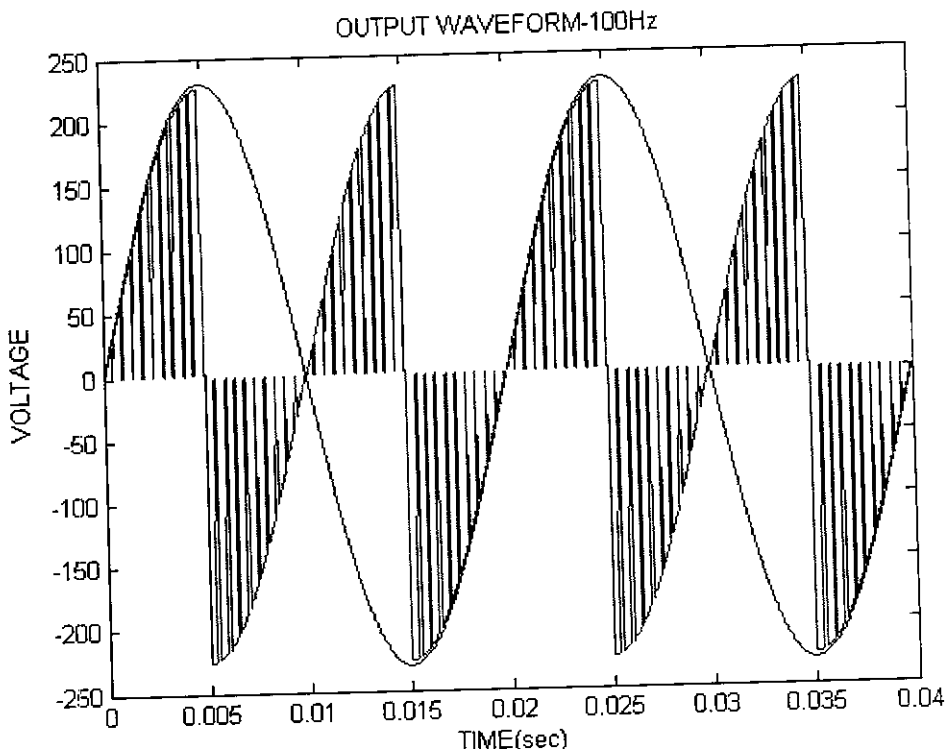
Table 5.3. Time delay for 25Hz Circuit

Switch		Start Time [ms]	End Time [ms]	Total ON [ms]	Pulse width (%)	Delay	
						ms	Sec
S1a	S4a	0	1	1	25%	0	0
S2b	S3b	1	2	1	25%	1	0.01
S3a	S2a	2	3	1	25%	2	0.02
S4b	S1b	3	4	1	25%	3	0.03

5.3. SIMULATION RESULTS:

5.3.1. OUTPUT WAVEFORM :(25,100 Hz)





5.3.2. OUTPUT WAVEFORM—150Hz:

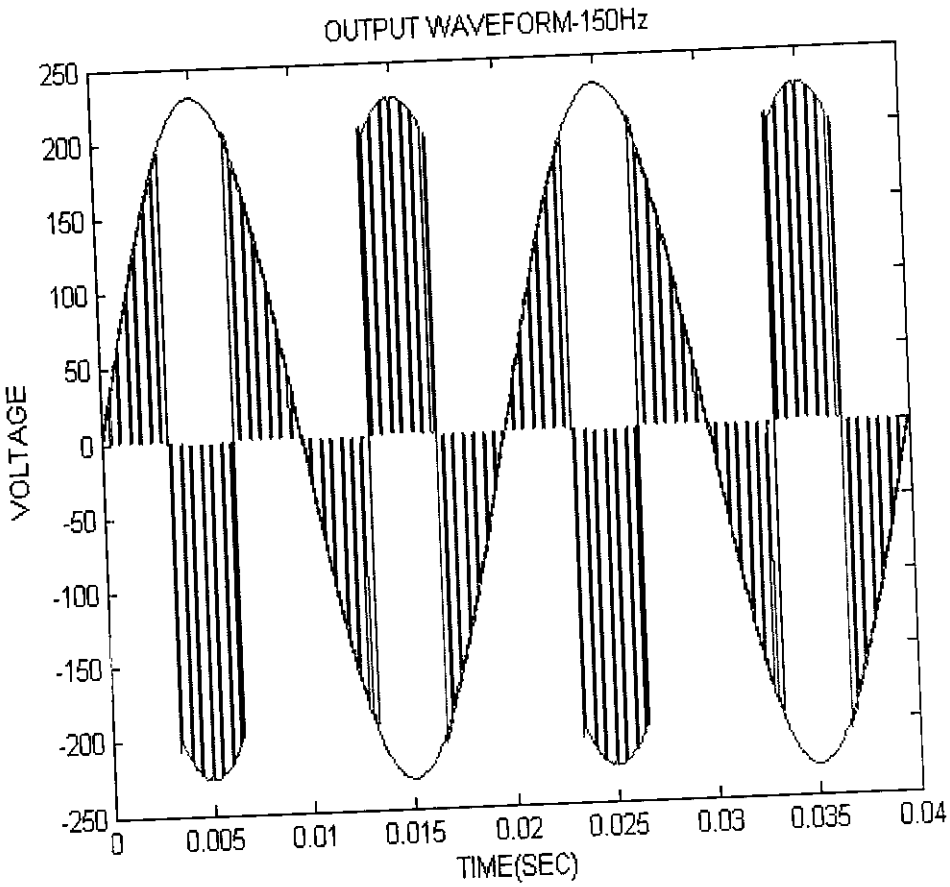


Fig. 5.3. Output waveforms

5.4. CONCULSION:

Thus in simulation model the ideal switching devices are used so harmonics contents are negligible. In comparison with conventional Cyclo-Converter, the bi-directional switches in Matrix topology can allow power to flow in either direction, hence the efficient operation can be achieved in all four quadrants. A matrix of semiconductor switches replaces the rectifier and DC link in the power section of conventional AC drives. With reference to the switching table the expected output waveforms for 25Hz, 100Hz, and 150 Hz are obtained.

CHAPTER 6

HARDWARE IMPLEMENTATION

6. DESIGN AND FABRICATION OF HARDWARE

6.1. INTRODUCTION:

The hardware implementation of the project is generally used to explain how the project is applicable practically in industries and other areas. The objective of this project is converting the fixed input frequency into variable output frequency to control the speed of AC drives and to implemented this in hardware.

6.2. HARDWARE DESCRIPTION:

The block diagram for the hardware implementation is shown in Fig. 6.1. It consist of

- Zero crossing detector circuit
- Control unit
- Driver circuit
- SPMC circuit

6.2.1. Zero Crossing Detector Circuit:

It is a circuit that converts the input line supply into the low voltage square pulses to analyze the zero crossing of the input sine wave. This circuit is designed with the help of Dual operational amplifier (LM358). The output terminal of the zero crossing detectors is connected to the input port of the Micro-Controller to fed the zero crossing data to the controller.

6.2.2. Control Circuit:

Micro-Controller is used to control the switching sequence of the MOSFETs present in SPMC circuit. PWM pulse is generated by the controller to trigger the gate terminal of MOSFETs . The frequency is varied by controlling the time of applying pulse to the gate of the MOSFETs. The type of controller used in this project is PIC (16F877A) due to its easiness, reliability, cost effective and various other features.

LOCK DIAGRAM:

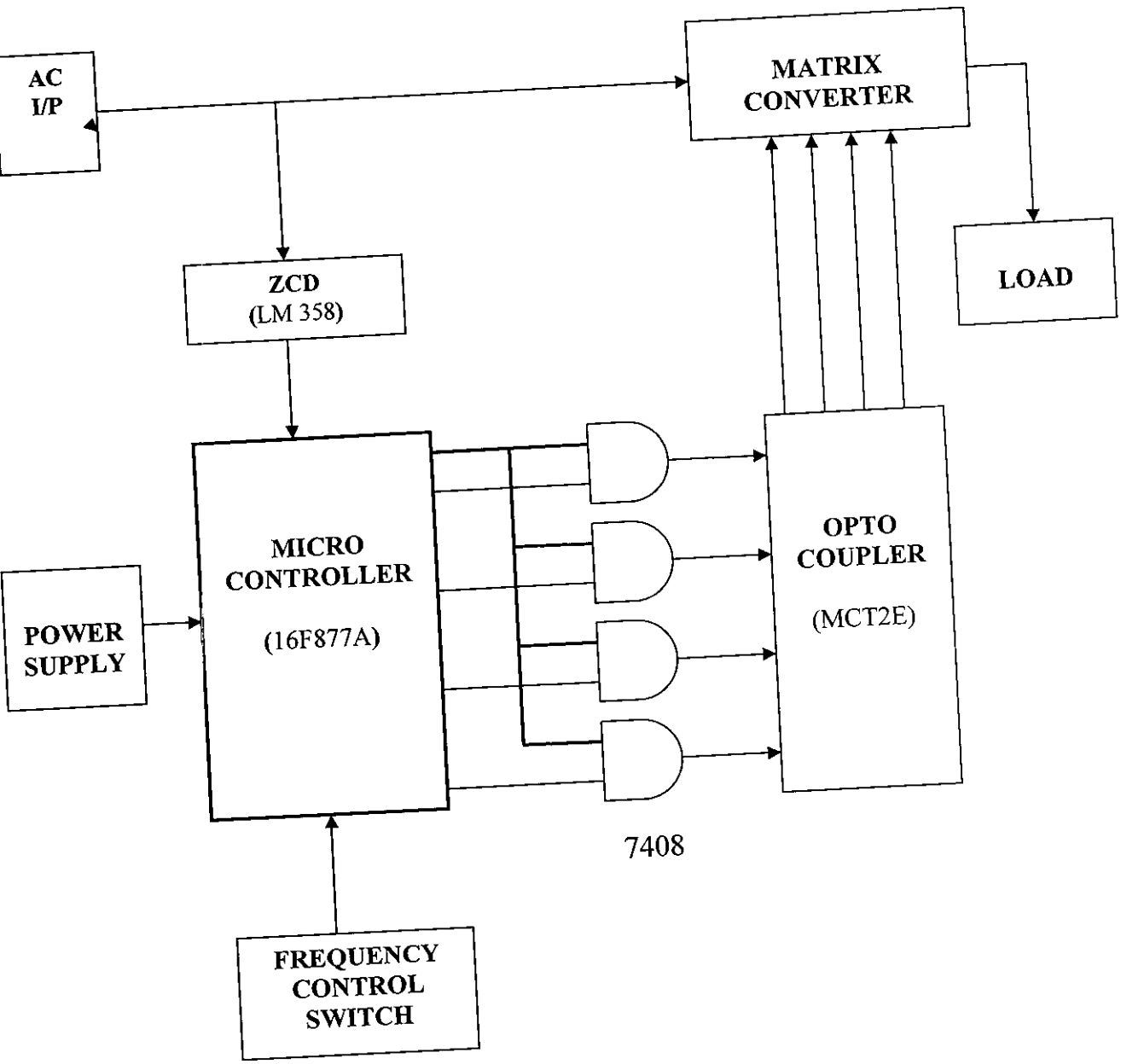


Fig.6.1. Schematic Representation

6.2.3. Driver Circuit:

The Micro-Controller output pins which generate gate signals for the MOSFETs cannot be directly connected to the gate terminal of the power device. If it so connected, there is a chance for the back flow of high voltage from the SPMC circuit, that may damage the Controller. In addition, the gate signal from the PIC controller may be weak that it cannot trigger a MOSFET. So it has to be amplified by gate driver circuit. Opto-transistor (MCT2E) is used in this project for isolating the controller output and the gate terminal of a MOSFET.

6.2.4. Single phase Matrix Converter (SPMC) Circuit:

This is the main part of this project which is a power electronic converter circuit to convert Single phase AC power at one frequency to AC power at another frequency by AC to AC conversion without an intermediate conversion link. The frequency of the input AC supply can be varied according to the user input to the frequency control switch and the output frequency can be above or below the input supply frequency. In this project the input frequency (50 Hz) is converted into 25 Hz and 100 Hz of output frequency.

6.3. POWER SUPPLY MODULE:

6.3.1. INTRODUCTION:

The power supply circuits built using filters, rectifiers, and then voltage regulators. Starting with an ac voltage, a steady dc voltage is obtained by rectifying the ac voltage, then filtering to a dc level, and finally, regulating to obtain a desired fixed dc voltage. The regulation is usually obtained from an IC voltage regulator unit, which takes a dc voltage and provides a somewhat lower dc voltage, which remains the same even if the input dc voltage varies, or the output load connected to the dc voltage changes.

A block diagram containing the parts of a typical power supply and the voltage at various points in the unit is shown in fig 6.2. The ac voltage, typically 120 V rms, is connected to a transformer, which steps that ac voltage down to the level for the desired dc output. A diode rectifier then provides a full-wave rectified voltage that is initially filtered by a simple capacitor filter to produce a dc voltage. This resulting dc voltage

usually has some ripple or ac voltage variation. A regulator circuit can use this dc input to provide a dc voltage that not only has much less ripple voltage but also remains the same dc value even if the input dc voltage varies somewhat, or the load connected to the output dc voltage changes. This voltage regulation is usually obtained using one of a number of popular voltage regulator IC units.

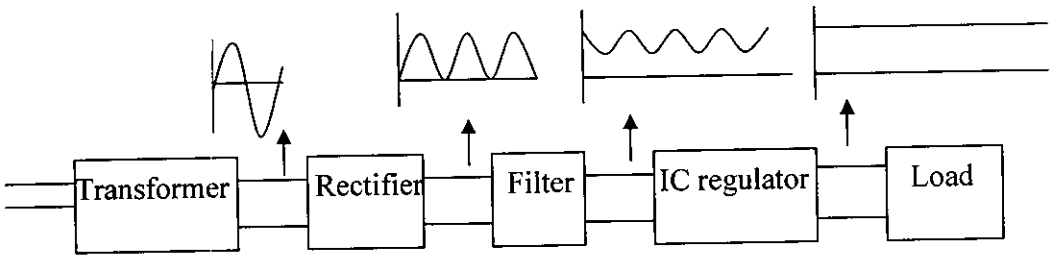


Fig.6.2. Block Diagram

6.3.2. DC REGULATED SUPPLY FOR MICRO-CONTROLLER:

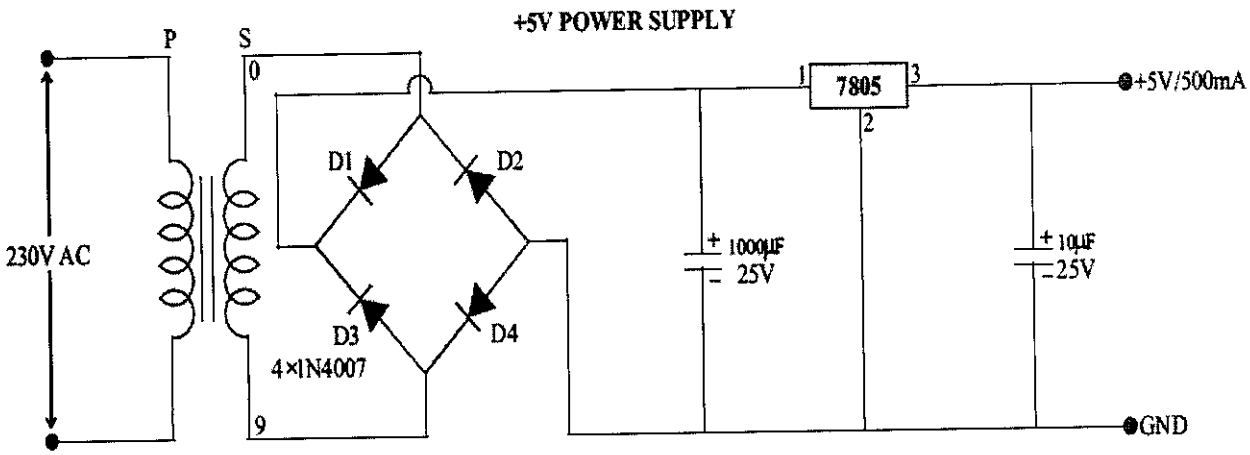


Fig.6.3. power supply circuit

The above figures illustrate the power supply module for Micro-Controller. The Micro-Controller needs a regulated 5V DC supply and power MOSFET is receiving 18 V AC supply directly from step-down transformer.

6.4. PCB LAYOUT:

6.4.1. CONTROL AND DRIVE CIRCUIT:

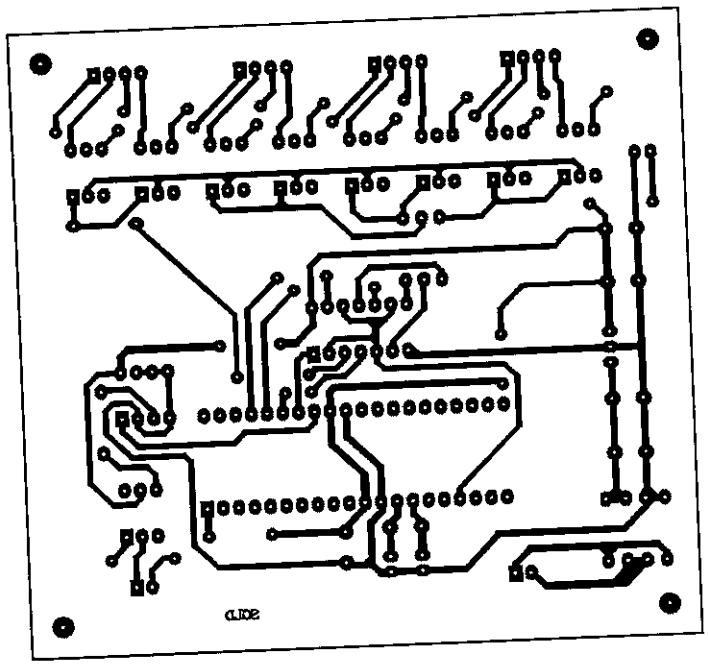


Fig.6.4. PCB layout for control and drive circuit

6.4.2. SPMC MODULE:

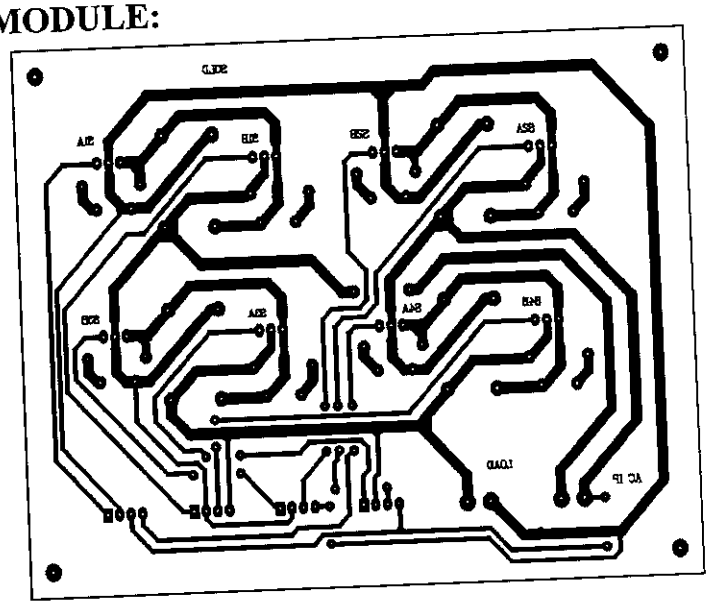
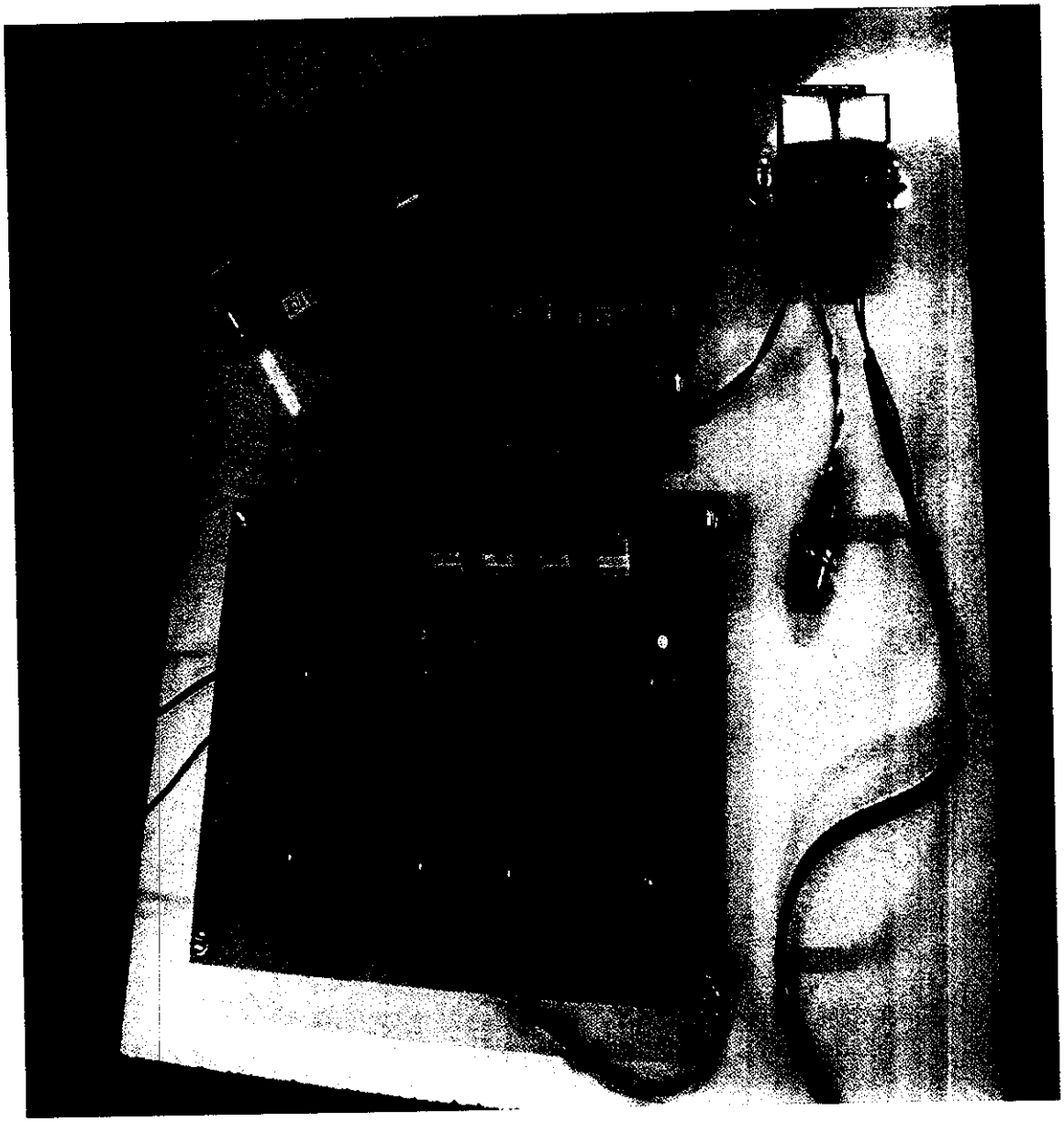


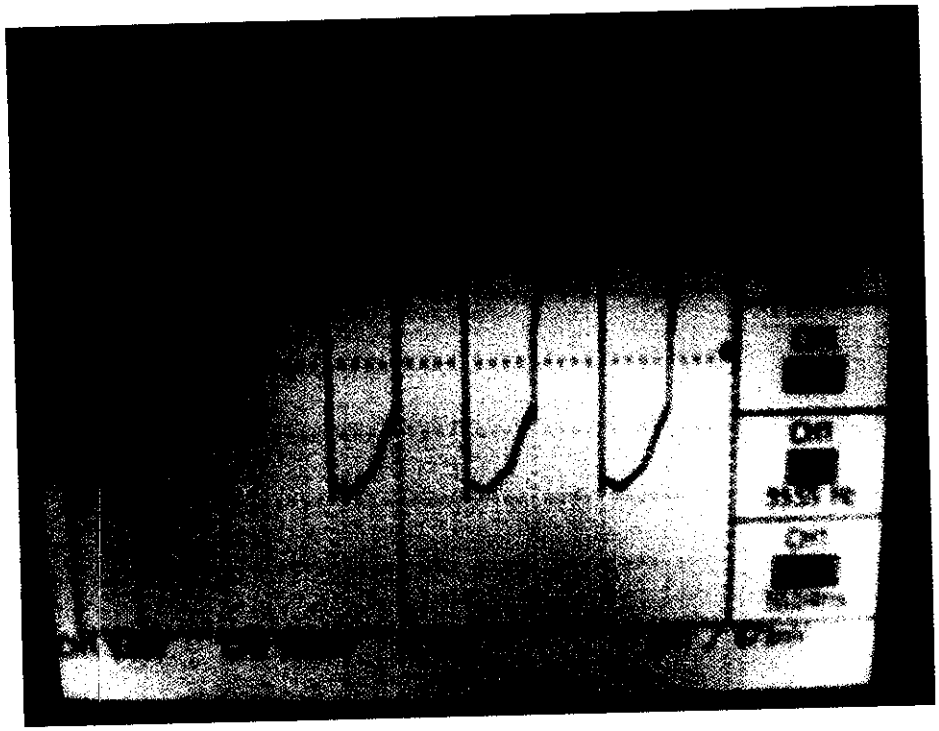
Fig.6.5. PCB Layout for SPMC module

6.5. DEVELOPED SPMC MODULE:

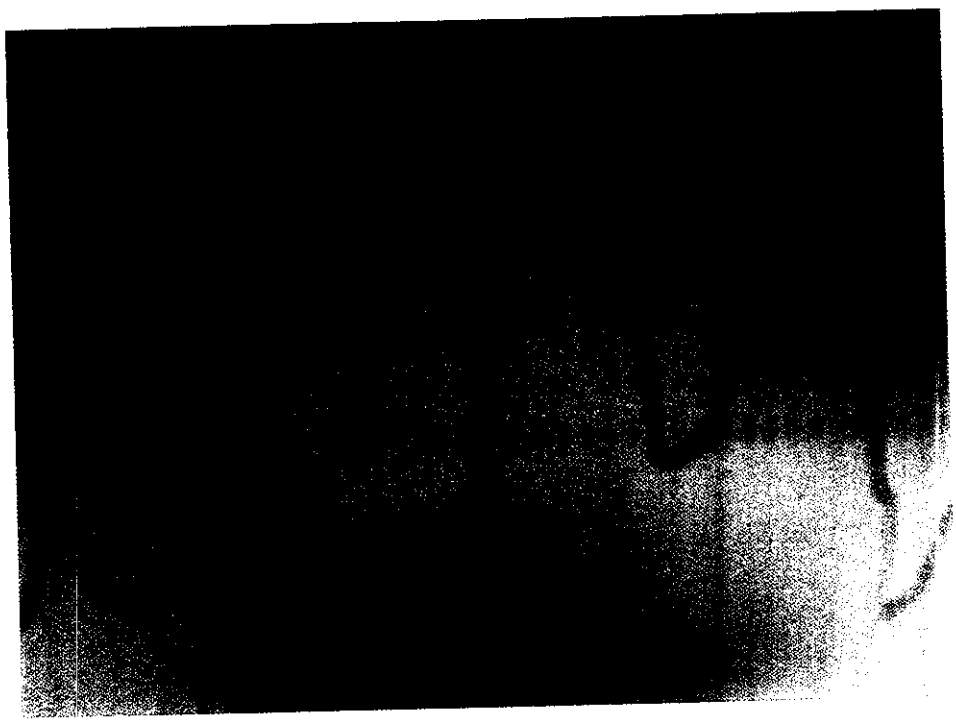


6.6. HARDWARE RESULTS:

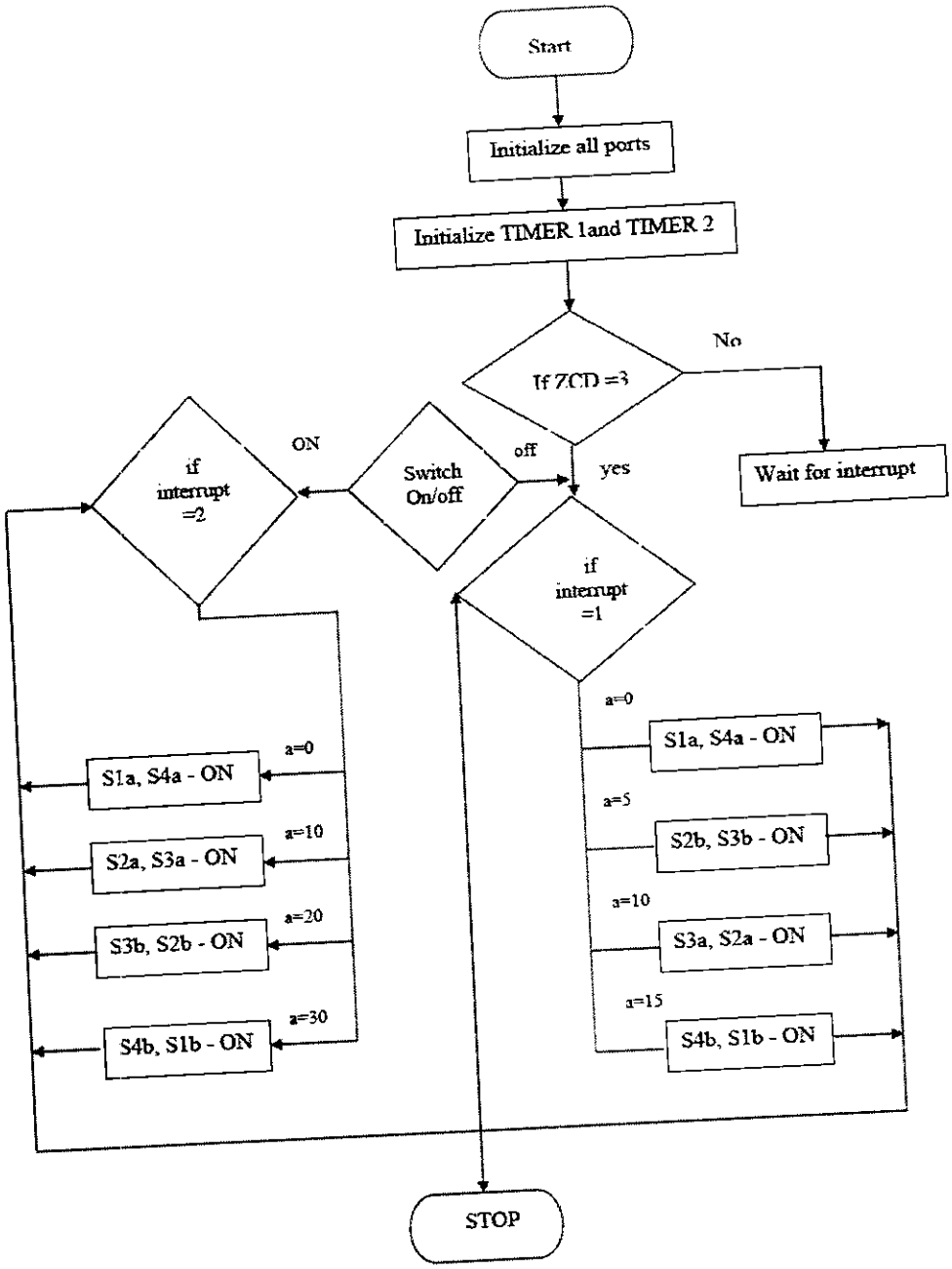
6.6.1. OUTPUT WAVEFORMS- 100Hz



6.6.2. OUTPUT WAVEFORM- 25Hz



6.7. FLOW CHART FOR PWM PULSE GENERATION



6.8. CONCULSION:

Thus the hardware is fabricated and implemented using PIC Controller (16F877A) and output waveforms for 25 Hz, 100 Hz are generated. When compare the hardware results with simulation, the output having slight variation in amplitude. This is because of the variation in the input supply frequency and due to that the time period is lagging for 0.02 seconds in one cycle of total time period. The PIC Controller program coding is given in the Appendix 1.

CHAPTER 7

CONCLUSION AND FUTURE SCOPE

CONCLUSION

For the frequency conversion of single-phase AC supply, Capacitors Rectifier-Inverter module is used. The DC link between the rectifier and the output bridge requires the use of large electrolytic capacitors, occupying lot of space. Advancement of technology replaced the Capacitor Rectifier-Inverter module with the solid-state switches.

In the conventional module of Cyclo – converter, the incoming AC supply is rectified by a diode bridge to produce DC voltage. This output is fed to an AC inverter bridge to produces a variable frequency AC output to drive the motor. The majority of Cyclo-Converter is naturally commutated MOSFET/ IGBT and the maximum output frequency is limited to a value that is only a fraction of input frequency (0-20 Hz output for 50 Hz input). More over the output voltage is present with high order of harmonics.

In this project, this defect of output frequency being fractional of the input frequency is rectified by the new design of Cyclo-Converter i.e., Single Phase Matrix converter (SPMC).Here bidirectional switches provided control of the magnitude and frequency of the generated output voltage/current incorporating PWM technique with reduced switching devices. It has an unlimited output frequency range variation i.e., less than input frequency or above the input frequency ($f_O \leq f_i$ & $f_O \geq f_i$) as it possess static switches with controlled turn on and turn off capability.

Thus designed, fabricated and successfully implemented the Single-phase matrix converter. Here, PWM technique converted the fixed input frequency to variable output frequency using PIC controller.

This project has many advantages such as, the bi-directional switches in Matrix topology can allow power to flow in either direction. Hence the efficient operation can be achieved in all four quadrants when compare with conventional Cyclo-Converter.

Prior to hardware implementation, simulations are performed to predict the behavior. Good agreement is obtained between simulation and laboratory experiments. Results of the SPMC for both the simulation and experiments illustrate that it is feasible to realize the converter as a frequency step-up and step-down converter.

Future scope:

- As observed from the hardware results, the output wave shape of voltage is not a pure sinusoidal waveform. By using suitable wave shaping circuits across the load, the sinusoidal waveform may be obtained
- Since the size and cost of this system is low, the future scope for this project can find in industries. This device can be used for Speed control of high power AC motor drives and also for Variable speed, constant frequency power generation.

APPENDIX

APPENDIX-1

CODING:

```
#include<pic.h>
#define S14A RB1
#define S23B RB3
#define S23A RB4
#define S41B RB2
unsigned char ZC, COUNT=0, LOW,HIGH,TCOUNT;
unsigned int i;

void main()
{
        TRISB=0X01;
        PORTB=0;
        TRISC=0;
        TRISD=0X01;

        OPTION=0X40;
        TMR1L=LOW;
        TMR1H=HIGH;

        PR2=99;
        CCPR1L=0X50;
        CCP1CON=0X0C;
        T2CON=0X04;

        GIE=PEIE=TMR1IE=INTE=1;

        if(ZC==3)
        {
```

```
        INTE=0;
        T1CON=0X01;
        PORTB=0X02;
        while(1)
        {
            if(RD0==1)
            {
                DEBOUNCE();
                TCOUNT++;
                DEBOUNCE();
            }
            if(RD0==0)
            {
                LOW=0XE0;
                HIGH=0XB1;
            }
            else if(RD0==1)
            {
                LOW=0X78;
                HIGH=0XEC;
            }
        }
    }

void interrupt isr()
{
    if(INTF==1)    //interrupt flag
    {
        INTF=0;
        T1CON=0X01;
        ZC++;
```

```
        }
        if(TMR1IF==1)
        {
                TMR1IF=0;
                TMR1L=LOW;
                TMR1H=HIGH;
                COUNT++;
                if(COUNT==1)
                {
                        PORTB=0X12;
                }
                else if(COUNT==2)
                {
                        PORTB=0X0C;
                }
                else if(COUNT==3)
                {
                        PORTB=0X04;
                }
                else if(COUNT==4)
                {
                        COUNT=0;
                        T1CON=0X00;
                        PORTB=0X02;
                }
        }
}
DEBOUNCE ()
{
        for(i=0;i<=1000;i++)
}}
```

APPENDIX-2

Order this document by LM358/D

MOTOROLA

LM358, LM258, LM2904, LM2904V

Dual Low Power Operational Amplifiers

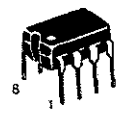
DUAL DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA

Utilizing the circuit designs perfected for recently introduced Quad Operational Amplifiers, these dual operational amplifiers feature 1) low power drain, 2) a common mode input voltage range extending to ground/V_{EE}, 3) single supply or split supply operation and 4) pinouts compatible with the popular MC1558 dual operational amplifier. The LM158 series is equivalent to one–half of an LM124.

These amplifiers have several distinct advantages over standard operational amplifier types in single supply applications. They can operate at supply voltages as low as 3.0 V or as high as 32 V, with quiescent currents about one–fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

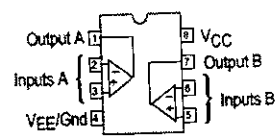
- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 32 V
- Low Input Bias Currents
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Single and Split Supply Operation
- Similar Performance to the Popular MC1558
- ESD Clamps on the Inputs Increase Ruggedness of the Device without Affecting Operation



N SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	LM258 LM358	LM2904 LM2904V	Unit
Power Supply Voltages Single Supply Split Supplies	 V_{CC} V_{CC}, V_{EE}	 32 ±16	 26 ±13	Vdc
Input Differential Voltage Range (Note 1)	V_{IDR}	±32	±26	Vdc
Input Common Mode Voltage Range (Note 2)	V_{ICR}	–0.3 to 32	–0.3 to 26	Vdc
Output Short Circuit Duration	t_{SC}	Continuous		
Junction Temperature	T_J	150		°C
Storage Temperature Range	T_{stg}	–55 to +125		°C
Operating Ambient Temperature Range LM258 LM358 LM2904 LM2904V	T_A	 –25 to +85 0 to +70 – –	 – – –40 to +105 –40 to +125	°C

NOTES: 1. Split Power Supplies.
2. For Supply Voltages less than 32 V for the LM258/358 and 26 V for the LM2904, the absolute maximum input voltage is equal to the supply voltage.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM2904D	T_A = –40° to +105°C	SO–8
LM2904N		Plastic DIP
LM2904VD	T_A = –40° to +125°C	SO–8
LM2904VN		Plastic DIP
LM258D	T_A = –25° to +85°C	SO–8
LM258N		Plastic DIP
LM358D	T_A = 0° to +70°C	SO–8
LM358N		Plastic DIP

Rev 2

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	LM258			LM358			LM2904			LM2904V			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage V_{CC} = 5.0 V to 30 V (26 V for LM2904, V), V_{IC} = 0 V to V_{CC} −1.7 V, V_O = 1.4 V, R_S = 0 Ω T_A = 25°C T_A = T_{high} (Note 1) T_A = T_{low} (Note 1)	V_{IO}	– – –	2.0 – –	5.0 7.0 2.0	– – –	2.0 – –	7.0 9.0 9.0	– – –	2.0 – –	7.0 10 10	– – –	– – –	– 13 10	mV
Average Temperature Coefficient of Input Offset Voltage T_A = T_{high} to T_{low} (Note 1)	$\Delta V_{IO}/\Delta T$	–	7.0	–	–	7.0	–	–	7.0	–	–	7.0	–	μV/°C
Input Offset Current T_A = T_{high} to T_{low} (Note 1)	I_{IO}	– –	3.0 –	30 100	– –	5.0 –	50 150	– –	5.0 45	50 200	– –	5.0 45	50 200	nA
Input Bias Current T_A = T_{high} to T_{low} (Note 1)	I_{IB}	– –	–45 –50	–150 –300	– –	–45 –50	–250 –500	– –	–45 –50	–250 –500	– –	–45 –50	–250 –500	
Average Temperature Coefficient of Input Offset Current T_A = T_{high} to T_{low} (Note 1)	$\Delta I_{IO}/\Delta T$	–	10	–	–	10	–	–	10	–	–	10	–	pA/°C
Input Common Mode Voltage Range (Note 2), V_{CC} = 30 V (26 V for LM2904, V) V_{CC} = 30 V (26 V for LM2904, V), T_A = T_{high} to T_{low}	V_{ICR}	0 0	– –	28.3 28	0 0	– –	28.3 28	0 0	– –	24.3 24	0 0	– –	24.3 24	V
Differential Input Voltage Range	V_{IDR}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	V
Large Signal Open Loop Voltage Gain R_L = 2.0 kΩ, V_{CC} = 15 V, For Large V_O Swing, T_A = T_{high} to T_{low} (Note 1)	A_{VOL}	50 25	100 –	– –	25 15	100 –	– –	25 15	100 –	– –	25 15	100 –	– –	V/mV
Channel Separation 1.0 kHz ≤ f ≤ 20 kHz, Input Referenced	CS	–	−120	–	–	−120	–	–	−120	–	–	−120	–	dB
Common Mode Rejection R_S ≤ 10 kΩ	CMR	70	85	–	65	70	–	50	70	–	50	70	–	dB
Power Supply Rejection	PSR	65	100	–	65	100	–	50	100	–	50	100	–	dB
Output Voltage–High Limit (T_A = T_{high} to T_{low}) (Note 1) V_{CC} = 5.0 V, R_L = 2.0 kΩ, T_A = 25°C V_{CC} = 30 V (26 V for LM2904, V), R_L = 2.0 kΩ V_{CC} = 30 V (26 V for LM2904, V), R_L = 10 kΩ	V_{OH}	3.3 26 27	3.5 – 28	– – –	3.3 26 27	3.5 – 28	– – –	3.3 22 23	3.5 – 24	– – –	3.3 22 23	3.5 – 24	– – –	V
Output Voltage–Low Limit V_{CC} = 5.0 V, R_L = 10 kΩ, T_A = T_{high} to T_{low} (Note 1)	V_{OL}	–	5.0	20	–	5.0	20	–	5.0	20	–	5.0	20	mV
Output Source Current V_{ID} = +1.0 V, V_{CC} = 15 V	I_{O+}	20	40	–	20	40	–	20	40	–	20	40	–	mA
Output Sink Current V_{ID} = −1.0 V, V_{CC} = 15 V V_{ID} = −1.0 V, V_O = 200 mV	I_{O-}	10 12	20 50	– –	10 12	20 50	– –	10 –	20 –	– –	10 –	20 –	– –	mA μA
Output Short Circuit to Ground (Note 3)	I_{SC}	–	40	60	–	40	60	–	40	60	–	40	60	mA
Power Supply Current (T_A = T_{high} to T_{low}) (Note 1) V_{CC} = 30 V (26 V for LM2904, V), V_O = 0 V, R_L = ∞ V_{CC} = 5 V, V_O = 0 V, R_L = ∞	I_{CC}	– –	1.5 0.7	3.0 1.2	– –	1.5 0.7	3.0 1.2	– –	1.5 0.7	3.0 1.2	– –	1.5 0.7	3.0 1.2	mA

NOTES: 1. T_{low} = −40°C for LM2904
= −40°C for LM2904V
= −25°C for LM258
= 0°C for LM358

T_{high} = +105°C for LM2904
= +125°C for LM2904V
= +85°C for LM258
= +70°C for LM358

2. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is V_{CC} −1.7 V.
3. Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Figure 1. Input Voltage Range

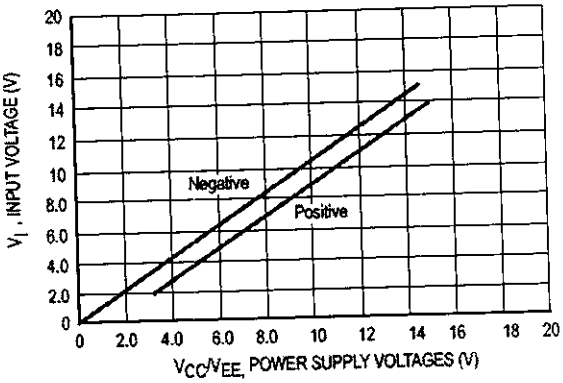


Figure 2. Large–Signal Open Loop Voltage Gain

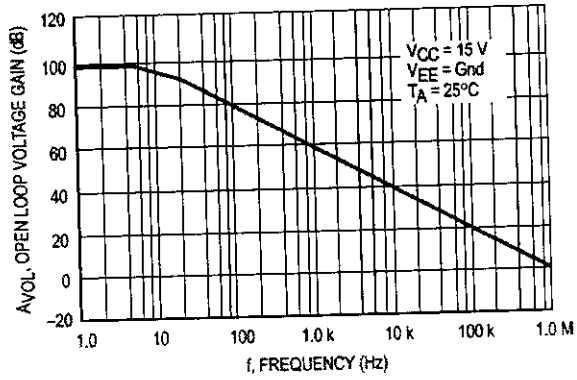


Figure 3. Large–Signal Frequency Response

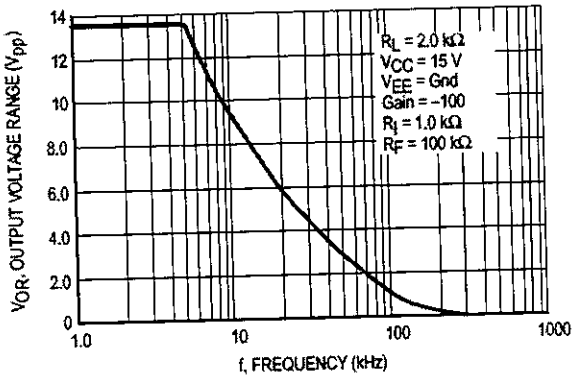


Figure 4. Small Signal Voltage Follower Pulse Response (Noninverting)

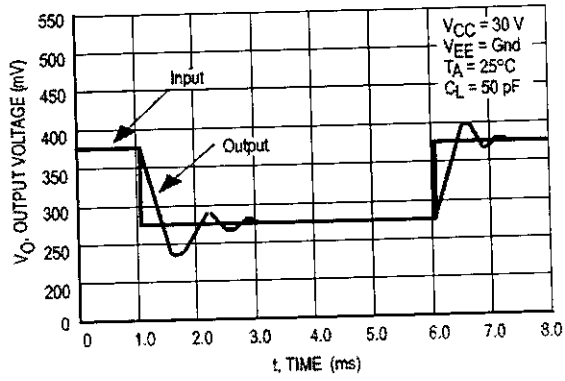


Figure 5. Power Supply Current versus Power Supply Voltage

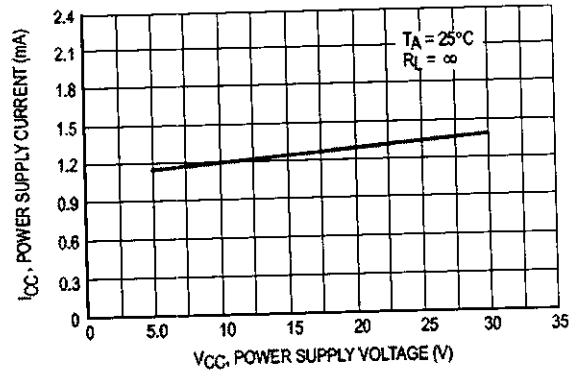
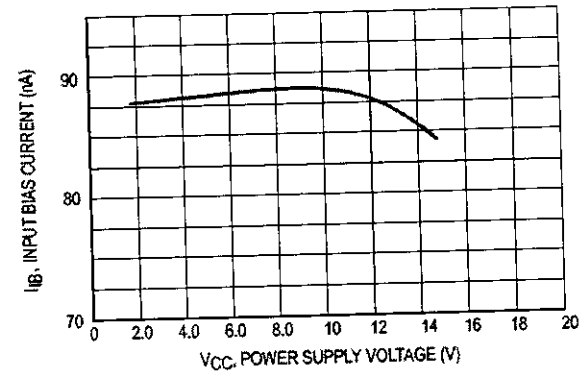


Figure 6. Input Bias Current versus Supply Voltage



APPENDIX-3

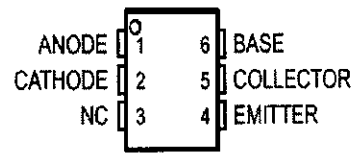
MCT2, MCT2E
OPTOCOUPLERS

SOES023 – MARCH 1983 – REVISED OCTOBER 1995

COMPATIBLE WITH STANDARD TTL INTEGRATED CIRCUITS

- **Gallium Arsenide Diode Infrared Source Optically Coupled to a Silicon npn Phototransistor**
- **High Direct-Current Transfer Ratio**
- **Base Lead Provided for Conventional Transistor Biasing**
- **High-Voltage Electrical Isolation . . . 1.5-kV, or 3.55-kV Rating**
- **Plastic Dual-In-Line Package**
- **High-Speed Switching:**
  t_r = 5 µs, t_f = 5 µs Typical
- **Designed to be Interchangeable with General Instruments MCT2 and MCT2E**

MCT2 OR MCT2E . . . PACKAGE
(TOP VIEW)



NC – No internal connection

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†

Input-to-output voltage: MCT2	± 1.5 kV
MCT2E	± 3.55 kV
Collector-base voltage	70 V
Collector-emitter voltage (see Note 1)	30 V
Emitter-collector voltage	7 V
Emitter-base voltage	7 V
Input-diode reverse voltage	3 V
Input-diode continuous forward current	60 mA
Input-diode peak forward current ($t_w \leq 1$ ns, PRF ≤ 300 Hz)	3 A
Continuous power dissipation at (or below) 25°C free-air temperature:	
Infrared-emitting diode (see Note 2)	200 mW
Phototransistor (see Note 2)	200 mW
Total, infrared-emitting diode plus phototransistor (see Note 3)	250 mW
Operating free-air temperature range, T_A	−55°C to 100°C
Storage temperature range, T_{stg}	−55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. This value applies when the base-emitter diode is open-circulated.
2. Derate linearly to 100 °C free-air temperature at the rate of 2.67 mW/°C.
3. Derate linearly to 100 °C free-air temperature at the rate of 3.33 mW/°C.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)CBO}$	Collector-base breakdown voltage		I_C = 10 µA, I_E = 0, I_F = 0		70			V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage		I_C = 1 mA, I_B = 0, I_F = 0		30			V
$V_{(BRECO)}$	Emitter-collector breakdown voltage		I_E = 100 µA, I_B = 0, I_F = 0		7			V
I_R	Input diode static reverse current		V_R = 3 V				10	µA
$I_{C(on)}$	On-state collector current	Phototransistor operation	V_{CE} = 10 V, I_B = 0, I_F = 10 mA		2	5		mA
		Photodiode operation	V_{CB} = 10 V, I_E = 0, I_F = 10 mA			20		µA
$I_{C(off)}$	Off-state collector current	Phototransistor operation	V_{CE} = 10 V, I_B = 0, I_F = 0			1	50	nA
		Photodiode operation	V_{CB} = 10 V, I_E = 0, I_F = 0			0.1	20	nA
H_{FE}	Transistor static forward current transfer ratio		V_{CE} = 5 V, I_C = 100 µA, I_F = 0	MCT2		250		
				MCT2E	100	300		
V_F	Input diode static forward voltage		I_F = 20 mA			1.25	1.5	V
$V_{CE(sat)}$	Collector-emitter saturation voltage		I_C = 2 mA, I_B = 0, I_F = 16 mA			0.25	4	V
r_{IO}	Input-to-output internal resistance		V_{in-out} = ±1.5 kV for MCT2, ±3.55 kV for MCT2E, See Note 4		10^{11}			Ω
C_{io}	Input-to-output capacitance		V_{in-out} = 0, f = 1 MHz, See Note 4			1		pF

NOTE 4: These parameters are measured between both input diode leads shorted together and all the phototransistor leads shorted together.

switching characteristics

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	Phototransistor operation	V_{CC} = 10 V, $I_{C(on)}$ = 2 mA, R_L = 100 Ω, See Test Circuit A of Figure 1		5		µs
t_f	Fall time						
t_r	Rise time	Photodiode operation	V_{CC} = 10 V, $I_{C(on)}$ 20 µA, R_L = 1 kΩ, See Test Circuit B of Figure 1		1		µs
t_f	Fall time						

TYPICAL CHARACTERISTICS

COLLECTOR CURRENT
vs
INPUT-DIODE FORWARD CURRENT

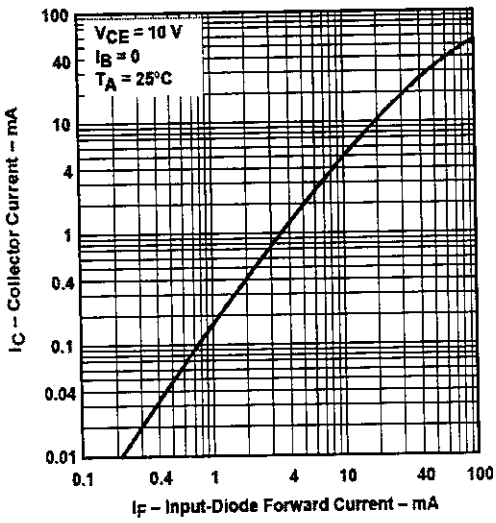
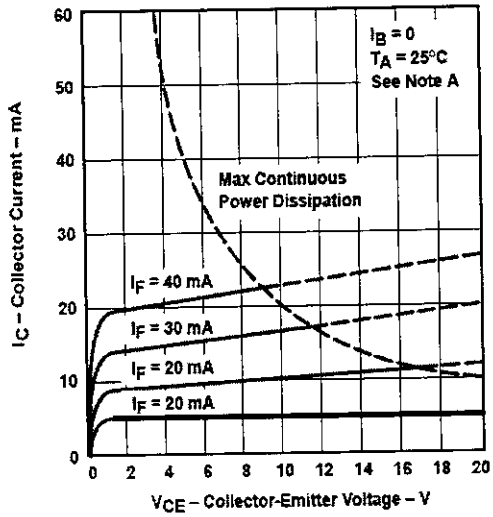


Figure 2

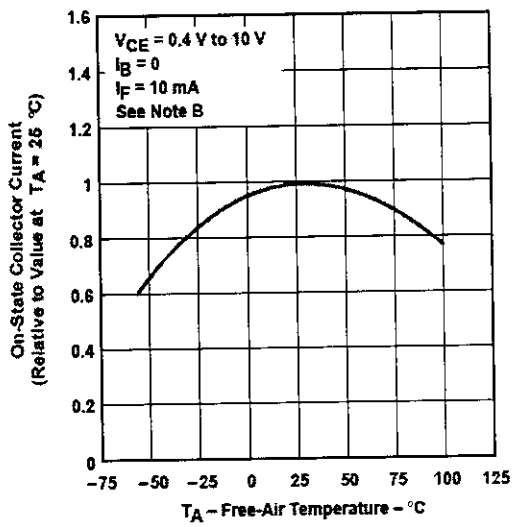
COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE



NOTE A: Pulse operation of input diode is required for operation beyond limits shown by dotted lines.

Figure 3

ON-STATE COLLECTOR CURRENT
(RELATIVE TO VALUE AT 25°C)
vs
FREE-AIR TEMPERATURE

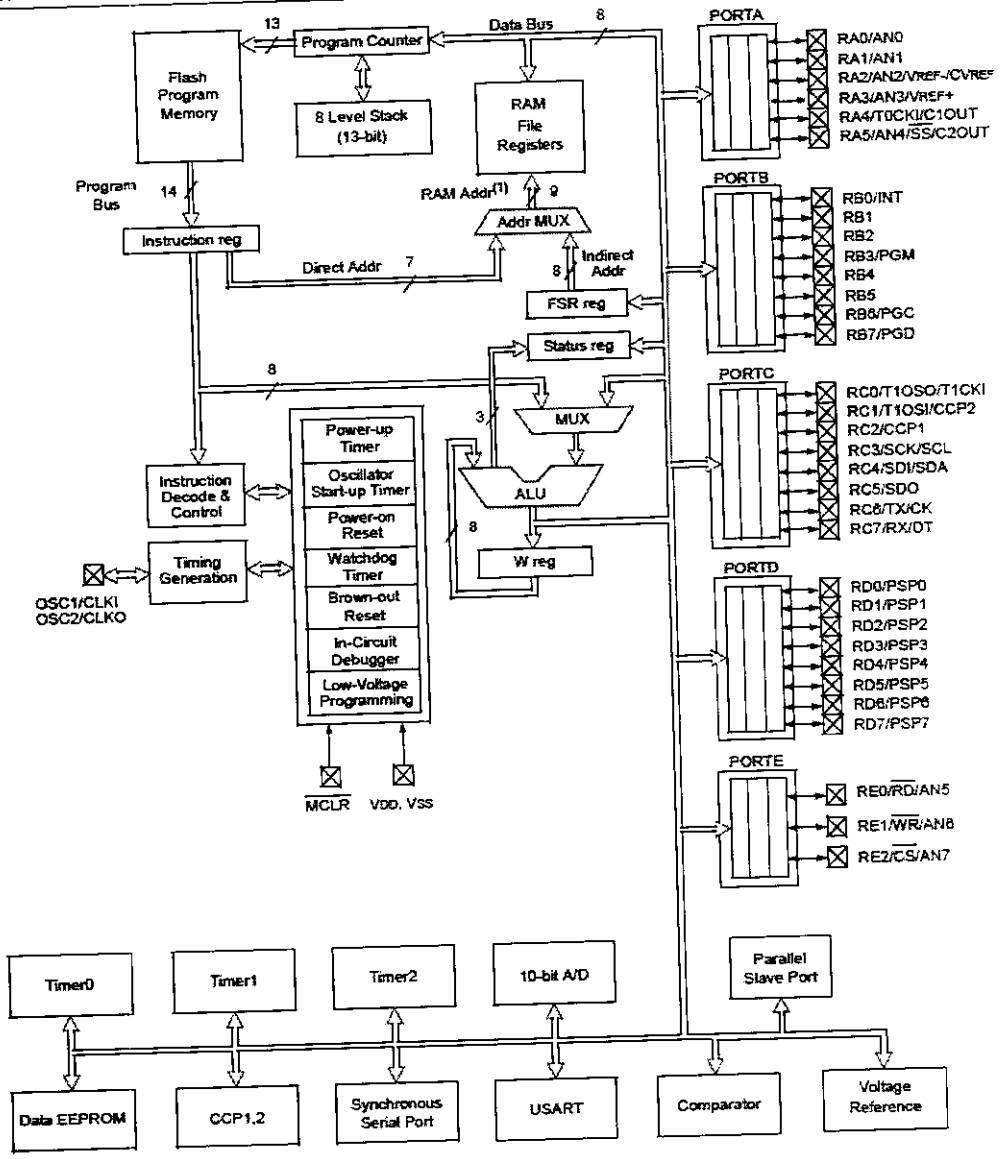


NOTE B: These parameters were measured using pulse techniques, t_w = 1 ms, duty cycle ≤ 2 %.

Figure 4

APPENDIX-4

FIGURE 1-2: PIC16F874A/877A BLOCK DIAGRAM



Device	Program Flash	Data Memory	Data EEPROM
PIC16F874A	4K words	192 Bytes	128 Bytes
PIC16F877A	8K words	368 Bytes	256 Bytes

Note 1: Higher order bits are from the Status register.

TABLE 4-3: PORTB FUNCTIONS

Name	Bit#	Buffer	Function
RB0/INT	bit 0	TTL/ST(1)	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit 1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit 2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3/PGM(3)	bit 3	TTL	Input/output pin or programming pin in LVP mode. Internal software programmable weak pull-up.
RB4	bit 4	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB5	bit 5	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB6/PGC	bit 6	TTL/ST(2)	Input/output pin (with interrupt-on-change) or in-circuit debugger pin. Internal software programmable weak pull-up. Serial programming clock.
RB7/PGD	bit 7	TTL/ST(2)	Input/output pin (with interrupt-on-change) or in-circuit debugger pin. Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode or in-circuit debugger.

3: Low-Voltage ICSP Programming (LVP) is enabled by default which disables the RB3 I/O function. LVP must be disabled to enable RB3 as an I/O pin and allow maximum compatibility to the other 28-pin and 40-pin mid-range devices.

TABLE 4-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
06h, 106h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
86h, 186h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
81h, 181h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

TABLE 4-5: PORTC FUNCTIONS

Name	Bit#	Buffer Type	Function
RC0/T1OSO/T1CKI	bit 0	ST	Input/output port pin or Timer1 oscillator output/Timer1 clock input.
RC1/T1OSI/CCP2	bit 1	ST	Input/output port pin or Timer1 oscillator input or Capture2 input/ Compare2 output/PWM2 output.
RC2/CCP1	bit 2	ST	Input/output port pin or Capture1 input/Compare1 output/ PWM1 output.
RC3/SCK/SCL	bit 3	ST	RC3 can also be the synchronous serial clock for both SPI and I^2C modes.
RC4/SDI/SDA	bit 4	ST	RC4 can also be the SPI data in (SPI mode) or data I/O (I^2C mode).
RC5/SDO	bit 5	ST	Input/output port pin or Synchronous Serial Port data output.
RC6/TX/CK	bit 6	ST	Input/output port pin or USART asynchronous transmit or synchronous clock.
RC7/RX/DT	bit 7	ST	Input/output port pin or USART asynchronous receive or synchronous data.

Legend: ST = Schmitt Trigger input

TABLE 4-6: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
07h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111

Legend: x = unknown, u = unchanged

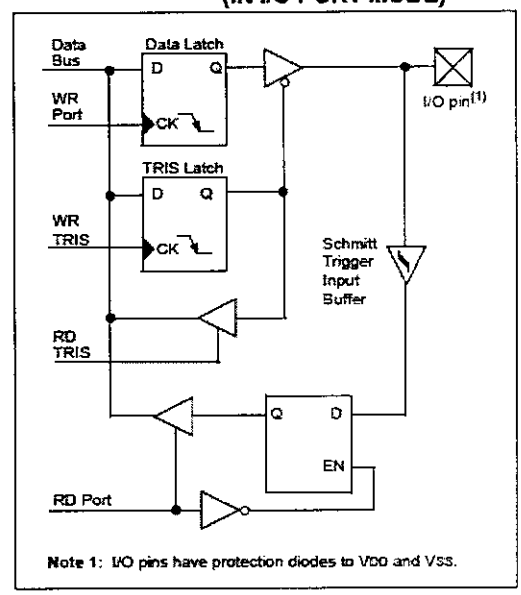
4.4 PORTD and TRISD Registers

Note: PORTD and TRISD are not implemented on the 28-pin devices.

PORTD is an 8-bit port with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output.

PORTD can be configured as an 8-bit wide microprocessor port (Parallel Slave Port) by setting control bit, PSPMODE (TRISE<4>). In this mode, the input buffers are TTL.

FIGURE 4-8: PORTD BLOCK DIAGRAM (IN I/O PORT MODE)



Note 1: I/O pins have protection diodes to VDD and VSS.

TABLE 4-7: PORTD FUNCTIONS

Name	Bit#	Buffer Type	Function
RD0/PSP0	bit 0	ST/TTL(1)	Input/output port pin or Parallel Slave Port bit 0.
RD1/PSP1	bit 1	ST/TTL(1)	Input/output port pin or Parallel Slave Port bit 1.
RD2/PSP2	bit2	ST/TTL(1)	Input/output port pin or Parallel Slave Port bit 2.
RD3/PSP3	bit 3	ST/TTL(1)	Input/output port pin or Parallel Slave Port bit 3.
RD4/PSP4	bit 4	ST/TTL(1)	Input/output port pin or Parallel Slave Port bit 4.
RD5/PSP5	bit 5	ST/TTL(1)	Input/output port pin or Parallel Slave Port bit 5.
RD6/PSP6	bit 6	ST/TTL(1)	Input/output port pin or Parallel Slave Port bit 6.
RD7/PSP7	bit 7	ST/TTL(1)	Input/output port pin or Parallel Slave Port bit 7.

Legend: ST = Schmitt Trigger input, TTL = TTL input

Note 1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffers when in Parallel Slave Port mode.

TABLE 4-8: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
08h	PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx xxxx	uuuu uuuu
88h	TRISD	PORTD Data Direction Register								1111 1111	1111 1111
89h	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Data Direction Bits			0000 -111	0000 -111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTD.

5.2 Using Timer0 with an External Clock

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, it is necessary for T0CKI to be high for at least 2 Tosc (and a small RC delay of 20 ns) and low for at least 2 Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

5.3 Prescaler

There is only one prescaler available which is mutually exclusively shared between the Timer0 module and the Watchdog Timer. A prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer and vice versa. This prescaler is not readable or writable (see Figure 5-1).

The PSA and PS2:PS0 bits (OPTION_REG<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF 1`, `MOVWF 1`, `BSF 1,x`....etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.

Note:	Writing to TMR0 when the prescaler is assigned to Timer0 will clear the prescaler count, but will not change the prescaler assignment.

REGISTER 5-1: OPTION_REG REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

bit 7 $\overline{\text{RBPU}}$

bit 6 INTEDG

bit 5 **T0CS**: TMR0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKO)

bit 4 **T0SE**: TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA**: Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS2:PS0**: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

TABLE 5-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
01h,101h	TMR0	Timer0 Module Register								xxxx xxxx	uuuu uuuu
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	0000 000u
81h,181h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer0.

APPENDIX-5

FAIRCHILD SEMICONDUCTOR®

November 2001

IRF840B/IRFS840B

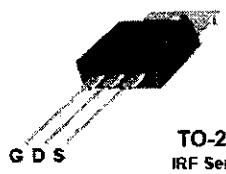
500V N-Channel MOSFET

General Description

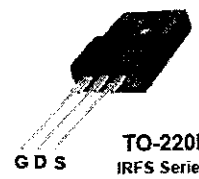
These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies, power factor correction and electronic lamp ballasts based on half bridge.

Features

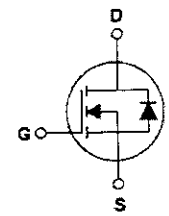
- 8.0A, 500V, $R_{DS(on)}$ = 0.8Ω @V_{GS} = 10 V
- Low gate charge (typical 41 nC)
- Low Crss (typical 35 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



TO-220
IRF Series



TO-220F
IRFS Series



Absolute Maximum Ratings

T_C = 25 C unless otherwise noted

Symbol	Parameter		IRF840B	IRFS840B	Units
V_{DSS}	Drain-Source Voltage		500		V
I_D	Drain Current - Continuous (T_C = 25 C)		8.0	8.0	A
	- Continuous (T_C = 100 C)		5.1	5.1	A
I_{DM}	Drain Current - Pulsed	(Note 1)	32	32	A
V_{GSS}	Gate-Source Voltage		± 30		V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	320		mJ
I_{AR}	Avalanche Current	(Note 1)	8.0		A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	13.4		mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	3.5		V/ns
P_D	Power Dissipation (T_C = 25 C)		134	44	W
	- Derate above 25 C		1.08	0.35	W/ C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150		C
T_L	Maximum lead temperature for soldering purposes. 1/8" from case for 5 seconds		300		C

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	IRF840B	IRFS840B	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case Max.	0.93	2.86	C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient Max.	62.5	62.5	C/W

Electrical Characteristics T_C = 25 C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	500	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25 C	--	0.55	--	V/ C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	--	--	10	µA
		V_{DS} = 400 V, T_C = 125 C	--	--	100	µA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 4.0 A	--	0.65	0.8	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 4.0 A (Note 4)	--	7.3	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	1400	1800	pF
C_{oss}	Output Capacitance		--	145	190	pF
C_{rss}	Reverse Transfer Capacitance		--	35	45	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250 V, I_D = 8.0 A, R_G = 25 Ω (Note 4, 5)	--	22	55	ns
t_r	Turn-On Rise Time		--	65	140	ns
$t_{d(off)}$	Turn-Off Delay Time		--	125	260	ns
t_f	Turn-Off Fall Time		--	75	160	ns
Q_g	Total Gate Charge	V_{DS} = 400 V, I_D = 8.0 A, V_{GS} = 10 V (Note 4, 5)	--	41	53	nC
Q_{gs}	Gate-Source Charge		--	6.5	--	nC
Q_{gd}	Gate-Drain Charge		--	17	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	8.0	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	32	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 8.0 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 8.0 A, dI_F / dt = 100 A/µs (Note 4)	--	390	--	ns
Q_{rr}	Reverse Recovery Charge		--	4.2	--	µC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 9.0mH, I_{AS} = 8.0A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25 C
3. I_{SD} ≤ 8.0A, di/dt ≤ 200A/µs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25 C
4. Pulse Test : Pulse width ≤ 300µs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Characteristics

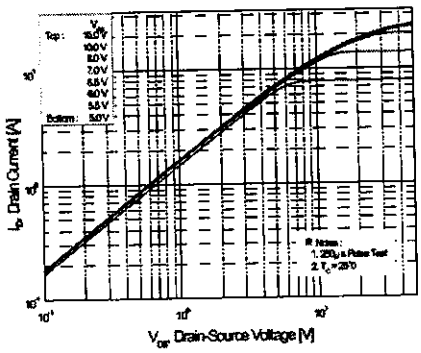


Figure 1. On-Region Characteristics

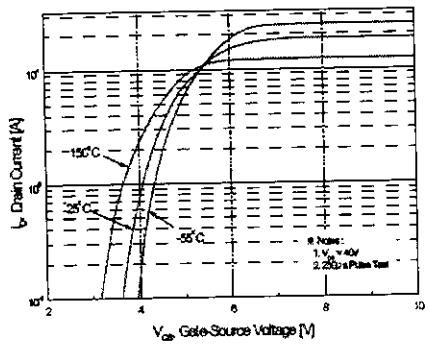


Figure 2. Transfer Characteristics

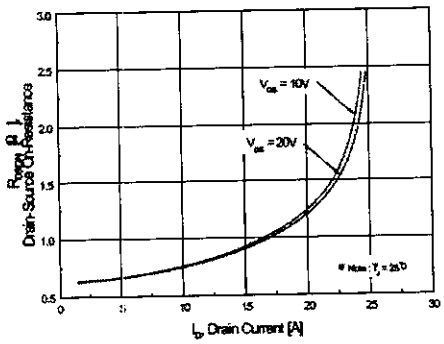


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

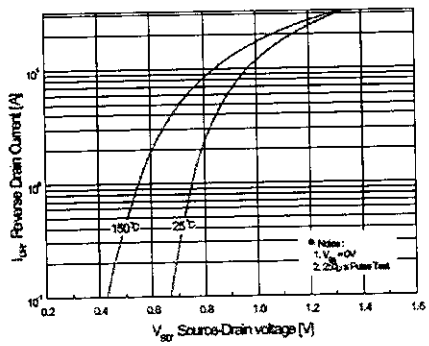


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

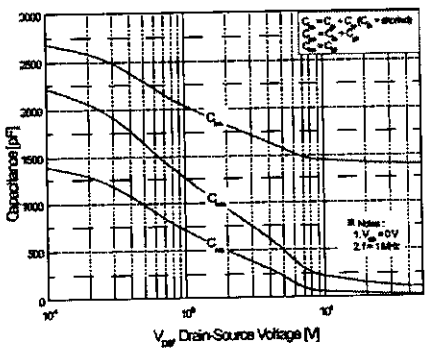


Figure 5. Capacitance Characteristics

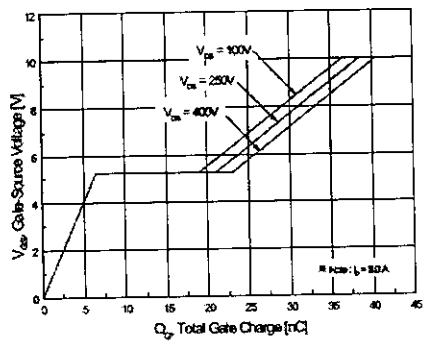


Figure 6. Gate Charge Characteristics

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REFERENCES

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