Design and Modeling of D- STATCOM

P-2361

A Project Report

Submitted by

S. Lakshmiganthan	**-71204105031**
M. Saravana Kumar	**-71204105046**
M.K. Suresh Kumar	**-71204105054**

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KUMARAGURU COLLEGE OF TECHNOLOGY
COIMBATORE – 641 006

ANNA UNIVERSITY: CHENNAI 600 025

APRIL 2008

ANNA UNIVERSITY: CHENNAI 600 025

BONAFIDE CERTIFICATE

Certified that this project report entitled **"Design and Modeling of D- STATCOM"** is the bonafide work of

Mr. S. Lakshmiganthan	- Register No. 71204105031
Mr. M. Saravana Kumar	- Register No. 71204105046
Mr. M.K. Suresh Kumar	- Register No. 71204105054

Who carried out the project work under my supervision.

Signature of the Head of the Department	Signature of the Guide
Prof. K. Regupathy Subramanian	Mrs. V. Sharmila Deve

Certified that the candidate with university Register No. 71204105031, 71204105046, 71204105054 was examined in project viva voce Examination held on 21/04/08

Internal Examiner **External Examiner**

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING
KUMARAGURU COLLEGE OF TECHNOLOGY, COIMBATORE 641 006

ABSTRACT

The aim of this project is to develop a model and control scheme for Distribution STAtic COMpensator (DSTATCOM) using c++ program. DSTATCOM is an emerging FACTS controller which is used to maintain a good voltage profile and for power factor improvement in a power system network. This project develops a method to operate a distribution static compensator (DSTATCOM) as a voltage regulator to maintain the voltage of a specified bus and assumed that the source voltages and loads are balanced and sinusoidal. The magnitude of the bus voltage is pre-specified while its phase angle is generated from the dc capacitor control loop. A hysteresis current controller for inverter is used for voltage tracking using the DSTATCOM. The customers connected to that bus would be supplied by a set of distorted voltages due to sudden load variation. Therefore, a DSTATCOM can be used at this bus to maintain quality voltage profile. The proposed structure is verified through detailed simulation and experimental results.

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CONTENTS

TITLE		PAGE NO
BONAFIDE CERTIFICATE		i
ABSTRACT		ii
ACKNOWLEDGEMENT		iii
CONTENTS		iv
LIST OF TABLES		vi
LISTOF FIGURES		vii
LIST OF SYMBOLS AND ABBREVATIONS		viii
CHAPTER 1	**INTRODUCTION**	1
1.1	GENERAL	2
1.2	PROBLEM STATEMENT	2
1.3	OBJECTIVE	3
1.4	ORGANISATION OF THE REPORT	3
CHAPTER 2	**D-STATCOM – AN OVERVIEW**	4
2.1	INTRODUCTION	5
2.2	DEFINITION	5
2.3	PRINCIPLE OF OPERATION	5
CHAPTER 3	**TYPES OF VOLTAGE SOURCE INVERTERS**	10
3.1	GENERAL	11
3.2	VARIOUS VSI TOPOLOGIES	11
	3.2.1 THREE PHASE, THREE LEG VSI TOPOLOGY	11
	3.2.2 THREE PHASE, FOUR LEG VSI TOPOLOGY	12
	3.2.3 THREE PHASE, H-BRIDGE VSI TOPOLOGY	12
	3.2.4 THREE PHASE, NEUTRAL CLAMPED VSI TOPOLOGY	13
	3.2.5 THREE PHASE, NEUTRAL CLAMPED CHOPPER-INVERTER TOPOLOGY	14
3.3	SWITCHING DYNAMICS OF VSI	14
3.4	DESIGN OF VARIOUS PARAMETERS FOR VSI	15
	3.4.1 SELECTION OF DC LINK VOLTAGE	15
	3.4.2 SELECTION OF DC STORAGE CAPACITOR	16
	3.4.3 SWITCHING FREQUENCY OF THE VSI	16
	3.4.4 SELECTION OF HYSTERESIS BAND	16
CHAPTER 4	**HYSTERESIS CURRENT CONTROLLER**	18
CHAPTER 5	**PROPOSED CONTROLLER FOR DSTATCOM**	22
5.1	OUTER LOOP CONTROL	24
5.2	INNER LOOP CONTROL	24
5.3	SYSTEM DATA	25
CHAPTER 6	**FLOWCHART AND ALGORITHM**	26
6.1	ALGORITHM	27
6.2	FLOWCHART	28
CHAPTER 7	**TEST SYSTEM, RESULTS AND DISCUSSIONS**	29
7.1	TEST SYSTEM	30
7.2	INPUT DATA	30
7.3	SWITCHING CONTROL	32
7.4	RESULTS	33
7.5	DISCUSSIONS	34
CHAPTER 8	**CONCLUSION**	35
	REFERENCES	37

LIST OF TABLES

TABLE	TITLE	PAGE NO
5.1	SYSTEM DATA	25
7.1	INPUT DATA	30

LIST OF FIGURES

FIGURE	TITLE	PAGE NO
2.1	VSC Connected To Ac Network Through a Shunt Transformer	6
2.2	Shunt Connected Variable Solid State Voltage Source	6
2.3	Reactive power exchange between the converter and the AC systems	7
3.1	Three-Phase, Three-Leg VSI Topology	11
3.2	Three-Phase, Four-Leg VSI Topology	12
3.3	Three-Phase, H-Bridge VSI Topology	13
3.4	Three-Phase, Neutral Clamped VSI Topology	13
3.5	Three-Phase, Neutral Clamped Chopper-Inverter Topology	14
3.6	Switching Dynamics of The VSI	15
4.1	Control scheme of hysteresis current controller	20
4.2	Current and voltage waves with hysteresis-band current control	21
5.1	Proposed controller for DSTATCOM	23
7.1	Test System	30
7.2	Thevenin's equivalent circuit	31
7.3	DSTATCOM inverter circuit	32
7.4	Total DC Capacitor Voltage	33
7.5	Voltage at PCC	33

LIST OF SYMBOLS AND ABBREVATIONS

NO	SYMBOLS	ABBREVATIONS
1	AC	Alternating Current
2	DC	Direct Current
3	VSC	Voltage Source Converter
4	PCC	Point of Common Coupling
5	PI	Proportional Integral Controller
6	PU	Per Unit
7	HB	Hysteresis Band
8	δ	Power Angle
9	$K_{p\delta}$	Proportional gain
10	$K_{i\delta}$	Integral gain
11	K_{PV}	Proportional controller gain
12	V_{dc}	Voltage across each capacitor
13	V_c	The summation of voltage across the two capacitors
14	V_m	The desired magnitude of the peak terminal voltage
15	V_{tref}	The reference voltage to be maintained at the terminal bus
16	P_{shref}	The amount of power that must be drawn from the compensator
17	P_{sh}	Amount of power drawn by shunt link
18	ω	Fundamental frequency of the system
19	T	Required time period

CHAPTER – 1

INTRODUCTION

1.1 GENERAL

In the last two decades, various schemes of load compensation have been proposed. These schemes can cancel the effect of unbalance and distortion in currents and can also correct the power factor at the load bus. All of these schemes assume the source voltages to be balanced and sinusoidal. The sensitive loads must be protected by a compensator that can regulate the bus voltage to provide balanced sinusoidal voltage of pre-specified magnitude.

In a distribution system, there may be several compensating devices. However, in a radial distribution system, the voltage of a particular bus can be distorted or unbalanced if the loads in any part of the system are nonlinear or unbalanced. The customers connected to that bus would be supplied by a set of unbalanced and distorted voltages, even when their loads are not contributing to the bus voltage pollution.

Therefore, a DSTATCOM can be used at the distribution bus to reduce voltage imbalance by absorbing or injecting reactive power.

1.2 PROBLEM STATEMENT

A five bus balanced system is used as the test system. A single phase inverter circuit supplied by two neutral clamped DC storage capacitors realizes the DSTATCOM which is connected at fifth bus of the distribution side. The magnitude of the reference voltage is chosen as nominal value, while its phase angle is obtained through a feedback loop that regulates the voltage at the point of common coupling. DSTATCOM is to be designed for the balanced system using C++ programming.

1.3 OBJECTIVE

- A closed loop control scheme, consisting of an outer DC capacitor voltage loop and an inner load angle control loop is to be designed.
- The control scheme is to maintain the power balance at the PCC (Point of Common Coupling).
- Finally, the DSTATCOM is to be designed for balanced system which will regulate the voltage profile of the distribution bus to which it is connected.

1.4 ORGANIZATION OF THE REPORT

- **Chapter 1** explains the motivation for this project to be undertaken, the brief description of the problem statement, objective, and the organization of the report.
- **Chapter 2** depicts what DSTATCOM is all about and its operations with the help of schematic and diagrammatic representations.
- **Chapter 3** is *"Types of Voltage Source Inverters (VSI)"*. This chapter presents the various types and topologies of voltage source inverters, its operation, switching dynamics along with design of various parameters of VSI.
- **Chapter 4** explains the *"Hysteresis Current Controller"* and how it works in the DSTATCOM. This chapter also provides the switching scheme of the controller.
- **Chapter 5** provides a method to operate the distribution static compensator (DSTATCOM) as a voltage regulator to maintain the voltage of a specified bus.
- **Chapter 6** explains the overall project in the form of flowchart and algorithm. Therefore, this chapter gives the complete sketch of the project.
- **Chapter 7** gives the test system description and its structure. The input data, results and discussions scheme is also explained in this chapter.
- **Chapter 8** concludes the works done so far. Extending, it also gives the future of DSTATCOM.

processing of the voltage and current waveforms in the **voltage source converter (VSC).** A single-line STATCOM power circuit is shown in the Fig.1.1 where a VSC is connected to a utility bus through magnetic coupling.

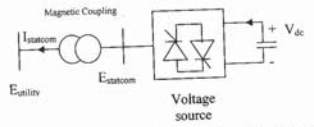


Fig.2.1.VSC connected to the AC network through a shunt transformer

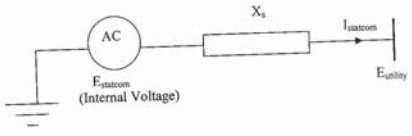


Fig.2.2.Shunt connected variable solid state voltage source.

In Fig.1.2, a STATCOM is seen as an adjustable voltage source behind a reactance i.e., the capacitor banks and shunt reactors are not needed for reactive power generation and absorption, thereby giving the STATCOM a compact design, or small footprint, as well as low noise and low magnitude impact.

The exchange of reactive power between the converter and the AC systems can be controlled by varying the amplitude of the 3-phase output voltage Es, of the converter as illustrated in the Fig .1.3. That is if the amplitude of the output voltage is increased beyond that of the utility bus voltage, Ei, then the current flows through the reactance from the converter to the AC system and the converter generates capacitive- reactive

CHAPTER - 2

D-STATCOM – An Overview

2.1 INTRODUCTION

This chapter presents the operating principles and applications of highly versatile controller – the STATCOM. This FACTS controller is based on nonthyristor devices such as gate turn-offs (GTOs) and insulated-gate bipolar transistors (IGBTs).

A STATCOM is analogous to an ideal synchronous machine, which generates a balanced set of three sinusoidal voltages- at the fundamental frequency- with controllable amplitude and phase angle. This ideal machine has no inertia, is practically instantaneous, does not significantly alter the existing system impedance, and can internally generate reactive (both capacitive and inductive) power.

2.2 DEFINITION

A distribution shunt-connected reactive power compensation device that is capable of generating and/ or absorbing reactive power in which the output can be varied to control the specific parameters of an electrical power system.

In general a solid state switching converter capable of generating or absorbing independently controllable real and reactive power at its output terminals when it is fed from an energy source or energy- storage device at its input terminals.

A voltage- source converter that, from a given input of DC voltage, produces a set of 3- phase AC output voltages, each in phase with and coupled to the corresponding AC system voltage through a relatively small reactance (which is provided by either an interface reactor or the leakage inductance of a coupling transformer). The DC voltage is provided by an energy storage capacitor.

2.3 PRINCIPLE OF OPERATION

A STATCOM is a controlled reactive power source. It provides the desired reactive power generation and absorption entirely by means of electronic

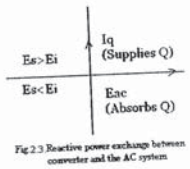


Fig.2.3 Reactive power exchange between converter and the AC system

power for the AC system. If the amplitude of the output voltage is decreased below the utility bus voltage, then the current flows from the AC system to the converter and the converter absorbs inductive- reactive power from the AC system. If the output voltage equals the AC system voltage, the reactive power exchange becomes zero, in which case the STATCOM is said to be in floating state.

Adjusting the phase shift between the converter output voltage and the AC input voltage can similarly control the real power exchange between the converter and the AC system. In other words, the converter can supply real power to the AC system from the DC energy storage if the converter output voltage is made to lead the AC system voltage. On the other hand, it can absorb real power from the AC system for the DC system if its voltage lags behind the AC system voltage.

A STATCOM provides the desired reactive power by exchanging the instantaneous reactive power among the phases of the system. The mechanism by which the converter internally generates and/ or absorbs the reactive power can be understood by considering the relationship between the output and input powers of the converter. The converter switches the DC input circuit directly to the AC output circuit. Thus the net instantaneous power at the AC output terminals must always be equal to the net instantaneous power at the DC input terminals (neglecting the losses).

If it is assumed that the converter is operated to supply only the reactive power output, the real power provided by the DC source as the input to the converter must be zero. Furthermore, because the reactive power at zero frequency (DC) is by definition zero, the DC source supplies no reactive power as the input to the converter and thus clearly plays no part in generation of reactive output power by the converter. In other words, the converter simply interconnects the three output terminals so that the reactive output currents can freely flow among them. If the terminals of the AC systems are regarded in this context, the converter establishes a circulating reactive power exchange among the phases. However, the real power that the converter exchanges at its AC terminals with the AC system must, of course, be supplied to absorbed from its DC terminals by the DC capacitor.

Although the reactive power is generated internally by the converter switches action, a DC capacitor must still be connected across the input terminals of the converter. The primary for the capacitor is to provide a circulating current path and acts as a voltage source. The magnitude of the capacitor is chosen so that the DC voltage across its terminals remains fairly constant to prevent it from contributing to the ripples in the DC current. The VSC output voltage is in the form of a staircase wave into which smooth sinusoidal current from the AC system is drawn, resulting in the slight fluctuations in the output power of the converter.

Depending on the converter configuration employed, it is possible to calculate the minimum capacitance required to meet the system requirements, such as ripple limits on the DC voltage and the rated reactive power support needed by the AC system.

The VSC has the same rated current capability when it operates with the capacitive or inductive reactive current. Therefore, a VSC having certain MVA rating gives the STATCOM twice the dynamic range in MVAR (this also contribute to a compact design). A DC capacitor bank is used for the operation of the VSC.

The reactive power of a STATCOM is produced by means of power electronic equipment of the voltage source converter type. The VSC may be a 2-level or 3-level type, depending on the required power output and voltage. A number of VSCs are combined in a multi-pulse connection to form a STATCOM. In the steady state, the VSCs operate with fundamental frequency switching to minimize converter losses. However, during transient conditions caused by the line faults, a pulse width modulated (PWM) mode is used to prevent the fault current from entering the VSCs. In this way, the STATCOM is able to withstand transients on the AC side.

CHAPTER - 3

TYPES OF VOLTAGE SOURCE INVERTRERS

3.1 GENERAL

The parameters and dynamic performance of the voltage source inverter (VSI) in current tracking mode play an important role while compensating unbalanced and non-linear loads. A VSI is generally operated in hysteresis band current control mode to track the desired reference currents and to inject them at the point of common coupling. The hysteresis band current controller has advantages like simplicity in implementation and fast response. Also, its operation is mostly independent of load Parameters.

3.2 VARIOUS VSI TOPOLOGIES

3.2.1 THREE-PHASE, THREE-LEG VSI TOPOLOGY

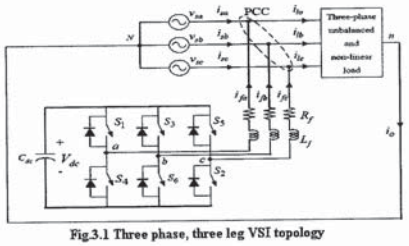


Fig.3.1 Three phase, three leg VSI topology

The zero sequence currents in the load cannot be compensated and hence the zero sequence currents flow in the neutral wire (N – *n)* between the source and the load. The zero sequence current thus returns to the power distribution system, thus degrading the power quality. The generation of the three compensator currents is not independent. Hence, this scheme is not suitable for three-phase, four-wire distribution system with load currents containing zero sequence components.

P-2361

3.2.2 THREE-PHASE, FOUR-LEG VSI TOPOLOGY

Three of its legs are connected to three phases and the fourth leg is connected to the load and supply neutral through an interface reactance. The reference current for the fourth leg is the negative sum of three-phase load currents. This nullifies the effect of DC component in load current. To maintain adequate charge in the DC storage capacitor, a PI controller is used to regulate the flow of real power from the source to compensator. When the compensator is working, the zero sequence current containing switching frequency components and harmonics component is routed through the path $n - n'$. Using fourth leg of inverter, the negative of zero sequence current $(0 - i)$ is tracked.

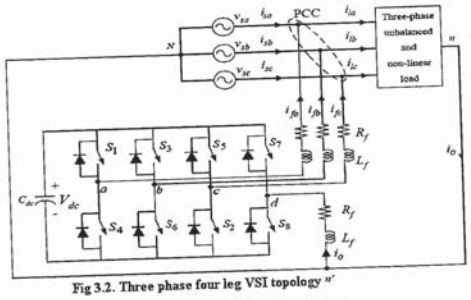


Fig 3.2. Three phase four leg VSI topology

3.2.3 THREE-PHASE, H-BRIDGE VSI TOPOLOGY

The purpose of these transformers is to provide isolation between the inverter legs and to prevent the DC storage capacitor from being shorted by switches in different inverter legs. This topology however is not suitable for compensation of load currents containing DC components, due to the presence of the isolation transformers.

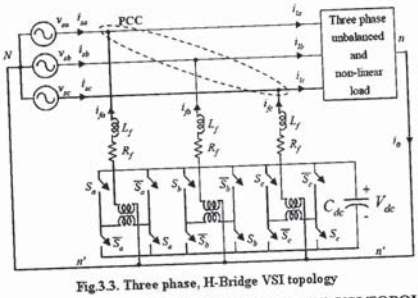


Fig.3.3. Three phase, H-Bridge VSI topology

3.2.4 THREE-PHASE, NEUTRAL CLAMPED VSI TOPOLOGY

This topology is well equipped to compensate DC components of the load, but due to the presence of DC components in VSIs, the two DC capacitors are charged to different voltages. The total voltage of DC capacitors however is maintained constant by using a PI voltage control loop. It is not only the DC current in load which can make drift in the DC capacitor voltages from the reference value, but also the unequal capacitance leakage currents, unequal delays in the semiconductor devices

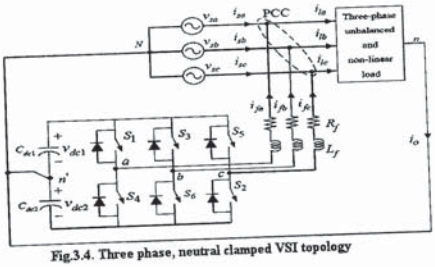


Fig.3.4. Three phase, neutral clamped VSI topology

3.2.5 THREE-PHASE, NEUTRAL CLAMPED CHOPPER-INVERTER TOPOLOGY

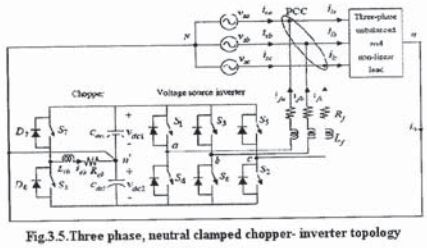


Fig.3.5.Three phase, neutral clamped chopper- inverter topology

The function of the chopper is to transfer energy between the two DC capacitors so as to make their voltages close to the reference value. The chopper circuit requires an additional control hence increases the control complexity.

3.3 SWITCHING DYNAMICS OF THE VSI

The reference and actual currents marked with time instants are shown in this fig.(9); an arbitrary reference filter current is shown by a discontinuous curve. The upper and lower limits of the reference currents are created by adding and subtracting the hysteresis band from the filter reference current. To track the positive I_{fref} at any time t_1, the switch 1 *S* is closed and 4 *S* is opened. This connects V_{dc1} to the inverter and the actual filter current rises from (I_{fref} -h) to (I_{fref} ' +h) through I_{fref} . Once the current I_f crosses the upper limit (I_{fref} '+h), it has to be brought back within the pre-defined band. To do this, switch 4 *S* is closed and the switch 1 *S* is opened. However, if the current *f i* remains positive, the switch 4 *S* will not conduct and conduction takes place through diode 4 *D* . When 4 *S* or 4 *D* conduct, the control input V_{dc2} is connected to the VSI. Similarly for negative current and positive slope current, diode 1 *D* conducts instead of switch S1

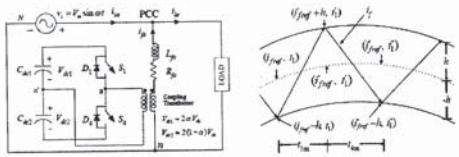


Fig.3.6.Switching dynamics of the VSI

3.4 DESIGN OF VARIOUS PARAMETERS FOR VSI

3.4.1SELECTION OF DC LINK VOLTAGE

The total harmonic distortion (THD) of the compensated source current is taken as the figure of merit. When the DC link voltage is approximately equal to 1.6 times the peak AC supply voltage, the percentage THD in the compensated source current is minimum. Due to the practical constraints, the DC link voltage should satisfy the following condition.

$$Vm<Vdc<Vdevice/2$$

Also,

$$m = \frac{1}{\sqrt{(1 - f_{swmin}/f_{swmax})}}$$

we should select f_{swmin} in such a way that the variation in the switching frequency (*s Δfsw)* is a minimum with a reasonable value of DC link voltage. Once the DC link voltage is computed, the selection of DC capacitor value is important. It can be selected based on the ability to regulate voltage under load transients.

3.4.2 SELECTION OF DC STORAGE CAPACITOR

Let us further assume that, the VSI compensator deals with half (i.e. $X / 2$) and twice (i.e. $2X$) kVA handling capacity under the transient conditions for n cycles with period of the system voltage T. Then the change in energy to be dealt by the DC capacitor is given as

$$\Delta E = (2X - X/2)\, n\, T$$

Now this change in energy should be supported by the DC capacitor.

$$C_{dc} = \frac{(2X - X/2)\, n\, T}{(1.8\, V_m)^2 - (1.4\, V_m)^2}$$

3.4.3 SWITCHING FREQUENCY OF THE VSI

Practically, the maximum switching frequency of the VSI depends on the type of power switches used. To achieve higher switching frequency in the range of 100 kHz, MOSFET switches should be used, but their voltage and current rating are smaller compared to IGBT. The IGBT switches are generally preferred due to their higher power handling capacity, good switching speed and low gating power. Typically, the switching frequency of IGBT switches is around 20 kHz, but it is recommended to operate at 10 kHz range.

3.4.4 SELECTION OF HYSTERESIS BAND

If a low value of hysteresis band is chosen, the bandwidth (switching frequency) requirement of the inverter becomes high. Similarly, when interface inductance is quite large, for a given bandwidth of VSI, smaller hysteresis band is required to maintain the product, hLf, as a constant when hysteresis band is high, the losses incurred due to the latter will be large as compared to switching losses. Hence, a cost function is formulated as given below.

$$J = k_1 \frac{V_m (2m^2 - 1)}{8\, h m\, L_f} + k_2 h^2$$

To minimize the cost function J with respect to h, Eqn. (4.17) is differentiated and

equated to zero.

$$h = \left(\frac{k_1}{k_2} \frac{(2m^2 - 1)}{4m^2} f_{sw\max} \right)^{1/2}$$

The constant k2 is solved by approximating ohmic losses due to hysteresis

$$h_{loss} = \left\{ (i_{f\,ref}^{+} + h) - (i_{f\,ref}^{-} - h) \right\}^2 R_f$$

Considering variation in R_f from 0.06 to 0.4 Ω, the corresponding values of h are found to be 10% and 4% respectively.

CHAPTER - 4

HYSTERESIS CURRENT CONTROLLER

Hysteresis current control is one of the PWM techniques used. Among the various 'WM techniques, the hysteresis band current control PWM method is popularly used because of s simplicity of implementation. Besides fast-response current loop and inherent-peak current imiting capability, the technique does not need any information about system parameters.

Sinusoidal command currents are compared with the respective machine phase urrents and the resulting errors through hysteresis-band current controllers command the ransistor base drives, as is shown below. The hysteresis bands that are normally fixed and the ame for all phases in a conventional system are shown being updated from a microcomputer in ıe proposed adaptive band system. The band (HB) can be modulated at different points of the ndamental frequency cycle to control the PWM switching pattern of the inverter.

ience the control method can be suitably denoted as follows and it is shown in Fig.4.1which is ıe control scheme of the hysteresis current controller.

	Upper switches	lower switches
$I_a < I_a^*$-hb	OFF	ON
$I_a < I_a^*$+hb	ON	OFF

Here, I_a is phase current

I_a^* is reference current

hb is hysteresis band.

The same condition is repeated for other phase currents also.

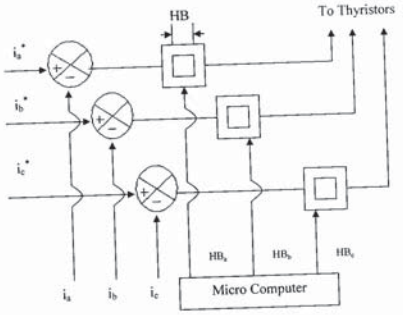


Fig.4.1. Control Scheme of hysteresis current controller

Current and voltage waves with hysteresis-band current control is shown as in Fig.4.2

Q_1 Upper Switch

Q_4 Lower Switch

The current *i*, tends to cross the lower hysteresis band at point 1, where the ransistor Q1 is switched on. The linearly rising current (i, +) then touches the upper band at point ², where the transistor Q4 is switched on.

Hence in this method current is maintained within the limit and accordingly lower or ıpper switches are made ON or OFF.

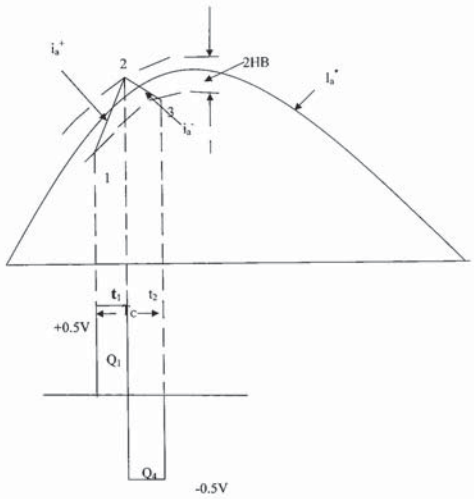


Fig.4.2. Current and voltage waves with hysteresis-band current control

CHAPTER – 5

PROPOSED CONTROLLER FOR DSTATCOM

In this project, a method is proposed to operate the Distribution STATic COMpensator (DSTATCOM) as a voltage regulator to maintain the voltage of a specified bus. The magnitude of the bus voltage is pre specified while its phase angle is generated from the DC capacitor control loop. A deadbeat controller for inverter is used for voltage tracking using the DSTATCOM.

The control method proposed in this method is a two loop control method. This method is explained in detail as follows

When two DC storage capacitors are supplying the DSTATCOM, the average of real power entering the PCC (terminal) from source must equal the sum of average load power and the losses in the DSTATCOM. Otherwise, the capacitors will continuously either charge or discharge. The magnitude of the terminal voltage can be arbitrarily chosen up to a certain limit. The lower limit of V_t is decided by the maximum permissible value of its angle $\delta < \pi/2$ with respect to the source voltage, while its upper limit set by the voltage rating of the inverter and the DC capacitors. The phase angle must be adjusted in a closed loop for power balance. The nominal value of the terminal voltage is chosen to be 1.0 p.u. and the phase angle is controlled by a two-loop feedback control shown

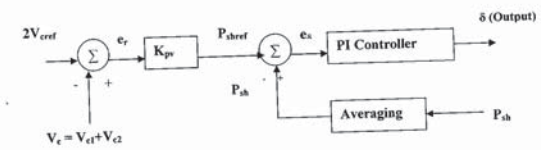


Fig.5.1. Proposed controller for DSTATCOM

5.1 OUTER VOLTAGE LOOP

Assuming that the voltage across each capacitor is V_{dc}, the total voltage across the DC link is 2 V_{dc}. The deviation of this total voltage from its reference value ($2V_{cref}$) is a good indication of losses in the inverter. Therefore, we add the two capacitor voltages and compare the total with the reference value. It is to be noted that the DC capacitor voltage usually contains the switching frequency components. Therefore, comparing its instantaneous value with that of the reference will result in a large error in control. Instead, the average value of the DC capacitors can be regulated around the reference value. Alternatively, the value of the total voltage across the capacitors at the end of a cycle can be regulated around a reference value. This is done through a proportional controller with a gain of K_{PV}. The output of this controller is P_{shref} which is the amount of power that must be drawn from the compensator in order to maintain the DC capacitor voltage.

$$P_{shref} = K_{PV}(V_c - 2V_{ref})$$

V_c = the summation of voltage across the two capacitors Since the loop maintains the capacitor voltage, we call it the outer voltage loop.

5.2 INNER POWER LOOP

The power angle δ (which is the phase angle between the terminal and the source voltages in their respective phases) is computed in such a way that it ensures that the shunt link draws an amount of power P_{sh} that is equal to P_{shref} To achieve this, a PI controller is used, the output of which is power angle δ. This is given as

$$\delta = K_{p\delta}(P_{sh} - P_{shref}) + K_{i\delta}\int (P_{sh} - P_{shref})\,dt$$

where $K_{p\delta}$ and $K_{i\delta}$ These gains must be carefully chosen, as high gain may cause unnecessary oscillations and may even cause instability.

It is to be noted that a positive value of P_{sh} corresponds to a direction of power flow from the compensator into the bus, which reduces the DC capacitor voltage. In the steady state, the average value of P_{sh} is negative due to the inverter losses. The

instantaneous value of P_{sh} obtained from the above equation is averaged over a cycle. This average value is denoted by and is used to implement the inner power loop to compute, as shown in block diagram. The angle is defined with the source voltage as reference. Thus, we require the zero crossing of the phase voltage of the source. This information can be obtained through telemetry when bus to be controlled is remotely located. The reference voltages for the PCC bus are given as

$$V_{trefa} = V_m \sin(\omega t - \delta)$$
$$V_{trefb} = V_m \sin(\omega t - 2\pi/3 - \delta)$$
$$V_{trefc} = V_m \sin(\omega t + 2\pi/3 - \delta)$$

Where V_m is the desired magnitude of the peak terminal voltage and ω is the fundamental frequency of the system.

5.3 SYSTEM DATA

System Voltage	565V ± 10%, Sinusoidal and may contain harmonics and exhibit swell, sag
Terminal bus voltage	565V (peak), Sinusoidal, balanced
Feeder Impedance	1+j3.14Ω
DC Capacitors (C1,C2)	2200uF each
Interface Inductors (L_{fa}, L_{fb}, L_{fc})	20mH, 0.2 Ω
AC Capacitors (C_{fa}, C_{fb}, C_{fc})	50uF in each phase
Voltage controller gains of DC capacitor loops	K_{pv} = 10
δ Control loop gains	$K_{p\delta}$ = 4e-6, $K_{i\delta}$ = 8e-6
Reference voltage of total DC Capacitor voltage	1200V
Control signals hysteresis band for each phase	H = 1

Table.5.1. System Data

CHAPTER – 6
ALGORITHM AND FLOWCHART

6.1 ALGORITHM

Step1: Read all bus data, line data, tolerance, convergence, etc.

Step2: Run load flow for t=0 sec to t=m1-1 sec.

Step3: At t=m1 sec, Create disturbance.

Step4: Run load flow, calculate voltages of all buses.

Err =Vref-V[i], where, i = disturbance created at i^{th} bus.

If Err>0.0001, go to step 5.

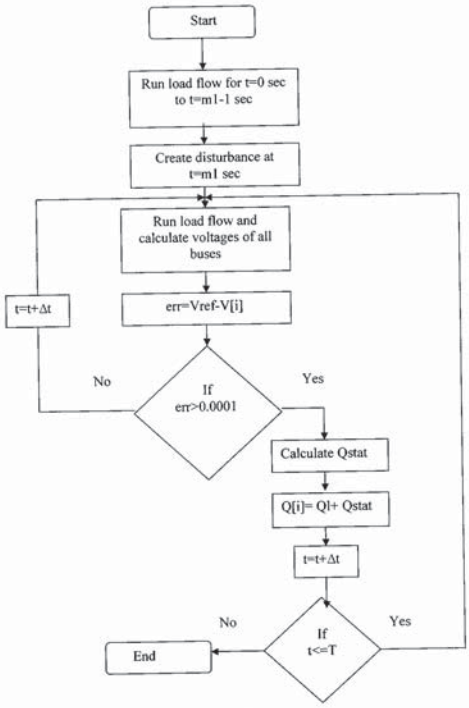
Step 5: Calculate Qstat, power injection from D-STATCOM according to the change in load.

Step 6: Q[i]= Q_f+ Q_{stat}

go to step 4.

Step 7: Repeat step 4 to 6 up to required time period.

6.2 FLOWCHART



CHAPTER - 7
TEST SYSTEM, RESULTS AND DISCUSSIONS

7.1 TEST SYSTEM

The test system used in this project was a five bus system with the DSTATCOM connected to the fifth bus. Hence the voltage of the fifth bus is regulated

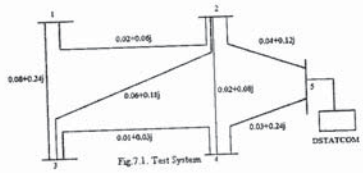


Fig.7.1. Test System

7.2 INPUT DATA

The input data for the above system is as follows

Bus No.	Bus type	V_{spec}(PU)	Generator		Load		Q_{min}	Q_{max}
			P	Q	P	Q		
1	Slack	1.06	-	-	-	-	-	-
2	PV	1.00	0.6	-	0.0	0.1	-1.0	1.3
3	PQ	-	-	-	0.45	0.15	-	-
4	PQ	-	-	-	0.4	0.05	-	-
5	PQ	-	-	-	0.6	0.1	-	-

Table.7.1. Input data

In a distribution system, there may be several compensating devices. However, in a radial distribution system, the voltage of a particular bus can be distorted or unbalanced if the loads in any part of the system are nonlinear or unbalanced. The customers connected to that bus would be supplied by a set of unbalanced and distorted voltages, even when their loads are not contributing to the bus voltage pollution. Therefore, a

DSTATCOM can be used at this bus to reduce harmonics and balance the bus voltages. Consider the three-phase, four-wire radial system shown in fig (7.1) Let us assume that we would like to correct the voltage of bus 5. The single-phase Thevenin equivalent of the system is shown in Fig(7.2). Here, and constitute the Thevenin equivalent looking toward the left into the network, while the equivalent load is the impedance looking toward the right into the network, at bus 5. Since the DSTATCOM is connected at this bus, it is called the *point of common coupling*. We now have to use the DSTATCOM in the voltage control mode at bus 5. However, since the Thevenin equivalents can change any time depending on the load, it is desirable that these parameters are not used in the voltage controller design. Below, we present a voltage control technique that only requires the timing information from the source for synchronization

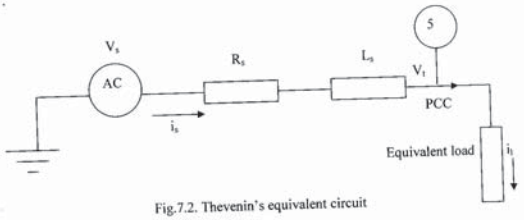


Fig.7.2. Thevenin's equivalent circuit

The DSTATCOM is realized by a two-level neutral-clamped voltage source converter (VSC). A filter capacitor is used in parallel with the VSC circuit to provide a path for the high-frequency components. The PCC is referred to as the terminal in this thesis.

7.3 SWITCHING CONTROL

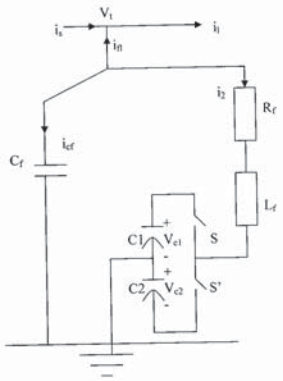


Fig.7.3. DSTATCOM inverter circuit

As mentioned earlier, the switching variable is constrained to be ±1. One leg of the neutral clamped inverter is chosen to realize DSTATCOM. Here, there are two DC storage capacitors, namely, C1 and C2 and the voltage across each capacitor is maintained at V_{dc}. The status of the top and the bottom switch is complementary which is shown in Fig.7.3. This means for, the top switch is closed (open), while the bottom switch is open (closed) connecting the output of the inverter leg to . Therefore, through switching the inverter supplies a voltage. The variable controls the status of the inverter switches through gate drive circuits. The switching variable is obtained from the continuous signal by a hysteresis action around zero, i.e.

If Uc(k) > h,then u=1

Else if Uc(k)<-h ,then u=-1

7.4 RESULTS:

The results obtained from the simulation is plotted and the resulted graph is shown below,

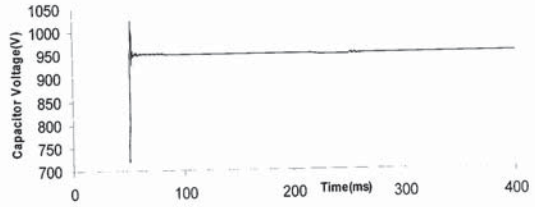


Fig.7.4.Total DC Capacitor Voltage

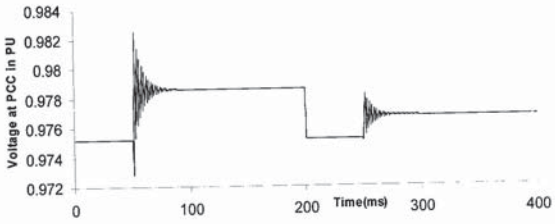


Fig.7.5. Voltage at PCC

7.5 DISCUSSIONS:

With respect to the graphs obtained from the simulation results, the following statements are made,

- For 0 to 50sec, no disturbance, the normal voltage is 0.975208V
- At 51st second, a load increase causes voltage to drop to 0.972988V
- When DSTATCOM is introduced at 51st second, the voltage improves and attains steady value of 0.978605V at 92nd second.
- At 200th second, the load is brought back to its normal load. Therefore, the voltage attains its original value of 0.975208V
- At 251st second, again load change is introduced. But DSTATCOM compensates to 0.976719 at 286sec

CHAPTER - 8
CONCLUSION

CONCLUSION

In the present work, an algorithm has been proposed to balance the sudden voltage fluctuation that arises due to load variations in a balanced radial distribution system.

- Thus, a single phase inverter circuit supplied by two neutral clamped DC storage capacitors realized the DSTATCOM.
- A closed loop control scheme, consisting of an outer DC capacitor voltage loop and an inner load angle control loop is used.
- It is shown that the DSTATCOM can regulate the voltage of the terminal bus at a nominal value against any distortion in the load side.

In future,

- DSTATCOM can be implemented to unbalanced systems
- This could be made use for Power factor Correction and Neutral current elimination.

REFERENCES

- M. K. Mishra, A. Ghosh, and A. Joshi, ***"A new STATCOM topology to compensate loads containing AC and DC components"*** in IEEE-PES Winter Meeting 2000, Singapore, 2000.
- Mahesh K. Mishra, ***"Operation of a DSTATCOM in Voltage Control Mode"***, IEEE TRANSACTIONS ON POWER DELIVERY, VOL. 18, NO. 1, JANUARY 2003.
- R. Mohan Mathur, Rajiv.K Varma, ***"Thyristor based FACTS controllers for electrical transmission systems"***, Wiley IEEE press.
- Narain.G Hingorani, Lazlo Gyugyi, ***"Understanding FACTS"*** Wiley IEEE press.