A GENERAL PWM STRATEGY FOR FOUR-SWITCH THREE PHASE INVERTER

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BONAFIDE CERTIFICATE

Certified that this project report titled "**A GENERAL PWM STRATEGY FOR FOUR-SWITCH THREE PHASE INVERTER**" is the bonafide work of **Mr.A.GOWRI SHANKAR (0720105004)** who carried out the project work under my supervision. Certified further, that to the best of my knowledge the work reported herein does not form part of any other project report of dissertation on the basis of which a degree or ward was conferred on an earlier occasion on this or any other candidate.

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"A General PWM Strategy for Four - Switch Three Phase Inverter"

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ABSTRACT

The proposed single-phase to three-phase inverter employs only four MOSFET switches. The proposed configuration incorporates a single phase diode bridge rectifier which gives a variable dc voltage and send through filter capacitor. This arrangement provides a constant dc voltage as an input to the inverter. A four-switch inverter configuration with split capacitors provides a three-phase output to the ac motor load at adjustable voltage and frequency. Since MOSFET switches can operate at high frequency, advanced PWM techniques like sinusoidal PWM control are used.

The entire circuit for four switch three phase inverter is designed and simulated using **PSIM 7.0.5** Software. The hardware is implemented for half HP induction motor load. PWM pulses are generated and controlled using PIC 16F877A microcontroller. These features of the four switch three phase inverter can find applications in variable speed drives, uninterruptible power supplies, and other power conversion systems.

ACKNOWLEDGEMENT

I humbly submit all the glory and thanks to the almighty for showering the blessings and giving the necessary wisdom for accomplishing this project.

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LIST OF SYMBOLS AND ABBREVIATIONS

PWM	Pulse Width Modulation
SPWM	Sinusoidal Pulse Width Modulation
PIC	Peripheral Interface Controller
ICD	In - Circuit Debugger
RISC	Reduced Instruction Set Computer
EEPROM	Electrically Erasable Programmable Read only Memory
SSP	Synchronous Serial Port
USART	Universal Synchronous Asynchronous Receiver Transmitter
PSP	Parallel Slave Port
WDT	Watch Dog Timer
SFR	Special Function Register
rpm	Rotations per minute
Vin	Input supply voltage, volts
Vp	Transformer primary voltage, volts
Vs	Transformer secondary voltage, volts
Vr	Unregulated DC voltage, volts
Vdc	Constant DC voltage, volts
Vab,Vbc,Vca	Three phase output voltage, volts
Ia,Ib,Ic	Three phase output current, volts

CHAPTER I

INTRODUCTION

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INTRODUCTION

1.1 INTRODUCTION

Within the last decade, there have been major advancements in power electronics. Power electronics have moved along with these developments with such things as digital signal processors being used to control power systems. An Inverter is basically a converter that converts DC-AC power. A voltage source inverter (VSI) is one that takes in a fixed voltage from a device, such as a dc power supply, and converts it to a variable-frequency AC supply.

Inverter circuits can be very complex so the objective of the project is to present some of the inner workings of inverters without getting lost in some of the fine details. Pulse-width modulation inverters take in a constant dc voltage. Diode-rectifiers are used to rectify the line voltage, and the inverter must control the magnitude and the frequency of the ac output voltages. To do this the inverter uses pulse-width modulation using its switches. There are different methods for doing the pulse-width modulation in an inverter in order to shape the output ac voltages to be very close to a sine wave. Pulse Width Modulation (PWM) is widely employed to control the output of static power inverters. The reason for using PWM is that they provide voltage and/or current wave shaping customized to the specific needs of the application under consideration. It is lastly performance and cost criteria which determines the choice of a PWM method in a specific application. PWM inverters can control their output voltage and frequency simultaneously. And also they can reduce the harmonic components in load currents.

These features have made the power candidate to use in many industrial applications such as variable speed drives, uninterruptible power supplies, and other power conversion systems. In addition, recent research reports published by the Electric Power Research Institute (EPRI) cite potential energy saving figures for operating the residential heating ventilation and air conditioning (HVAC) systems at variable speed. The report also suggests this technology for HVAC systems. The power converter for the ac motor must satisfy low-cost and low-harmonic pollution requirements.

1.2 OBJECTIVE

To design and implement a single phase to three phase four-switch inverter using pulse width modulation (PWM) control.

1.3 ORGANISATION OF THE PROJECT

1.3.1 PROJECT OVERVIEW

The proposed single-phase to three-phase inverter employs only four MOSFET switches. The proposed configuration incorporates a diode bridge rectifier structure that provides the dc link with an active input current shaping feature. A four-switch inverter configuration with split capacitors in the dc link provides a balanced three-phase output to the ac motor load at adjustable voltage and frequency. Since MOSFET switches can operate at high frequency, advanced PWM techniques known for inverter control can be used. The feature of the proposed scheme is

- Reduced switches
- Dc link voltage control
- Power factor improvement
- Three phase balanced output voltage

1.3.2 REPORT LAYOUT

The layout gives the complete organization of the report. Chapter 2 describes the operation of proposed inverter and the components used. Chapter 3 gives the simulation results of the proposed four switch three phase inverter. Chapter4 contains the information about the microcontroller used and the coding used in the microcontroller for PWM operation of inverter. Chapter 5 describes the hardware implementation of the project. Chapter 6 gives the conclusion and recommendations for future work.

CHAPTER II

INTRODUCTION TO INVERTERS

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INTRODUCTION TO INVERTERS

2.1 TRADITIONAL SOURCE INVERTERS

Traditional source inverters are Voltage Source Inverter and Current Source Inverter. The input of Voltage Source Inverter is a stiff dc voltage supply, which can be a battery or a controlled rectifier both single phase and three phase voltage source inverter are used in industry. The switching device can be a conventional MOSFET, Thyristor, or a power transistor.

Voltage source inverter is one which the dc source has small or negligible impedance. In other words a voltage source inverter has stiff dc source voltage at its input terminals. A current-fed inverter or current source inverter is fed with adjustable dc current source. In current source inverter output current waves are not affected by the load.

2.1.1 VOLTAGE SOURCE INVERTER

When the power requirement is high, three phase inverters are used. When three single phase inverters are connected in parallel, we can get the three phase inverter. The gating signals for the three phase inverters have a phase difference of 120°. These inverters take their dc supply from a battery or from a rectifier and can be called as six-step bridge inverter. Fig.2.1 shows the three phase inverter using six MOSFET's and with diodes. A large capacitor is connected at the input terminals tends to make the input dc voltage constant. This capacitor also suppresses the harmonics fed back to the source.

The Voltage Source Inverter is widely used. However, it has the some conceptual and theoretical barriers and limitations. The AC output voltage is limited and cannot exceed the AC input voltage. Therefore the Voltage Source Inverter is only buck (step down) inverter operation for DC to AC power conversion or boost (step-up) operation for AC to DC power conversion.

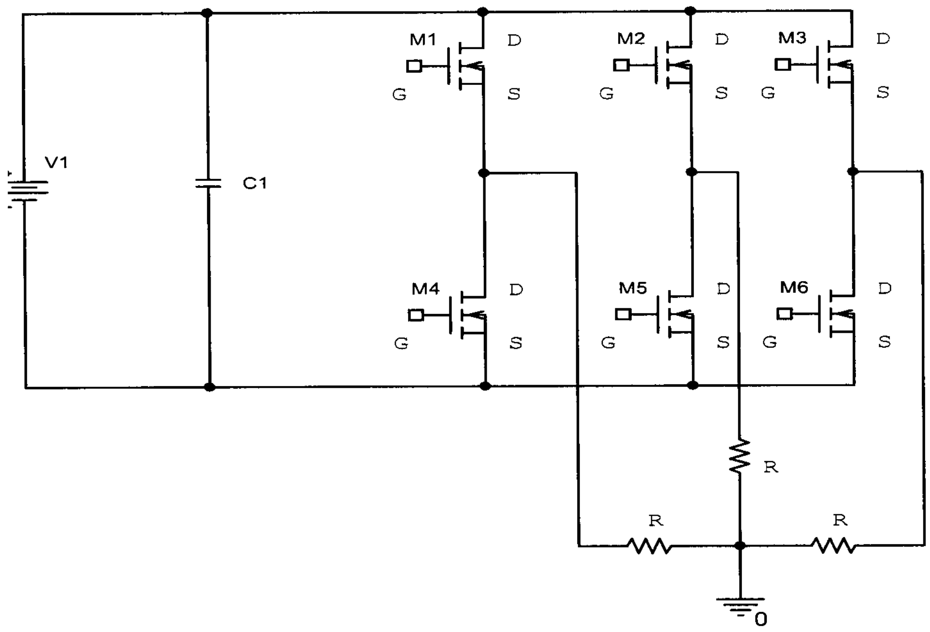


Fig.2.1 Voltage Source Inverter

For applications where over drive is desirable and the available dc voltage is limited, an additional dc-dc boost converter is needed to obtain a desired ac output. The additional power converter stage increases system cost and lowers efficiency. The upper and lower devices of each phase leg cannot be gate on simultaneously either by purpose or by EMI noise. Otherwise a shoot through problem by Electromagnetic interference noise's misgating–on is major killer to the inverter reliability. Dead time to block both upper and lower devices has to provide in the Voltage Source Inverter which causes the waveform distortion, etc.

An output LC filters needed for providing a sinusoidal voltage compared with Current Source Inverter which causes additional power loss and control complexity.

2.1.2 CURRENT SOURCE INVERTER

A Current Source Inverter is fed from a constant current source. Therefore load current remains constant irrespective of the load on the inverter. The load voltage changes as per the magnitude of load impedance. When a voltage source has a large inductance in series with it, it behaves as a Current Source .The large inductance maintains the current constant.

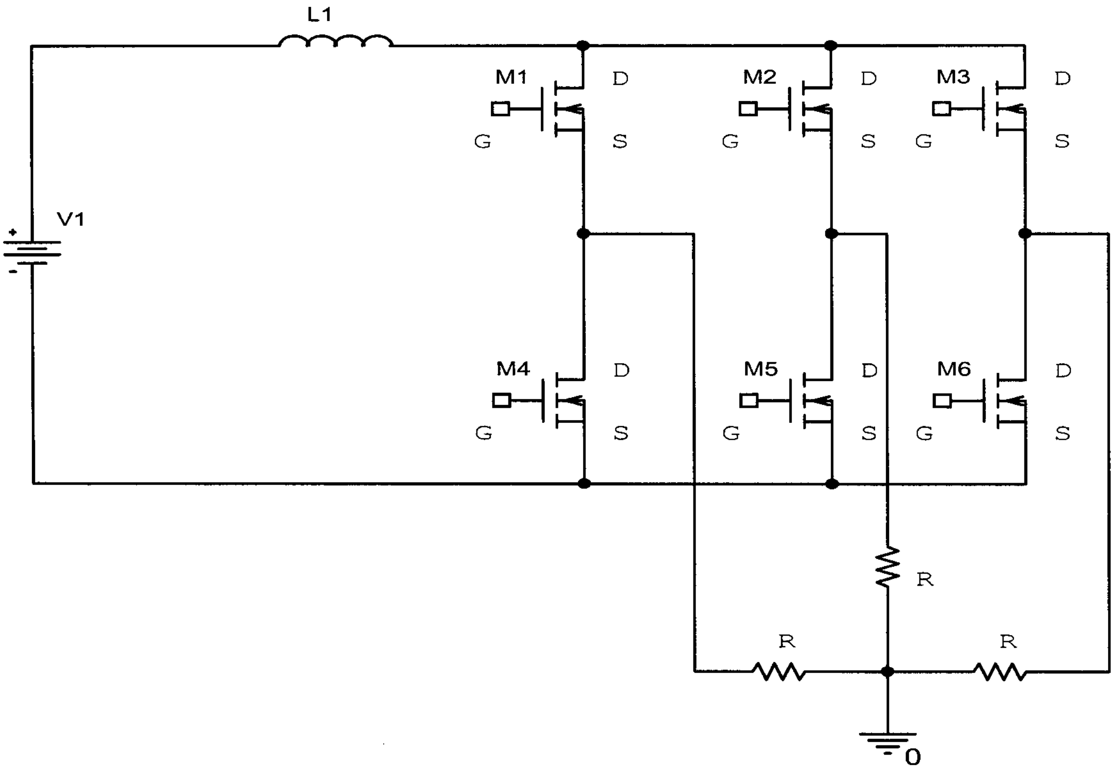


Fig.2.2 Current Source Inverter

The traditional three phase Current Source Inverter structure is shown in Fig.2.2. A dc current source feeds the three phase main inverter circuit. The dc current source can be a relatively large dc inductor fed by a Voltage Source such as a battery or a rectifier. It consists of six switches and with anti parallel diodes. This diode provides the bidirectional current flow and unidirectional voltage blocking capability.

Current Source Inverter has the following conceptual and theoretical barriers and limitations. The ac output voltage has to be greater than the original dc voltage that feeds the dc inductor or the dc voltage produced is always smaller than the ac input voltage. Therefore this inverter is a boost inverter for dc to ac power conversion. For applications where a wide voltage range is desirable, an additional dc to dc buck converter is needed. The additional power conversion stage increases system cost and lowest efficiency.

At least one of the upper devices and one of the lower devices have to be gated on and maintained on at any time. Other wise, an open circuit of the DC inductor would occur and destroy the devices. The open circuit problem by EMI noise's misgatting-off is a major concern of the converters reliability. A current source inverter is fed from a constant current source. Therefore load current remains constant irrespective of the load on the Inverter. The load voltage changes as per the magnitude of load impedance. When a voltage source has a large inductance in series with it, it behaves as a current source .The large inductance maintains the current constant.

2.2 BLOCK DIAGRAM OF THE PROPOSED HARDWARE

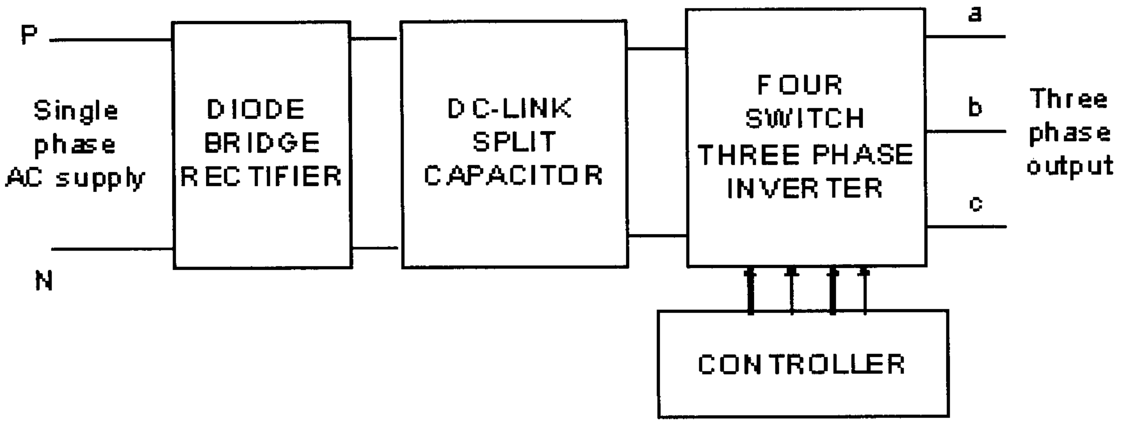


Fig.2.3 Block diagram of the proposed hardware

2.3 PRINCIPLE OF OPERATION

2.3.1 POWER SUPPLY

2.3.1.1 Input supply

Single phase 230V, 50Hz AC supply.

2.3.1.2 Transformer

A transformer is a static piece of which electric power in one circuit is transformed into electric power of same frequency in another circuit. It can raise or lower the voltage in the circuit, but with a corresponding decrease or increase in current. It works with the principle of mutual induction. In our project we are using a step down transformer with transformation ratio 2:1 to providing a necessary supply for the electronic circuits. Here we step down a 230v ac into 100v ac.

2.3.2 DIODE BRIDGE RECTIFIER

A dc level obtained from a sinusoidal input can be improved 100% using a process called full wave rectification. Here in our project for full wave rectification we use bridge rectifier. From the basic bridge configuration we see that two diodes (say D2 & D3) are conducting while the other two diodes (D1 & D4) are in off state during the period t = 0 to T/2.Accordingly for the negative cycle of the input the conducting diodes are D1 & D4 .Thus the polarity across the load is the same. Thus we obtained unregulated dc output voltage.

2.3.3 FILTER

In order to obtain a dc voltage of 0 Hz, we have to use a low pass filter. so that a capacitive filter circuit is used where a capacitor is connected at the rectifier output& a dc is obtained across it. The filtered waveform is essentially a dc regulated voltage with negligible ripples.

2.3.4 FOUR SWITCH THREE PHASE INVERTER

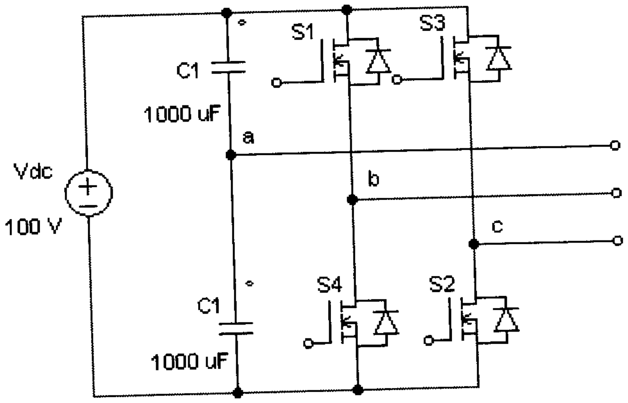


Fig.2.4 Circuit diagram of the proposed hardware

The output side of the proposed single-phase to three phase converter consists of a four switch (S_1 to S_4) inverter. The center point of the capacitors forms the third phase "a." A two leg inverter which gives a three phase VVVF output voltage. For the induction motor drive, the three phase voltage references are given in balanced set. There are two kinds of voltage modulation schemes for the two leg three phase PWM inverter. One is named vector modulation scheme, which uses the phase voltages in calculating the switching time. Here scalar modulation scheme is adopted since it is simple and straight forward.

By controlling the switches S_2 and S_3 in a PWM fashion, the output voltage V_{ca} can be defined. Further, switches S_1 and $S4$ determine the V_{bc} voltage. In order to generate balanced three-phase output voltages, the voltage V_{bc} is phase shifted by -60° from V_{ca}. Thus the control of switches S_1 to S_4 to have -60° phase shift between V_{ca} and V_{bc}, voltages ensures that the third voltage V_{ab} has the same magnitude (fundamental) and proper phase in accordance with the three phase laws.

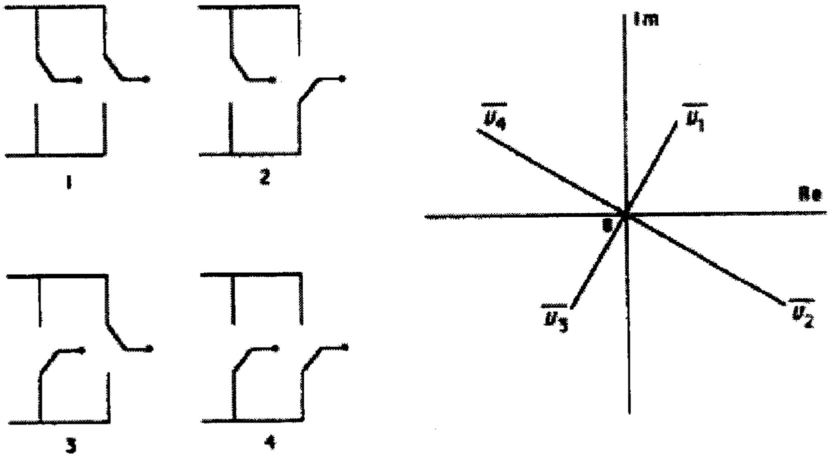


Fig 2.5 Inverter switching state and Voltage vectors

The modulation strategy suggested can produce three phase balanced sinusoidal waveforms at a reduced output voltage of 0.866 compared with the conventional six switch inverter .The line to ground voltages are uniquely determined by the PWM inverter switching according to the voltage or current controller.

2.3.5 MODULATION TECHNIQUES

In this project a fixed DC input voltage from the output of the diode bridge rectifier is given to the Inverter and a controlled AC voltage is obtained at the output by adjusting the ON and OFF period of the power MOSFET's. The PWM technique has the following advantages

- The output voltage control in this method can be obtained without any additional components
- The lower order harmonic can be minimized along with the output voltage control.

The pulse width modulation techniques can be classified mainly as:

(a) Single Pulse Width Modulation

(b) Multiple Pulse Width Modulation

(c) Sinusoidal Pulse Width Modulation

2.3.5 (a) SINGLE PULSE WIDTH MODULATION

The output voltage from the single phase PWM Inverter is shown below .It consists of a pulse of width 2d located symmetrically about n /2 and the another pulse located symmetrically about 3 п /2 .The range of pulse width varies from 0 to п (0<2d< п) .The output voltage is controlled by the pulse width of 2d.The shape of the output voltage is a quasi-square wave.

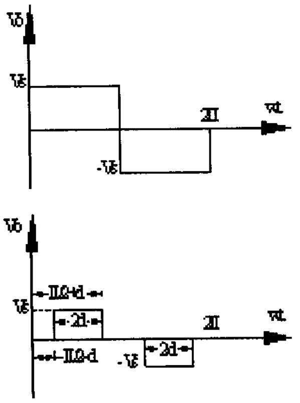


Fig 2.6 Single Phase PWM Output

2.3.5 (b) MULTIPLE PULSE WIDTH MODULATION

The Multiple Pulse Width Modulation uses two symmetric pulses per half cycle. The symmetrical modulated wave form is shown below:

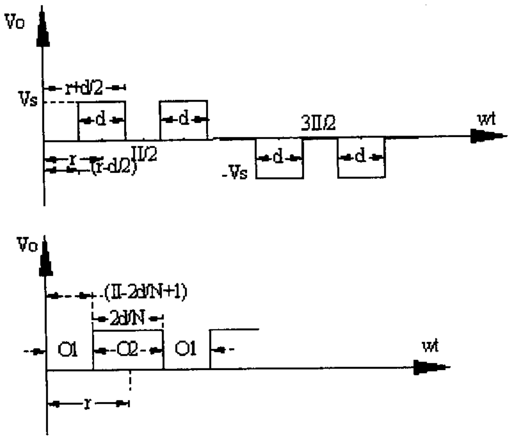


Fig 2.7 Symmetrical modulated wave for Multiple Pulse Width Modulation

This symmetric modulated wave can be generated by comparing an adjustable square voltage wave Vr of frequency ω_c as shown in below:

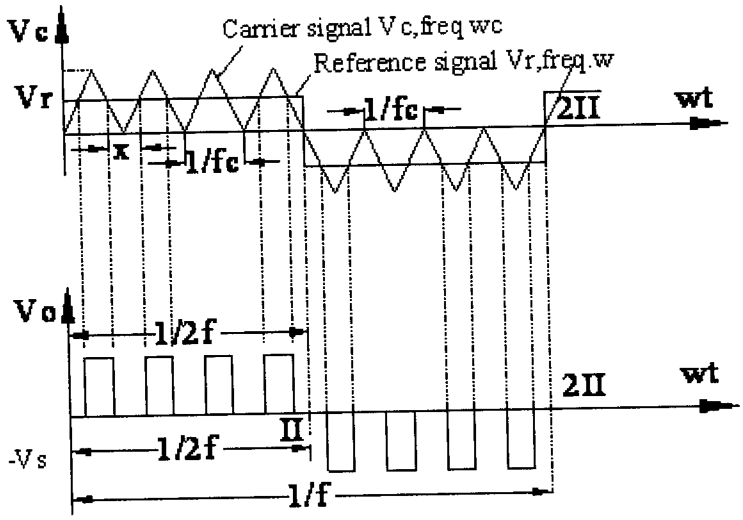


Fig 2.8 Output Voltage waveform with Multiple Pulse Width Modulation

The firing pulse for the power MOSFET is given by the intersection of carrier and reference signal .The firing pulses so generated turn ON the MOSFET so that the output voltage is available during the interval triangular modulating wave exceeds the square modulating wave.

2.3.5 (c) SINUSOIDAL PULSE WIDTH MODULATION

In this modulation, several pulses per half cycle are used. In Multiple Pulse Width Modulation, the pulse width is equal for all pulses whereas in Sinusoidal PWM the pulse width is a sinusoidal function of the angular position of the pulse given in the cycle.

For releasing sine PWM, a higher frequency triangular wave is compared Vc is compared with the sinusoidal reference wave Vr of desired frequency. The value of Vr/Vc is called Modulation Index and it controls the harmonic content of the output waveform. The intersection of Vc and Vr determines the switching instant and commutation of the modulated pulse. The below diagram shows the Sinusoidal PWM:

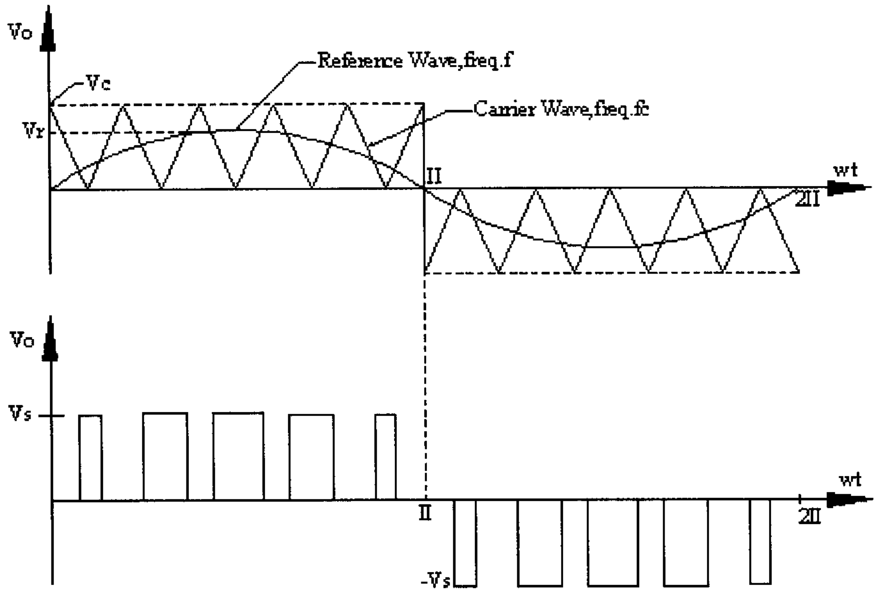


Fig 2.9 Output Voltage waveform with Sinusoidal Pulse Width Modulation

2.3.6 DRIVER CIRCUIT

The driver circuit forms the most important part of the hardware unit because it acts as the backbone of the inverter because it gives the triggering pulse to the switches in the proper sequence.

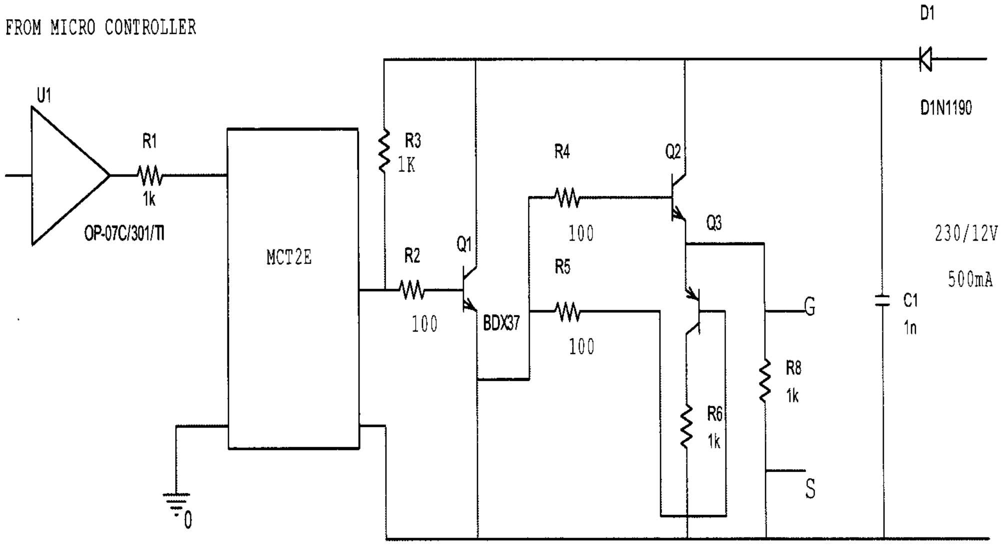


Fig.2.10 Driver circuit

- This driver circuit, which produces amplified, pulses for the Mosfet's power circuit, which uses emitter coupled amplifier circuit to boost the triggering pulse low voltage to the high voltage.
- The MCT2E is an opto coupler IC.
- D1 diode used as a rectifier circuit.
- The Q2 which uses the CK100, and Q3 which uses the 2N2222 transistors.

2.3.6.1 OPTOCOUPLER

Optocoupler is also termed as optoisolator. Optoisolator a device which contains a optical emitter, such as an LED, neon bulb, or incandescent bulb, and an optical receiving element, such as a resistor that changes resistance with variations in light intensity, or a transistor, diode, or other device that conducts differently when in the presence of light. These devices are used to isolate the control voltage from the controlled circuit.

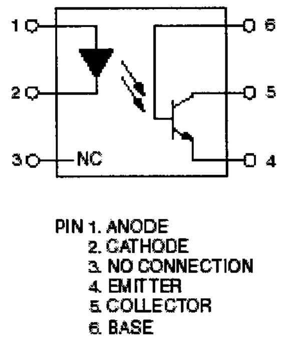


Fig.2.11 Pin details of MC2TE

2.3.7 THREE PHASE LOAD

AC motors operate from alternating current (AC) power sources. The magnetic fields typically are generated using coils on the rotor and stator, and the field movement occurs naturally in the stator due to the alternating nature of the input power. These motors are inexpensive to build and operate, reliable, and usually run from standard line power. The power supply frequency determines the speed of an AC motor, so if operated from line power, the speed of rotation is always the same.

2.3.7.1 SQUIRREL CAGE ROTOR

Most common AC motors use the squirrel cage rotor, which will be found in virtually all domestic and light industrial alternating current motors. The squirrel cage takes its name from its shape - a ring at either end of the armature, with bars connecting the rings running the length of the rotor. It is typically cast aluminum poured between the iron laminates of the rotor, and usually only the end rings will be visible. The vast majority of the rotor currents will flow through the bars rather than the higher-resistance and usually varnished laminates. Very low voltages at very high currents are typical in the bars and rings; high efficiency motors will often use cast copper in order to reduce the resistance in the rotor.

In operation, the squirrel cage motor may be viewed as a transformer with a rotating secondary - when the rotor is not rotating in sync with the magnetic field, large rotor currents are induced; the large rotor currents magnetize the rotor and interact with the stator's magnetic fields to bring the rotor into synchronization with the stator's field. An unloaded squirrel cage motor at synchronous speed will only consume electrical power to maintain rotor speed against friction and resistance losses; as the mechanical load increases, so will the electrical load - the electrical load is inherently related to the mechanical load. This is similar to a transformer, where the primary's electrical load is related to the secondary's electrical load.

This is why, as an example, a squirrel cage blower motor may cause the lights in a home to dim as it starts, but doesn't dim the lights when its fanbelt (and therefore mechanical load) is removed. Furthermore, a stalled squirrel cage motor (overloaded or with a jammed shaft) will consume current limited only by circuit resistance as it attempts to start; overheating and failure will be the result.

A common type of squirrel cage motor is a shaded pole motor, found in most inexpensive low-noise and low-torque applications like fans. Shaded pole motors are inherently inefficient, and most incorporate some form of impedance protection to limit stalled current. With the exception of shaded pole motors, most squirrel cage motors are extremely efficient.Virtually every washing machine, dishwasher, standalone fan, record player, etc. uses some variant of a squirrel cage motor.The core of the rotor is built of a stack of iron laminations. The drawing shows only three laminations of the stack.

CHAPTER III

SIMULATION USING PSIM 7.0.5

CHAPTER III

SIMULATION USING PSIM 7.0.5

3.1 INTRODUCTION TO PSIM SOFTWARE

PSIM 7.0.5 is Power Simulation software specifically designed for Power Electronics and Motor Drives. With fast simulation and user friendly interface, PSIM provides a powerful Simulation environment for power electronics, analog and digital control, magnetic, and motor drive system studies. The PSIM has the following Modules:

1) Motor Drive Module
2) Digital Control Module
3) Sim Coupler Module
4) Thermal Module
5) MagCoupler Module
6) MagCoupler-RT Module

- The Motor Drive Module has built-in machine models and mechanical load models for motor drive system studies.
- The Digital Control Module provides discrete elements such as zero-order hold, z domain transfer function blocks, quantization blocks, digital filters, for digital control system analysis.
- The SimCoupler Module provides interface between PSIM and Matlab/Simulink for co-simulation.
- The Thermal Module provides the capability to calculate semiconductor devices losses.
- The MagCoupler Module provides interface between PSIM and the electromagnetic field analysis software JMAG for co-simulation.
- The MagCoupler-RT Module links PSIM with JMAG-RT data files. In addition, PSIM supports links to third-party software through custom DLL blocks.

The overall PSIM environment is shown below.

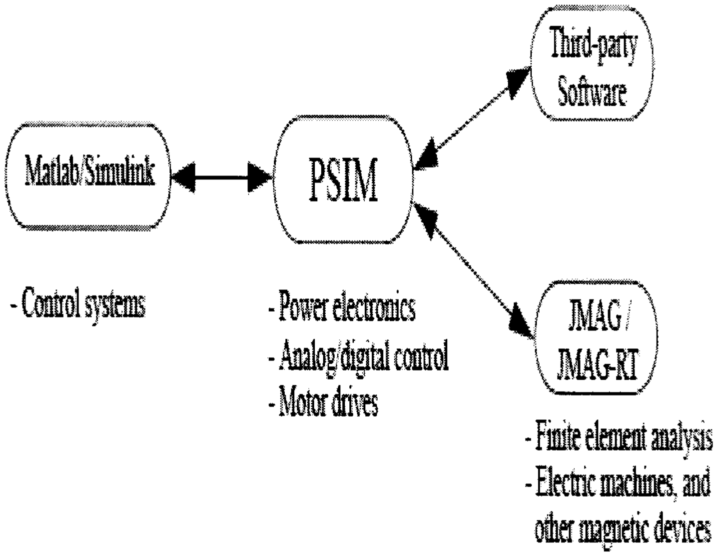


Fig 3.1 Overall PSIM environment

The PSIM simulation environment consists of the circuit schematic program PSIM, the Simulator engine, and the waveform processing program Simview.

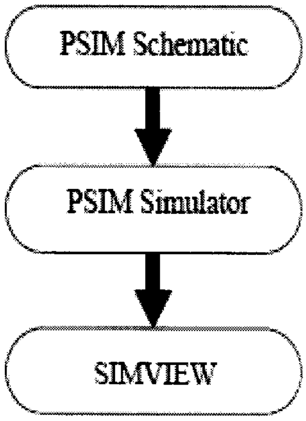


Fig 3.2 Simulation Process of PSIM

The circuit schematic is used to draw the circuits; the simulator engine is used for the simulation of the circuits drawn and the Simview is used to see the simulated outputs.

3.2 OVERALL CIRCUIT DIAGRAM

The simulation circuit for the four switch three phase inverter along with diode bridge rectifier is shown below. The simulated circuit clearly depicts that single phase is converted into three phase using four switch inverter.

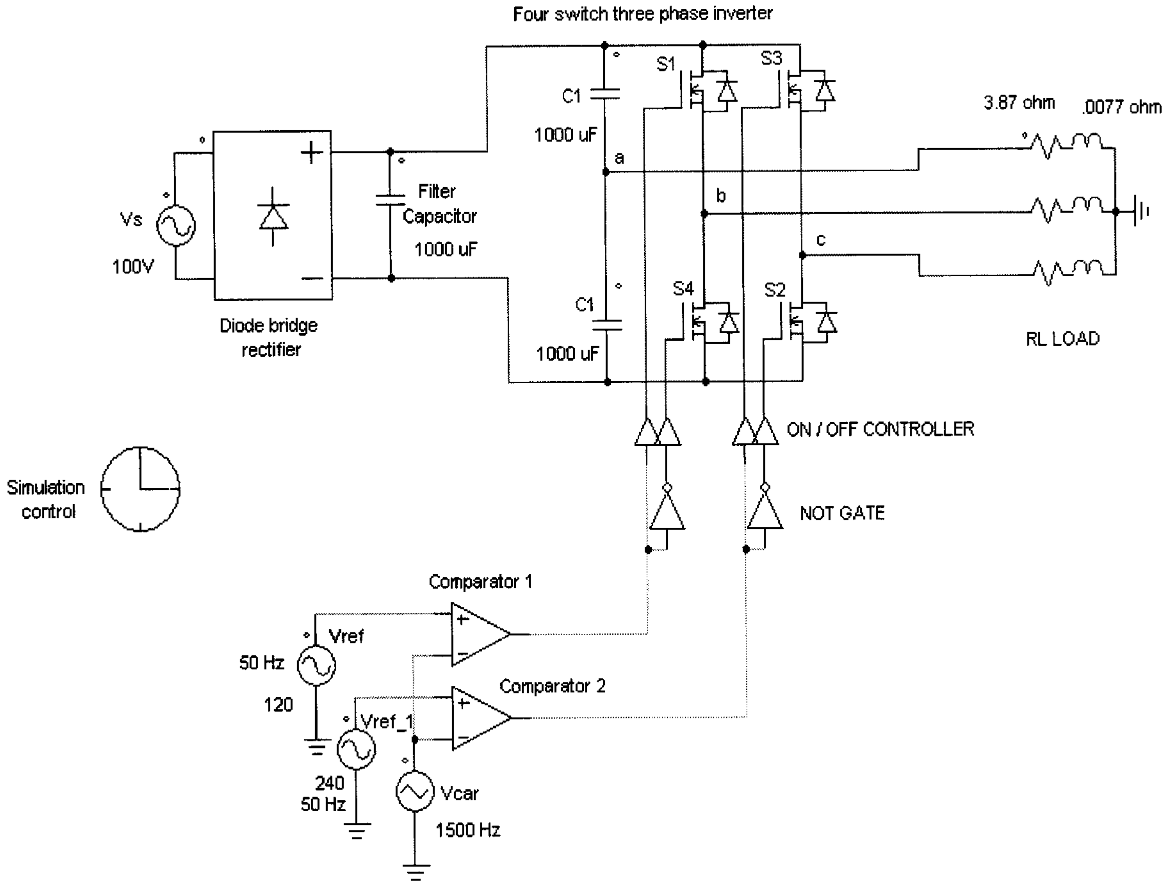


Fig 3.3 Overall simulation circuit using **PSIM 7.0.5**

3.3 SIMULATION OF BRIDGE DIODE RECTIFIER

The simulation circuit for the single phase Diode Bridge Rectifier is shown below. The single phase ac supply 230 V , 50 Hz is given to transformer primary side. The step down transformer converts 230 V into 100 V , 50 Hz. The secondary side voltage is fed into single phase diode bridge rectifier .The output voltage Vr is a rectified DC voltage (Unregulated).

The simulation circuit and the results of diode bridge rectifier with unregulated dc output voltage are follows.

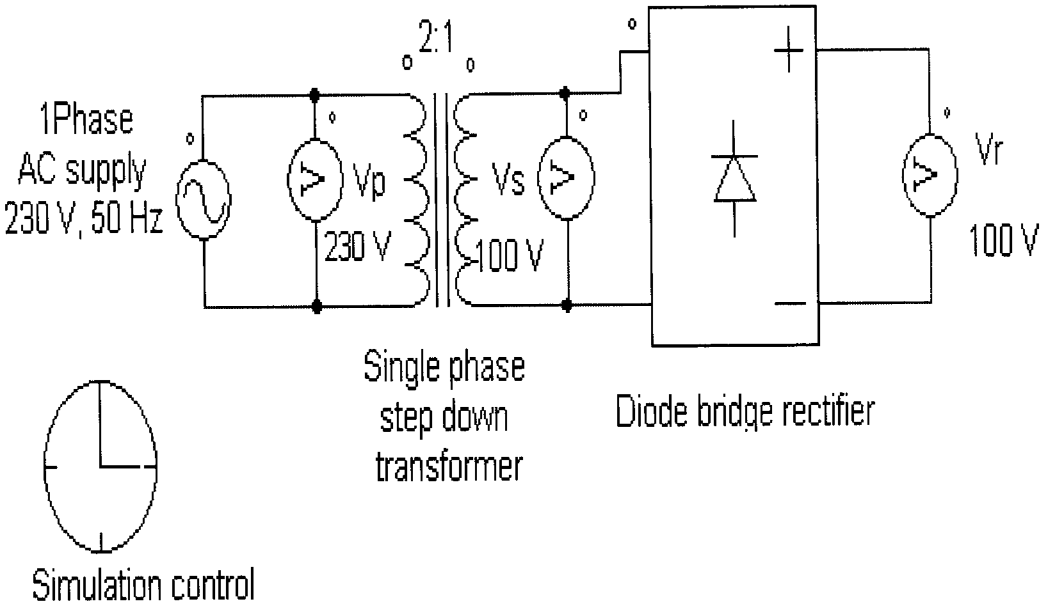
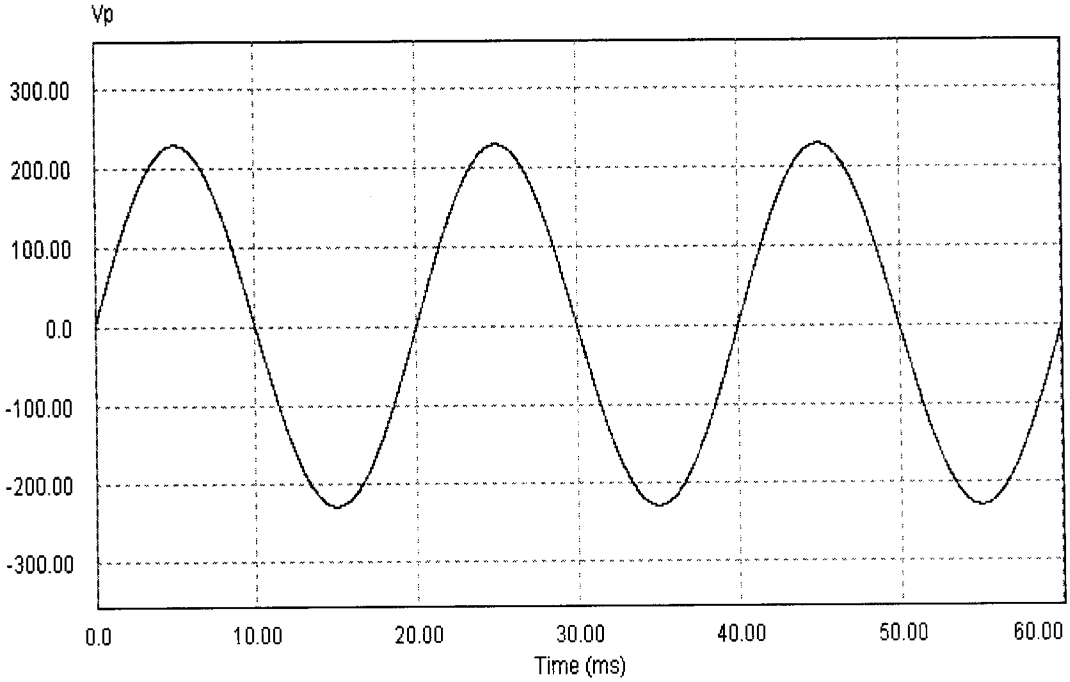
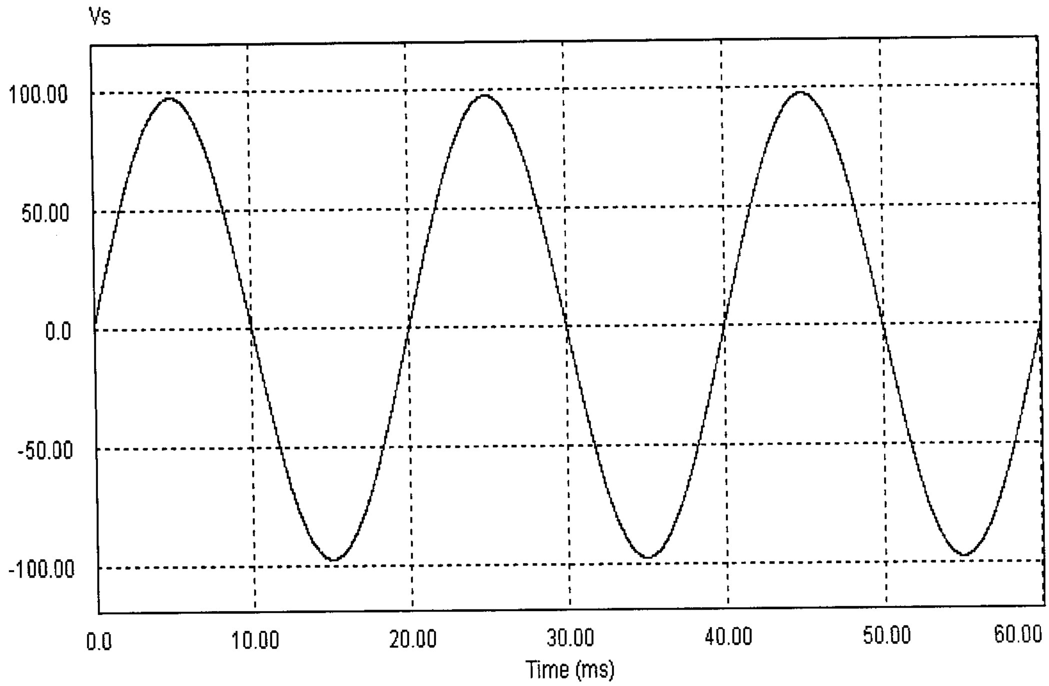


Fig 3.4 Simulation Circuit of Diode Bridge Rectifier



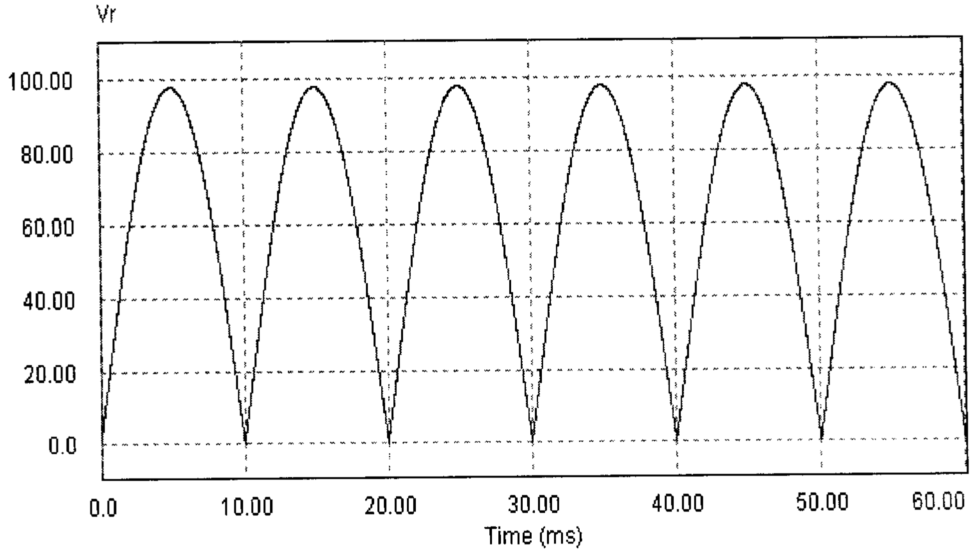
X axis – time (ms)   Y axis – Transformer primary voltage, volts

Fig 3.5 Simulated input supply voltage waveform



X axis – time (ms)   Y axis – Transformer secondary voltage, volts

Fig 3.6 Simulated output voltage waveform of transformer secondary



X axis – time (ms)   Y axis – Unregulated DC voltage, volts

Fig 3.7 Simulated output voltage waveform of Diode Bridge Rectifier

The output obtained from single phase diode bridge rectifier is an unregulated output voltage Vr. By passing through low pass filter the regulated dc output voltage Vdc is obtained . The simulation circuit of single phase diode bridge rectifier with filter capacitor and the simulation results are shown below

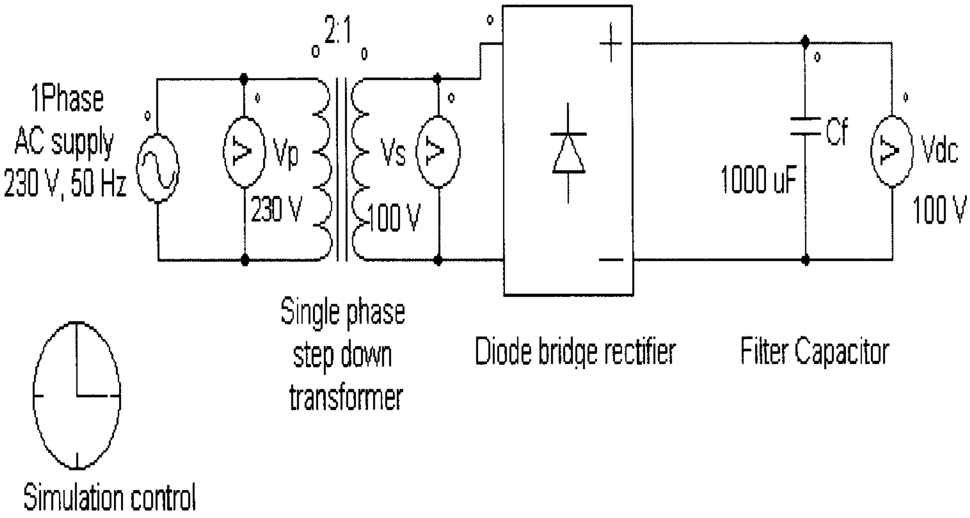
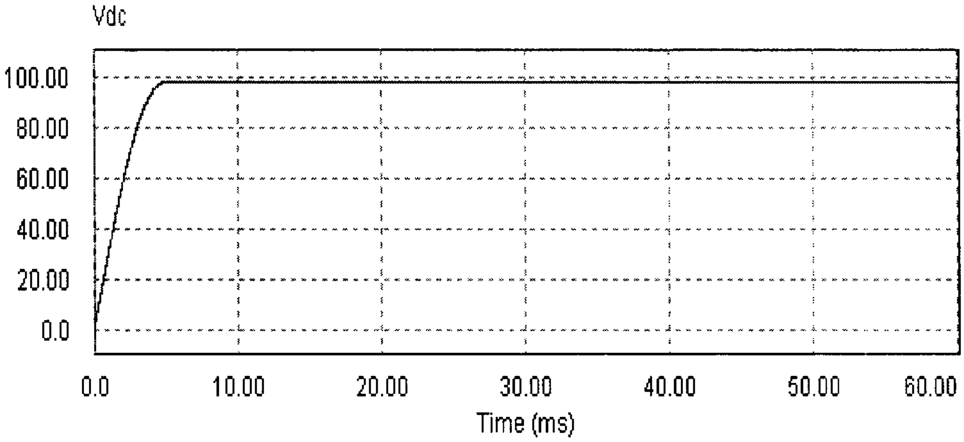


Fig 3.8 Simulation Circuit of Diode Bridge Rectifier with filter capacitor



X axis – time (ms) Y axis – Constant DC voltage, volts

Fig 3.9 Simulated output voltage waveform of filter capacitor

3.4 SIMULATION OF PROPOSED THREE PHASE INVERTER

The simulation circuit of four switch inverter with dc link split capacitor is developed with input dc supply of 100V. The output side of the proposed single-phase to three phase converter consists of a four switch (S_1 to S_4) inverter. The center point of the capacitors forms the third phase "a." A two leg inverter which gives a three phase VVVF output voltage. The obtained three phase output is fed to a three phase RL load (for ex. induction motor). The switches are triggered in PWM fashion.

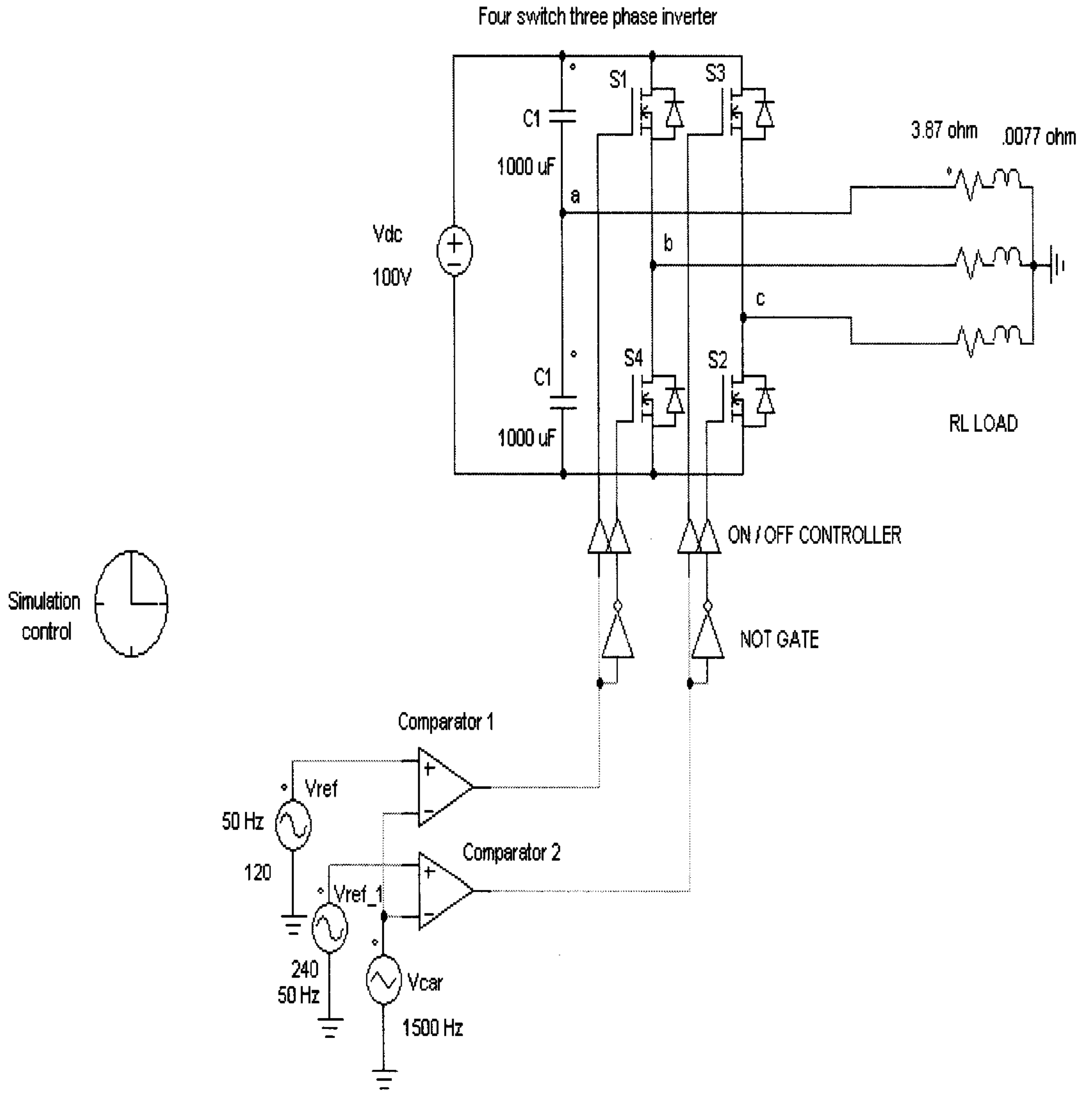


Fig 3.10 Simulation circuit for the four switch three phase inverter

Gate pulse to the inverter can be done using sinusoidal PWM technique. Here triangular wave is carrier signal with 1.5 KHz frequency. With 120 degree phase displacement and 50 Hz frequency sinusoidal wave is used for reference signal.The simulation results of gating pulses to the inverter switches are shown below. The width of the pulse is changed according to the amplitude of the sine wave reference

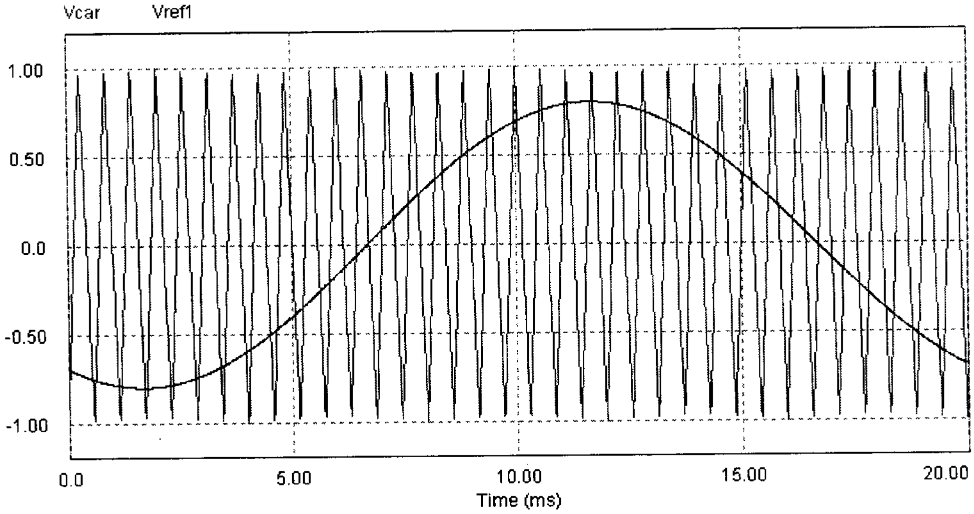


Fig 3.11 Reference and carrier signal waveforms of Comparator 1

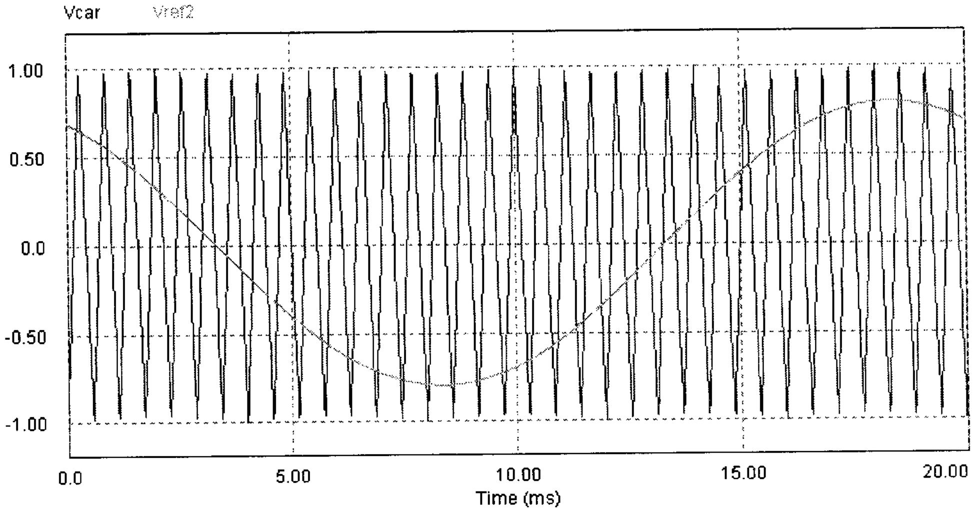
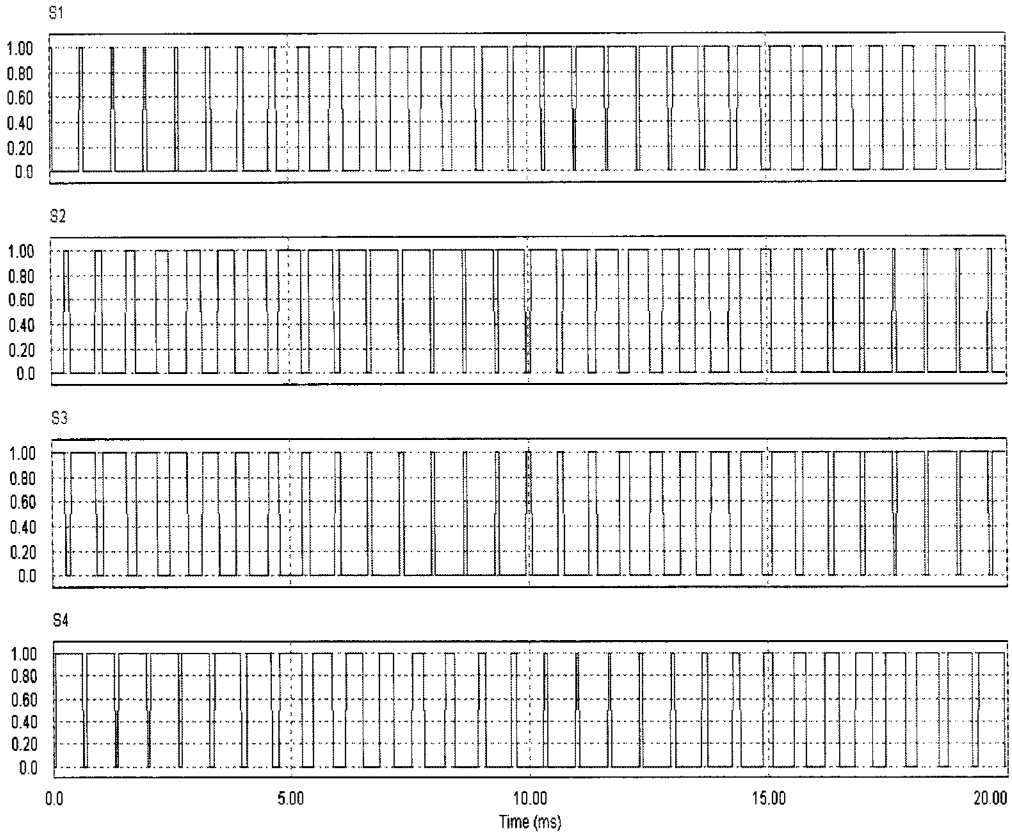


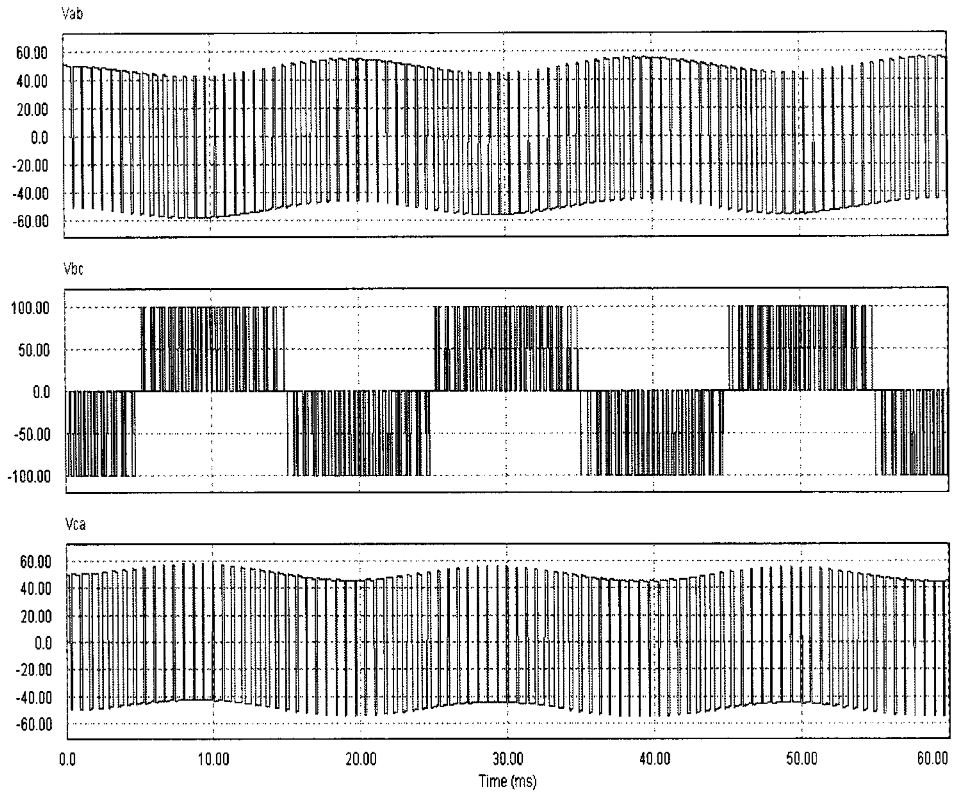
Fig 3.12 Reference and carrier signal waveforms of Comparator 2



X axis – time (ms)   Y axis –Gating pulses, volts

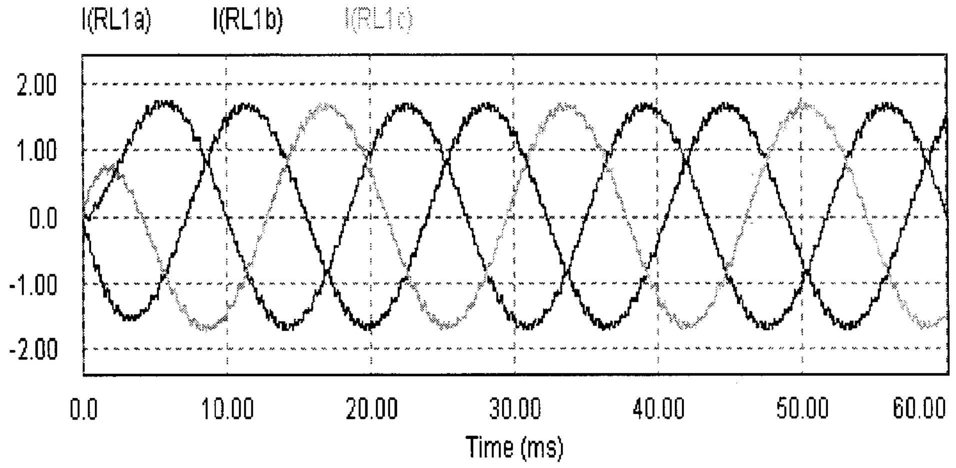
Fig 3.13 PWM pulse pattern to inverter switches

By controlling the switches S_1 and S_4 in a PWM fashion, the output voltage V_{ab} can be defined. Further, switches S_2 and S_3 determine the V_{ca} voltage. In order to generate balanced three-phase output voltages, the voltage V_{bc} is phase shifted by -60° from V_{ca}. Thus the control of switches S_1 to S_4 to have *-60* ° phase shift between V_{ca} and V_{ab}, voltages ensures that the third voltage V_{bc} has the same magnitude (fundamental) and proper phase in accordance with the three phase laws. Fig 3.14 and 3.15 illustrates the inverter output voltages V_{ab}, V_{bc}, V_{ca} and the line currents for an RL load. It is noted that voltage V_{bc} is a three-level PWM swinging between $V_{0/2}$, 0, and - $V_{0/2}$. On the other hand, the voltages V_{ab} and V_{ca} are the two-level type swinging between $V_{0/2}$ and- $V_{0/2}$. Further, the fundamental content is the same in the three-phase output voltages.



X axis – time (ms) Y axis – Inverter O/P voltage, volts

Fig 3.14 Simulation results of proposed inverter output voltage



X axis – time (ms) Y axis - Inverter O/P current, Amps

Fig 3.15 Simulation result of proposed inverter output current

CHAPTER IV

EMBEDDED PART

CHAPTER IV

EMBEDDED PART

4.1 NEED FOR THE MICROCONTROLLER

PWM Inverter are controlled using PIC16F877A microcontroller .In this project , PWM Inverter uses a separate PIC 16F877A.Since the pulse generated from PIC microcontroller cannot drive the MOSFET's of the power circuit ,a driver circuit is needed. Thus the pulses generated from the PIC microcontroller are increased to a higher voltage level using driver circuits.

4.2 PIN CONFIGURATION OF PIC16F877A

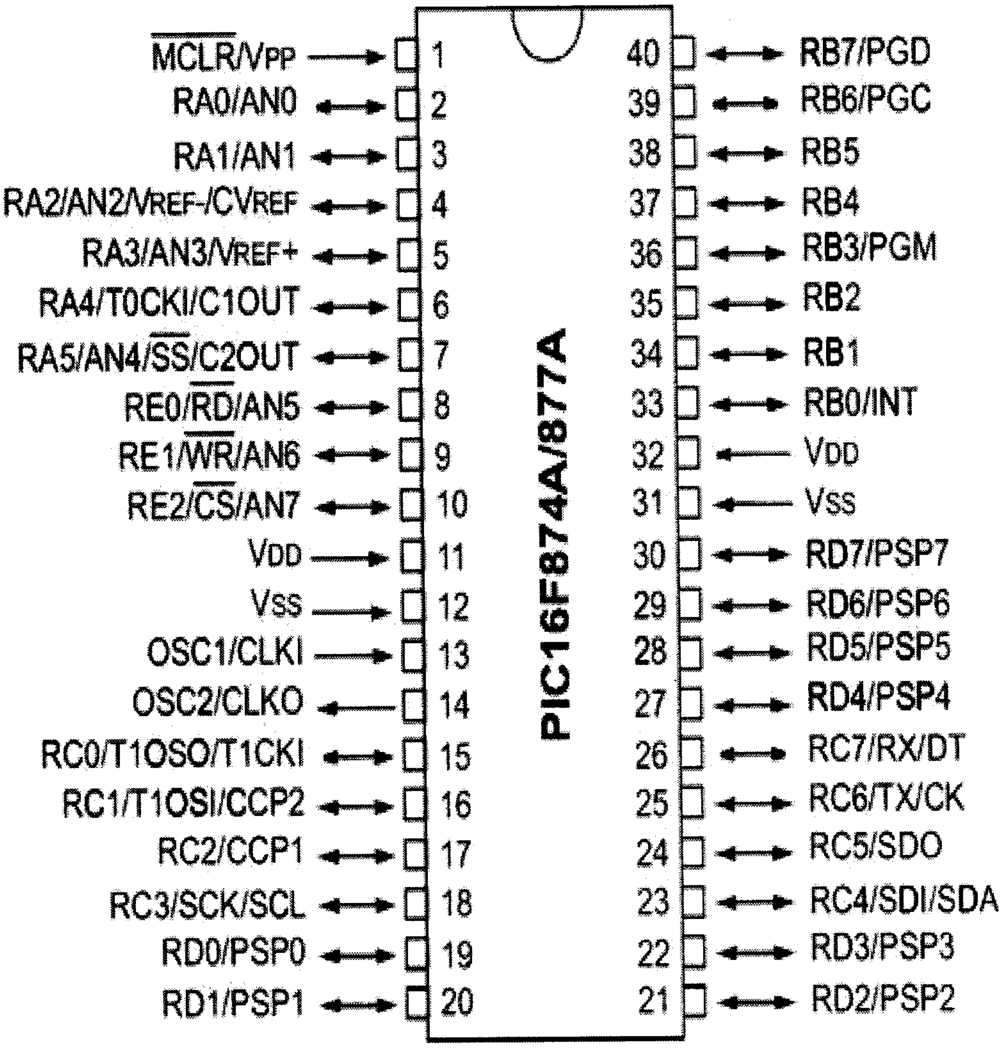


Fig 4.1 Pin Diagram of PIC 16F877A

4.3 FEATURES OF THE MICROCONTROLLER PIC16F877A

The microcontroller has the following features:

- High-performance RISC CPU
- All single cycle instructions except for program branches which are two cycle
- It has up to 8K x 14 words of FLASH Program Memory,
- It has up to 368 x 8 bytes of Data Memory (RAM)
- It has up to 256 x 8 bytes of EEPROM data memory
- Direct, indirect and relative addressing modes
- Power-on Reset (POR)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Power saving SLEEP mode
- Selectable oscillator options
- Low-power, high-speed CMOS FLASH/EEPROM technology
- Single 5V In-Circuit Serial Programming capability
- Wide operating voltage range: 2.0V to 5.5V

4.4 PERIPHERAL FEATURES OF THE MICROCONTROLLER PIC16F877A

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler, can be incremented during sleep via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules
- Capture is 16-bit, max. resolution is 12.5 ns
- Compare is 16-bit, max. resolution is 200 ns
- PWM max. resolution is 10-bit
- 10-bit multi-channel Analog-to-Digital converter
- Synchronous Serial Port (SSP) with SPI (Master Mode) and I2C (Master/Slave)
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with 9-bit address detection

- Parallel Slave Port (PSP) 8-bits wide, with external RD, WR and CS controls
- Brown-out detection circuitry for Brown-out Reset (BOR)

4.5 MEMORY ORGANIZATION

The PIC16F877A has a 13-bit program counter capable of addressing an 8K x 14 program memory space. The PIC16F877A devices have 8K x 14 words of FLASH program memory. Accessing a location above the physically implemented address will cause a wraparound. The reset vector is at 0000h and the interrupt vector is at 0004h.

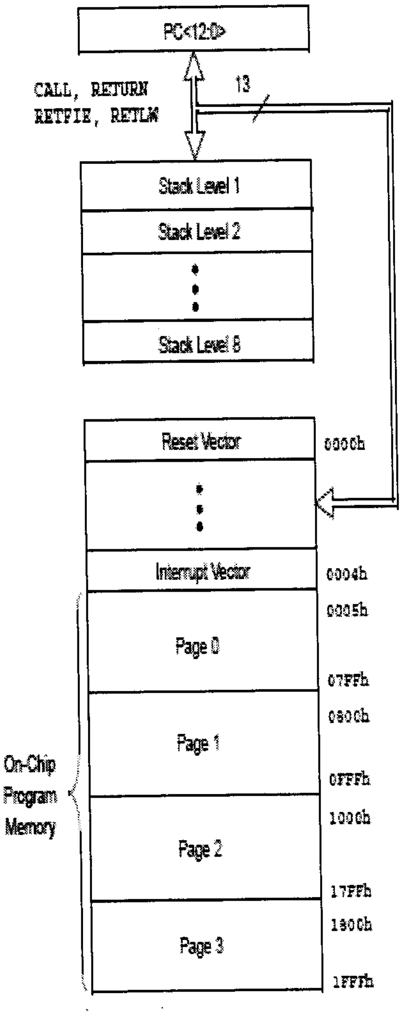


Fig 4.2 Memory Organization of PIC 16F877A

4.6 FLASH PROGRAM MEMORY

The Data EEPROM and FLASH Program Memory are readable and writable during normal operation over the entire VDD range. The data memory is not directly mapped in the register file space. Instead it is indirectly addressed through the Special Function Registers (SFR). There are six SFRs used to read and write the program and data EEPROM memory. These registers are:

- EECON1
- EECON2
- EEDATA
- EEDATH
- EEADR
- EEADRH

The PIC 16F877A also has three timers namely:

- Timer 0 Module
- Timer 1 Module
- Timer 2 Module

4.6(a) TIMER 0 MODE

Timer mode is selected by clearing bit T0CS (OPTION_REG 5). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler).Counter mode is selected by setting bit T0CS (OPTION_REG 5). In counter mode, Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the Timer0 Source Edge Select bit T0SE of (OPTION_REG 4). Clearing bit T0SE selects the rising edge. The prescaler is mutually exclusively shared between the Timer0 module and the watchdog timer.

4.6(b) TIMER 1 MODE

The Timer1 module is a 16-bit timer/counter consisting of two 8-bit registers (TMR1H and TMR1L), which are readable and writable. The TMR1 Register pair (TMR1H:TMR1L) increments from 0000h to FFFFh and rolls over to 0000h.

Timer1 can operate in one of two modes:

- As a timer
- As a counter

The operating mode is determined by the clock select bit, TMR1CS (T1CON 1).

In timer mode, Timer1 increments every instruction cycle. In counter mode, it increments on every rising edge of the external clock input. Timer1 can be enabled/disabled by setting/clearing control bit TMR1ON (T1CON 0).

4.6(c) TIMER 2 MODE

Timer 2 is an 8-bit timer with a prescaler and a postscaler. It can be used as the PWM time-base for the PWM mode of the CCP module(s). The TMR2 register is readable and writable, and is cleared on any device reset. The Timer2 module has an 8-bit period register PR2.Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to FFh upon reset.

4.7 CAPTURE/COMPARE/PWM MODES

Each Capture/Compare/PWM (CCP) mode contains a 16-bit register which can operate as a:

- 16-bit Capture register
- 16-bit Compare register
- PWM master/slave Duty Cycle register

Both the CCP1 and CCP2 modules are identical in operation, with the exception being the operation of the special event trigger.

4.7(a) CCP 1 MODE

Capture/Compare/PWM Register1 (CCPR1) is comprised of two 8-bit registers: CCPR1L (low byte) and CCPR1H (high byte). The CCP1CON register controls the operation of CCP1. The special event trigger is generated by a compare match and will reset Timer1.

4.7(b) CCP 2 MODE

Capture/Compare/PWM Register 2 (CCPR2) is comprised of two 8-bit registers: CCPR2L (low byte) and CCPR2H (high byte). The CCP2CON register controls the operation of CCP2. The special event trigger is generated by a compare match and will reset Timer 2 and start an A/D conversion.

4.7(c) PWM MODE

In pulse width modulation mode, the CCPx pin produces up to a 10-bit resolution PWM output. Since the CCP1 pin is multiplexed with the PORT C data latch, the TRISC 2 bit must be cleared to make the CCP1 pin an output. The Block Diagram of the PWM Mode and the PWM output is given below:

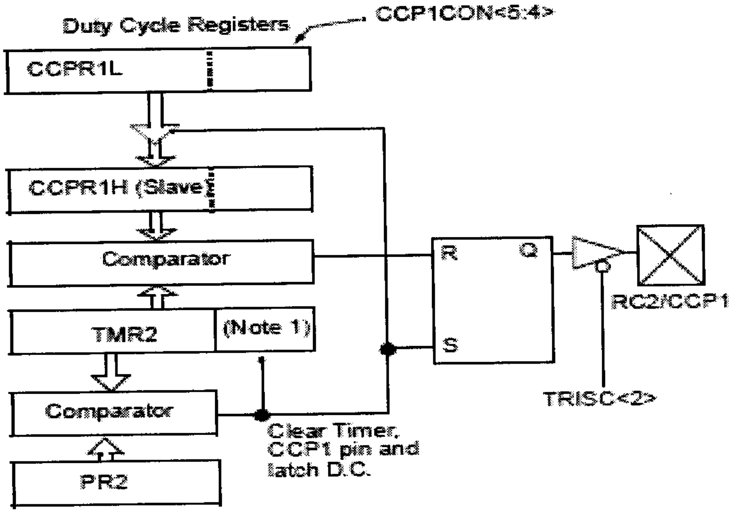


Fig 4.3 Functional Block Diagram of PWM operation

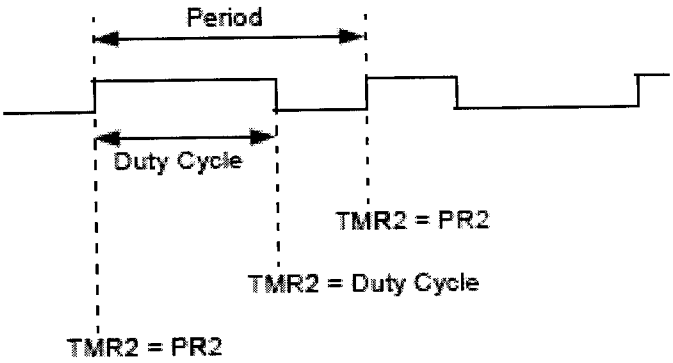


Fig 4.4 PWM output

A PWM output has a time-base (period) and a time that the output has high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).

The PWM period is specified by writing to the PR2 register. The PWM period is calculated using the following formula:

PWM period = [(PR2) + 1] * 4 *TOSC

4.7(d) PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON 5, 4 bits. Up to 10-bit resolution is available. The CCPR1L contains the eight MSBs and the CCP1CON5, 4 contains the two LSBs. This 10-bit value is represented by CCPR1L:CCP1CON 5, 4.

The following equation is used to calculate the PWM duty cycle in time:

PWM duty cycle = (CCPR1L:CCP1CON 5, 4) * Tosc * (TMR2 prescale value)

CCPR1L and CCP1CON 5,4 can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read-only register.

The following steps should be taken when configuring the CCP module for PWM operation:

1. Set the PWM period by writing to the PR2 register.
2. Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON 5, 4 bits.
3. Make the CCP1 pin an output by clearing the TRISC 2 bit.
4. Set the TMR2 prescale value and enable Timer2 by writing to T2CON.
5. Configure the CCP1 module for PWM operation.

4.8 PIC 16F877A MICROCONTROLLER TO DRIVE PWM INVERTER

In this part of the PWM Inverter port B and port C Timer 0 and TRISB registers are initialized. The PWM pulses are generated from RB4, RB5, RB6, and RB7 of port B. By adjusting the time delay generated from the microcontroller suitable triggering pulses are given to the power MOSFET to get turn ON and turn OFF.

For this adjustment of the time delay embedded C codes are written in the microcontroller .This embedded C is compiled in MPLAB IDE. The debugger used is In- Circuit Debugger ICD 2.

4.8.1 DRIVER CIRCUIT FOR PWM INVERTER

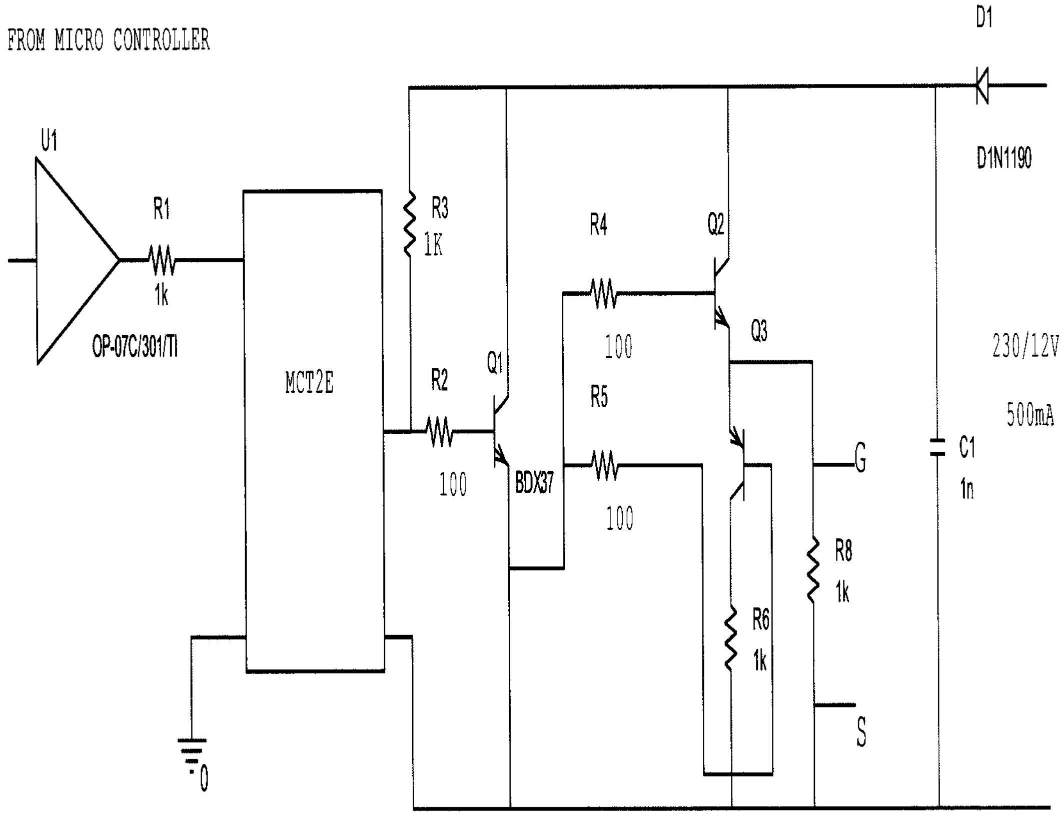


Fig 4.5 Circuit Diagram to drive power MOSFET'S of PWM Inverter

4.8.2DRIVER CIRCUIT OPERATION FOR PWM INVERTER

In order to give triggering pulse to the power MOSFET'S for PWM Inverter, the triggering pulse are generated from PB4, PB5, PB6 and PB7 of port B. These output pins drive the transistor BC 547. Depending on the output voltage (Logic 0 or Logic 1) the transistor gets turn ON and turn OFF. The voltage thus obtained is isolated by using optocoupler IC 6N135.The purpose of the isolation is to give constant output voltage to drive the power MOSFET'S so that the variation in the input voltage will not affect the output voltage .Thus the isolated output voltage now drives the other transistor BC 547 and gives the triggering pulse to the power MOSFETS.

4.8.3 FLOW CHART OF THE MICROCONTROLLER OPERATION IN PWM INVERTER

The following flowchart explains PWM operation of an inverter gating signal used in PIC 16F877A.Each gating pulses are initialized in the port accumulator and the timer loop is started from zero. When the assigned condition is not satisfied then counter loop increases by one value. The process comes to end only the conditions are satisfied

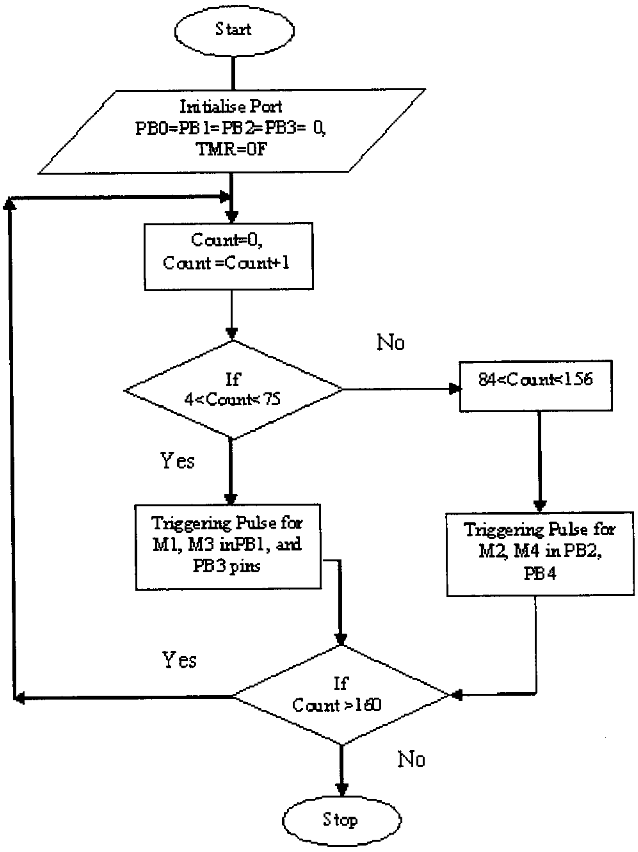


Fig 4.6 Flow Chart for PWM Inverter Operation

4.8.4 PROGRAM CODING FOR PWM INVERTER OPERATION

The following coding clearly depicts the operation of PWM gating pulse to the inverter.

```
#include<pic.h>
static bit p1 @ ((unsigned) &PORTB*8+0);
static bit p2 @ ((unsigned) &PORTB*8+1);
```

```
static bit p3 @ ((unsigned) &PORTB*8+2);
static bit p4 @ ((unsigned) &PORTB*8+3);
unsigned int count;
void main()
{
TRISC=0x0f;                                    // Port C as o/p port
TRISB=0x00;
p1=p2=p3=p4=0;
count=0;
GIE=1;      // enable global interrupt
PEIE=1;     // enable peripheral interrupt
T0IE=1;     // enable timer0 interrupt
OPTION = 0x01;          // set prescale (00)
TMR0 = 0xfc;            // timer reg set value for ten micro sec F7

while (1)
{
}
}
void interrupt timer(void)
{
 if(T0IF=1)
 {
  T0IF=0;
  count++;
          if(count>160) count=0;
          if(count>=4&&count<=75) p3=p1=1;
          else p3=p1=0;
          if(count>=84&&count<=156) p4=p2=1;
          else p4=p2=0;
  TMR0 = 0Xfc;
 }
 }
```

CHAPTER V

HARDWARE DESCRIPTION

CHAPTER V
HARDWARE DESCRIPTION

5.1 HARDWARE PHOTOGRAPHS

The single phase ac supply 230 V, 50 Hz is given to transformer primary side. The step down transformer converts 230 V into 100 V, 50 Hz. The secondary side voltage is fed into single phase diode bridge rectifier .The output voltage Vr is a rectified DC voltage (Unregulated). The output obtained from single phase diode bridge rectifier is an unregulated output voltage. By passing through low pass filter the regulated dc output voltage is obtained.

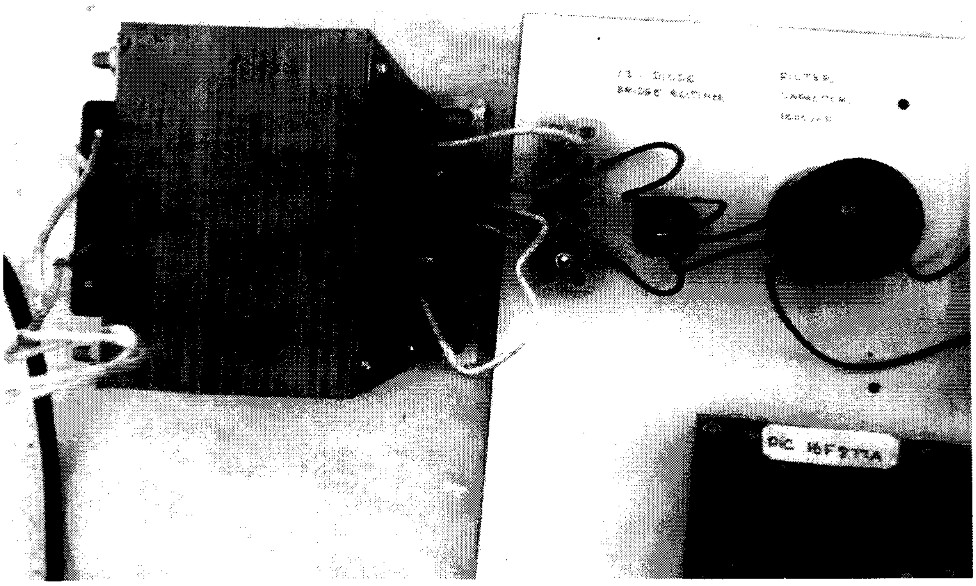


Fig 5.1 Single -Phase Diode Bridge Rectifier hardware setup

The power MOSFET used for four switch three phase PWM Inverter is IRFP 460 which has voltage rating and current ratings as 500V, 20A respectively. The split capacitors used in four switch three phase inverter are 1000 μF each. The constant DC voltage of 100V is given as input to the three phase PWM Inverter.

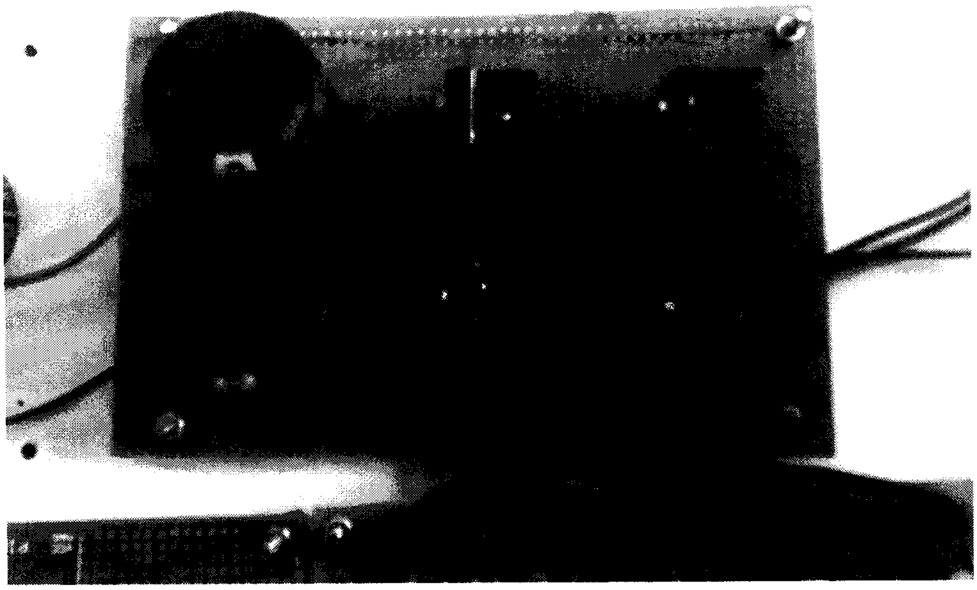


Fig 5.2 Four switch three phase PWM inverter hardware setup

The driver circuit, which produces amplified pulses for the MOSFET's power circuit, which uses emitter coupled amplifier circuit to boost the triggering pulse low voltage to the high voltage.

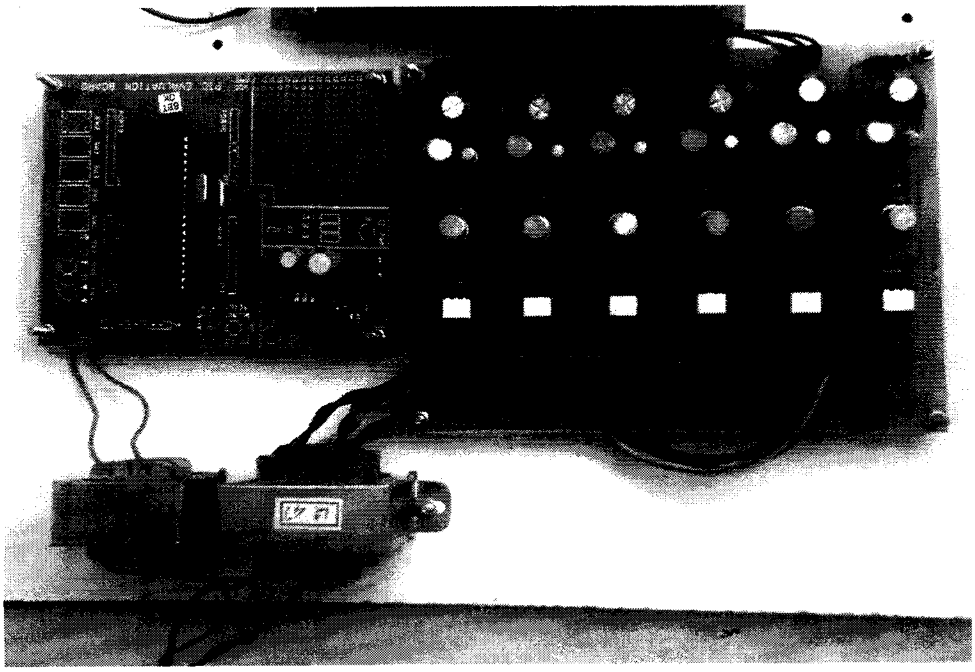


Fig 5.3 PIC16F877A and optocoupler hardware setup

The MCT2E is used as an opto coupler IC for isolating purpose and hence the MOSFET switches are protected during dangerous condition. The CK100 and 2N2222 are two transistors forms Darlington pair

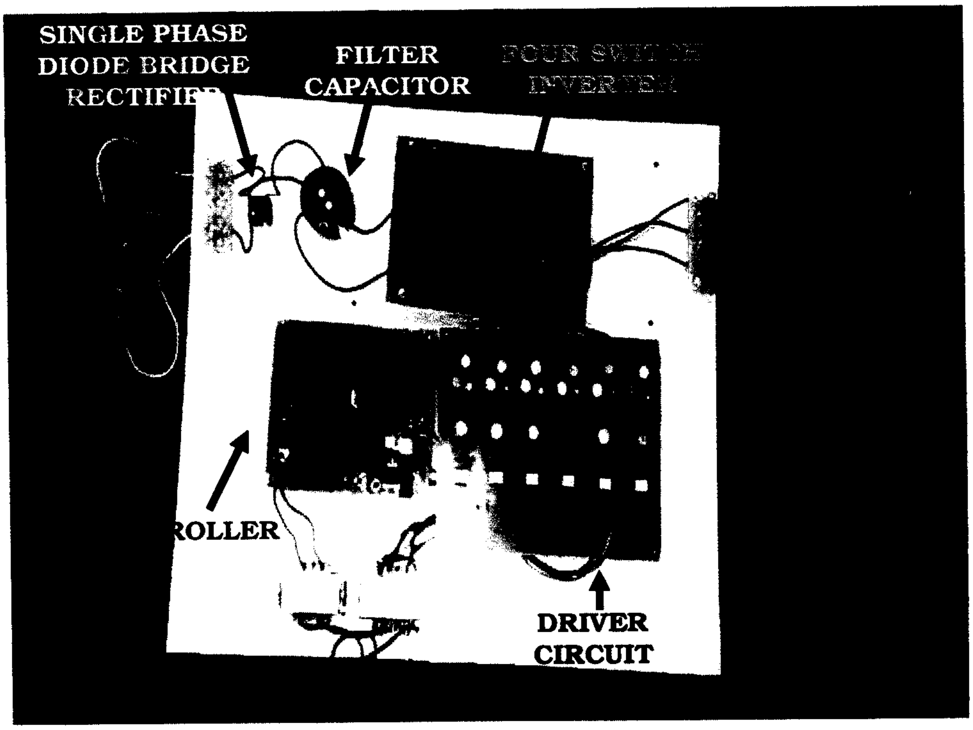


Fig 5.4 Complete circuit hardware setup

5.2 HARDWARE RESULTS

The PWM pulse generated from the Microcontroller is given below.

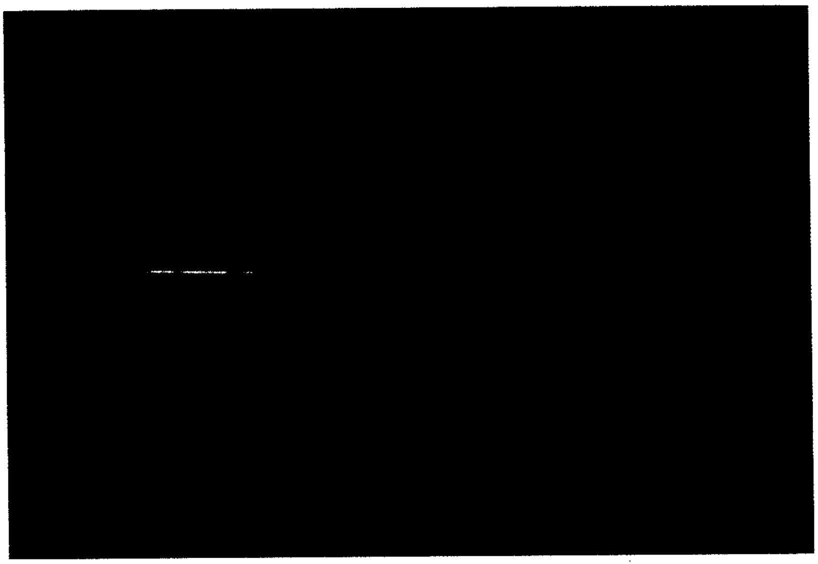


Fig 5.5 CRO output waveform of PWM Pulse

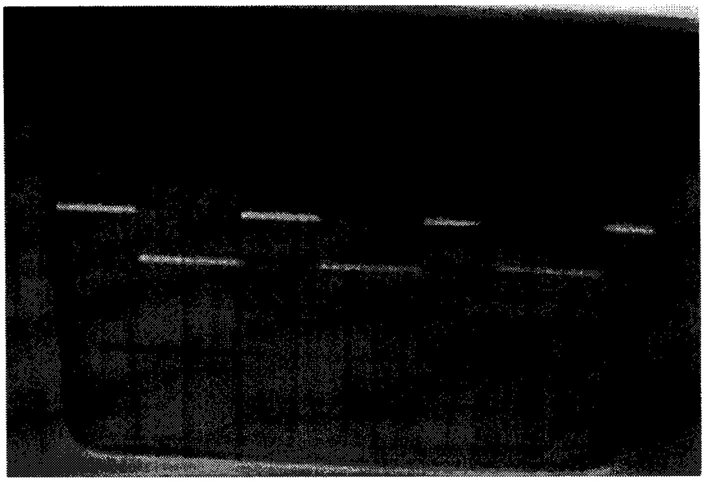


Fig 5.6 CRO output waveform of PWM Pulse

CHAPTER VI

CONCLUSION AND FUTURE SCOPE

CHAPTER VI

CONCLUSION AND FUTURE SCOPE

6.1 CONCLUSION

In this project, the power electronics control mechanism is carried out for the inverter-fed ac motor drives using PWM techniques. Here the concept of diode bridge rectifier and three phase four switch PWM inverter is implemented both in hardware and software. Both the hardware and software results are found to be satisfactory. The output is connected to ac motor load as a part of consumer requirement. The simulations are carried out using the simulation software **PSIM 7.0.5.**

6.2 FUTURE SCOPE

In the future scope of the work, the concept of four switch PWM inverter can be implemented for closed loop control of ac motor drives. Also the power electronics switches can be modified by using IGBT for utility interface of variable speed wind turbine generators.

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REFERENCES

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[11] www.powersimtech.com

[12] www.microchip.com

APPENDIX A

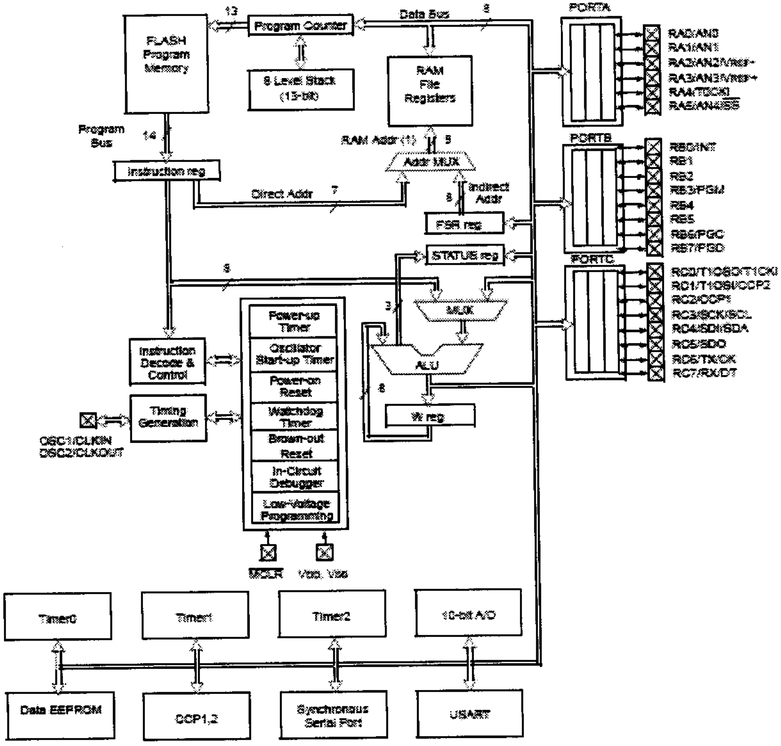
PIC 16F877A

APPENDIX A

PIC 16F877A

ARCHITECTURE OF PIC 16F877A

Device	Program FLASH	Data Memory	Data EEPROM
PIC16F873	4K	192 Bytes	128 Bytes
PIC16F876	8K	368 Bytes	256 Bytes



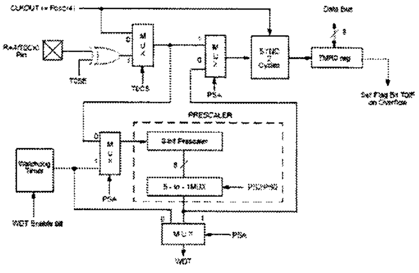
TIMER 0 CONTROL REGISTER:

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

bit 7: **RBPU**
bit 6: **INTEDG**
bit 5: **T0CS**: TMR0 Clock Source Select bit
  1 = Transition on T0CKI pin
  0 = Internal instruction cycle clock (CLKOUT)
bit 4: **T0SE**: TMR0 Source Edge Select bit
  1 = Increment on high-to-low transition on T0CKI pin
  0 = Increment on low-to-high transition on T0CKI pin

bit 3: **PSA**: Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module
bit 2-0: **PS2 PS1 PS0**: Prescaler Rate Select bits

TIMER 0 BLOCK DIAGRAM:



TIMER 1 CONTROL REGISTER:

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON
bit7							bit0

bit 7-6: **Unimplemented:** Read as '0'

bit 5-4: **T1CKPS1:T1CKPS0**: Timer1 Input Clock Prescale Select bits

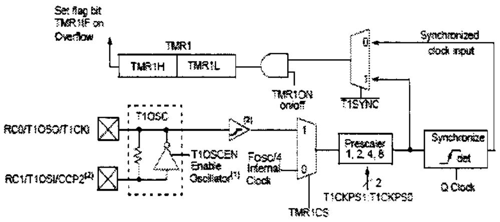
11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value
bit 3: **T1OSCEN**: Timer1 Oscillator Enable Control bit
1 = Oscillator is enabled
0 = Oscillator is shut off (The oscillator inverter is turned off to eliminate power drain)
bit 2: **T1SYNC**: Timer1 External Clock Input Synchronization Control bit
TMR1CS = 1
1 = Do not synchronize external clock input
0 = Synchronize external clock input
TMR1CS = 0
This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.

bit 1: **TMR1CS**: Timer1 Clock Source Select bit
1 = External clock from pin RC0/T1OSO/T1CKI (on the rising edge)

0 = Internal clock (FOSC/4)

bit 0: **TMR1ON**: Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1

TIMER 1 BLOCK DIAGRAM:

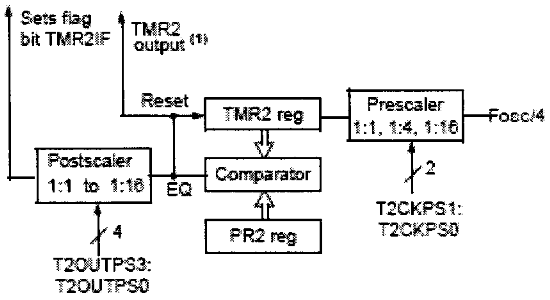


TIMER 2 CONTROL REGISTER:

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit7							bit0

bit 7: **Unimplemented:** Read as '0'
bit 6-3: **TOUTPS3:TOUTPS0**: Timer2 Output Postscale Select bits
0000 = 1:1 Postscale
0001 = 1:2 Postscale
0010 = 1:3 Postscale
1111 = 1:16 Postscale
bit 2: **TMR2ON**: Timer2 On bit
1 = Timer2 is on
0 = Timer2 is off
bit 1-0: **T2CKPS1:T2CKPS0**: Timer2 Clock Prescale Select bits
00 = Prescaler is 1
01 = Prescaler is 4
1x = Prescaler is 16

TIMER2 BLOCK DIAGRAM:



CCP1CON REGISTER/CCP2CON REGISTER:

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CCPxX	CCPxY	CCPxM3	CCPxM2	CCPxM1	CCPxM0
bit7							bit0

bit 7-6: **Unimplemented:** Read as '0'

bit 5-4: **CCPxX :CCPxY**: PWM Least Significant bits

Capture Mode: Unused

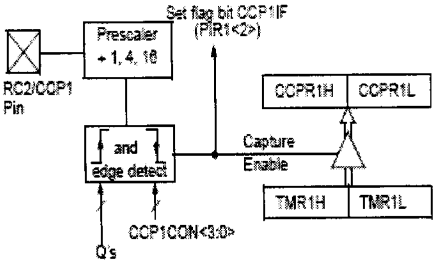
Compare Mode: Unused

PWM Mode: These bits are the two LSB s of the PWM duty cycle. The eight MSB s are found in CCPRxL.

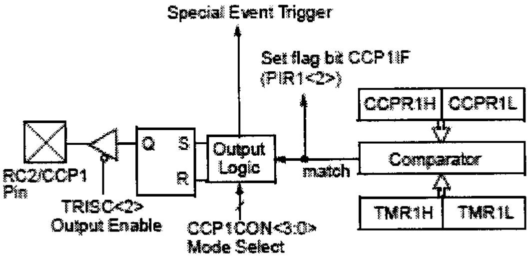
bit 3-0: **CCPxM3:CCPxM0**: CCPx Mode Select bits

0000 = Capture/Compare/PWM off (resets CCPx module)
0100 = Capture mode, every falling edge
0101 = Capture mode, every rising edge
0110 = Capture mode, every 4th rising edge
0111 = Capture mode, every 16th rising edge
1000 = Compare mode, set output on match (CCPxIF bit is set)
1001 = Compare mode, clear output on match (CCPxIF bit is set)
1010 = Compare mode, generate software interrupt on match (CCPxIF bit is set, CCPx pin is unaffected)
1011 = Compare mode, trigger special event (CCPxIF bit is set, CCPx pin is unaffected); CCP1 resets TMR1; CCP2 resets TMR1 and starts an A/D conversion (if A/D module is enabled)
11xx = PWM mode

CAPTURE MODE OPERATION BLOCK DIAGRAM:



COMPARE MODE OPERATION BLOCK DIAGRAM:



APPENDIX B

MCT2E OPTOISOLATOR

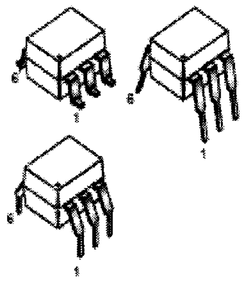
APPENDIX B
MCT2E OPTOISOLATOR

FAIRCHILD
SEMICONDUCTOR®

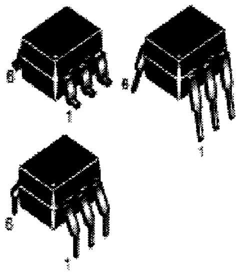
PHOTOTRANSISTOR OPTOCOUPLERS

MCT2	**MCT2E**	**MCT210**	**MCT271**
MCT2200	**MCT2201**	**MCT2202**	

WHITE PACKAGE (-M SUFFIX)



BLACK PACKAGE (NO -M SUFFIX)



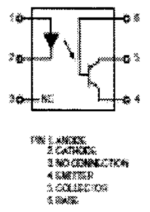
DESCRIPTION

The MCT2XXX series optoisolators consist of a gallium arsenide infrared emitting diode driving a silicon phototransistor in a 6-pin dual in-line package.

FEATURES

- UL recognized (File # E90700)
- VDE recognized (File # 94766)
  - -Add option V for white package (e.g., MCT2V-M)
  - -Add option 300 for black package (e.g., MCT2.300)
- MCT2 and MCT2E are also available in white package by specifying -M suffix, eg. MCT2-M

SCHEMATIC



APPLICATIONS

- Power supply regulators
- Digital logic inputs
- Microprocessor inputs

FAIRCHILD
SEMICONDUCTOR®

PHOTOTRANSISTOR OPTOCOUPLERS

MCT2 **MCT2200** **MCT2E** **MCT2201** **MCT210** **MCT2202** **MCT271**

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Device	Value	Units
TOTAL DEVICE Storage Temperature	T_{STG}	ALL	-55 to +150	°C
Operating Temperature	T_{OPR}	ALL	-55 to +100	°C
Lead Solder Temperature	T_{SOL}	ALL	260 for 10 sec	°C
Total Device Power Dissipation @ $T_A = 25°C$	P_D	-M	250	mW
		Non-M	260	
Derate above 25°C		-M	2.94	mW/°C
		Non-M	3.3	
EMITTER DC/Average Forward Input Current	I_F	-M	60	mA
		Non-M	100	
Reverse Input Voltage	V_R	ALL	3	V
Forward Current - Peak (300µs, 2% Duty Cycle)	$I_F(pk)$	ALL	3	A
LED Power Dissipation @ $T_A = 25°C$	P_D	-M	120	mW
		Non-M	150	
Derate above 25°C		-M	1.41	mW/°C
		Non-M	2.0	
DETECTOR Collector Current	I_C	ALL	50	mA
Collector-Emitter Voltage	V_{CEO}	ALL	30	V
Detector Power Dissipation @ $T_A = 25°C$	P_D	ALL	150	mW
Derate above 25°C		-M	1.76	mW/°C
		Non-M	2.0	

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PHOTOTRANSISTOR OPTOCOUPLERS

MCT2 **MCT2200** **MCT2E** **MCT2201** **MCT210** **MCT2202** **MCT271**

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ Unless otherwise specified.)

INDIVIDUAL COMPONENT CHARACTERISTICS

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
EMITTER							
Input Forward Voltage	($I_F = 20$ mA)	V_F	MCT2/-M MCT2E/-M MCT271 MCT2200 MCT2201 MCT2202		1.25	1.50	V
	($T_A = 0$-70°C, $I_F = 40$ mA)		MCT210		1.33		
Reverse Leakage Current	($V_R = 3.0$ V)	I_R	MCT2/-M MCT2E/-M MCT271 MCT2200 MCT2201 MCT2202		0.001	10	µA
	($T_A = 0$-70°C, $V_R = 6.0$ V)		MCT210				
DETECTOR Collector-Emitter Breakdown Voltage	($I_C = 1.0$ mA, $I_F = 0$)	BV_{CEO}	ALL	30	100		V
	($T_A = 0$-70°C)		MCT210				
Collector-Base Breakdown Voltage	($I_C = 10$ µA, $I_F = 0$)	BV_{CBO}	MCT2/-M MCT2E/-M MCT271 MCT2200 MCT2201 MCT2202	70	120		V
	($T_A = 0$-70°C)		MCT210	30			
Emitter-Collector Breakdown Voltage	($I_E = 100$ µA, $I_F = 0$)	BV_{ECO}	MCT2/-M MCT2E/-M MCT271 MCT2200 MCT2201 MCT2202	7	10		V
	($T_A = 0$-70°C)		MCT210	6	10		
Collector-Emitter Dark Current	($V_{CE} = 10$ V, $I_F = 0$)	I_{CEO}	ALL		1	50	nA
	($V_{CE} = 5$ V, $T_A = 0$-70°C)					30	µA
Collector-Base Dark Current	($V_{CB} = 10$ V, $I_F = 0$)	I_{CBO}	ALL			20	nA
Capacitance	($V_{CE} = 0$ V, f = 1 MHz)	C_{CE}	ALL		8		pF

** Typical values at $T_A = 25°C$

PHOTOTRANSISTOR OPTOCOUPLERS

MCT2 MCT2200 MCT2E MCT2201 MCT210 MCT2202 MCT271

TRANSFER CHARACTERISTICS (T_A = 25°C Unless otherwise specified.)

DC Characteristic	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
Output Collector Current	(T_A = 0-70°C) (I_F = 10 mA, V_{CE} = 5 V)	CTR	MCT210	150			%
			MCT2200	20			
			MCT2201	100			
			MCT2202	63		125	
	(I_F = 10 mA, V_{CE} = 10 V)		MCT2 MCT2-M MCT2E MCT2E-M	20			
			MCT271	45		90	
	(I_F = 3.2 mA to 32 mA, V_{CE} = 0.4 V) (T_A = 0-70°C)		MCT210	50			
Collector-Emitter Saturation Voltage	(I_C = 2 mA, I_F = 16 mA)	$V_{CE (SAT)}$	MCT2 MCT2-M MCT2E MCT2E-M MCT271			0.4	V
	(I_C = 16 mA, I_F = 32 mA, T_A = 0-70°C)		MCT210				
	(I_C = 2.5 mA, I_F = 10 mA)		MCT2200 MCT2201 MCT2202				
AC Characteristic Saturated Turn-on Time from 5 V to 0.8 V	(I_F = 15 mA, V_{CC} = 5 V, R_L = 2 kΩ) (R_B = Open) (Fig. 20)	t_{on}	MCT2		1.1		µs
			MCT2E		1.1		
	(I_F = 20 mA, V_{CC} = 5 V, R_L = 2 kΩ) (R_B = 100 kΩ) (Fig. 20)		MCT2		1.3		
			MCT2E		1.3		
Saturated Turn-off Time from SAT to 2.0 V	(I_F = 15 mA, V_{CC} = 5 V, R_L = 2 kΩ) (R_B = Open) (Fig. 20)	t_{off}	MCT2		50		
			MCT2E		50		
	(I_F = 20 mA, V_{CC} = 5 V, R_L = 2 kΩ) (R_B = 100 kΩ) (Fig. 20)		MCT2		20		
			MCT2E		20		
Turn-on Time	(I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)	t_{on}	MCT2-M MCT2E-M		2		
Turn-off Time	(I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)	t_{off}	MCT2-M MCT2E-M		2		
Rise Time	(I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)	t_r	MCT2-M MCT2E-M		2		
Fall Time	(I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)	t_f	MCT2-M MCT2E-M		1.5		

** Typical values at T_A = 25°C

TRANSFER CHARACTERISTICS (Cont.)

AC Characteristic	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
Saturated turn-on time	(I_F = 16 mA, R_L = 1.9kΩ, V_{CC} = 5 V) (Fig. 20)	t_{on}	MCT271		1.0		µs
Saturated turn-off time (Approximates a typical TTL interface)		t_{off}			48		
Saturated turn-on time	(I_F = 16 mA, R_L = 4.7kΩ, V_{CC} = 5 V) (Fig. 20)	t_{on}			1.0		
Saturated turn-off time (Approximates a typical low power TTL interface)		t_{off}			98		
Saturated rise time	(I_F = 16 mA, R_L = 560Ω, V_{CC} = 5 V) (Fig. 20, 21)	t_r	MCT210		1.0		
Saturated fall time		t_f			11		
Saturated propagation delay - high to low	(I_F = 16 mA, R_L = 2.7kΩ) (Fig. 20, 21)	$T_{PD\,(HL)}$			1.0		
Saturated propagation delay - low to high		$T_{PD\,(LH)}$			50		
Non-saturated turn on time	(I_C = 2 mA, V_{CC} = 10 V, R_L = 100Ω (Fig. 20)	T_{ON}	MCT2200 MCT2201 MCT2202		2	10	
Non-saturated turn off time		T_{OFF}			2	10	
Non-saturated rise time	(I_C = 2 mA, V_{CC} = 5 V, R_L = 100Ω) (Fig. 20)	t_r	MCT210		2		
Non-saturated fall time		t_f			2		
Non-saturated turn-on time	(I_C = 2 mA, V_{CC} = 5 V, R_L = 100Ω) (Fig. 20)	t_{on}	MCT271		2	7	
Non-saturated turn-off time		t_{off}			2	7	

** Typical values at T_A = 25°C

APPENDIX C

2N2222 TRANSISTOR

APPENDIX C

2N2222 TRANSISTORS

Philips Semiconductors **Product specification**

NPN switching transistors 2N2222; 2N2222A

FEATURES

- High current (max. 800 mA)
- Low voltage (max. 40 V).

APPLICATIONS

- Linear amplification and switching.

DESCRIPTION

NPN switching transistor in a TO-18 metal package.
PNP complement: 2N2907A.

PINNING

PIN	DESCRIPTION
1	emitter
2	base
3	collector, connected to case

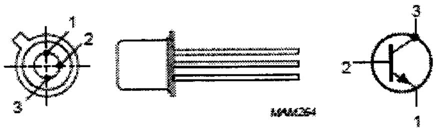


Fig.1 Simplified outline (TO-18) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	2N2222		–	60	V
	2N2222A		–	75	V
V_{CEO}	collector-emitter voltage	open base			
	2N2222		–	30	V
	2N2222A		–	40	V
I_C	collector current (DC)		–	800	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	500	mW
h_{FE}	DC current gain	$I_C = 10$ mA; $V_{CE} = 10$ V	75	–	
f_T	transition frequency	$I_C = 20$ mA; $V_{CE} = 20$ V; f = 100 MHz			
	2N2222		250	–	MHz
	2N2222A		300	–	MHz
t_{off}	turn-off time	$I_{Con} = 150$ mA; $I_{Bon} = 15$ mA; $I_{Boff} = -15$ mA	–	250	ns

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	2N2222		–	60	V
	2N2222A		–	75	V
V_{CEO}	collector-emitter voltage	open base			
	2N2222		–	30	V
	2N2222A		–	40	V
V_{EBO}	emitter-base voltage	open collector			
	2N2222		–	5	V
	2N2222A		–	6	V
I_C	collector current (DC)		–	800	mA
I_{CM}	peak collector current		–	800	mA
I_{BM}	peak base current		–	200	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	500	mW
		$T_{case} \leq 25$ °C	–	1.2	W
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		–	200	°C
T_{amb}	operating ambient temperature		−65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	in free air	350	K/W
$R_{th\ j\text{-}c}$	thermal resistance from junction to case		146	K/W

CHARACTERISTICS

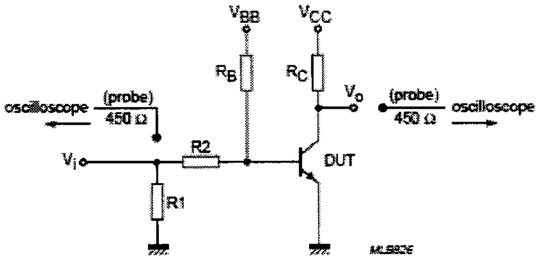
$T_j = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{CBO}	collector cut-off current				
	2N2222	$I_E = 0$; $V_{CB} = 50$ V	–	10	nA
		$I_E = 0$; $V_{CB} = 50$ V; $T_{amb} = 150$ °C	–	10	µA
I_{CBO}	collector cut-off current				
	2N2222A	$I_E = 0$; $V_{CB} = 60$ V	–	10	nA
		$I_E = 0$; $V_{CB} = 60$ V; $T_{amb} = 150$ °C	–	10	µA
I_{EBO}	emitter cut-off current	$I_C = 0$; $V_{EB} = 3$ V	–	10	nA
h_{FE}	DC current gain	$I_C = 0.1$ mA; $V_{CE} = 10$ V	35	–	
		$I_C = 1$ mA; $V_{CE} = 10$ V	50	–	
		$I_C = 10$ mA; $V_{CE} = 10$ V	75	–	
		$I_C = 150$ mA; $V_{CE} = 1$ V; note 1	50	–	
		$I_C = 150$ mA; $V_{CE} = 10$ V; note 1	100	300	
h_{FE}	DC current gain	$I_C = 10$ mA; $V_{CE} = 10$ V; $T_{amb} = -55$ °C			
	2N2222A		35	–	
h_{FE}	DC current gain	$I_C = 500$ mA; $V_{CE} = 10$ V; note 1			
	2N2222		30	–	
	2N2222A		40	–	
V_{CEsat}	collector-emitter saturation voltage				
	2N2222	$I_C = 150$ mA; $I_B = 15$ mA; note 1	–	400	mV
		$I_C = 500$ mA; $I_B = 50$ mA; note 1	–	1.6	V
V_{CEsat}	collector-emitter saturation voltage				
	2N2222A	$I_C = 150$ mA; $I_B = 15$ mA; note 1	–	300	mV
		$I_C = 500$ mA; $I_B = 50$ mA; note 1	–	1	V
V_{BEsat}	base-emitter saturation voltage				
	2N2222	$I_C = 150$ mA; $I_B = 15$ mA; note 1	–	1.3	V
		$I_C = 500$ mA; $I_B = 50$ mA; note 1	–	2.6	V
V_{BEsat}	base-emitter saturation voltage				
	2N2222A	$I_C = 150$ mA; $I_B = 15$ mA; note 1	0.6	1.2	V
		$I_C = 500$ mA; $I_B = 50$ mA; note 1	–	2	V
C_c	collector capacitance	$I_E = i_e = 0$; $V_{CB} = 10$ V; f = 1 MHz	–	8	pF
C_e	emitter capacitance	$I_C = i_c = 0$; $V_{EB} = 500$ mV; f = 1 MHz			
	2N2222A		–	25	pF
f_T	transition frequency	$I_C = 20$ mA; $V_{CE} = 20$ V; f = 100 MHz			
	2N2222		250	–	MHz
	2N2222A		300	–	MHz
F	noise figure	$I_C = 200$ µA; $V_{CE} = 5$ V; $R_S = 2$ kΩ; f = 1 kHz; B = 200 Hz			
	2N2222A		–	4	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Switching times (between 10% and 90% levels); see Fig.2					
t_{on}	turn-on time	I_{Con} = 150 mA; I_{Bon} = 15 mA; I_{Boff} = −15 mA	–	35	ns
t_d	delay time		–	10	ns
t_r	rise time		–	25	ns
t_{off}	turn-off time		–	250	ns
t_s	storage time		–	200	ns
t_f	fall time		–	60	ns

Note

1. Pulse test: $t_p \leq 300$ µs; $\delta \leq 0.02$.



V_i = 9.5 V; T = 500 µs; t_p = 10 µs; $t_r = t_f \leq 3$ ns.
R1 = 68 Ω; R2 = 325 Ω; R_B = 325 Ω; R_C = 160 Ω.
V_{BB} = −3.5 V; V_{CC} = 29.5 V.
Oscilloscope input impedance Z_i = 50 Ω.

Fig.2 Test circuit for switching times.