A New Method for DC-AC conversion using simplified Multilevel Inverter - Design and analysis using PSIM

BY

V.GOWRI SHANKAR

Reg.NO:072015005

of

KUMARAGURU COLLEGE OF TECHNOLOGY

(AUTONOMOUS)

COIMBATORE – 641 006

A PROJECT REPORT

Submitted to the

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

In partial fulfillment of the requirements
for the award of the degree
Of

Master of Engineering
IN
Power Electronics and Drives

MAY - 2009

BONAFIDE CERTIFICATE

Certified that this project report entitled "A New Method for DC–AC Conversion using Simplified Multilevel Inverter –design and analysis using PSIM" is the bonafide work of

V.GOWRI SHANKAR - Register No: 072015005

Who carried out the project work under my supervision.

Signature of the Head of the Department
Prof.K.Regupathy Subramanian

Signature of the supervisor
Mr.C.Udhaya Shankar

Certified that the candidate with university Register No...072015005.....
Was examined in project viva voice examination held on...06.05.09...

Internal Examiner

06.05.09

External Examiner

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

KUMARAGURU COLLEGE OF TECHNOLOGY

COIMBATORE 641 006

(An Autonomous Institution Affiliated to Anna University, Coimbatore)

Karunya UNIVERSITY

DECLARED AS A DEEMED TO BE UNIVERSITY UNDER SEC. 3 OF THE UGC ACT,1956

NATIONAL CONFERENCE ON

"TRENDS IN ELECTRONICS, INSTRUMENTATION, EMBEDDED SYSTEM AND AUTOMATION"

28th FEBRUARY 2009

This is to certify that Dr/Mr/Mrs/Ms V. Gowri Shankar, C. Udhayashankar has participated as invited ~~Speaker~~ / Delegate in the national conference organized by the Department Of Electronics And Instrumentation, Karunya University, Coimbatore, Tamilnadu. He / She has also presented a paper entitled "A New Method For DC-AC Conversion Using Simplified Multilevel Inverter - Design and Analysis Using PSIM"

Prof.K.Rajasekaran
Convenor

Dr. Anne Mary Fernandez
Registrar

ACKNOWLEDGEMENT

The satisfaction and euphoria that accompanies the successful completion of any task would be incomplete without acknowledging the people who were responsible for the completion of the project.

I offer my sincere, hearty thanks to my guide **Mr.C.Udhaya Shankar., M.Tech.** Senior Lecturer, EEE for help, guidance and timely suggestion for successful preparation of this project report.

I sincerely thank all the teaching and non-teaching staffs of EEE Department for giving creative ideas, which helped me to finish the project successfully at the right time.

I thank my Parents for their constant guidance and care showered upon me to complete the project work in a successful manner. Finally, it give me a great pleasure to express my sincerely thanks to all my friends who have helped me during the course of this work.

ABSTRACT

Multilevel converters offer high power capability, associated with lower outputs harmonics and lower commutation losses. Their main disadvantage is their complexity, requiring a great number of power devices and passive components, and a rather complex control circuitry. The main objective of this project is to reduce the number of power devices and capacitors required to implement a multilevel converter and to reduce the harmonics at the output voltage using pulse accelerator method.

This work reports a new multilevel inverter topology using an H-bridge output stage with a bidirectional auxiliary switch. The new topology produces a significant reduction in the number of power devices and capacitors required to implement a multilevel output. The new topology is used in the design of a five-level inverter; only 5 controlled switches, 8 diodes, and 2 capacitors are required to implement the five-level inverter using the proposed topology. The new topology achieves a 37.5% reduction in the number of main power switches. The power circuit is simulated in PSIM. The analysis of output waveforms and its harmonics spectrum is carried out.

Many different PWM-strategies for multi-level inverters exist. This project proposes various multi level circuits with gate blocking switch strategies for Inverters. Operating principles with switching functions are analyzed for Single Phase Five level inverter. The controller is also designed to keep the output voltage sinusoidal and to have high dynamic performances. The proposed inverter is implemented on a prototype. The single-phase five-level inverter is presented to alleviate harmonic components of output voltage and the load current. The validity of the proposed inverter is verified through simulation and experiments. To assess the proposed inverter, it is compared with the conventional single-phase three-level PWM inverter under the conditions of identical supply dc voltage and switching frequency.

TABLES OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

Power-electronic inverters are becoming popular for various industrial drives applications. In recent years also high-power and medium-voltage drive applications have been installed. To overcome the limited semiconductor voltage and current ratings, some kind of series and/or parallel connection will be necessary. Due to their ability to synthesize waveforms with a better harmonic spectrum and attain higher voltages, multi-level inverters are receiving increasing attention in the past few years. The multilevel inverter was introduced as a solution to increase the converter operating voltage above the voltage limits of classical semiconductors. The multilevel voltage source inverter is recently applied in many industrial applications such as ac power supplies, static VAR compensators, drive systems, etc. One of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output. The output voltage waveform of a multilevel inverter is composed of the number of levels of voltages, typically obtained from capacitor voltage sources. The so-called multilevel starts from three levels.

As the number of levels reach infinity, the output THD (Total Harmonic Distortion) approaches zero. The number of the achievable voltage levels, however, is limited by voltage unbalance problems, voltage clamping requirement, circuit layout, and packaging constraints. Multilevel inverters synthesizing a large number of levels have a lot of merits such as improved output waveform, a smaller filter size, a lower EMI (Electro Magnetic Interference), and other advantages. The principle advantage of using multilevel inverters is the low harmonic distortion obtained due to the multiple voltage levels at the output and reduced stresses on the switching devices used.Improvements in fast switching power devices have led to an increased interest in voltage source inverters (VSI) with pulse width modulation control (PWM).It is generally accepted that the performance of an inverter, with any switching strategies, can be related to the harmonic contents of its output voltage. Power electronics researchers have always studied many novel control techniques to reduce harmonics in such waveforms.

Up-to-date, there are many techniques, which are applied to multilevel inverter topologies. Pulse Width Modulation (PWM) is widely employed to control the output of static power inverters. The reason for using PWM is that they provide voltage and/or current wave shaping customized to the specific needs of the application under consideration. It is lastly performance and cost criteria which determines the choice of a PWM method in a specific application. PWM inverters can control their output voltage and frequency simultaneously. And also they can reduce the harmonic components in load currents.

These features have made them power candidate in many industrial applications such as variable speed drives, uninterruptible power supplies, and other power conversion systems. However, the reduction of harmonic components in output currents is still the focus of major interest to alleviate the influences of electromagnetic interferences or noise and vibrations.

In general, neutral point clamped PWM three-phase inverter which uses four switching elements in each arm has the five- level voltage waveforms that results in considerable suppression of the harmonic currents comparing with the conventional full-bridge type three-level PWM inverters. However, this is not the case of single-phase PWM inverter. In these days, the popular single-phase inverters adopt the full-bridge type using approximate sinusoidal modulation technique as the power circuits. The output voltage of them has three values: zero, positive and negative supply dc voltage levels. Therefore, the harmonic components of their output voltage are determined by the carrier frequency and switching functions. Moreover, the harmonic reduction of them is limited to a certain degree.

Under these technical backgrounds, a single-phase five-level PWM (Pulse Width Modulation) and gate blocking switch technique is presented in the project. The main objective of the project is to design a single-phase five-level inverter to reduce the harmonic components of the output voltage and the load current. The proposed inverter can reduce the harmonic components compared with that of traditional full-bridge three-level PWM inverter. Simulation is an effective tool by which we can experience the practical results through the software. There are a number of simulation software available and the most efficient tool is the PSIM. Hence, the simulink part of the PSIM is employed.

1.1 ORGANIZATION OF THE PROJECT

1.1.1 Project Overview

The proposed single-phase five-level inverter whose output voltage has five values: zero, half and full supply dc voltage levels (positive and negative, respectively), so called a five level single-phase inverter. The inverter can reduce the harmonic components compared with that of traditional full-bridge three-level PWM inverter under the condition of identical supply dc voltage and switching frequency. Operational principles and switching functions are analyzed. The proposed inverter improves the dynamic performances. To assess the proposed inverter, it is compared with the conventional single-phase three-level PWM inverter under the conditions of identical supply dc voltage and switching frequency. Simulation and experimental results are presented to verify the validities of the proposed inverter.

1.1.2 Report Layout

The layout gives the complete organization of the report. Chapter 2 describes the general circuit topology of multilevel inverter. Chapter 3 deals with the modulation topologies of multilevel inverters. Chapter 4 deals with the operating principle of proposed inverter. Chapter 5 gives the simulation of the proposed inverter. Chapter 6 describes the hardware implementation of the project. Chapter 7 gives the conclusion and recommendations for future work.

CHAPTER 2
GENERAL CIRCUIT TOPOLOGY OF MULTILEVEL INVERTER

2.1 INTRODUCTION

In general, increasing the switching frequency in voltage source inverters (VSI) leads to the better output voltage / current waveforms. Harmonic reduction in controlling a VSI with variable amplitude and frequency of the output voltage is of importance and thus the conventional inverters which are referred to as two-level inverters have required increased switching frequency along with various PWM switching strategies. In the case of high power / high voltage applications, however, the two-level inverters have some limitations to operate at high frequency mainly due to switching losses and constriction of device rating itself. Moreover, the semiconductor switching devices should be used in such a manner as problematic series / parallel combinations to obtain capability of handling high power. Nowadays the use of multilevel approach is believed to be promising alternative in such a very high power conversion processing system. Advantages of this multilevel approach include good power quality, good electromagnetic compatibility (EMC), low switching losses, and high voltage capability.

2.2 MULTILEVEL CONCEPT

Recent advances in power electronics have made the multilevel concept practical. In fact, the concept is so advantageous that several major drives manufacturers have obtained recent patents on multilevel power converters and associated switching techniques. It is evident that the multilevel concept will be a prominent choice for power electronic systems in future years, especially for medium-voltage operation.Multi-level inverters are the modification of basic bridge inverters. They are normally connected in series to form stacks of level. The topological structure of multilevel inverter must cope with the following points.

1) It should have less switching devices as far as possible.
2) It should be capable of enduring very high input voltage such as HVDC transmission for high power applications.
3) Each switching device should have lower switching frequency owing to multilevel approach.

There are various multilevel concepts used for various applications. Various multilevel circuits are used to generate multiple voltage levels. Some of the multilevel concepts with various voltage levels are given below.

2.2.1 Representation of Single- Level Voltage

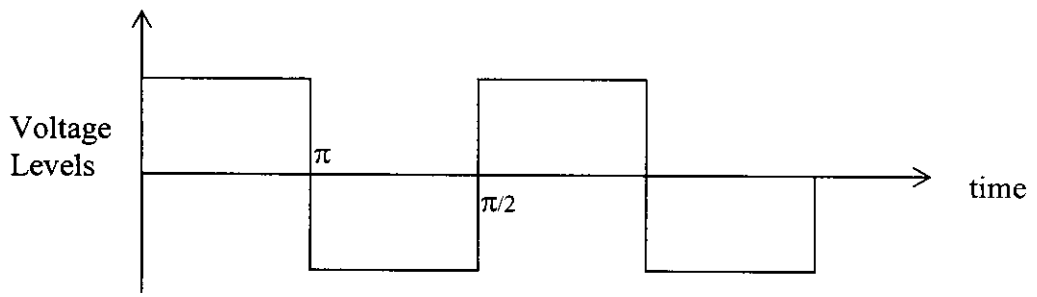


Fig 2.1 single- level voltage waveform

The figure given above represents the single- level voltage. It represents only a single level voltage waveform.

2.2.2 Representation of Two- Level Voltage

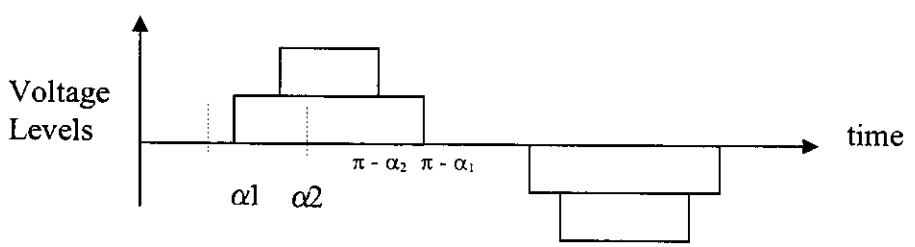


Fig 2.2 Two- level voltage waveform

The figure given above represents the two- level voltage. It represents two- level voltage waveform.

2.2.3 Quarter-Wave Symmetric Multilevel Waveform

The optimized harmonic stepped waveform is assumed to be the quarter-wave

Symmetric. The first half cycle of the quarter-wave symmetric waveform is depicted in Fig. 2.3

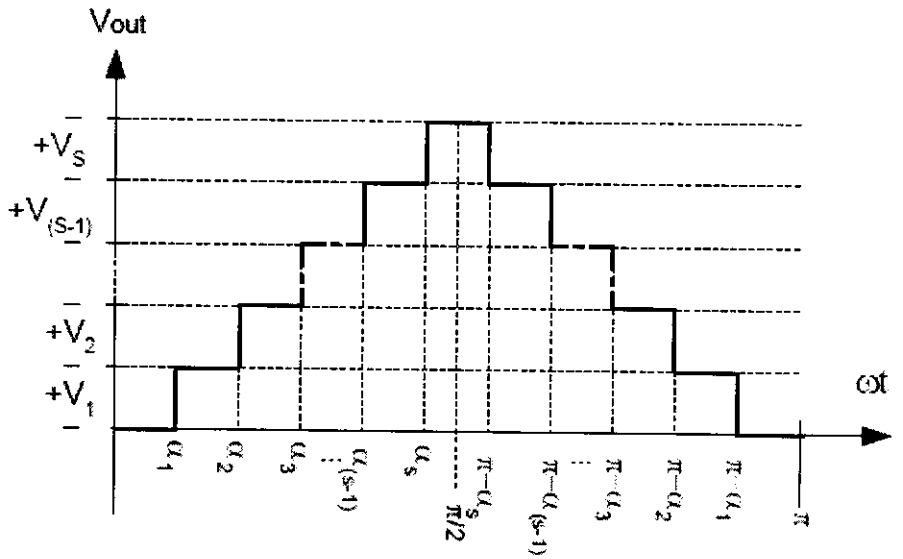


Fig 2.3 First half cycle of the quarter-wave symmetric waveform

The output voltage level is zero from $\omega t = 0$ to $\omega t = \alpha 1$. At $\omega t = \alpha 1$, the output voltage level is changed from zero to +V1, and from +V1 to +(V1+V2) at $\omega t = \alpha 2$. The process will be repeated until $\omega t = \pi/2$, and the output voltage level becomes +V1 +V2+...+V(S-1) +VS. Then, in the second quarter, the level of output voltage will be decreased to +V1 +V2+...+V(S-1) at $\omega t = \pi - \alpha S$. The process will be repeated until $\omega t = \pi - \alpha 1$ and output voltage becomes zero again. In the second half of the waveform, the process will be repeated all of previous steps except the amplitude of the dc sources change from positive to negative. The next period will then repeat the same cycle.

2.3 ADVANTAGES OF MULTILEVEL VOLTAGES

In general, multilevel power converters can be viewed as voltage synthesizers, in which the high output voltage is synthesized from many discrete smaller voltage levels. The main advantages of this approach are summarized as follows:

- The voltage capacity of the existing devices can be increased many times without the complications of static and dynamic voltage sharing that occur in series-connected devices.
- Spectral performance of multilevel waveforms is superior to that of their two-level counterparts.

- Multilevel waveforms naturally limit the problems of large voltage transients that occur due to the reflections on cables, which can damage the motor windings and cause other problems.

2.4 TYPES OF MULTILEVEL CIRCUITS

Multilevel power conversion technology is a very rapidly growing area of power electronics with good potential for further development. The most attractive applications of this technology are in the medium- to high-voltage range (2-13 kV), and include motor drives, power distribution, power quality and power conditioning applications. There are different types of multi level circuits involved.

The first topology introduced was the series H-bridge design. This was followed by the diode clamped converter, which utilized a bank of series capacitors. A later invention detailed the flying capacitor design in which the capacitors were floating rather than series-connected. Another multilevel design involves parallel connection of inverter phases through inter-phase reactors. In this design, the semiconductors block the entire dc voltage, but share the load current. Several combinational designs have also emerged some involving cascading the fundamental topologies. These designs can create higher power quality for a given number of semiconductor devices than the fundamental topologies alone due to a multiplying effect of the number of levels.

The most actively developed of multilevel topologies are listed in figure 2.4.

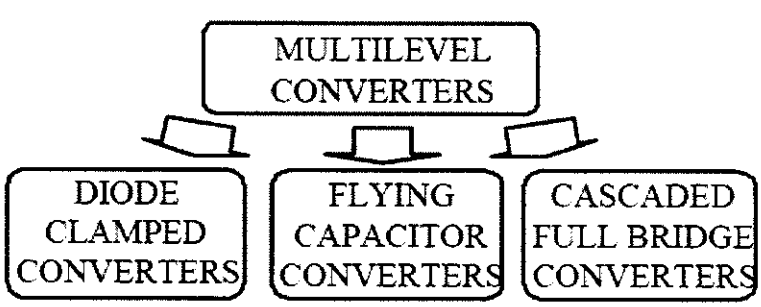


Fig 2.4 Multilevel converter topologies.

2.4.1 Diode-Clamped Multilevel Topology

The first practical multilevel topology is the neutral-point-clamped (NPC) PWM topology. The three-level version of this topology, shown in Figure 2.5(b), has several distinct advantages over the two-level topology.

The advantages are:

- ❖ Voltages across the switches are only half of the dc-link voltage.
- ❖ The first group of voltage harmonics is centered on twice the switching frequency.

This topology can be generalized, and the principles used in the basic three-level topology can be extended for use in topologies with any number of levels. However, practical experience with this topology revealed several technical difficulties that complicate its application for-high power converters.

These are as follows:

- ❖ This topology requires high speed clamping diodes that must be able to carry full load current and are subject to severe reverse recovery stress. Although measures to alleviate this problem can be applied, this remains a serious consideration.
- ❖ For topologies with more than three levels the clamping diodes are subject to increased voltage stress equal to Vpn.(n-1)/n. Therefore, series connection of diodes might be required.

This complicates the design and raises reliability and cost concerns. The issue of maintaining the charge balance of the capacitors is still an open issue for NPC topologies with more than three-levels. Although the three-level NPC topology works well with high power factor loads, NPC topologies with more than three levels are mostly used for static var compensation circuits.

2.4.2 Flying capacitor Multilevel Topology

The flying capacitor multilevel topology is considered to be the most serious alternative to the diode-clamped topology. Figure 2.6 gives the Three- and Four-level flying capacitor phase leg. The significant advantage of this topology is that

1) It eliminates the clamping diode problems present in the diode-clamped multilevel topologies.

2) Additionally, this topology naturally limits the dV/dt stress across the devices and introduces additional switching states that can be used to help maintain the charge balance in the capacitors.

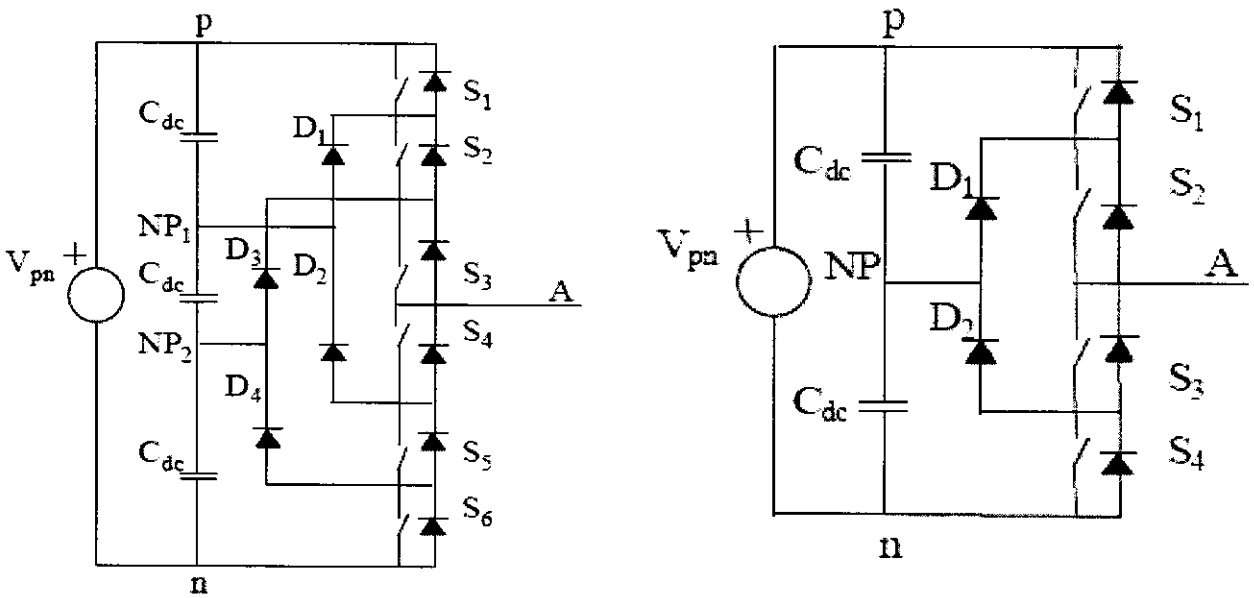


Fig 2.5 (a) (b) Two-level and Three-level version of Diode clamped topology.

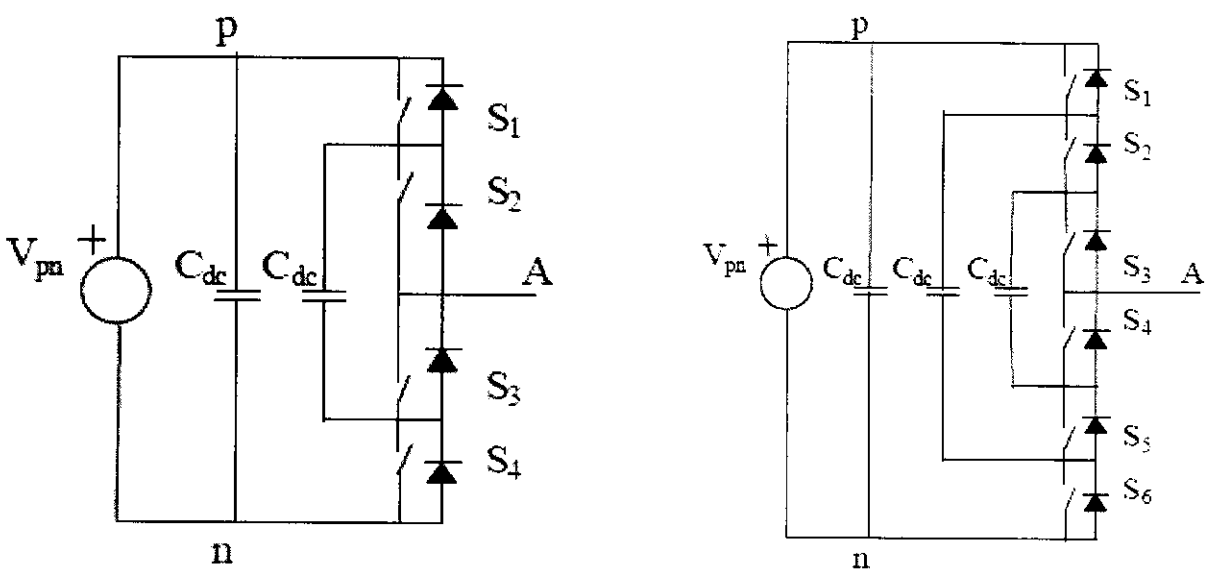


Figure 2.6 (a) Single Phase Three -level flying capacitor inverter

(b) Single Phase Four -level flying capacitor inverter

Unlike the diode-clamped converter, the flying capacitor topology has enough switching states to control the charge balance in the single isolated leg with converters having any number of levels, even if the phase current is unidirectional. This makes this topology attractive even for the dc/dc converters. They are:

- ❖ The dc-link capacitor charge controller adds complexity to the control of the whole circuit.
- ❖ The flying capacitor topology might require more capacitance than the equivalent diode clamped topology.

In addition, it is obvious that rather large rms currents will flow through these capacitors. There is a potential for parasitic resonance between decoupling capacitors.

2.4.3 Multilevel Configurations with Cascaded Two-Level Full-Bridge Inverters

The modularity of this structure allows easier maintenance and provides a very convenient way to add redundancy into the system. The multilevel inverter using cascaded-inverter with separate DC sources synthesizes a desired voltage from several independent sources of dc voltages, which may be obtained from batteries, fuel cells, or solar cells. This configuration recently becomes very popular in ac power supply and adjustable speed drive applications. This new inverter can avoid extra clamping diodes or voltage balancing capacitors. A single-phase m-level configuration of such an inverter is shown in Fig 2.7(a)

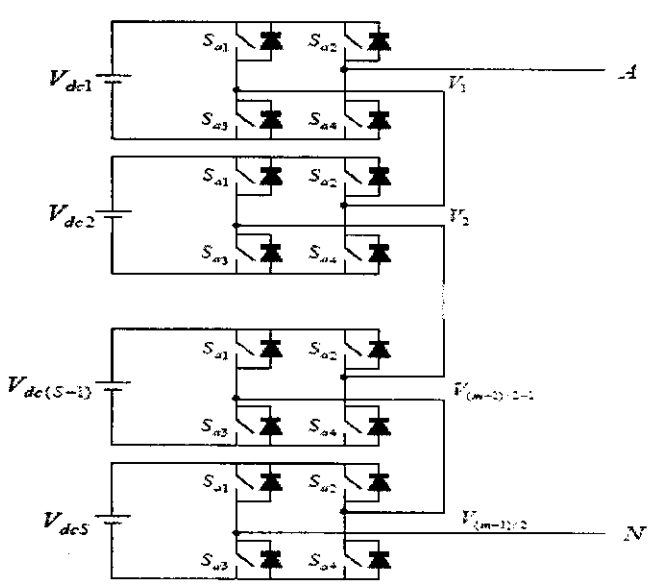


Figure 2.7(a) Single Phase cascaded bridge inverter

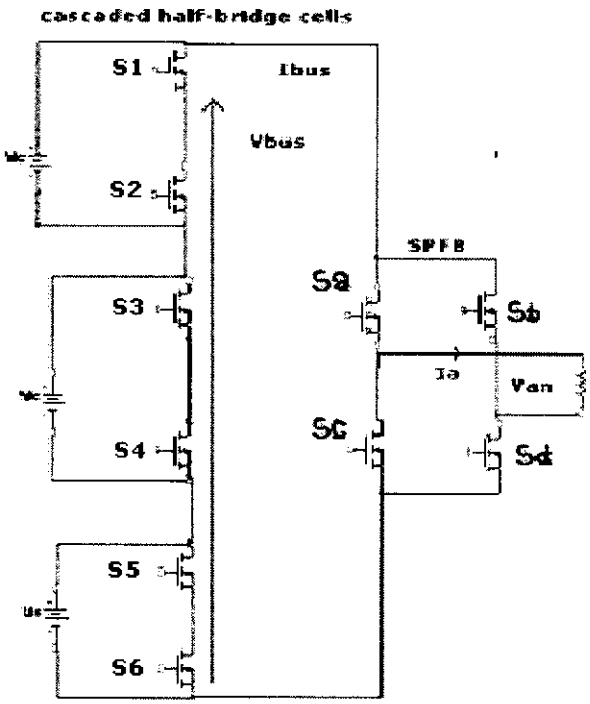


Figure 2.7(b) Single Phase cascaded half-bridge inverter.

One major advantage of this hybrid approach is that the number of output can be further increased without addition of any new components, requiring only the dc sources with different voltage levels.

2.5 PROPOSED INVERTER CIRCUIT

The proposed inverter circuit is the single-phase five-level inverter. The schematic circuit of the proposed inverter is given below.

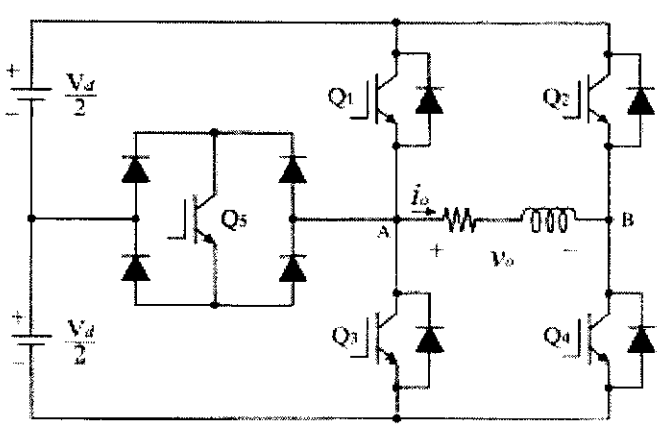


Fig 2.8 Single-phase five level inverter

Hence, the circuit topology shown in Fig.2.8 might be preferred not only under the aspect of harmonic content reduction due to several level of the output voltage as an essential feature of multilevel scheme, but also under the aspect of full utilization of semiconductor device in case that high voltage of dc-link could be applied

The five level inverter has very simple commutation sequence which could make it possible to freely change output phase voltages between arbitrary two voltage levels, requiring no additional commutation circuitry. Commutation procedure between some levels should be divided into each one level commutation of unit change of voltage in order to guarantee voltage stress of both main switches and main diodes within unit level voltage En during transient time. One-level commutation can be carried out by first turning off the most upper (lower) main switch in one-state and turning on the opposite lower (upper) main switch in off-state after a required dead time. It should be noted that such commutation sequence facilitates utilization of switching devices even with different turn off times.

2.6 COMPARISON AMONG THREE MULTILEVEL INVERTERS IN APPLICATION ASPECTS

In high power system, the multilevel inverters can appropriately replace the exist system that use traditional multi-pulse converters without the need for transformers. All three multilevel inverters can be used in reactive power compensation without having the voltage unbalance problem. Table 2.1 compares the power component requirements per phase leg among the three multilevel voltage source inverter mentioned below. It shows that the number of main switches and main diodes, needed by the inverters to achieve the same number of voltage levels. Clamping diodes were not needed in flying-capacitor and cascaded-inverter configuration, while balancing capacitors were not needed in diode clamp and cascaded-inverter configuration. Implicitly, the multilevel converter using cascaded-inverters requires the least number of components.

TABLE 2.1

COMPARISON BETWEEN POWER COMPONENTS REQIUREMENT OF DIFFERNET LEVEL OF INVERTERS

Multilevel inverter type	Diode clamped	Capacitor Clamped	H-bridge topology
Main controlled switches	8	8	4
Auxiliary controlled switches	0	0	1
Diodes	20	8	8
Capacitors	4	10	2

In very high power application especially with very high input voltage, traditional two-level VSI could not avoid to sue the series connected semiconductor switches so as to cope with limitations of device rating utilized and it may be very cumbersome and even problematic mainly due to difficulty of device matching deteriorating utilization factor of switching devices. The multilevel topology, however, suggests a good solution for such a problem.

2.7 UTILIZATION OF SEMICONDUCTOR DEVICE

Multilevel inverters, in general, employ relatively many semiconductor devices due to their distinct structure so that it would be seen at glance to be less attractive. However, it is reasonable that the real evaluation of such an inverter should be primarily in the context of device utilization. In some inverter structures such as direct realization with bi-directional switches, the device utilization may be poor resulting in high voltage and or current stress at the device. But our multilevel inverters make it possible to utilize their semiconductor devices fully allowing low devices ratings.

CHAPTER 3

MODULATION TOPOLOGIES OF MULTI LEVEL INVERTERS

3.1 INTRODUCTION

The multilevel topology involves several modulation techniques. Each technique involves different modulation methods. The well-known modulation topologies for multi level inverters as follows:

1) Sinusoidal or "Sub harmonic" Natural Pulse Width Modulation (SPWM).
2) Selective Harmonic Eliminated Pulse Width Modulation (SHE PWM) or Programmed-Waveform Pulse Width Modulation (PWPWM).
3) Optimized Harmonic Stepped-Waveform Technique (OHSW).

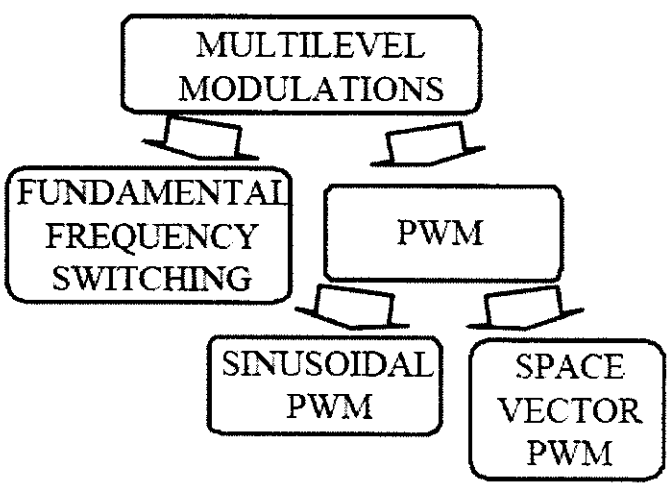


Figure 3.1. Multilevel modulation techniques.

3.2 PULSE WIDTH MODULATION TECHNIQUE

The advent of the transformer less multilevel inverter topology has brought forth various pulse width modulation (PWM) schemes as a means to control the switching of the active devices in each of the multiple voltage levels in the inverter. The most efficient method of controlling the output voltage is to incorporate pulse width modulation control (PWM control) within the inverters. In this method, a fixed D.C. input voltage is supplied to the inverter and a controlled A.C. output voltage is obtained by adjusting the on and–off periods of the inverter devices. Voltage-type PWM inverters have been applied widely to such fields as power supplies and motor drivers. This is because: (1) such inverters are well adapted to high-speed self turn-off switching devices that, as solid-state power converters, are provided

with recently developed advanced circuits; and (2) they are operated stably and can be controlled well.

The PWM control has the following advantages:

(i) The output voltage control can be obtained without any additional components.

(ii) With this type of control, lower order harmonics can be eliminated or minimized along with its output voltage control. The filtering requirements are minimized as higher order harmonics can be filtered easily.

The commonly used PWM control techniques are:

(a) Sinusoidal pulse width modulation (sin PWM)

(b) Space vector PWM

The performance of each of these control methods is usually judged based on the following parameters: a) Total harmonic distortion (THD) of the voltage and current at the output of the inverter, b) Switching losses within the inverter, c) Peak-to-peak ripple in the load current, and d) Maximum inverter output voltage for a given DC rail voltage.

From the above all mentioned PWM control methods, the Sinusoidal pulse width modulation (sin PWM) is applied in the proposed inverter since it has various advantages over other techniques. **Sinusoidal PWM inverters provide an easy way to control amplitude, frequency and harmonics contents of the output voltage.**

3.3 PWM MODULATION TECHNIQUE

These are the classical and most widely used methods of pulse width modulation. They have as common characteristic sub cycles of constant time duration, a sub cycle being defined as the total duration ***Ts*** during which an active inverter leg assumes two consecutive switching states of opposite voltage polarity. Operation at sub cycles of constant duration is reflected in the harmonic spectrum by two salient sidebands, centered around the carrier frequency, and additional frequency bands around integral multiples of the carrier.

The multi carrier modulation technique is very suitable for a multilevel inverter circuit. By employing this technique along with the multilevel topology, the low THD output waveform without any filter circuit is possible. Switching devices, in addition, turn on and off only one time per cycle. That can overcome the switching loss problem, as well as EMI problem.

Harmonic analysis of the output modulated voltage wave reveals that SPWM has the following features:

(i) For modulation index less than one, the largest harmonic amplitudes in the output voltage are associated with harmonics of order $2Np\pm1$, where Np is the number of pulses per half-cycle. Thus, by increasing the number of pulses per half-cycle, the order of dominant harmonic frequency can be raised, which can then be filtered out easily. For $Np=5$, harmonics of order of 9 and 11 become significant in the output voltage. It may be noted that the highest order of significant harmonic of modulated voltage wave is centered around the carrier frequency.

(ii) For modulation index greater than one, lower order harmonics appear since for modulation index greater than one, pulse width is no longer a sinusoidal function of the angular position of the pulse.

CHAPTER 4

OPERATING PRINCIPLE OF PROPOSED INVERTER

In recent years multi-level voltage source inverters have become quite popular, mainly due to their capability to increase the output-voltage magnitude and to reduce the output voltage and current harmonic content. Many different strategies for the multi-level pulse-width modulation (PWM) exist. Usually the modulator is chosen to match the hardware topology. However, this choice does not always correspond to the PWM-strategy which generates the least harmonic content. This least- harmonics PWM-strategy can be used for all hardware topologies. It only requires a logic circuit to decode the PWM-output to the individual switch commands. Multilevel voltage-source inverters' unique structure allows them to span high voltages and to reduce individual device switching frequency without the use of transformers. **Multi-level inverters, (including five-level inverters), have significant operational advantage, such as the ability to drive a motor with nearly sinusoidal current waveforms and at higher output voltages.**

4.1 OPERATIONAL PRINCIPLE OF PROPOSED INVERTER

The proposed single-phase five-level inverter involves various steps of operation. The configuration and the principle of operation of the proposed inverter is given below of the proposed single-phase five level inverter.

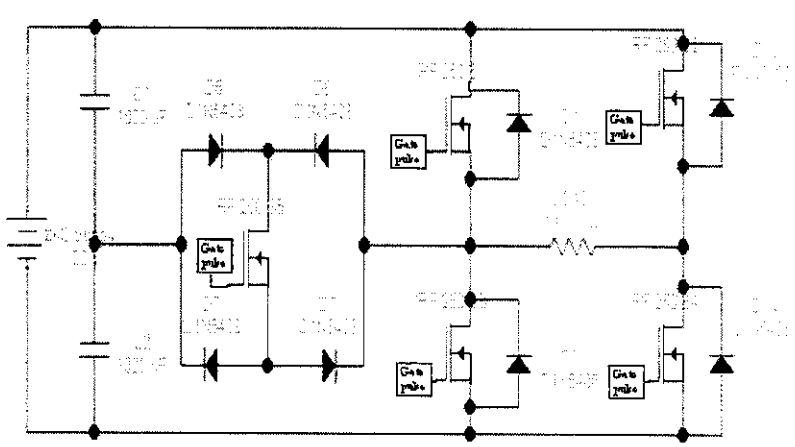


Fig.4.1 single phase five-level inverter

Fig.4.1 shows a configuration of the proposed single-phase five-level inverter. One switching element and four diodes added in the conventional full-bridge inverter are connected to the center-tap of dc power supply. Proper switching control of the auxiliary switch can generate half level of dc supply voltage. The operation of proposed inverter can be divided into 10 switching states as illustrated in Fig.4.2.

4.2 POWER STAGE OPERATION

4.2.1. MAXIMUM POSITIVE OUTPUT (Vs):

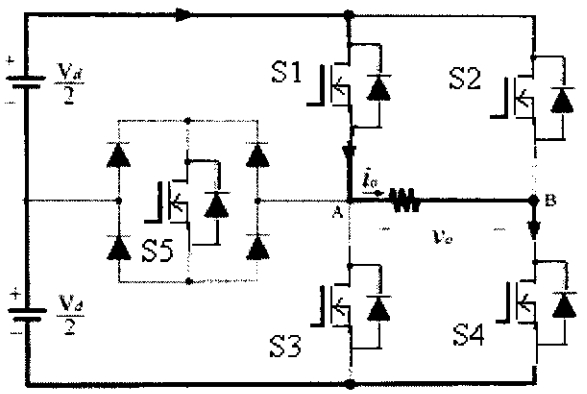


Fig 4.2.a Power flow path to generate Vs voltage (forward direction)

Switch1 is ON, connecting the load positive terminal to Vs, and switch 4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminal is Vs. Fig.4.2.a & Fig 4.2.b shows the current paths that are active at this stage.

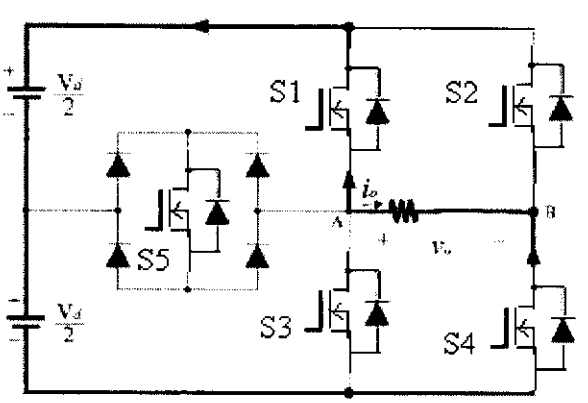


Fig 4.2.b Power flow path to generate Vs voltage (reverse direction)

4.2.2 HALF-LEVEL POSITIVE OUTPUT (Vs/2):

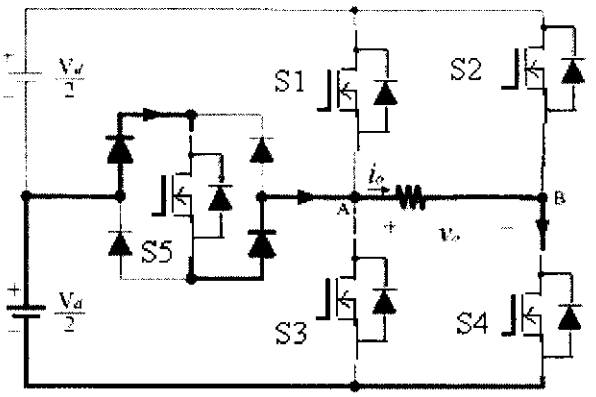


Fig 4.2.c Power flow path to generate Vs/2 voltage (forward direction)

The auxiliary switch, switch 5 is ON, connecting the load positive terminal to point A, through diodes D5 and D8, and switch 4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is Vs/2.Fig.4.2.c & Fig 4.2.d shows the current paths are active at this stage.

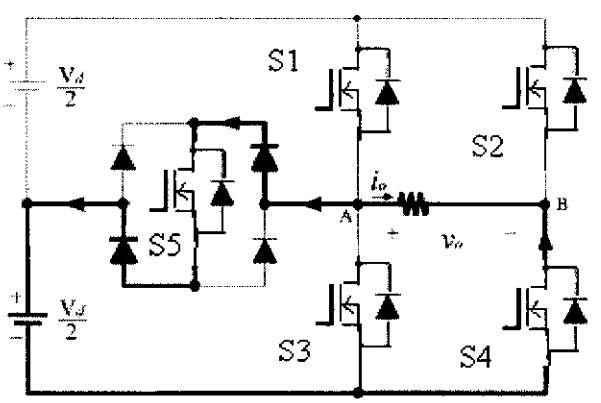


Fig 4.2.d Power flow path to generate Vs/2 voltage (reverse direction)

4.2.3 ZERO OUTPUT VOLTAGE

The two main switches switch3 and switch4 are ON, short-circuiting the load. All other controlled switches are OFF; or the main switches switch1 and switch2 are ON, short-circuiting the load. All other controlled switches are OFF; the voltage applied to the load terminals is zero. Fig.4.2.e & Fig 4.2.f shows the current paths that are active at this stage.

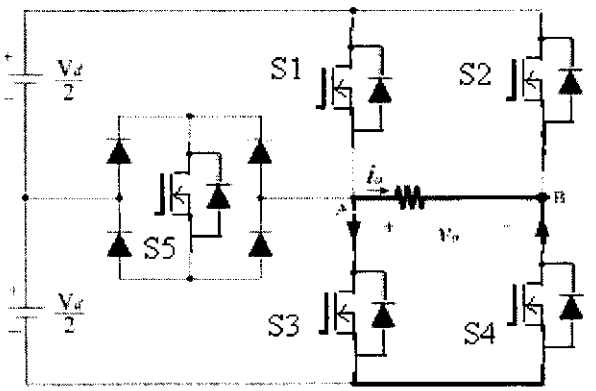


Fig 4.2.e Power flow path to generate Zero voltage (forward direction)

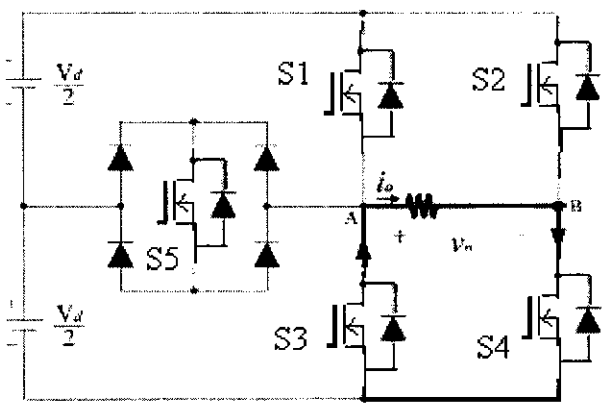


Fig 4.2.f Power flow path to generate Zero voltage (Reverse direction)

4.2.4 HALF – LEVEL NEGATIVE OUTPUT (-Vs/2)

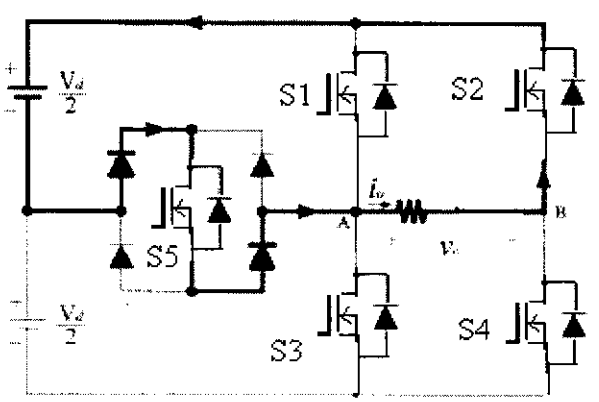


Fig 4.2.g Power flow path to generate –Vs/2 voltage (forward direction)

The auxiliary switch, switch 5 is ON, connecting the load positive terminal to point A, through diodes D6 and D7, and switch 2 is ON, connecting the load negative terminal to Vs. All other controlled switches are OFF; the voltage applied to the load terminals is (-Vs/2).Fig.4.2.g & Fig 4.2.h shows the current paths that are active at this stage.

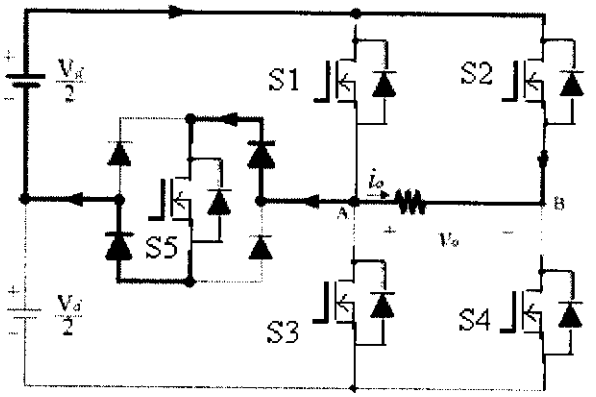


Fig 4.2.h Power flow path to generate –Vs/2 voltage (forward direction)

4.2.5 MAXIMUM NEGATIVE OUTPUT (-Vs)

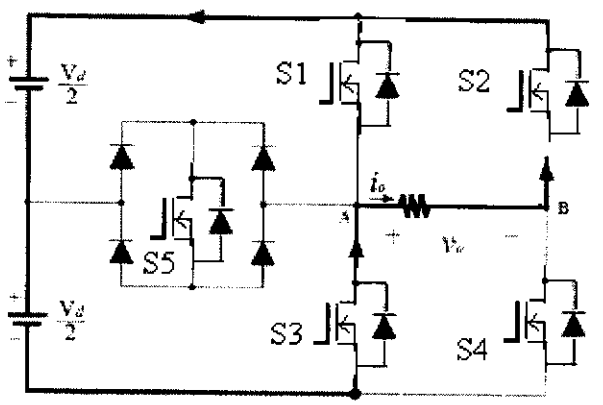


Fig 4.2.i Power flow path to generate –Vs voltage (forward direction)

Switch2 is ON, connecting the load negative terminal to Vs, and switch3 is ON, connecting the load positive terminal to ground. All other controlled switches are OFF; the voltage applied to load terminals is (-Vs).Fig.4.2.i & Fig 4.2.j shows the current paths that are active at this stage.

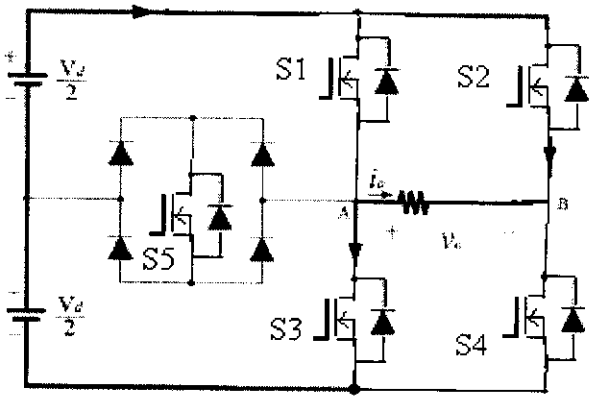


Fig 4.2.j Power flow path to generate –Vs voltage (reverse direction)

Fig.4.2 Operational states according to the switch on off conditions and the direction of load current. (a) State 1: Vo= Vd, Io = (+). (b) State 2: Vo = Vd, Io = (-). (c) State 3: Vo = Vd/2, Io = (+). (d) State 4: Vo = Vd/2, Io = (-). (e) State 5: Vo = 0, Io = (+). (f) State 6: Vo = 0, Io = (-). (g) State 7: Vo = -Vd/2, Io = (+). (h) State 8: Vo = -Vd/2, Io = (-). (i) State 9: Vo= -Vd, Io = (+). (j) State 10: Vo = -Vd, Io = (-).

Operational states of the conventional inverter are shown in Fig.4.2 (a), (b), (e), (f), (i), and (j) in sequence, and additional states in the proposed inverter synthesizing half level of dc bus voltage are shown in Fig.4.2 (c), (d), (g), and (h). The additional switch Q5 must be properly switched considering the direction of load current. The single-phase five-level inverter whose output voltage has five values: zero, half and full supply dc voltage levels (positive and negative, respectively), so called a five-level single-phase inverter.

CHAPTER5

SIMULATION MODEL OF THE PROPOSED INVERTER

5.1 PSIM:

PSIM is simulation software specifically designed for power electronics and motor drives. With fast simulation and friendly user interface, PSIM provides a powerful simulation environment for power electronics, analog and digital control, magnetics, motor drives, and dynamic system studies. In PSIM, the simulation time step is fixed throughout the simulation. In order to ensure accurate simulation results, the time step must be chosen properly. Factors that limit the time step include the switching period, widths of the pulses/waveforms, and intervals of transients. It is recommended that the time step be at least one magnitude smaller.

PSIM includes the following add-on options:

Motor drive module includes built-in electric machine models and mechanical load models for motor drive system studies. Digital control module includes z-domain discrete elements, such as zero-order hold, unit delay, z-domain transfer function blocks, digital filters, for digital control system analysis. Sim coupler module provides the interface for co-simulation between PSIM and Matlab/Simulink. Thermal module provides the capability to calculate semiconductor devices losses.PSIM runs in Microsoft Windows environment (95/98/NT/2000) on PC computers. The minimum RAM memory requirement is 32 MB. The power circuit consists of switching devices, RLC branches, transformers, and coupled inductors. The control circuit is represented in block diagram. Components in s domain and z domain, logic components (such as logic gates and flip flops), and on linear components (such as multipliers and dividers) can be used in the control circuit. Sensors measure power circuit voltages and currents and pass the values to the control circuit.

The simulation model is developed for the proposed inverter using PSIM. The figure below represents the model of the proposed single-phase five-level inverter.

5.2 SIMULATED CIRCUIT

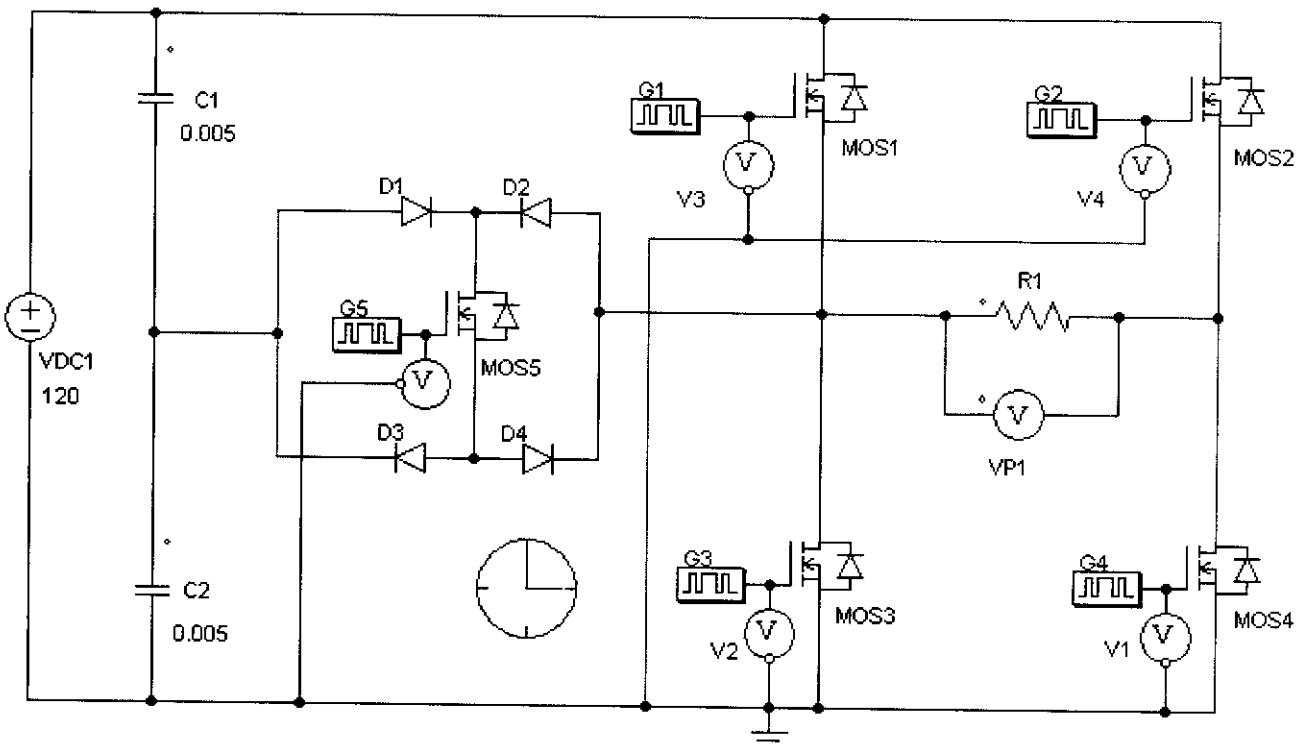


Fig.5.1 simulated model of the single-phase Five-level inverter.

The new topology five-level inverter operation was simulated in PSIM.Fig.8 shows the simulated circuit diagram. It consists of main circuit and sub circuit. The sub circuit (gating circuit) gives the gating signals of all the five switches. Here input supply is Vdc = 120 v .An n-channel MOSFET consists of a transistor in anti-parallel with a diode. It is turned on when the gating is high and the drain-to-source is positively biased. It is turned off when the gating is low or the current drops to zero.

The gate pulse for MOSFET is generated with the help of switch gating block. The switch gating block defines the gating pattern of a switch or a switch module. Each turn-on or turn-off action is counted as one switching point. Electrolytic capacitors have voltage polarity requirement. The positive polarity must be connected to the higher voltage potential, and the negative polarity must be connected to the negative potential. The diode conduction voltage drop is usually around 0.6 to 0.7 V. It may be higher for high power diodes.

5.3 SWITCHING PATTERN

The switching patterns adopted in the proposed inverter are illustrated in Fig.5.2

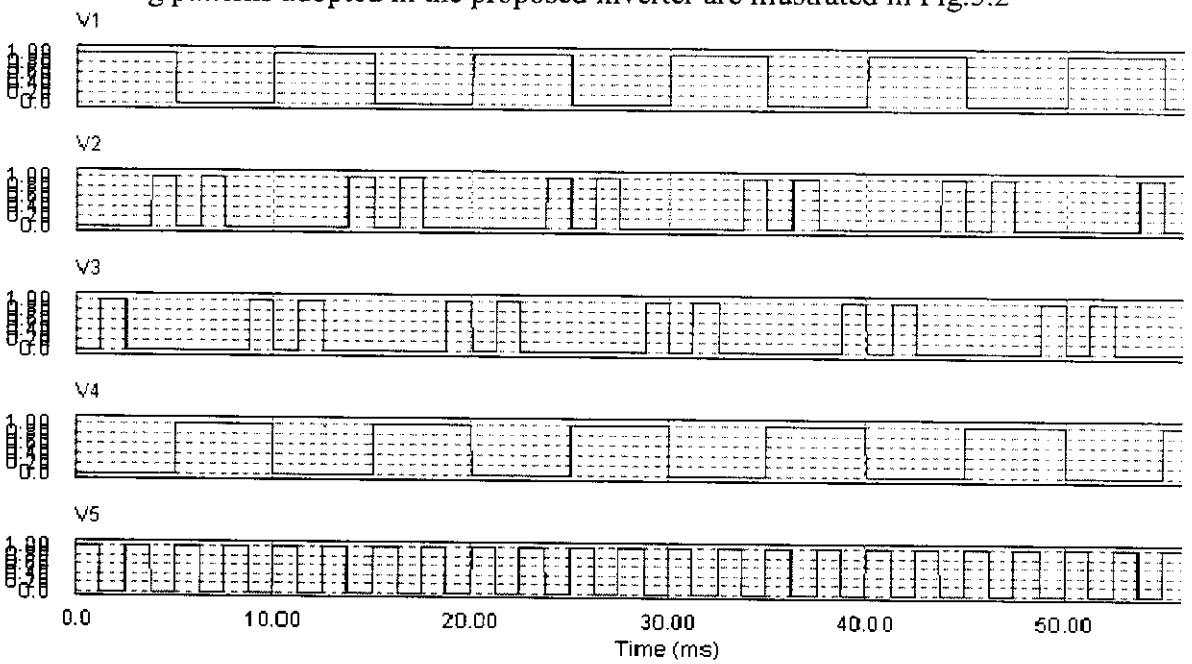


Table 4.1

Output Voltage according to the Switch ON-OFF Conditions

S1	S2	S3	S4	S5	Vo
ON	OFF	OFF	ON	OFF	Vs
OFF	OFF	OFF	ON	ON	Vs/2
OFF	OFF	ON	ON	OFF	0
OFF	ON	OFF	OFF	ON	-Vs/2
ON	OFF	OFF	ON	OFF	Vs

The figure 5.2 given above represents the switching pattern developed for the proposed inverter. The figure represents the pulse for switches 1,2,3,4 and 5 respectively. The switching pattern is developed by the gate blocking for switches for the proposed inverter. The switches are turned on and off according to the gate signals given for the switches. The output voltage according to the switch ON-OFF conditions are given in the Table 4.1

5.4. SIMULATION RESULTS OF PROPOSED INVERTER

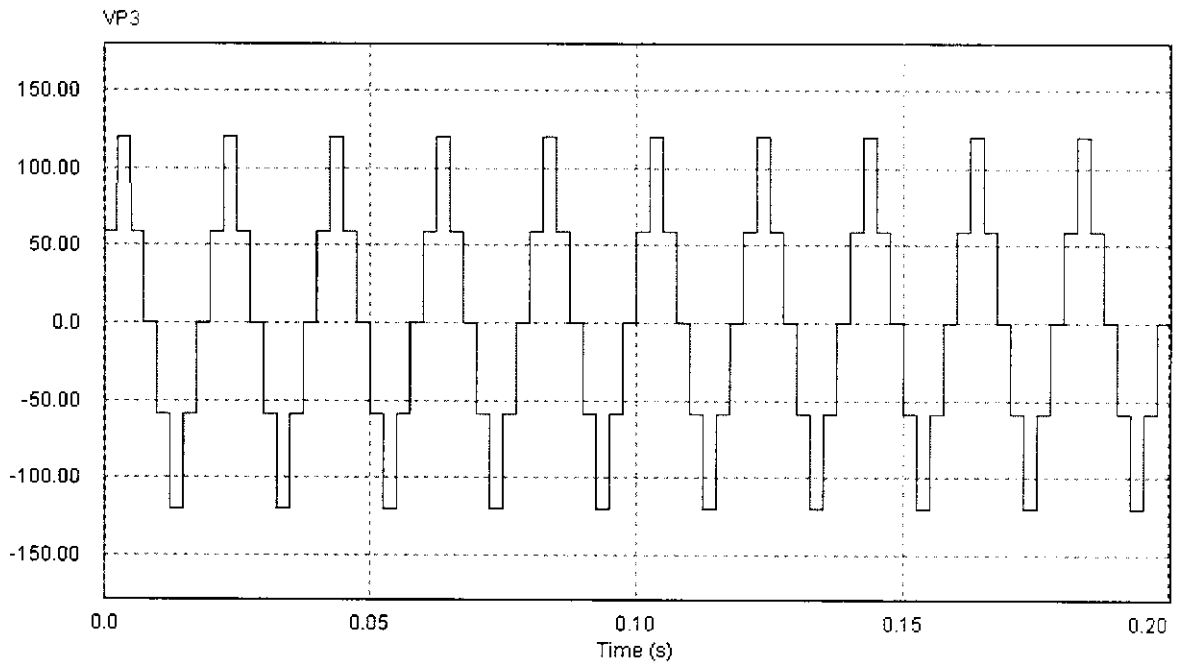


Fig. 5.3. Output voltage of the proposed inverter

The output voltage of the proposed inverter is given above. Here input supply given to inverter circuit is 120v DC.The switching pattern for each switch is discussed above. Here the capacitor value is choosing such that to generate voltage free from ripple, the value of capacitor is 1e-6 farad. Thus here five level voltages are obtained across the load such as (Vs, Vs/2, 0,-Vs/2,-Vs). Shows the simulated output voltage waveform taken from the load terminals. Here in X-axis time period is represented in seconds and in Y-axis amplitude is represented with respect to voltage. It can be seen that the pulse duration is variable, depending on the pulse accelerator. The five voltage levels in the Fig.5.3.are Vs=120V, Vs/2=60v, 0,-Vs/2=-60,-Vs=-120.Fig.11 shows the output voltage frequency spectrum upto 1 KHz.

CHAPTER 6

HARDWARE IMPLEMENTATION

6.1HARDWARE BLOCK DIAGRAM

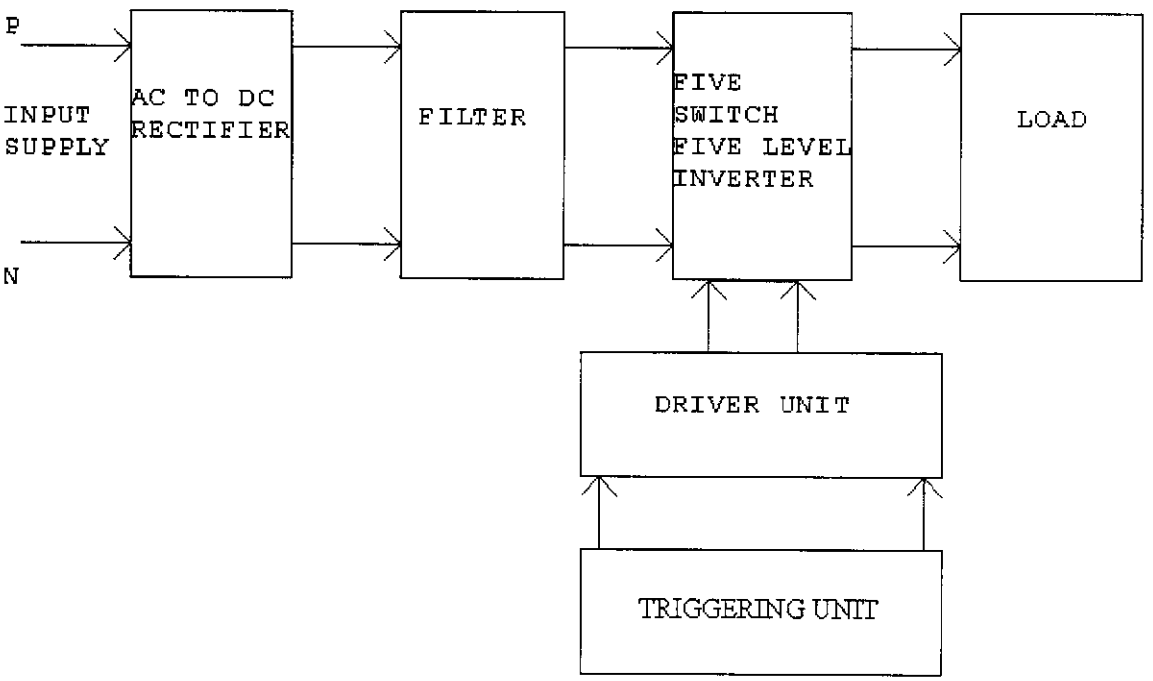


Fig 6.1 Hardware block diagram

The above fig 6.1 shows the block diagram of the proposed inverter. Here it's mainly categories into three units they are triggering circuit unit, driver circuit and power circuit. For every unit input supply may vary according to their nature.

6.2. POWER SUPPLY

All electronic circuits works only in low DC voltage, so we need a power supply unit to provide the appropriate voltage supply for their proper functioning .This unit consists of transformer, rectifier, filter & regulator. AC voltage of typically 230v rms is connected to a transformer voltage down to the level to the desired ac voltage. A diode rectifier that provides the full wave rectified voltage that is initially filtered by a simple capacitor filter to produce a dc voltage. This resulting dc voltage usually has

some ripple or ac voltage variation . A regulator circuit can use this dc input to provide dc voltage that not only has much less ripple voltage but also remains the same dc value even the dc voltage varies some what, or the load connected to the output dc voltages changes.

6.3 DRIVER CIRCUIT OPERATION

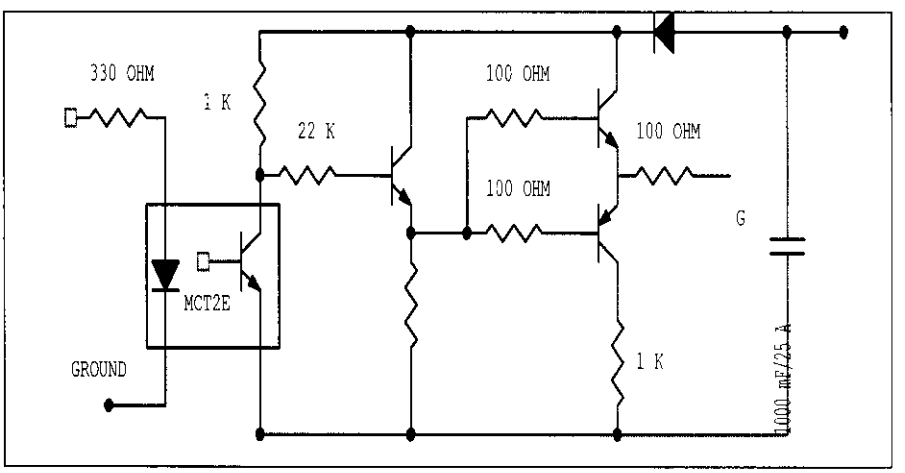


Fig 6.2 Driver circuit

The driver circuit forms the most important part of the hardware unit because it acts as the backbone of the inverter because it gives the triggering pulse to the switches in the proper sequence. The diagram given above gives the circuit operation of the driver unit. The driver unit contains the following important units.

A. Optocoupler
B. Totem pole
C. Capacitor
D. Supply
E. Diode
F. Resistor

The above mentioned components perform certain operation. The Optocoupler provides isolation between the power circuit and triggering circuit. The role of Totem pole is boost the voltage level need for MOSFET gate pulse. The need for capacitor is to provide proper voltage to Darlington pair and for whole drive circuit unit.

6.4 TRIGGERING UNIT: PIC 16F877A MICROCONTROLLER

The microcontroller that has been used for this project is from PIC series. PIC microcontroller is the first RISC based microcontroller fabricated in CMOS (complimentary metal oxide semiconductor) that uses separate bus for instruction and data allowing simultaneous access of program and data memory.

The main advantage of CMOS and RISC combination is low power consumption resulting in a very small chip size with a small pin count. The main advantage of CMOS is that it has immunity to noise than other fabrication techniques.

PIC (16F877): Various microcontrollers offer different kinds of memories. EEPROM, EPROM, FLASH etc. are some of the memories of which FLASH is the most recently developed. Technology that is used in pic16F877 is flash technology, so that data is retained even when the power is switched off. Easy Programming and Erasing are other features of PIC 16F877.

6.4.1. SPECIAL FEATURES OF PIC MICROCONTROLLER:

CORE FEATURES:

- High-performance RISC CPU
- Only 35 single word instructions to learn
- All single cycle instructions except for program branches which are two cycle
- Operating speed:
    - ✓ DC - 20 MHz clock input
    - ✓ DC - 200 ns instruction cycle
- Up to 8K x 14 words of Flash Program Memory,
- Up to 368 x 8 bytes of Data Memory (RAM)
- Up to 256 x 8 bytes of EEPROM data memory
- Pin out compatible to the PIC16C73/74/76/77
- Interrupt capability (up to 14 internal/external
- Eight level deep hardware stack
- Direct, indirect, and relative addressing modes
- Power-on Reset (POR)

- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC Oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options
- Low-power, high-speed CMOS EPROM/EEPROM technology
- Fully static design
- In-Circuit Serial Programming (ICSP) via two pins
- Only single 5V source needed for programming capability
- In-Circuit Debugging via two pins
- Processor read/write access to program memory
- Wide operating voltage range: 2.5V to 5.5V
- High Sink/Source Current: 25 mA
- Commercial and Industrial temperature ranges
- Low-power consumption:
    - ✓ < 2mA typical @ 5V, 4 MHz
    - ✓ < 20mA typical @ 3V, 32 kHz
    - ✓ < 1mA typical standby current

PERIPHERAL FEATURES:

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler, can be incremented during sleep via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules
    - ✓ Capture is 16-bit, max resolution is 12.5 ns,
    - ✓ Compare is 16-bit, max resolution is 200 ns,
    - ✓ PWM max. resolution is 10-bit
- 10-bit multi-channel Analog-to-Digital converter
- Synchronous Serial Port (SSP) with SPI. (Master Mode) and I2C. (Master/Slave)
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with
- 9- bit addresses detection.
- Brown-out detection circuitry **for Brown-out Reset (BOR)**

6.4.2. PIN DIAGRAM OF PIC 16F877A:

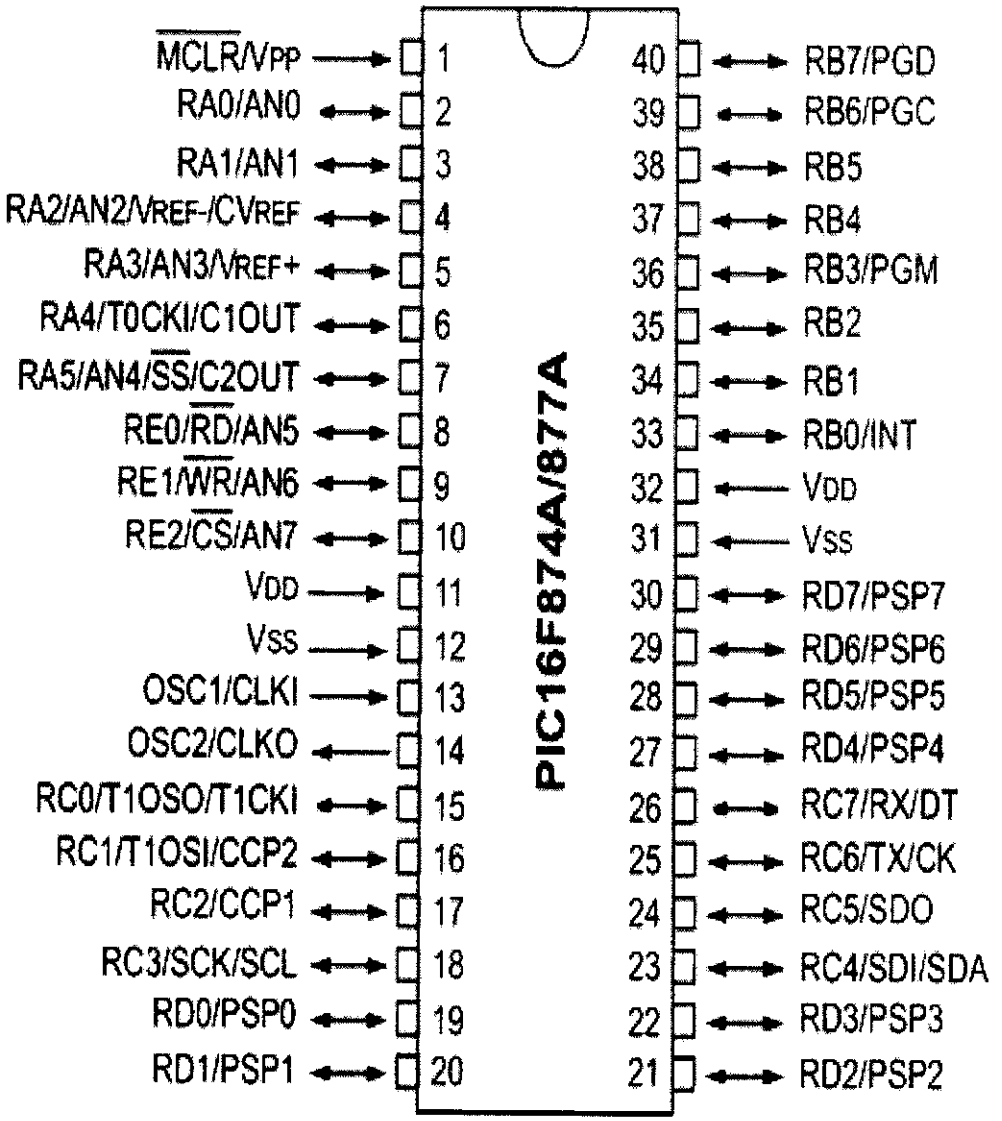


Fig 6.3 Pin diagram of PIC16F877A

- It has on chip Timers. There are 3 Timers for usage
- It has in built Analog to Digital Converter
- In built Multiplexer availability for signal Selection
- It has serial as well as Parallel Communication facilities
- In built Capture, Compare and Pulse width modulation
- It has 5 Ports for Internal and External usage

6.4.3 TRIGGERING CIRCUIT:

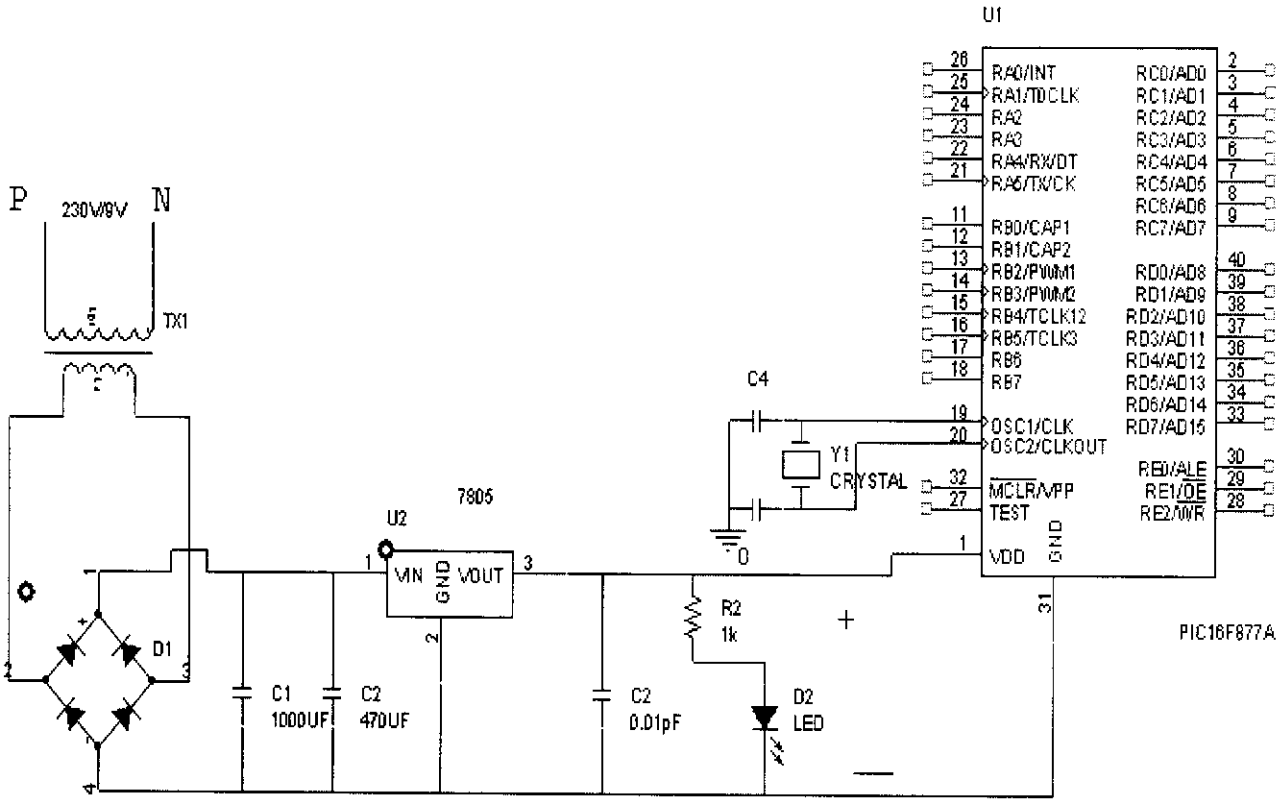


Fig 6.4 Triggering circuit.

6.5. SOFTWARE USED

6.5.1 PIC 'C' COMPILER

The programming for the microcontroller 16F877 is done by using this software. In this programming is prepared in 'c' language and then converted to hex file. Thus the developed program is converted to hex file with help MP LAB device tool.

6.5.2 MPLAB Integrated Development Environment (IDE)

MPLAB Integrated Development Environment (IDE) is a free, integrated toolset for the development of embedded applications employing Microchip's PIC® and dsPIC® microcontrollers. MPLAB IDE runs as a 32-bit application on MS Windows®, is easy to use and includes a host of free software components for fast application development and super-charged debugging.

6.5.3WINPIC800:

This software is used to embedded program into the microcontroller. Initially program is loaded into the software and transferred to microcontroller by using a specialized interfacing circuit. Here hex file format is converted to some voltage and finally loaded into IC.

6.6 HARDWARE SETUP

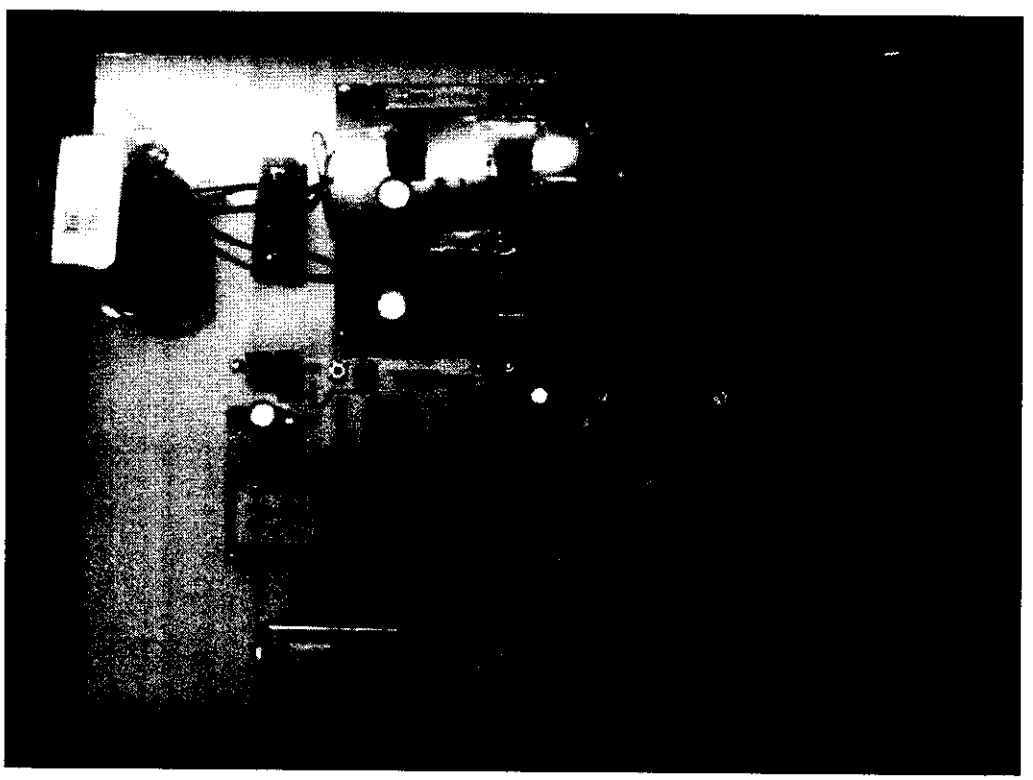


Fig 6.5 Hardware set up for five level multilevel inverter

The Step down transformer (230/24V) is used to give supply to the power circuit. The step down transformer (230/12V) is used to give supply to the triggering circuit and driver circuit. The gate pulse for MOSFET is generated using PIC Microcontroller. The output voltage of the microcontroller is 5V which is not sufficient to drive MOSFET and therefore driver circuit and output waveform is viewed in CRO.

6.7 CRO OUTPUT WAVEFORM FOR FIVE-LEVEL INVERTER

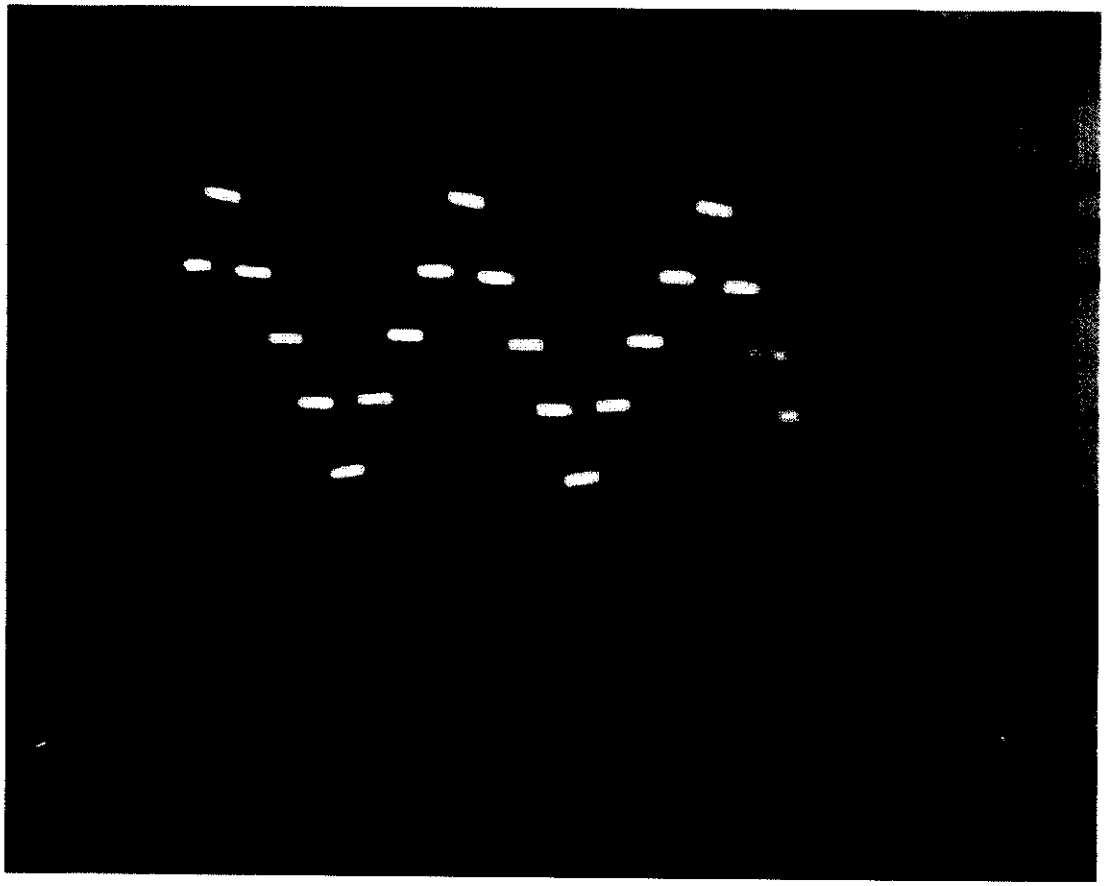
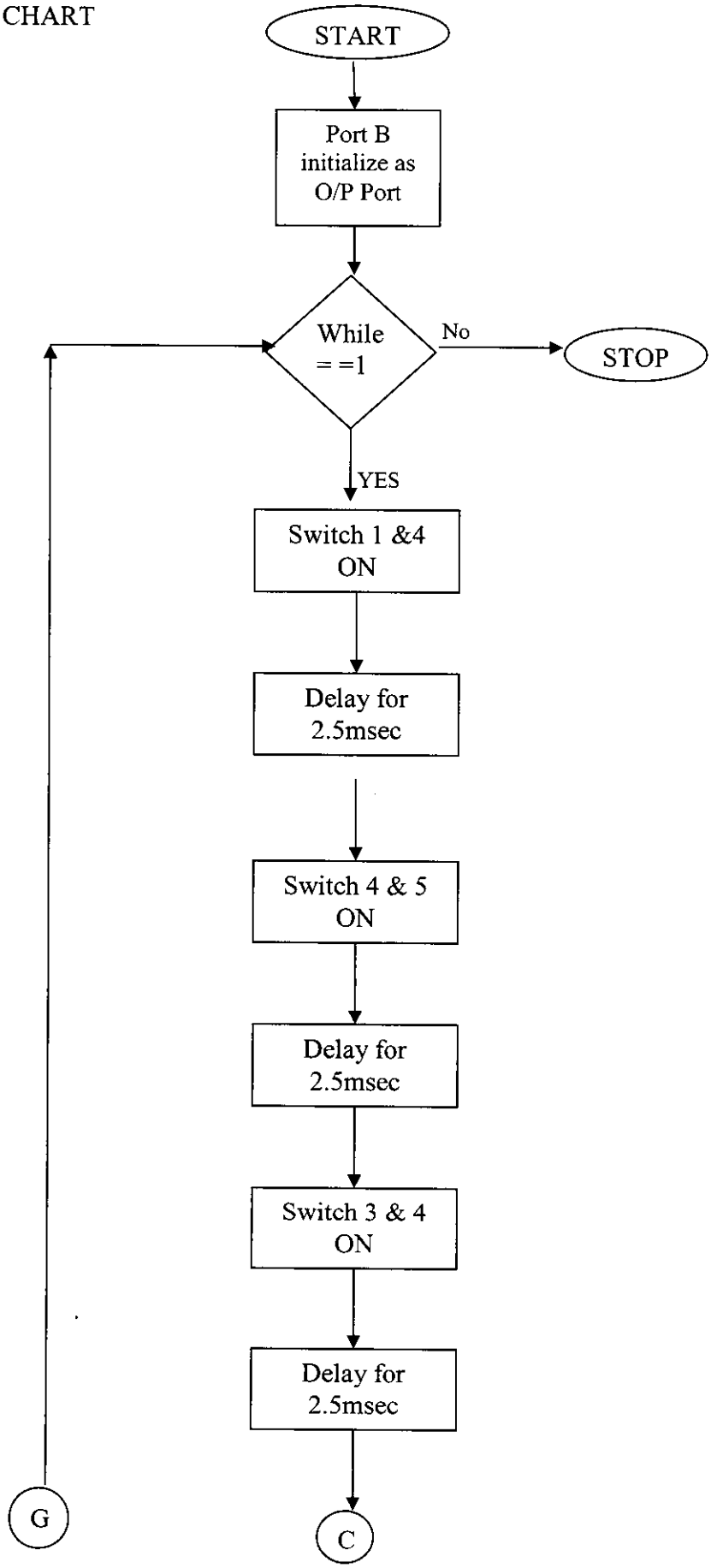
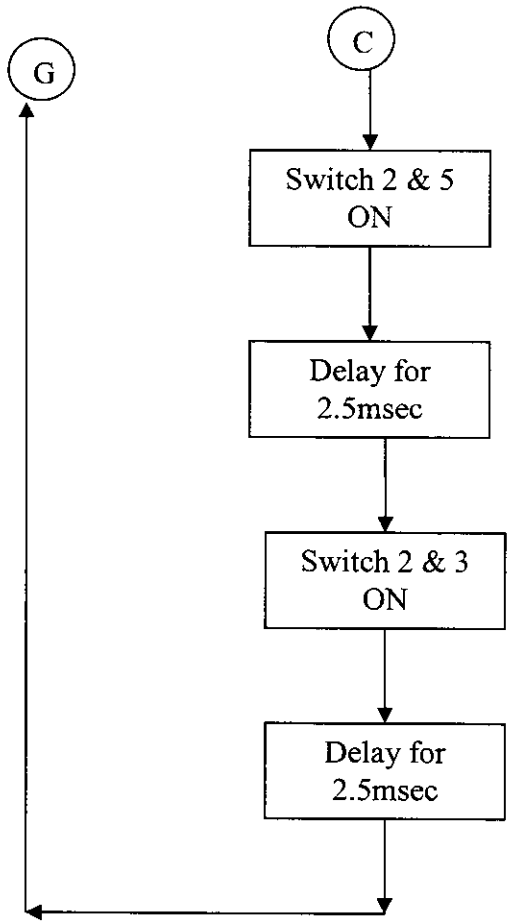


Fig 6.6 CRO output waveform for five level multilevel inverter

The above presents the output voltage waveform showing the desired five voltage levels. The five output voltage levels are Vs=120V,Vs/2=60 V, 0 V,-Vs/2 =60 V,-Vs=120 V.Here the waveform is measured across the load

6.8 FLOW CHART





- Gate pulse for MOSFET1 is generated in PORT B (Pb0)
- Gate pulse for MOSFET2 is generated in PORT B (Pb1)
- Gate pulse for MOSFET3 is generated in PORT B (Pb2)
- Gate pulse for MOSFET4 is generated in PORT B (Pb3)
- Gate pulse for MOSFET5 is generated in PORT B (Pb4)

6.9 SOFTWARE CODING

```
#include<pic.h>                    //PIC16F Header File Declaration
#include<stdio.h>                  //Embedded C Header File Declaration
#include "delay"                   //Subroutine Declaration
__CONFIG (0x3f71);                 //IC Initialization
Void main ()                       //Main Program
{
        TRISB=0x00;                //port B assign as a output port
        PORTB=0;                   //Clear PORT B
        While (1)                  // Continuous Operation
        {
                PORTB=0xcc;        //Generate first part signal     1
                DelayMs (2);       //Call Delay
                DelayUs (500);
                PORTB=0x39;        //Generate Second Part Signal    2
                DelayMs (2);       //Call Delay
                DelayUs (500);
                PORTB=0x99;        //Generate first part signal     3
                DelayMs (2);       //Call Delay
                DelayUs (500);
                PORTB=0x39;        //Generate first part signal     4
                DelayMs (2);       //Call Delay
                DelayUs (500);
                PORTB=0xcc;        //Generate first part signal     5
                DelayMs (2);       //Call Delay
                DelayUs (500);
                }
        }
```

CHAPTER 7

CONCLUSION

This project deals with the design and implementation of single-phase five-level multilevel inverter. Simulated results show the new multilevel topology with the bidirectional auxiliary switch works as expected, generating the required five-level output using only five power switches, and only one center tap provided by two capacitors. There are many multilevel inverters developed according to the voltage levels required. The operational and the switching functions are analyzed in detail. The simulation results shows that the developed five-level inverter has many merits such as reduce number of switches, lower EMI, less harmonic distortion. Here Simulation result is compared with Hardware result. Thus proposed inverter involves many advantages over the conventional inverter. The study can further be investigated by employing control schemes to have higher dynamic responses and by using higher level inverters.

REFERENCES

1. Gerardo Celiga,Victor Member,IEEE,Carlos Sanchez, Fernando Ibanez, Julio Walter, and Maria I.Gimenez,Member,IEEE, "A New Simplified Multilevel Inverter Topology for DC-AC Conversation" ,Power Electronics,IEEE Transactions volume No:5;Issue Month: Sep;Issue Year:2006.

2. J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multi-level inverter: a survey of topologies, controls, and applications," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, Aug. 2002.

3. M. Marchesoni and P. Tensa, "Diode-clamped multilevel converters: a practicable way to balance DC-link voltages," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 752–765, Aug. 2002.

4. Y. Chen, B. Mwinyiwiwa, Z.Wolanski, and B.-T. Ooi, "Unified Power Flow Controller (UPFC) based on chopper stabilized diode-clamped multilevel converters," IEEE Trans. Power Electron., vol. 15, no. 2, pp.258–267, Mar. 2000.

5. N. P. Schibli, T. Nguyen, and A. C. Rufer, "A three-phase multilevel Converter for high-power induction motors," IEEE Trans. Power. Electron. vol. 13, no. 5, pp. 978–986, Sep. 1998.

6. Y. Cheng and M. L. Crow, "A Diode-Clamped Multi-Level Inverter for the StatCom/BESS," in Proc. IEEE PESWinter Meeting, Jan. 2002, vol. 1, pp. 470–475.

7. John B.Peatman, "Design with PIC Microcontroller", Pearson Education Asia, third Indian reprint prentice hall of India, 2002.

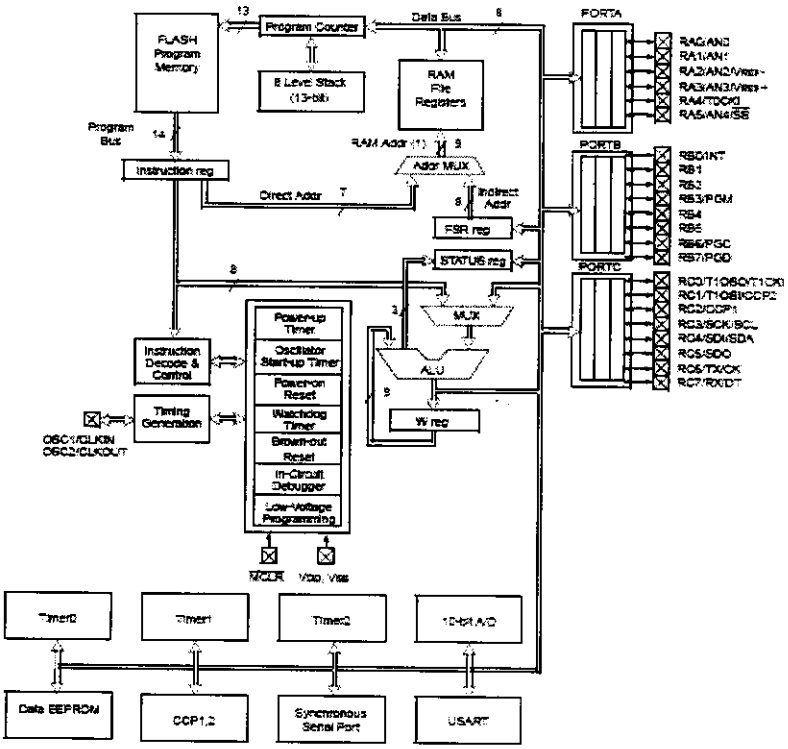
8. www.alldatasheet.com

9. www.PICmicrocontroller.com

APPENDIX
PIC 16F877A

ARCHITECTURE OF PIC 16F877A:

Device	Program FLASH	Data Memory	Data EEPROM
PIC16F873	4K	192 Bytes	128 Bytes
PIC16F876	8K	368 Bytes	256 Bytes



TIMER 0 CONTROL REGISTER:

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

bit 7: **RBPU**
bit 6: **INTEDG**
bit 5: **T0CS**: TMR0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)
bit 4: **T0SE**: TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

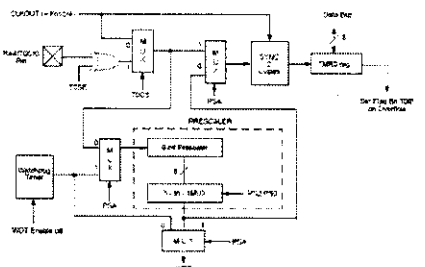
bit 3: **PSA**: Prescaler Assignment bit

1 = Prescaler is assigned to the WDT

0 = Prescaler is assigned to the Timer0 module

bit 2-0: **PS2 PS1 PS0**: Prescaler Rate Select bits

TIMER 0 BLOCK DIAGRAM:



TIMER 1 CONTROL REGISTER:

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON
bit7							bit0

bit 7-6: **Unimplemented:** Read as '0'

bit 5-4: **T1CKPS1:T1CKPS0**: Timer1 Input Clock Prescale Select bits

11 = 1:8 Prescale value

10 = 1:4 Prescale value

01 = 1:2 Prescale value

00 = 1:1 Prescale value

bit 3: **T1OSCEN**: Timer1 Oscillator Enable Control bit

1 = Oscillator is enabled

0 = Oscillator is shut off (The oscillator inverter is turned off to eliminate power drain)

bit 2: **T1SYNC**: Timer1 External Clock Input Synchronization Control bit

TMR1CS = 1

1 = Do not synchronize external clock input

0 = Synchronize external clock input

TMR1CS = 0

This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.

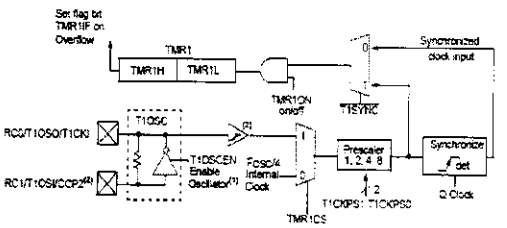
bit 1: **TMR1CS**: Timer1 Clock Source Select bit

1 = External clock from pin RC0/T1OSO/T1CKI (on the rising edge)

0 = Internal clock (FOSC/4)

bit 0: **TMR1ON**: Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1

TIMER 1 BLOCK DIAGRAM:

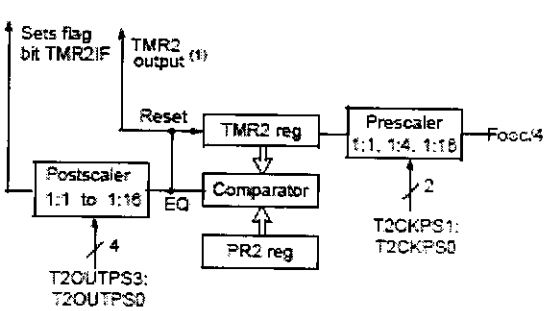


TIMER 2 CONTROL REGISTER:

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit7							bit0

bit 7: **Unimplemented:** Read as '0'
bit 6-3: **TOUTPS3:TOUTPS0**: Timer2 Output Postscale Select bits
0000 = 1:1 Postscale
0001 = 1:2 Postscale
0010 = 1:3 Postscale
1111 = 1:16 Postscale
bit 2: **TMR2ON**: Timer2 On bit
1 = Timer2 is on
0 = Timer2 is off
bit 1-0: **T2CKPS1:T2CKPS0**: Timer2 Clock Prescale Select bits
00 = Prescaler is 1
01 = Prescaler is 4
1x = Prescaler is 16

TIMER2 BLOCK DIAGRAM:

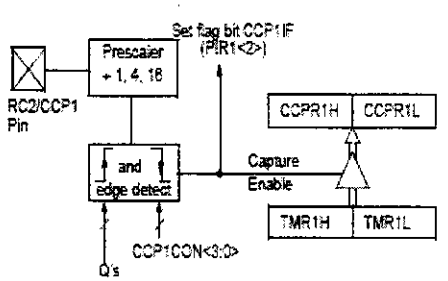


CCP1CON REGISTER/CCP2CON REGISTER:

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CCPxX	CCPxY	CCPxM3	CCPxM2	CCPxM1	CCPxM0
bit7							bit0

bit 7-6: **Unimplemented:** Read as '0'
bit 5-4: **CCPxX :CCPxY**: PWM Least Significant bits
Capture Mode: Unused
Compare Mode: Unused
PWM Mode: These bits are the two LSB s of the PWM duty cycle. The eight MSB s are found in CCPRxL.
bit 3-0: **CCPxM3:CCPxM0**: CCPx Mode Select bits
0000 = Capture/Compare/PWM off (resets CCPx module)
0100 = Capture mode, every falling edge
0101 = Capture mode, every rising edge
0110 = Capture mode, every 4th rising edge
0111 = Capture mode, every 16th rising edge
1000 = Compare mode, set output on match (CCPxIF bit is set)
1001 = Compare mode, clear output on match (CCPxIF bit is set)
1010 = Compare mode, generate software interrupt on match (CCPxIF bit is set, CCPx pin is unaffected)
1011 = Compare mode, trigger special event (CCPxIF bit is set, CCPx pin is unaffected); CCP1 resets TMR1; CCP2 resets TMR1 and starts an A/D conversion (if A/D module is enabled)
11xx = PWM mode

CAPTURE MODE OPERATION BLOCK DIAGRAM:



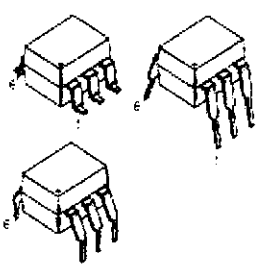
APPENDIX B
MCT2E OPTOISOLATOR

FAIRCHILD
SEMICONDUCTOR®

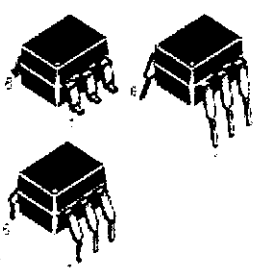
PHOTOTRANSISTOR OPTOCOUPLERS

MCT2	MCT2E	MCT210	MCT271
MCT2200	MCT2201	MCT2202	

WHITE PACKAGE (-M SUFFIX)



BLACK PACKAGE (NO -M SUFFIX)



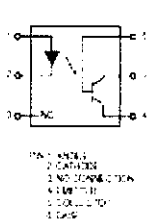
DESCRIPTION

The MCT2XXX series optoisolators consist of a gallium arsenide infrared emitting diode driving a silicon phototransistor in a 6-pin dual in-line package.

FEATURES

- UL recognized (File # E90700)
- VDE recognized (File # 94766)
  - -Add option V for white package (e.g., MCT2V-M)
  - -Add option 300 for black package (e.g., MCT2.300)
- MCT2 and MCT2E are also available in white package by specifying -M suffix, eg. MCT2-M

SCHEMATIC



APPLICATIONS

- Power supply regulators
- Digital logic inputs
- Microprocessor inputs

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Device	Value	Units
TOTAL DEVICE				
Storage Temperature	T_{STG}	ALL	-55 to +150	°C
Operating Temperature	T_{OPR}	ALL	-55 to +100	°C
Lead Solder Temperature	T_{SOL}	ALL	260 for 10 sec	°C
Total Device Power Dissipation @ T_A = 25°C	P_D	-M	250	mW
		Non-M	260	
Derate above 25°C		-M	2.94	mW/°C
		Non-M	3.3	
EMITTER				
DC/Average Forward Input Current	I_F	-M	60	mA
		Non-M	100	
Reverse Input Voltage	V_R	ALL	3	V
Forward Current - Peak (300µs, 2% Duty Cycle)	I_F(pk)	ALL	3	A
LED Power Dissipation @ T_A = 25°C	P_D	-M	120	mW
		Non-M	150	
Derate above 25°C		-M	1.41	mW/°C
		Non-M	2.0	
DETECTOR				
Collector Current	I_C	ALL	50	mA
Collector-Emitter Voltage	V_{CEO}	ALL	30	V
Detector Power Dissipation @ T_A = 25°C	P_D	ALL	150	mW
Derate above 25°C		-M	1.76	mW/°C
		Non-M	2.0	